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## Design and Optimization of Superjunction Vertical DMOS Power Transistors using Sentaurus Device Simulation

Raul Mendoza Macias  
*University of Central Florida*



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DESIGN AND OPTIMIZATION OF SUPERJUNCTION  
VERTICAL DMOS POWER TRANSISTORS  
USING SENTAURUS DEVICE SIMULATION

by

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B.S. Escuela Superior Politécnica del Litoral, 2012

A thesis submitted in partial fulfillment of the requirements  
for the degree of Master of Science  
in the Department of Electrical & Computer Engineering  
in the College of Engineering and Computer Science  
at the University of Central Florida  
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## **ABSTRACT**

Vertical double-diffused metal oxide semiconductor (VDMOS) power transistor has been studied. The use of superjunction (SJ) in the drift region of VDMOS has been evaluated using three-dimensional device simulation. All relevant physical models in Sentaurus are turned on. The VDMOS device doping profile is obtained from process simulation. The superjunction VDMOS performance in off-state breakdown voltage and specific on-resistance is compared with that in conventional VDMOS structure. In addition, electrical parameters such as threshold voltage and charge balance are also examined. Increasing the superjunction doping in the drift region of VDMOS reduces the on-resistance by 26%, while maintaining the same breakdown voltage and threshold voltage compared to that of the conventional VDMOS power transistor with similar device design without using a superjunction.

To my parents and family for their continuous guidance and support, and for everyone else who accompany me along this journey.

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## CHAPTER 1: INTRODUCTION

As the focus of this thesis being the analysis and optimization of the transistor known as VDMOS (Vertical double-diffuse metal oxide semiconductor). First, it will be specified what is the main purpose or area of application of this transistor. This is where power electronics comes in as one of the major uses for the VDMOS transistor. Therefore, to begin with, it should be clear what is power electronics and why it is important.

### 1.1 Power Electronics Fundamentals

Even though power electronics is widely used in current technology, there is actually no single definition for it. Power electronics is in fact a field that is used in a variety of applications [1]. Since it has a multidisciplinary nature, knowledge from many of the electrical engineering topics is required such as: electronic devices, power, electronic circuits, signal processing, electrical machines, and control. In a few words, power electronics is the circuit that changes one type of energy coming from the source to another one that is needed in the load. Therefore, power electronics can be summarized as the combination of three electrical engineering fields: power, electronics, and control. The interaction of these three electrical engineering fields are illustrated in Fig. 1.

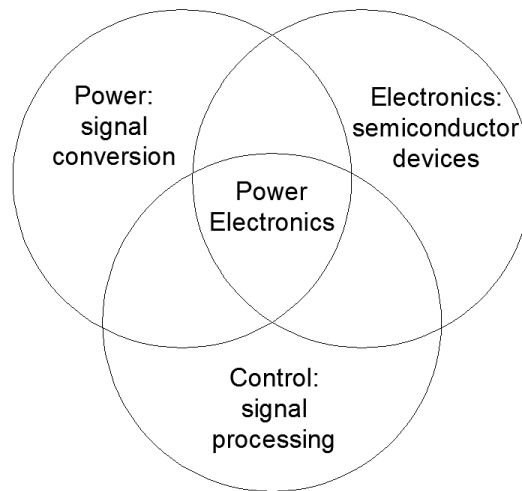


Figure 1: Power Electronics as the combination of three electrical engineering fields.

These three electrical fields deal with different objectives within power electronics. The control area is used to obtain steady state signal stability for the closed loop system. The electronics area is present within the semiconductor devices that are the ones forming the circuits for signal processing and conversion. The power area is the one dealing with static and rotating machinery to obtain signal conversion. Thus, it can be said that power electronics is the use of power semiconductor devices and circuits for the control and conversion of electrical energy.

One integral part of power electronics is that it involves switching devices. It should be cleared out that two types of switching are implicated. One of them is used in the high power circuits handling up to hundreds of gigawatts depending on the application. The other type is used in the low power circuits handling up to hundreds of milliwatts for the feedback control. Consequently, power electronics circuits are in fact switching circuits, which components or transistors work with power from milliwatts to gigawatts. This thesis focuses on the semiconductor devices portion of the power electronics field, studying specifically the switching transistor known as VDMOS.

## 1.2 The VDMOS Transistor

VDMOS is one of the most commonly used field effect transistors in high voltage devices. Its structure is similar to a conventional MOS transistor except for two specifications. The first one is that the drain contact is located at the bottom of the device. The second one is that it has an area known as drift region above the body/substrate of the device. Fig. 2 shows the VDMOS device structure.

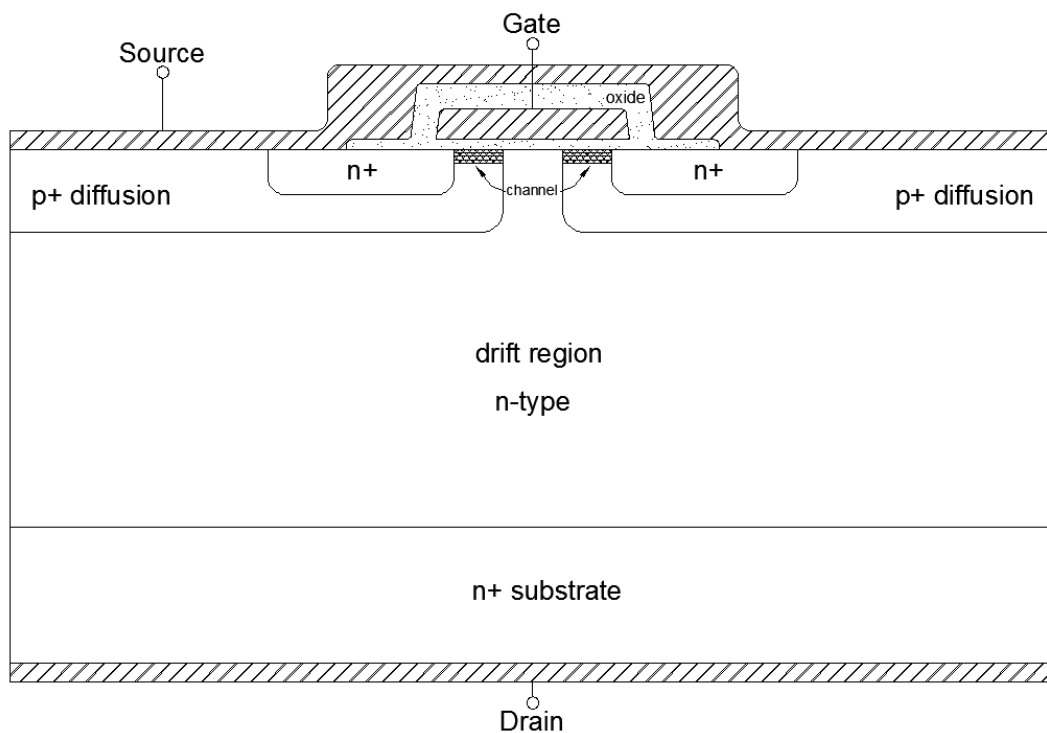


Figure 2: VDMOS device structure, showing its source, gate, drain contacts, channel and drift-region location.

One of the main purposes of VDMOS transistors is to be used as a high power transistor [2]. This translates into switching and rectifying applications. Looking at the transistor as an ideal switching device, it can be said that when the switch is open the contacts are not connected and there is no electrical current passing through. On the other hand, when the switch is closed the contacts are connected and there should be current flow without losses. In reality, non-idealities have to be considered, thus some



issues come into account for the solid-state device. When the switch is open there is actually leakage current present flowing through. In addition, at high voltages, breakdown will follow, which means high current passing through the device. When the switch is closed, resistive losses will be present in the semiconductor material. Therefore, there are two important parameters to be adjusted besides minimizing the leakage current when the device is off. These are the breakdown voltage ( $V_{BR}$ ) and the on-resistance ( $R_{on}$ ). The breakdown voltage should be sufficiently high for the application in which the transistor is going to be used, and the on-resistance should be as small as possible to reduce power losses.

There is in fact a trade-off when adjusting the breakdown voltage and the on-resistance. That is, when increasing the breakdown voltage the on-resistance also increases and vice versa. This implies that in order to optimize the device, one of them is adjusted to a desired point of operation and the other one follows. This is significant since high power MOS devices already have relatively high on-resistance.

In addition, the word vertical in VDMOS devices comes from the fact that the current flows from the top to the bottom of the wafer, and double-diffuse comes from the need of a double diffusion in the fabrication process to build the device channel. As the whole silicon substrate is used for the device, high resistivity is introduced in the current path, which also allows the device to support high voltages. The problem comes for medium to high voltage applications where the losses due to the substrate resistance become relevant. To solve this kind of issues, an alternate device called LDMOS with the RESURF technique can be studied.

### 1.3 History

As years go by, new ideas and better technology is found that replaces the current one with improved characteristics. Looking back at 1970s, silicon bipolar transistors were the dominant devices in terms of power technology [3, 4, 5]. These transistors provided a solution that was cost and robust adequate for the time. Characteristics like desired gain, efficiency, and power were achieved with bipolar transistors, although power gain and thermal issues like negative temperature coefficient producing thermal runaway were actually some of its weakness; besides the need of more linear and energy efficient devices when scaling the device. These bipolar transistor limitations were responsible for looking into an alternative device that could offer a greater performance.

During the early 1980s, the double diffused MOS (DMOS) transistor was discovered [6, 7]. These devices showed improved characteristics over the bipolar transistor. Among them, a better frequency response due to the use of majority carrier transport compared to minority carrier transport in bipolar transistors. High breakdown voltage can also be achieved and designed without affecting the frequency response, which implies the power supply voltage could be increased. Additionally, these MOS devices possess positive thermal resistance coefficient, which prevents thermal runaway contrary to bipolar transistors.

DMOS technology was then classified in two groups depending on the current flow direction. These are the structure known as Lateral DMOS (LDMOS) and the one known as Vertical DMOS (VDMOS) [8]. For both devices, the channel region doping profile is formed by the addition of lateral diffusion processes. Besides this, each device has their own advantages and disadvantages. LDMOS devices keep the drain

region and current flow as the name states laterally close to the surface. By keeping the drain there, it is easier to adjust and design it, thus allowing to obtain linear efficiency and a high frequency operation. Instead, VDMOS keeps the drain region and current flow vertically beneath the surface. This structure allows to obtain optimal power density which translates into low  $R_{ds(on)}/area$ , but it is not so good at high frequencies.

#### 1.4 Applications

The continuous look for power handling devices and radio frequency needs led to further research for power MOSFETs. Thus, the eventual discovery of VDMOS satisfied the necessity in power and RF applications. Nowadays, VDMOS can be found in a variety of different circuits [9] like switching power supplies, motor drivers, DC/DC converters, automotive electronics, voltage regulator modules, and many more. Plenty of research showing VDMOS for power and RF applications can be seen in [10, 11, 12, 13, 14].

Additionally, contrary to LDMOS, which is still under simulation and research study, VDMOS is actually commercially available. It is fabricated with the improved structure known as superjunction. Among them, The VDMOS can be found in the market under different names like CoolMOS [15, 16], STM [17, 18], VTR-DMOS [19], PFVDMOS [20], etc. One of the main concerns during fabrication is the interdiffusion of the p-n pillars in the superjunction structure; this issue comes from the thermal process involved in the fabrication process, which represents problems when trying to achieve charge balance. CoolMOS was the first one commercially available being able to work on the 600 V point of operation.

This thesis is split into four chapters. The first one currently explored was about VDMOS introduction and its applications. The second chapter is about the VDMOS physics and its parameters. The third chapter is about the superjunction structure and fabrication. The fourth and final chapter is about analysis results and conclusions.

## CHAPTER 2: VDMOS BACKGROUND THEORY

As the VDMOS transistor is analyzed, a look into the device properties and physics is needed. That is the reason why this chapter focuses on how a typical VDMOS transistor works, what differentiates it from a regular MOS transistor, and what are the physical phenomena that control its behavior.

The purpose of the drift region is to create a voltage variable resistor so that there would be a voltage drop in the drain region. This would allow for the voltage reaching the gate to be considerably less than the one applied on the drain contact. In the end, the gate oxide is preserved and hot carrier injection is minimized.

The depletion region located along the lightly doped drain n-drift region and the epitaxial layer surrounding is the one that expands and depletes free carriers with the increasing drain voltage. By adjusting the depth and the doping of both the epitaxial layer and the n-drift region, the peak electric field can be controlled such that it will not exceed its critical value. In this way, the avalanche breakdown can be prevented when the drain voltage is applied. Fig. 3 shows how the depletion region typically appears in a p-n junction.

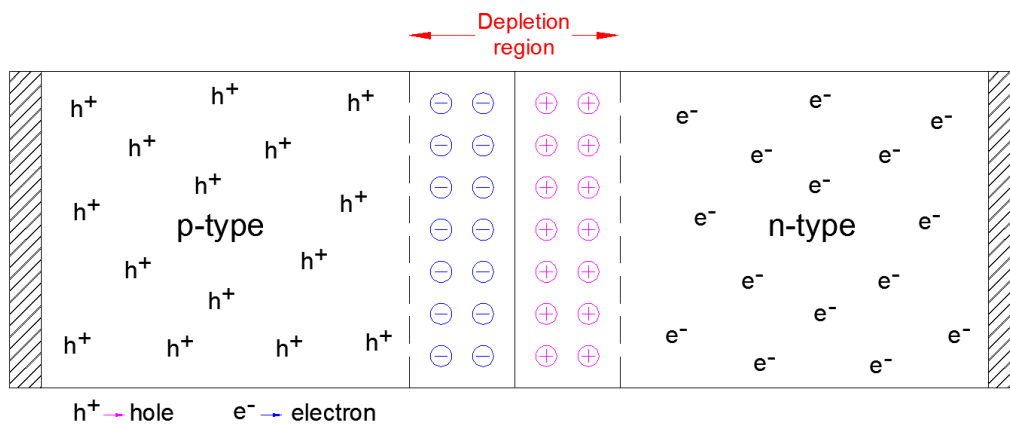


Figure 3: P-n junction structure showing its depletion region.

This resistance created along the drift region represents one of the biggest portion in the transistor. It directly influences the magnitude of the drain saturation current and hence the power of the transistor. One of the goals in designing the transistors is to maintain a low resistance while having a suitable breakdown voltage. The fact that they are related leads to a tradeoff between these two parameters to achieve the best point of operation. This is why the drain structure is the main concern when optimizing the device. In addition, the epitaxial layer plays an important role when adjusting the drain to source capacitance,  $C_{DS}$ . This capacitance optimization can lead to good results in terms of high frequency performance.

When building the channel in the VDMOS, it is done by using different doping throughout the channel. This asymmetrical characteristic differentiates it from a regular MOSFET. An implantation process is used to create a doping grading in the channel also known as PHV implant. It is in fact followed by an annealing process, which is the one that diffuses the dopants along the channel. When talking about the DMOS transistor, the letter D in the name actually comes from the diffusion process that was just mentioned. The current path will then have four regions, which will be n+ source, PHV, n-drift region, and n+ drain. The advantage in creating this grading in the channel, with a more heavily doped source compared to the drain, is that this gradient generates an electric field, which produces an increase to the device current transport. In addition, the graded doping in the channel lets the transistor handle large amount of supply voltage without failing to the punch-through. This phenomena occurs when increasing the drain voltage, which is the reason why the depletion region expands from the p-n junction (n-drift region and epi region). Eventually, if the depletion region were to spread enough as to reach the n+ source, a sudden big supply of electrons

would be introduced into the channel and into the drain by the applied electric field. This short circuit effect is known as punch-through. The PHV more heavily doped region helps prevent punch-through due to the depletion region being inversely proportional to doping concentration. Thus, the transistor is able to manage high voltage power supply.

## 2.1 VDMOS And LDMOS Comparison

One of the differences with the LDMOS transistor is that the substrate or body is n-type instead of p-type. Besides this, the body in the VDMOS works as the drain whereas in the LDMOS the body is the source contact. Within the structure, the VDMOS n-drift region is typically built on top of the substrate and is an epi layer lightly doped compared to the heavily doped substrate. This n-drift region is the main area where most of the parasitic resistance will be found. Also, this resistance will spread towards the back of the wafer instead of just remaining on the surface like the LDMOS device. In terms of accomplishing high breakdown voltage, the VDMOS n-drift design allows to obtain voltages in the 200 V range compared to using the LDMOS lateral structure with typical voltage operation in the range of 50 V. The contrast between LDMOS and VDMOS lies in the fact that the LDMOS possesses high gain, efficiency and operating frequency whereas the VDMOS handles high power with high drain voltage but at lower frequencies.

Even though the vertical n-drift structure of the VDMOS brings advantages like high breakdown voltage and power handling, some of the disadvantages it has compared to the LDMOS device is that it cannot incorporate a field plate, which is the reason why LDMOS can accomplish low  $R_{on}$  without affecting the breakdown voltage.

Another disadvantage in the VDMOS is that by having the drain contact on the back of the wafer, some issues about connections and packaging become present. This occurs due to the backside of the wafer typically connected to heat sink, which is grounded. Lastly, current transport in the VDMOS in fact changes from lateral to vertical, which creates current crowding or nonhomogeneous current distribution that can reduce performance. This behavior can be seen in Fig. 3

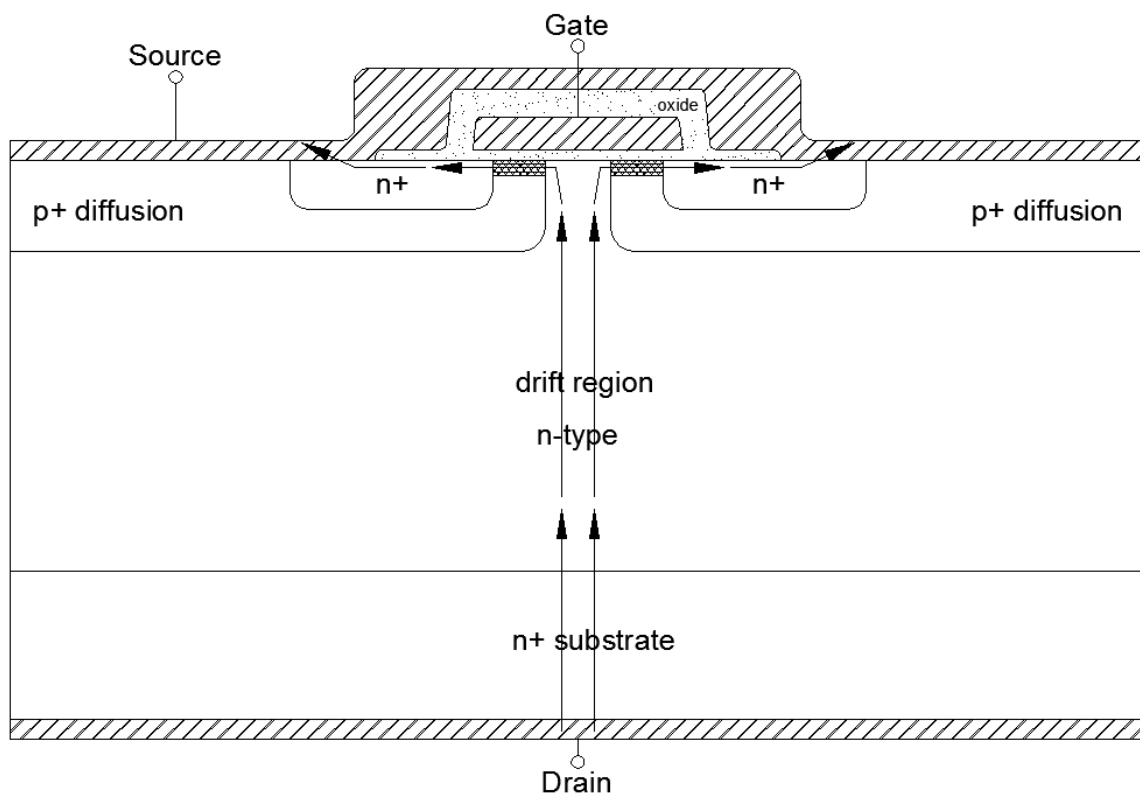


Figure 4: VDMOS current transport direction

## 2.2 Current Transport

In terms of how device physics act within the transistor, it can be pointed out that DMOS transistors present the same operation as any other regular three terminal n-MOSFET. The I-V curves of a VDMOS transistor is shown in Fig. 5.



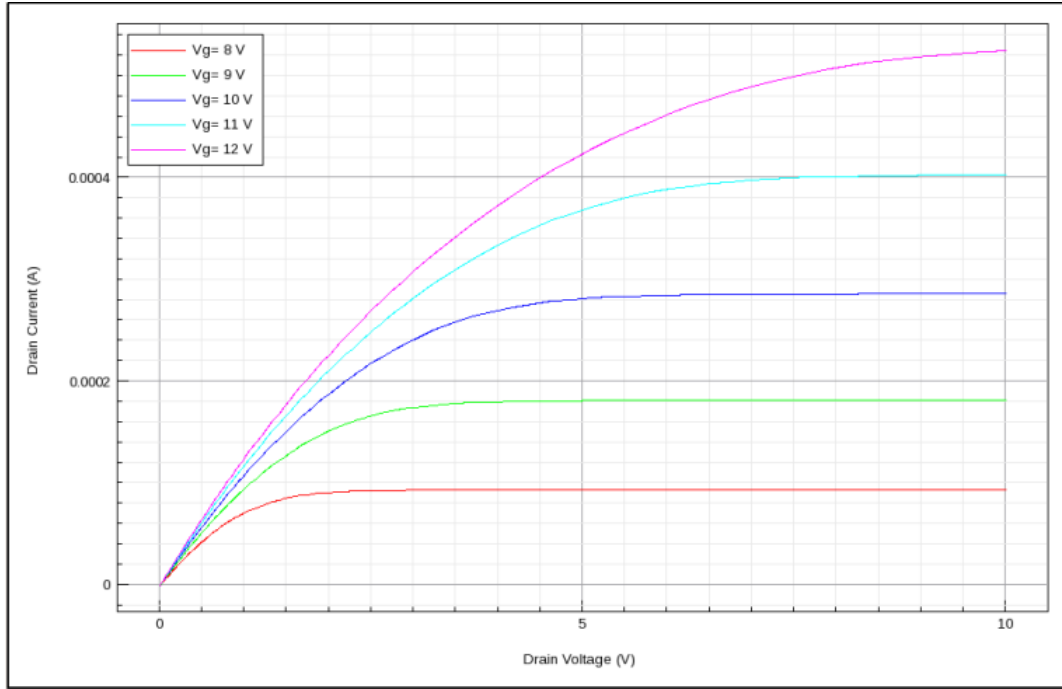


Figure 5: VDMOS typical  $I_D - V_D$  curves.

As it can be seen, it possesses the same regions as a typical MOSFET, which are: linear, cut-off, and saturation regions. Thus, the equations that describe the curve for the linear and saturation regions respectively are as follows.

$$I_D = \frac{\mu_s C_{ox} W}{L} \left[ (V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad (1)$$

$$I_D = \frac{\mu_s C_{ox} W}{2L} (V_G - V_T)^2 \quad (2)$$

Where  $I_D$  is the drain current,  $V_D$  is the drain voltage,  $V_G$  is the gate voltage,  $V_T$  is the threshold voltage,  $\mu_s$  is the electron mobility at the surface,  $C_{ox}$  is the oxide capacitance per unit area of the gate,  $W$  is the gate width,  $L$  is the gate length. As a result of using a graded channel doping, an induced electric field is added to the device, which incorporates a drift current component not existing in regular MOSFETs. This effect increases the carrier mobility and the transconductance. Also, it is worth noting that when using a small drain voltage, the term  $V_D^2$  can be neglected from equation (2) and the relationship between  $I_D$  and  $V_D$  becomes linear as seen next.

$$I_D = \frac{\mu_s C_{ox} W}{L} [(V_G - V_T)V_D] \quad (3)$$

It also can be remarked that the VDMOS device can only be used as a three terminal device, due to body being strictly connected to the drain contact. The advantage this design structure has is that now only two-top side contacts are needed (gate and source). Thus, the layout in the wafer can be reduced, which also translates into high voltage operation. To accomplish this, the drain is connected to the body internally. The current path starts at the drain contact located at the backside of the wafer; it continues moving vertically passing through the body and n-drift region, which is created by the epitaxial layer. Then, it goes through the channel to finally reach the source contact where it leaves the device. On the other hand, the electron flow goes in the opposite way.

### 2.3 VDMOS Parameters

In order to obtain high performance, there is trade-off that has to be done between these two parameters: breakdown voltage ( $V_{BR}$ ) and the on-resistance  $R_{on}$ . This is why the design is done in order to get the best results out of these parameters, which most of it is controlled by the drain region. This technique is known as drain engineering, and consists of managing the drain in terms of the n-drift region doping and length.

#### 2.3.1 Breakdown Voltage ( $V_{BR}$ )

Breakdown voltage ( $V_{BR}$ ) occurs between the drain and source while keeping the gate voltage at zero volts (transistor is turned off). Depending on the application, the breakdown voltage is adjusted by designing the lightly doped n-drift region. Thus,

an understanding of the breakdown mechanism is necessary in order to design the transistor.

The breakdown mechanism occurs when a very high electric field, that exceeds a critical value, is applied between the drain and source n-p junction. Thus, a phenomena known as avalanche breakdown takes place. When the p-n junction is reversed biased, which happens when the n-type drain is positively biased and the p-type source is negatively biased, makes the depletion region already present in each side of the junction, extend and grow further away from the junction. During this process, the charge remains balance within the depletion region even if different doping concentration is present on each side of the junction. Also, no carrier flow crosses the p-n depletion region during this process. Thus, the name depletion comes from the fact that this region is depleted of free carriers. Then, instead of having free carriers, the dopant atoms within the depletion region in the silicon lattice show a fixed charge. This charge is positive on the n-type side and negative on the p-side of the depletion region due to the atoms being ionized in the lattice. This charge difference creates an electric field going through the depletion region. In addition, the fixed charge on one side of the junction is equal in magnitude and opposite in charge to the other side, which is what makes it balanced. Thus, when increasing the drain voltage, the depletion region expands more, and more fixed charge is present which leads to a higher induced electric field. The size of the depletion region will depend on the doping concentration in the silicon. That is with higher concentration the depletion region will be shorter but with lower concentration the depletion region will be larger. Even though the depletion region as mentioned before is shorter in size, it actually contains a large amount of fixed charge depending on the doping concentration, which

is equal and balances out the other side of the depletion region. The alternate case would be with a large depletion region, the fixed charge is small and dopant dependent but it will be sufficient as to balance the other side of the depletion region. The size of the depletion region is important because when applying a voltage, the peak electric field generated over a large distance will be smaller than one that is made over a smaller size. After all, it is the peak electric field that generates the avalanche breakdown.

When analyzing the phenomena within the depletion region, electron-hole pairs are being generated due to the electric field. The applied field swiftly moves these generated carriers, which end up as leakage current in device. The higher the drain voltage, the higher the electric field. The peak electric field has a certain limit that once is surpassed, makes the electrons gain sufficient energy as to collide with the atoms in the lattice and break their covalent bonds. Thus, more electron-hole pairs are generated. These newly generated free carriers repeat the same process and as their number increases, an exponential increase of leakage current is generated as a result of the applied voltage. The process is also known as avalanche breakdown and can be seen in Fig. 6.

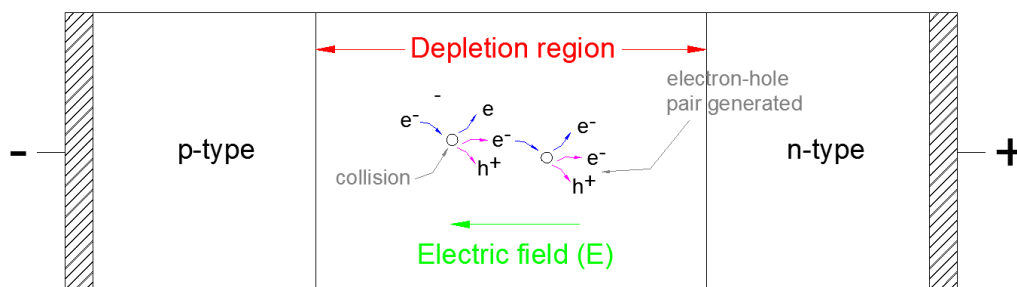


Figure 6: Avalanche breakdown effect in a p-n junction.

To obtain high breakdown voltage, a lightly doped concentration should be used in both sides of the junction, which are the drain and the source. In terms of the VDMOS, the body, which is connected to the source, is usually lightly doped already. On the other hand, the drain has a couple of alternatives to achieve high breakdown. First, as mentioned before is to use a light doping concentration. The next choice is to manipulate the length and depth of the drain, which becomes the n-drift region. By designing these two parameters, the depletion region will expand laterally and vertically across the n-drift region. This spread will reduce the electric field since now it will be split in two components (lateral and vertical). Therefore, in order to maximize the breakdown voltage, the electric field peaks located near the channel (lateral location) and near the n+ drain (vertical location) contact are designed to be equal, since the peak field is the one that creates the avalanche phenomena.

### 2.3.2 On-Resistance ( $R_{on}$ )

When analyzing the  $I_D$ - $V_{DS}$  MOSFET curve as seen in Fig. 5, the linear, pinch off, and saturation regions can be seen. It is in particular the linear region that has an important role since it is the one where the  $R_{on}$  can be extracted. In fact, the  $R_{on}$  will be the reciprocal of the slope in the linear region. This means that in case of having a steeper slope, the  $R_{on}$  will be low and it will produce high power and efficiency. On the other hand, a higher  $R_{on}$  will produce more delay. The objective of designing the transistor is to have the lowest  $R_{on}$  possible. In order to accomplish this, the n-drift region is manipulated. As stated before a lightly doped drain is needed to obtain high breakdown voltage, but the problem is that it would also increase the resistance. This is why a trade-off is made to obtain an optimized device. Thus, the whole design is

mostly done in the drain region due to this trade-off. Additionally, the  $R_{on}$  is composed of several components, like the source resistance and the channel resistance which will be explored next and can be seen in Fig.7.

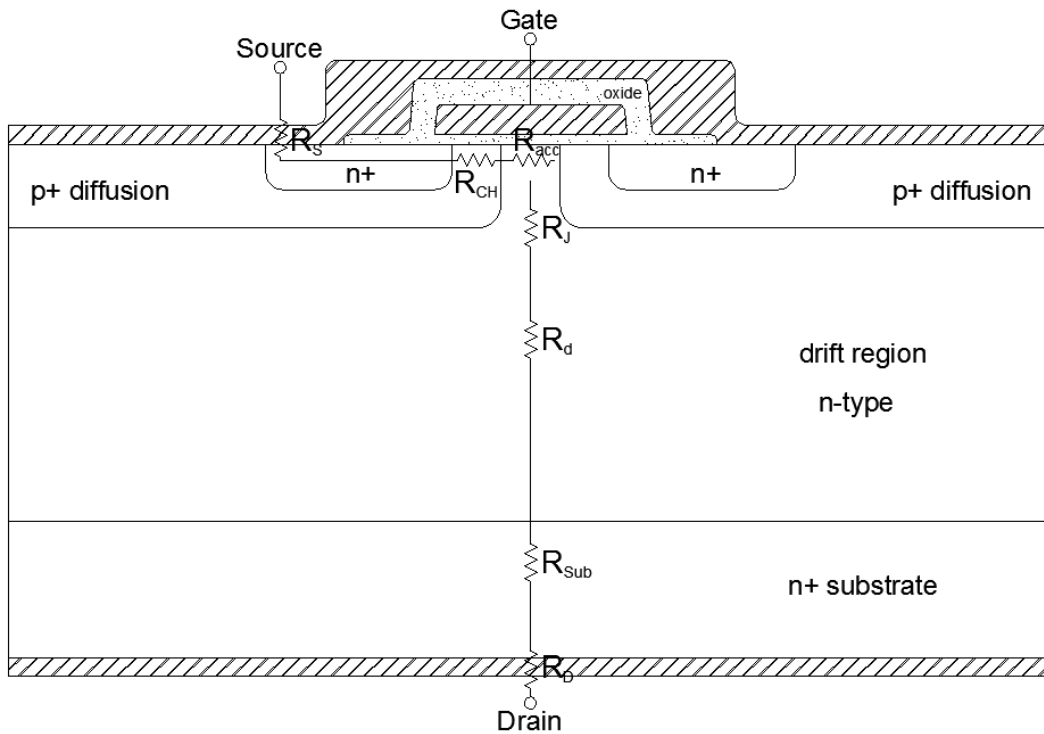


Figure 7: VDMOS structure showing the location of all the components of the total on-resistance in the device.

The addition of all the parasitic resistances would provide as a result the total on-resistance as expressed in eq. 4. Each of the individual resistances meaning is explained next [21].

$$R_{on} = R_S + R_{CH} + R_{acc} + R_J + R_d + R_{Sub} + R_D \quad (4)$$

$R_S$ : Source resistance. It is the resistance addition between the source terminal and the channel, which is the source wire bond, metallization, and n+ well.

$R_{CH}$ : Channel resistance. This resistance is inversely proportional to the channel width, and it has significant contribution in low-voltage applications.

$R_{acc}$ : Accumulation resistance. This resistance is in the epitaxial region just below the gate, and at this location the current changes from horizontal to vertical.

$R_J$ : JFET resistance. This resistance is created by the parasitic JFET, which reduces the width of the current flow. The p implantation forms the gate of the parasitic transistor.

$R_d$ : Drift region resistance. This is the region responsible for sustaining the blocking voltage. It is designed to be thick (high voltage) and lowly doped (high resistance). Thus, this is the resistance component that contributes the most in high-voltage applications.

$R_{Sub}$ : Substrate resistance. This is the resistance that is produced by the substrate.

$R_D$ : Drain resistance. It is the resistance addition between the drain terminal and the substrate, which is the drain wire bond, and metallization.

The importance of each of the on-resistance components depend on the applied voltage. The percentage of each component to add to the total on-resistance at different voltages is shown in Table 1.

Table 1: Parasitic resistance components percentages at different voltage ratings.

Resistances \ Voltage ratings	50 V	100 V	500 V
$R_S+R_D$	22.4 %	14.9 %	4 %
$R_{CH}$	34.3 %	28.4 %	4 %
$R_J$	13.4 %	14.9 %	16.4 %
$R_d$	22.4 %	35.8 %	71.6 %
$R_{Sub}$	7.5 %	6.0 %	4 %

Based on information from [21]

As can be seen from table 1, at low voltages, the on-resistance ( $R_{on}$ ) is mainly composed of the channel resistance ( $R_{CH}$ ), the drift resistance ( $R_d$ ), and the source and drain contact resistances ( $R_S+R_D$ ). On the other hand, at higher voltages the drift region resistance starts to dominate, which is the reason why a good design of the drift region is of utmost importance to reduce the total on-resistance.

## 2.4 Ideal Silicon Limit

The main goal in terms of finding the limit in a conventional DMOS power device is to understand how the current is blocked at high reverse voltages. When looking at the off-state operation ( $V_G=0$ ) of the device, the applied drain to source voltage in the VDMOS device mostly biases the p-body and the n-drift region, which increases the depletion region. Thus, the analysis can be performed in a simplified structure like the p-n junction as shown in Fig. 8. The electric field acting on the device is shown as well.

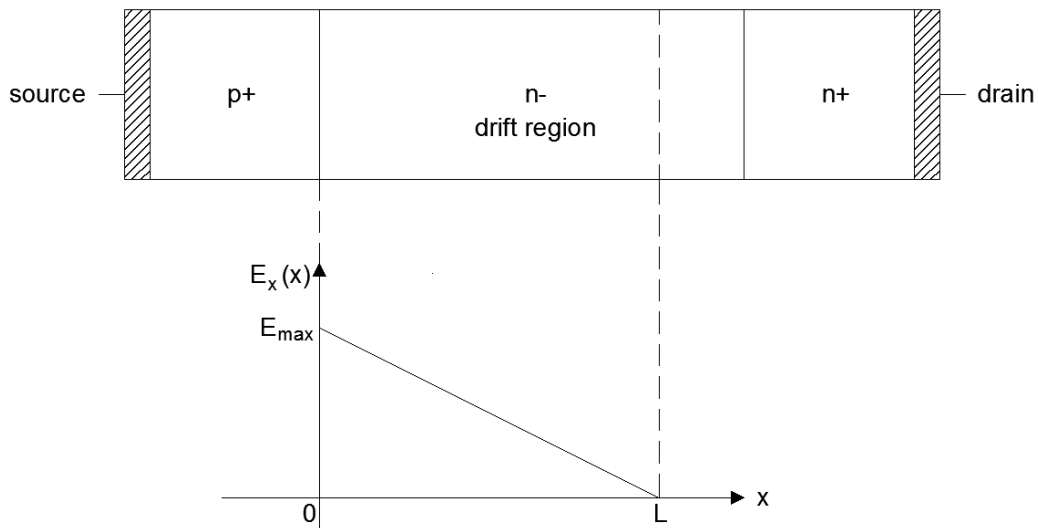


Figure 8: Simplified VDMOS structure and electric field for ideal silicon limit analysis.



To understand the limitation of the power device, a relationship between on-resistance ( $R_{on}$ ) and breakdown voltage ( $V_{BR}$ ) in a conventional VDMOS device has to be obtained [21]. Therefore, to begin with, the Poisson equation needs to be solved. The equation in the n-drift region is used as follows.

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = \frac{E_{max}}{L} - \frac{Q(x)}{\epsilon_s} = -\frac{qN_D}{\epsilon_s} \quad (5)$$

Using the boundary conditions  $E = E_{max}$  at  $x = 0$  and  $E = 0$  at  $x = L$ . The following solution for electric field is obtained:

$$E(x) = \frac{qN_D}{\epsilon_s}(L - x) \quad (6)$$

Where  $E(x) = E_{max}$  at  $x = 0$

$$E_{max} = \frac{qN_D L}{\epsilon_s} \quad (7)$$

Also, by integrating the electric field along the depletion region in the n-drift area and approximating no electric field distribution in the p+ body, the voltage can be obtained as follows.

$$V(x) = \frac{qN_D}{\epsilon_s}\left(Lx - \frac{x^2}{2}\right) \quad (8)$$

And at  $x = L$ , the voltage would be:.

$$V(L) = \frac{qN_D L^2}{2\epsilon_s} \quad (9)$$

The breakdown voltage ( $V_{BR}$ ) occurs when the maximum electric field reaches what is known as the critical electric field. Thus,  $V(L)$  becomes  $V_{BR}$  when  $E(x) = E_{max} = E_C$  and  $L$  becomes the depletion region length at  $E(x) = E_{max}$  as shown next.

$$V_{BR} = \frac{qN_D \left(\frac{E_C \epsilon_s}{qN_D}\right)^2}{2\epsilon_s} = \frac{\epsilon_s E_C^2}{2qN_D} \quad (10)$$

Where  $\epsilon_s$  is the silicon permittivity,  $q$  is the electron charge, and  $N_D$  is the n-drift doping concentration. The breakdown voltage can also be obtained by the electric field

integration at  $E_{max} = E_C$  (area under the curve) in Fig. 8. The critical electric field can be approximated with the following expression.

$$E_C = 4010 \cdot N_D^{1/8} \quad (11)$$

By combining the previous two equations, the following relation can be obtained.

$$V_{BR} = 5.34 \times 10^{13} N_D^{-3/4} \quad (12)$$

From this equation, it can be seen that for conventional DMOS reducing the doping concentration is the only solution to increase the breakdown voltage.

As discussed before, the applied voltage is mainly supported in the n-drift depletion region. When this reverse voltage is sufficiently high, the electric field is increased, thus providing the free carriers with enough high energy to start a collision process also known as impact ionization. This phenomena has been explained before and when the impact ionization is really high, the device is said to go under avalanche breakdown, which is a condition [22] that can be expressed mathematically with the following equation.

$$\int_0^W \alpha \cdot dx = 1 \quad (13)$$

Where  $\alpha$  is the impact ionization coefficient and can be expressed as follows.

$$\alpha = 1.8 \times 10^{-35} \cdot E^7 \quad (14)$$

By substituting and combining eqns. (6), (13), and (14), the depletion region length ( $L$ ) can be found.

$$L = 2.67 \times 10^{10} N_D^{-7/8} \quad (15)$$

By substituting eqn. (12), the depletion depth can be expressed in terms of breakdown voltage.

$$L = 2.58 \times 10^{-6} V_{BR}^{7/6} \quad (16)$$

The on-resistance, which is found in eq. (4) and contains all its individual components can be used next but is expressed now as the specific on-resistance.

$$R_{on\_sp} = R_{on} \cdot A = \frac{L}{q\mu N_D} \quad (17)$$

By substituting eqns. (15), (16) and using the values of  $q = 1.602 \cdot 10^{-19} C$  and  $\mu = 1500 cm^2/V - s$  into the previous equation the following is obtained.

$$R_{on\_sp} = 5.4 \times 10^{-9} \times V_{BR}^{2.5} \quad (18)$$

This expression is known as the silicon limit, and it shows that the on-resistance increases with the 2.5 power of the breakdown voltage in a conventional VDMOS. The high exponential increase of the on-resistance with the breakdown voltage clearly establishes the limit in the device performance. Thus, this relation also shows exactly how it is not possible to reduce one without a trade-off with the other one.

Furthermore, one of its characteristics is that in order to increase the breakdown voltage, the n-drift region length ( $L$ ) has to be increased or the n-drift region doping ( $N_D$ ) has to be reduced, as seen in eq. 10. This becomes an issue given that any of these two actions would also increase the on-resistance as expressed in eq. 17.

## CHAPTER 3: SUPER JUNCTION THEORY

This chapter focuses on why the superjunction is relevant and can be used as an improved structure compared to a conventional VDMOS structure. Also, a fabrication process to build the VDMOS device using Sentaurus is presented, This transistor is the one used to obtain the final device with optimized parameters.

### 3.1 What Is The Superjunction Structure?

Superjunction is a technique implemented in DMOS devices for the purpose of obtaining high breakdown voltage but with smaller on-resistance than the conventional device. In order to accomplish this, the drift region structure is modified and by doing this, the previous obstacle in the device identified as silicon limit is overcome. The superjunction drift region is composed of at least two oppositely doped pillars n and p, as opposed to the conventional device where the drift region is made out of only one type of doping. Actually, more than two pillars can be used when implementing the device This can have benefits over using just two, but certain conditions have to be taken into considerations.

To understand the reasons why this different structure works, an analysis on electric field and charge balance is needed. Fig. 9 shows a VDMOS transistor using a three-pillar superjunction structure, which can be seen differs from the conventional device shown in Fig. 2.

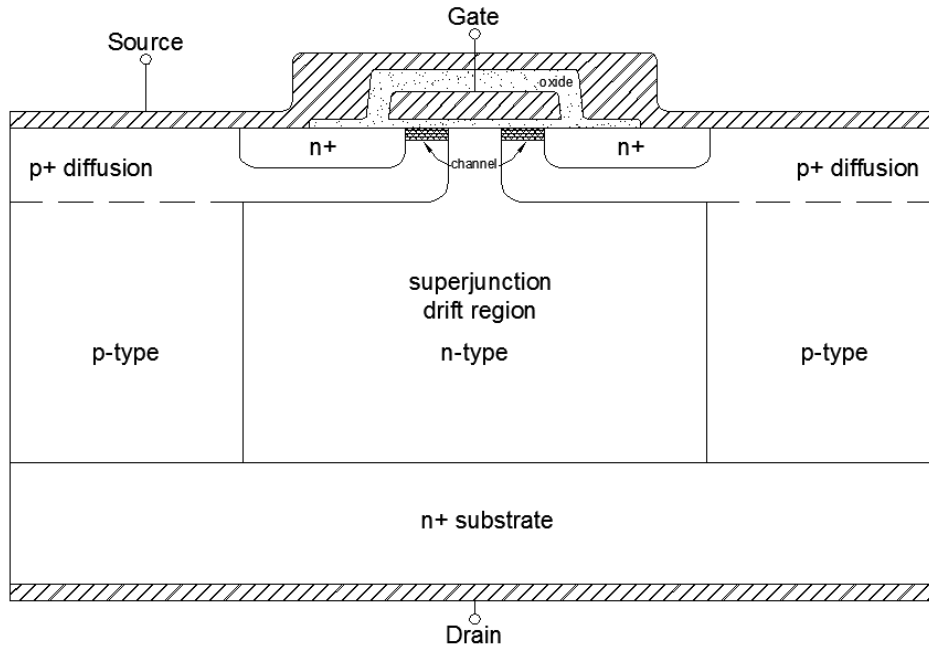


Figure 9: VDMOS three-pillar superjunction structure, showing its source, gate, drain contacts, channel and drift-region pillars location.

### 3.2 Charge Balance

When considering the conventional VDMOS electric field distribution, the breakdown voltage is given by the integral of the electric field curve. When looking at Fig. 8, it can be seen that this integral would be equal to the area under the curve, which has triangular shape. Thus, the best way to maximize the breakdown voltage would be by having a constant electric field throughout the entire drift region length ( $L$ ) whose magnitude is  $E_C$ . In this way, the area under the curve now would be rectangular and the breakdown voltage could be expressed as  $V_{BR} = W \cdot E_C$  [23].

To achieve a constant electric field distribution, the electric field slope should be zero, and as expressed by the Poisson equation (eq. 5), this could be done by having a zero doping concentration  $N_D$  (intrinsic concentration). Unfortunately, this would also make the on-resistance infinite (ideally) consequently not improving the silicon limit.

To obtain an equivalent to zero doping, the drift region could be uniformly doped with n and p type concentration. If both dopants used have the same amount of dopant concentration, the positive charge would balance the negative charge (net charge equals zero) and a region similar to intrinsic concentration is obtained. This structure would create a constant electric field but the on-resistance would still be infinite (ideal). An alternative would be to instead of having the n and p dopant atoms randomly distributed through the drift region; they can be arranged in pillars throughout the drift region. The electric field would remain constant creating a maximized breakdown voltage. More importantly, this structure now provides a path with low resistance where the current can flow easily. Therefore, the on-resistance would no longer be infinite and it can be reduced and designed to obtain an optimized device. These structures are illustrated in Fig. 10.

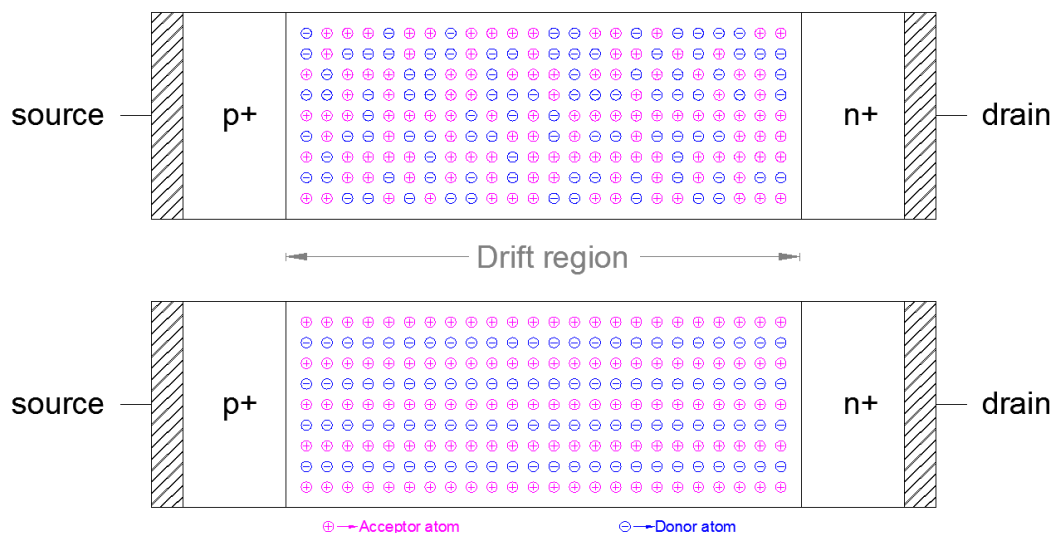


Figure 10: drift region with uniformly random (top) and pillar/row (bottom) distributed dopant atoms.

As a device with atom arranged dopants can not be built, dopant columns are manufactured in the drift region instead. In the end, a superjunction structure as shown in Fig. 11 can be made. This structure improves the silicon limit presented in the conventional device due to the charge balance located in the drift region.

### 3.3 The SJ Electric Field

Another alternative to analyze the superjunction structure is by looking at the electric field. Since this structure now has a p-n junction in the drift region, a two dimensional electric field is present which means it now has x and y components, as seen in Fig. 11. In addition, the depletion region expands more rapidly in the superjunction due to the n and p pillars depleting each other compared to conventional device. The applied reverse voltage makes the superjunction fully depleted at lower voltage compared to conventional devices. Thus, when reaching full depletion of the drift region, the electric field distribution goes from triangular to rectangular shape as mentioned before.

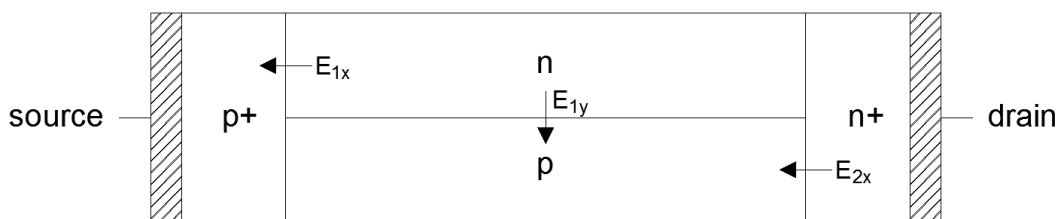


Figure 11: Electric field horizontal and vertical components in superjunction structure.

Now, by applying the Poisson equation into the two dimensional electric field, the following is obtained.

$$\nabla E = \frac{dE_x}{dx} + \frac{dE_y}{dy} = \frac{qN_D}{\epsilon_s} \quad (19)$$

Looking at the n-type pillar, the electric field x component can be expressed as:

$$\frac{dE_x}{dx} = \frac{qN_D}{\epsilon_s} - \frac{dE_y}{dy} \quad (20)$$

As can be seen by the previous equation, the electric field which drives the current through the device no longer depends only on the doping concentration ( $N_D$ ), but it is actually reduced by the electric field present perpendicular in the y direction. Now the breakdown voltage is given by the integral of the x component electric field along the drift region length. Thus, in order to maximize the breakdown voltage, the slope of the x component electric field needs to be reduced and this can now be done by using the y component of the electric field. Therefore, by optimizing the device design, the y component electric field can be used in such a way that it allows a constant electric field in the x direction regardless of the pillar doping.

### 3.4 Surpassing The Silicon Limit

To understand how the superjunction structure can surpass the conventional device, the relation between on-resistance and breakdown voltage has to be found. A simplified superjunction VDMOS structure and electric field are analyzed in Fig. 12.

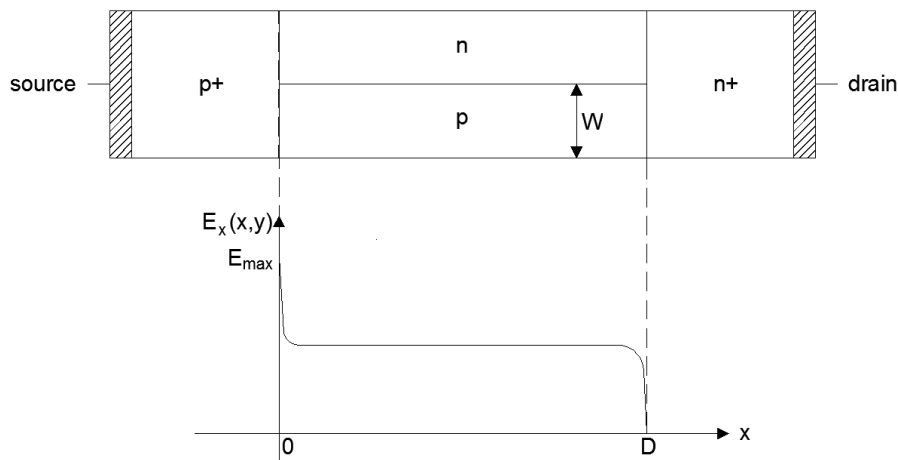


Figure 12: Simplified superjunction VDMOS structure and electric field distribution.



Given that the superjunction structure has a two dimensional electric field distribution in the drift region, the Poisson equation shown in eq. 19 has to be solved. The solution for the x component of the electric field ( $E_x$ ) is made of two parts:  $E_0$  and  $E_1$  [24].  $E_0$  is a constant value produced by the applied reverse voltage, expressed as follows.

$$E_0 = \frac{V_B}{D} \quad (21)$$

Where  $V_B$  is the applied reverse voltage and  $D$  is the drift region length/depth. On the other hand,  $E_1$  is produced by the drift region charge. Since charge balance is accomplished, the n and p pillars compensate each other charge. The problem lies near the edges where the n+ and p+ contacts are located. Thus,  $E_1$  is mostly zero throughout the drift region but it has peak values near the contacts, a positive peak near the p+ column and a negative peak near the n+ column. By adding both solutions, an electric field distribution as shown in Fig. 12 is obtained. To optimize the structure, the electric field should follow the following condition  $E_0 = E_1 = E_C/2$ , which means that the breakdown voltage (area under the curve) can be expressed as  $E_0 \times L$ .

The maximum electric field is found next. For this, the assumption of having same width pillars ( $w_N = w_P = w$ ) and doping ( $N_D = N_A = N$ ) is done. Also, before the p and n column full depletion, the electric field increases in the n+/p and p+/n junctions near the contacts. A merging lateral voltage is produced at the p and n columns and can be expressed as:

$$V_{lateral} = \frac{qNw^2}{4\epsilon_s} \quad (22)$$

This voltage produces a depletion depth ( $x_n$ ) in the n column as follows.

$$x_n = \left[ \frac{2\epsilon_s V_{lateral} N_{p+}}{q(N+N_{p+})N} \right]^{1/2} \approx \frac{1}{\sqrt{2}} w \quad (23)$$

Also, the electric field created at the p+/n junction is given by:

$$E_A = x_n \left( \frac{qN}{\epsilon_s} \right) = \frac{qN}{\sqrt{2}\epsilon_s} w \quad (24)$$

When this electric field reaches its peak value, it also means it reaches the critical electric field, as expressed next.

$$E_{max} = E_A = E_C \quad (25)$$

From eq. 11 the relation between critical electric field and doping is given. By combining eqns. 11, 24, and 25 and using the values of  $q = 1.602 \cdot 10^{-19} \text{ C}$  and  $\epsilon_s = 11.9 \times 8.85 \times 10^{-14} \text{ F/cm}$ , the column doping concentration ( $N$ ) is obtained.

$$N = 1.2 \times 10^{12} w^{-8/7} \quad (26)$$

When using the optimized doping concentration, the breakdown voltage can be obtained as follows.

$$V_{BR} = E_0 \times D = \frac{E_C}{2} \times D = \frac{E_A}{2} \times D \quad (27)$$

When substituting eq. 24 in the previous equation.

$$V_{BR} = \frac{qN}{2\sqrt{2}\epsilon_s} wD \quad (28)$$

Now, by using the specific on-resistance definition and combining it with eq. 28, the following is obtained.

$$R_{on\_sp} = \frac{2 \times D}{q\mu N} = \frac{2 \times \left( \frac{2\sqrt{2} \times \epsilon_s \times V_{BR}}{qNw} \right)}{q\mu N} = \frac{4\sqrt{2} \times \epsilon_s \times V_{BR}}{q^2 \mu N^2 w} \quad (29)$$

Finally, the specific on-resistance and breakdown voltage relation is obtained by substituting eq. 26.

$$R_{on\_sp} = 0.107 w^{9/7} V_{BR} \quad (30)$$

This final relation between on-resistance and breakdown voltage for the superjunction structure is ideal, as the one obtained in a conventional device in the silicon limit relation. However, it has two major differences with respect to the

conventional device. First, there is a linear relationship between the on-resistance and the breakdown voltage. The other one is that the on-resistance is now also dependent on the superjunction width. Eq. 18 represents the ideal silicon limit and eq. 30 represents the ideal superjunction performance. Curves using both equations were plotted and shown in Fig. 13 where a comparison between them can be made.

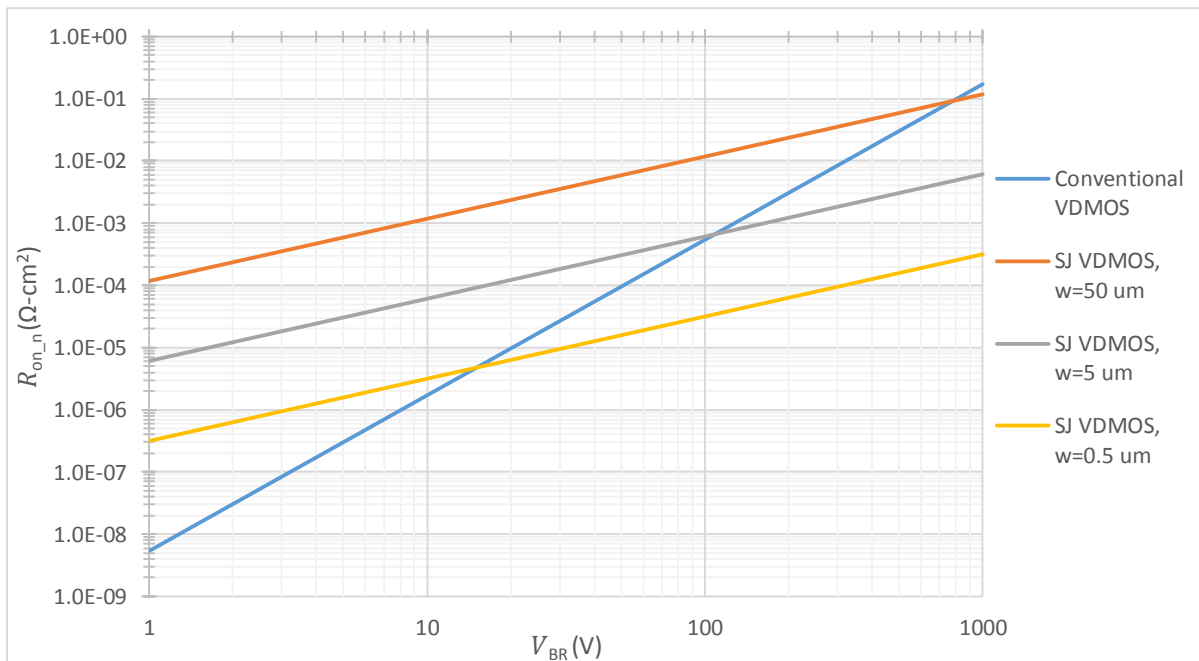


Figure 13: Conventional and superjunction on-resistance vs breakdown voltage curves.

A comparison between the superjunction structure and the conventional device can be done from the previous figure. To determine which structure is better, it really depends on the type of application the device is to be used for. For example, it can be seen that for breakdown voltage higher than 100 V, the superjunction structure shows lower on-resistance, which also depends on the superjunction pillar width. The silicon limit is surpassed at high breakdown voltages and the superjunction benefit stands out.

### 3.5 Superjunction Design Parameters

Conventional DMOS devices can adjust two parameters in order to modify the breakdown voltage. These are the drift region thickness and doping ( $N_D$ ). This makes the design not too complex. On the other hand, the superjunction structure actually has five parameters that can be used for the device design. These are the drift region length/depth ( $D$ ), the n and p pillars widths ( $W_N$ ,  $W_P$ ), and the n and p pillars doping ( $N_D$ ,  $N_A$ ). Thus, making the superjunction design more challenging than conventional devices. These parameters are illustrated in Fig. 14.

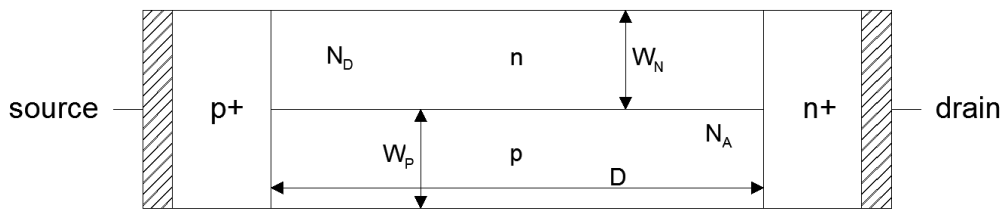


Figure 14: Superjunction structure showing the design parameters.

When having all these parameters, one way to design a superjunction device would be by using a simulator like Sentaurus to optimize the device. As a starting point, the simplest way to design the n-drift region is by having a symmetrical structure as well as keeping the charge balanced. A symmetrical structure is obtained by having  $W_N = W_P$ . However, to obtain charge balance where the n and p pillars have  $N_D$  and  $N_A$  doping concentrations respectively, the following condition has to be accomplished.

$$W_N N_D = W_P N_A \quad (31)$$

From the previous equation, it can be seen that by having a symmetrical structure, charge balance is achieved by having equal doping concentration on the drift region pillars  $N_D = N_A$ .

### 3.6 VDMOS Fabrication Process Using Sentaurus

The fabrication process of the VDMOS transistor is illustrated next step by step for a complete understanding of how the device could be implemented. A software called Sentaurus was used for the simulation. It should be point out that even though the process simulation was used; the process used to implement the device is likely to be too ideal compared to a real fabrication process. However, it still provides a solution and an idea on how the VDMOS could be built if desired [25].

The process starts with a wafer with the following characteristics.

- Silicon Concentration: Boron:  $1 \times 10^{10}$ , Phosphorus:  $1 \times 10^{18}$
- Wafer orientation: 100

Once the silicon wafer is chosen, the process continues as follows.

#### 3.6.1 Pillars

- Oxide deposition: 1  $\mu\text{m}$  thickness (Isotropic)
- Photoresist deposition: 3  $\mu\text{m}$  (using mask “ppillar”)

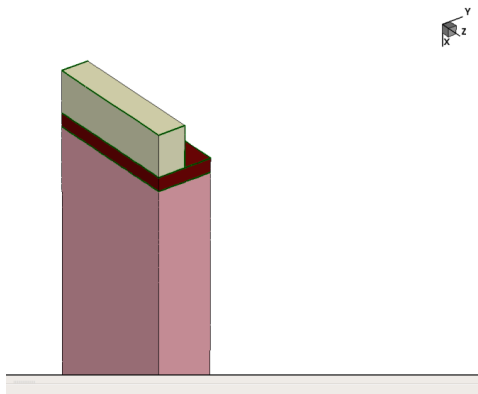


Figure 15: VDMOS fabrication step 1

- Oxide etching: 2 $\mu\text{m}$  thickness (Anisotropic)
- Silicon etching: 5  $\mu\text{m}$  thickness (“D” length) (Anisotropic)
- Photoresist Strip

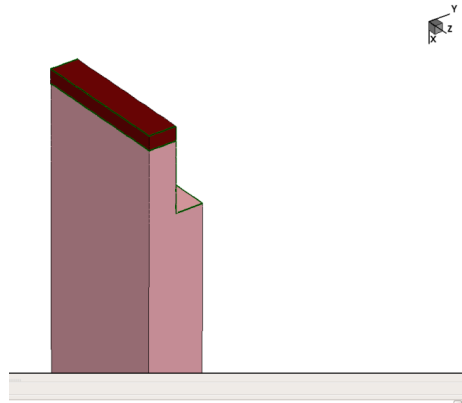


Figure 16: VDMOS fabrication step 2

- Epitaxial growing process: 2.2  $\mu\text{m}$  thickness.

Boron concentration:  $17.5 \times 10^{15}$ , Temperature: 100  $^{\circ}\text{C}$ , time= 200 min.

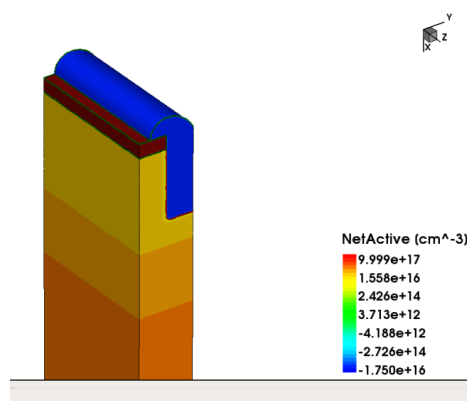


Figure 17: VDMOS fabrication step 3

- Oxide strip
- Chemical Mechanical Polishing (CMP)

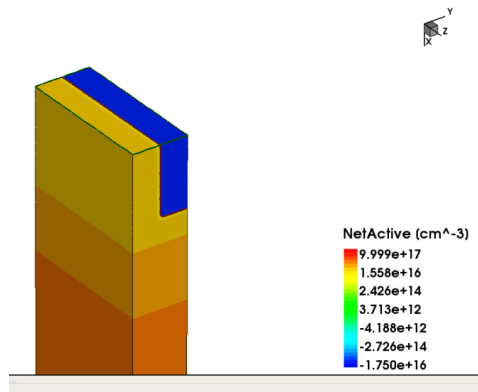


Figure 18: VDMOS fabrication step 4

- Epitaxial growing process: 2  $\mu\text{m}$  thickness.  
Phosphorus concentration:  $1 \times 10^{16}$ , Temperature: 800  $^{\circ}\text{C}$ , time= 100 min.
- Oxide deposition: 0.1  $\mu\text{m}$  thickness (Isotropic)

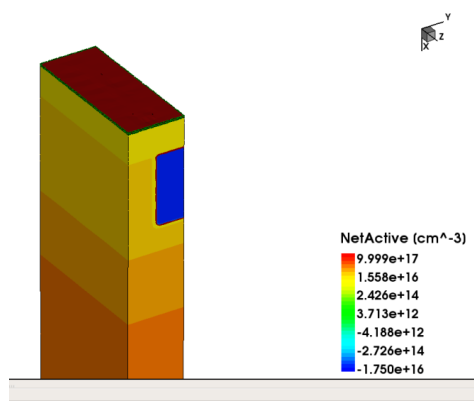


Figure 19: VDMOS fabrication step 5

### 3.6.2 p-well

- Photoresist deposition: 3  $\mu\text{m}$  (using mask "pwell")
- Boron Implantation:
  - Dose:  $2.5 \times 10^{13}$ , energy: 260 KeV, tilt: 0, rotation: 0.
  - Dose:  $2.5 \times 10^{13}$ , energy: 60 KeV, tilt: 0, rotation: 0.

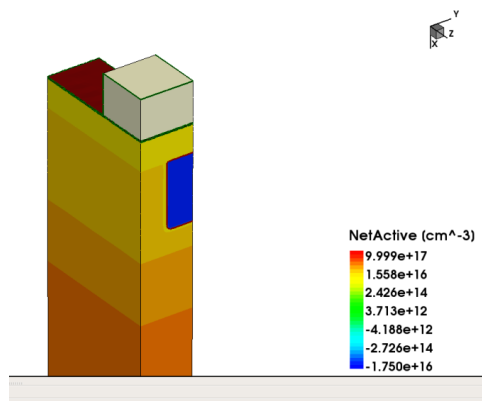


Figure 20: VDMOS fabrication step 6

- Photoresist Strip
- Diffusion Process:
  - From 700 °C to 1100 °C in 100 min (4 °C/min)
  - Remains in 1000 °C for 100 min.
  - From 1100 °C to 700 °C in 150 min (-2.67 °C/min)

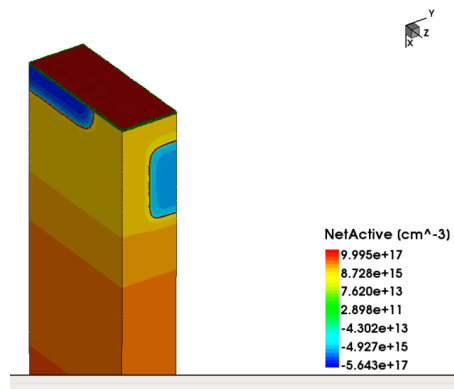


Figure 21: VDMOS fabrication step 7



### 3.6.3 Gate

- Oxide strip
- Oxide deposition: 0.05  $\mu\text{m}$  thickness (gate oxide) (Isotropic)
- Polysilicon deposition: 2  $\mu\text{m}$  thickness (Isotropic)

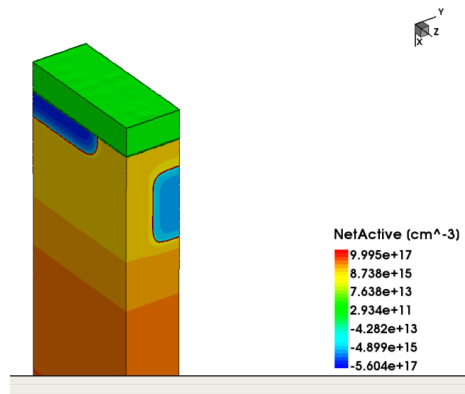


Figure 22: VDMOS fabrication step 8

- Photoresist deposition: 3  $\mu\text{m}$  (using mask "gate")

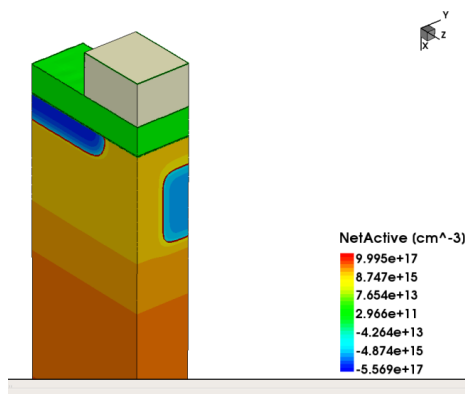


Figure 23: VDMOS fabrication step 9

- Polysilicon etching: 4  $\mu\text{m}$  thickness (Anisotropic)
- Photoresist Strip

- Diffusion Process (Annealing):
  - From 700 °C to 1000 °C in 90 min ( 3.33 °C/min)
  - Remains in 1000 °C for 115 min.
  - From 1000 °C to 700 °C in 120 min ( -2.5 °C/min)

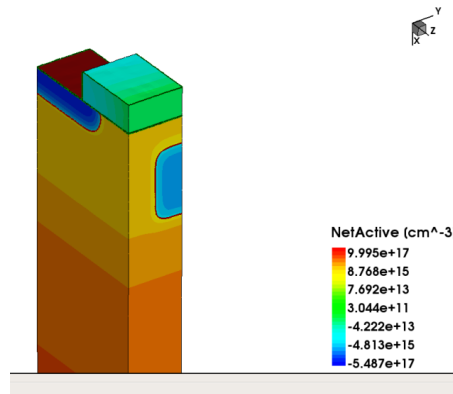


Figure 24: VDMOS fabrication step 10

### 3.6.4 n+ source

- Photoresist deposition: 3 μm (using mask “nplus”)
- Implantation process:
  - Arsenic, dose:  $2 \times 10^{15}$ , energy: 100 KeV, tilt: 0, rotation: 0.
  - Phosphorus, dose:  $1 \times 10^{15}$ , energy: 100 KeV, tilt: 0, rotation: 0.

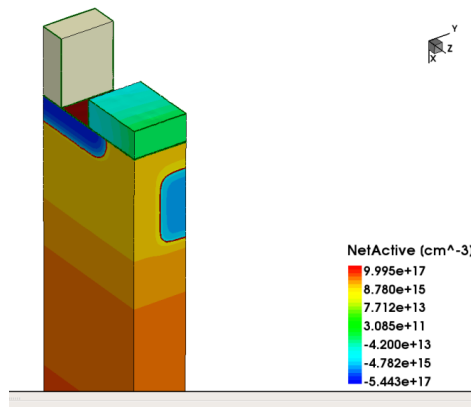


Figure 25: VDMOS fabrication step 11

- Photoresist Strip

- Diffusion Process:

From 700 °C to 1050 °C in 0.25 min (1400 °C/min)

Remains in 1050 °C for 1 min.

From 1050 °C to 700 °C in 0.42 min (-833.33 °C/min)

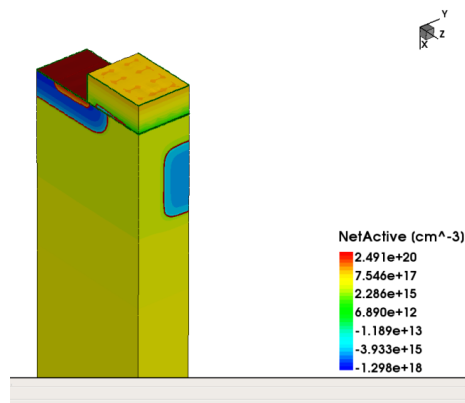


Figure 26: VDMOS fabrication step 12

### 3.6.5 p+ contact

- Photoresist deposition: 3 μm (using mask “pplus”)

- Boron Implantation:

Dose:  $2 \times 10^{15}$ , energy: 30 KeV, tilt: 0, rotation: 0.

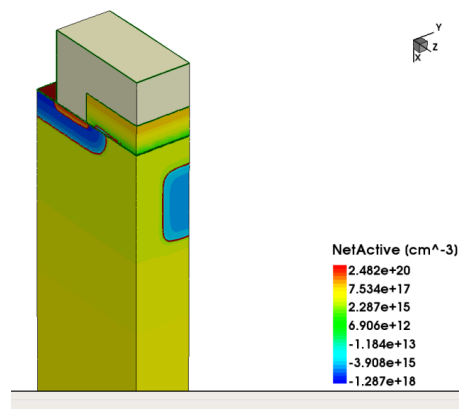


Figure 27: VDMOS fabrication step 13

- Photoresist Strip
- Diffusion Process:
  - From 700 °C to 1000 °C in 0.2 min (1500 °C/min)
  - Remains in 1000 °C for 1 min.
  - From 1000 °C to 700 °C in 0.37 min (-810.81 °C/min)

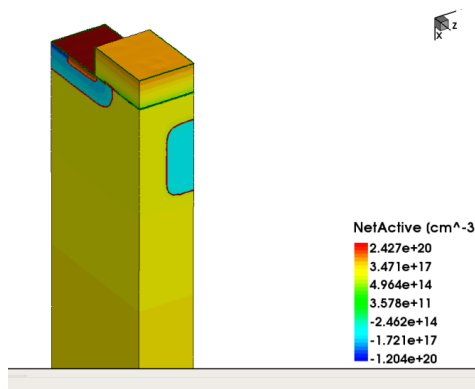


Figure 28: VDMOS fabrication step 14

### 3.6.6 Backend

- Oxide etching: 1 μm thickness (Anisotropic)
- Metal deposition: 1 μm thickness (Isotropic)

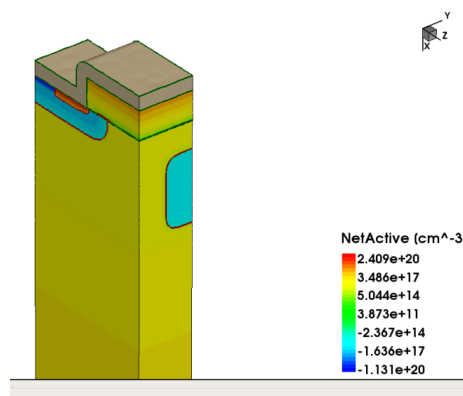


Figure 29: VDMOS fabrication step 15

- Photoresist deposition: 3  $\mu\text{m}$  (using mask “source”)

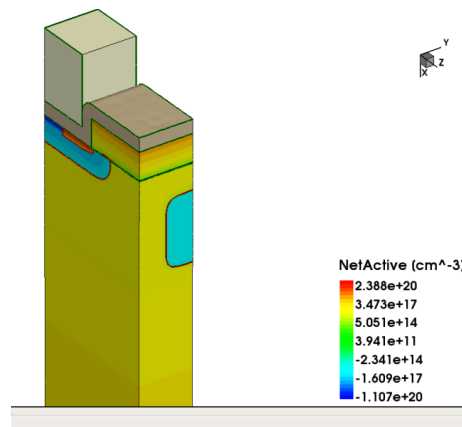


Figure 30: VDMOS fabrication step 16

- Metal etching: 5  $\mu\text{m}$  thickness (Anisotropic)
- Photoresist Strip
- Metal etching: 0.5  $\mu\text{m}$  thickness (Anisotropic)

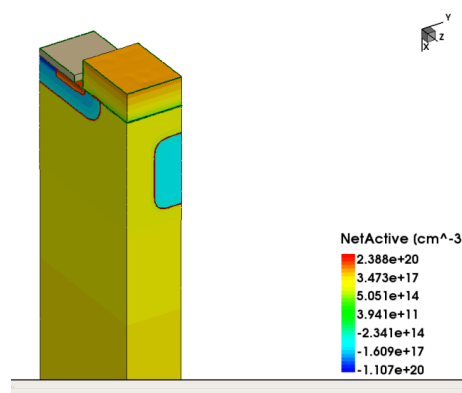


Figure 31: VDMOS fabrication step 17

Finally, Table 2 presents the final optimized device most important dimensions, thus the size of the device is better understood.

Table 2: Summarized final device dimensions.

Channel length	2 $\mu\text{m}$
Device width	4 $\mu\text{m}$
Device length	10 $\mu\text{m}$
Pillar width	2 $\mu\text{m}$
Pillar depth	5 $\mu\text{m}$

In addition, the final device complete view can be seen in Fig. 32 where the total size can be appreciated. The final device in this figure is ready for simulation.

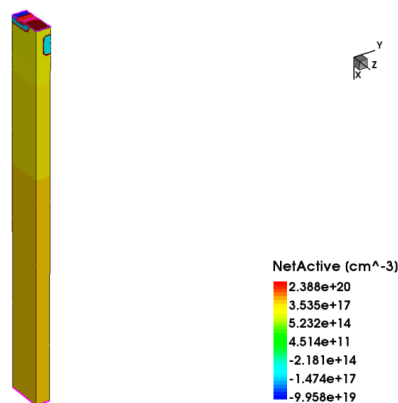


Figure 32: VDMOS device final structure.

## CHAPTER 4: VDMOS RESULTS

This chapter focuses on presenting the results obtained from the VDMOS Sentaurus simulation. That is, all the I-V curves and parameter extractions like threshold voltage, breakdown voltage and on-resistance at different device conditions. Additionally, the goal is to obtain a device for a 70 V application.

The process to obtain the optimized device is done in three steps. First, the superjunction structure is implemented. Then, the drift region pillar depth is decreased. Finally, the drift region doping concentration is increased.

### 4.1 Conventional VDMOS And Superjunction VDMOS

A comparison between the conventional VDMOS structure and superjunction VDMOS is presented next. For this, the  $I_D$  vs  $V_G$ ,  $I_D$  vs  $V_D$  curves are presented and the  $V_T$ ,  $V_{BR}$  and  $R_{on}$  parameters are extracted.

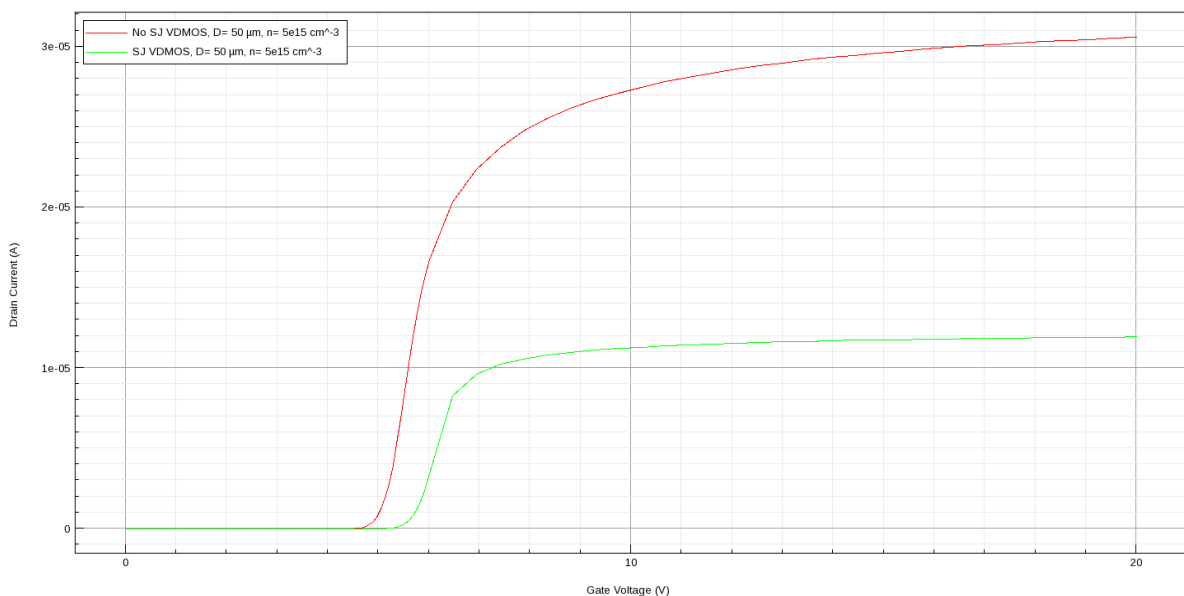


Figure 33:  $I_D$  vs  $V_G$  curve for conventional (red) and superjunction (green) VDMOS devices.

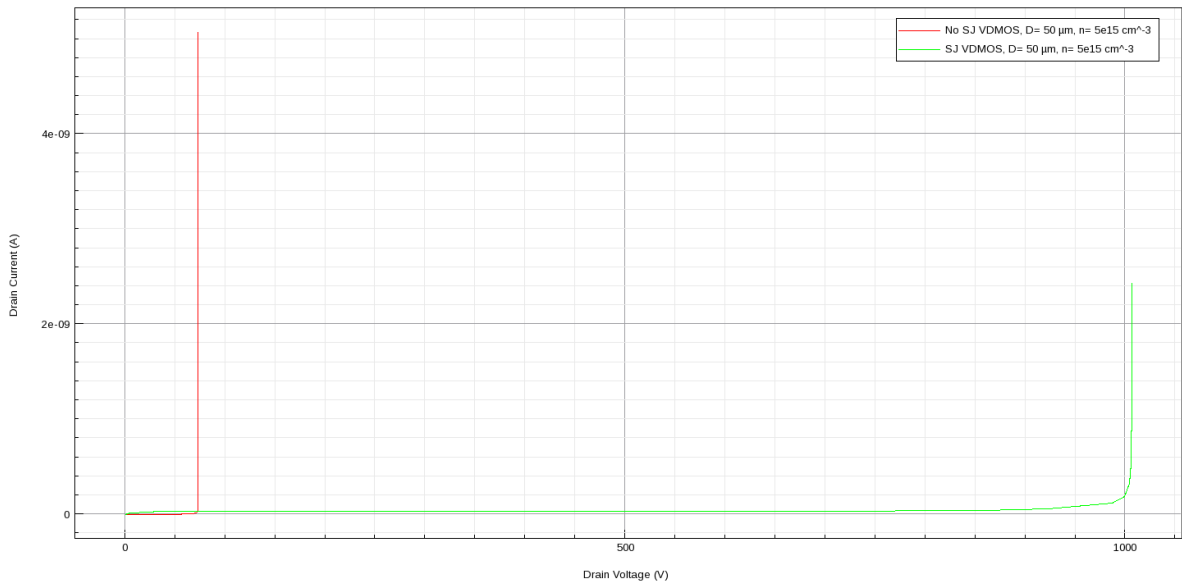


Figure 34:  $I_D$  vs  $V_D$  curve at  $V_G=0$  V for conventional (red) and superjunction (green) VDMOS devices.

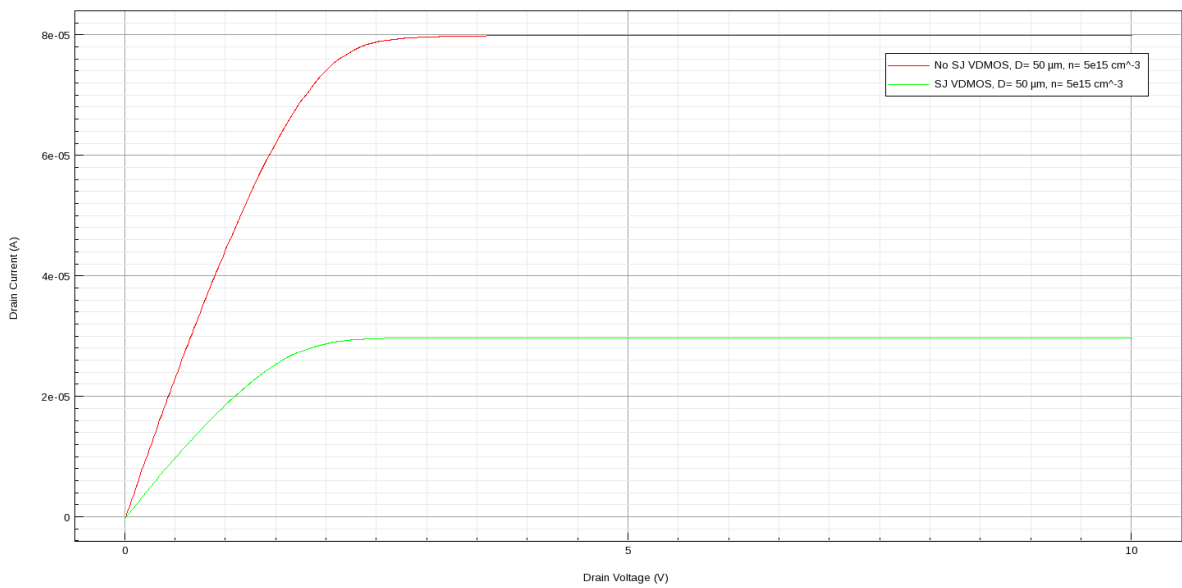


Figure 35:  $I_D$  vs  $V_D$  curve at  $V_G=0.5$  V for conventional (red) and superjunction (green) VDMOS devices.

The threshold voltage, breakdown voltage and on-resistance parameters are extracted and summarized in table 3.



Table 3: No SJ and SJ VDMOS results

	$n$ ( $\text{cm}^{-3}$ )	$D$ ( $\mu\text{m}$ )	$V_T$ (V)	$V_{BR}$ (V)	$R_{on\_sp}$ ( $\Omega\text{-mm}^2$ )
No SJ	$5 \times 10^{15}$	50	4.88	72	0.83
SJ	$5 \times 10^{15}$	50	5.6	985	1.94

#### 4.2 Decreasing Superjunction Depth “D”

Next, a comparison between the conventional VDMOS structure and superjunction VDMOS is presented by decreasing the superjunction depth “D”. For this, the  $I_D$  vs  $V_G$ ,  $I_D$  vs  $V_D$  curves are presented and the  $V_T$ ,  $BV$  and  $R_{DS(on)}$  parameters are extracted.

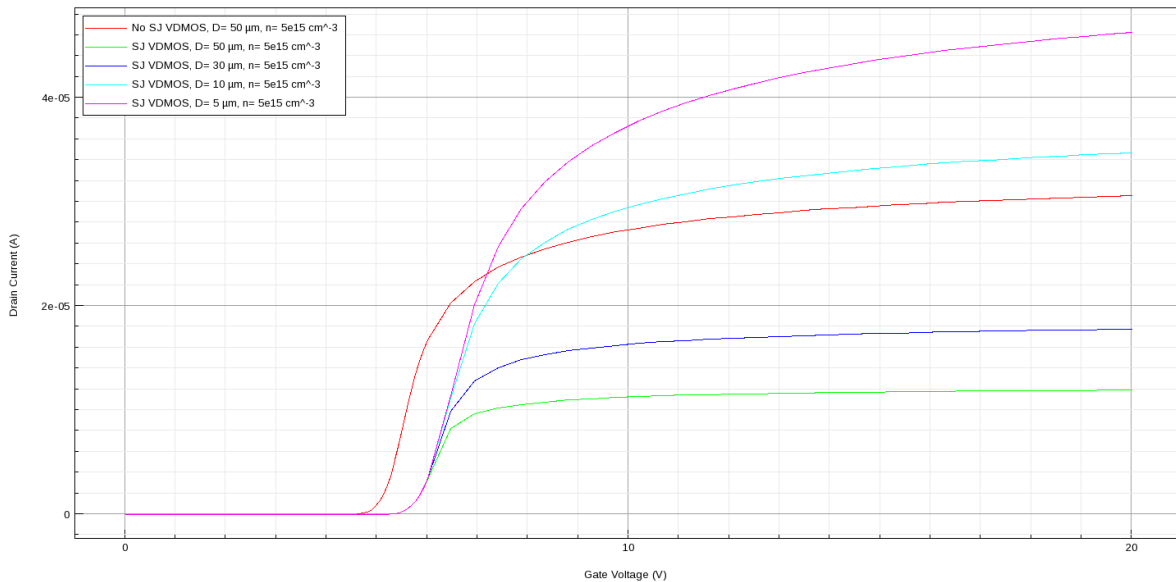


Figure 36:  $I_D$  vs  $V_G$  curve for conventional  $D=50\mu\text{m}$  (red) and superjunction  $D=50\mu\text{m}$  (green),  $D=30\mu\text{m}$  (blue),  $D=10\mu\text{m}$  (cyan),  $D=50\mu\text{m}$  (pink) VDMOS devices.

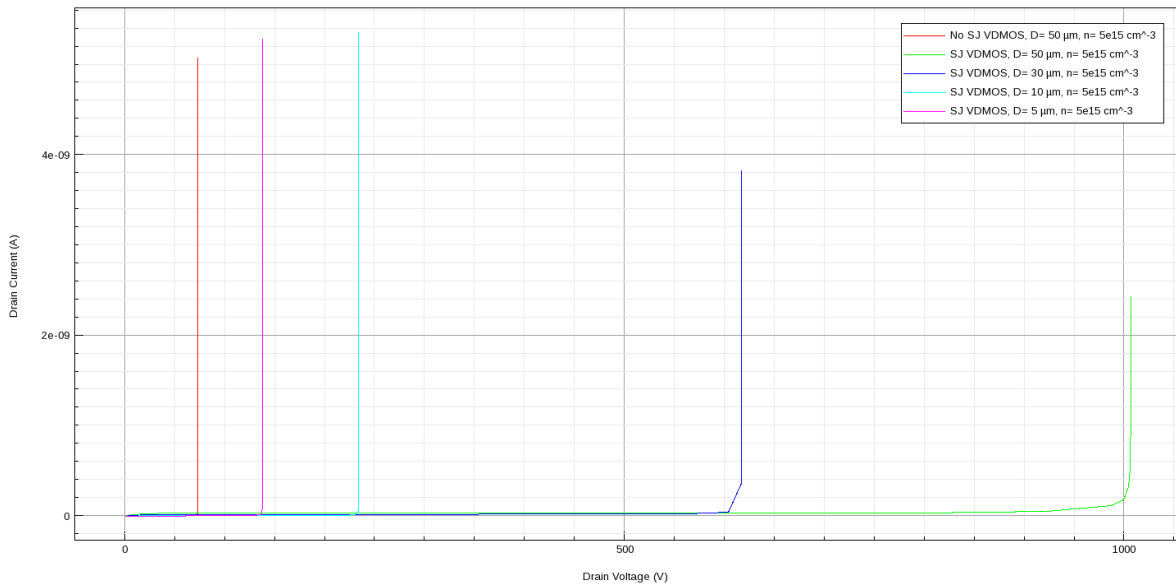


Figure 37:  $I_D$  vs  $V_D$  curve at  $V_G=0$  V for conventional  $D=50\mu\text{m}$  (red) and superjunction  $D=50\mu\text{m}$  (green),  $D=30\mu\text{m}$  (blue),  $D=10\mu\text{m}$  (cyan),  $D=50\mu\text{m}$  (pink) VDMOS devices.

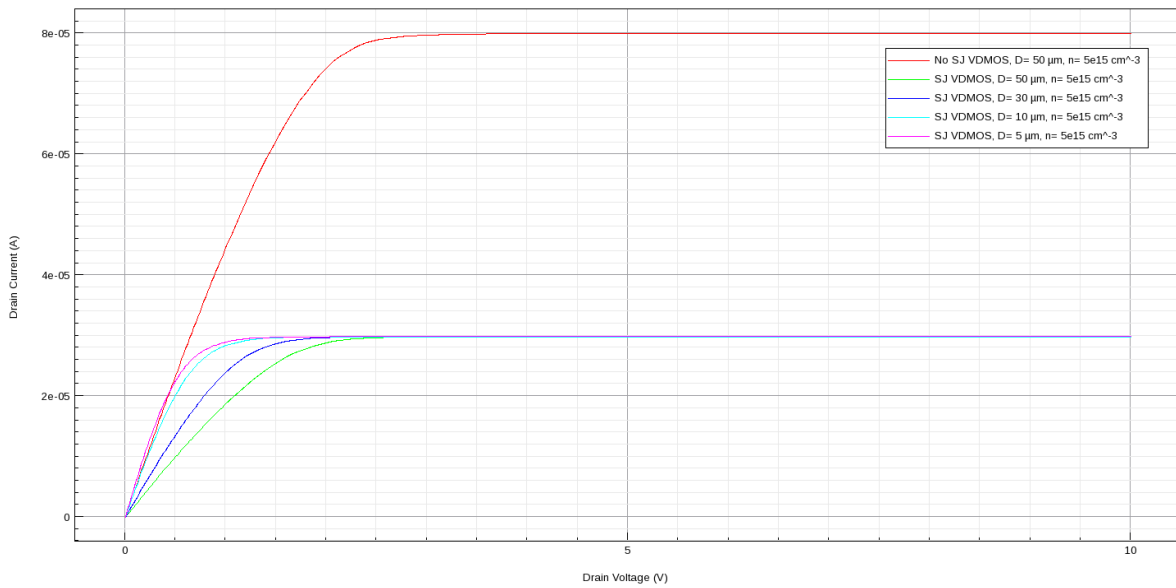


Figure 38:  $I_D$  vs  $V_D$  curve at  $V_G=0.5$  V for conventional  $D=50\mu\text{m}$  (red) and superjunction  $D=50\mu\text{m}$  (green),  $D=30\mu\text{m}$  (blue),  $D=10\mu\text{m}$  (cyan),  $D=50\mu\text{m}$  (pink) VDMOS devices.

The threshold voltage, breakdown voltage and on-resistance parameters are extracted and summarized in table 4.

Table 4: No SJ and SJ VDMOS results when decreasing superjunction depth “D”

	$n$ (cm <sup>-3</sup> )	D (μm)	V <sub>T</sub> (V)	V <sub>BR</sub> (V)	R <sub>on_sp</sub> (Ω-mm <sup>2</sup> )
No SJ	5x10 <sup>15</sup>	50	4.88	72	0.83
SJ	5x10 <sup>15</sup>	50	5.6	985	1.94
	5x10 <sup>15</sup>	30	5.6	605	1.41
	5x10 <sup>15</sup>	10	5.6	233	0.88
	5x10 <sup>15</sup>	5	5.6	136	0.75

### 4.3 Increasing Doping Concentration “n”

Next, a comparison between the conventional VDMOS structure and superjunction VDMOS is presented when increasing the doping concentration “n”. For this, the I<sub>D</sub> vs V<sub>G</sub>, I<sub>D</sub> vs V<sub>D</sub> curves are presented and the V<sub>T</sub>, BV and R<sub>DS(on)</sub> parameters are extracted.

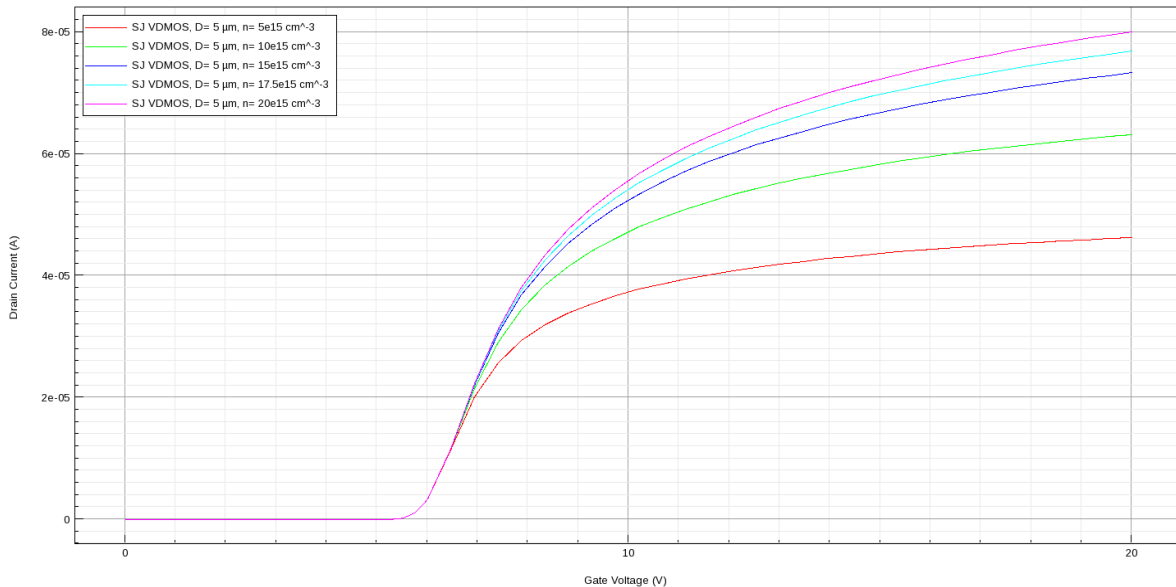


Figure 39: I<sub>D</sub> vs V<sub>G</sub> curve for superjunction n=5x10<sup>15</sup>cm<sup>-3</sup> (red), n=10x10<sup>15</sup>cm<sup>-3</sup> (green), n=15x10<sup>15</sup>cm<sup>-3</sup> (blue), n=17.5x10<sup>15</sup>cm<sup>-3</sup> (cyan), n=20x10<sup>15</sup>cm<sup>-3</sup> (pink) VDMOS.

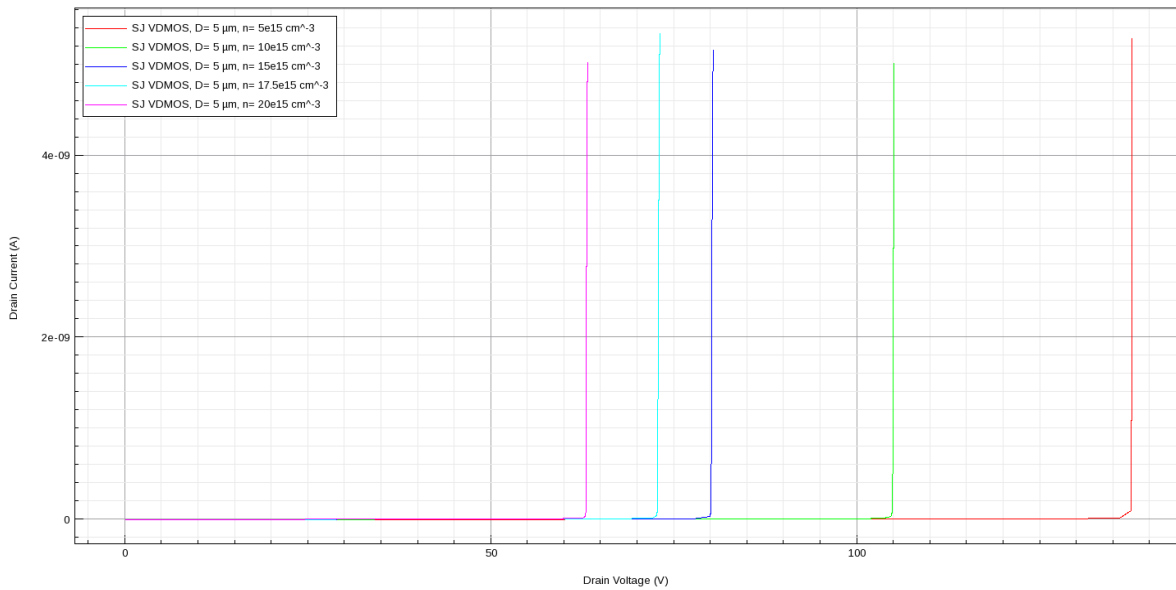


Figure 40:  $I_D$  vs  $V_D$  curve at  $V_G=0$  V for superjunction  $n=5 \times 10^{15} \text{ cm}^{-3}$  (red),  $n=10 \times 10^{15} \text{ cm}^{-3}$  (green),  $n=15 \times 10^{15} \text{ cm}^{-3}$  (blue),  $n=17.5 \times 10^{15} \text{ cm}^{-3}$  (cyan),  $n=20 \times 10^{15} \text{ cm}^{-3}$  (pink) VDMOS devices.

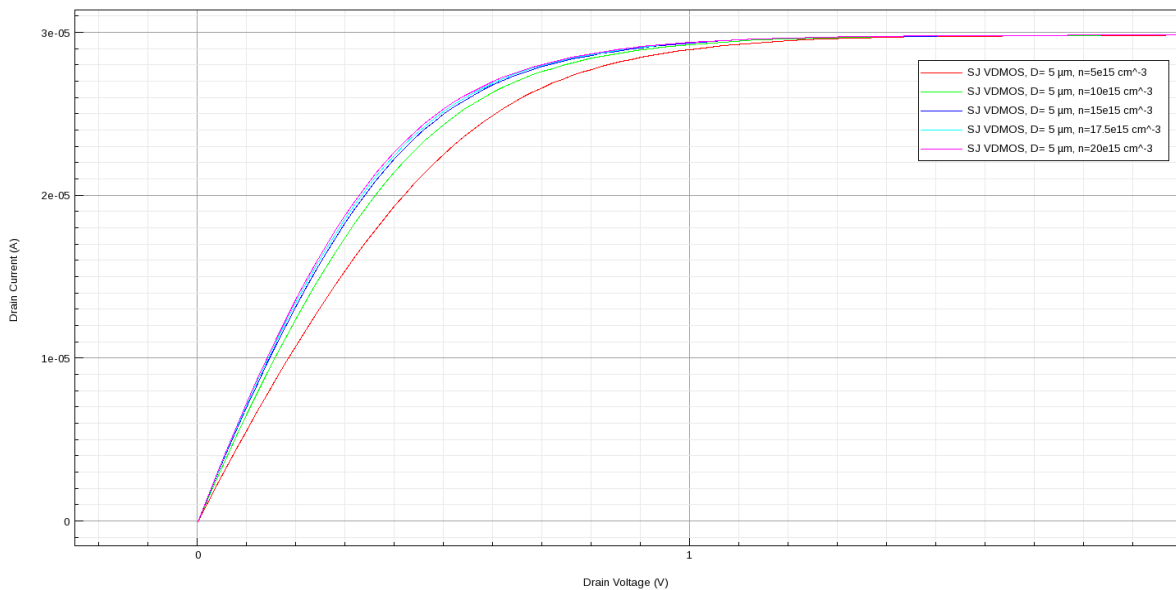


Figure 41:  $I_D$  vs  $V_D$  curve at  $V_G=0.5$  V for superjunction  $n=5 \times 10^{15} \text{ cm}^{-3}$  (red),  $n=10 \times 10^{15} \text{ cm}^{-3}$  (green),  $n=15 \times 10^{15} \text{ cm}^{-3}$  (blue),  $n=17.5 \times 10^{15} \text{ cm}^{-3}$  (cyan),  $n=20 \times 10^{15} \text{ cm}^{-3}$  (pink) VDMOS devices.

The threshold voltage, breakdown voltage and on-resistance parameters are extracted and summarized in table 5.

Table 5: No SJ and SJ VDMOS results when increasing doping concentration “n”

	$n$ (cm <sup>-3</sup> )	D (μm)	V <sub>T</sub> (V)	V <sub>BR</sub> (V)	R <sub>on_sp</sub> (Ω·mm <sup>2</sup> )
No SJ	5x10 <sup>15</sup>	50	4.88	72	0.83
SJ	5x10 <sup>15</sup>	5	5.6	136	0.75
	10x10 <sup>15</sup>	5	5.6	104	0.66
	15x10 <sup>15</sup>	5	5.6	79.8	0.63
	17.5x10 <sup>15</sup>	5	5.6	72.5	0.61
	20x10 <sup>15</sup>	5	5.6	62.8	0.60

#### 4.4 Final Optimized Device “n”

Next, the final optimized VDMOS device and a summary of the previous structures is presented. For this, the I<sub>D</sub> vs V<sub>G</sub>, I<sub>D</sub> vs V<sub>D</sub> curves are shown and the V<sub>T</sub>, BV and R<sub>DS(on)</sub> parameters are extracted.

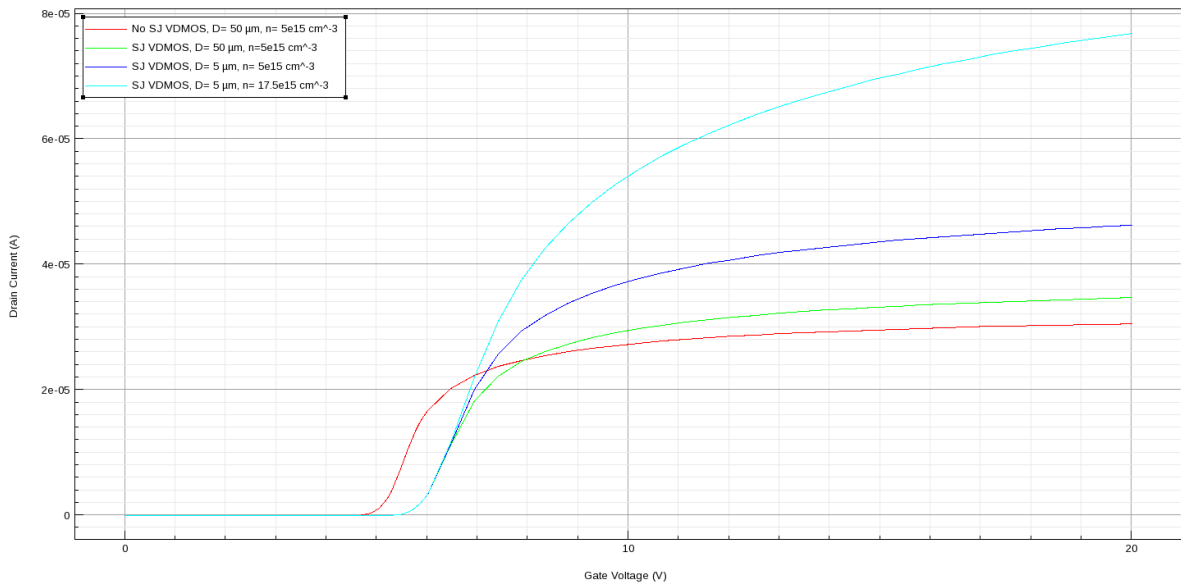


Figure 42: I<sub>D</sub> vs V<sub>G</sub> curve for conventional D=50μm n=5x10<sup>15</sup> cm<sup>-3</sup> (red) and superjunction D=50μm n=5x10<sup>15</sup> cm<sup>-3</sup> (green), D=5μm n=5x10<sup>15</sup> cm<sup>-3</sup> (blue), D=5μm n=17.5x10<sup>15</sup> cm<sup>-3</sup> (cyan) VDMOS devices.

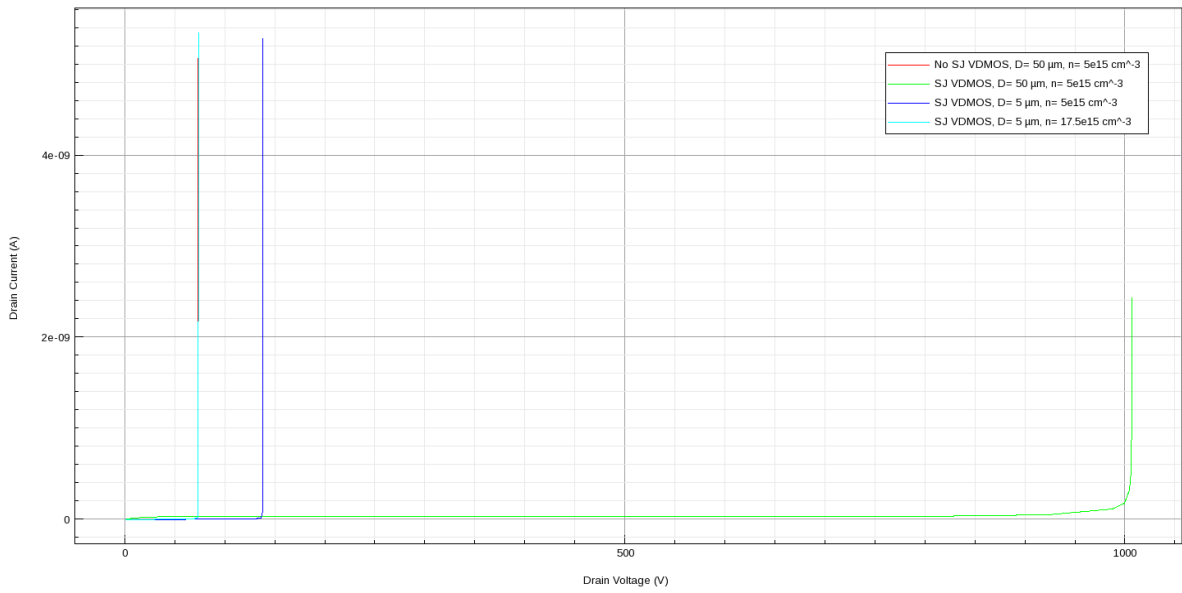


Figure 43:  $I_D$  vs  $V_D$  curve at  $V_G=0$  V for conventional  $D=50\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (red) and superjunction  $D=50\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (green),  $D=5\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (blue),  $D=5\mu\text{m}$   $n=17.5 \times 10^{15} \text{ cm}^{-3}$  (cyan) VDMOS devices.

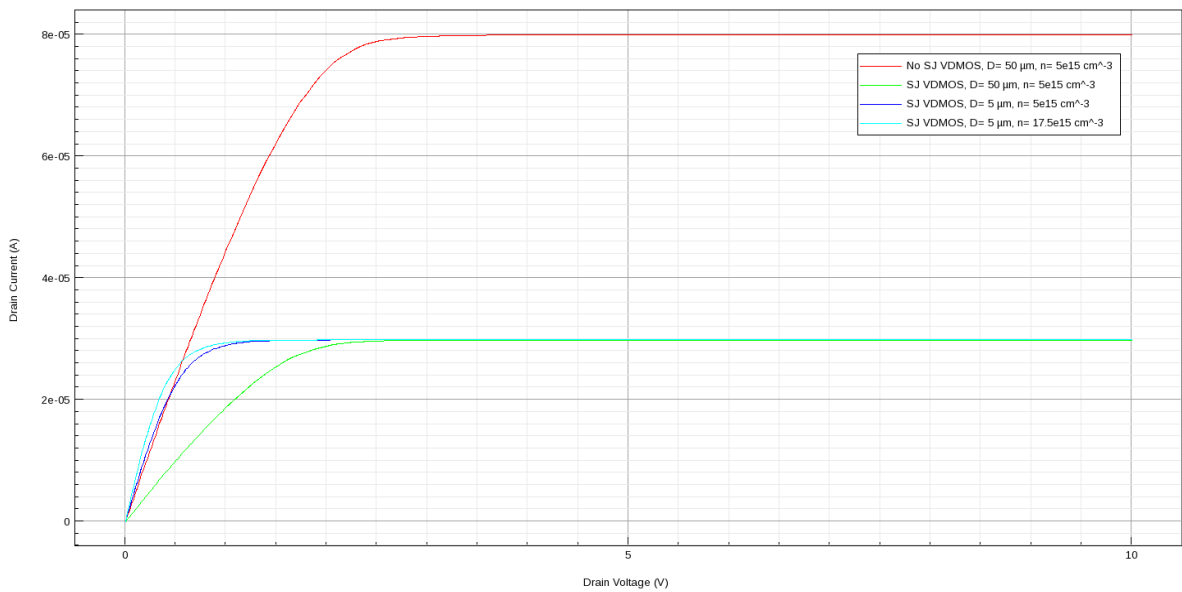


Figure 44:  $I_D$  vs  $V_D$  curve at  $V_G=0.5$  V for conventional  $D=50\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (red) and superjunction  $D=50\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (green),  $D=5\mu\text{m}$   $n=5 \times 10^{15} \text{ cm}^{-3}$  (blue),  $D=5\mu\text{m}$   $n=17.5 \times 10^{15} \text{ cm}^{-3}$  (cyan) VDMOS devices.

The threshold voltage, breakdown voltage and on-resistance parameters are summarized in table 6.

Table 6: No SJ and SJ VDMOS summarized final results.

	$n$ (cm <sup>-3</sup> )	$D$ (μm)	$V_T$ (V)	$V_{BR}$ (V)	$R_{on\_sp}$ (Ω-mm <sup>2</sup> )
No SJ	$5 \times 10^{15}$	50	4.88	72	0.83
SJ	$5 \times 10^{15}$	50	5.6	985	1.94
	$5 \times 10^{15}$	5	5.6	136	0.75
	$17.5 \times 10^{15}$	5	5.6	72.5	0.61

From the previous plots and tables, the following can be said:

- The threshold voltage remained practically the same throughout the conventional and all the superjunction device modifications. This is a result of only modifying the drift region but not modifying the gate charge nor the gate dimensions.

- The superjunction main advantage was that it allowed a huge increase of the breakdown voltage, almost 10 times the conventional one even though the on-resistance was increased too. This is the reason why the next step was a trade-off between the  $V_{BR}$  and the  $R_{on\_sp}$ .

- Decreasing the drift region depth “D” led to a decrease in the breakdown voltage and the on-resistance. The pillar depth was decreased just enough as to obtain a smaller on-resistance than the conventional device. This was accomplished and an improved device was obtained, but it can be further be improved by increasing the doping concentration.

- Increasing the drift region doping concentration led again to a decrease in breakdown voltage and on-resistance. Managing this trade-off is how the device was optimized to its best point of operation.

#### 4.5 Conventional vs Superjunction Electric Field Profiles

As seen in chapter 2 and 3, the electric field can be analyzed as follows.

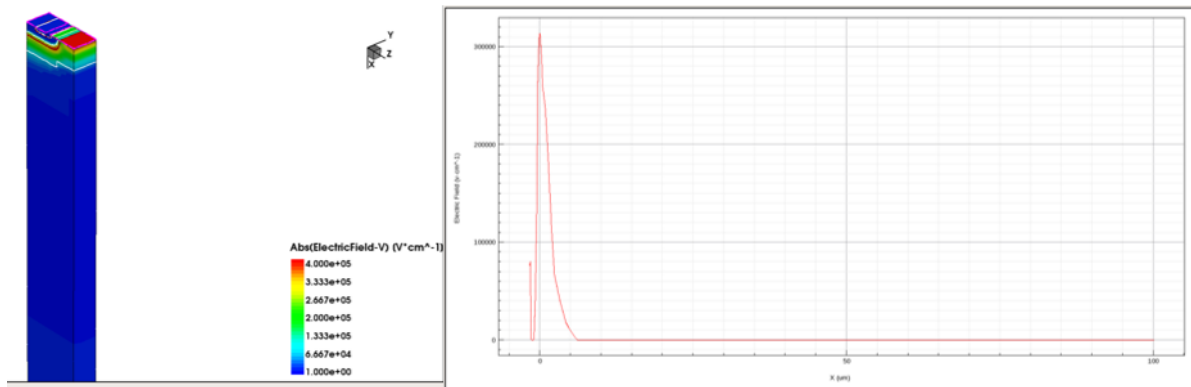


Figure 45: Electric field distribution during breakdown in the device (left) and throughout the x dimension (right) for the conventional device.

From the conventional device, it can be seen that the electric field remains at the very top of the drift region. When looking at the electric field curve, the triangular shape appears as to be expected. Thus, the area under the curve would represent the breakdown voltage, since the profile was obtained at  $V_G=0$  V and during breakdown.

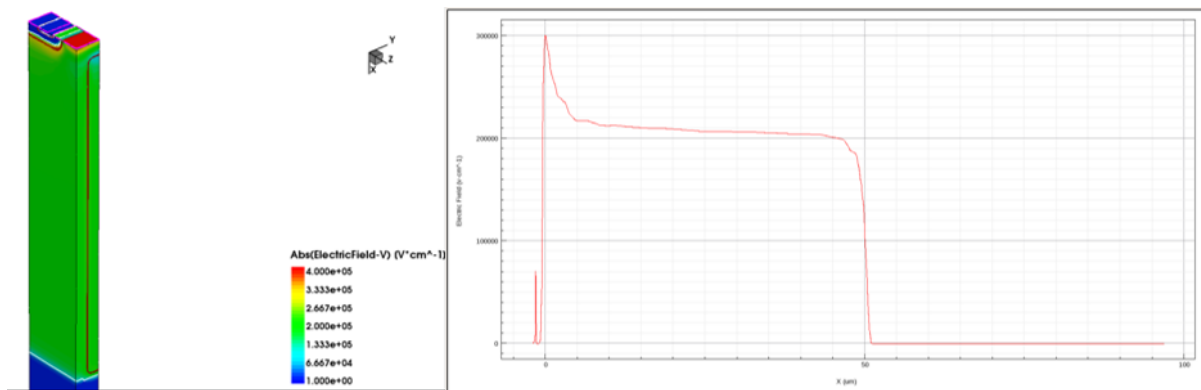


Figure 46: Electric field distribution during breakdown in the device (left) and throughout the x dimension (right) for the superjunction structure.

From the superjunction device, it can be seen the electric field is relatively constant and distributed throughout the drift region. The area under the electric field curve would be the breakdown voltage and it can be clearly seen that it is considerably bigger than the conventional case.



#### 4.6 Conclusions

- By modifying the superjunction drift region dimensions and doping, an optimized device is obtained, as long as charge balance is accomplished and the electric field distribution is well distributed through the drift region.

- The trade-off between breakdown voltage and on-resistance is always present, but the superjunction structure makes the relationship easier to handle. That is the relation between on-resistance and breakdown voltage in conventional devices is power to the 2.5, whereas in superjunction devices it becomes linear ideally.

- The superjunction structure works better at high voltages. In order to be used at lower voltage applications like in the present work (in the range of 70 V), an alternative route was used contrary to what the superjunction theory suggests. The drift region depth was reduced significantly first and then doping was increased.

- Looking at the electric field profiles clearly proves the superjunction theory. It can be seen how the superjunction drift region distributes the electric field throughout the drift region so that the breakdown voltage increases tremendously.

- By reducing the drift region depth 10 times and then increasing the doping 3.5 times, the VDMOS transistor accomplished a 26% on-resistance reduction (going from 0.83 to 0.61  $\Omega\text{-mm}^2$ ) while keeping the same breakdown voltage as the conventional device (72V).

**APPENDIX:  
SENTAURUS CODE**

The cmd file/sentaurus code used to build the VDMOS transistor is here.

```

#-----#
# Numerics controls
#-----#

AdvancedCalibration
#rem # PARALLEL simulation strategy and unified coordinate system
math numThreads= 4
math coord.ucs

#rem # Initial pdb settings to optimize simulation run-time
pdbSet          Diffuse      MaxGrowthStep          100.0
pdbSet          Diffuse      IncreaseRatio           5.0
pdbSet          Diffuse      InitTimeStep            1.0
pdbSet          Diffuse      delT                    50.0
pdbSet          Si          Dopant                    DiffModel
ChargedFermi
pdbSet          Mechanics   EtchDepoRelax           0

#rem # Initialize DRAM Dimension
fset           D           @D@;          # Drift region length/depth
fset           W           @W@;          # Drift region width
fset           PW          @PW@;        # Super-junction pitch width
fset           left       0.0
fset           right      [expr $PW/2.0]
fset           back       0.0
fset           front      [expr $W/2.0]
fset           Lpwell      [expr 0.6*$W]; # p-type well length
fset           Lgate       [expr 0.5*$W]; # Gate length

line           x location= 0.0<um>      tag= top
line           x location= $D<um>
line           x location= 100<um>      tag= bottom

line           y location= $left<um>     tag= left
line           y location= $right<um>    tag= right

line           z location= $back<um>     tag= back
line           z location= $front<um>    tag= front

region                Silicon xlo= top xhi= bottom ylo= left yhi= right zlo= back
zhi= front substrate
init                  Silicon concentration= 1e10 field= Boron wafer.orient= 100

```

```

pdbSet Grid SnMesh min.normal.size 0.1

refinebox name= Active_1 Silicon min= "[expr $D-2.0] $left $back" max=
"[expr $D+0.1] $right $front" xrefine= "0.25"
refinebox name= Active_2 Silicon min= "-0.55 $left $back" max= "1.0
$right $front" xrefine= "0.25" yrefine= "@<PW/16.0>@"

refinebox name= Active_3 Silicon min= "-0.5 [expr ( 0.24+0.0)*$PW] $back"
max= "[expr $D+0.5] [expr ( 0.26+0.0)*$PW] $front" yrefine= "@<PW/16.0>@"

refinebox name= Active_4 Silicon min= "-2.0 $left $back" \
max= " 0.0 $right [expr $back+0.50*$Lpwell+2.0]" xrefine= "0.2"
zrefine= "0.4"
refinebox name= Active_5 Silicon min= "-2.0 $left [expr
$back+0.50*$Lpwell]" \
max= " 0.0 $right [expr $back+0.50*$Lpwell+2.0]" zrefine= "0.2"

select z= "(x>$D)?1e18:@Cp@" Silicon name= Phosphorus store; ##
Cp = the pillar doping concentration

#if @<SJ==1>@
deposit oxide thickness= 1.0<um> isotropic

struct tdr= 1

polygon name= pwell_1 rectangle min= "$left [expr
$back+0.0*$W+0.50*$Lpwell]" max= "$right [expr $back+1.0*$W-0.50*$Lpwell]"
mask name= pwell polygons= [list pwell_1] negative
photo mask= pwell thickness= 3.0<um>
strip photoresist

polygon name= ppillar_1 rectangle min= "[expr (-0.25+0.0)*$PW] $back"
max= "[expr ( 0.25+0.0)*$PW] $front"
mask name= ppillar polygons= [list ppillar_1] negative
photo mask= ppillar thickness= 3.0<um>

struct tdr= 2

etch oxide thickness= 2.0<um> anisotropic
etch silicon trapezoidal thickness= $D angle= 90
strip photoresist

struct tdr= 3

```

```

diffuse      thick= [expr 0.125*$PW]<um> temperature= 1000<C> time=
100.0<min> epi epi.doping= {Boron = @Cp@} epi.layers= 10 epi.model= 1

struct tdr= 4

diffuse      thick= [expr 0.15*$PW]<um> temperature= 1000<C> time=
100.0<min> epi epi.doping= {Boron = @Cp@} epi.layers= 10 epi.model= 1

struct tdr= 5

etch        silicon cmp coord= 0.0

struct tdr= 6

strip       oxide
#endif

struct tdr= 7

diffuse      thick= 2.0<um> temperature= 800<C> time= 100.0<min> epi
epi.doping= {Phosphorus = 1e16} epi.layers= 5

deposit      oxide thickness= 0.1<um> isotropic

#-----#
#split      PWell
#-----#

#line       z location= $back<um> tag= back
#line       z location= $front<um> tag= front

#refinebox  name= Active_4 Silicon min= "-2.0 $left $back" \
#           max= " 0.0 $right [expr $back+0.50*$Lpwell+2.0]" xrefine= "0.2"
zrefine= "0.4"
#refinebox  name= Active_5 Silicon min= "-2.0 $left [expr
$back+0.50*$Lpwell]" \
#           max= " 0.0 $right [expr $back+0.50*$Lpwell+2.0]" zrefine= "0.2"

polygon     name= pwell_1 rectangle min= "$left [expr
$back+0.0*$W+0.50*$Lpwell]" max= "$right [expr $back+1.0*$W-0.50*$Lpwell]"
mask name= pwell polygons= [list pwell_1] negative
photo mask= pwell thickness= 3.0<um>

struct tdr= 8

implant     boron dose= 2.5e13<cm-2> energy= 260<keV> tilt= 0 rotation= 0
implant     boron dose= 2.5e13<cm-2> energy= 60<keV> tilt= 0 rotation= 0

```

```

strip    photoresist

struct tdr= 9

    temp_ramp name=  welldrv  temp=  700<C>    ramprate=  (1100.0-
700.0)/100.0<C/min> time= 100.0<min>
    temp_ramp name=  welldrv temp= 1100<C> ramprate= 0.0          time=
100.0<min>
    temp_ramp name=  welldrv  temp=  1100<C>    ramprate=  (700.0-
1100.0)/150.0<C/min> time= 150.0<min>
    diffuse    temp_ramp= welldrv

#-----#
#split      Gate
#-----#

strip      oxide
deposit    oxide thickness= 0.05<um> isotropic
deposit    poly thickness= 2.0<um> isotropic

struct tdr= 10

polygon    name= gate_1      rectangle  min=    "$left  [expr
$back+0.0*$W+0.50*$Lgate]" max= "$right [expr $back+1.0*$W-0.50*$Lgate]"
mask      name= gate  polygons= [list gate_1] negative
photo     mask= gate  thickness= 3.0<um>

struct tdr= 11

etch      poly thickness= 4.0<um> anisotropic
strip    photoresist

struct tdr= 12

    temp_ramp name=  gate  temp=    700.0<C>    ramprate=  (1000.0-
700.0)/90.0<C/min> time= 90.0<min>
    temp_ramp name=  gate temp= 1000.0<C> ramprate=          0.0<C/min>
time= 25.0<min>
    temp_ramp name=  gate temp= 1000.0<C> ramprate=          0.0<C/min>
time= 30.0<min>
    temp_ramp name=  gate temp= 1000.0<C> ramprate=          0.0<C/min>
time= 60.0<min>
    temp_ramp name=  gate  temp=    1000.0<C>    ramprate=  (700.0-
1000.0)/120.0<C/min> time= 120.<min>
    diffuse    temp_ramp= gate

```

```

#-----#
#split      Nplus
#-----#

refinebox   name= Active_6 Silicon min= "-2.0 $left $back" max= " -1.5 $right
[expr $back+0.0*$W+0.50*$Lpwell+2.0]" xrefine= "0.1" zrefine= "0.1"
refinebox   name= Active_7 Silicon min= "-2.0 $left [expr $back+$Lgate/2.0-
0.55]" \
max= "-1.5 $right [expr $back+$Lgate/2.0+0.55]" xrefine= "0.05"
zrefine= "0.05"

fset      Lnplus      [expr $Lgate-($W-$Lgate)*0.6]
polygon   name= nplus_1  rectangle      min=      "$left      [expr
$back+0.0*$W+0.50*$Lnplus]" max= "$right [expr $back+1.0*$W-0.50*$Lnplus]"
mask      name= nplus    polygons= [list nplus_1]
photo     mask= nplus    thickness= 3.0<um>

struct tdr= 13

implant   arsenic  dose= 2e15<cm-2> energy= 100<keV> tilt= 0 rotation=
0
implant   phosphorus dose= 1e15<cm-2> energy= 100<keV> tilt= 0
rotation= 0
strip     photoresist

struct tdr= 14

temp_ramp name=  nplusdrv  temp=  700<C>    ramprate=  (1050.0-
700.0)/0.25<C/min> time= 0.25<min>
temp_ramp name=  nplusdrv  temp= 1050<C> ramprate=      0.00<C/min>
time= 1.00<min>
temp_ramp name=  nplusdrv  temp=  1050<C>    ramprate=  (700.0-
1050.0)/0.42<C/min> time= 0.42<min>
diffuse   temp_ramp= nplusdrv

#-----#
#split      Pplus
#-----#

fset      Lpplus      [expr $Lgate-($W-$Lgate)*0.6]

polygon   name= pplus_1  rectangle      min=      "$left      [expr
$back+0.0*$W+0.50*$Lpplus]" max= "$right [expr $back+1.0*$W-0.50*$Lpplus]"
mask      name= pplus    polygons= [list pplus_1] negative
photo     mask= pplus    thickness= 3.0<um>

struct tdr= 15

```

```

implant      boron dose= 2e15<cm-2> energy= 30<keV> tilt= 0 rotation= 0
strip      photoresist

struct tdr= 16

temp_ramp name=  pplusdrv  temp=    700<C>  ramprate=  (1000.0-
700.0)/0.20<C/min> time= 0.20<min>
temp_ramp name=  pplusdrv  temp=  1000<C>  ramprate=          0.0<C/min>
time= 1.00<min>
temp_ramp name=  pplusdrv  temp=  1000<C>  ramprate=  (700.0-
1000.0)/0.37<C/min> time= 0.37<min>
diffuse      temp_ramp= pplusdrv

#-----#
#split BackEnd
#-----#

etch      oxide thickness= 1.0<um> anisotropic

deposit   Metal thickness= 1.0<um> isotropic

struct tdr= 17

polygon   name=      source_1      rectangle min=  "$left [expr
$back+0.0*$W+0.50*$Lgate-1.0]" max=  "$right [expr  $back+1.0*$W-
0.50*$Lgate+1.0]"
mask      name= source1      polygons= [list source_1]
photo     mask= source1      thickness= 3.0<um>

struct tdr= 18

etch      Metal thickness= 5.0<um> anisotropic
strip     photoresist
etch      Metal cmp coord= -2.5

#-----#
#split Mesh
#-----#

# clear the process simulation mesh
line      clear
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines

```



```

# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh min.normal.size 1.0

refinebox name= Substrate refine.max.edge= "100.0 100.0 100.0"
refine.min.edge= "0.1 @<PW/32.0>@ 0.1" \
    refine.fields= {NetActive} def.max.asinhdiff= 1.0 adaptive Silicon
refinebox name= Channel_Interface min.normal.size= 0.05
normal.growth.ratio= 1.5 interface.materials= {Silicon}

grid remesh

# assign contacts
contact name= "source" point Metal x= -2.3 y= 0.1 z= [expr
$back+0.0*$W+0.5]
contact name= "drain" bottom Silicon
contact name= "gate" point PolySilicon x= -2.5 y= 0.1 z= [expr
$back+0.5*$W-0.5]

struct tdr= n@node@ !gas

exit

```

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