2017

Advanced Control Techniques for Efficiency and Power Density Improvement of a Three-Phase Microinverter

Seyed Milad Tayebi
University of Central Florida

ADVANCED CONTROL TECHNIQUES FOR EFFICIENCY AND POWER DENSITY IMPROVEMENT OF A THREE-PHASE MICROINVERTER

by

SEYED MILAD TAYEBI
B.S. Babol University of Technology, 2009
M.S. Iran University of Science and Technology, 2011

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Summer Term
2017

Major Professor: Issa Batarseh

ABSTRACT

Inverters are widely used in photovoltaic (PV) based power generation systems. Most of these systems have been based on medium to high power string inverters. Microinverters are gaining popularity over their string inverter counterparts in PV based power generation systems due to maximized energy harvesting, high system reliability, modularity, and simple installation. They can be deployed on commercial buildings, residential rooftops, electric poles, etc and have a huge potential market. Emerging trend in power electronics is to increase power density and efficiency while reducing cost. A powerful tool to achieve these objectives is the development of an advanced control system for power electronics.

In low power applications such as solar microinverters, increasing the switching frequency can reduce the size of passive components resulting in higher power density. However, switching losses and electromagnetic interference (EMI) may increase as a consequence of higher switching frequency. Soft switching techniques have been proposed to overcome these issues.

This dissertation presents several innovative control techniques which are used to increase efficiency and power density while reducing cost. Dynamic dead time optimization and dual zone modulation techniques have been proposed in this dissertation to significantly improve the microinverter efficiency. In dynamic dead time optimization technique, pulse width modulation (PWM) dead times are dynamically adjusted as a function of load current to minimize MOSFET body diode conduction time which reduces power dissipation. This control method also improves total harmonic distortion (THD) of the inverter output current. To further improve the microinverter efficiency, a dual-zone modulation has been proposed which introduces one more

soft-switching transition and lower inductor peak current compared to the other boundary conduction mode (BCM) modulation methods.

In addition, an advanced DC link voltage control has been proposed to increase the microinverter power density. This concept minimizes the storage capacitance by allowing greater voltage ripple on the DC link. Therefore, the microinverter reliability can be significantly increased by replacing electrolytic capacitors with film capacitors. These control techniques can be readily implemented on any inverter, motor controller, or switching power amplifier. Since there is no circuit modification involved in implementation of these control techniques and can be easily added to existing controller firmware, it will be very attractive to any potential licensees.

To my family

Faeze Mohamadi, Mohsen Tayebi,

Shima Tayebi, and Mona Tayebi

ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my advisor, Dr. Issa Batarseh, for his kind support and inspiration to my research work throughout my studies and research at the Florida Power Electronics Center (FPEC). I would also like to thank him for giving me great freedom to pursue independent work.

I would like to thank Dr. Kalpathy B. Sundaram, Dr. Nasser Kutkut, Dr. Wasfy B. Mikhael and Dr. Wei Sun for serving as my committee members, and for their constructive comments and kind suggestions.

I would like to express my deep gratitude to Mr. Charles Jourdan who patiently guided me to the area of the power converters and kindly gave me insightful suggestions throughout my studies and research.

I would also like to thank Dr. Nasser Kutkut and Dr. Haibing Hu for all the advice they have given me to improve my research study.

I would also like to thank the research group at the FPEC, Siddhesh Shinde, Xi Chen, Anirudh Pise, Mahmood Alharbi, Michael Pepper and Christopher Hamilton for their support and intellectual discussions.

At the end, I would like to thank my parents, Faeze Mohamadi and Mohsen Tayebi, for all the love and support they have given me throughout my life. I would also like to thank my sisters, Mona and Shima, for their kind advice and motivations in my life and research work.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1. INTRODUCTION

1.1 Background and Challenges

Among renewable energy sources, solar energy has gained considerable attention in recent years [1], [2]. In order to convert this source of energy into electricity and inject it into the utility grid, power converters with high efficiency and power density need to be developed. There are three basic architectures for photovoltaic (PV) solar systems; centralized inverter, string inverter and microinverter. PV microinverter architecture is the fastest growing technology due to its advantages such as enhanced energy harvesting, high reliability, and simple installation. Microinverters with typical power levels from 200 W to 400 W can be directly mounted on the back of the PV panels.

Emerging trend in power electronics is to increase power density and efficiency of the microinverters while reducing cost. Employing high switching frequency and soft switching techniques reduce cost by reducing the size of passive components and improve efficiency by decreasing switching losses. Soft switching can be improved by minimizing MOSFET body diode conduction time. In order to achieve high power conversion efficiency and power density, a comprehensive investigation and research have been conducted on new topologies and control techniques.

1.2 Microinverter Efficiency Improvement using Dead Time Optimization

Figure 1-1 depicts a single-phase half-bridge inverter with a controller providing duty cycles and dead times for the MOSFETs. The inverter MOSFET gates are driven by alternating PWM signals

so that when one MOSFET is on, the other is off. Dead time is the state where both MOSFETs are off and one MOSFET's body diode is conducting. Since body diode conduction losses are higher than MOSFET conduction losses, efficiency is maximized when body diode conduction time is small. Body diode conduction time is directly proportional to dead time, therefore it is advantageous to select a dead time value that minimizes body diode conduction time without resulting in shoot-through current.

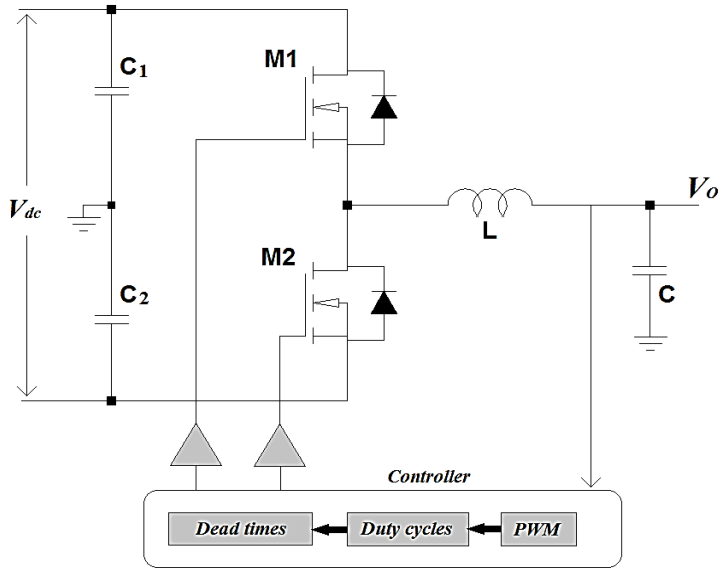


Figure 1-1: Single-phase half-bridge inverter with the corresponding controller.

Excessive dead time can also have a negative impact on inverter efficiency especially at higher operating frequencies where it is a large percentage of the conduction time.

Typically, a fixed dead time is determined based on the worst-case operating conditions such as load, voltage and temperature variations. The body diode conduction loss can be approximated as follows:

$$P_{loss,BD} \approx V_{DS}.I_L.(t_{d1} + t_{d2}).f_{sw} \qquad (1\text{-}1)$$

where, V_{DS} is drain to source voltage or the diode forward voltage drop, I_L is inductor current during the dead times, t_{d1} and t_{d2} are turn-on and turn-off dead times, respectively and f_{sw} is switching frequency. Referring to equation (1-1), it can be seen that excessive dead time increases the body diode conduction loss due to the diode's forward voltage drop.

A number of research papers on PWM dead time optimization for various buck derived topologies have been published [3]-[13].

Switching current sensing was proposed in [3] for buck converters to measure the current flowing through the synchronous MOSFET and detect shoot-through current. When shoot-through occurs, the dead times must be increased. However, this method requires high bandwidth sensors for current measurement which makes its implementation difficult and adds cost.

Switching voltage sensing is sub-divided into the adaptive [4]-[6] and predictive [7]-[9] types. Adaptive control measures the switching voltage across the synchronous rectifier and adjusts the dead times accordingly. Predictive control uses the information from the previous switching cycle to adjust the dead times in the current cycle. Although the experimental results show a significant reduction in body diode losses, these control methods require additional circuit components which drive cost up and decrease reliability. Therefore, sensorless optimization methods have been proposed that do not require additional components.

Sensorless dead time optimization for dc-dc converters was proposed in [10] based on maximum power point tracking (MPPT). This method optimizes the dead time by indirectly measuring the efficiency of the converter. Another sensorless dead time optimization method proposed in [11] optimizes the efficiency by minimizing the duty cycle in dc-dc converters. This method is able to

optimize both turn-on and turn-off dead times. A perturb and observe algorithm (P&O) was proposed in [12] to detect dead time resulting in maximum efficiency.

Several methods have been proposed to overcome the dead time issues in inverters. A correlation-based control technique was introduced in [13] to optimize dead time in motor drive inverters. The algorithm dynamically minimizes the input current resulting in minimum power loss. The technique proposed in [14] compensates for the effect of dead time by adjusting the switching frequency in sinusoidal pulse-width-modulated voltage-source inverters. Another dead time compensation method was presented in [15] based on harmonic analysis and filtering of the voltage distortion produced by dead time effects by adding a predetermined compensation signal to the voltage reference in ac motor drives. However, this method requires extra components which increases the cost and circuit complexity.

The method introduced in [16] improves THD and the magnitude of the inverter output voltage by preventing the unnecessary dead time. Another switching strategy for PWM power converters was proposed in [17] on the basis of using independent on/off switching action according to the current polarity. As long as the current polarity does not change, the dead time is not needed. These methods can be affected by detection circuit delay, harmonics and A/D converter errors.

A dynamic dead time optimization technique is proposed and will be discussed in the next chapter of this dissertation wherein the PWM dead times are calculated by sensing the grid voltage which is also used for duty cycle calculation.

1.3 Boundary Conduction Mode Soft-Switching Techniques

In most soft-switching techniques, resonant circuits or auxiliary components are used to achieve zero voltage switching (ZVS) or zero current switching (ZCS). These additional auxiliary components and switches will reduce reliability and add cost to the inverter design. These techniques can be basically classified into dc-side and ac-side topologies.

In dc-side topologies, the auxiliary circuits are placed between the input dc power supply and main bridges. One-switch clamped resonant DC link [18], passive clamped using the couple inductors [19], and one-switch resonant inverter [20], [21] have been proposed to achieve soft switching. However, these topologies suffer from voltage stress and reliability issues. Parallel resonant DC link techniques have been proposed in [22], [23] which require large active component count.

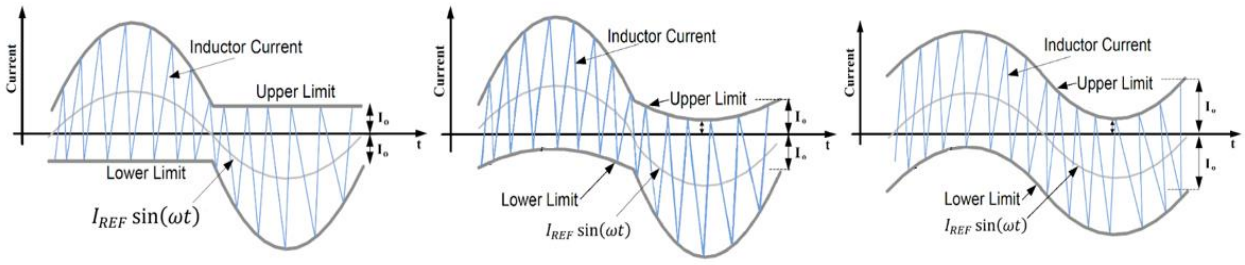
AC-side topologies are used for high-power applications where the auxiliary circuits are placed on the ac side of the main power bridge. These techniques are classified into zero-voltage transition (ZVT) and zero-current transition (ZCT). Topologies such as ZVT inverter with coupled inductor feedback [24], [25] and three auxiliary switches [26], [27] have been proposed in this category. However, they are not suitable for practical implementation due to their circuit and control complexity. ZCT topologies are typically used in high-power inverters where diode reverse recovery and turn-off losses are dominant. ZCT inverter topologies with three [28] and six [29]-[31] auxiliary switches have been introduced which maintain low voltage stress across diodes and switches. However, cost, control and circuit complexity are the main disadvantages.

The above mentioned soft-switching techniques require additional components and auxiliary devices which reduce reliability and add cost and control complexity to the inverter design.

To solve these issues, several boundary conduction mode (BCM) modulation methods have been proposed that can achieve soft switching without the need for additional components or analog circuits.

ZVS BCM peak current control is a promising soft switching candidate for low power applications where the switching losses are usually dominant [32]-[34]. For this purpose, three different peak current mode control methods have been introduced in [35]: BCM with fixed reverse current, BCM with variable reverse current, and BCM with fixed bandwidth. In these modulation methods, the inductor current is bidirectional during switching cycle to achieve turn-on ZVS. Although BCM control results in increased rms current, conduction losses and core losses when compared to continuous-conduction mode (CCM), switching losses are greatly reduced.

Figure 1-2 shows these three BCM modulation methods where the inductor current is reversed during each switching cycle to achieve turn-on ZVS for each switch.



(a) (b) (c)

Figure 1-2: Three ZVS BCM modulation methods: (a) fixed reverse current, (b) variable reverse current, (c) fixed band width.

In order to further improve efficiency, a new BCM modulation technique is proposed in this dissertation that introduces one more soft-switching transition and lower inductor peak current compared to the three mentioned BCM modulation methods.

1.4 DC Link Voltage Control Techniques

Figure 1-3 shows a common two-stage microinverter topology. This topology which connects the PV panel to the grid consists of a DC/DC converter and a DC/AC inverter along with a decoupling (DC link) capacitor in between the two stages. Typically, the first stage provides a maximum power point tracking (MPPT) function for the PV panel and boosts its low voltage to a constant DC link voltage.

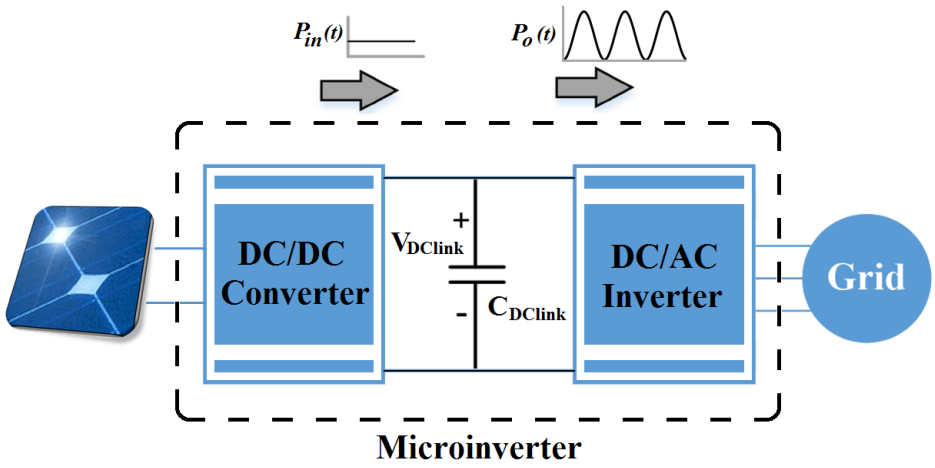


Figure 1-3: Two-stage microinverter topology.

Figure 1-4 shows a typical DC link voltage control system. In a two-stage microinverter, the DC link voltage control continually senses the DC link voltage and compares it with an average voltage reference so that the compensator loop regulates the inverter output current accordingly. Presence of large voltage ripple on the DC link capacitor introduces large ripples in the DC link voltage sense path to the controller and consequently in the inverter output current if it is not filtered by the DC link voltage control loop. There exists two approaches in order to mitigate this effect: 1) Large values of DC link capacitors are often employed to attenuate DC link voltage ripple. This requires the use of electrolytic capacitors that suffer from limited lifetime and poor reliability, or

high value polypropylene film capacitors that are expensive and bulky which reduces power density and increases cost. 2) An alternative method is to use analog or digital filters to attenuate harmonic distortion in the inverter output current caused by the DC link voltage ripple. In the case of high peak-to-peak voltage ripple on the DC link, an analog filter requires a very high attenuation at low frequencies which results in lower loop bandwidth. Therefore, an analog low-pass filter placed in the DC link voltage sense path will exhibit poor transient response as well as adding cost to the design. Digital low-pass filters of varying complexity have also been proposed in order to mitigate the harmonic content in the error signal [36]-[39]. These filters provide some improvement but increase complexity and computation time, and are unable to eliminate all of the harmonic content.

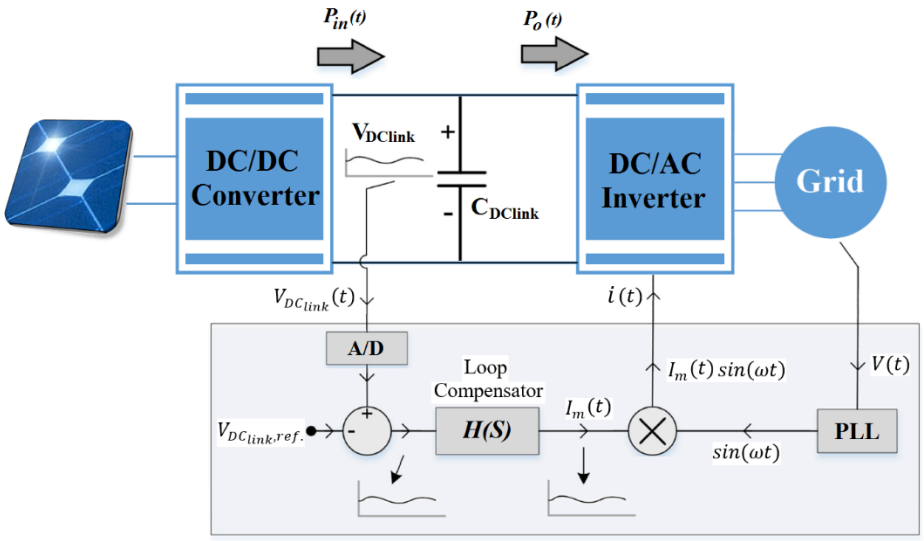


Figure 1-4: Typical DC link voltage control system.

Various DC link voltage control techniques have been proposed to mitigate the effect of DC link voltage ripple. Figure 1-5 shows the DC link voltage control using a digital finite impulse response (FIR) filter proposed in [36]. A digital FIR filter is used in [36] to sample the DC link voltage at a

low-frequency rate and then calculate the average voltage in order to reduce output current harmonics. However, the controller response to even small power transients is quite slow.

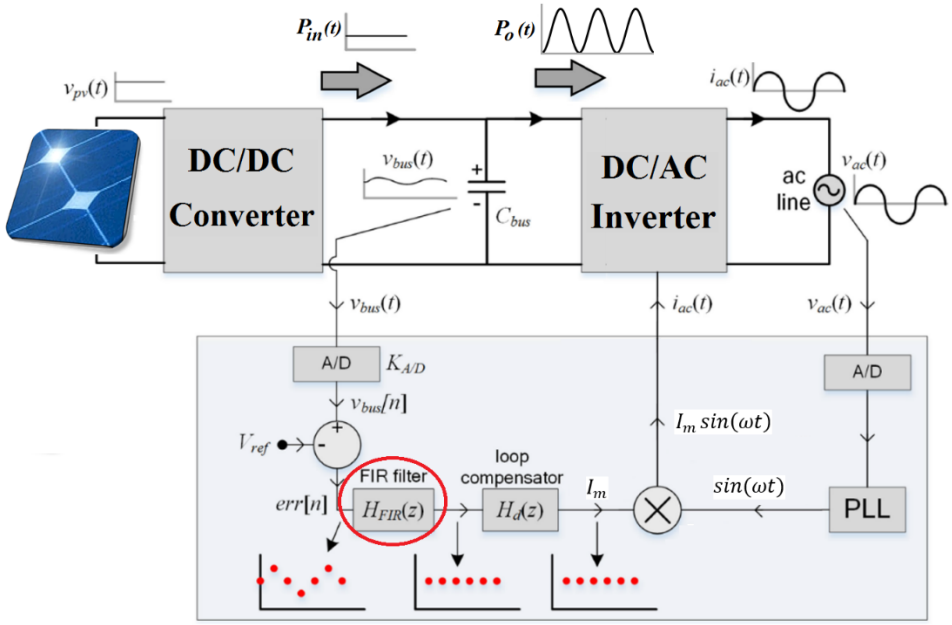


Figure 1-5: DC link voltage control using a digital finite impulse response (FIR) filter [36].

Figure 1-6 shows another technique to reduce the effect of DC link voltage ripple on the inverter output current [37]. This technique uses a digital current regulator to filter harmonics caused by the DC link voltage ripple. However, the voltage loop cutoff frequency is low which degrades the system dynamic performance.

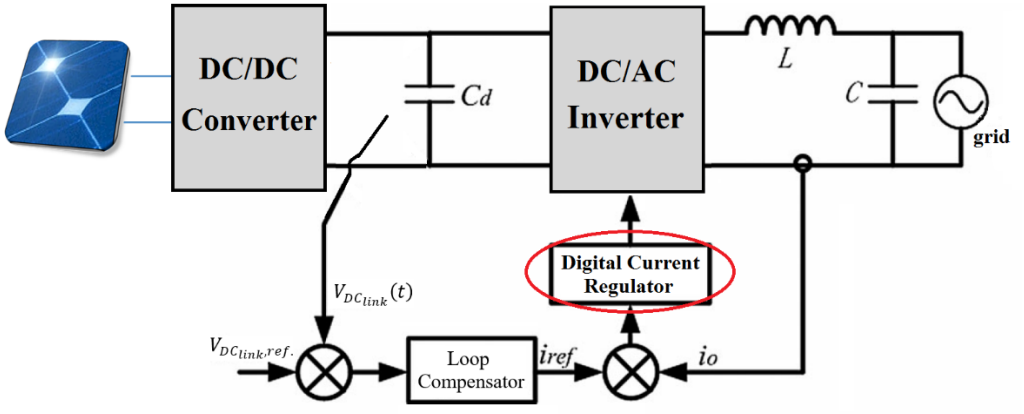


Figure 1-6: Control method proposed by Brekken *et al.* [37].

Figure 1-7 shows voltage ripple estimation method proposed by Ninad and Lopes [38]. In an effort to mitigate the effect of DC link voltage ripple on the inverter output current, voltage ripple is estimated to be added to the DC link reference voltage. The result will then be compared with the measured DC link voltage to be fed to the loop compensator. Another predictive control method was proposed in [39] based on power balance and the relationship between energy and DC capacitor voltage to filter the DC link voltage ripple. In these techniques [38], [39], accuracy and computation time will suffer.

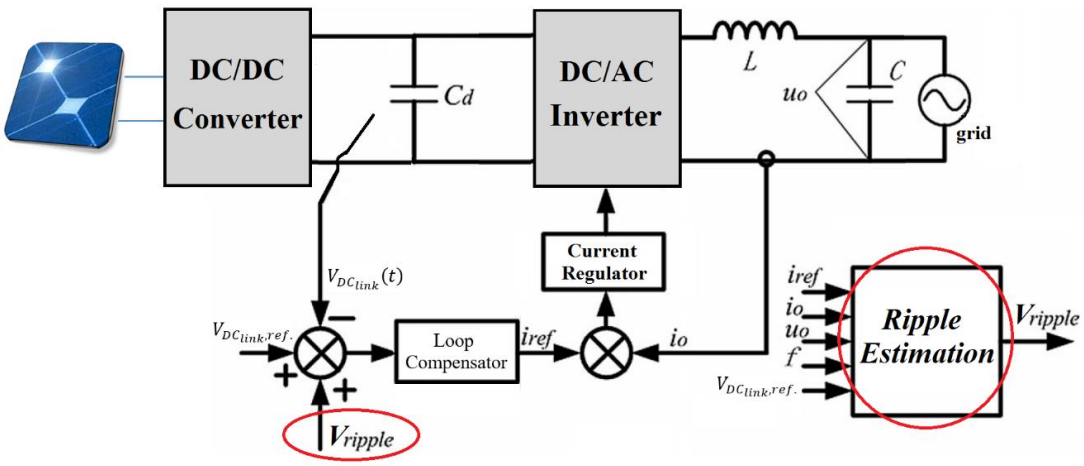


Figure 1-7: Voltage ripple estimation method proposed by Ninad and Lopes [38].

A coupled inductor filter is presented in [40] to eliminate a specific frequency from the output of a DC/DC converter which adds ciricuit component and cost to the design. A control loop compensator is proposed in [41] and [42] to minimize the output harmonics using a high-order filter with low-frequency poles and zeros which increases complexity and computation time. A third ripple port in a single-phase inverter is presented in [43] to cancel the DC link voltage ripple using a small capacitor which requires additional circuit components.

In this dissertation, a PLL-synchronized DC link voltage control is proposed to tightly regulate the DC link voltage regardless of large voltage ripple without the need for analog or digital filters.

1.5 Research Motivation and Objective

The objective of this dissertation is to improve the microinverter efficiency and power density by developing advanced control techniques without the need for additional components and analog circuits. Therefore, the development targets can be summarized as follows:

- To employ dead time optimization without any additional circuit components
- To implement soft switching technique in digital controller firmware
- To achieve more than 96% efficiency in the inverter stage
- To increase the microinverter system's lifespan to more than 20 years
- To increase the microinverter power density more than 12 W/in^3

With this in mind, the research objectives of this dissertation are summarized as follows:

- To develop a dynamic dead time optimization technique and implement it in the inverter digital controller firmware

- To improve total harmonic distortion of the inverter output current caused by dead time
- To optimize the boundaries of BCM modulation methods and develop a new soft-switching modulation technique for further efficiency improvement
- To develop a new DC link voltage control that allows higher voltage ripple and increases power density
- To increase the microinverter reliability by replacing electrolytic capacitors with film capacitors

CHAPTER 2. DYNAMIC DEAD TIME OPTIMIZATION

2.1 Introduction

This chapter introduces two efficiency improvement techniques for a grid-tied micro-inverter with current mode control zero voltage switching (ZVS) output stages. The first technique is dynamic dead time optimization wherein PWM dead times are dynamically adjusted as a function of load current. The second method is advanced phase-skipping control which maximizes inverter efficiency by controlling power on individual phases depending on the available input power from the PV source. Neither of the techniques require any additional circuit components and both can be easily implemented in digital controller firmware. The two techniques were designed and implemented in a 400W three-phase micro-inverter prototype and the experimental results validate the theoretical analysis of these techniques and demonstrate that a significant efficiency improvement can be achieved.

2.2 ZVS Boundary Conduction Mode Current Control of Three-Phase Grid-Tied Inverter

Figure 2-1 depicts a standard three-phase half-bridge grid-tied inverter. MOSFET body diodes and parasitic capacitors play an important role when implementing ZVS in an inverter output stage. In order to achieve ZVS, the bidirectional current flow discharges the MOSFET parasitic capacitor and then the body diode conducts prior to each switching transition to apply zero voltage across the MOSFET.

Although the three phases operate independently, it can be assumed that the system is balanced. Therefore, the analysis can be performed on one of the three phases. In order to simplify the

analysis of the inverter stage, steady state operation is assumed with the output voltage equal to the grid voltage. The output voltage is considered to be constant during one switching period of the output stage due to the large difference between the inverter switching frequency and the grid frequency.

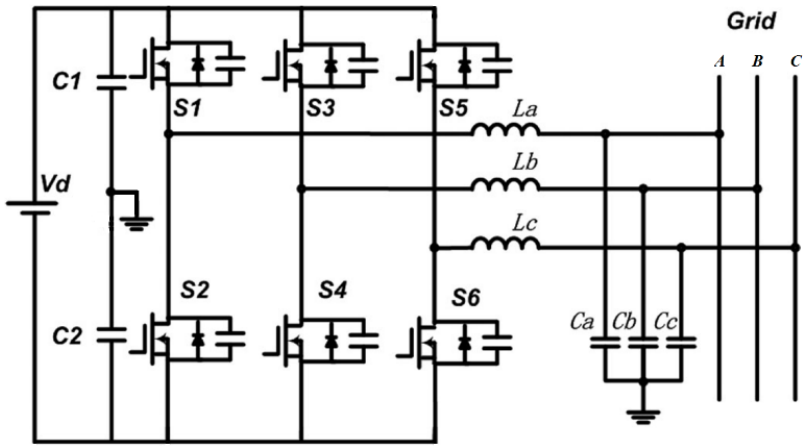


Figure 2-1: Three-phase half-bridge inverter.

Interval 1 (t_1-t_3): In this interval, as shown in Figures 2-2 and 2-3, the upper switch (S_1) is on while the lower switch (S_2) is off. Since voltage across the inductor is positive, the inductor current is linearly increasing. The inductor current can be calculated as follows:

$$i_L(t) = \frac{V_{dc}/2 - V_{ac}}{L} t + i_L(t_1) \qquad (2\text{-}1)$$

Interval 2 (t_3-t_4): In this interval, the inductor current reaches the upper limit and then the upper switch (S_1) is turned off. As shown in Figure 2-2, both switches are off and the parasitic capacitors of the MOSFETs S_1 and S_2 are being respectively charged and discharged by the inductor current. This interval is the resonant interval, and the inductor current and parasitic capacitors voltage can be calculated as follows:

$$\begin{cases} i_L(t) = \frac{V_{dc}/2 - V_{ac}}{Z_o} sin\omega_o(t-t_3) + i_L(t_3) cos\omega_o(t-t_3) \\ V_{CS1}(t) = (V_{dc}/2 - V_{ac}) + i_L(t_3) Z_o sin\omega_o(t-t_3) \\ \qquad\qquad -(V_{dc}/2 - V_{ac}) cos\omega_o(t-t_3) \\ V_{CS2}(t) = (V_{dc}/2 + V_{ac}) - i_L(t_3) Z_o sin\omega_o(t-t_3) \\ \qquad\qquad +(V_{dc}/2 - V_{ac}) cos\omega_o(t-t_3) \end{cases} \quad (2\text{-}2)$$

where, ω_o, the natural resonant frequency, and Z_o, the characteristic impedance of the resonant tank are respectively defined as follows:

$$\begin{cases} \omega_0 = {}^{1}/_{\sqrt{L.2C}} \\ Z_0 = \sqrt{{}^{L}/_{2C}} \\ C_{s1} = C_{s2} = C \end{cases} \quad (2\text{-}3)$$

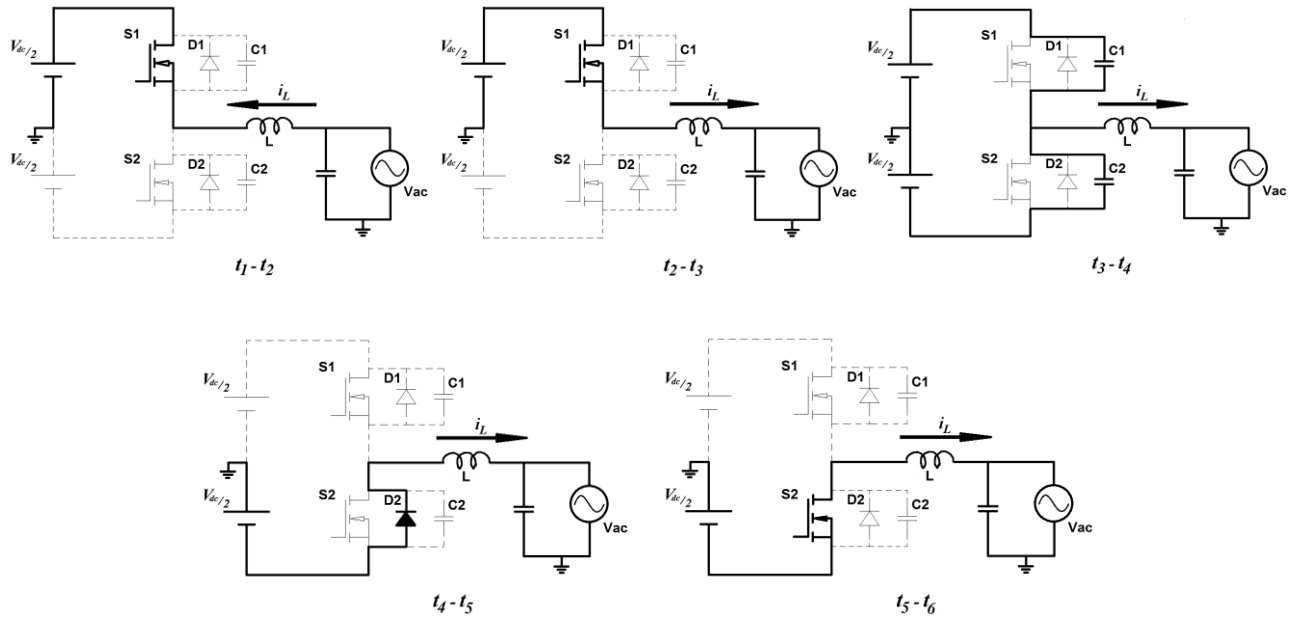


Figure 2-2: Operating intervals of a single-phase half-bridge inverter.

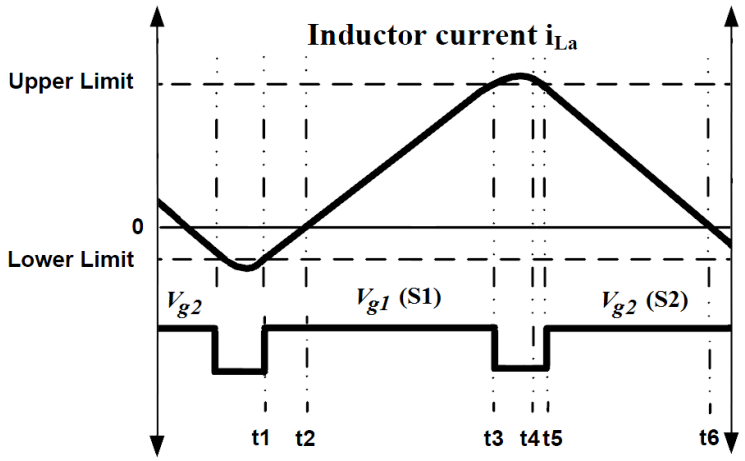


Figure 2-3: Inductor current and driving signals for BCM ZVS current control.

Interval 3 (t_4-t_6): In this interval, as soon as the parasitic capacitors of the MOSFETs S_1 and S_2 are fully charged and discharged respectively and the voltage on C_2 is zero, the body diode of MOSFET S_2 (D_2) starts conducting at t_4. Therefore, zero voltage is applied across MOSFET S_2 and it is ready to be turned on under ZVS condition. At t_5, the lower switch (S_2) turns on and the inductor current flowing through the body diode is transferred to the switch (S_2).

During this interval, since voltage across the inductor is negative, the inductor current is linearly decreasing and can be approximated as follows:

$$i_L(t) = \frac{-V_{dc}/2 - V_{ac}}{L} t + i_L(t_4) \qquad (2\text{-}4)$$

For ZVS boundary conduction mode (BCM) control implementation, the upper and lower boundaries of the inductor current need to be determined so that the inverter injects only AC current to the grid. Therefore, the average output current must be equal to the reference current during each switching cycle.

There are three possible inductor current modulation methods satisfying this requirement: BCM with fixed reverse current, BCM with variable reverse current, and BCM with fixed bandwidth.

Figure 2-4 depicts the upper and lower boundaries of BCM with fixed reverse current modulation along with the average inductor current. For the positive half cycle, the upper boundary is determined so that the average current is equal to the reference current during each switching cycle, while the lower boundary provides the reverse current to discharge the MOSFET parasitic capacitors in order to achieve ZVS during each switching period.

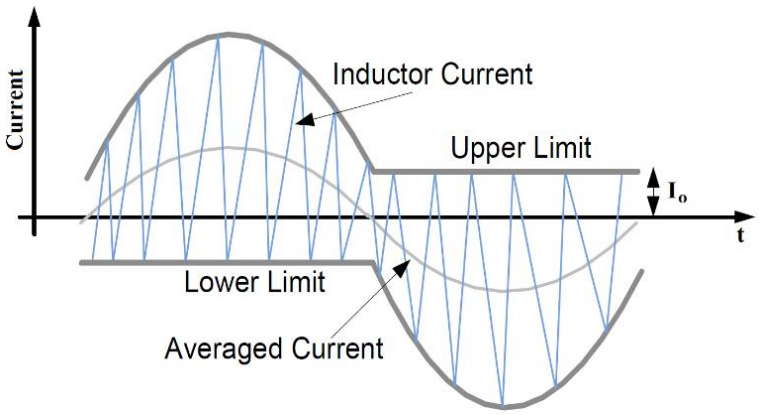


Figure 2-4: Upper and lower boundaries for BCM ZVS current control with fixed reverse current.

Similarly, for the negative half cycle, the upper limit provides ZVS for the MOSFETs and the lower limit produces the reference current. It can be seen that the average current is equal to the reference current. The upper and lower boundaries for this inductor current modulation can be calculated as follows:

$$\begin{cases} I_{upper} = 2I_{REF}\sin(\omega t) + I_o \\ I_{lower} = -I_o \end{cases} \quad ,\text{if } \sin(\omega t) \geq 0$$

$$\begin{cases} I_{upper} = I_o \\ I_{lower} = 2I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) < 0 \qquad (2\text{-}5)$$

where, I_o is the reverse current for achieving ZVS and I_{REF} is the reference peak current. It should be noted that I_{REF} is a function of the available input power and I_o selection criteria are addressed in [44].

Referring to Figure 2-4, during the time where the inductor current transitions from positive to negative on positive half cycles and from negative to positive on negative half cycles, ZVS is realized. The power dissipation during this interval is a function of the amount of time that the ZVS MOSFET's body diode is conducting. This time is determined by the amount of fixed dead time provided by the controller.

With fixed dead time control, a constant value of dead time is applied for both turn-on and turn-off transitions throughout the entire grid cycle. The dead times must be long enough to achieve ZVS by allowing the inductor current to fully charge and discharge the MOSFET parasitic capacitors. The required dead time can be calculated as follows:

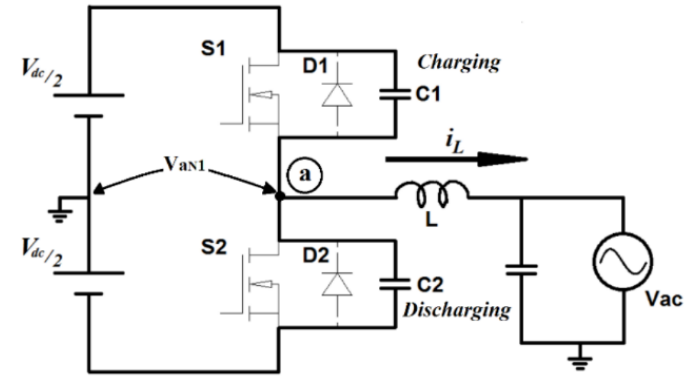
$$t_d = \frac{2CV_{dc}}{I_o} \quad (2\text{-}6)$$

where, C is the MOSFET parasitic capacitors, V_{dc} is the voltage on the MOSFET parasitic capacitors and I_o is the minimum worst-case reverse inductor current.

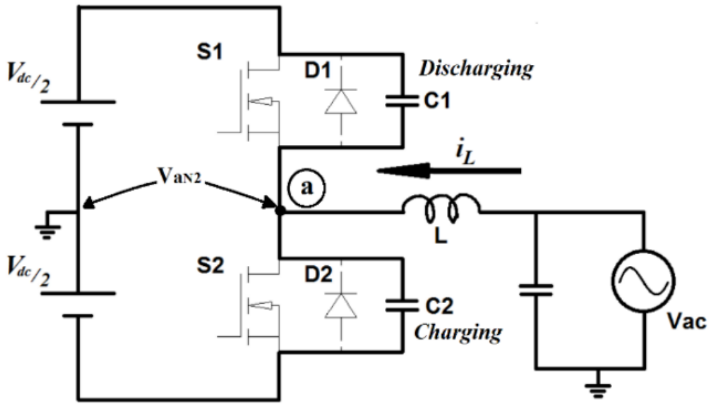
2.3 Proposed Dynamic Dead Time Optimization

The dead time interval consists of the resonant interval and the body diode conduction time. Dynamic Dead Time Optimization minimizes the MOSFET's body diode conduction time during the dead time interval [45]. The resonant intervals $(t_3\text{-}t_4)$ and $(t_7\text{-}t_8)$ are shown in Figure 2-5(a) and (b), respectively. During the first resonant interval $(t_3\text{-}t_4)$, turn-on dead time, the MOSFETs parasitic capacitance voltage can be calculated as follows:

$$\begin{cases} V_{CS1}(t) = (V_{dc}/2 - V_{ac}) - (V_{dc}/2 - V_{ac})cos\omega_o(t - t_3) \\ \qquad +Z_o.I_{upper}sin\omega_o(t - t_3) \\ V_{CS2}(t) = (V_{dc}/2 + V_{ac}) + (V_{dc}/2 - V_{ac})cos\omega_o(t - t_3) \\ \qquad -Z_o.I_{upper}sin\omega_o(t - t_3) \end{cases} \quad (2\text{-}7)$$



(a)



(b)

Figure 2-5: ZVS dead time resonant intervals: (a) turn-on dead time interval (t_{d1}), (b) turn-off dead time interval (t_{d2}).

Similarly, during the second resonant interval *(t_7-t_8)*, turn-off dead time, the MOSFETs parasitic capacitance voltage can be determined as follows:

$$\begin{cases} V_{CS1}(t) = (V_{dc}/2 - V_{ac}) + (V_{dc}/2 + V_{ac})cos\omega_o(t - t_7) \\ \qquad +Z_o.I_{lower}sin\omega_o(t - t_7) \\ V_{CS2}(t) = (V_{dc}/2 + V_{ac}) - (V_{dc}/2 + V_{ac})cos\omega_o(t - t_7) \\ \qquad -Z_o.I_{lower}sin\omega_o(t - t_7) \end{cases} \quad (2\text{-}8)$$

Referring to Figure 2-5, if the voltage at the switch node 'a' is known, the voltage on the MOSFET parasitic capacitors can be determined. The switch node voltage $V_{aN}(t)$ during dead time is given by

$$V_{aN}(t) = V_{dc}/2 - V_{CS1}(t) = V_{CS2}(t) - V_{dc}/2 \quad (2\text{-}9)$$

Using equations (2-7), (2-8) and (2-9), the switch node voltages, $V_{aN1}(t)$ and $V_{aN2}(t)$, during the turn-on dead time (t_{d1}) and turn-off dead time (t_{d2}) can be calculated as follows, respectively:

$$V_{aN1}(t) = V_{ac} + \left(\frac{V_{dc}}{2} - V_{ac}\right) cos\omega_o(t_{d1}) - Z_o . I_{upper} sin\omega_o(t_{d1}) \quad (2\text{-}10)$$

$$V_{aN2}(t) = V_{ac} - \left(\frac{V_{dc}}{2} + V_{ac}\right) cos\omega_o(t_{d2}) - Z_o . I_{lower} sin\omega_o(t_{d2}) \quad (2\text{-}11)$$

where, t_{d1} and t_{d2} are t_4-t_3 and t_8-t_7, respectively.

2.4 Effects of Circuit Component Nonlinearities

Device parasitic capacitances are inherent due to semiconductor physics and have a nonlinear nature. These nonlinear capacitances have a negative impact on switching transition times and therefore on switching loss. A nonlinear capacitor can be modeled by a linear equivalent [46], [47] or circuit simulators [48], [49].

During each resonant interval, the MOSFET parasitic capacitance voltage (V_{CS}) transitions from 0 V to V_{dc} or vice versa depending on the switching edge. For example, in Figure 2-5(a), the upper MOSFET's parasitic capacitor voltage ($V_{CS1}(t)$) transitions from 0 V to V_{dc}, while $V_{CS2}(t)$ transitions from V_{dc} to 0 V. $V_{CS1}(t)$ and $V_{CS2}(t)$ are defined by equation (2-7). During these transition times, the MOSFET parasitic capacitance varies with the value of $V_{CS1}(t)$ and $V_{CS2}(t)$. This capacitance can be expressed as

$$C_{OSS} = C_{OSS}(V_{ds}) \quad (2\text{-}12)$$

Therefore, the definition from (2-3) can be rewritten as follows:

$$\begin{cases} \omega_0 = {}^{1}\!/\!\sqrt{L.2C_{OSS}(V_{ds})} \\ Z_0 = \sqrt{{}^{L}\!/\!{2C_{OSS}(V_{ds})}} \\ C_{s1} = C_{s2} = C_{OSS}(V_{ds}) \end{cases} \quad (2\text{-}13)$$

Figure 2-6 demonstrates the variation in C_{OSS} for a Fairchild FCB20N60F MOSFET extracted from the device datasheet and fitted to a curve using discrete data points. Referring to the figure, the value of the capacitance drastically drops when V_{ds} increases from 0 V to 50 V, whereas it has a relatively constant value for voltages greater than 50 V.

The nonlinear nature of the MOSFET output capacitance has been taken into account in computing optimum dead times in equations (2-10) and (2-11). In both simulated and experimental results, the DC link voltage was set at 400 V. Therefore, the nonlinear voltage dependent capacitance must be charged and discharged from 0 V to 400 V.

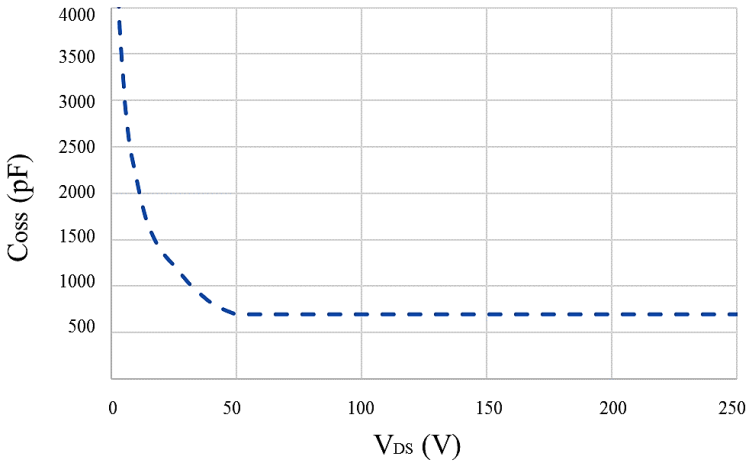


Figure 2-6: Coss versus Drain Source voltage for Fairchild FCB20N60F MOSFET.

Virtually all inductors used in power filter circuits exhibit a decrease in inductance with increasing current. This inductance decrease is often nonlinear and varies with core material and magnetic

circuit structure. Figure 2-7 shows the inductance versus DC current for a 270 μH, 4 A gapped ferrite inductor.

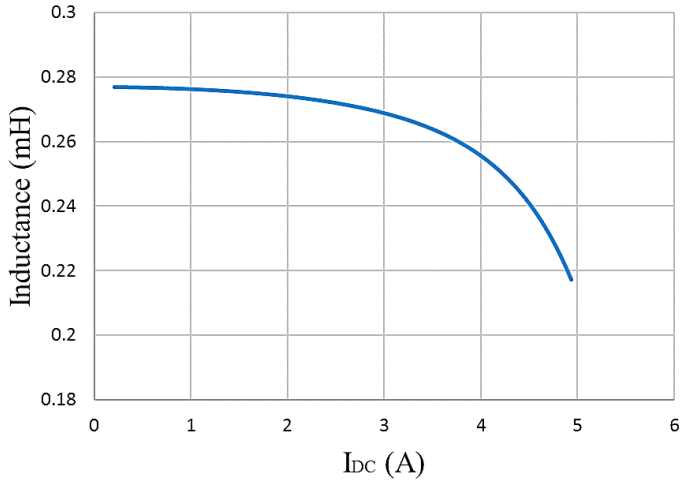


Figure 2-7: Inductance versus DC current for a gapped ferrite inductor.

Figure 2-8 shows Z_o versus dead time at peak current and full load with both fixed and variable inductance values. It can be seen in the figure that a varying inductance value has a minimal effect on the value of Z_o and consequently from equations (2-10) and (2-11) an insignificant effect on dead time when compared to the effect of the nonlinear parasitic capacitance of a MOSFET.

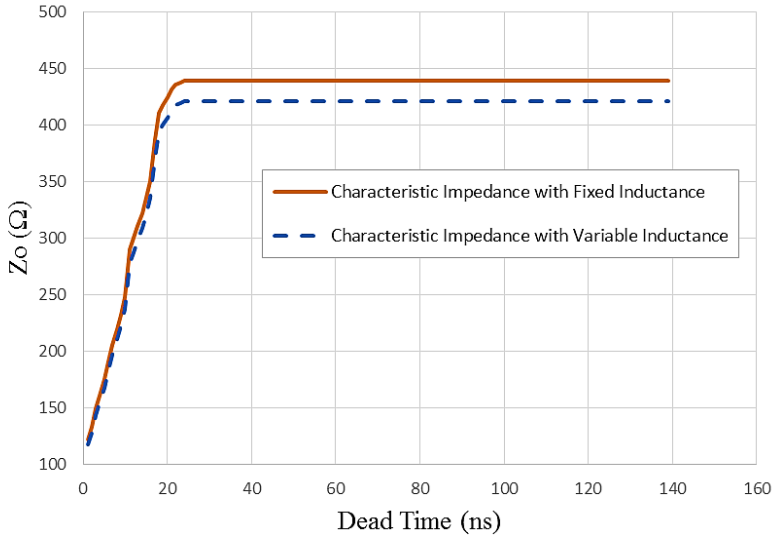


Figure 2-8: Z_0 versus dead time at full load (Peak current).

Optimum dead time is calculated for each switching cycle iteratively as opposed to fixed dead time where one dead time value would be selected for all operating points. Equations (2-10) and (2-11) were implemented in MATLAB. t_{d1} and t_{d2} were incremented in one nano second steps to yield a range of optimum dead time values for switch node voltages between +200 V and -200 V for each switching cycle. Figure 2-9 shows optimum dead times calculated using equations (2-10) and (2-11) during positive and negative half cycles for the 400-W three-phase micro-inverter prototype operating at full load, given the fact that $V_{aN1}(t)$ transitions from $V_{dc}/2$ to $-V_{dc}/2$ and $V_{aN2}(t)$ transitions from $-V_{dc}/2$ to $V_{dc}/2$. The fixed dead time for this prototype was set at 530 ns for both turn-on and turn-off transitions. The MOSFETs used are Fairchild FCB20N60F with V_{dc}=*400 V* and a 270 μH gapped ferrite output filter inductor.

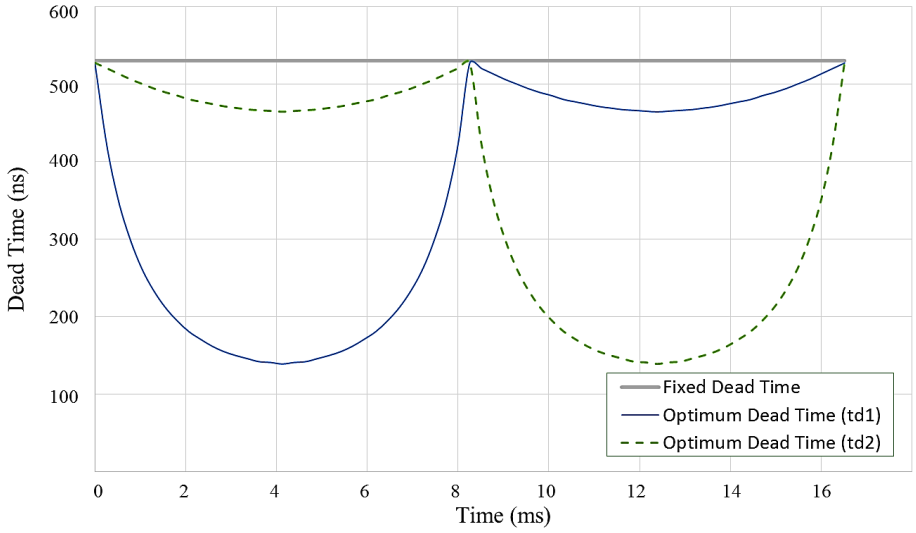


Figure 2-9: Optimum dead time versus fixed dead time at full load.

For positive half cycles, the optimum turn-on dead time (t_{d1}) varies with changes in output current due to the fact that the upper boundary in BCM is sinusoidal, while the optimum turn-off dead time (t_{d2}) varies only slightly with load variations due to the fixed reverse current in BCM

modulation. Similarly, during negative half cycles, t_{d1} varies slightly and t_{d2} changes with output current.

2.5 Simulation Results

In order to verify the proposed Dynamic Dead Time Optimization technique, Linear Technology's LTspice simulation software was used to simulate a half-bridge single-phase 130W inverter operating with BCM ZVS current control. The simulation circuit parameters are as follows: DC bus voltage 400 V, AC grid voltage 120 V rms, 60 Hz, inductor value 270 µH and switching frequency range 20-185 kHz. The high frequency current in the filter inductor with 60 Hz modulation is shown in Figure 2-10.

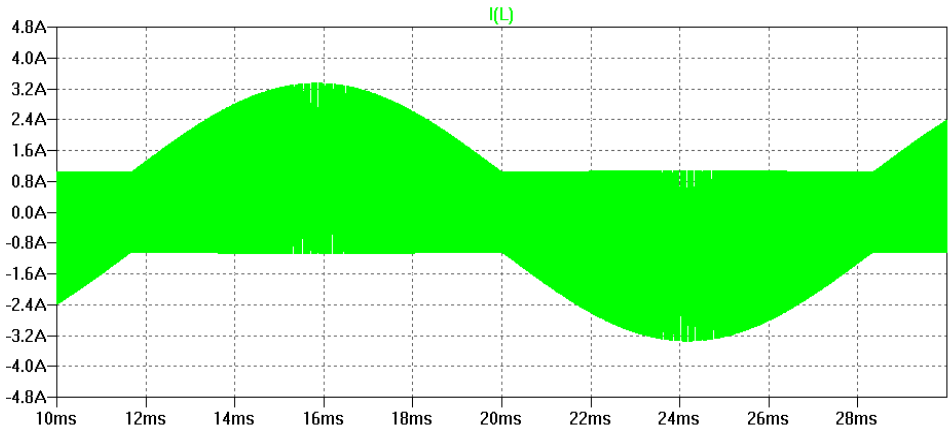


Figure 2-10: Inductor current with BCM current control and fixed reverse current.

Figure 2-11 shows filter inductor current, MOSFET gate drive voltages and switch node voltage (V_{aN}) with a fixed turn-on and turn-off dead time of 300 ns at the peak of the grid current.

The simulation waveforms in Figure 2-12 depict how Dynamic Dead Time Optimization independently changes the gate drive turn-on and turn-off dead time. Once the MOSFET parasitic

capacitors are fully charged/discharged, the dynamic dead time optimization controller enables the gate drive, thereby minimizing MOSFET body diode conduction time.

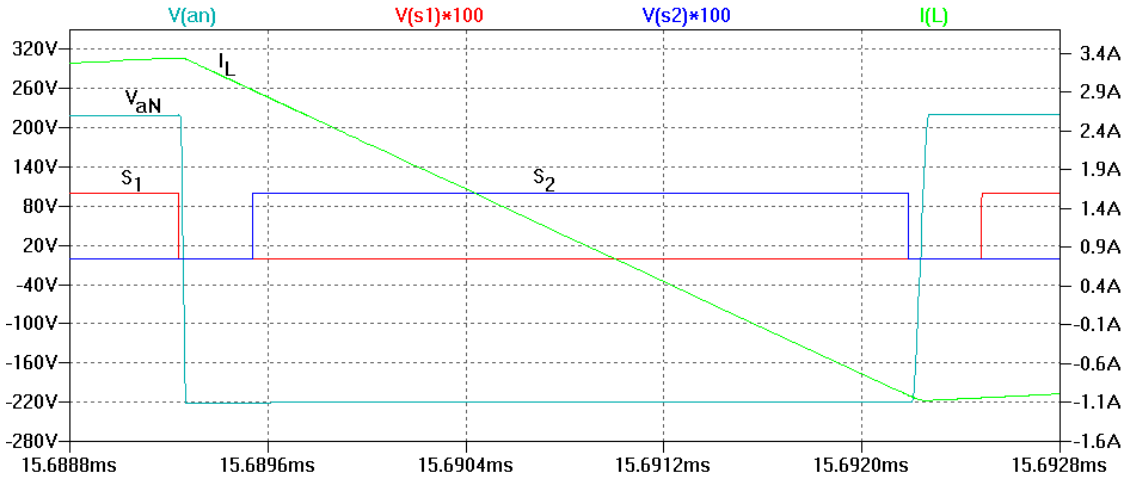


Figure 2-11: Fixed dead time gate drive, inductor current and switch node voltage.

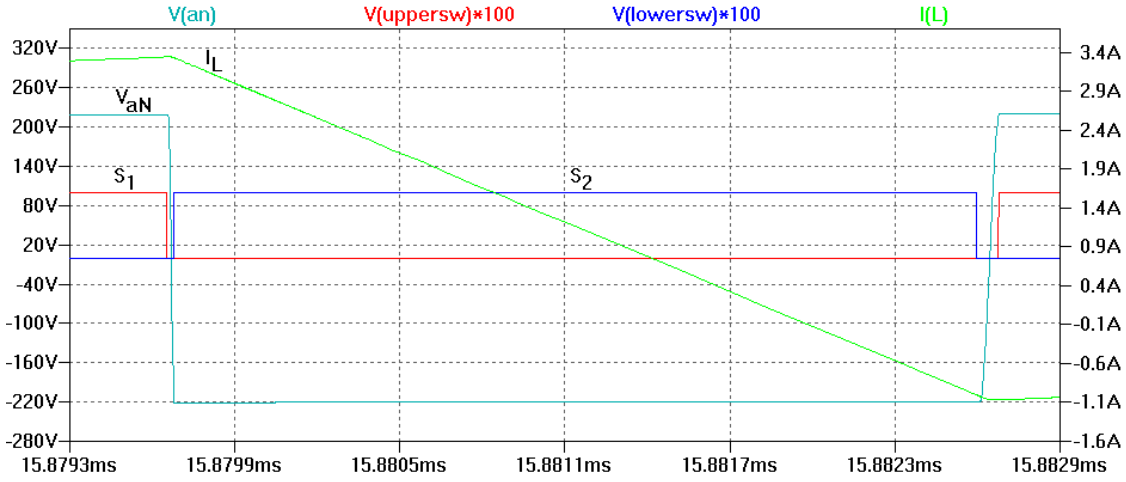


Figure 2-12: Dead times with Dynamic Dead Time Optimization.

2.6 Advanced Phase Skipping Control

In three-phase inverters and microinverters, it is advantageous to operate at or close to rated power where efficiency is the highest. However, when power levels drop, the available power is distributed evenly among the three phases. This results in reduced efficiency because load

independent loss will become a bigger portion of the overall losses. In single-phase inverters, techniques such as pulse skipping [50] are commonly employed in an effort to improve light-load efficiency. This method is not predictable and can become problematic in large installations. Advanced Phase Skipping Control maximizes the output stage efficiency of a three-phase micro-inverter by managing the amount of power on each phase based on the available power [51]. The available power is determined by the PV side MPPT controller.

In an Advanced Phase Skipping system, there are three possible modes of operation: normal three-phase mode, two-phase mode and single-phase mode. The controller transitions between these three modes in order to maximize inverter efficiency. Based on the available power, the controller can disable one or two phases of the three-phase system. At power levels above two-thirds of rated power, all three phases are enabled. At one-third to two-thirds of rated power, the controller disables one phase. At power levels below one-third of rated power, the controller enables only one phase. It should be noted that in single and two-phase modes, the ripple current in the DC link capacitor will be considerably higher. This problem is mitigated by the fact that in this mode the power level is much less and the controller can compensate for this by adjusting the DC link voltage to ensure that there is enough headroom to run the output stage.

Available power may vary over a wide range during a typical day due to environmental factors such as clouds and shading as well as low irradiance during morning and afternoon. During times when available power is low, the three-phase micro-inverter will most likely be operating in single-phase mode. As available power increases during the day, the controller will enable two and eventually all three phases and distribute power evenly in each phase in order to maximize overall system efficiency.

Unlike phase shedding techniques employed in multiphase converters commonly used in Voltage Regulator Modules (VRMs) and interleaved Power Factor Correction (PFC) circuits, in an Advanced Phase Skipping system, the overall number of operating phases does not change and in fact this control technique is used to maintain three-phase system balance. Actual phase skipping is done at the micro-inverter level in order to maintain the integrity of all three phases at the system level. However, the overall strategy would require a system level controller to dynamically manage the power from each micro-inverter to ensure power imbalance between the three phases is minimized.

2.7 Experimental Results

Experimental results were obtained from a 400-W three-phase half-bridge micro-inverter prototype using two different manufacturer's MOSFETs for switching devices. The MOSFETs specifications are included in Table 2-1 for reference. MOSFETs with large differences in C_{OSS} were chosen for this work in order to demonstrate the effectiveness of the proposed Dynamic Dead Time Optimization for a wide range of MOSFET parasitic capacitors. The DSP used is a Microchip dsPIC33FJ16GS504. The experimental circuit parameters are as follows: DC bus voltage 400 V, AC grid voltage 120 V rms, 60 Hz, inductor value 270 μH and switching frequency range 20-185 kHz. Using equations (2-10) and (2-11) in MATLAB, a lookup table can be generated which contains the optimum dead time values for each circuit operating point. This table can then be programmed into the DSP where the optimum dead time values are selected based on the DSP's measurement of dynamic circuit operating parameters.

Table 2-1: Two Different Manufacturer's MOSFETs Specifications

Manufacturer Part Number	V_{dss} (V)	I_d (A)	R_{ds}-ON (Ω)	C_{iss} (pF)	C_{oss} (pF)	C_{rss} (pF)	V_{SD}* (V)
FCB20N60F	600	20	0.150	2370	1280	95	1.4
STB21N65M5	650	17	0.150	1950	46	3	1.5

* Drain to Source Diode Forward Voltage

The experimental waveforms of Figures 2-13, 2-14 and 2-15 correspond to Figures 2-10, 2-11 and 2-12 in the simulation results respectively.

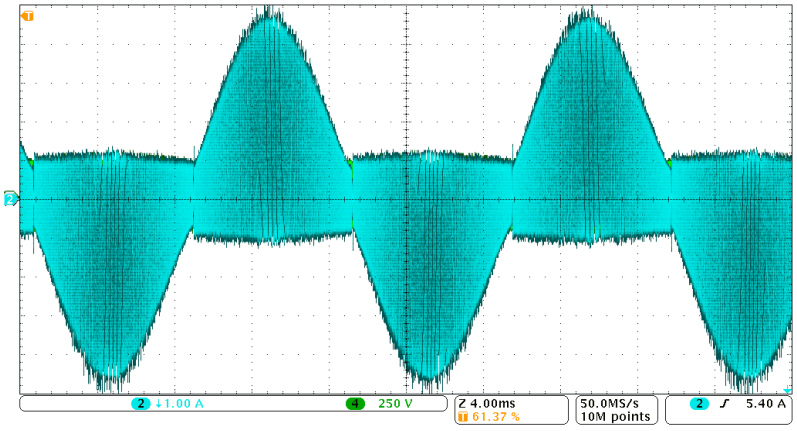


Figure 2-13: Filter inductor current.

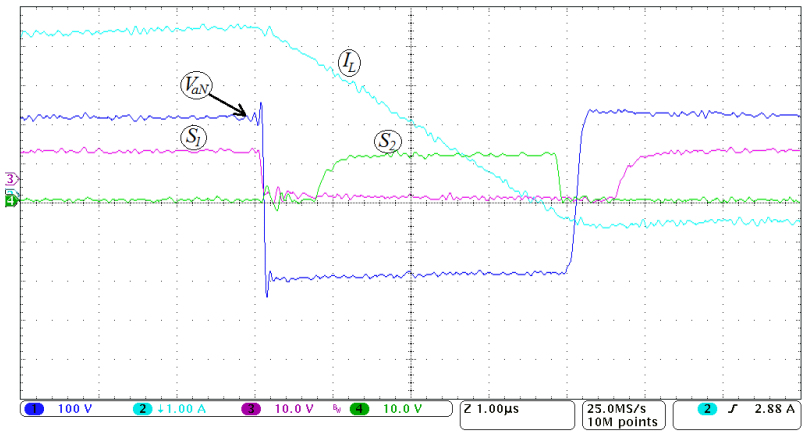


Figure 2-14: Experimental waveforms with fixed dead time.

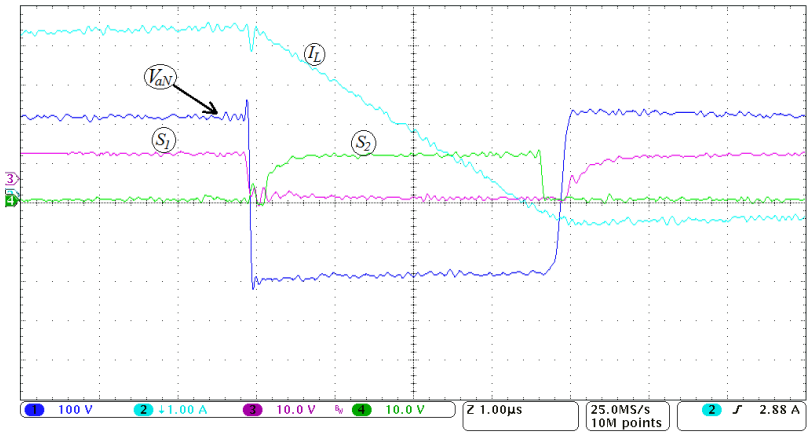


Figure 2-15: Experimental waveforms with Dynamic Dead Time Optimization.

The micro-inverter was tested in four different modes of operation: normal operation (with fixed dead time and no phase skipping), with Dynamic Dead Time Optimization (DTO) only, with Advanced Phase Skipping Control only, and with both Dynamic DTO and Advanced Phase Skipping Control.

Figures 2-16 and 2-17 show the efficiency measured with a Yokogawa PZ4000 power analyzer for each of the micro-inverter operating modes for FCB20N60F and STB21N65M5 MOSFETs respectively.

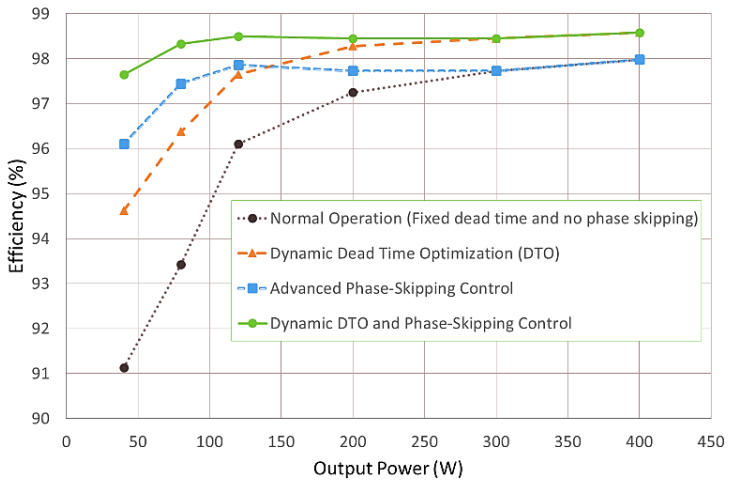


Figure 2-16: Micro-inverter output stage efficiency with FCB20N60F MOSFET.

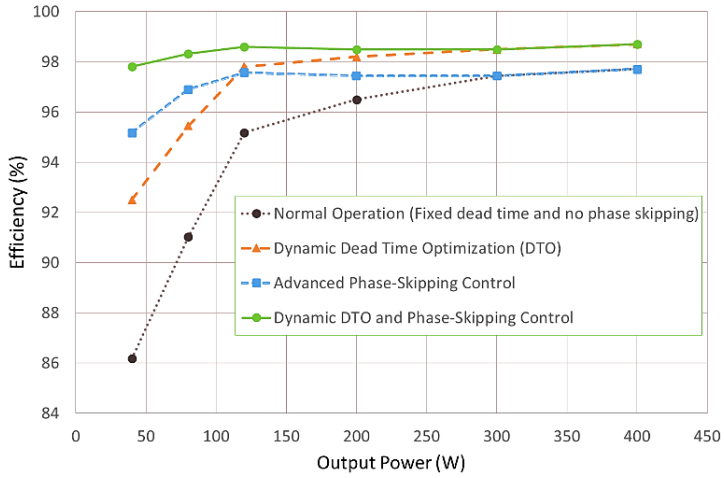


Figure 2-17: Micro-inverter output stage efficiency with STB21N65M5 MOSFET.

Referring to the efficiency figures, it can be seen that both manufacturer's MOSFETs exhibited similar performance with respect to each of the four micro-inverter operating modes. Efficiency was the lowest over the entire load range when the micro-inverter was operated in normal mode for both manufacturer's MOSFETs. A noticeable improvement in efficiency was achieved by implementing Dynamic Dead Time Optimization. Efficiency improvement was the highest at light loads where switching frequency is maximum. Implementing Advanced Phase Skipping Control also resulted in significant efficiency improvement especially at light loads. The best efficiency was realized with a combination of Dynamic Dead Time Optimization and Advanced Phase Skipping Control. CEC weighted efficiency is shown in Table 2-2 for both manufacturer's MOSFETs and for each mode of operation.

Table 2-2: CEC Weighted Efficiency for Different Modes of Operation

Manufacturer Part Number	Normal Operation (Fixed Dead Time)	Dynamic DTO	Advanced Phase Skipping Control	Dynamic DTO + Advanced Phase Skipping Control
FCB20N60F	96.96%	98.06%	97.67%	98.42%
STB21N65M5	96.21%	97.97%	97.35%	98.48%

Combining Dynamic Dead Time Optimization and Advanced Phase Skipping Control produced an additional 1.5 percentage points in CEC efficiency for FCB20N60F MOSFET and 2.3 percentage points in CEC efficiency for STB21N65M5 MOSFET.

It is worth noting that neither of the two efficiency improvement techniques described in this chapter require any additional circuit components. Therefore, reliability and cost will not be negatively impacted and in fact reliability will be improved due to lower operating junction temperatures. Research on reliability of power MOSFETs and predicting their failures shows that it is possible to predict failure of power MOSFETs due to thermal stress without estimating the junction temperature [52], [53]. This is achieved by developing a mathematical framework to capture the drop in on voltage of a MOSFET due to aging and developing prognostic models [54]. Although advanced phase skipping control is applicable only to three-phase inverters and micro-inverters, dynamic dead time optimization will improve efficiency of both three-phase and single-phase inverters and micro-inverters that employ soft switching techniques such as BCM ZVS current control.

2.8 THD Improvement with Dynamic Dead Time Optimization

Since optimizing the dead time minimizes inductor current excursion beyond the upper and lower fixed reverse thresholds in BCM ZVS current control, an improvement in THD is realized. Figure 2-18 shows output current and inductor current at 80 W with fixed dead time. It can be seen that the reverse current threshold is not constant and in fact varies with the peak current. This anomaly tends to increase THD by subtracting from the output peak current.

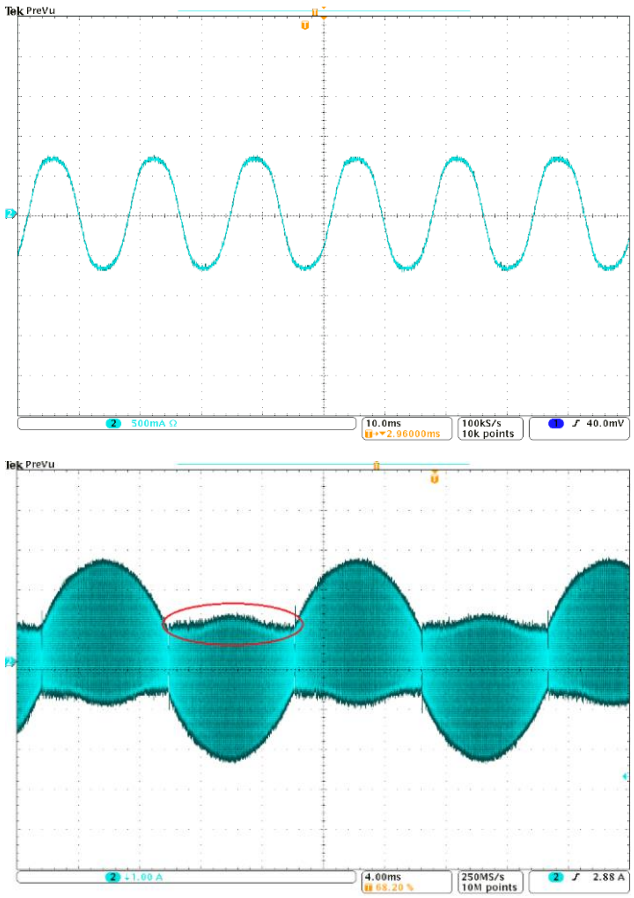


Figure 2-18: Output current and inductor current with fixed dead time.

The THD in Figure 2-18 is 7.78% measured with a Yokogawa PZ4000 power analyzer. This effect is more significant at light loads since the fixed dead time becomes a larger portion of the switching

period. Identical conditions with implementation of Dynamic Dead Time Optimization control is shown in Figure 2-19. The anomaly shown in Figure 2-18 is greatly reduced due to the fact that dead time is now proportional to the switching period resulting in a much improved THD of 4.74%.

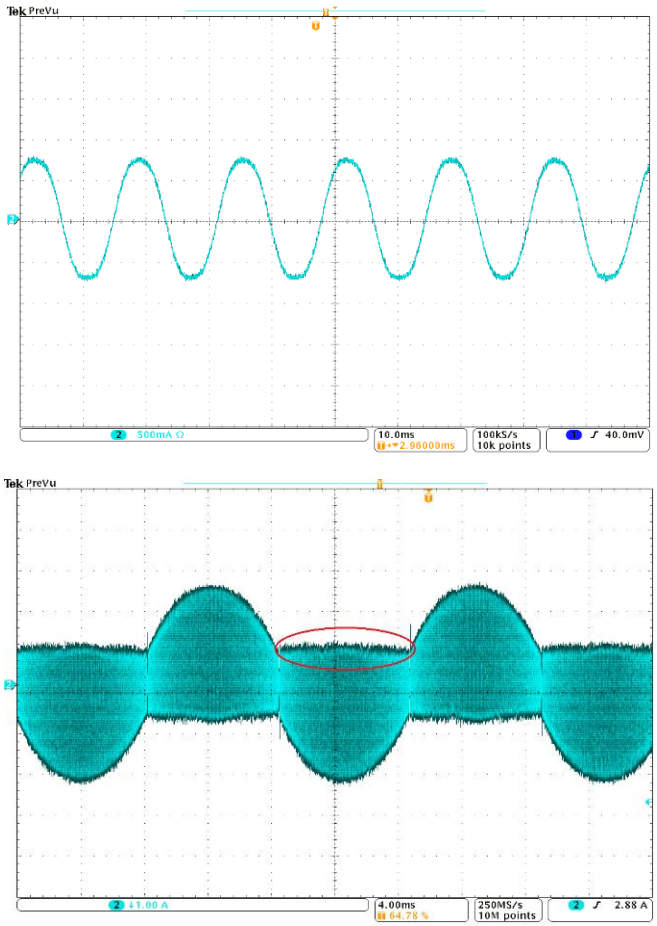


Figure 2-19: Output current and inductor current with dynamic dead time optimization.

2.9 Summary

In this chapter, two efficiency improvement techniques have been introduced and implemented in a three-phase micro-inverter. Practical implementation of these two techniques has been verified by experimental results on a 400-W three-phase micro-inverter prototype. It is very important to

note that no additional circuit components are required and the techniques can be implemented entirely in the digital controller firmware.

Dynamic Dead Time Optimization minimizes MOSFET body diode conduction time which reduces power dissipation. Therefore, reliability will be improved due to lower operating junction temperatures. THD will also be improved in inverters using BCM ZVS current control. This technique can be digitally implemented on three-phase and single-phase inverters and micro-inverters that employ soft switching techniques. Advanced Phase Skipping Control is applicable to three-phase inverters and micro-inverters. Depending on the available input power from the PV source, this control method features distributed power to individual phases so that the maximum DC/AC stage efficiency of the three-phase micro-inverter is achieved. The experimental results show that the proposed hybrid digital control algorithm which combines Dynamic Dead Time Optimization and Advanced Phase Skipping Control can significantly improve the CEC efficiency of a 400-W three-phase half-bridge micro-inverter prototype.

CHAPTER 3. ANALYSIS AND OPTIMIZATION OF VARIABLE-FREQUENCY SOFT-SWITCHING PEAK CURRENT MODE CONTROL TECHNIQUES FOR MICROINVERTERS

3.1 Introduction

This chapter presents a detailed power loss model for a microinverter with three different zero voltage switching (ZVS) boundary conduction mode (BCM) current modulation methods. The model is used to calculate the optimum peak current boundaries for each modulation method. Based on the power loss model, a dual-zone modulation method is proposed to further improve the microinverter efficiency. The proposed modulation method provides two main benefits: the addition of one more soft switching transition and low inductor peak current. The additional soft switching transition reduces switching losses by means of zero current switching (ZCS). The lower peak current boundary reduces inductor rms current and conduction losses as well as allowing the output filter inductor to be smaller and more efficient. An improved BCM peak current control method was proposed and implemented on a microinverter prototype. The control circuit provides a highly accurate representation of the filter inductor current waveform and also provides galvanic isolation which simplifies control circuit design. The experimental results on a 400-W three-phase half-bridge microinverter validate the theoretical analysis of the power loss distribution and demonstrate that further improvement in efficiency can be achieved by using the proposed dual-zone modulation method.

3.2 Variable-Frequency Peak Current Mode Control Techniques

Three ZVS BCM peak current mode control methods are described and compared in this section. Figure 3-1 depicts a standard power circuit of a three-phase half-bridge inverter. The body diode and the parasitic capacitance of the MOSFETs help to achieve ZVS in an inverter output stage. In order to implement turn-on ZVS, the bidirectional inductor current discharges the MOSFET parasitic capacitance until its body diode conducts prior to each switching transition.

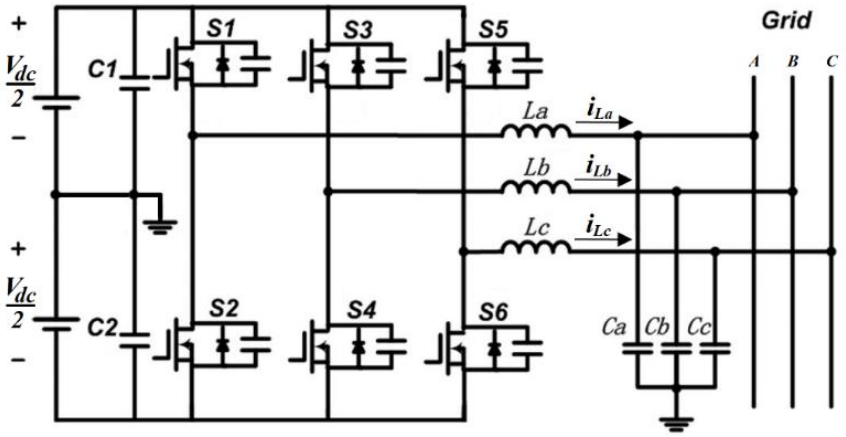
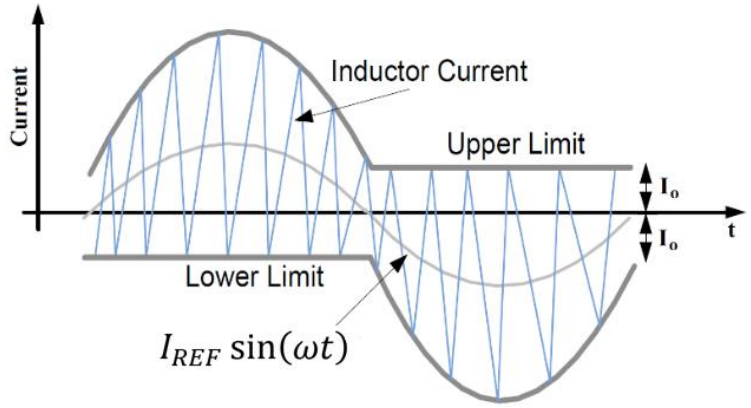


Figure 3-1: Three-phase half-bridge inverter.

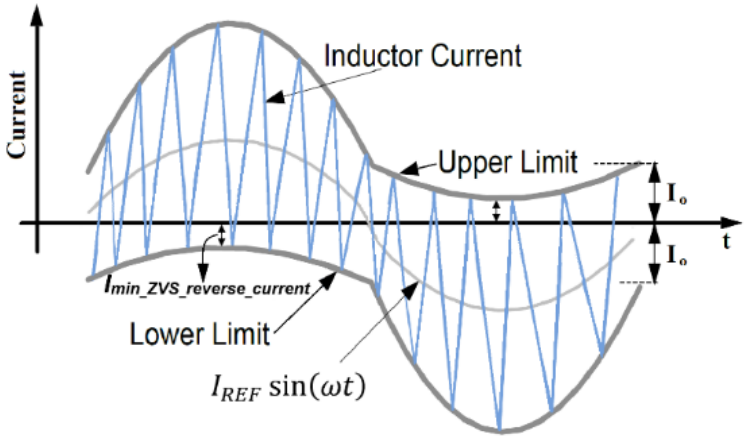
In order to inject AC current into the grid, the average inductor current must be equal to the reference current during each switching cycle. Therefore, the inductor current has to be between two predetermined boundaries. Three current modulation methods with different boundary shapes have been introduced in [35] which satisfy this requirement: BCM with fixed reverse current, BCM with variable reverse current, and BCM with fixed bandwidth.

As shown in Figure 3-2, the inductor current has to be between the upper and lower limits for all the three modulation techniques in order to generate an average current equal to the reference

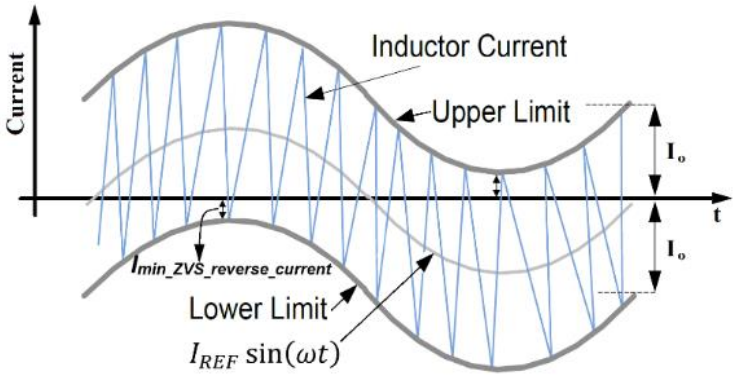
current. Since the inverter power loss is to be analyzed in this chapter, the inductor current and switching frequency are calculated for each of the three modulation techniques.



(a)



(b)



(c)

Figure 3-2: Three different ZVS BCM modulation methods: (a) fixed reverse current, (b) variable reverse current, (c) fixed band width.

The upper and lower boundaries and switching frequency for BCM with fixed reverse current modulation can be calculated as follows:

$$\begin{cases} I_{upper} = 2I_{REF}\sin(\omega t) + I_o \\ I_{lower} = -I_o \end{cases} \quad ,\text{if } \sin(\omega t) \geq 0$$

$$\begin{cases} I_{upper} = I_o \\ I_{lower} = 2I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) < 0 \qquad (3\text{-}1)$$

$$f_{sw}(t) = \frac{\left({}^{V_{dc}}/_{2}\right)^2 - (V_m \sin(\omega t))^2}{LV_{dc}(2I_{REF}\sin(\omega t) + 2I_o)} \qquad (3\text{-}2)$$

where, I_{REF} is the output peak current reference, I_o is the reverse current for achieving ZVS, V_{dc} is the input voltage for the half-bridge inverter, V_m is the grid or output peak voltage and L is the output filter inductor.

The boundaries and switching frequency for BCM with variable reverse current modulation can be found from equations (3-3) and (3-4).

$$\begin{cases} I_{upper} = \frac{3}{2} I_{REF}\sin(\omega t) + I_o \\ I_{lower} = \frac{1}{2} I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) \geq 0$$

$$\begin{cases} I_{upper} = \frac{1}{2} I_{REF}\sin(\omega t) + I_o \\ I_{lower} = \frac{3}{2} I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) < 0 \qquad (3\text{-}3)$$

$$f_{sw}(t) = \frac{\left({}^{V_{dc}}/_{2}\right)^2 - (V_m \sin(\omega t))^2}{LV_{dc}(I_{REF}\sin(\omega t) + 2I_o)} \qquad (3\text{-}4)$$

The upper and lower limits and switching frequency for BCM with fixed bandwidth modulation can be expressed as follows:

$$\begin{cases} I_{upper} = I_{REF}\sin(\omega t) + I_o \\ I_{lower} = I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) \geq 0$$

$$\begin{cases} I_{upper} = I_{REF}\sin(\omega t) + I_o \\ I_{lower} = I_{REF}\sin(\omega t) - I_o \end{cases} \quad ,\text{if } \sin(\omega t) < 0 \qquad (3\text{-}5)$$

$$f_{sw}(t) = \frac{\left(V_{dc}/_2\right)^2 - (V_m\sin(\omega t))^2}{LV_{dc}(2I_o)} \qquad (3\text{-}6)$$

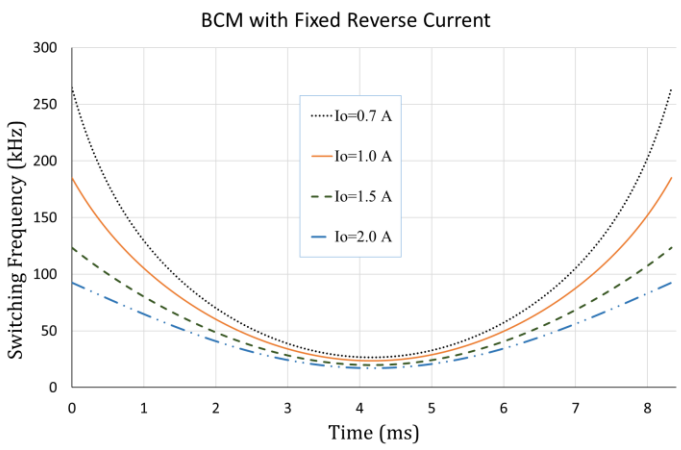
Note that for all three modulation methods, T_1 and T_2 are the required time for inductor current to traverse from the lower limit to the upper limit and from the upper limit to the lower limit, respectively and calculated as follows:

$$\begin{cases} T_1 = \frac{L\left(I_{upper} - I_{lower}\right)}{\left(V_{dc}/_2\right) - V_{grid}} \\ T_1 = \frac{L\left(I_{upper} - I_{lower}\right)}{\left(V_{dc}/_2\right) + V_{grid}} \end{cases} \qquad (3\text{-}7)$$

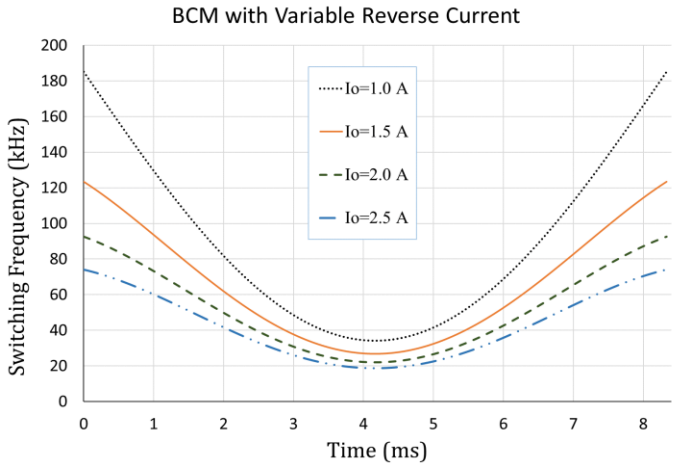
Switching frequency is derived from (3-7) as follows:

$$f_{sw} = \frac{\left(V_{dc}/_2\right)^2 - (V_{grid})^2}{LV_{dc}(I_{upper} - I_{lower})} \qquad (3\text{-}8)$$

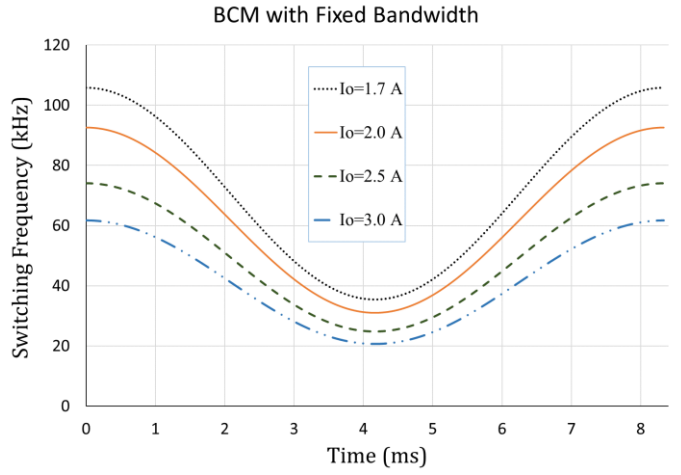
The switching frequency and inductor rms current are determined by the peak current boundaries. Figures 3-3 and 3-4 depict the full load switching frequency and inductor rms current for each modulation method at different boundary values. An output inductor value of 270 μH was selected to ensure that the minimum switching frequency was above the maximum audible value of 20 kHz.



(a)



(b)



(c)

Figure 3-3: Switching frequency over a half 60-Hz line cycle with varying I_o for: (a) fixed reverse current, (b) variable reverse current, and (c) fixed band width.

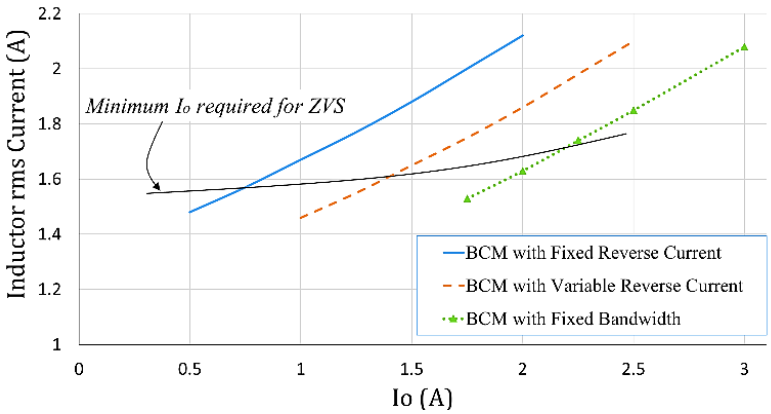


Figure 3-4: Inductor rms current versus I_o for each modulation method at full load.

Referring to equations (3-2), (3-4) and (3-6), switching frequency for all three modulation methods is a function of the grid or output voltage and the peak current boundaries and is the highest at zero crossings. For example, BCM with fixed reverse current has the widest switching frequency range because both the instantaneous output voltage and the peak current boundaries decrease at zero crossings. BCM with fixed bandwidth has the narrowest switching frequency range since its peak current boundaries are constant over the entire output voltage range. Likewise, at full load, BCM with fixed reverse current has the lowest inductor rms current, while BCM with fixed bandwidth has the highest inductor rms current.

The minimum reverse current for achieving ZVS depends on the MOSFET's specification (parasitic capacitance, C_{OSS}), the voltage across the MOSFET (V_{dc}) and dead time (t_d), and for this topology is approximately calculated as follows [55]:

$$I_{\min\_ZVS\_reverse\_current} \approx \frac{2C_{OSS}V_{dc}}{t_d} \qquad (3\text{-}9)$$

An optimum combination of dead time (800 ns) and reverse current (0.8 A) was selected experimentally for this work. Therefore, in order to ensure ZVS operation for each modulation method, a minimum reverse current of 0.8 A is required to discharge the MOSFET parasitic

capacitance. With this in mind, the minimum I_o required to maintain the 0.8 A reverse current for each modulation method at full load is shown in Figure 3-4. In all three modulation methods, ZVS is achieved during the entire grid cycle. Therefore, for each modulation I_o is determined in such a way that ZVS can even be achieved for the lowest reverse current.

Since only turn-on ZVS can be achieved with these modulation methods, higher switching frequency generally results in proportionally higher switching losses. Larger boundary values reduce switching frequency but also increase inductor rms current and conduction losses.

A detailed power loss analysis will be presented in the next section which determines the optimum boundary values for each modulation method in order to maximize efficiency.

3.3 Power Loss Analysis

A loss model was designed in order to predict the power loss in the three-phase half-bridge microinverter prototype. Table 3-1 shows the prototype operating parameters. This model can be used to calculate the most efficient peak current boundary for each of the three modulation methods. Four sources of loss have been taken into consideration in this model: switching loss (including MOSFET body diode conduction loss), MOSFET conduction loss, inductor core loss and inductor winding loss.

Since all three modulation methods can achieve turn-on ZVS, only turn-off switching loss is calculated in the loss model using the following equation:

$$P_{sw(OFF)}(t) = \frac{1}{2} \times I_i(t) \times V_{DS} \times f_{sw}(t) \times t_{s(H-L)} \qquad (3\text{-}10)$$

Table 3-1: Inverter Prototype Operating Parameters

Grid parameters	V_{grid} *(nominal) = 120* V_{rms} *(Line-Neutral)* *208* V_{rms} *(Line-Line)* f_{grid} *(nominal) = 60 Hz*
Output power	P_o *= 130 W (each phase)*
Input Voltage	V_{dc} *= 400 V (+200V, -200V)*
Switching devices	*Fairchild FCB20N60F MOSFET*
Output capacitor	C_o *= 1µF polypropylene film (each phase)*
Main inductor	*L = 270 µH (each phase), peak current= 4.5 A* R_{dc} *= 85 mΩ, magnetic core RM12/N95 ferrite,* *wire: Litz, 60 strands #38, 36.5 turns, air gap = 0.86 mm*

where, I_i ($i=1, 2$) is the peak boundary current for the upper and lower MOSFETs, respectively, V_{DS} is the MOSFET drain-source voltage, $f_{SW}(t)$ is the instantaneous switching frequency and $t_{S(H-L)}$ is the MOSFET turn-off time.

To avoid shoot through current between the MOSFETs, dead time is included in the complementary gate drives. During the dead time, the MOSFETs body diode conducts which results in power loss and is calculated as follows:

$$P_{BD}(t) = I_i(t) \times V_{SD} \times f_{sw}(t) \times (t_{d1} + t_{d2}) \quad (3\text{-}11)$$

where, V_{SD} is the diode forward voltage drop, t_{d1} and t_{d2} are the upper and lower MOSFET body diode conduction times, respectively.

MOSFET conduction loss is a function of the MOSFETs' on resistance and inductor rms current as follows:

$$P_{conduction} = \frac{R_{DS(ON)}}{T_S} \int_0^{T_S} {i_L}^2(t)\, dt \qquad (3\text{-}12)$$

where, $R_{DS(ON)}$ is the on-resistance of the MOSFET, T_S is the switching period and $i_{L(t)}$ is the instantaneous inductor current.

Since I_i and f_{sw} change at each switching cycle, referring to equations (3-1)-(3-6), instantaneous values have been considered in the loss calculation. The losses are computed for each switching cycle and then averaged over the entire 60-Hz line cycle. For example, the upper MOSFET turn-off switching loss in BCM with fixed reverse current for a positive half cycle is calculated as follows:

$$P_{upper\_sw(OFF)} = \frac{V_{DS} \times t_{s(H-L)}}{T} \int_0^{\frac{T}{2}} (2I_{REF} \sin(\omega t) + I_o) \times \frac{\left({}^{V_{dc}}/_{2}\right)^2 - (V_m \sin(\omega t))^2}{L V_{dc} (2I_{REF} \sin(\omega t) + 2I_o)}\, dt \qquad (3\text{-}13)$$

where, T is the 60-Hz line cycle period. Results were obtained using trapezoidal numerical integration in MATLAB.

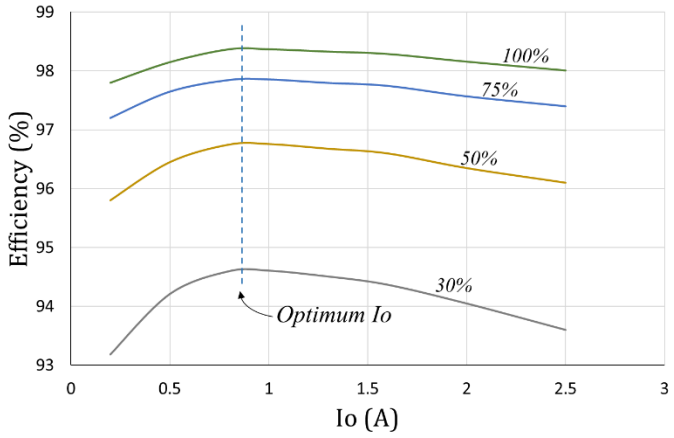
The core geometry and winding parameters for the 270 μH inductor were input into the inductor core loss model in the MATLAB program [56]. The results were then incorporated into the power loss model presented in this chapter. The loss model takes into account the varying switching frequency and core flux density to produce a more accurate core loss value. Winding losses consist of ac and dc losses. DC losses are simple function of inductor rms current and inductor dc resistance. AC losses are more complex and consist of skin effect and proximity effect which are a function of switching frequency and ac inductor current and tend to greatly increase the ac resistance of the inductor winding. The ac resistance value is often many times that of the dc

resistance. Note that since inductor current is bidirectional in all three modulation methods, there is no diode reverse recovery loss.

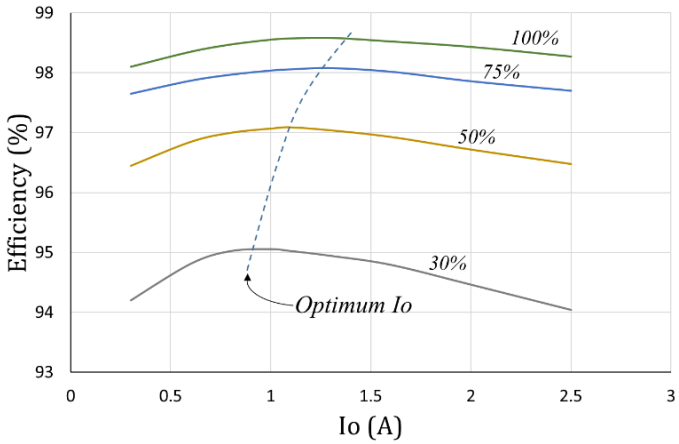
Figure 3-5 shows plots of efficiency as a function of peak current boundary at different output power levels for each of the three modulation methods. Efficiency is calculated using the loss model and plotted for various percentages of full load power for each modulation method. In BCM with fixed reverse current, maximum efficiency is obtained when the peak boundary current is 0.8 A, as shown in Figure 3-5(a). Peak current boundaries greater than the optimum value reduce the switching frequency and switching losses but increase the inductor rms current, MOSFET conduction losses and AC winding losses. However, peak current boundaries smaller than the optimum value increase the switching frequency significantly which causes increased inductor core loss. Similarly, in BCM with variable reverse current, the optimum peak current boundary changes slightly as power level increases and efficiency may be improved by dynamic adjustment of I_o, as depicted in Figure 3-5(b).

In BCM with fixed bandwidth, the plot of efficiency as a function of peak current boundaries at different output power levels shows that maximum efficiency is achieved when the peak current boundary is close to the minimum I_o required for ZVS as shown in Figure 3-4. Fixed bandwidth modulation lends itself to dynamic adjustment of the peak current boundary based on the value of load current in order to further improve efficiency.

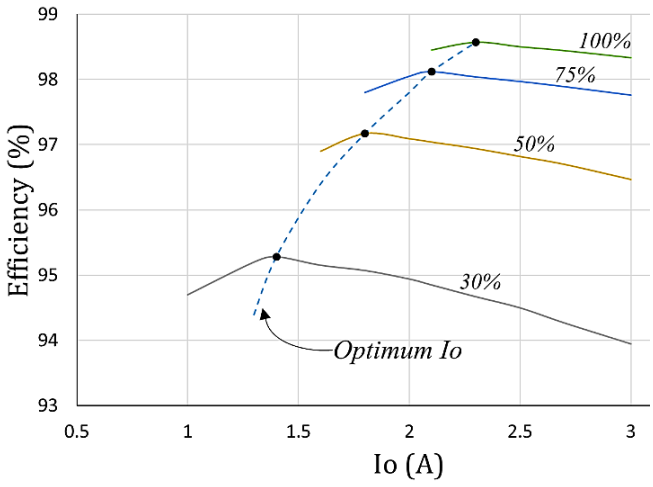
Note that for all three modulation methods, reducing the peak current boundaries below the minimum I_o required for ZVS results in hard switching and significantly increased switching losses. Plots based on the power loss model show that each of the three modulation methods has a unique range of optimum I_o value that will produce maximum efficiency for varying power levels.



(a)



(b)



(c)

Figure 3-5: Optimum peak current boundaries for three modulation methods at various power levels.

Notice that BCM with fixed reverse current and BCM with variable reverse current have a fairly narrow range of optimum I_o values, while BCM with fixed bandwidth has a wide range of optimum I_o values depending on the power level.

3.4 Proposed Dual-Zone Modulation

Based on the presented power loss model, a dual-zone modulation method is proposed to further improve efficiency. This modulation method provides two main benefits: the addition of one more soft switching transition and low inductor peak current. The proposed dual-zone modulation method divides the 60-Hz waveform into two distinct zones each having its own peak current boundaries and switching frequency range. Figure 3-6 shows the proposed dual-zone modulation method. Peak current boundaries and switching frequency for zone 1 can be determined as follows:

$$\begin{cases} I_{upper} = I_{REF}\sin(\omega t) + h\times I_o \\ I_{lower} = I_{REF}\sin(\omega t) - h\times I_o \end{cases} \quad \text{, if } |I_{REF}\sin(\omega t)| \le I_o \qquad (3\text{-}14)$$

$$f_{sw}(t) = \frac{\left(V_{dc}/_2\right)^2 - (V_m\sin(\omega t))^2}{LV_{dc}(2h\times I_o)} \qquad (3\text{-}15)$$

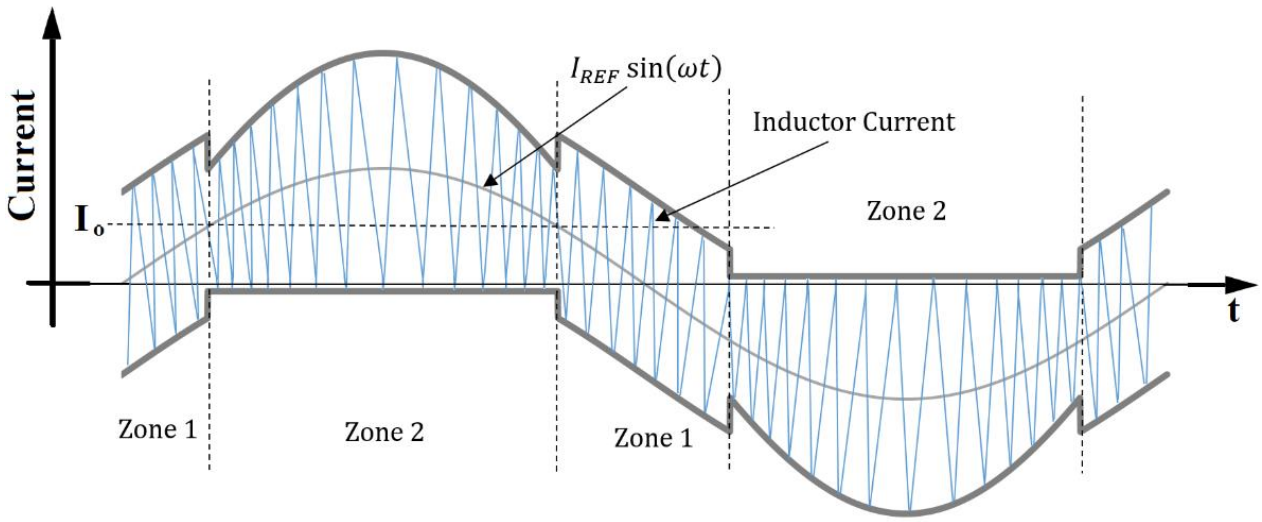


Figure 3-6: Dual-zone modulation method.

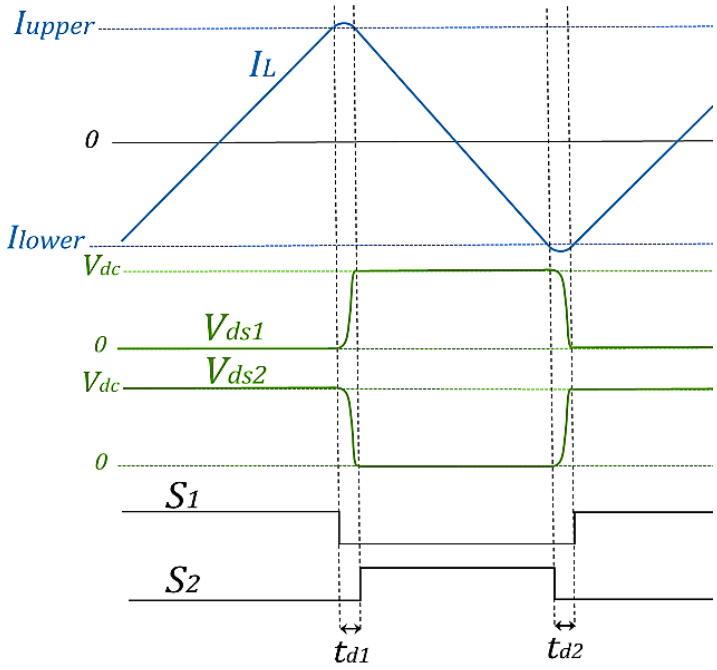
Similarly, peak current boundaries and switching frequency for zone 2 are calculated as follows:

$$\begin{cases} I_{upper} = 2I_{REF}\sin(\omega t) \\ I_{lower} = 0 \end{cases} \quad \text{, if } I_{REF}\sin(\omega t) > I_o$$

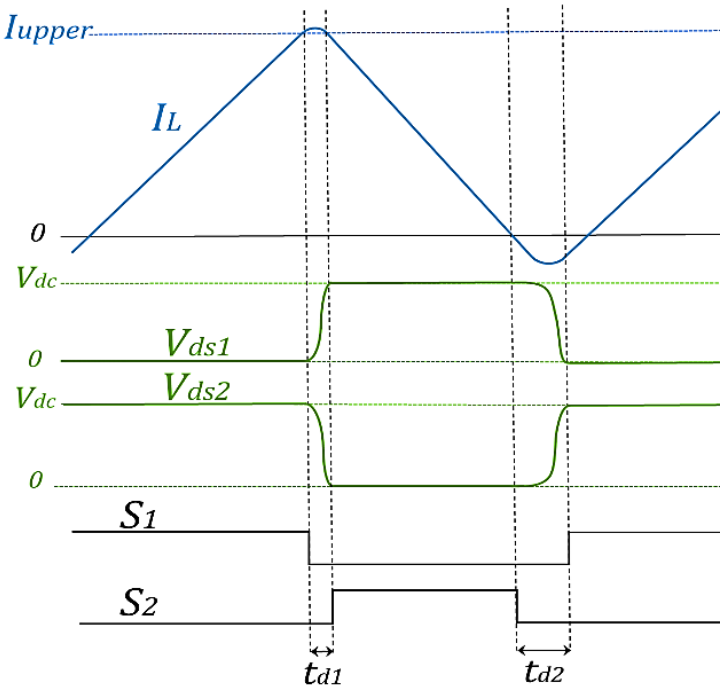
$$\begin{cases} I_{upper} = 0 \\ I_{lower} = 2I_{REF}\sin(\omega t) \end{cases} \quad \text{, if } I_{REF}\sin(\omega t) < -I_o \qquad (3\text{-}16)$$

$$f_{sw}(t) = \frac{\left({}^{V_{dc}}/_{2}\right)^2 - (V_m\sin(\omega t))^2}{LV_{dc}(2I_{REF}\sin(\omega t))} \qquad (3\text{-}17)$$

Zone 1 is similar to fixed bandwidth modulation where turn-on ZVS can be achieved for both MOSFETs. The peak current boundaries are set by the value of *h* as referenced in equation (3-11). Figure 3-7(a) shows an expanded view of switching waveforms for zone 1. When the upper MOSFET (S1) is conducting, inductor current increases linearly until it crosses the upper boundary at which time it is turned off under hard switching. During the first dead time (t_{d1}), both MOSFETs are off and the inductor current completely discharges the lower MOSFET's parasitic capacitance which provides turn-on ZVS for the lower MOSFET (S2). At the end of t_{d1}, the lower MOSFET is turned on and the inductor current decreases linearly until it reaches the lower current boundary. The lower MOSFET is then turned off under hard switching and the second dead time (t_{d2}) begins. During t_{d2}, the inductor current completely discharges the upper MOSFET's parasitic capacitance which allows the upper MOSFET to be turned on under ZVS. In zone 1, two of the four switching transitions are ZVS and the dead time intervals, t_{d1} and t_{d2}, are almost equal.



(a)



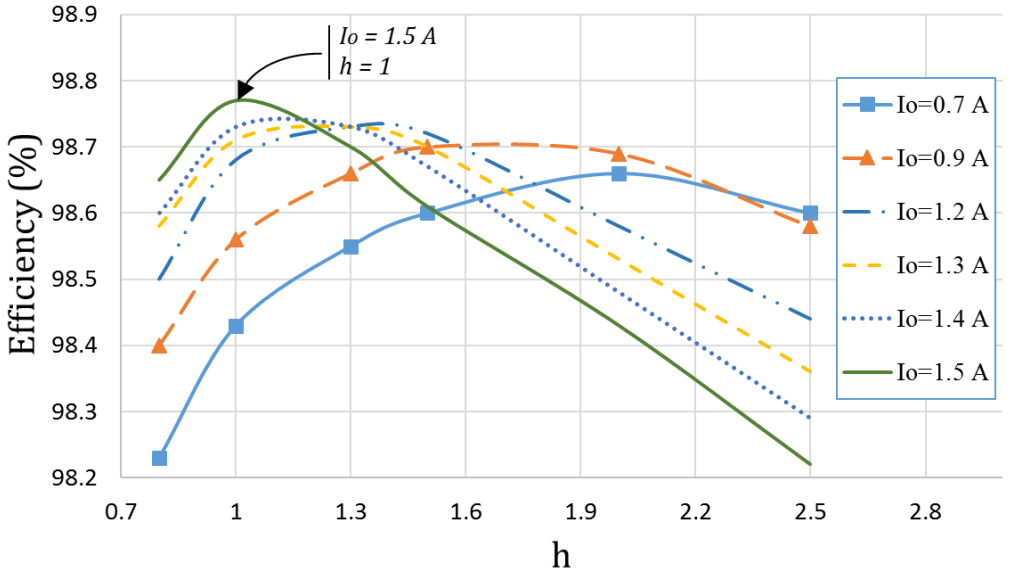
(b)

Figure 3-7: Dual-zone modulation method switching waveforms: (a) Zone 1, (b) Zone 2.

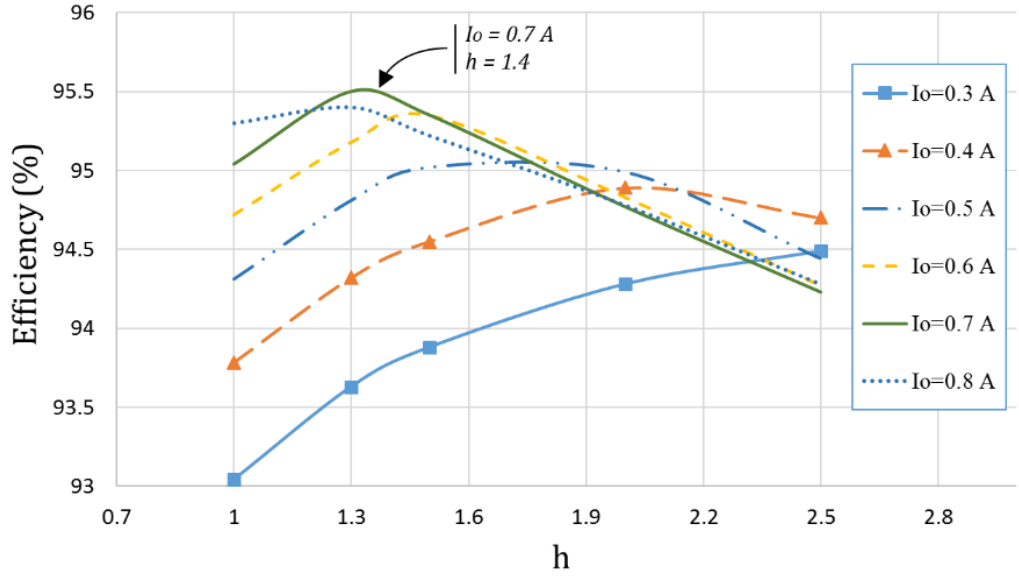
Zone 2 resembles BCM with fixed reverse current modulation where both ZVS and ZCS can be achieved. Figure 3-7(b) illustrates an expanded view of switching waveforms for zone 2. When the inductor current crosses the upper boundary, the upper MOSFET (S1) is turned off under hard switching. During the first dead time (t_{d1}), the inductor current completely discharges the lower MOSFET's parasitic capacitance which allows the lower MOSFET (S2) to be turned on under ZVS. As the inductor current falls to zero, the lower MOSFET is turned off under ZCS. During the second dead time (t_{d2}), the inductor current becomes negative and completely discharges the upper MOSFET's parasitic capacitance. If t_{d2} is sufficiently long so that the upper MOSFET's parasitic capacitance is completely discharged, the upper MOSFET can then be turned on under ZVS. In zone 2, three of the four switching transitions are soft switched but unlike zone 1, the dead time intervals, t_{d1} and t_{d2}, are quite different. Implementing Dynamic Dead Time Optimization (DDTO) [44] ensures that soft switching will be maintained in zone 2 over the entire operating range of the inverter.

The power loss model described in section III has been used for the dual-zone modulation method to predict the optimum combination of h and I_o at various power levels. Figure 8 shows plots of efficiency as a function of h for different values of I_o at 100% and 30% of rated power. At full load, maximum efficiency is achieved when I_o and h are 1.5 A and 1, respectively. At values of h below 1, soft switching is not guaranteed over the entire 60-Hz line cycle and efficiency decreases significantly. However, at 30% of rated power, the power loss analysis shows that the total loss is lowest when the value of h is greater than 1 for different values of I_o. Note that the values of I_o and h depend on the power level, with h varying from 1.6 to 1 and I_o varying from 0.7 A to 1.5 A as shown in Figure 8. In order to reduce computation time in the DSP, the optimum values of I_o and

h were calculated using MATLAB for a range of power levels and placed in a lookup table in the DSP. The DSP then selects the values of *h* and I_o based on the inverter operating power.



(a)



(b)

Figure 3-8: Optimum peak current boundaries for dual-zone modulation method at (a) 100%, (b) 30% of rated power.

Figure 3-9 shows inductor peak current boundaries for high power and low power using dual-zone modulation. At high power, zone 1 is larger than zone 2 which reduces the overall switching frequency, while at low power, zone 2 is larger than zone 1 which reduces the inductor rms current. In the proposed control technique, inductor rms current and switching frequency are controlled according to the output power level. At high power levels, the switching frequency range is similar to the other three modulation methods. However, the inductor rms current is reduced resulting in lower conduction losses. At low power levels, the switching frequency range is higher than that of the other three modulation methods. However, the increased switching losses are offset by the addition of one more soft switching transition. Also, inductor rms current is lower than that of the other three modulation methods which results in lower conduction losses. The combination of the additional soft switching transition and reduced inductor rms current produces an overall improvement in efficiency. Dual-zone modulation switching frequency range for 100% and 30% of rated power for half a 60-Hz line cycle is shown in Figure 3-10. The sudden change in switching frequency at 30% of rated power is due to the different current boundaries in transition from zone 1 to zone 2, referring to Figure 3-9(b) and equations (3-14) and (3-16).

The Power loss distribution for a 400-W three-phase half-bridge microinverter with four different BCM modulation methods is shown in Figure 3-11. Since BCM with fixed bandwidth has the highest inductor rms current, MOSFET conduction losses and inductor winding losses are the highest with this modulation. However, MOSFET conduction losses and inductor winding losses are the lowest with dual-zone modulation because of its lower inductor rms current. Since in BCM with fixed bandwidth, the peak current boundaries are constant over the entire 60-Hz line cycle, it has the narrowest switching frequency range and therefore the lowest inductor core loss.

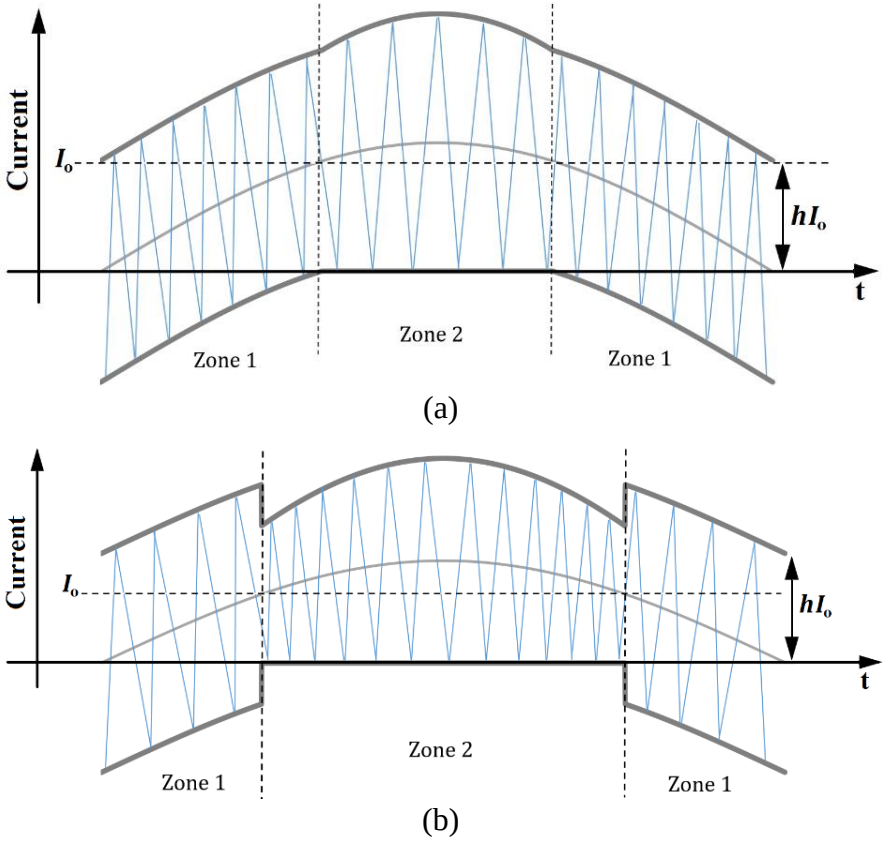


Figure 3-9: Dual-zone peak current modulation at (a) high power, (b) low power.

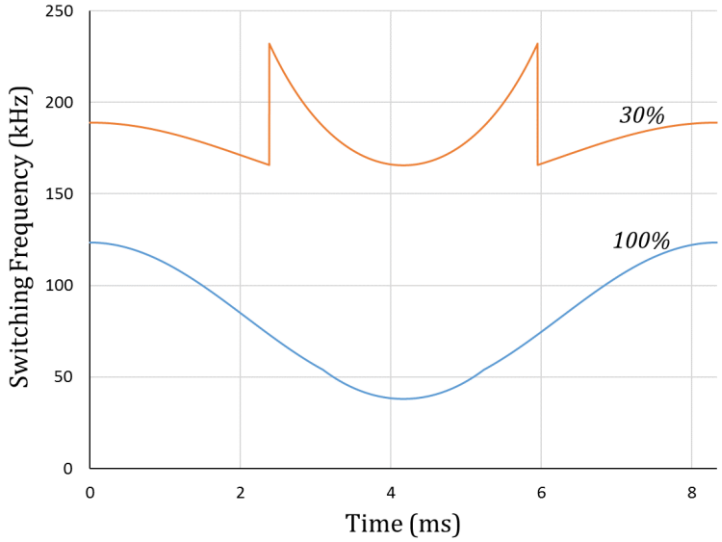


Figure 3-10: Dual-zone modulation switching frequency range for 100% and 30% of rated power.

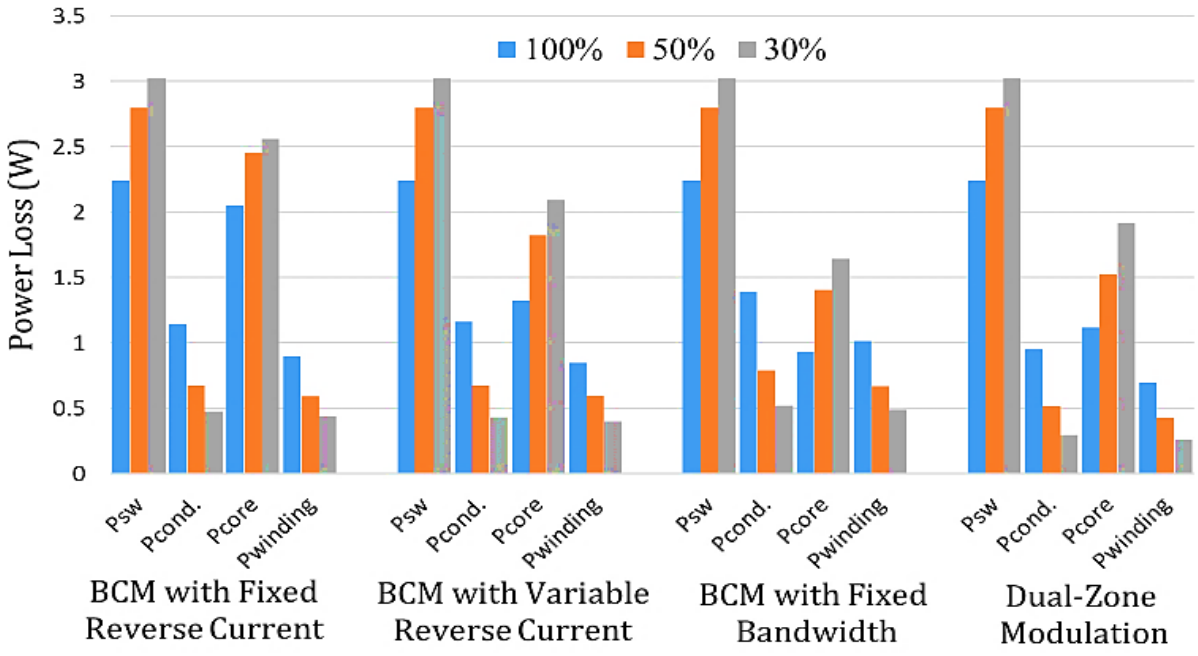


Figure 3-11: Power loss distribution with different BCM modulation methods at 100%, 50% and 30% of microinverter rated power.

Unlike BCM with fixed bandwidth, BCM with fixed reverse current modulation has the widest switching frequency range and therefore the highest inductor core loss due to the fact that switching frequency has a major impact on the inductor core loss calculation. As shown in Fig. 11, MOSFET switching losses are the largest portion of the total loss and increase as the output power level decreases. Even though the peak current boundaries decrease at light loads in all of the modulation methods, the switching frequency increases significantly resulting in increased switching losses.

Although dual-zone modulation has a higher switching frequency in zone 2 compared to the other three modulation methods, the peak current boundaries are lower and it has one more soft switching transition. The lower peak current boundaries reduce MOSFET conduction losses and

inductor winding losses thereby reducing overall power loss. Since the inductor peak current is low compared to the other three current modulation methods, the output filter inductor can be designed with fewer turns and a smaller gap which reduces inductor winding losses. Operating flux density can also be lower resulting in reduced core losses. The inductor could also be physically smaller which improves power density and also has lower core loss due to the reduction in core volume.

3.5 BCM Peak Current Control

Implementation of BCM peak current control for one phase in a DSP is shown in Figure 3-12. In order to guarantee ZVS over the entire grid cycle, the controller requires a precise measurement of the inductor current. Since the switching frequency varies over the 60-Hz line cycle and could go as high as 300 kHz depending on the modulation method used, inductor current cannot be accurately sampled using conventional A/D converters such as those found in digital signal controllers. To avoid this issue, the three-phase half-bridge microinverter prototype uses hybrid BCM current control [57], which is a combination of predictive control along with hardware reset. Predictive control calculates the duty cycle required for each operating point over the 60-Hz line cycle. Hardware reset is implemented by using the digital signal controller's internal high speed comparators to terminate the on time once the peak current threshold has been crossed.

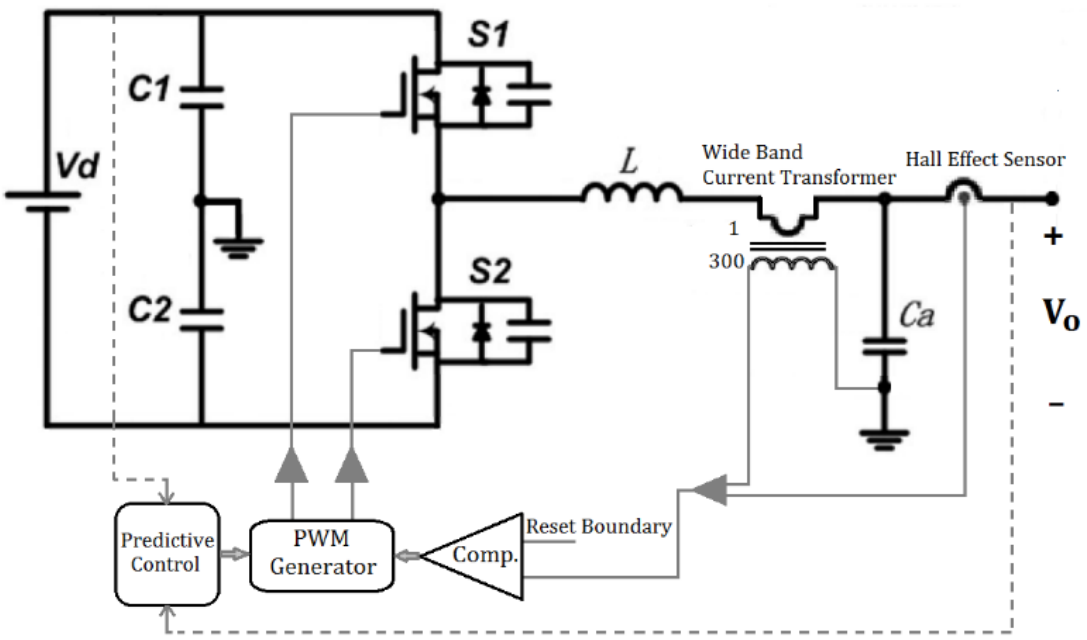


Figure 3-12: DSP implementation of BCM peak current control.

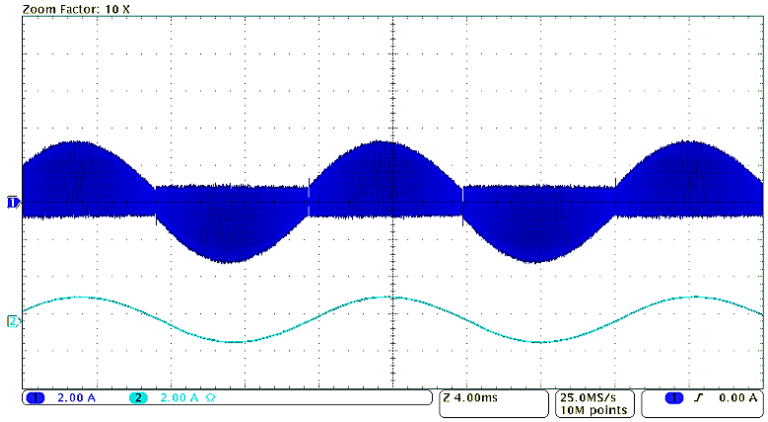
Hardware reset requires an accurate wide bandwidth current sensing circuit for measuring the inductor current. To accomplish this, a high performance nano-crystalline core 300:1 current transformer was designed and included in the prototype. This current transformer exhibits zero-degree phase shift at 60 Hz while having an upper bandwidth limit of greater than 500 kHz and can easily reproduce the inductor current waveform with no distortion. The Hall effect sensor is only required to measure dc current to ensure that the output current has no dc component. The current transformer and Hall effect sensor outputs are combined to produce an accurate inductor current measurement which is input to the high speed comparator inside the DSP.

3.6 Experimental Results

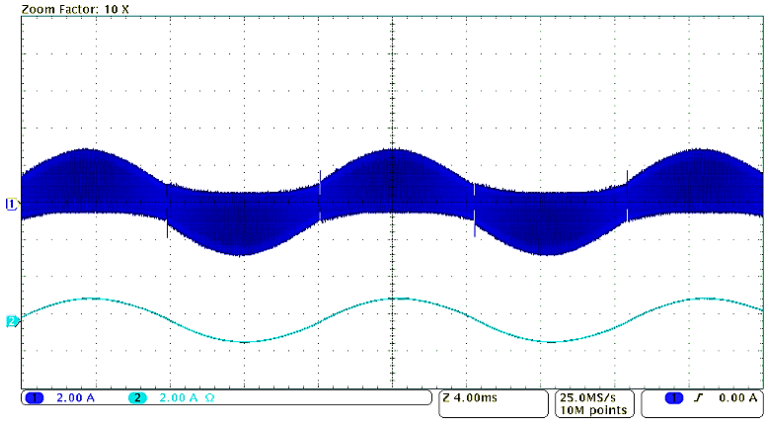
Experimental results were measured on a 400-W three-phase half-bridge microinverter prototype. The four previously discussed BCM modulation methods were implemented on a Microchip dsPIC33FJ16GS504. For the purpose of this experiment, the dc bus voltage was set to 400 V, the output inductor value was 270 μH for each phase and the line frequency was 60 Hz. The microinverter was tested using BCM with fixed reverse current, BCM with variable reverse current and BCM with fixed bandwidth [58], [59]. The filter inductor high frequency current and average current for each of the three modulation methods is shown in Figure 3-13.

Figure 3-14 shows the measured efficiency as a function of peak current boundary at different output power levels for each of the three modulation methods. Note that the empirical data closely resembles the efficiency calculated using the power loss model shown in Figure 3-5. The optimum I_o measured on the prototype for each of the three modulation methods is almost identical to the calculated values. The experimental results at high power and high values of I_o could not be obtained due to the saturation limit of the output filter inductor.

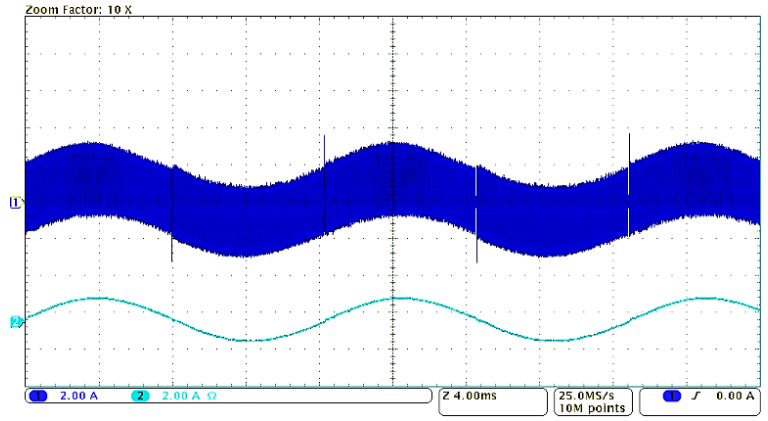
The filter inductor high frequency current and average current in Figure 3-15 were measured at high power and low power using the proposed dual-zone modulation technique. It can be seen that at high power, zone 1 is larger than zone 2 which reduces the overall switching frequency, while at low power, zone 2 is larger than zone 1 which reduces the inductor rms current. The switching waveforms for upper and lower MOSFETs in zone 1 and zone 2 were measured and are shown in Figure 3-16.



(a)

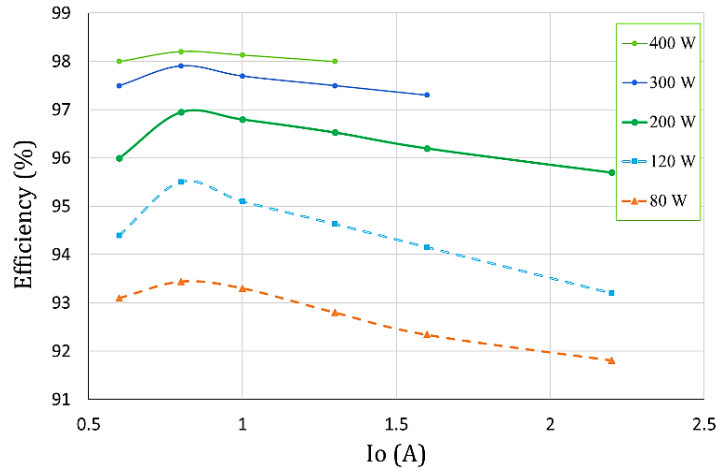


(b)

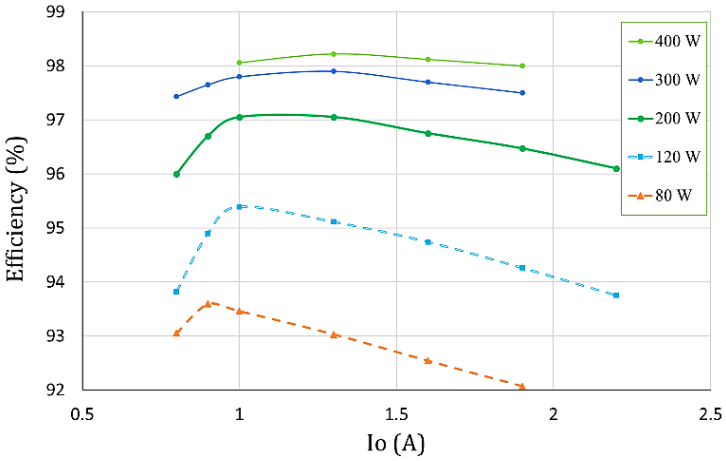


(c)

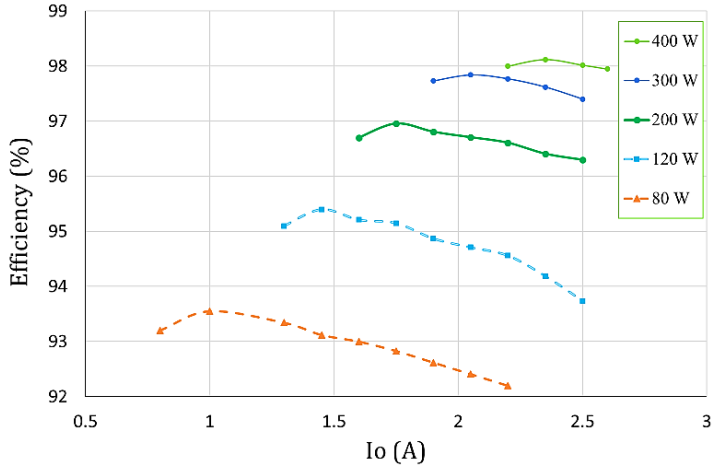
Figure 3-13: Filter inductor current and output current for (a) BCM with fixed reverse current, (b) BCM with variable reverse current, (c) BCM with fixed bandwidth.



(a)

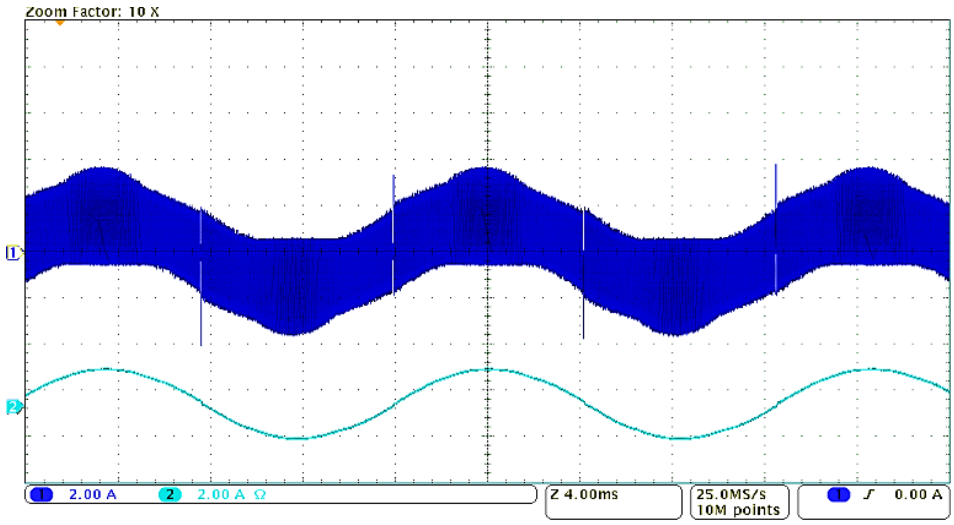


(b)

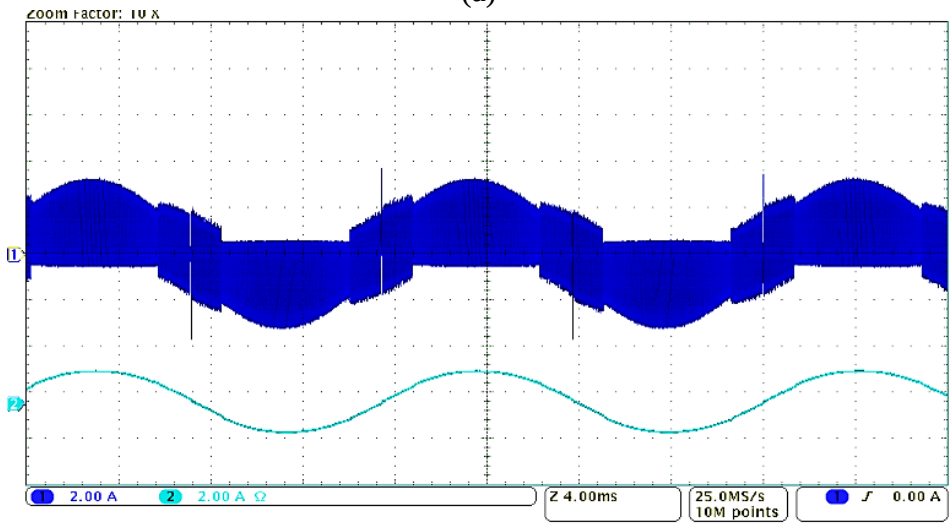


(c)

Figure 3-14: Optimum peak current boundaries for three modulation methods at various power levels.



(a)

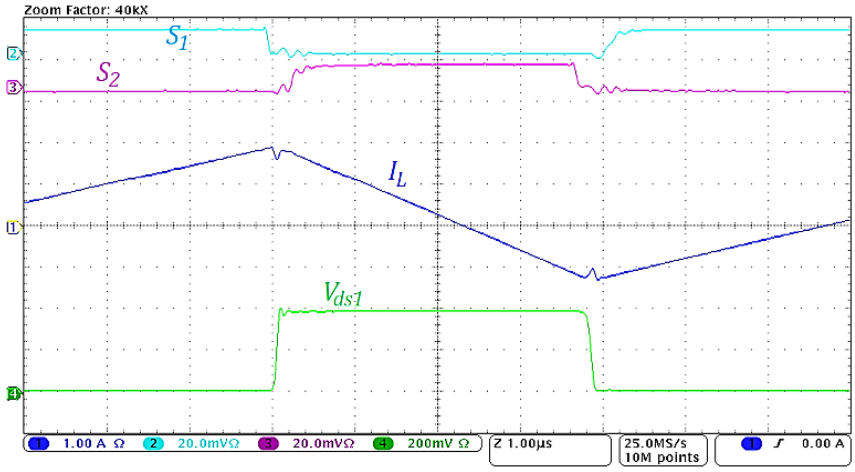


(b)

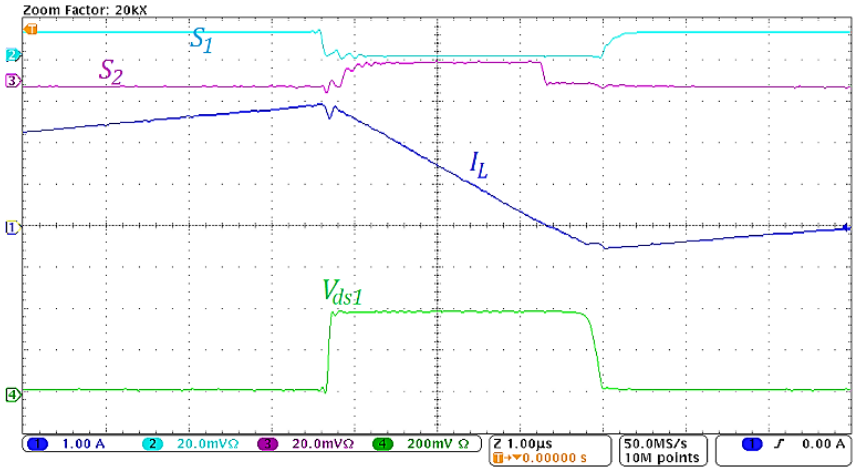
Figure 3-15: Dual-zone peak current modulation at (a) high power, (b) low power.

Referring to this figure in zone 1, the dead times are equal and turn-on ZVS is achieved for both MOSFETs. In zone 2, in addition to turn-on ZVS for both MOSFETs, turn-off ZCS is achieved for the lower MOSFET as shown in Figure 3-16(b). The dead times are quite different due to the small amount of inductor current that is available to discharge the MOSFET's parasitic

capacitance. The dead times in both zone 1 and zone 2 have been optimized over a 60-Hz line cycle using DDTO technique.



(a)



(b)

Figure 3-16: Dual-zone modulation method switching waveforms: (a) Zone 1, (b) Zone 2.

Figure 3-17 shows the maximum efficiency for each of the modulation methods measured with a Yokogawa PZ4000 power analyzer. It can be seen that higher efficiency can be achieved using the proposed dual-zone modulation method without additional circuit components or cost. THD is an

important parameter to be considered when designing an inverter. Full power current THD and inductor rms current for all four modulation methods are shown in Table 3-2. Dual-zone modulation exhibits the lowest inductor rms current and its current THD is well within the limits specified by IEEE 1547.

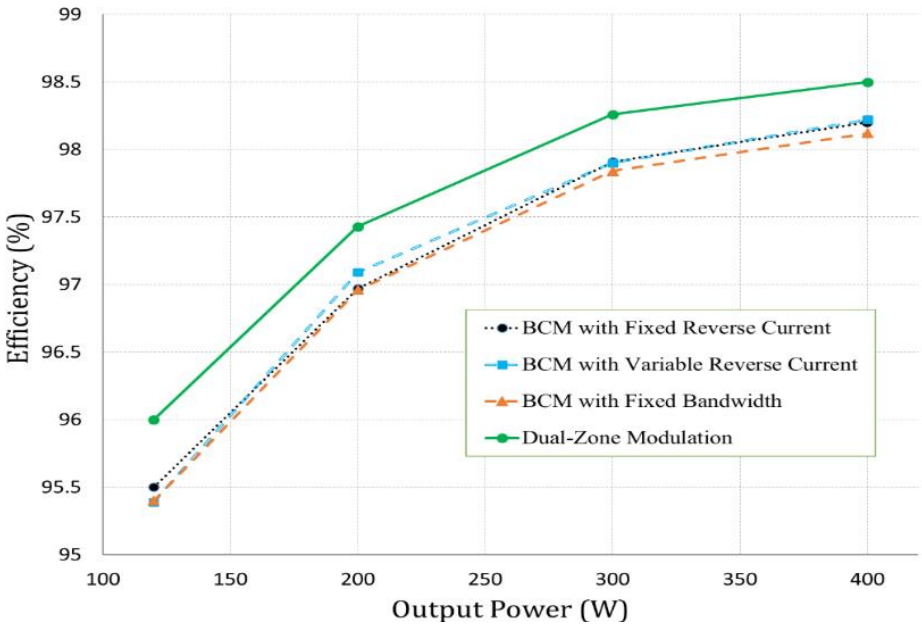


Figure 3-17: Microinverter output stage efficiency with different modulation methods.

Table 3-2: THD and Inductor RMS Current for Four Current Modulation Methods

	THD	RMS
BCM with Fixed Reverse Current	2.5%	1.59
BCM with Variable Reverse Current	1.9%	1.61
BCM with Fixed Bandwidth	1.4%	1.76
Dual-Zone Modulation	2.4%	1.45

3.7 Summary

In this chapter, a precise power loss model has been presented to calculate the optimum peak current boundary for three different modulation methods: BCM with fixed reverse current, BCM with variable reverse current, and BCM with fixed bandwidth. The power loss analysis shows that the optimum peak current boundary is almost constant for BCM with fixed reverse current at different power levels, while it varies with load current for BCM with variable reverse current and BCM with fixed bandwidth. The experimental results on a 400-W three-phase half-bridge microinverter prototype verify the accuracy of the power loss model.

A dual-zone modulation method along with an improved control method have been proposed in this chapter which further improve the efficiency of the microinverter prototype. Dual-zone modulation divides the 60-Hz waveform into two distinct zones. The power loss model was used to determine the size of each zone and calculate peak current boundaries. This modulation technique not only produces one more soft switching transition but also reduces inductor rms current which results in an overall improvement in efficiency. In addition, dual-zone modulation produces the lowest inductor peak current compared to the other three modulation methods so that the output filter inductor can be a smaller and more efficient design with fewer turns and lower flux density. The improved peak current control method proposed in this chapter consists of a wide-band current transformer that is accurate from 60 Hz to 500 kHz with zero-degree phase shift. The current transformer provides isolation and allows the entire inductor ac current waveform to be sensed. DDTO from previous work was also implemented on the prototype.

CHAPTER 4. ADVANCED DC LINK VOLTAGE REGULATION AND CAPACITOR MINIMIZATION FOR THREE-PHASE MICROINVERTER

4.1 Introduction

This chapter investigates DC link capacitor minimization for three-phase photovoltaic (PV) based microinverters. This concept minimizes the storage capacitance by allowing greater voltage ripple on the DC link. Therefore, the microinverter reliability can be significantly increased by replacing electrolytic capacitors with film capacitors. However, this intentionally increased voltage ripple can introduce harmonic distortion on the output current of the inverter stage if it is not mitigated by the DC link voltage controller. For this purpose, a robust and accurate DC link voltage control is proposed to filter this ripple while regulating the DC link voltage without using any additional circuit components. The experimental results on a 400-W three-phase half-bridge microinverter prototype validate the theoretical analysis of the DC link capacitor minimization and show that a significant reduction of the DC link capacitor requirement can be achieved. The proposed high accuracy DC link voltage controller is also implemented on this prototype to demonstrate very low harmonic distortion of the inverter output current while tightly regulating the DC link voltage even during transients.

4.2 Determining Minimum DC Link Capacitor Value

Figure 4-1 shows a common two-stage microinverter topology. This topology which connects the PV panel to the grid consists of a DC/DC converter and a DC/AC inverter along with a decoupling (DC link) capacitor in between the two stages. Typically, the first stage provides a MPPT function

for the PV panel and boosts its low voltage to a constant DC link voltage. The energy produced by the PV panel is stored in the DC link capacitor. The second stage converts the energy stored in this capacitor into ac current which is injected into the grid synchronized to the grid voltage.

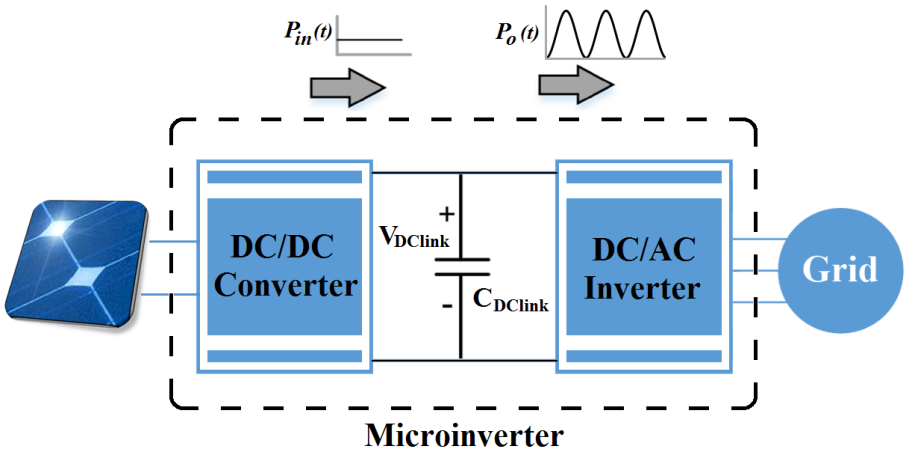


Figure 4-1: Two-stage microinverter topology.

The DC link capacitor is charged by DC input power from the PV and discharged by the pulsating power injected into the grid. The ac current drawn from the DC link capacitor introduces a harmonic component on the DC link voltage. This voltage ripple on the DC link capacitor may adversely affect the inverter efficiency and the quality of power injected into the grid [60], [61]. Total harmonic distortion (THD) of the inverter output current will increase as the DC link voltage ripple increases [42]. This natural phenomenon cannot be mitigated by the inverter control. The following expression approximates the DC link instantaneous voltage for a single-phase full-bridge inverter:

$$v_{DC_{link}}(t) \approx V_{DC_{link},avg.} + \frac{P_{in}}{2\omega V_{DC_{link},avg.} C_{DC_{link}}} sin(2\omega t) \qquad (4\text{-}1)$$

where, $V_{DClink,avg.}$ is the average DC link voltage, P_{in} is the input power from the PV panel and C_{DClink} is the DC link capacitance. Referring to (4-1), higher capacitance results in smaller voltage

ripple on the DC link.

Electrolytic capacitors with high capacitance are often used for the DC link in order to mitigate this effect. Since electrolytic capacitors have a limited lifetime, they are not compatible with the microinverter systems lifetime which can be longer than 20 years [62]. Therefore, in order to increase the microinverter systems lifetime, electrolytic capacitors can be replaced by lower capacitance film capacitors which are more tolerant of voltage ripple. Since film capacitors are more expensive than electrolytic capacitors, it is advantageous to minimize the size of these capacitors [63].

Since the DC link voltage normal operating range must be greater than the grid voltage plus some operating headroom, the DC link capacitor rated voltage should be higher than this value with the addition of some voltage derating. Therefore, the DC link voltage must be maintained within this range by the inverter controller. This controller regulates the DC link voltage with variations in input power, output voltage and load current transients. A feedback loop senses the DC link voltage, compares it with the desired reference voltage and determines the inverter output current in order to regulate the DC link voltage. This controller should have sufficient bandwidth to compensate for input and output transients. The inverter output current THD must be also considered when designing the DC link voltage control system [64], [65]. A coupled inductor filter is presented in [66] to eliminate a specific frequency from the output of a DC/DC converter. A control loop compensator is proposed in [41] and [42] to minimize the output harmonics using a high-order filter with low-frequency poles and zeros. A third ripple port in a single-phase inverter is presented in [67] to cancel the DC link voltage ripple using a small capacitor which requires additional circuit components. A digital finite impulse response (FIR) filter is introduced in [36]

to sample the DC link voltage at a low-frequency rate and then calculate the average voltage in order to reduce output current harmonics. However, the controller response to even small power transients is quite slow.

As shown in Figure 4-1, the DC link capacitor is charged by DC input power from the PV panel. The capacitor is discharged by the pulsating power injected into the grid which results in voltage ripple. In this section, the energy stored in the DC link capacitor is calculated to determine the relationship between the DC link voltage ripple and storage capacitance value. This relationship along with the DC link voltage normal operating range will then be used to determine the size of the storage capacitor.

The grid voltage for a three-phase system is defined as

$$\begin{aligned} V_a(t) &= V_m \sin(\omega t) \\ V_b(t) &= V_m \sin\left(\omega t - {}^{2\pi}/_{3}\right) \\ V_c(t) &= V_m \sin\left(\omega t + {}^{2\pi}/_{3}\right) \end{aligned} \qquad (4\text{-}2)$$

and assuming unity power factor, the three-phase inverter output current injected into the grid is expressed as follows:

$$\begin{aligned} i_a(t) &= I_m \sin(\omega t) \\ i_b(t) &= I_m \sin\left(\omega t - {}^{2\pi}/_{3}\right) \\ i_c(t) &= I_m \sin\left(\omega t + {}^{2\pi}/_{3}\right) \end{aligned} \qquad (4\text{-}3)$$

where, V_m and I_m are the peak values of voltage and current, respectively. The inverter instantaneous output power can be derived from (4-2) and (4-3) as follows:

$$P_a(t) = \frac{V_m I_m}{2}(1 - cos(2\omega t))$$
$$P_b(t) = \frac{V_m I_m}{2}\left(1 - cos(2\omega t - {}^{4\pi}/_{3})\right) \quad (4\text{-}4)$$
$$P_c(t) = \frac{V_m I_m}{2}\left(1 - cos(2\omega t + {}^{4\pi}/_{3})\right)$$

Assuming 100% efficiency for the two-stage microinverter, the average output power must be equal to the PV input power expressed as follows:

$$P_{o,avg} = \langle P_a(t) + P_b(t) + P_c(t) \rangle = P_{in} = 3\frac{V_m I_m}{2} \quad (4\text{-}5)$$

where, $P_{o,avg}$ is the inverter average output power and P_{in} is the input power from the PV panel. Since a half-bridge topology uses a bipolar DC link ($V^{\pm}_{DClink}$) with identical capacitors as shown in Figure 4-2, half of the output power is drawn from each capacitor. Similarly, each capacitor is charged by half of the input power from the PV panel. Note that in buck-derived topologies, during positive half cycles, grid current is predominantly sourced from V^{+}_{DClink} due to the fact that the upper MOSFET's on time is greater than that of the lower MOSFET. Similarly, during negative half cycles, negative grid current is predominantly sourced from V^{-}_{DClink}.

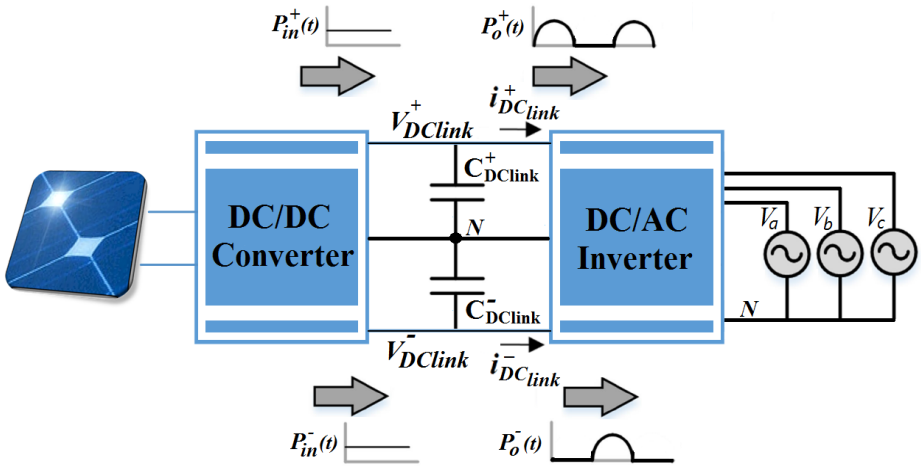


Figure 4-2: Three-phase half-bridge microinverter with a bipolar DC link.

Figure 4-3 shows simulation results of average main inductor current (sourced from V^{+}_{DClink} and V^{-}_{DClink}) and grid current on the same scale for single-phase operation. It can be seen that during positive half cycles, almost all of the positive grid current is indeed sourced from V^{+}_{DClink} (i^{+}_{DClink}), although some amount of current is sourced from i^{-}_{DClink}. The same is true for negative half cycles.

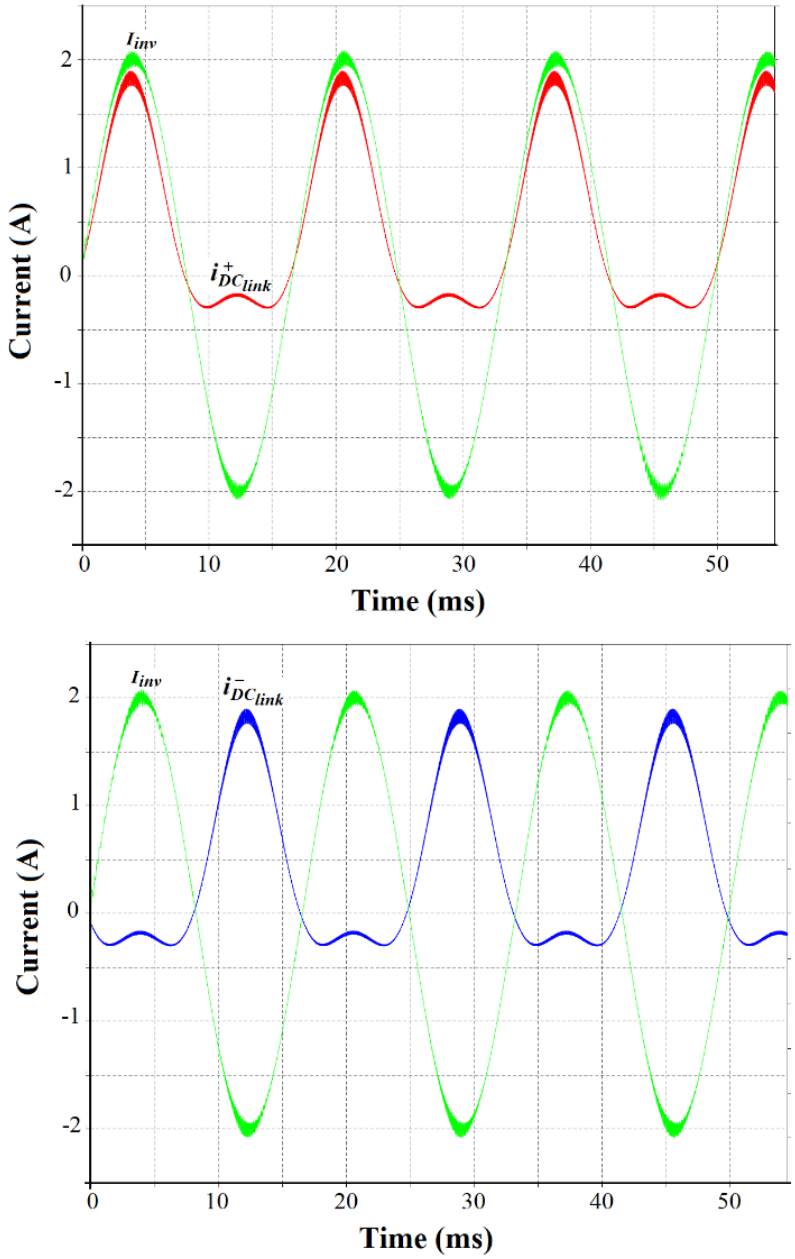


Figure 4-3: Simulation results of single-phase operation.

For simplicity, it is assumed that all positive current is sourced from V^{+}_{DClink} and all negative current is sourced from V^{-}_{DClink}. Since the circuit is symmetrical, the analysis will be performed on only one of the capacitors. Therefore, the definition from (4-5) can be rewritten as follows:

$$P^{+}_{o,avg} = \langle P^{+}_{a}(t) + P^{+}_{b}(t) + P^{+}_{c}(t) \rangle = P^{+}_{in} = \frac{3}{2}\frac{V_m I_m}{2} \quad (4\text{-}6)$$

where, $P^{+}_{o,avg}$ is the inverter average output power sourced by C^{+}_{DClink} capacitor, P^{+}_{in} is the half of input power from the PV panel to charge C^{+}_{DClink} capacitor and $P^{+}_{a,b,c}(t)$ is the inverter instantaneous output power for each phase during positive half cycles. For example, $P^{+}_{a}(t)$ is defined as

$$P^{+}_{a}(t) = \begin{cases} P_a(t), & 0 \le t < \frac{T}{2} \\ 0, & \frac{T}{2} \le t < T \end{cases} \quad (4\text{-}7)$$

Figure 4-4 shows the key waveforms of the microinverter. It can be seen that V^{+}_{DClink} is increasing when $P^{+}_{in} > P^{+}_{o}(t)$ during intervals *(0,T/6)*, *(T/3,T/2)* and *(2T/3,5T/6)*, and similarly V^{+}_{DClink} is decreasing when $P^{+}_{in} < P^{+}_{o}(t)$ during intervals *(T/6,T/3)*, *(T/2,2T/3)* and *(5T/6,T)*. Therefore, the minimum and maximum values of V^{+}_{DClink} ($V^{+}_{DClink\_min}$ and $V^{+}_{DClink\_max}$) occur at 0, T/3, 2T/3 and T/6, T/2, 5T/6, respectively.

Referring to Figure 4-4, the energy required to charge C^{+}_{DClink} during the interval *(0,T/6)* can be calculated as

$$\Delta E = \int_0^{\frac{T}{6}} (P^{+}_{in} - P^{+}_{o}(t))\, dt = \frac{V_m I_m}{2\omega}\left(\frac{\sqrt{3}}{2} - \frac{\pi}{6}\right) \quad (4\text{-}8)$$

where, $P^{+}_{o}(t)$ is $P^{+}_{a}(t)+P^{+}_{c}(t)$ in this interval as shown in Figure 4-4. The stored energy in C^{+}_{DClink} can also be expressed as follows:

$$\Delta E = \frac{1}{2} C^{+}_{DC_{link}} \left(V^{+^2}_{DC_{link}\_max} - V^{+^2}_{DC_{link}\_min} \right) \quad (4\text{-}9)$$

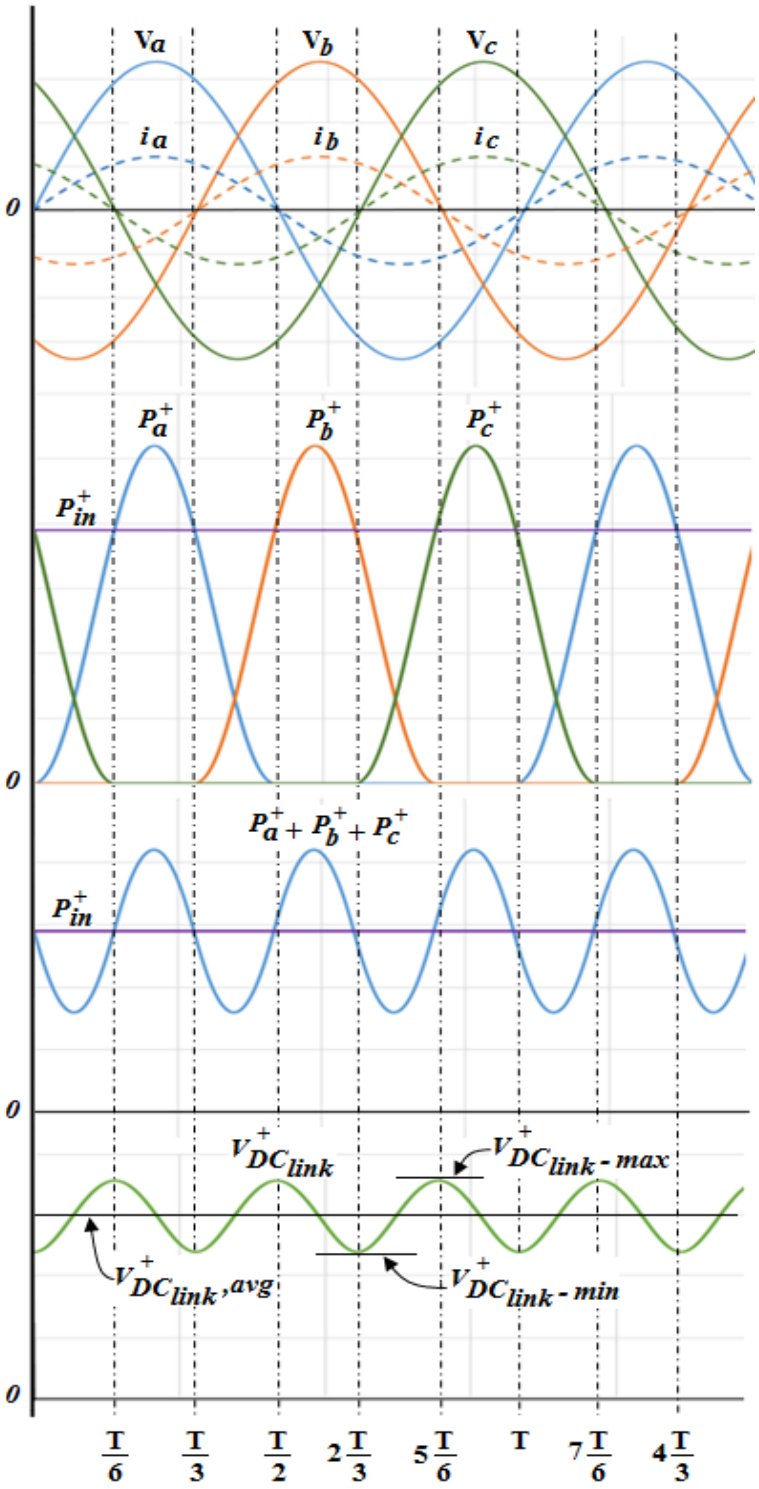


Figure 4-4: Key waveforms of the microinverter.

Therefore, the relationship between the DC link voltage ripple and storage capacitance is derived from (8) and (9) as

$$C^{+}_{DC_{link}} = \frac{V_m I_m}{2.\omega.\Delta V^{+}_{DC_{link}}.V^{+}_{DC_{link},avg}}\left(\frac{\sqrt{3}}{2} - \frac{\pi}{6}\right) \quad (4\text{-}10)$$

where, ΔV^{+}_{DClink} is the DC link voltage ripple and $V^{+}_{DClink,avg}$ is the DC link average voltage defined as follows:

$$\begin{cases} \Delta V^{+}_{DC_{link}} = V^{+}_{DC_{link\_}max} - V^{+}_{DC_{link\_}min} \\ V^{+}_{DC_{link},avg} = \frac{V^{+}_{DC_{link\_}max} + V^{+}_{DC_{link\_}min}}{2} \\ \omega = \frac{2\pi}{T} \end{cases} \quad (4\text{-}11)$$

Therefore, the DC link voltage of a three-phase half-bride topology can be expressed in (4-12). Referring to this equation and Figure 4-4, the DC link voltage contains a third harmonic component which is superimposed on the average voltage compared to a single-phase full-bridge inverter which has a second harmonic component.

$$V^{+}_{DC_{link}}(t) = V_{DC_{link},avg.} + \frac{V_m I_m}{4\omega V^{+}_{DC_{link},avg} C^{+}_{DC_{link}}}\left(\frac{\sqrt{3}}{2} - \frac{\pi}{6}\right) sin\left(3\omega t - \frac{\pi}{2}\right) \quad (4\text{-}12)$$

Note that in a balanced three-phase three-wire system, there is no third harmonic ripple on the DC link. This is also true for the three-phase four-wire system described in the chapter if the DC link voltage is measured from V^{+}_{DClink} to V^{-}_{DClink}. However, if V^{+}_{DClink} and V^{-}_{DClink} are measured with respect to Neutral, their ripple voltage contains a third harmonic component. The Neutral current also contains a very small third harmonic component along with high frequency component. This is an artifact of high-frequency modulation and more noticeable with small values of DC link capacitor.

Similarly, the energy required to discharge C^{+}_{DClink} during the interval *(T/6,T/3)* can be calculated

as

$$\Delta E = \int_{T/6}^{T/3} (P_o^+(t) - P_{in}^+)\, dt = \frac{V_m I_m}{2\omega}\left(\frac{\sqrt{3}}{2} - \frac{\pi}{6}\right) \quad (4\text{-}13)$$

where, $P^+_o(t)$ is equal to $P^+_a(t)$ during this interval as shown in Figure 4-4. The same relationship between the DC link voltage ripple and storage capacitance which was derived in (4-10) can be obtained from (4-9) and (4-13).

Referring to (4-10), the size of storage capacitor can be significantly reduced if the DC link voltage ripple (ΔV^+_{DClink}) is slightly increased. This allows lower value film capacitors to be used instead of electrolytic capacitors.

In an effort to calculate the DC link instantaneous voltage, the energy stored in C^+_{DClink} can be determined as

$$E_C(t) = E_C(0) + \int_0^t (P_{in}^+ - P_o^+(t))\, dt \quad (4\text{-}14)$$

This equation can also be expressed as

$$\frac{1}{2} C^+_{DC_{link}} V^{+^2}_{DC_{link}}(t) =$$

$$\frac{1}{2} C^+_{DC_{link}} V^{+^2}_{DC_{link\_min}} + \int_0^t \frac{V_m I_m}{2}\left(-\frac{1}{2} + cos(2\omega t) + cos(2\omega t + \frac{4\pi}{3})\right) dt \quad (4\text{-}15)$$

From (4-15), the DC link instantaneous voltage can be derived in (4-16).

$$V^+_{DC_{link}}(t) = \sqrt{V^{+^2}_{DC_{link\_min}} + \frac{V_m I_m}{2\omega C^+_{DC_{link}}}\left(-\omega t + sin(2\omega t) + sin(2\omega t + \frac{4\pi}{3}) + \frac{\sqrt{3}}{2}\right)} \quad (4\text{-}16)$$

The voltage-sourced inverter is a buck-derived topology, so the input voltage must be greater than the peak grid voltage plus some operating headroom to accommodate transients and variations in grid voltage (±10%), i.e.

$$V^+_{DC_{link}}(t) \geq V_m sin(\omega t) + h \quad (4\text{-}17)$$

From (4-16) and (4-17), $V^{+}_{DClink\_min}$ can be determined in (4-18).

$$V^{+}_{DC_{link}\_min} \geq$$

$$\sqrt{\frac{V_m^2}{2} - \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\frac{\sqrt{3}}{2} + \frac{V_m I_m}{2C^{+}_{DC_{link}}}t - \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}sin\left(2\omega t + \frac{4\pi}{3}\right) - Asin(2\omega t + \alpha) + 2hV_m sin(\omega t) + h^2}$$

$$A = \sqrt{\left(\frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\right)^2 + \left(\frac{V_m^2}{2}\right)^2}, \quad \alpha = tan^{-1}\frac{\frac{V_m^2}{2}}{\frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}} \qquad (4\text{-}18)$$

Referring to this equation, a higher grid voltage and a larger C^{+}_{DClink} result in a higher $V^{+}_{DClink\_min}$. Note that a reduction in C^{+}_{DClink} will also increase the DC link maximum voltage. Therefore, in order to avoid high voltage stress on the microinverter power devices, the maximum allowable DC link voltage must be also taken into account. The energy stored in C^{+}_{DClink} can also be expressed as

$$E_C(t) = E_C\left(\frac{T}{6}\right) - \int_{\frac{T}{6}}^{t}(P_o^{+}(t) - P_{in}^{+})\,dt \qquad (4\text{-}19)$$

Similarly, $V^{+}_{DClink\_max}$ is derived in (4-20).

$$V^{+}_{DC_{link}\_max} \geq$$

$$\sqrt{\frac{V_m^2}{2} + \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\left(\frac{\pi}{3} + \frac{\sqrt{3}}{2}\right) - \frac{V_m I_m}{2C^{+}_{DC_{link}}}t - Asin(2\omega t + \alpha) + 2hV_m\,sin(\omega t) + h^2} \qquad (4\text{-}20)$$

In order for one to effectively use the analysis presented in this chapter, a number of design parameters must be determined. These include system power level ($V_m I_m/2$), minimum acceptable DC link voltage ($V^{+}_{DClink\_min}=V_m+h$), maximum acceptable DC link voltage ($V^{+}_{DClink\_max}$) and operating headroom (h). once defined, these parameters can be used along with equation (4-10) to determine the minimum acceptable DC link capacitor value.

Figure 4-5 shows the bipolar DC link voltage and grid voltage with different values of storage capacitance for the microinverter prototype when the DC link average voltage is set at +200 V and -200 V with a balanced grid voltage of 120 V_{rms}. Referring to the figure, as the storage capacitance decreases, the DC link voltage ripple increases. With 200 V DC link average voltage and a 40 μF storage capacitor typically used in a conventional design, 2 V of voltage ripple (peak-to-peak) is observed. Note that further reduction of C^{+}_{DClink} can be achieved if the DC link average voltage is increased. However, in order to keep the switching losses in the MOSFETs low, it is advantageous to select the lowest possible value of DC link average voltage. Similarly, Figure 4-6 shows the DC link voltage ripple with an unbalanced grid voltage where phase A is at nominal voltage, phase B at -10% of nominal voltage and phase C at +10% of nominal voltage.

As mentioned earlier, the relationship between the DC link voltage ripple and storage capacitance along with the DC link voltage normal operating range is taken into account to determine the minimum acceptable value of the storage capacitor. Therefore, equations (4-10), (4-18) and (4-20) along with the microinverter operating parameters are used in MATLAB to calculate the minimum value of the DC link capacitor. The results show that an 8 μF storage capacitor with 205 V DC link average voltage is minimum for the microinverter prototype. A film capacitor greater than or equal to the minimum value should be selected. Polypropylene film capacitors in this range of values are readily available in the market.

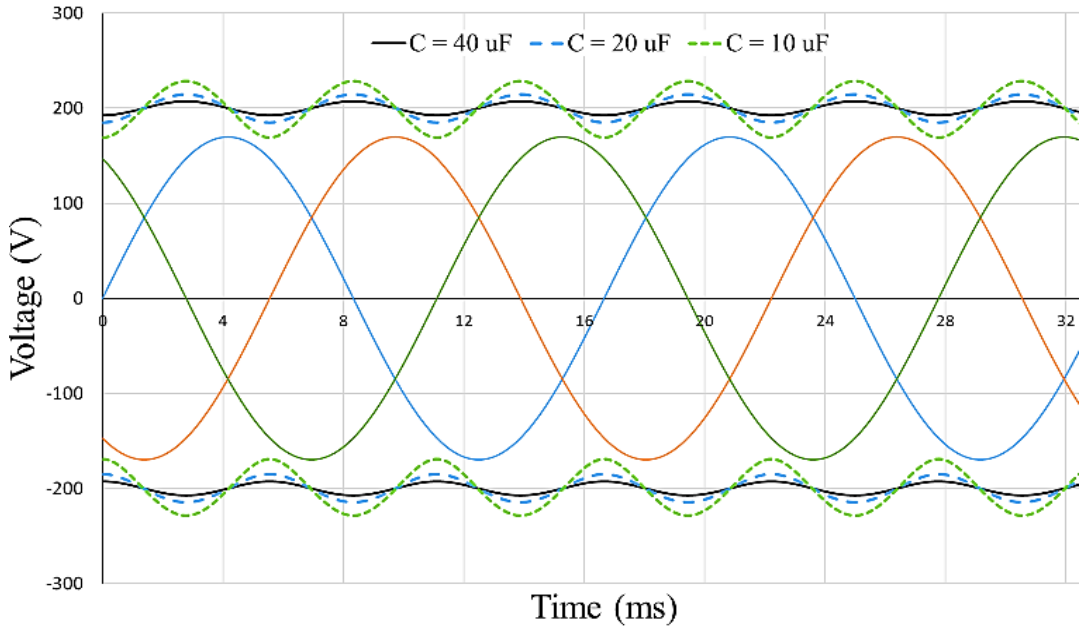


Figure 4-5: Bipolar DC link voltage ripple with different storage capacitance in a balanced system.

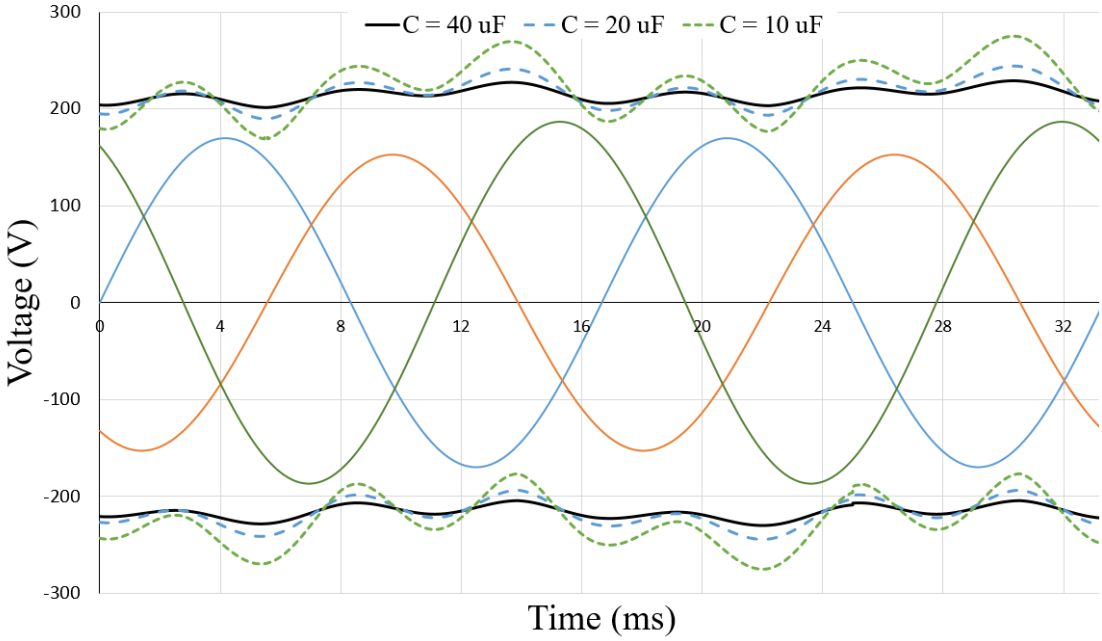


Figure 4-6: Bipolar DC link voltage ripple with different storage capacitance in an unbalanced system.

Notice that if this voltage ripple is not filtered by the inverter DC link voltage control, it may introduce harmonic distortion in the output current injected into the grid. An advanced DC link voltage control which is able to address this issue will be presented in the next section.

4.3 Advanced DC Link Voltage Control

This section describes the design of an advanced DC link voltage control system which tightly regulates the DC link average voltage without being adversely affected by the presence of relatively large voltage ripple. This controller is designed to measure the DC link average voltage without the need for additional circuit components or digital filters.

A typical DC link voltage control system is shown in Figure 4-7. The controller senses the DC link voltage and compares it with the average voltage reference. The compensator uses the error signal to determine the inverter output peak current. A sinusoidal output current which is synchronized to the grid voltage using a phase-locked loop (PLL) is generated. In effect, the DC link voltage is regulated by adjusting the inverter output peak current. When the input power from the PV panel is greater than the average output power injected into the grid, the DC link voltage will increase. In order to balance the input PV power with the average output power, the controller increases the inverter output peak current. The opposite occurs when the input PV power is less than the average output power.

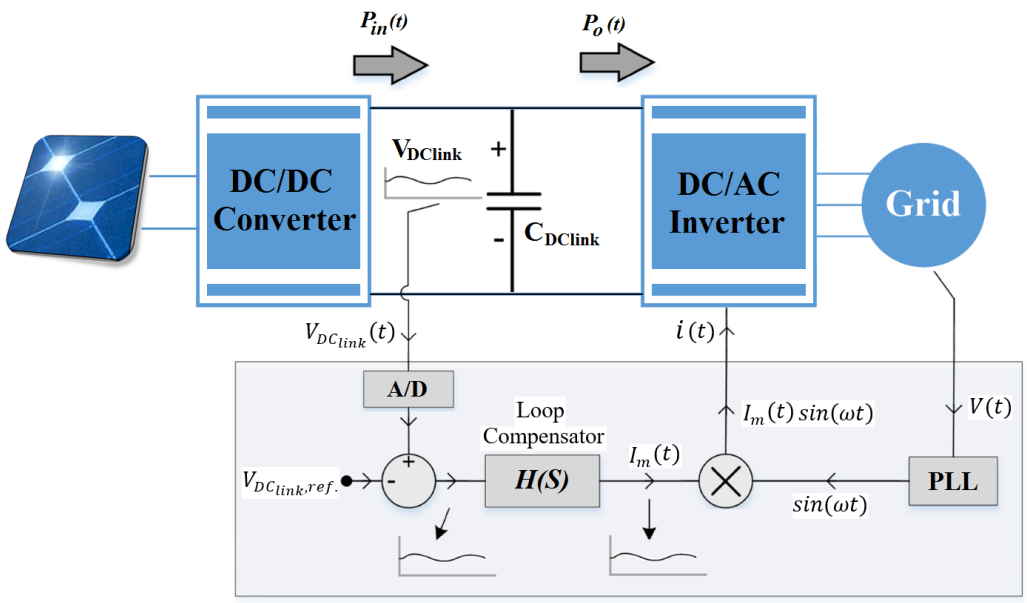


Figure 4-7: Typical DC link voltage control system.

Typical controllers sample the DC link voltage at several kilohertz. Consequently, the voltage ripple is included in the sampling causing the error signal to have a harmonic content. If the harmonic content in the error signal is left unfiltered, it will cause harmonic distortion in the inverter output current injected into the grid. Placing an analog low-pass filter in the DC link voltage sense path will reduce the loop bandwidth and result in poor transient response. Digital low-pass filters of varying complexity have also been proposed in order to mitigate the harmonic content in the error signal [68]-[70]. These filters provide some improvement but are unable to eliminate all of the harmonic content.

If the DC link voltage is sampled at specific predetermined points, an accurate measurement of the DC link average voltage can be made with little or no harmonic distortion. Since most inverters contain a highly accurate PLL in order to synchronize with the grid voltage, the PLL can also be used to control the exact timing of the A/D's that sample the DC link voltage. A diagram of the

proposed PLL-based DC link voltage control system is shown in Figure 4-8. Since the harmonics present in the DC link voltage are phase locked to the grid voltage as shown in Figure 4-5, this relationship can be used to accurately predict where the ac component of the ripple voltage intersects the DC link average voltage value. If the A/D's sample at this time, they will be sampling the DC link average voltage without any of the distortion found in other DC link voltage regulators.

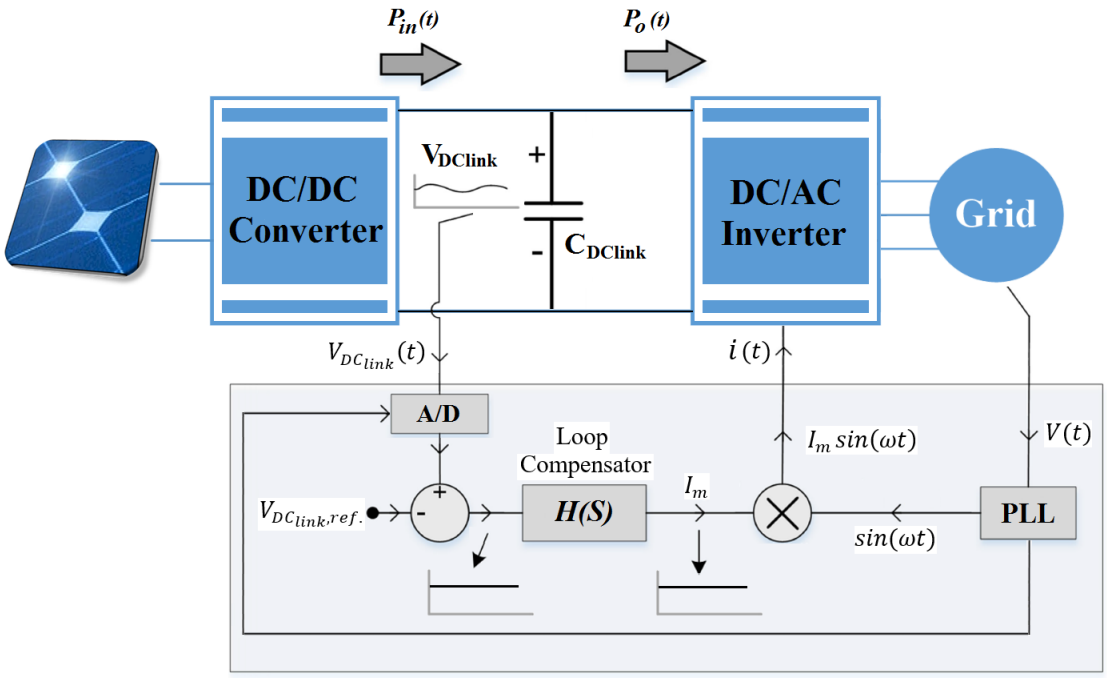


Figure 4-8: Proposed PLL-based DC link voltage control system.

This simple and accurate sampling method uses existing controller functional blocks and eliminates the need for additional analog and digital filters while minimizing the inverter output current distortion. The error signal input to the loop compensator is now a dc value which produces a dc peak current reference. This peak current reference multiplied by the PLL generates a pure sine wave input to the pulse-width modulation (PWM) block [71].

The objective of the DC link voltage controller is to control the average value of the DC link

voltage independent of the voltage ripple. Since the DC link voltage control loop is neither linear nor time invariant, a direct analysis to find a dynamic model of the control system is highly complex. A simple method is to develop a linear and time invariant dynamic model using signals that are averaged over half a line cycle [72], [73]. Notice that this averaged model does not contain harmonic components. As mentioned earlier, the difference between the input power from the PV panel and the inverter average output power injected into the grid determines the DC link voltage as defined in (4-21).

$$V_{DC_{link}}(t) = \frac{1}{C_{DC_{link}}} \int_{-\infty}^{t} \frac{P_{in} - P_{o,avg.}}{V_{DC_{link}}(t)} dt \qquad (4\text{-}21)$$

Referring to this equation, since $V_{DClink}(t)$ is the controlled variable, the division by $V_{DClink}(t)$ is nonlinear. A Taylor approximation can linearize it as follows [73]:

$$\frac{1}{V_{DC_{link}}(t)} \approx \frac{1}{V_{DC_{link},avg.}} \qquad (4\text{-}22)$$

Therefore, the DC link voltage control loop can be illustrated in Figure 4-9. The loop compensator generates the inverter output peak current reference which controls the average output power. The difference between the input power from the PV panel and the inverter average output power injected into the grid divided by the DC link average voltage defines the DC link capacitor current. The integral of this current divided by the DC link capacitance determines the DC link average voltage. This voltage is then sampled by the A/D synchronized with the PLL and compared with the DC link reference voltage. The loop compensator uses the error signal to continually adjust the inverter output peak current. Note that a PI controller is used for the loop compensator.

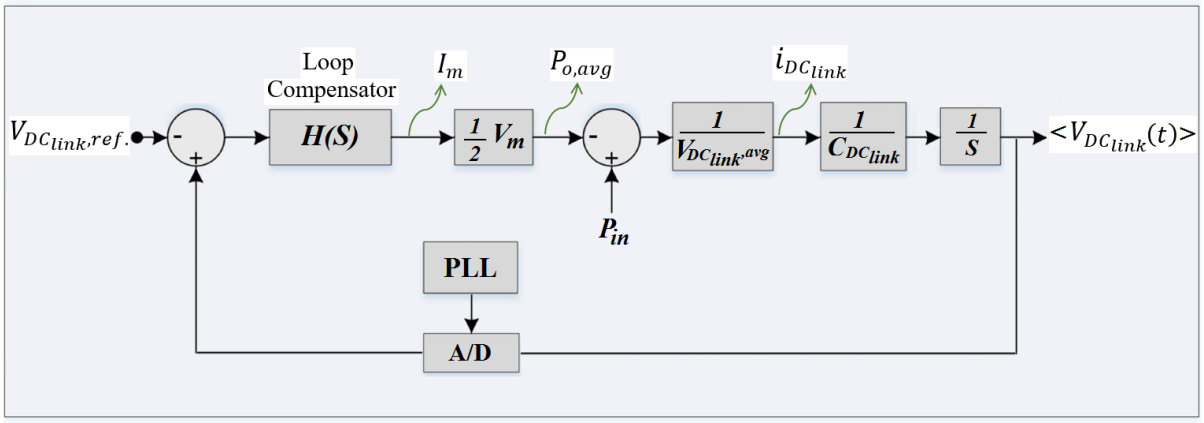


Figure 4-9: PLL-based DC link voltage control dynamic model.

4.4 Experimental Results

The two-stage 400-W three-phase microinverter prototype topology is shown in Figure 4-10. The DC/DC stage is a full-bridge LLC resonant converter with a voltage doubler secondary which boosts the input PV voltage of 45 V to the DC link voltage of +200 VDC and -200 VDC. As minimized in section II, two 8 μF polypropylene film capacitors rated at 300 V are used as the storage capacitor in the DC link. The second stage is a three-phase half-bridge inverter with LCL filter which is connected to a 120 V_{rms}, 60 Hz, three-phase output voltage. A STM32F103C8T7 is used to control the LLC resonant input stage and a DSPIC33FJ16GS504 is used to control the output inverter stage. The microinverter prototype operating parameters are shown in Table 4-1. The inverter stage operates in peak current controlled boundary conduction mode (BCM) [56], [74] with a switching frequency that varies from 20 kHz to 180 kHz. Zero voltage switching (ZVS) is achieved for both upper and lower MOSFETs on each phase. The MPPT function is provided by the DC/DC stage control which senses the PV input voltage and current and maximizes the input power from the PV source.

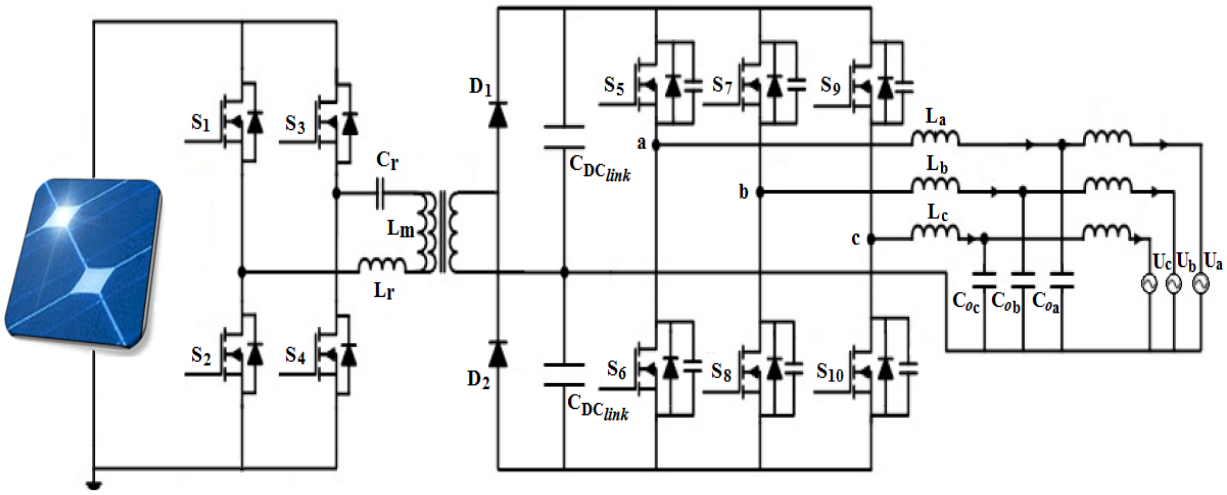
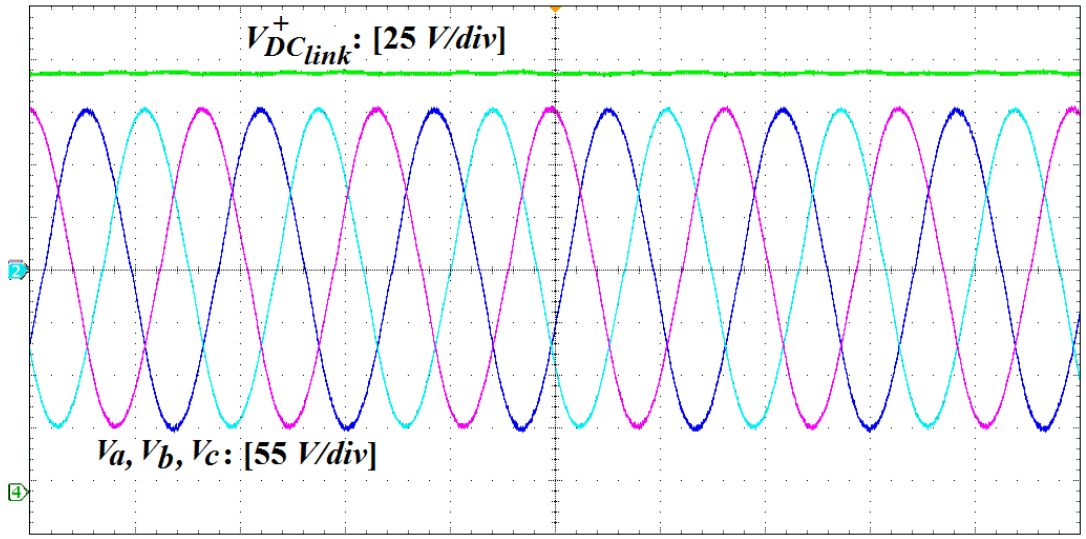


Figure 4-10: Two-stage three-phase microinverter prototype topology.

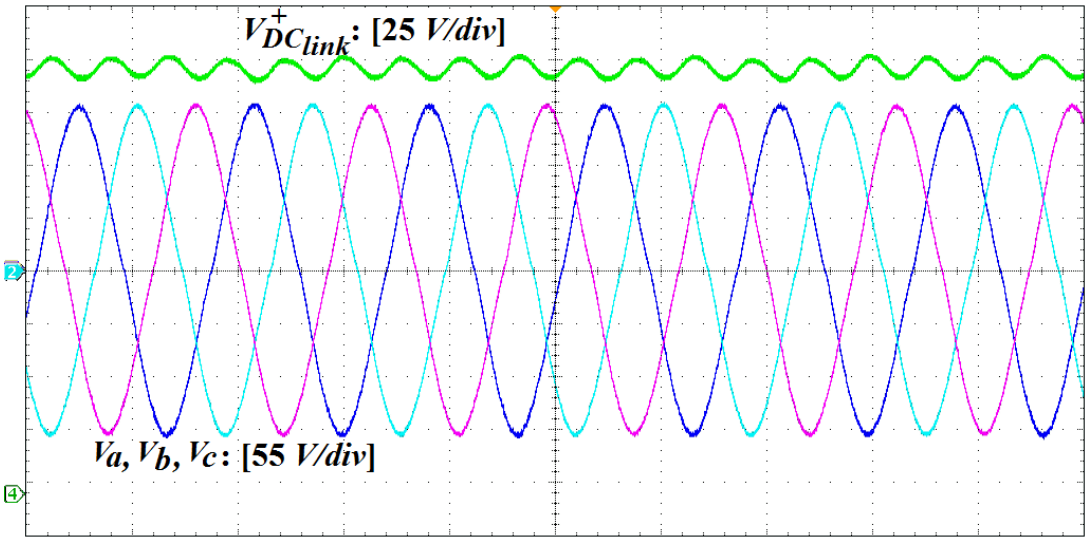
Figure 4-11 shows the microinverter's DC link voltage and the three-phase output voltage with 40 μF and 8 μF DC link capacitors operating at 300 W. With 40 μF of DC link capacitance, the peak to peak voltage ripple is 2 V which is 1% of the ±200 V DC link. The 8 μF capacitor produces 15 V peak to peak voltage ripple which is 7.5% of the DC link average voltage of 205 VDC. Using the lower value of DC link capacitor results in an approximately one-third size reduction which reduces the microinverter cost and improves power density. The relatively high 180-Hz voltage ripple present on the DC link capacitor produces negligible self heating due to its inherent low ESR compared to that of electrolytic capacitors. In general, film capacitors are more reliable and have a longer lifetime than electrolytic capacitors.

Table 4-1: Microinverter Prototype Operating Parameters

PV panel	*Peak power = 400 W, V_{mpp} = 48.7 V, I_{mpp} = 8.2 A*
Grid parameters	*V_{grid} (nominal) = 120 V_{rms} (Line-Neutral) 208 V_{rms} (Line-Line), f_{grid} (nominal) = 60 Hz*
Output power	*P_o = 130 W (each phase)*
Resonant inductance	*L_r = 1.9 µH*
Resonant capacitor	*C_r = 680 nF*
Magnetizing inductance	*L_m = 10.3 µH*
DC link capacitor	*C_{DClink} = 40 µF polypropylene film, C_{DClink}(minimized) = 8 µF polypropylene film*
DC link voltage	*V_{DClink} = 400 V (+200V, -200V)*
Primary switches	*Fairchild FDB047N10 MOSFET*
Secondary switches	*Fairchild FCB20N60F MOSFET*
Rectifier diodes	*STTH3R06S (D_1, D_2)*
Primary controller	*STM32F103C8T7*
Secondary controller	*DSPIC33FJ16GS504*
Output capacitor	*C_o = 1µF polypropylene film (each phase)*
Inverter main inductor	*L = 270 µH (each phase), peak current= 4.5 A, R_{dc} = 85 mΩ, magnetic core RM12/N95 ferrite, wire: Litz, 60 strands #38, 36.5 turns, air gap = 0.86 mm*



(a)



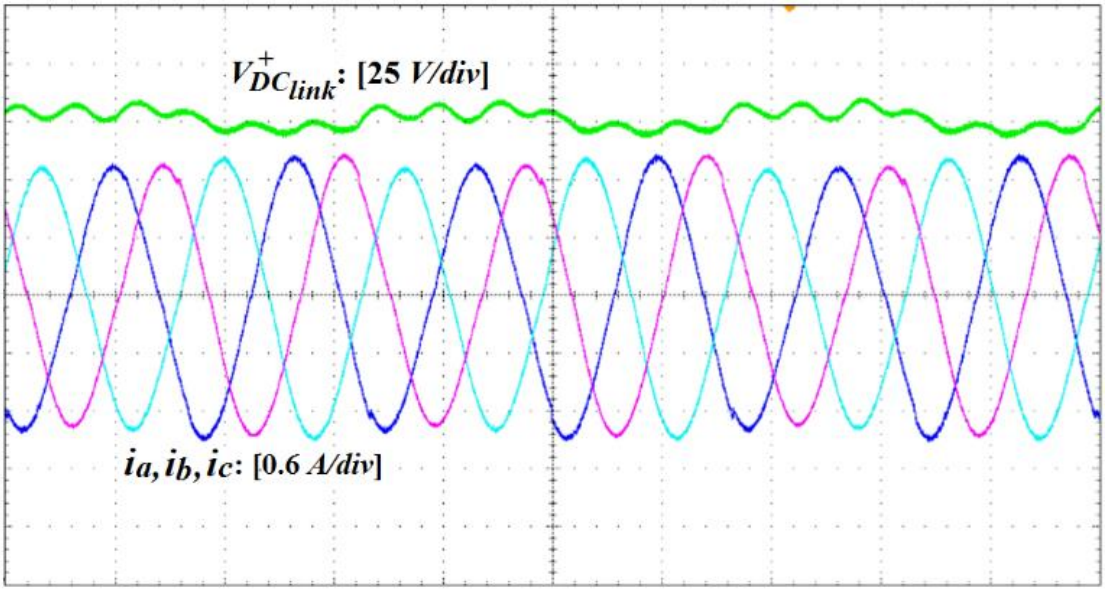
(b)

Figure 4-11: Microinverter DC link voltage and three-phase output voltage with (a) 40 μF and (b) 8 μF DC link capacitors.

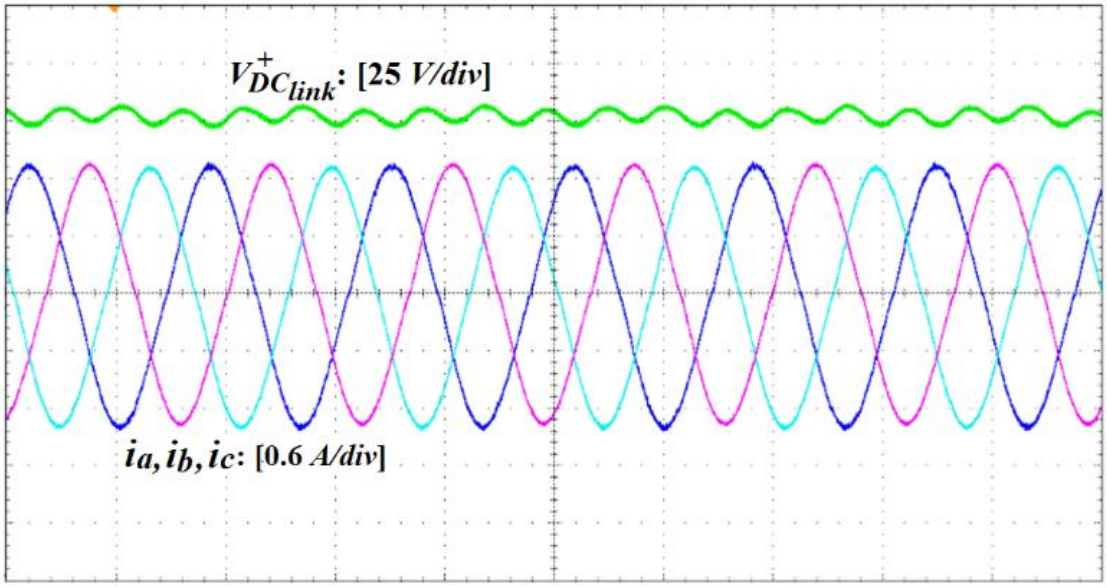
Figure 12 shows three-phase inverter output current and DC link voltage. Figure 4-12(a) shows unstable system dynamic performance that is exhibited when the PI compensator coefficients, K_P and K_I, are intentionally chosen to produce zero-degree open loop phase margin. Since the control

loop is unstable, it is continually adjusting the inverter output current in an attempt to reach the steady state DC link average voltage. In order to maintain a balanced system and avoid unwanted harmonics in the output current waveform, the current in all three phases is adjusted only every line cycle. This causes the low frequency anomaly seen in the DC link voltage in Figure 4-12(a). Figure 4-12(b) shows stable properly compensated dynamic system operation when the PI compensator coefficients are selected to produce 45^{O} open loop phase margin. Notice that the low-frequency DC link voltage and output current instability of Figure 4-12(a) is eliminated. Inverter output current THD with the properly compensated controller was measured at 1.84% which is far exceeds the requirements of the IEEE 1457 standard. The proposed controller makes it possible to employ the methodology used in section II to minimize the DC link capacitor value by avoiding the adverse impacts of the relatively high DC link peak-to-peak voltage ripple.

Figure 4-13 shows PV input current, inverter output current and DC link voltage with an input power step from 260 W to 375 W. With the input power from the PV panel at 260 W, this system is in stable operation with the inverter output power equal to the input power and a constant DC link average voltage. When the input power steps from 260 W to 375 W, the DC link voltage rises due to the positive power imbalance ($P_{in} > P_{o,avg}$). The controller senses the increase in the DC link voltage and commands a corresponding increase in the inverter output current reference which increases the inverter output power to drive the system back to a state of equilibrium. Note that the response is relatively fast and smooth with steady state reached after five cycles of the ac line.



(a)



(b)

Figure 4-12: Three-phase inverter output current and DC link voltage in (a) an unstable and (b) a stable system.

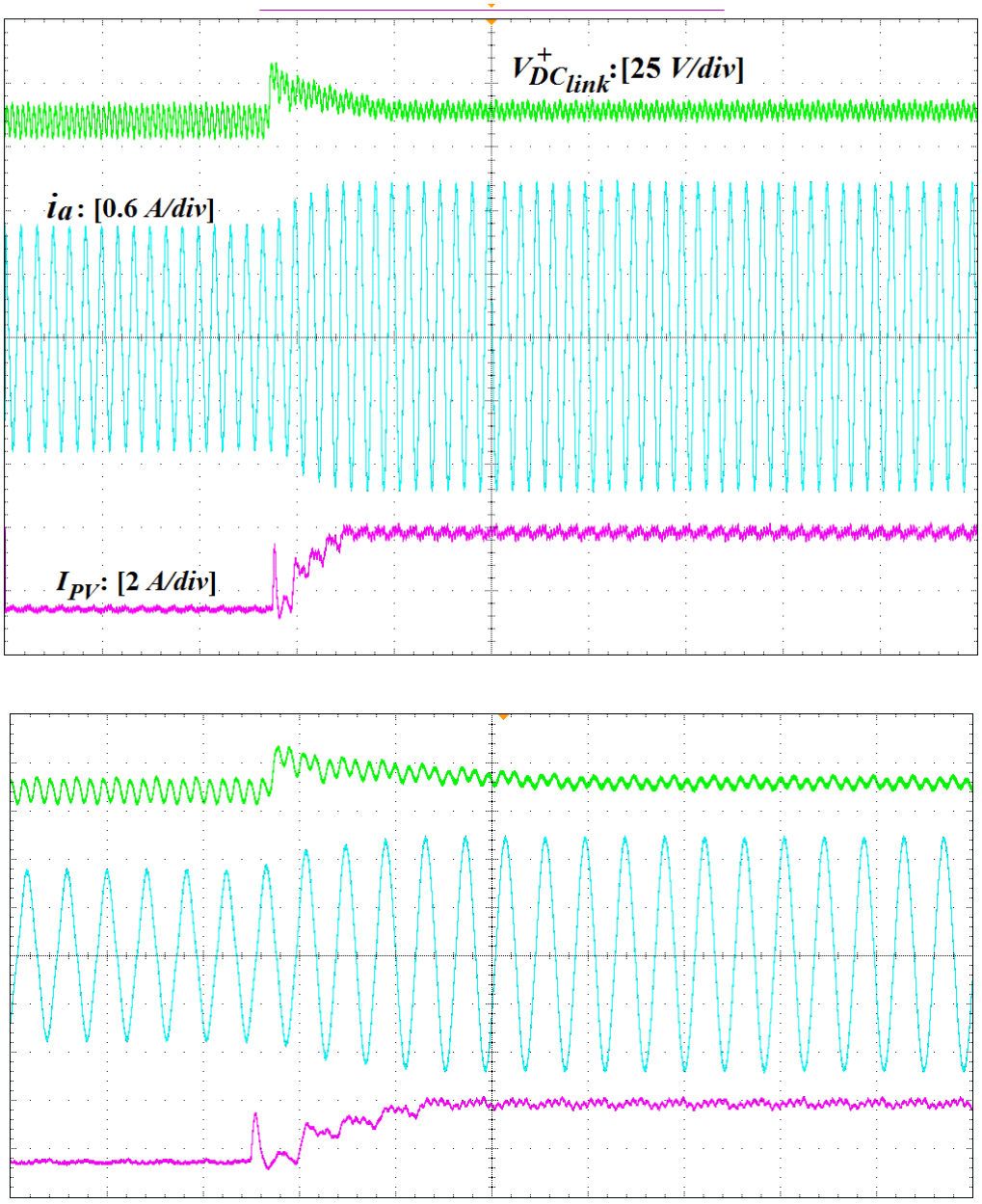


Figure 4-13: Dynamic response to the step change in the input power from 260 W to 375 W along with an expanded view.

Figure 14 shows the system dynamic response when the input power from the PV panel steps from 375 W to 260 W. In this case, the power imbalance is negative ($P_{in} < P_{o,avg}$) which causes the DC link voltage to drop. The controller responds by decreasing the current reference and therefore

reduces the inverter output power to maintain equilibrium. Once again, the system response is fast and smooth with recovery to steady state within three ac line cycles.

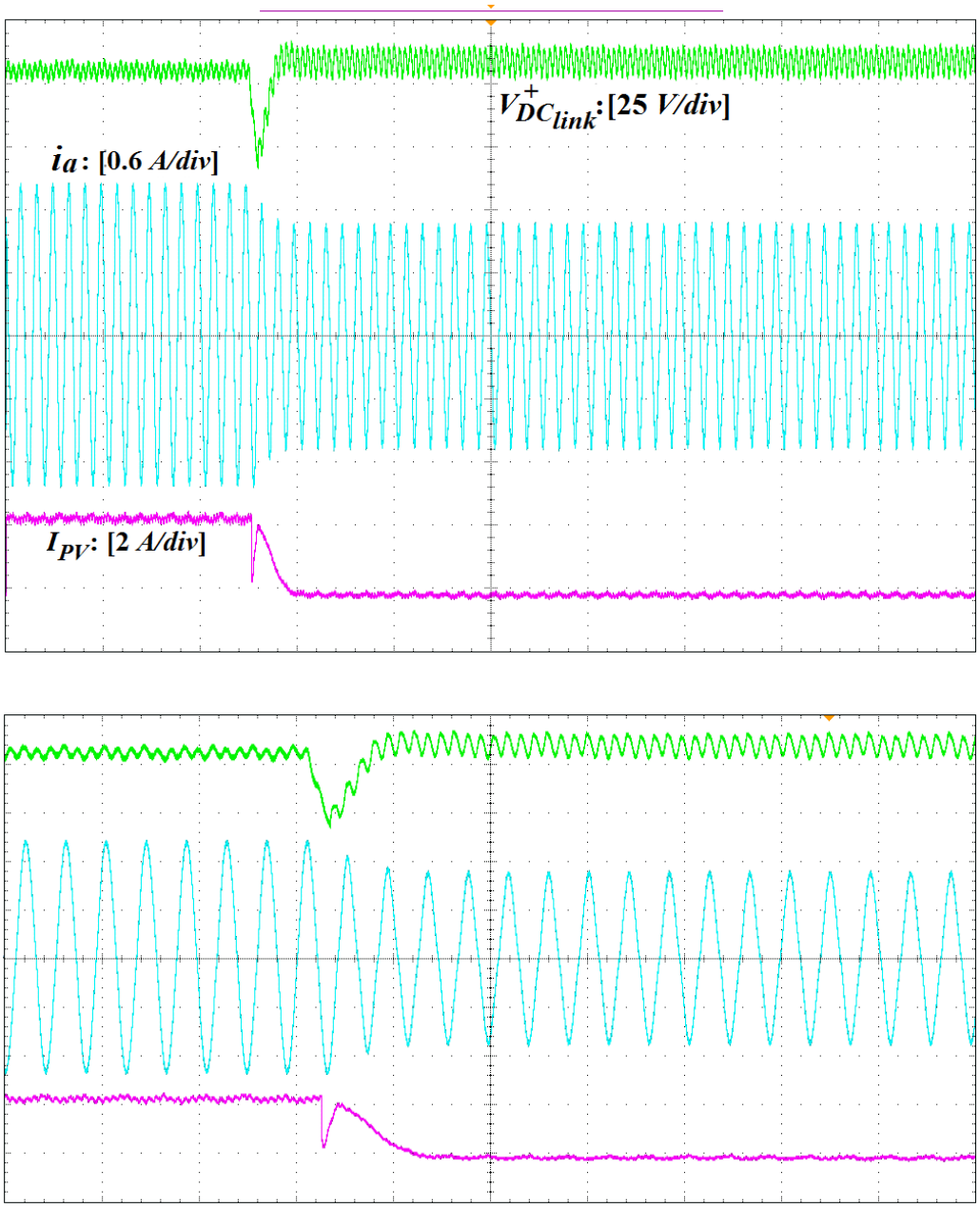


Figure 4-14: Dynamic response to the step change in the input power from 375 W to 260 W along with an expanded view.

The microinverter prototype was tested with greater power step changes than might be expected in a normal PV operating environment. Notice that in Figures 4-13 and 4-14, an input step change of 115 W did not cause the DC link voltage to drop below the output voltage. However, in the event of a transient large enough to cause the DC link voltage to drop close to the peak output voltage level, the inverter protection will be activated to shut down the PWM until the DC link voltage has recovered to its nominal value. The operating headroom included in DC link average voltage is designed to accommodate up to a 10% variation in grid voltage. Therefore, a phase voltage imbalance less than 10% will not affect the operation of the inverter. Note that a grid-tied PV inverter does not experience step load changes because the inverter output current is strictly a function of the input power from the PV source. PV inverters are special case and with typically low control loop bandwidth due to the fact that changes in output current can only be made at the line frequency in order to avoid unwanted harmonics injected into the grid. In addition, the PV source power slew rate is relatively low and does not require a high bandwidth control loop [75].

4.5 Summary

Replacing electrolytic capacitors with polypropylene film capacitors increases microinverters reliability and lifetime. Since film capacitors are more expensive than electrolytic capacitors, it is advantageous to minimize their size. This chapter selects the minimum acceptable DC link capacitor value in a three-phase half-bridge microinverter by intentionally increasing voltage ripple on the DC link. The relationship between the DC link voltage ripple and storage capacitance along with the DC link voltage normal operating range is taken into account to minimize the size of the storage capacitor. The voltage ripple present on the DC link film capacitor produces

negligible self heating due to its inherent low ESR compared to that of electrolytic capacitors. Note that the minimized value of DC link capacitor results in an approximately one-third size reduction which reduces the microinverter cost and improves power density.

As the DC link capacitor value is reduced, the voltage ripple will increase. The voltage ripple present on the DC link may introduce harmonic distortion in the inverter output current injected into the grid if it is not filtered by the inverter control loop. An advanced DC link voltage control is proposed in this chapter to tightly regulate the DC link average voltage without being adversely affected by the presence of relatively large voltage ripple. This controller is designed to accurately measure the DC link average voltage without the need for additional circuit components or digital filters while minimizing the inverter output current harmonic distortion. The experimental results on a 400-W three-phase half-bridge microinverter prototype validate both the steady state and transient performance of the control system while achieving only 1.84% of THD in the inverter output current. This chapter proposes a simple and accurate DC link voltage control method which demonstrates that low current THD can be achieved in spite of large values of DC link voltage ripple.

CHAPTER 5. DC LINK VOLTAGE CONTROL WITH PHASE SKIPPING

5.1 Introduction

This chapter investigates selection of the minimum DC link capacitor value for three-phase photovoltaic (PV) based microinverters using phase skipping control. This control method distributes power on individual phases depending on the available input power from the PV panel in order to maximize the output stage efficiency of a three-phase microinverter. Since the microinverter operates in single-phase, two-phase or three-phase mode, its DC link capacitor must be selected so that the DC link voltage ripple does not exceed the maximum allowable value. This chapter determines the minimum acceptable value of the DC link capacitor by allowing the maximum voltage ripple on the DC link. This allows for the use of film capacitors instead of electrolytic capacitors in order to improve the microinverter reliability. Unfortunately, higher DC link voltage ripple introduces harmonic distortion on the inverter output current waveform if it is not accounted for by the DC link voltage controller. This chapter proposes two advanced control functions to regulate the DC link voltage and implement dynamic phase skipping without using any additional circuit components. The DC link voltage controller is synchronized with the phase-locked loop (PLL) and samples the average value of DC link voltage without introducing unwanted harmonics into the voltage sense path. The phase skipping control block uses the calculated output power in order to determine how much power is apportioned to each phase so that the output stage is always operating at its maximum efficiency. Experimental results are obtained from a 300-W three-phase half-bridge microinverter prototype in order to verify operation with the calculated minimum DC link capacitor value. The proposed DC link voltage controller is implemented to

mitigate the effects of the large DC link voltage ripple. Additionally, a phase skipping management function is included in the controller to maximize the inverter stage efficiency at all power levels.

5.2 Phase Skipping Control

Depending on the amount of power available, advanced phase-skipping control distributes the power to individual phases in order to maximize the output stage efficiency of the three-phase micro-inverter. The micro-controller constantly monitors the available input power from the PV side MPPT controller [51].

In advanced phase-skipping control, there are three modes of operations: normal three-phase operation, one-phase skipped and two-phase skipped. When the input power from the PV source is above two-thirds of rated power, the controller enables normal three-phase operation. From one-third of rated power to two-thirds of rated power, the micro-inverter enters into one-phase skipped mode. If the power is below one-third of rated power, the micro-controller commands the micro-inverter to skip two phases. The three-phase micro-inverter operation modes with thresholds are shown in Figure 5-1.

During periods of low irradiance such as when the sun is low on the horizon or affected by overcast conditions, the available power is likely to be low. Therefore, the micro-inverter will be operating in two-phase skipped mode. Once the available power exceeds the rated power of a single phase, another phase is enabled and half of the available power is distributed to each of two phases until such time that the available power exceeds the capacity of the two phases, after which the third phase is enabled and one third of the available power is distributed to each phase.

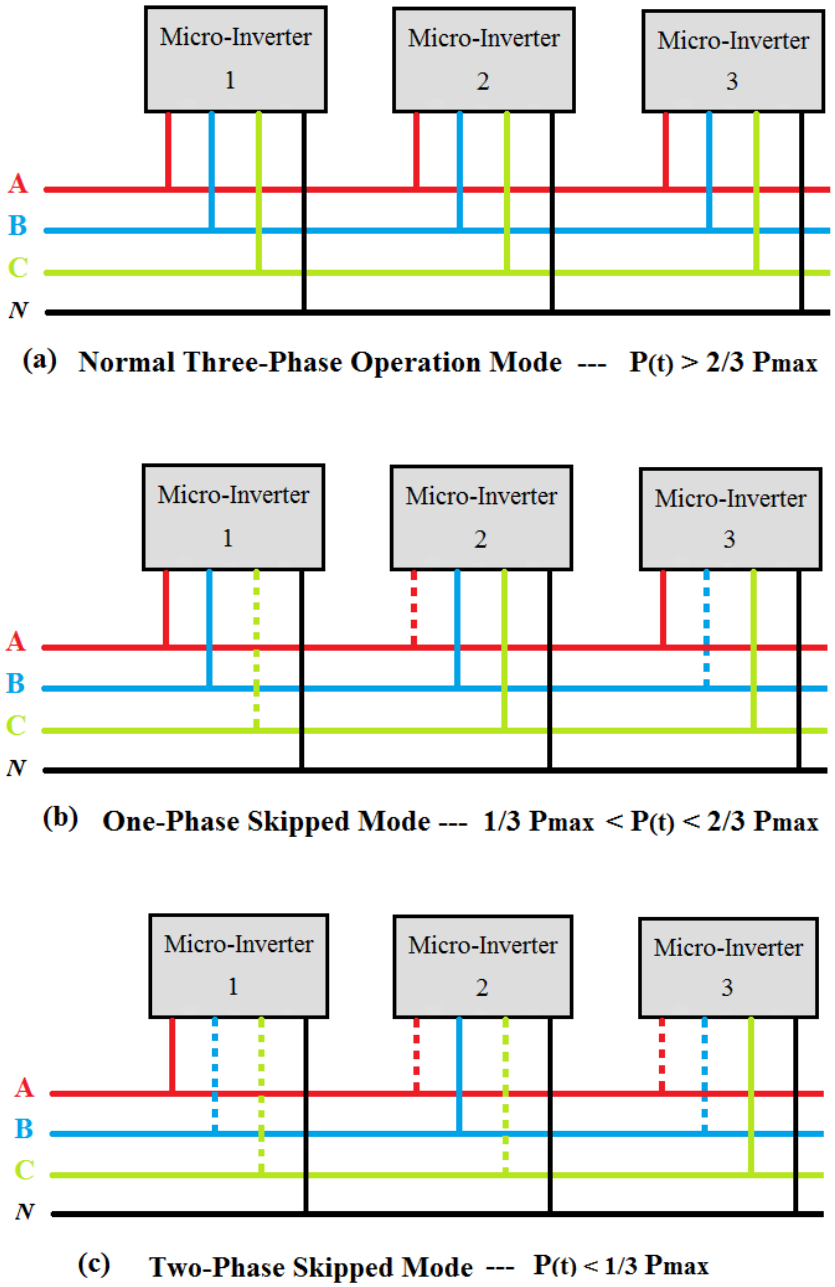


Figure 5-1: Three-phase micro-inverter operating modes.

In order to implement advanced phase-skipping control, a minimum of three micro-inverters is required so that a balanced three-phase system can be maintained.

5.3 Calculation of Minimum DC Link Capacitor Value with Phase Skipping

Figure 5-2 shows a three-phase half-bridge microinverter topology which uses a bipolar DC link ($V^{\pm}_{DClink}$) with identical capacitors. Each capacitor is charged by half of DC input power from the PV panel and similarly, half of the output power injected into the grid is drawn from each capacitor. Due to the symmetrical circuit, the analysis will be performed on only one of the capacitors. Notice that during positive half cycles, grid current is predominantly sourced from V^{+}_{DClink}, and during negative half cycles, grid current is predominantly drawn from V^{-}_{DClink}. Therefore,

$$P^{+}_{o,avg} = \frac{1}{T}\int_0^T \left(P^{+}_a(t) + P^{+}_b(t) + P^{+}_c(t)\right) dt = P^{+}_{in} = \frac{3}{2}\frac{V_m I_m}{2} \qquad (5\text{-}1)$$

where, V_m and I_m are the peak values of voltage and current for each phase, respectively, $P^{+}_{o,avg}$ is the inverter average output power sourced by C^{+}_{DClink} capacitor, P^{+}_{in} is the half of DC input power to charge C^{+}_{DClink} capacitor and $P^{+}_{a,b,c}(t)$ is the inverter instantaneous output power for each phase during positive half cycles and defined as

$$P^{+}_{a,b,c}(t) = \begin{cases} P_{a,b,c}(t), & positive\ half\ cycles \\ 0, & negative\ half\ cycles \end{cases} \qquad (5\text{-}2)$$

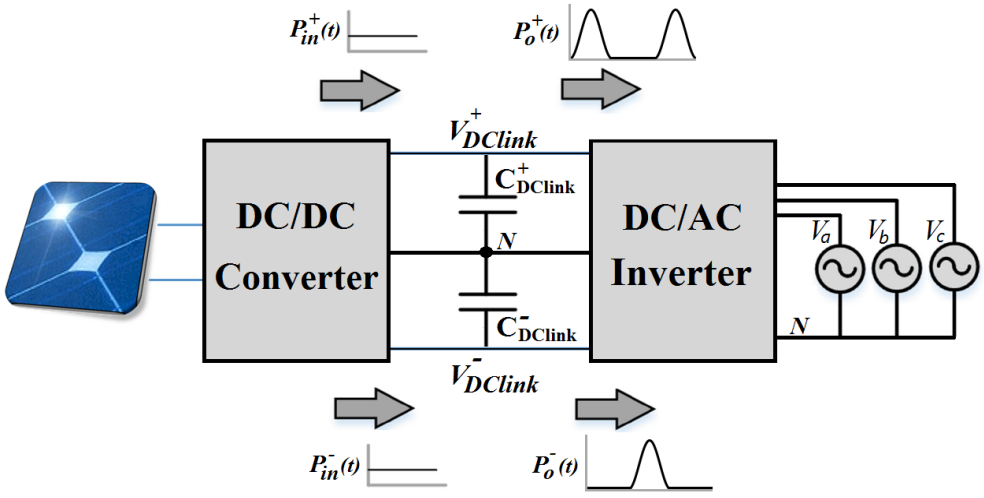


Figure 5-2: Three-phase half-bridge microinverter with a bipolar DC link.

Since the three-phase microinverter can operate in phase skipping mode where one or two phases may be skipped depending on the available input PV power, the relationship between the DC link voltage ripple and storage capacitor value is determined in single-phase and two-phase modes of operation.

5.3.1 Single-Phase Mode

Figure 5-3 shows the key waveforms of the microinverter when operating in single-phase mode. It can be seen that V^{+}_{DClink} is decreasing when $P^{+}_{a}(t) > P^{+}_{in}$ during the interval *(T/12,5T/12)*, and similarly V^{+}_{DClink} is increasing when $P^{+}_{a}(t) < P^{+}_{in}$ during intervals *(5T/12,T/2)*, *(T/2,T)* and *(T,13T/12)*. Therefore, the minimum and maximum values of V^{+}_{DClink} ($V^{+}_{DClink\_min}$ and $V^{+}_{DClink\_max}$) occur at 5T/12 and T/12, respectively.

Referring to Figure 5-3, the energy required to discharge C^{+}_{DClink} during the interval *(T/12,5T/12)* can be calculated as

$$\Delta E = \int_{\frac{T}{12}}^{5\frac{T}{12}} (P_o^+(t) - P_{in}^+)\, dt = \frac{V_m I_m}{2\omega}\left(\frac{\sqrt{3}}{2} + \frac{\pi}{3}\right) \quad (5\text{-}3)$$

where, $P^{+}_{o}(t)$ and P^{+}_{in} are $P^{+}_{a}(t)$ and $V_m I_m/4$, respectively, in this interval as shown in Figure 5-3. The stored energy in C^{+}_{DClink} can also be calculated as follows:

$$\Delta E = \frac{1}{2} C^{+}_{DC_{link}} \left(V^{+^2}_{DC_{link\_max}} - V^{+^2}_{DC_{link\_min}}\right) \quad (5\text{-}4)$$

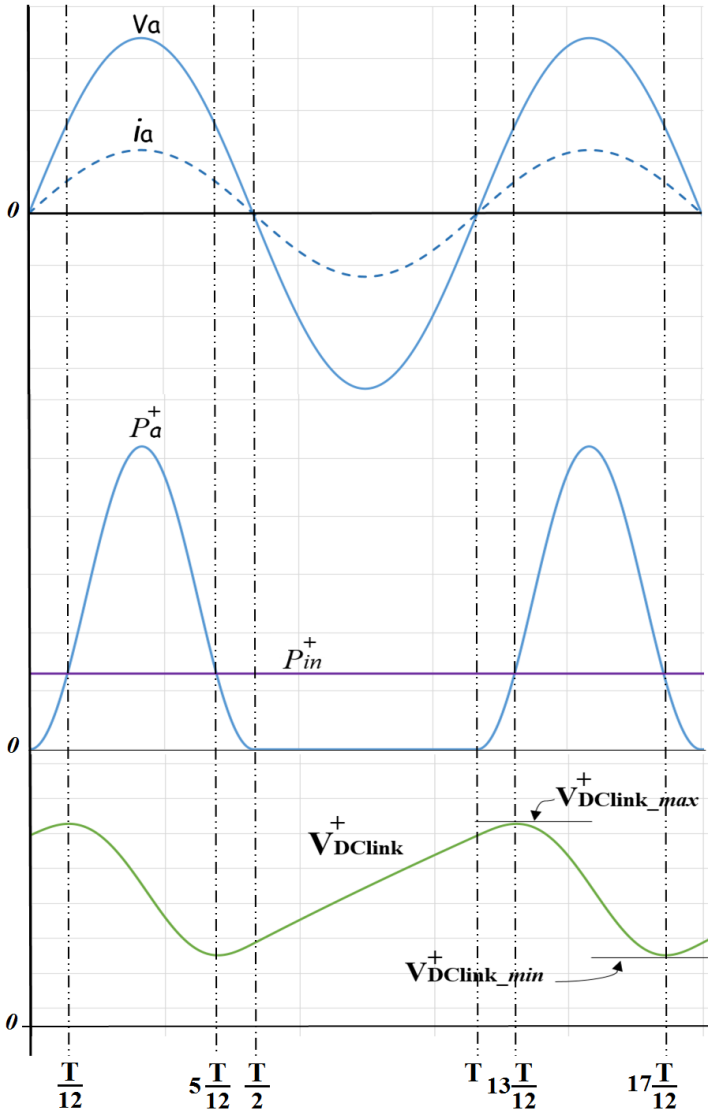


Figure 5-3: Key waveforms of the microinverter in single-phase mode.

Therefore, the relationship between the DC link voltage ripple and storage capacitor value is derived from (5-3) and (5-4) as

$$C_{DC_{link}}^{+} = \frac{V_m I_m}{2.\omega.\Delta V_{DC_{link}}^{+}.V_{DC_{link},avg}^{+}}\left(\frac{\sqrt{3}}{2}+\frac{\pi}{3}\right) \quad (5\text{-}5)$$

where, ΔV^{+}_{DClink} is the DC link peak-to-peak voltage ripple and $V^{+}_{DClink,avg}$ is the DC link average voltage defined as follows:

$$\begin{cases} \Delta V^{+}_{DC_{link}} = V^{+}_{DC_{link}\_max} - V^{+}_{DC_{link}\_min} \\ V^{+}_{DC_{link},avg} \approx \frac{V^{+}_{DC_{link}\_max} + V^{+}_{DC_{link}\_min}}{2} \\ \omega = \frac{2\pi}{T} \end{cases} \tag{5-6}$$

The DC link instantaneous voltage shown in Figure 5-3 can be derived in (5-7). The detailed derivation is given in the Appendix.

$V^{+}_{DC_{link}}(t) =$

$$\begin{cases} \sqrt{V^{+2}_{DC_{link}\_max} - \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\left(\omega t + \left(1 - \frac{\pi}{6}\right) - \sin(2\omega t)\right)} & , \quad \frac{T}{12} < t < 5\frac{T}{12} \\ \sqrt{V^{+2}_{DC_{link}\_min} + \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\left(-\omega t + \left(\frac{\sqrt{3}}{2} + \frac{5\pi}{6}\right) + \sin(2\omega t)\right)} & , \quad 5\frac{T}{12} < t < \frac{T}{2} \\ \sqrt{V^{+2}_{DC_{link}}\left(\frac{T}{2}\right) + \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}(\omega t - \pi)} & , \quad \frac{T}{2} < t < T \\ \sqrt{V^{+2}_{DC_{link}}(T) + \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}(-\omega t + 2\pi + \sin(2\omega t))} & , \quad T < t < 13\frac{T}{12} \end{cases} \tag{5-7}$$

5.3.2 Two-Phase Mode

Figure 5-4 shows the key waveforms of the microinverter when operating in two-phase mode. Referring to this figure, V^{+}_{DClink} is decreasing when $P^{+}_{a}(t)+P^{+}_{b}(t) > P^{+}_{in}$ during intervals *(T/8,T/3)*, *(T/3,T//2)* and *(T/2,17T/24)*, and similarly V^{+}_{DClink} is increasing when $P^{+}_{a}(t)+P^{+}_{b}(t) < P^{+}_{in}$ during intervals *(17T/24,5T/6)*, *(5T/6,T)* and *(T,9T/8)*. Therefore, the minimum and maximum values of V^{+}_{DClink} occur at 17T/24 and T/8, respectively.

The energy required to discharge C^{+}_{DClink} during the interval *(T/8,17T/24)* can be calculated as

$$\Delta E = \int_{\frac{T}{8}}^{17\frac{T}{24}} (P^{+}_{o}(t) - P^{+}_{in})\, dt = \frac{V_m I_m}{2\omega}\left(1 + \frac{\pi}{3}\right) \tag{5-8}$$

where, $P^{+}_{o}(t)$ and P^{+}_{in} are $P^{+}_{a}(t)+P^{+}_{b}(t)$ and $V_m I_m/2$, respectively. Therefore, the relationship

between the DC link voltage ripple and storage capacitor value is derived from (5-8) and (5-4) as

$$C^{+}_{DC_{link}} = \frac{V_m I_m}{2.\omega.\Delta V^{+}_{DC_{link}}.V^{+}_{DC_{link},avg}}\left(1+\frac{\pi}{3}\right) \tag{5-9}$$

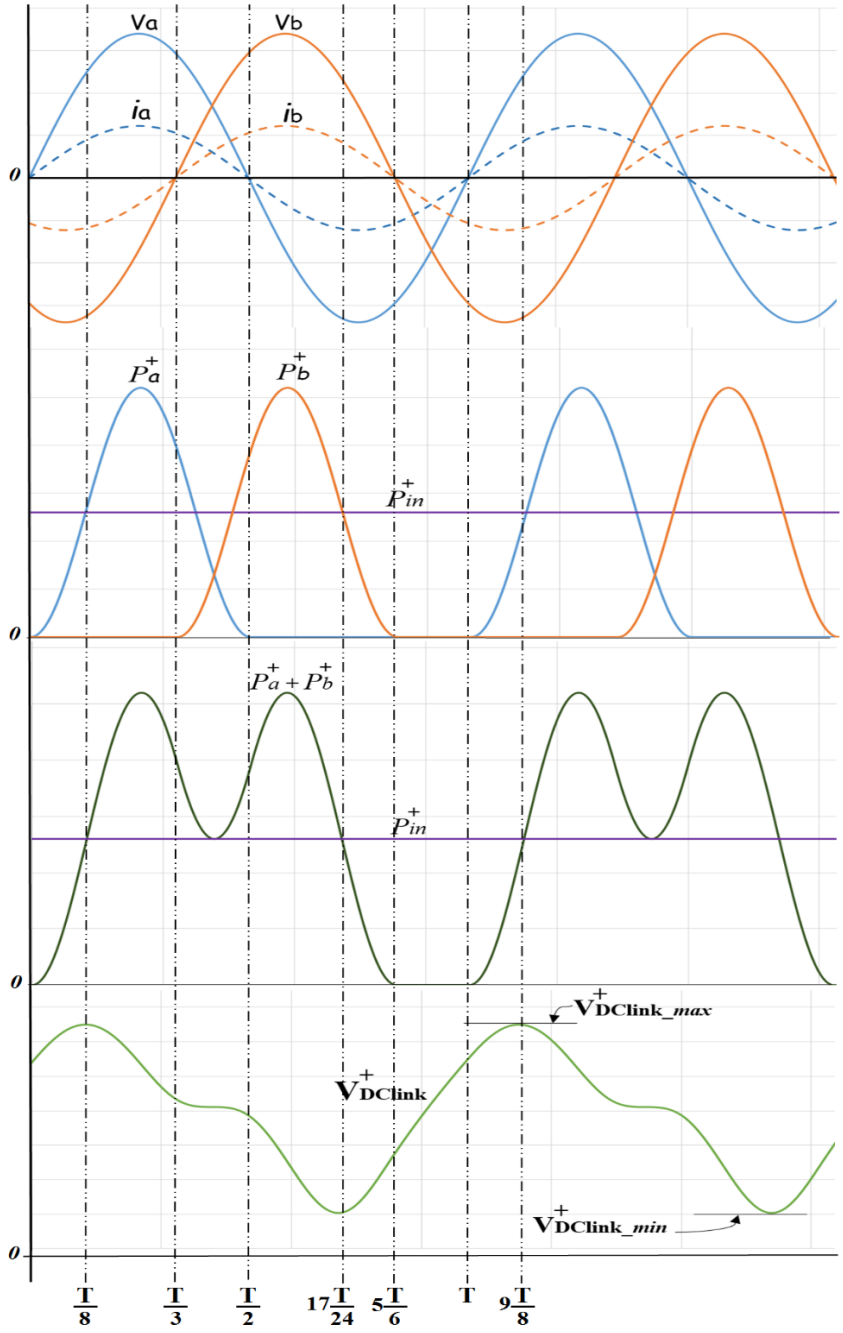


Figure 5-4: Key waveforms of the microinverter in two-phase mode.

The DC link instantaneous voltage shown in Figure 5-4 can be derived in (5-10).

$$V_{DC_{link}}^{+}(t) =$$

$$\begin{cases} \sqrt{V_{DC_{link\_}max}^{+2} - \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}(1-\sin(2\omega t))} & , \quad \frac{T}{8} < t < \frac{T}{3} \\ \sqrt{V_{DC_{link}}^{+2}\left(\frac{T}{3}\right) - \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}\left(2\omega t - \left(\frac{\sqrt{3}}{2}+\frac{4\pi}{3}\right) - \sin(2\omega t) - \sin\left(2\omega t - \frac{4\pi}{3}\right)\right)}, & \frac{T}{3} < t < \frac{T}{2} \\ \sqrt{V_{DC_{link}}^{+2}\left(\frac{T}{2}\right) + \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}\left(\sin\left(2\omega t - \frac{4\pi}{3}\right) - \frac{\sqrt{3}}{2}\right)} & , \quad \frac{T}{2} < t < 17\frac{T}{24} \\ \sqrt{V_{DC_{link\_}min}^{+2} + \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}\left(1+\sin\left(2\omega t - \frac{4\pi}{3}\right)\right)} & , \quad 17\frac{T}{24} < t < 5\frac{T}{6} \\ \sqrt{V_{DC_{link}}^{+2}\left(5\frac{T}{6}\right) + \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}\left(2\omega t - \frac{10\pi}{3}\right)} & , \quad 5\frac{T}{6} < t < T \\ \sqrt{V_{DC_{link}}^{+2}(T) + \frac{V_m I_m}{2\omega C_{DC_{link}}^{+}}\sin(2\omega t)} & , \quad T < t < 9\frac{T}{8} \end{cases} \quad (5\text{-}10)$$

From the preceding analysis, the DC link capacitor value can be reduced if the maximum allowable DC link voltage ripple is realized enabling smaller value film capacitors to be used instead of electrolytic capacitors. As can be seen from equations (5-5) and (5-9), two-phase mode produces the largest DC link peak-to-peak voltage ripple. Given the fact that two-phase mode has been established as the worst case operating mode, equation (5-9) along with the minimum and maximum DC link voltage operating limits will be used to determine the minimum acceptable value of the DC link capacitor.

Since the inverter stage normally operates as a buck converter, the DC link voltage must be greater than the peak grid voltage plus some operating headroom to allow for transients and variations in grid voltage, i.e.

$$V_{DC_{link}}^{+}(t) \geq V_m sin\left(\omega t - {}^{2\pi}/_{3}\right) + h \quad (5\text{-}11)$$

where, *h* is the operating headroom. From (5-10) and (5-11), $V^{+}_{DClink\_min}$ can be derived in (5-12).

From (5-12), a higher grid voltage and a larger C^{+}_{DClink} value produce a higher $V^{+}_{DClink\_min}$. Similarly, a smaller value of C^{+}_{DClink} will result in a higher DC link maximum voltage ($V^{+}_{DClink\_max}$). Therefore, the maximum allowable DC link voltage derived in (5-13) must be taken into account when evaluating voltage stress on the microinverter power devices.

$$V^{+}_{DC_{link\_}min} \geq \sqrt{\frac{V_m^2}{2} - \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}} - A\sin(2\omega t - \frac{4\pi}{3} + \alpha) + 2hV_m \sin(\omega t - \frac{2\pi}{3}) + h^2}$$

$$A = \sqrt{\left(\frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}\right)^2 + \left(\frac{V_m^2}{2}\right)^2}, \quad \alpha = tan^{-1}\frac{\frac{V_m^2}{2}}{\frac{V_m I_m}{2\omega C^{+}_{DC_{link}}}} \qquad (5\text{-}12)$$

$$V^{+}_{DC_{link\_}max} \geq \sqrt{\frac{V_m^2}{2} + \frac{V_m I_m}{2\omega C^{+}_{DC_{link}}} - A\sin(2\omega t + \alpha) + 2hV_m \sin(\omega t) + h^2} \qquad (5\text{-}13)$$

As stated previously, the relationship between the DC link voltage ripple and storage capacitor value along with the DC link normal operating voltage range is used to calculate the minimum acceptable value of the DC link capacitor. Therefore, equations (5-9), (5-12), (5-13) and the microinverter operating parameters are input in MATLAB to perform this calculation.

Figure 5 shows the bipolar DC link voltage and 120 V_{rms} grid voltage with different values of storage capacitance for the microinverter prototype when operating in two-phase mode. Referring to the figure, the DC link voltage ripple increases with smaller capacitor values. It should be noted that if the DC link average voltage is increased, the minimum value of C^{+}_{DClink} can be reduced. However, in order to minimize switching losses in the MOSFETs, the lowest possible value of DC link average voltage should be selected. The results calculated in MATLAB show that a 34 μF storage capacitor along with 219 V DC link average voltage is optimum for the microinverter

prototype. A commonly available polypropylene film capacitor greater than or equal to this calculated value will be selected for the prototype.

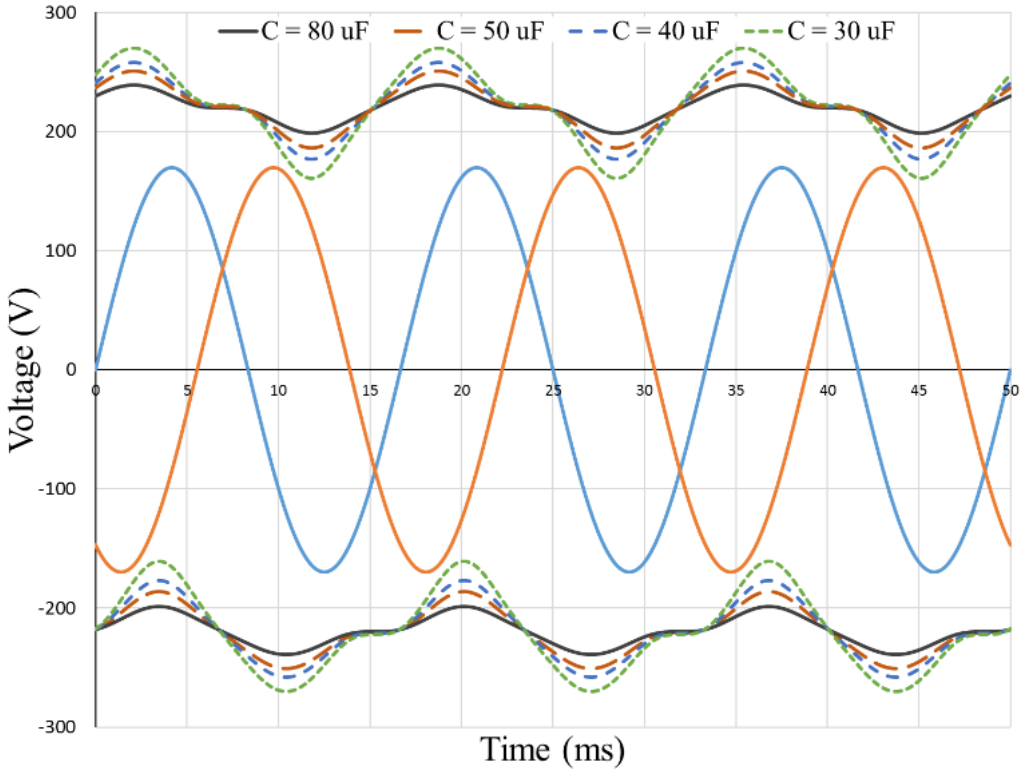


Figure 5-5: Bipolar DC link voltage ripple with different storage capacitance in two-phase mode.

Notice that if this relatively large voltage ripple present on the DC link is not attenuated by the inverter DC link voltage control loop, it will introduce harmonic distortion in the inverter output current injected into the grid. To address this, an advanced DC link voltage control will be presented in the next section.

5.4 Synchronous DC Link Voltage Control with Phase Skipping

This section introduces two proposed control functional blocks; synchronous DC link voltage control and dynamic phase skipping control. The DC link voltage controller tightly regulates the

DC link voltage by precisely measuring the average value of DC link voltage without introducing harmonics into the voltage sense path. This control system is able to produce minimum distortion in the inverter output current without being adversely affected by the presence of relatively large voltage ripple on the DC link. The phase skipping control block uses the calculated output power in order to determine how much power is apportioned to each phase so that the output stage is always operating at its maximum efficiency.

Figure 5-6 shows a typical DC link voltage control system. The controller samples the DC link voltage and compares it with the desired reference value. The error signal is then used by the control loop compensator to determine the inverter output peak current. The controller uses a PLL to generate a sinusoidal output current waveform which is synchronized to the grid voltage. The control loop regulates the DC link voltage by adjusting the inverter output peak current. When the input power from the PV panel is greater than the average output power, the DC link voltage increases. Similarly, When the input PV power is less than the average output power injected into the grid, the DC link voltage decreases. In an effort to balance the input PV power with the average output power, the control loop compensator increases or decreases the inverter output peak current as required.

Since typical controllers sample the DC link voltage at many kilohertz, voltage ripple present on the DC link is included in the sampling causing the error signal to have a harmonic content. If the harmonics in the error signal are not filtered, distortion will be introduced in the inverter output current injected into the grid. An analog low-pass filter placed in the DC link voltage sense path will reduce the loop bandwidth resulting in poor transient response. Although various digital low-

pass filters have also been proposed as a means of reducing harmonic content in the error signal, they are unable to eliminate all of the harmonic content.

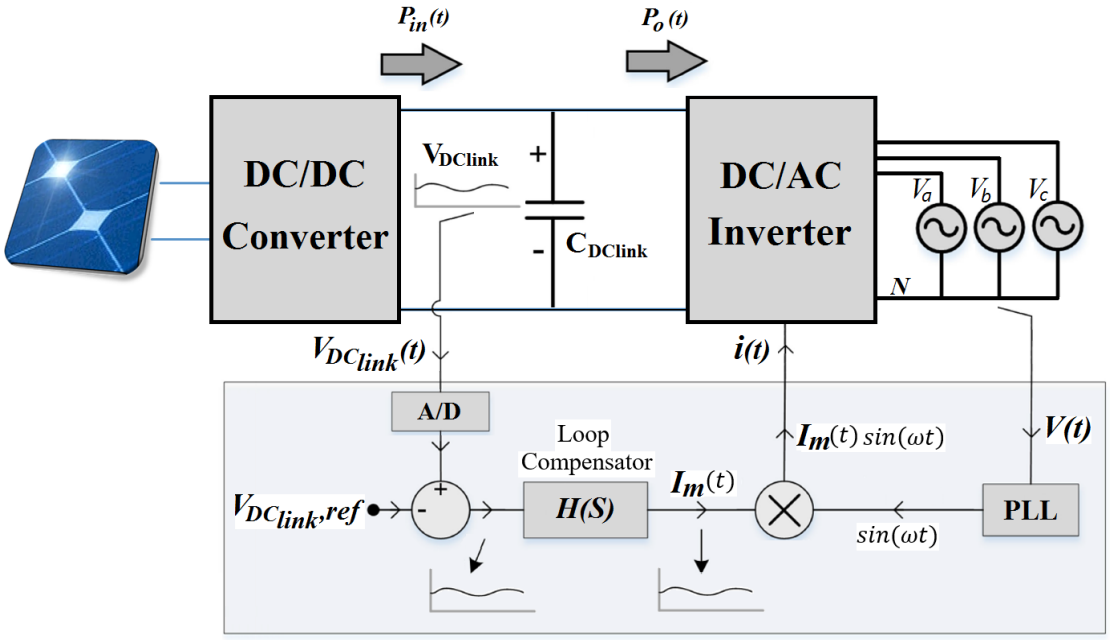


Figure 5-6: Typical DC link voltage control system.

By sampling the DC link voltage at specific predetermined points, the DC link average voltage can be accurately measured without introducing harmonic distortion. Since a highly accurate PLL is used in most inverters in order to synchronize with the grid voltage, it can be used to control the sample timing of the A/Ds that measure the DC link voltage. The voltage ripple present on the DC link is in phase with the grid voltage as shown in Figure 5-5. This fact can be used to sample the DC link voltage where it intersects the DC link average voltage value. By sampling at this time, the A/Ds will be measuring the DC link average voltage without the distortion present in other DC link voltage regulators.

Figure 5-7 shows the proposed PLL-synchronized DC link voltage control system with a phase skipping control function. It can be seen from this figure that the proposed DC link voltage controller uses existing control functional blocks along with PLL-synchronized A/D sampling thereby eliminating the requirement for additional analog or digital filters in the voltage sense path. Figure 5-8 shows the proposed PLL-synchronized DC link voltage sampling time. Since the A/Ds are now sampling the DC link average voltage, the loop compensator error signal is a dc value resulting in a peak current reference that is free of unwanted harmonics. This peak current reference is used to generate a pure sine wave input to the pulse-width modulation (PWM) block. Note that the inverter current is adjusted only every line cycle in order to avoid unwanted harmonics in the output current waveform. This simple and accurate synchronous sampling method measures the exact average DC link voltage despite the presence of large voltage ripple especially when operating in phase skipping mode. The proposed method makes it possible to design the DC link with the minimum acceptable capacitor value. This facilitates the use of low value film capacitors which reduces the design cost and improves microinverter reliability and power density [76], [77].

The phase skipping control block uses the DC link voltage control loop compensator output multiplied by the number of phases to calculate the inverter stage output power. The output power is then used by the phase skipping management function to determine the number of phases to be operated. The phase skipping management function operates all three phases when the output power is greater than two-thirds of the inverter stage rated power. When the output power is between one-third and two-thirds of rated power, two-phase operation is selected. Similarly, the

inverter operates in single-phase mode when the output power is less than or equal to one-third of rated power.

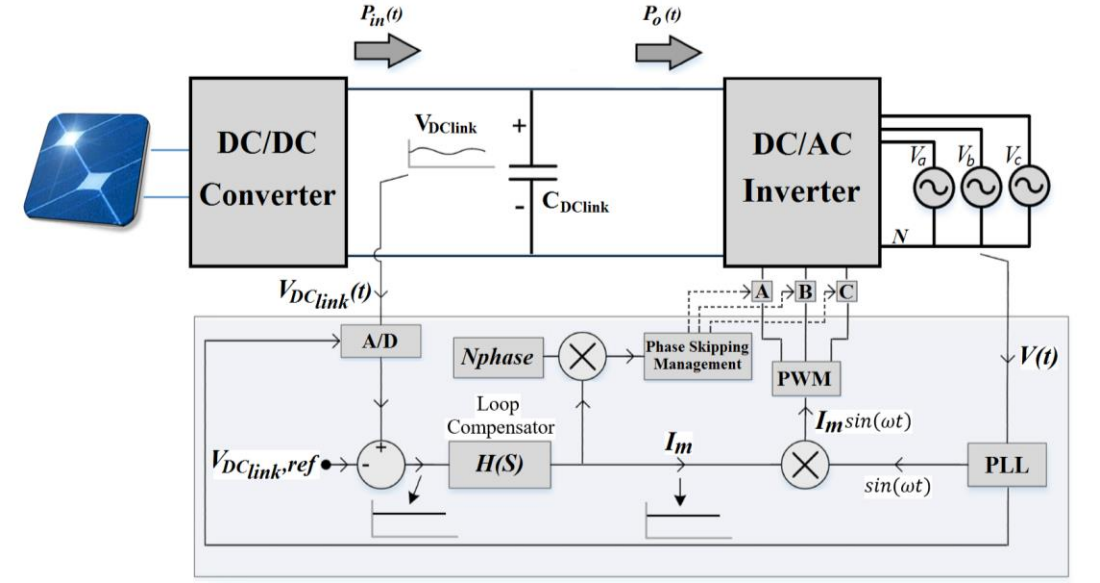


Figure 5-7: Proposed PLL-synchronized DC link voltage control system with phase skipping control.

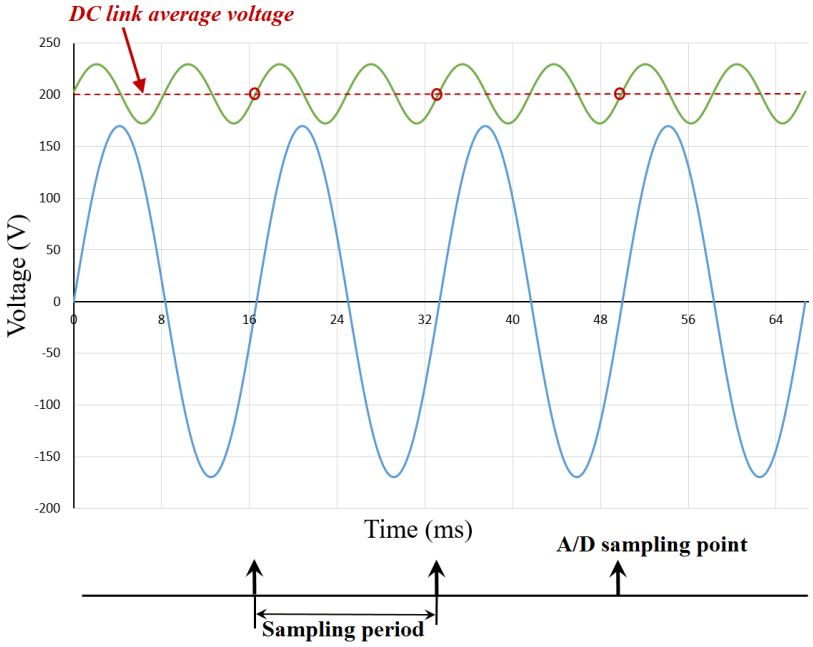


Figure 5-8: Proposed PLL-synchronized DC link voltage sampling time in the single-phase mode.

The DC link voltage control loop average model is shown in Figure 5-9. The average output power is determined by the inverter output peak current reference generated by the control loop compensator. The DC link capacitor current is defined by the difference between the input PV power and average output power divided by the DC link average voltage. The DC link instantaneous voltage is equal to the integral of the DC link capacitor current divided by the DC link capacitance. The DC link average voltage is then measured by a PLL-synchronized A/D and compared with the DC link reference voltage. The resulting error voltage is used by the control loop compensator to adjust the inverter output peak current. Notice that the control loop compensator uses a PI controller.

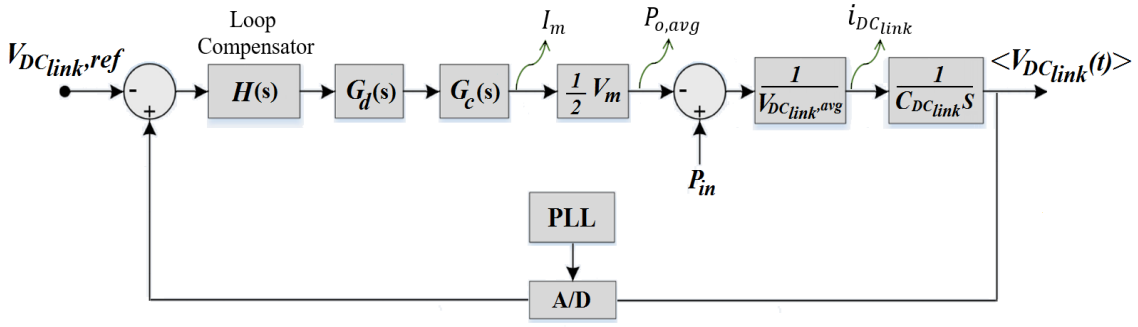


Figure 5-9: PLL-synchronized DC link voltage control dynamic model.

The digital control loop contains computation delay, PWM delay and the sampler which are included in $G_d(s)$, respectively, as follows:

$$G_d(s) = e^{-sT_d} \cdot \frac{1-e^{-sT_s}}{s} \cdot \frac{1}{T_s} \qquad (5\text{-}14)$$

where, T_d is the period of time between the sampling of the DC link voltage and the update of the current reference, and T_s is the sampling period. Since the current regulator operates at hundreds of kilohertz and the DC link voltage controller operates at 60 Hz, $G_c(s)$ is assumed to be 1 in the control loop.

In order to verify the control loop's transient response, a ramp change in input power is analyzed using the input-to-output power transfer function expressed as

$$T(s) = \frac{V_m}{2C_{DC_{link}} V_{DC_{link}.avg}.T_s} \cdot \frac{(k_p s + k_i)(1 - e^{-sT_s})e^{-sT_d}}{s^3} \qquad (5\text{-}15)$$

Input PV power changes are generally in the form of an ascending or descending ramp with 10% to 80% of rated power in three seconds considered to be a fast ramp rate of PV insolation [75]. Figure 5-10 shows the response of the closed-loop input-to-output transfer function to a 100 W per second ramp change in input PV power which is used to validate the proposed control system performance. Note that the 100 W per second ramp used is much greater than the fast ramp described in [75]. Referring to the figure, the controller response is fast and the inverter output power is able to track the input PV power within four ac line cycles. Notice that k_p and k_i of the compensated loop gain *T(s)* are 0.005 and 0.116, respectively. The cutoff frequency f_c is set at 10 Hz with a phase margin of 38^{O}.

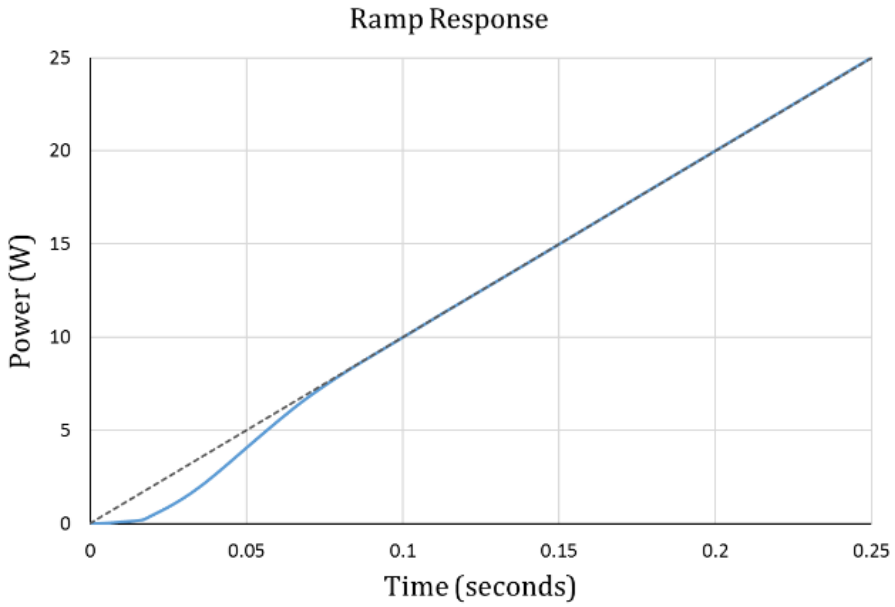


Figure 5-10: Proposed controller response to a ramp change in input PV power.

5.5 Experimental Results

Figure 5-11 shows the two-stage 300-W three-phase microinverter prototype topology. The input PV voltage of 45 V is boosted to the DC link voltage of +210 VDC and -210 VDC by means of a full-bridge LLC resonant step-up converter with a secondary that is configured as a voltage doubler. The DC link storage capacitor consists of two 34 μF, 300 V polypropylene film capacitors as calculated in section II. The inverter stage is a three-phase half-bridge topology with a LCL output filter which is then connected to a 120 V_{rms}, 60 Hz, three-phase output voltage. The microcontroller used to control the LLC resonant step-up converter is a STM32F103C8T7. The inverter stage is controlled by a DSPIC33FJ16GS504. The inverter output stage operates in zero voltage switching (ZVS) boundary conduction mode (BCM) using peak current control with an operating frequency range of 20 kHz to 180 kHz. The DC/DC resonant converter stage includes a MPPT function that senses the input PV voltage and current to ensure that maximum power is supplied from the PV source. The two proposed control functional blocks are implemented in the inverter stage microcontroller to regulate the DC link voltage and determine the number of phases to be operated.

Figure 5-12 shows the microinverter's DC link voltage and output voltage with 34 μF DC link capacitors operating in three-phase, two-phase and single-phase modes. The two-phase mode produces the highest peak-to-peak voltage ripple of 87 V on the DC link with average voltage of 219 V. This figure depicts the DC link voltage ripple in different modes of operation to validate the theoretical analysis in section 5.3.

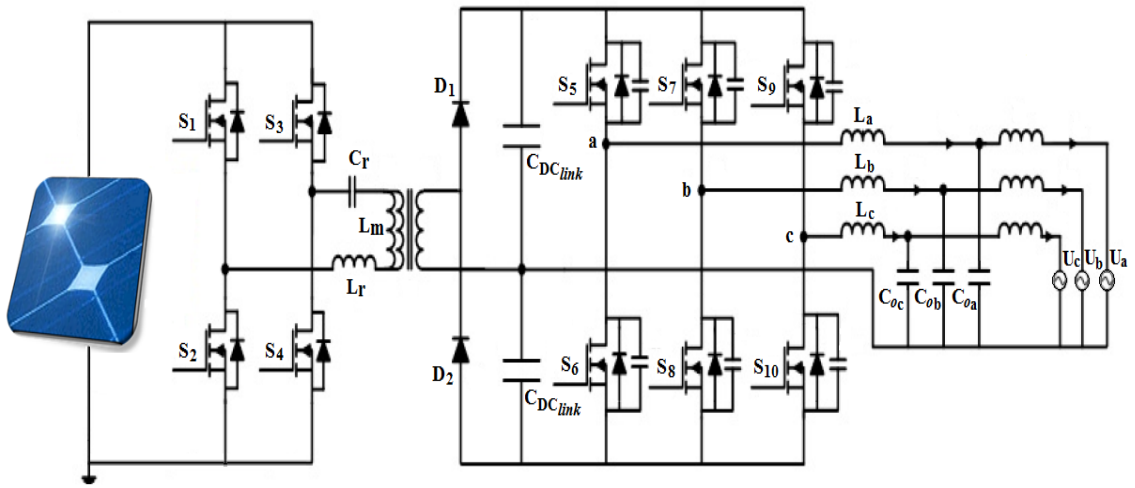
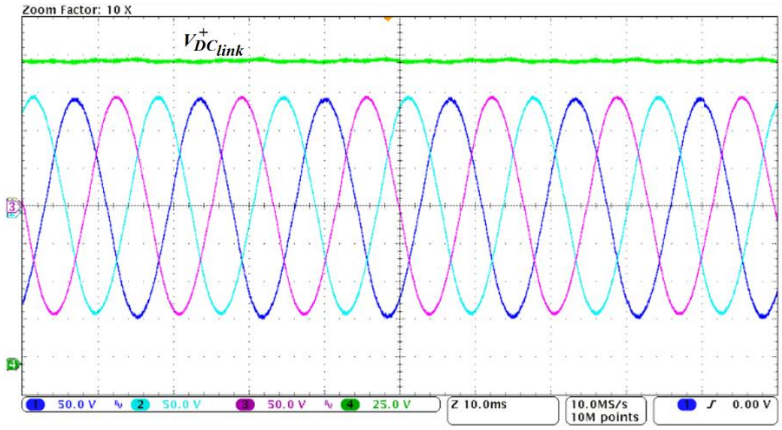
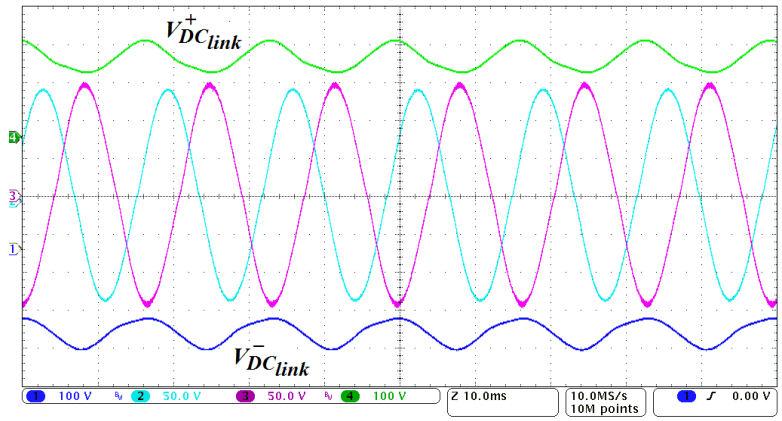


Figure 5-11: Two-stage three-phase microinverter prototype topology.

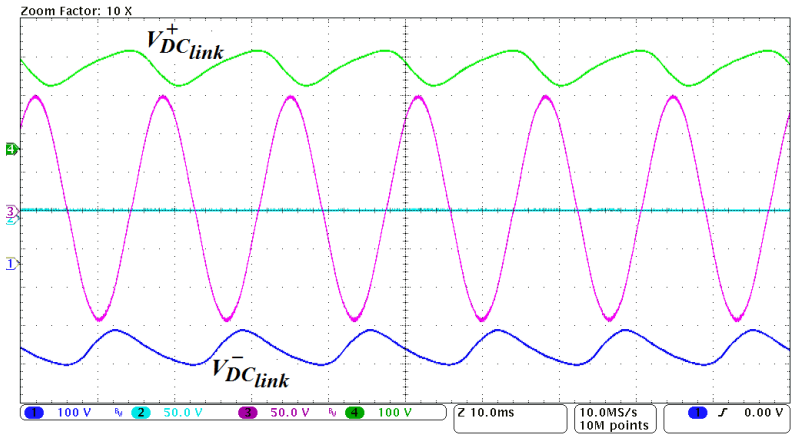
Figure 5-13 depicts the performance of the proposed DC link voltage control with phase skipping operation. Figure 5-13(a) shows the inverter output current and DC link voltage with an input PV power step from 180 W (two-phase mode) to 255 W (three-phase mode). Referring to this figure, once the third phase is activated, the DC link voltage decreases until the DC link voltage controller can respond by reducing the inverter output current thereby returning the DC link average voltage to its nominal value. Figure 5-13(b) shows the input PV power step change from 75 W (single-phase mode) to 140 W (two-phase mode). Referring to figure 5-13, the proposed DC link voltage control is able to tightly regulate the inverter output current regardless of high peak-to-peak voltage ripple on the DC link. The transition is smooth and without any transients or distortion on the inverter output current. Note that the controller response is fast and smooth with recovery to steady state in less than four ac line cycles while achieving only 1.6% THD in the inverter output current in all three operating modes. This is a significant improvement over the 3.8% THD measured on a high-frequency DC link voltage controller with identical loop bandwidth using the same PV inverter prototype.



(a)

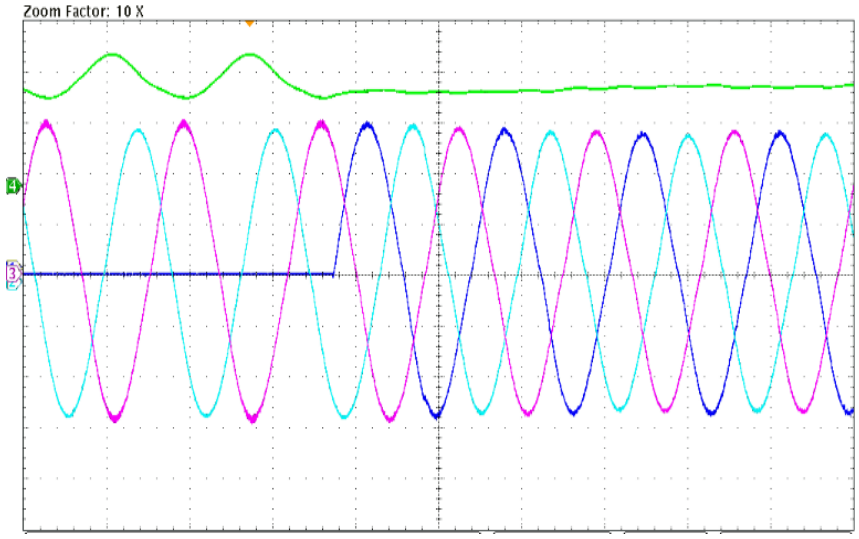


(b)

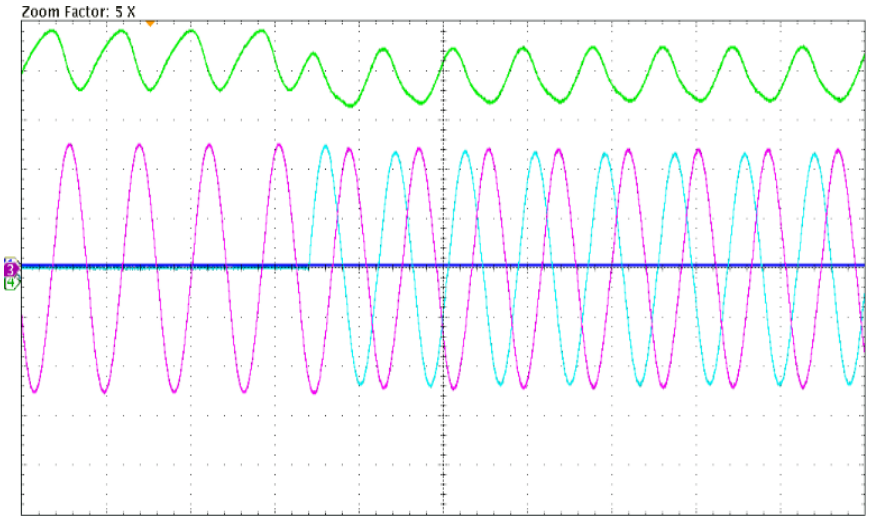


(c)

Figure 5-12: Microinverter DC link voltage and output voltage in (a) three-phase mode, (b) two-phase mode, and (c) single-phase mode.



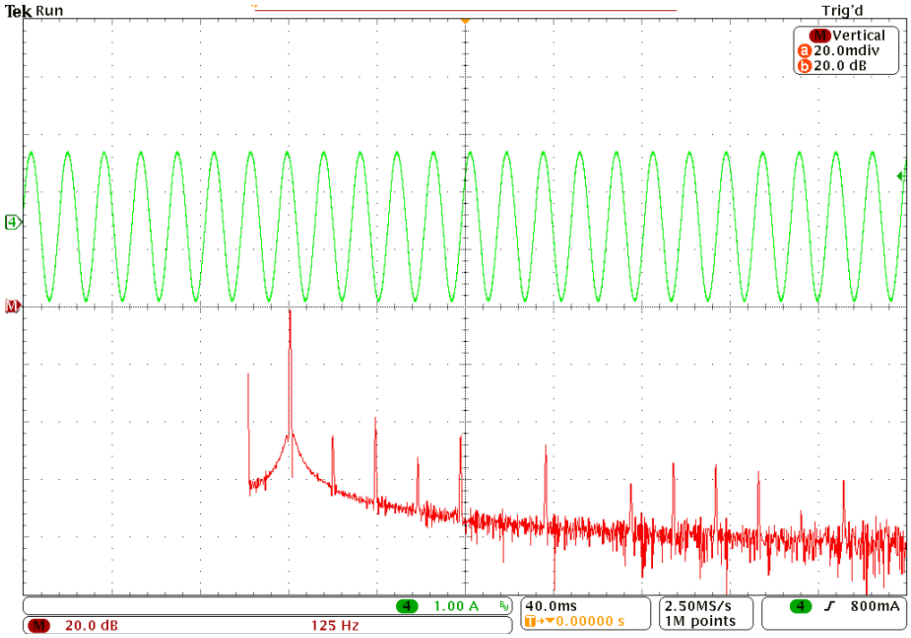
(a)



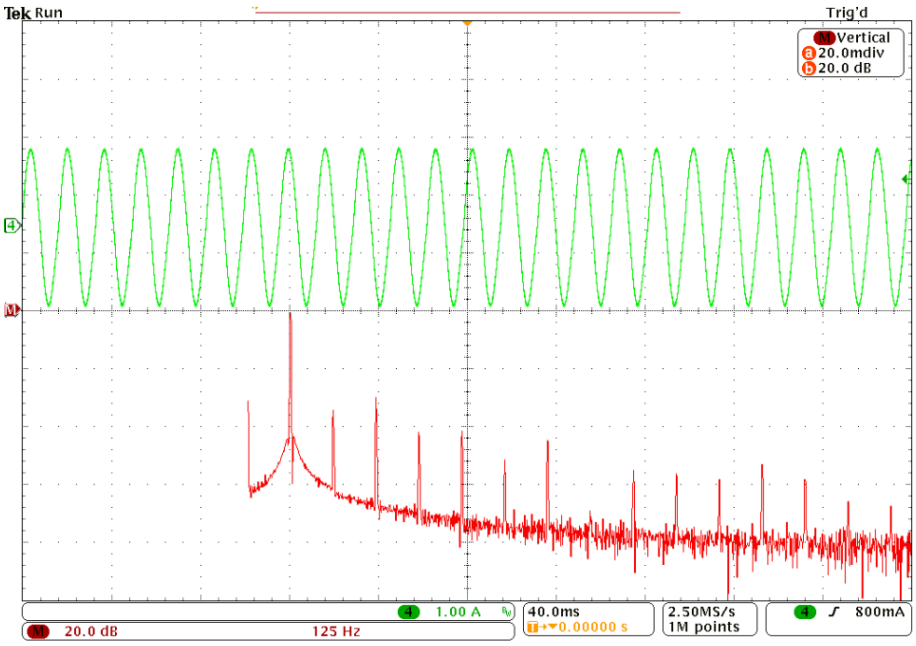
(b)

Figure 5-13: Dynamic response to the step change in the input power.

Notice that THD was measured with a Yokogawa PZ4000 power analyzer. Figure 5-14 shows the inverter output current with its harmonic spectrum using the proposed DC link voltage control method and a high-frequency DC link voltage control. Note that the inverter is operating in two-phase mode with 87 V peak-to-peak ripple on the DC link.



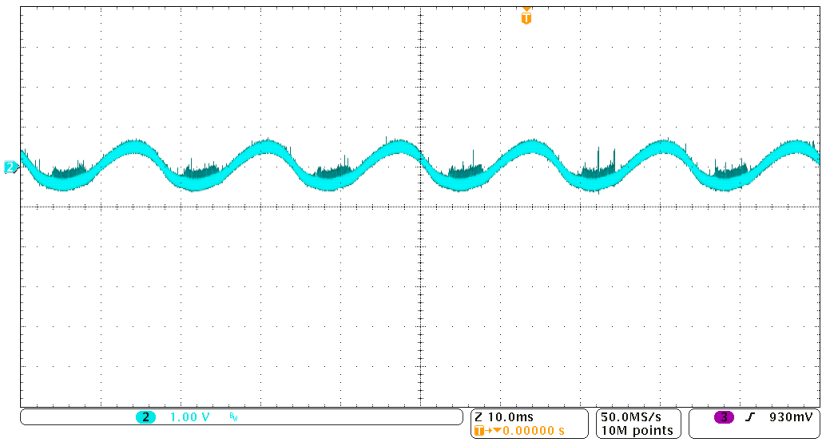
(a)



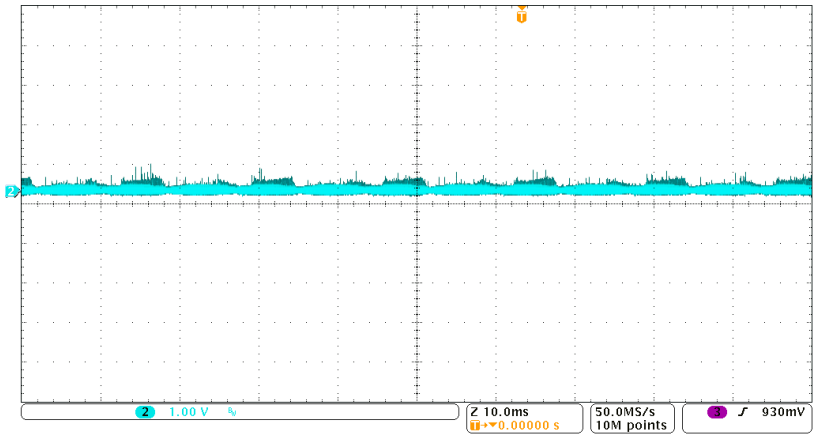
(b)

Figure 5-14: Inverter output current and its harmonic spectrum with, (a) the proposed DC link voltage control, (b) a high-frequency DC link voltage control.

Figure 5-15(a) shows the measured control error signal using the digital-to-analog converter (DAC) on the inverter dsPIC with a high-frequency DC link voltage control. This harmonic content on the control error signal introduces harmonic distortion on the inverter output current (THD=3.8%). Similarly, the control error signal with the proposed control method is measured and shown in Figure 5-15(b). It can be seen that this error signal is now a dc value which significantly reduces harmonic distortion on the inverter output current (THD=1.6%). Note that the inverter is operating in two-phase mode with 87 V peak-to-peak voltage ripple on the DC link.



(a)



(b)

Figure 5-15: Control error signal with, (a) a high-frequency DC link voltage control (THD=3.8%), (b) the proposed DC link voltage control (THD=1.6%).

When the input PV power changes, the DC link voltage controller adjusts the inverter output current to maintain the DC link average voltage at its reference value. After ten cycles of DC link voltage steady state operation, the phase skipping controller is activated to determine the number of phases to be operated based on the new inverter output power calculation. Figure 5-16 shows the transition from three-phase operation at 220 W to two-phase operation at 150 W. Although the peak-to-peak voltage ripple increases dramatically, the DC link voltage controller returns the DC link average voltage to its reference value. In order to avoid the introduction of unwanted harmonics, the phase skipping controller is enabled only at zero crossings. This figure shows the performance of both the DC link voltage control and phase skipping management in one capture. The first step change is the DC link voltage controller response to the PV power dropping from 220 W to 150 W which results in reduced output current within two line cycles. Once steady state has been reached, the phase skipping management control responds to the reduced PV power by changing from three-phase operation to two-phase operation at zero crossing. This is the second step change showing in the figure. Since one phase is disabled, power is distributed among two phases. Therefore, the DC link voltage control has to regulate the inverter output current with the presence of high peak-to-peak voltage ripple. This accomplishes within three line cycles.

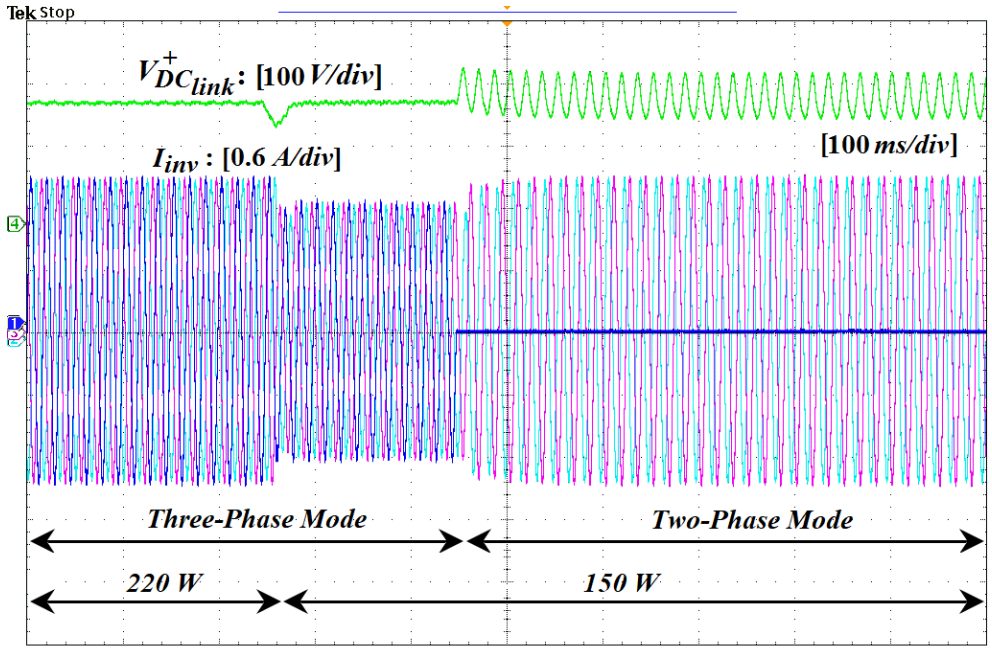


Figure 5-16: Controller performance when PV power changes from 220 W to 150 W.

5.6 Summary

This chapter determines the minimum acceptable value of the DC link capacitor by allowing the maximum voltage ripple on the DC link in a three-phase half-bridge microinverter with phase skipping control where one or two phases may be skipped. However, higher DC link voltage ripple introduces harmonic distortion on the inverter output current waveform if it is not attenuated by the DC link voltage controller. This chapter proposes a robust and accurate DC link voltage controller that tightly regulates the DC link average voltage even during transients while minimizing the inverter output current harmonics. The proposed controller is able to accurately measure the average DC link voltage regardless of the presence of relatively large voltage ripple without the need for additional circuit components or digital filters. The analysis presented in this chapter is also applicable to single-phase two-stage inverter topologies. In addition, the phase

skipping control is implemented as a part of the DC link voltage controller to provide real time optimization of the inverter stage efficiency at all power levels. Experimental results demonstrating both the transient and steady state performance of the proposed DC link voltage controller and phase skipping control function were obtained from a 300-W three-phase half-bridge microinverter prototype. Inverter output current THD of 1.6% was achieved over the entire operating range of the inverter even though the DC link peak-to-peak voltage ripple reached as high as 87 V.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusion

Among clean energy sources, solar energy has gained considerable attention in recent years. In the field of solar energy, PV microinverter architecture is the fastest growing technology due to its advantages such as enhanced energy harvesting, high reliability, and simple installation. Microinverters can be directly mounted on the back of the PV panels with power level ranging from 200 W to 400 W. Emerging trend in power electronics is to increase power density and efficiency of the microinverters while reducing cost. Several innovative control techniques have been proposed in this dissertation to increase efficiency and power density while reducing cost.

Dynamic dead time optimization was proposed to minimize MOSFET's body diode conduction time which improves the microinverter efficiency and THD. In chapter three, a dual-zone modulation technique was proposed to further improve efficiency. Compared to the other boundary conduction mode (BCM) modulation methods, this control technique provides one more soft-switching transition and lower inductor peak current.

Replacing electrolytic capacitors with polypropylene film capacitors increases microinverters reliability and lifetime. Since film capacitors are more expensive than electrolytic capacitors, it is advantageous to minimize their size. Chapter four investigates the minimum acceptable DC link capacitor value in a three-phase half-bridge microinverter by intentionally increasing voltage ripple on the DC link. The minimized value of DC link capacitor results in an approximately one-third size reduction which reduces the microinverter cost and improves power density.

Chapter four also proposes an advanced DC link voltage control to tightly regulate the DC link average voltage without being adversely affected by the presence of relatively large voltage ripple. The DC link average voltage is measured accurately without the need for additional circuit components or digital filters while minimizing the inverter output current harmonic distortion.

Chapter five calculates the minimum acceptable value of the DC link capacitor by allowing the maximum voltage ripple on the DC link in a three-phase half-bridge microinverter with phase skipping control where one or two phases may be skipped. This chapter proposes two advanced control functions to regulate the DC link voltage and implement dynamic phase skipping without using any additional circuit components. The DC link voltage controller is synchronized with the phase-locked loop (PLL) and samples the average value of DC link voltage without introducing unwanted harmonics into the voltage sense path. The phase skipping control block uses the calculated output power in order to determine how much power is apportioned to each phase so that the output stage is always operating at its maximum efficiency.

6.2 Future Works

For future work, dynamic dead time optimization technique could be applied to other application areas such as power supplies and motor controllers. In addition, advanced phase skipping control implementation requires the development of a system-level master controller in order to maintain a balanced three-phase system.

The synchronous DC link voltage control proposed in this dissertation is constrained to grid-tied application with unity power factor controlled by the inverter which comprises the vast majority of microinverter installations. A nonlinear load may affect the performance of the proposed

method in microgrid or other standalone applications. Since the proposed controller is PLL based, it requires presence of the grid for proper operation. Therefore, only grid-tied operation was considered. In future work, more research can be conducted to improve the proposed control method to be applicable to standalone applications.

REFERENCES

[1] F. Blaabjerg, Z. Chen, S.B. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Systems," IEEE Transactions on Power Electronics, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.

[2] "Technology Roadmap - Solar Photovoltaic Energy". [Online]. Available: www.iea.org

[3] H.W. Huang, C. Y. Hsieh, K. H. Chen, and S. Y. Kuo, "Load dependent dead-times controller based on minimized duty cycle technique for DC-DC buck converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2037–2041.

[4] P. T. Krein and R. M. Bass, "Autonomous control technique for high-performance switches," *IEEE Trans. Ind. Electron.*, vol. 39, no. 3, pp. 215–222, Jun. 1992.

[5] W. L. W. Lau and S. Sanders, "An integrated controller for a high frequency buck converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 246–254.

[6] B. Acker, C. Sullivan, and S. Sanders, "Synchronous rectification with adaptive timing control," in *Proc. IEEE Power Electron. Spec. Conf.*, 1995, pp. 88–95.

[7] A. Zhao, A. A. Fomani, and W. T. Ng, "One-step digital dead-time correction for DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 132–137.

[8] L. Mei, D. Williams, and W. Eberle, "A Synchronous Buck Converter Using a New Predictive Analog Dead-Time Control Circuit to Improve Efficiency," Canadian Journal of Electrical and Computer Engineering, vol. 36, no. 4, pp. 181–187, 2013.

[9] O. Trescases, W. T. N. W. T. Ng, and S. C. S. Chen, "Precision gate drive timing in a zero-voltage-switching DC-DC converter," in *Proc. IEEE ISPSD*, May 2004, pp. 55–58.

[10] J. Abu-Qahouq, H. M. H. Mao, H. Al-Atrash, and I. Batarseh, "Maximum Efficiency Point Tracking (MEPT) Method and Digital Dead Time Control Implementation," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1273–1281, Sept. 2006.

[11] V. Yousefzadeh and D. Maksimovi´c, "Sensorless optimization of dead times in dc-dc converters with synchronous rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 994–1002, Jul. 2006.

[12] A. V. Peterchev and S. R. Sanders, "Digital multimode buck converter control with loss-minimizing synchronous rectifier adaptation," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1588–1599, Nov. 2006.

[13] J. W. Kimball and P. T. Krein, "Real-time optimization of dead time for motor control inverters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 597–600.

[14] A. C. Oliveira, C. B. Jacobina, and A. M. N. Lima, "Improved dead-time compensation for sinusoidal PWM inverters operating at high switching frequencies," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2295–2304, Aug. 2007.

[15] S. Y. Kim and S.Y. Park, "Compensation of dead-time effects based on adaptive harmonic filtering in the vector-controlled AC motor drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1768–1777, Jun. 2007.

[16] J. S. Choi, J. Y. Yoo, S. W. Lim, and Y. S. Kim, "A novel dead-time minimization algorithm of the PWM inverter," in *Proc. IEEE IAS Conf. Rec.*, 1999, pp. 2188–2193.

[17] K. M. Cho,W. S. Oh, Y. T. Kim, and H. J. Kim, "A new switching strategy for pulse width modulation (PWM) power converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 330–337, Feb. 2007.

[18] D. M. Divan and G. Skibinski, “Zero switching loss inverters for high power applications,” in *Proc. IEEE-IAS Annu. Meeting*, 1987, pp. 627–634.

[19] S. Chen and T. A. Lipo, “A passively clamped quasi resonant DC link inverter,” in *Proc. IEEE-IAS Annu. Meeting*, 1994, pp. 841–848.

[20] R. Li, Z. Ma, and D. Xu, “A ZVS grid-connected three-phase inverter,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3595–3604, Aug. 2012.

[21] R. Gurunathan and A. K. S. Bhat, “Zero-voltage switching DC Link single-phase pulsewidth-modulated voltage source inverter,” *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1610–1618, Sep. 2007.

[22] J. He and N. Mohan, “Parallel resonant DC-link circuit- a novel zero switching loss topology with minimum voltage stresses,” in *Proc. IEEEPESC*, 1989, pp. 1006–1012.

[23] J. Cho, H. Kim, and G. Cho, “Novel soft-switching PWM converter using a parallel resonant DC-link,” in *Proc. IEEE-PESC*, 1991, pp. 241–247.

[24] S. Frame, D. Katsis, D. H. Lee, D. Boroyevich, and F. C. Lee, “A three phase zero voltage-transition inverter with inductor feedback,” in *Proc. VPEC Semin.*, 1996, pp. 189–193.

[25] X. Yuan and I. Barbi, “Analysis, designing, and experimentation of a transformer-assisted PWM zero-voltage switching pole inverter,” *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 72–82, Jan. 2000.

[26] J. Choi, D. Boroyevich, and F. C. Lee, “A novel ZVT inverter with simplified auxiliary circuit,” in *Proc. IEEE-APEC*, 2001, pp. 1151–1157.

[27] H. G. Eckel, L. Sack, and K. Rascher, “FPGA based control of an ARCP inverter without additional sensors,” in *Proc. IEE-EPE*, 1997, pp. 4385–4390.

[28] Y. P. Li, F. C. Lee, and D. Boroyevich, “A simplified three-phase zero current-transition inverter with three auxiliary switches,” *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 802–813, May 2003.

[29] G. Hua, E. Yang, Y. Jiang, and F. C. Lee, “Novel zero-current-transition PWM converters,” in *IEEE PESC Conf. Rec.*, 1996, pp. 438–442.

[30] H. Mao, F. C. Lee, X. Zhou, and D. Boroyevich, “Improved zero-current transition converters for high power applications,” in *Proc. IEEE-IAS Annu. Meeting*, 1996, pp. 1145–1152.

[31] Y. Li, F. C. Lee, and D. Boroyevich, “A three-phase soft-transition inverter with a novel control strategy for zero-current and near zero-voltage switching,” *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 710–723, Sep. 2001.

[32] R. C. Beltrame, J. R. Zientarski, M. L. Martins, and J. R. Pinheiro, “Simplified zero-voltage-transition circuits applied to bidirectional poles: Concept and synthesis methodology,” *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1765–1776, Jun. 2011.

[33] R. Li, Z. Ma, and D. Xu, “A ZVS grid-connected three-phase inverter,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3595–3604, Aug. 2012.

[34] Y. Levron and R.W. Erickson, "High Weighted Efficiency in Single-Phase Solar Inverters by a Variable-Frequency Peak Current Controller", *IEEE Trans. Power Electron*., vol. 31, no. 1, pp. 248-257, Jan. 2016.

[35] Q. Zhang, H. Hu, D. Zhang, X. Fang, J. Shen, and I. Bartarseh, “A controlled-type ZVS technique without auxiliary components for the low power DC/AC inverter,” *IEEE Trans. Power Electron*., vol. 28, no. 7, pp. 3287–3296, Jul. 2013.

[36] Y. Levron, S. Canaday, and R.W. Erickson, “Bus Voltage Control with Zero Distortion and High Bandwidth for Single-Phase Solar Inverters,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 258–269, Jan. 2016.

[37] T. Brekken, N. Bhiwapurkar, M. Rathi, N. Mohan, C. Henze, and L. R. Moumneh, “Utility-connected power converter for maximizing power transfer from a photovoltaic source while drawing ripple-free current,” in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf.*, 2002, vol. 3, pp. 1518–1522.

[38] N. A. Ninad and L. A. C. Lopes, “A low power single-phase utility interactive inverter for residential PV generation with small dc link capacitor,” http://sbrn.solarbuildings.ca/c/sbn/file_db/Doc_File_f/A_LOW_POWER_SINGLEPHASE_UTILITY_INTERACTIVE_INVERTER_FOR_RESIDENTIAL_PV_GENERATION_WITH_SMALL_DC_LINK_CAPACITOR1.pdf

[39] A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Predictive dc voltage control of single-phase PV inverters with small dc link capacitance,” in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 2003, vol. 2, pp. 793–797.

[40] R. Balog and P. T. Krein, “Automatic tuning of coupled inductor filters,” in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf*., 2002, vol. 2, pp. 591–596.

[41] S. A. Khajehoddin, M. Karimi-Ghartemani, P. K. Jain, and A. Bakhshai, “DC-bus design and control for a single-phase grid-connected renewable converter with a small energy storage component,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3245–3254, Jul. 2013.

[42] M. Karimi-Ghartemani, S. A. Khajehoddin, P. Jain, and A. Bakhshai, “A systematic approach to DC-bus control design in single-phase grid connected renewable converters,” *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3158–3166, Jul. 2013.

[43] P. T. Krein, R. S. Balog, and M. Mirjafari, “Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port,” *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[44] S. M. Tayebi, C. Jourdan, and I. Batarseh, “Dynamic Dead Time Optimization and Phase-Skipping Control Techniques for Three-Phase Micro-Inverter Applications,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7523–7532, Dec. 2016.

[45] S. M. Tayebi, X. Mu, and I. Batarseh, “Improved three-phase microinverter using dynamic dead time optimization and phase-skipping control techniques,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 1381–1386.

[46] G. Hua, C.-S. Leu, Y. Jiang, and F. Lee, “Novel zero-voltage-transition PWM converters,” *IEEE Trans. Power Electron.*, vol. 9, no. 2, pp. 213–219, Mar. 1994.

[47] R. Watson and F. Lee, “Analysis, design, and experimental results of a 1-kW ZVS-FB-PWM converter employing magamp secondary-side control,” *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 806–814, Oct. 1998.

[48] U. Drofenik, A. Musing, and J. Kolar, “Voltage-dependent capacitors in power electronic multi-domain simulations,” in *Proc. IEEE Int. Power Electron. Conf.*, 2010, pp. 643–650.

[49] G. Chindris, O. Pop, G. Alin, and F. Hurgoi, “New PSPICE model for power MOSFET devices,” in Proc. IEEE Int. Spring Seminar Electron. Technol., 2001, pp. 158–162.

[50] H. Hu, W. Al-Hoor, N. H. Kutkut, I. Batarseh, and Z. J. Shen, “Efficiency Improvement of Grid-Tied Inverters at Low Input Power Using Pulse-Skipping Control Strategy," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3129-3138, Dec. 2010.

[51] S. M. Tayebi, C. Jourdan, and I. Batarseh, “Advanced phase-skipping control with improved efficiency of three-phase microinverters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 3802–3806.

[52] S. Dusmez, S. Ali, M. Heydarzadeh, A. Kamath, and H. Duran, and B. Akin, “Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches,” *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 251-260, 2016.

[53] S. Dusmez, M. Heydarzadeh, M. Nourani, and B. Akin, “Remaining Useful Lifetime Estimation for Power MOSFETs Under Thermal Stress with RANSAC Outlier Removal,” *IEEE Trans. Ind. Inform.*, vol. 13, no. 3, pp. 1271-1279, 2017.

[54] M. Heydarzadeh, S. Dusmez, M. Nourani, and B. Akin, “Bayesian remaining useful lifetime prediction of thermally aged power MOSFETs,” in Proc. *IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 2718–2722.

[55] S. M. Tayebi, N Kutkut, and I. Batarseh, “Effects of Circuit Nonlinearities on Dynamic Dead Time Optimization for a Three-Phase Microinverter,” in Proc. *IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 1462–1466.

[56] Y. Levron. (2014). Automatic Design of Inductors for Power Conversion [Online]. Available at: http://www.mathworks.com

[57] D. Zhang, Q. Zhang, H. Hu, A. Crishina, J. Shen, and I. Batarseh, “High efficiency current mode control for three-phase micro-inverters,” in *Proc. IEEE Energy Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 892–897.

[58] S. M. Tayebi and I. Batarseh, “Analysis and Optimization of Variable-Frequency Peak Current Mode Control Techniques for Microinverters,” *IEEE Trans. Power Electron.*, in Print, 2017.

[59] S. M. Tayebi, N Kutkut, and I. Batarseh, “Analysis and Optimization of BCM Peak Current Mode Control Techniques for Microinverters,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 2644–2651.

[60] L. Gu, X. Ruan, M. Xu, and K. Yao, “Means of eliminating electrolytic capacitor in AC/DC power supplies for led lightings,” *IEEE Trans. Power. Electron.*, vol. 24, no. 5, pp. 1399–1408, May 2009.

[61] C. R. Sullivan, J. J. Awerbuch, and A. M. Latham, “Decrease in photovoltaic power output from ripple: Simple general calculation and the effect of partial shading,” *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 740–747, Feb. 2013.

[62] E. D. Dunlop, D. Halton, andH.A.Ossenbrink, “20 years of life and more: Where is the end of life of a PV module?” in *Proc. IEEE Photovoltaic Spec. Conf.*, 2005, pp. 1593–1596.

[63] S. Harb and R. S. Balog, “Reliability of candidate photovoltaic module integrated-inverter (PV-MII) topologies—A usage model approach,” *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 3019–3027, Jun. 2013.

[64] Y. Levron, H. Kim, and R.W. Erickson, “Design of EMI filters having low harmonic distortion in high-power-factor converters,” *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3403–3413, Jul. 2014.

[65] A. J. Roscoe, S. J. Finney, and G. M. Burt, “Tradeoffs between AC power quality and DC bus ripple for 3-phase 3-wire inverter-connected devices within microgrids,” *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 674–688, Mar. 2011.

[66] R. Balog and P. T. Krein, “Automatic tuning of coupled inductor filters,” in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf.*, 2002, vol. 2, pp. 591–596.

[67] P. T. Krein, R. S. Balog, and M. Mirjafari, “Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port,” *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[68] H. Alatrash , A. Mensah , E. Mark , R. Amarin and J. Enslin, “Generator Emulation Controls for Photovoltaic Inverters,” *IEEE Trans. Smart Grid,* vol. 3, no. 2, pp. 996–1011, Jun. 2012.

[69] R. Jalilzadeh Hamidi, H. Livani, S. H. Hosseinian, and G. B. Gharehpetian, “Distributed cooperative control system for smart microgrids,” *Electric Power System Research*, vol. 130, pp. 241-250, 2016.

[70] S. Shinde, S. M. Tayebi, H. Hu, N. Kutkut, and I. Batarseh, “Virtual Resistance Technique for Power Limit Management of Microgrid DG Inverters,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 1–7.

[71] S. M. Tayebi, H. Hu and I. Batarseh, “Advanced DC Link Voltage Regulation and Capacitor Minimization for Three-Phase Microinverters,” *IEEE Trans. Power Electron.*, in Print, 2017.

[72] R. W. Erickson and D. Maksimovic, “Pulse-width modulated rectifiers,” in Fundamentals of Power Electronics, 2nd ed. New York, NY, USA: Springer, 2001, ch. 18.

[73] Kjær, S. B. (2005). Design and Control of an Inverter for Photovoltaic Applications. Aalborg Universitet: Institut for Energiteknik, Aalborg Universitet.

[74] X. Chen, A. Pise, J. Elmes, and I. Batarseh, "A New Adaptive Switching Frequency Modulation for Optimizing Low Power Cascaded Buck-Boost Converter." *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1-7, Oct. 2017.

[75] W. Bower, C. Whitaker, W. Erdman, M. Behnke, and M. Fitzgerald. (2004). Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic Systems [Online]. Available at:http://www.energy.ca.gov/renewables/02-REN-1038/documents/2004-12-01_INVERTER_TEST.PDF

[76] S. M. Tayebi, and I. Batarseh, "Mitigation of Current Distortion in a Three-Phase Microinverter with Phase Skipping using a Synchronous Sampling DC Link Voltage Control," *IEEE Trans. Ind. Electron.*, in Print, 2017.

[77] S. M. Tayebi, S. Shinde, M. Pepper, H. Hu, and I. Batarseh, "Implementing Synchronous DC Link Voltage Control with Phase Skipping on a Three-Phase Microinverter using Minimum DC Link Capacitance," in *Proc. IEEE Energy Convers. Congr. Expo.*, Oct. 2017, pp. 1–8.