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DEVELOPMENT OF AN EFFICIENT MOLECULAR SINGLE-ELECTRON TRANSPORT SPECTROSCOPY

by

ALVAR RODRIGUEZ GARRIGUES B.S. University of Science and Arts of Oklahoma, 2010

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in the Department of Physics in the College of Science at the University of Central Florida Orlando, Florida

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Major Professor: Enrique del Barco

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ABSTRACT

In this thesis I present a complete and detailed guide for the development process and fabrication of efficient single-electron transistors (SETs) and a better single-molecule magnets (SMMs) deposition yield. Starting from a commercial Si/SiO_2 wafer I show the steps for the deposition of different layers to fabricate a SET as well as the improvements achieved in those for a completely functional SET device. The development process is based on a combination of optical lithography and e-beam lithography with metal deposition in ultra-high vacuum. The improvements involve a better conductance in the Al gate component, with a controlled formation of the superficial oxide layer and a faster feedback electromigration-induced breaking of Au nanowires for the creation of nanogaps at room temperature. The gate component is improved by increasing its thickness and exposing it to plasma oxidation for the complete oxidation of its surface. The nanowire breaking is realized at room temperature to make use of the surface tension of Au, which, after a previous feedback procedure, eventually opens the final gap in the nanowire. Finally, I demonstrate a new technique that allows increasing the yield of having a SMM connected in the nanowire gap. This new technique is based on monitoring the resistance of the broken nanowires during the SMM deposition from a controlled liquid solution at room temperature. When the resistance (>G Ω for open gaps) drops to values below Mega-ohms (characteristic resistance of a molecule bridging the gap) for a number of nanowires in the chip, the device is then ready for low temperature measurements.

To my family and my friends

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CHAPTER ONE: INTRODUCTION

Single-electron transistors (SETs) are very interesting experimental tools for investigating the transport properties of quantum systems, such as individual molecules, including single-molecule magnets (SMMs). In particular, SETs provide a exceptional way to study the unique characteristics of SMMs, such as quantum tunneling of the magnetization (QTM) and Berry phase interference (BPI) [1-3], at the individual molecular level. In the past 20 years SMMs have become a very attractive object of study in the physics and chemistry fields [4], particularly after the discovery of the important characteristics that these quantum systems present and the possibility of employing them in technology. SMMs are mostly composed of multiple transition-metal ions covered by organic ligands. The transition-metal ions give the molecules a large magnetic moment, which eventually results from the superexchange coupling between the constituent ions. The fact that the ligands leave the molecule well isolated from the surrounding environment and its intrinsic zero-field splitting (ZFS) provide the molecule with an uniaxial magnetic anisotropy, making SMMs behave as dependent microscopic quantum magnets embedded in a crystal lattice. One of the most interesting characteristics of these molecules is that the main magnetic parameters can be chemically modified at will, i.e. the ions in the core or the ligands surrounding them, in order to achieve molecules specifically designed for our studies.

Motivation

During the last years, SMMs have been proposed as systems for possible novel applications in emerging technologies, such as quantum computation and spintronics [5, 6]. With one bit per molecule SMMs can be used for ultra-high density magnetic memory devices and ultra-fast writing/reading memory units thanks to their singular magnetic behavior. SMMs have usually been studied in their macroscopic crystal form, where the quantum properties of a large number of identical SMMs show the magnetic characteristics coming from each single one. Although they have been extensively studied in their solid state form, a few studies have revealed the behavior of SMMs by means of measuring their single-electron transport behavior [7-9]. The most distinctive characteristics of SMMs are the quantum tunneling of the magnetization (QTM) and Berry phase interference (BPI), which result from the quantum superpositions of high-spin states of the molecule. Although the coherent manipulation of quantum states in individual SMMs have not been achieved yet, the fields' effort is pointing in that direction. Studying individually SMMs is a very challenging and interesting enterprise from the theoretical and the technological point of views. Controlling and understanding SMMs out of their natural crystalline environment by means of electric transport measurements will lead to important advances in quantum information and spintronics devices.

State of the Art

There are not many groups studying electrical transport through SMMs, partially due to the complexity that these experiments carry, since high technology instrumentation is necessary in order to make working transistors, as well as the great challenge of producing efficient depositions of individual molecules on the SETs. Physicists focus on achieving and controlling the magnetic properties of SMMs for a better understanding of their intrinsic behavior as individual entities. On the other hand, chemistry efforts are directed to obtain more stable molecules to survive the entire process of deposition, i.e. several research groups have demonstrated that from chemical functionalization of the ligands, SMMs can be attached to Au surfaces remaining their intrinsic characteristics unaltered [10]. In general, the progress in this field goes towards facilitating the study of the main quantum characteristics of SMM through single-electron transport measurements, which provide a spectroscopic tool to extract the energy landscape associated to the molecules at individual level.

Single-Electron Transistors (SETs)

SETs constitute an amazing device for measuring the transport properties of individual molecules. They consist on a three-terminal device in which the molecule is deposited in between the source and drain electrodes, directly atop the gate electrode. Figure 1 shows a schematic diagram of a molecular three-terminal SET device. Once the molecule is in between the two electrodes, electrons can jump through a sequential tunneling process in and out of the molecule when an electric potential is applied to the source, V_{bias} . The tunneling rates are represented by Γ_s and Γ_d , defining the number of electrons that tunnel though the potential barrier per unit of time, and when multiplied by |e| it gives the electrical current through the transistor. In a SET, the molecule is capacitively coupled with the electrodes giving three different capacitances: C_s , C_d and C_g . Finally, a voltage applied to the gate, V_{gate} , creates an external electric field which tunes the molecule's energy levels.

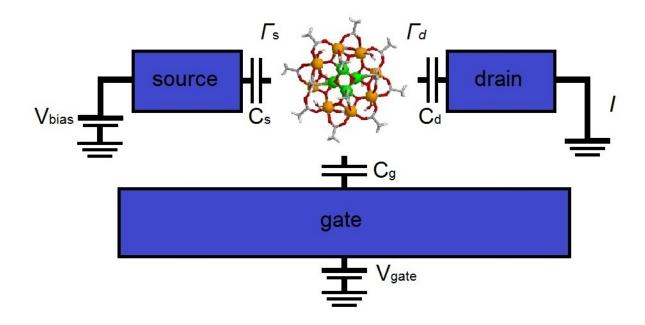


Figure 1: Schematic diagram of a SETs device. A molecule is trapped in the gap formed by the source and the drain electrodes and on top the gate component. V_{bias} is the electric potential difference applied in between the source and the drain electrodes. V_{gate} is the gate voltage applied to the gate component in order to generate an electric field which tunes the molecule's energy levels. C_s , C_d and C_g are the different capacitances between the molecule and the three electrodes. Γ_s and Γ_d are the tunneling rates for the electrons going in and out of the molecule.

Theory

Electronic transport in a macroscopic system is well defined by the Ohm's law:

$$\mathbf{J} = \boldsymbol{\sigma} \mathbf{E} \tag{1.1}$$

where the current density, **J**, is equal to the conductivity, σ , multiplied by the electric field , **E**. Although Ohm's law works perfectly in many macroscopic systems it fails in microscopic systems, where the conductance is quantized. However, this can be due to several reasons. For example, in small dimension systems, the charge carriers have no scattering with the conductor and ballistic conduction may occur. The main reason for this is that the mean free path is bigger than the whole system. Also, in molecular systems, the intrinsic properties of the electrodes in the contact areas can modify the electric transport since the molecules have a large charge addition energy and a quantized excitation spectrum [11]. In addition, transport experiments through microscopic systems need to be taken at very low temperatures in order to distinguish transport excitations associated to different electronic levels of the system, whose energy separation is characterized by ΔE . This means that:

$$k_{\rm B}T < \Delta E$$
 ($k_{\rm B} = 8.617\,3324 \cdot 10^{-5} \frac{\rm eV}{\rm K}$) (1.2)

The energy range in mesoscopic systems typically lies in the order of several electron volts. Consequently, experiments must be carried at sub-kelvin temperatures.

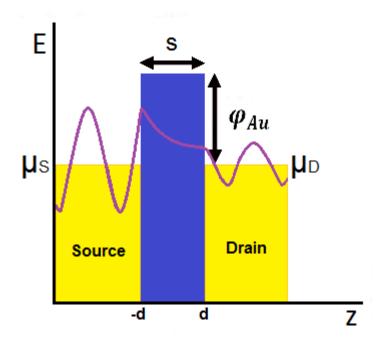


Figure 2: Schematic diagram of the electron wave function tunneling through a thin insulating film acting as a potential barrier. The potential barrier distance, s, is the separation between the source and the drain electrodes. The potential difference between the source/drain Fermi energies (represented by its electrochemical potentials, μ_S and μ_D , respectively) and the potential barrier is the work function, $\varphi_{Au} = 5.1 \ eV$ for gold.

In order to solve the Physics problems associated to a SET, we can divide the situation into two problems: a) A single-barrier problem; and, b) a double-barrier problem. On the one hand, when no molecule lies between the SET electrodes, the situation reduces to the problem of tunneling in one dimension with a single-rectangular potential barrier. Figure 2 shows an energy diagram of the single-barrier problem. In blue there is the potential barrier representing the distance of the gap, s. The electrodes, made of Au (in yellow), whose Fermi energy is represented by its electrochemical potential $(\mu_s \text{ and } \mu_D, \text{ respectively})$ have a work function of $\varphi_{Au} = 5.1 \text{ eV}$, which is the ionization energy or minimum energy required to remove one electron form it. This work function is lower than the potential barrier and in quantum mechanics when this is the case the wave function that represents the possibility of having a particle undergo tunneling through the barrier is not zero. Solving Schödinger's equation, in the three regions of the space, we obtain the solution:

$$\varphi(z) = \begin{cases} \varphi_1(z) = I_1 e^{ik_1 z} + R_1 e^{-ik_1 z} & z \le -d \\ \varphi_2(z) = I_2 e^{k_2 z} + R_2 e^{-k_2 z} & 0 < z < d \\ \varphi_3(z) = I_3 e^{ik_1 z} & x \ge d \end{cases}$$
(1.3)

$$k_1 = 8\pi^2 m E/h^2 \tag{1.3.1}$$

$$k_2 = 8\pi^2 m(V - E)/h^2 \tag{1.3.2}$$

Now applying the continuity conditions, the coefficient of transition or tunnel probability is:

$$T = \frac{|I_3|^2}{|I_1|^2} = \left[1 + \frac{1}{4} \left(\frac{k_1^2 + k_2^2}{k_1 k_2}\right)^2 \sinh^2(k_2 d)\right]^{-1}$$
(1.4)

This is a quantum effect only and it is due to the wave nature of microscopic systems. So, the electron can jump from one electrode to the other through the potential barrier with a certain tunnel probability. Now, using the WKB approximation in the intermediate-voltage range ($V < \frac{\varphi_{Au}}{e}$), the current flowing through the barrier is [12]:

$$J = \left(\frac{e}{2\pi\hbar s^2}\right) \left\{ \left(\varphi_{Au} - \frac{eV}{2}\right) e^{\left[-\frac{4\pi s}{\hbar}\sqrt{2m}\sqrt{\varphi_{Au} - \frac{eV}{2}}\right]} - \left(\varphi_{Au} + \frac{eV}{2}\right) e^{\left[-\frac{4\pi s}{\hbar}\sqrt{2m}\sqrt{\varphi_{Au} + \frac{eV}{2}}\right]} \right\}$$
(1.5)

expanding the square root in the same voltage range, the current tunneling through a nanogap is given by:

$$J \approx \left(\frac{e}{\pi h s^2}\right) \varphi_{Au} e^{-\frac{2\pi s \sqrt{2m\varphi_{Au}}}{h}} sinh\left(\frac{2\pi e s}{h} \sqrt{\frac{m}{2\varphi_{Au}}}V\right)$$
(1.6)

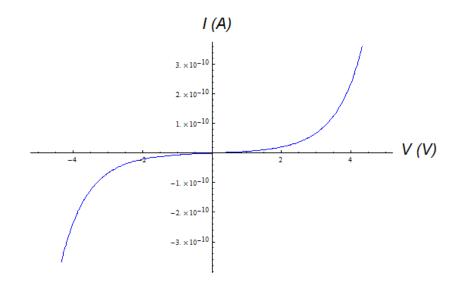


Figure 3: An example of theoretical current tunneling through a nanogap. Current, *I* (in A), in the y-axis and Voltage (in V) in the x-axis. From the slope of the graph near zero it is possible to extract the tunnel resistance $R = V \div I$ and obtain the approximate size of the gap [13]. Formula (1.6) has been used to obtain this graph with the following parameters: $\varphi_{Au} = 5.1$ eV, s = 1nm (gap size) and, in order to solve for the current, a cross sectional area equal to 850 nm² (thickness = 17 nm and width = 50 nm) have been employed, which constitute the characteristic cross-sectional dimensions of my SET electrodes.

From the solution of the single barrier problem, and measuring the tunnel resistance it is possible to obtain an estimate for the size of the nanogap, s, [13] and confirm that the SET is properly fabricated.

Our goal is to solve the problem in which the molecule is in between the source and the drain electrodes. This case corresponds to a double-rectangular barrier problem and in order to solve it we divide it into two parts: *i*) from the source to the molecule and *ii*) from the molecule to the drain. For a better understanding of this physics, Figures 4-7 illustrate the behavior of a SMM coupled with a SET. Figure 4 reproduces the energy scenery of transport in a one-molecular SET device with a molecule trapped in between the two electrodes. In the source and the drain (blue regions), electrons are in equilibrium and the Fermi energy is characterized by the electrochemical potential of these two electrodes, μ_S and μ_D , respectively, which can be tuned by changing the voltage between them, V_{bias} . The black regions represent the potential barriers between the molecule and the electrodes. These barriers are

related to the separation between the core of the molecule and the electrodes, which is maintained by the molecular ligands, which ultimately determine the tunnel characteristics of the device. The blue lines represent the occupied levels within the molecule, being the top one the highest occupied molecular orbital (HOMO). The white lines are the unoccupied energy levels of the molecule, being the bottom one the lowest unoccupied molecular orbital of the molecule (LUMO). As well, the electrochemical potential of the molecule is defined by the number of electrons, N, in its thermal equilibrium, μ_N . This first diagram (Figure 4a) represents the Coulomb blockade regime since the current cannot flow through the device, because no molecular levels are accessible for conduction. This is caused because the first unoccupied level is above the Fermi energy level of the source. In order to have electron transport, the Fermi energy of the source must be equal or larger than the first excited state of the molecule, i.e. $\mu_S \ge \mu_{N+1}$. Only in that case, the molecule can accept an extra electron and open a new channel for electrical conduction. This can be achieved by increasing the V_{bias} , rising the Fermi level of the source, until it reaches enough energy $\left(\frac{e^2}{c} + \Delta E\right)$, $\Delta E \equiv$ molecular electronic level spacing) to tunnel through the barrier and occupy the LUMO, as seen in Figure 4b. Once that level is occupied, further increasing of the V_{bias} does not translate to a further increase of the current through the device, since the next molecular energy level is not available to accept a second conduction electron (see Figure 4c). Consequently, the current only increases in steps separated by an energy equal to the energy separation between the molecular levels, ΔE .

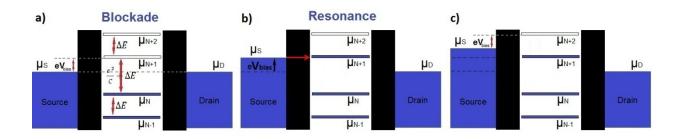


Figure 4: Schematic diagrams of blockade and resonance processes achieved varying V_{bias} . Source and drain are represented in blue, the two potential barriers in black and the molecule's energy levels lie in between them. The occupied levels are marked in blue and the unoccupied in white. μ_S , μ_D , and μ_N denote the electrochemical potentials representing the Fermi energy in the source, the drain and the molecule, respectively. a) Shows the blockade in the system since $\mu_S <$

 μ_N . b) shows the tunneling process when V_{bias} has increased μ_S , making $\mu_S \ge \mu_N$. c) Further increasing in the V_{bias} leads to a similar situation in where the current cannot continue to increase.

Besides using the bias voltage, the same conduction and blockade regimens can be achieved making use of the gate electrode. In this case, the gate voltage shifts up or down the energy levels of the molecule. Figure 5a shows the Coulomb blockade diagram with the Fermi energies well defined in the electrodes and in the molecule, and the occupied and unoccupied energy levels of the molecule. Increasing the gate voltage (V_{gate}) makes the energy levels of the molecule to move, making available the LUMO without having to apply a bias voltage. As shown in Figure 5b, once the LUMO level is occupied current will flow through the device. Further increasing of V_{gate} will make the system to enter into the Coulomb blockade regime again, having the molecule charged with N+1 electrons and where the new LUMO level (corresponding to the molecule with N+2 electrons) is not available for conduction, as illustrated in Figure 5c.

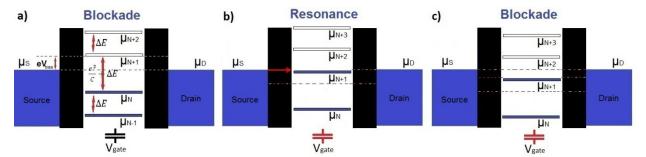


Figure 5: Schematic diagrams of blockade and resonances processes varying V_{gate} . a) Shows the Coulomb blockade in the system since $\mu_S < \mu_N$. b) Shows the tunneling process when the V_{gate} has decreased the energy of the molecule's energy levels, making $\mu_S \ge \mu_N$. c) The molecule, in the N+1 charge state, enters the Coulomb blockade regime again when the gate voltage is further increased.

Recording the blockade and resonance regimes upon varying both V_{bias} and V_{gate} , complete I-V graphs can be obtained. In a basic I- V_{bias} graph, the blockade regimes will be characterized by a constant current value and the resonance transitions by a rapid increase of the current. The peculiarity in this graph is that the transition (transport excitations or steps in the I-V curve) can be shifted by the application a gate voltage, V_{gate} . The gate voltage will move the blockade and tunneling transport steps, caused by V_{bias} .

to the left or to the right of the graph. In Figure 6a, there are three I-V_{bias} curves corresponding to three different V_{gate} values (current, *I*, in the y-axis and V_{bias} in the x-axis). The red one corresponds to a gate voltage that brings the first resonance down to zero bias voltage, while for the other two lines (different gate voltages), the system is in Coulomb blockade regime at zero bias (i.e. I = 0). This is due to the tuning of energy levels allowed by the gate. For the green and the blue lines there is not an available energy level around zero bias. On the contrary, in the red one, electrons find an unoccupied energy level at zero bias, which has been displaced by the gate. Moreover, a collection of these graphs can be united in a dI/dV contour-plot with the V_{gate} in the x-axis, V_{bias} in the y-axis and current, *I*, in the z-axis (color-coded), as illustrated in Figure 6b, which shows the characteristic response of a molecular SET. The three dashed vertical lines correspond to the curves depicted in Figure 6a, in order to appreciate how the characteristic SMM diamond plot is shaped and obtained by the excitations of the molecular energy levels. The two blue regimens differentiate two available charge states *N* and *N*+*I* of the molecule which can be achieved increasing V_{gate} or V_{bias}.

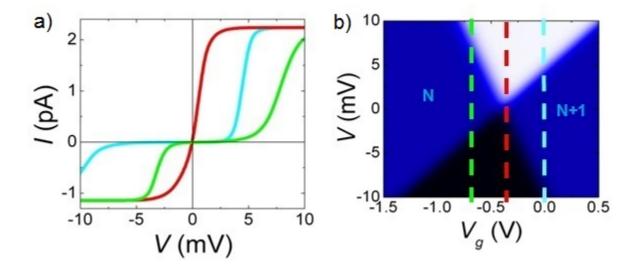


Figure 6: a). I-V_{bias} plot of three different V_{gate} values. b) Shows the Coulomb blockade diamond, characteristic fingerprint of a SET. It is obtained by a dI/dV contour-plot of the transport excitations of the molecular energy states and the Coulomb blockade regimes. In the contour-plot, V_{gate} is in the x-axis, V_{bias} in the y-axis and current, *I*, in the z-axis (color-coded). The three dashed color lines indicate the curves shown in a).

Once the different examples of having transport through a SMM have been noticed, the conclusion arrives to that all of them need an extra energy to change the equilibrium in the system and cause the single-electron transport. In order to know how much energy is necessary to break this equilibrium and let an electron jumps in and out of the molecule the problem needs to be treated theoretically. The coupling of the molecule with the source and the drain electrodes is of capacitance nature [14] and, any change on it, will change the electrostatic energy in the molecule [11]. To understand this, the system can be considered as a spherical capacitor, with the two shields separated by at least the length of the ligands, giving the following capacitance:

$$C = 4\pi\epsilon \left(\frac{1}{r_1} - \frac{1}{r_2}\right) \tag{1.7}$$

$$r_1 \equiv radius \ of \ the \ core \ of \ the \ molecule$$
 (1.7.1)

$$r_2 \equiv radius from the center of the molecule to the electrodes$$
 (1.7.2)

In a neutral molecule, there is a well-defined number of electrons, *N*, therefore, the charging electrostatic energy of the molecule is:

$$\frac{Q^2}{2C} = \frac{(Ne)^2}{2C}$$
(1.8)

And the corresponding molecular energy is the electrochemical potential, μ_N . Therefore, the total energy becomes:

$$U(N) = \sum_{1}^{N} E_{i} + \frac{(Ne)^{2}}{2C}$$
(1.9)

$$E_i \equiv chemical potential energy of the molecule with i electrons$$
 (1.9.1)

When an electron is added to the system, the total energy increases to:

$$U(N+1) = \sum_{1}^{N+1} E_i + \frac{\left((N+1)e\right)^2}{2C}$$
(1.10)

Giving a change in energy:

$$\mu_N = U(N) - U(N-1) = E_N + \frac{(N-\frac{1}{2})e^2}{C}$$
(1.11)

Which is the minimum energy required to add the *N*-th electron to the molecule. So, in order to have one more electron in the system of:

$$\mu_{N+1} = \mu_N + \frac{e^2}{c} + \Delta E \tag{1.12}$$

The electron needs to have an energy equal or greater than:

$$\frac{e^2}{c} + \Delta E \tag{1.13}$$

This last term is the charge addition energy where ΔE is the molecular electronic level spacing and $\frac{e^2}{c} = E_c$ is the charging energy.

Summarizing the above, in SETs there is only tunneling transport through the molecule when the electrons coming from the source beat the energy barrier such that their energy is $\geq E_C + \Delta E$ and they can jump in and out of the molecule, one by one in a sequential way. Moreover, SETs have two ways to achieve this tunneling transport: a) increasing V_{bias} , which gives the electrons enough charge energy to hop into the lowest unoccupied molecular orbital, or; b) increasing the V_{gate} , which tunes the molecule's energy levels by the charge energy amount producing that the lowest unoccupied molecular orbital equals the same energy level than the Fermi energy of the source. Typically, the charging energy in molecules (redox potential) lies in the order of 0.2 - 1 Volt, so it is important to select molecules with low redox potentials.

When looking at the electrostatic energy of the molecule one should also take into account the presence of the electrodes, which are capacitively coupled to the molecule. Including these effects, Equation (1.11) should be replaced by:

$$\mu_N = U(N) - U(N-1) = E_N + \frac{(N-1/2)e^2}{c_t} + eV_M$$
(1.14)

Where the electrochemical potential of the system is now affected by the external electric potentials applied at the source and gate, as follows:

$$V_M = \frac{1}{c_t} \sum C_i V_i = \frac{c_s}{c_t} V_{bias} + \frac{c_g}{c_t} V_{gate}$$
(1.14.1)

With total capacitance:

$$C_t = C_s + C_d + C_g \tag{1.14.2}$$

The new term (eV_M) describes the effect of the capacitive coupling of the individual electrodes with the molecule depending on V_{bias} and V_{gate} where C_t is the arithmetic sum of the three capacitances (source, drain and gate) [11]. Notice that there is no third term for the drain coupling in V_M , such as $C_d/C_t V_{\text{drain}}$, since V_{drain} is grounded. Moreover, the number of electrons, *N*, does not affect V_M , meaning that the charge addition energy ($E_C + \Delta E$) remains the same. However, the relative energy difference between the Fermi energy levels in the molecule, μ_N , and in the two electrodes, μ_S and μ_D , can be modified by increasing or decreasing V_{bias} and/or V_{gate} and it is proportional to the ratio between the total and the individual capacitances of the electrodes.

With this new term we can define the electrochemical potential of the N+1 electron state, μ_{N+1} , as:

$$\mu_{N+1} = E_0 + eV_M \tag{1.15}$$

where E_0 defines the chemical potential when V_{bias} and V_{gate} are initially equal to zero.

Moreover a new concept needs to be introduced in the case that conduction is allowed and electrons can hop in and out of the molecule by using the V_{gate} . The aligning of the LUMO with the Fermi energy of the source electrode defines the potential of crossing:

$$V_C = \frac{E_0}{|e|} \frac{C_t}{C_g} \tag{1.16}$$

which is the peak in the transport conductance and allows us to calculate the conductance of our system as a function of V_{gate} .

Collecting this new information and knowing that the transport depends on the capacitances besides of the tunnel probabilities, the ratio between the capacitances of the system can be extracted from the slopes in Figure 7b. Using Formulas (1.14.1), (1.15) and (1.16), the electrochemical potential of the N+1 electron state, μ_{N+1} , when the conductance is allowed or, in other words, when level alignment between the LUMO and the μ_s is achieved ($\mu_{N+1} = \mu_s$), gives:

$$\mu_{N+1} = E_0 + e \frac{(V_{bias}C_s + V_{gate}C_g)}{C_t} = e \frac{(V_{bias}C_s + (V_{gate} - V_C)C_g)}{C_t} = eV_{bias} = \mu_S$$
(1.17)

In which solving for V_{bias} gives:

$$V_{bias} = \frac{c_g}{c_t - c_s} \left(V_{gate} - V_C \right) = \frac{c_g}{c_g + c_d} \left(V_{gate} - V_C \right)$$
(1.18)

And in the case of solving (1.17) when the alignment is produced between the LUMO and the drain electrode ($\mu_{N+I} = \mu_D$) gives:

$$V_{drain} = -\frac{c_g}{c_s} \left(V_{gate} - V_C \right) \tag{1.19}$$

Formulas (1.18) and (1.19) are the relation of the capacitances between the electrodes and the molecule. This relation can be observed in the two slopes represented in Figure 7b which is the plot derivative of Figure 7a. We already described Figure 7a above in which the excitations separate the blockade regimes with N and N+1 electrons in the molecule, forming the characteristic diamond shape of a SET. Note that different slopes in Figure 7b correspond to different couplings to the electrodes, which is the common scenario in molecular SETs, where the molecule is uncontrollably deposited in the transistor gap, and attaches differently to the source and drain electrodes.

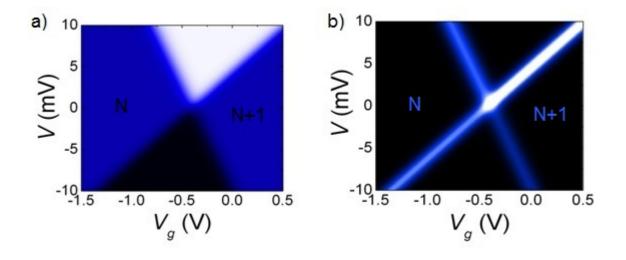


Figure 7: a) shows the Coulomb blockade diamond, characteristic fingerprint of a SET. It is obtained by a dI/dV contourplot of the transport excitations of the molecular energy states and the Coulomb blockade regimes. In the contour-plot, V_{gate} is in the x-axis, V_{bias} in the y-axis and current, *I*, in the z-axis (color-coded). b) is the plot derivative of a) from which the relation between the individual capacitances created with the molecule and the electrodes can be extracted using Formula (1.18) and (1.19).

Single-Molecule Magnets (SMMs)

Since the discovery of magnetic bistability in Mn_{12} physicists and chemists have worked together in order to obtain a better understanding of single-molecule magnets [4]. SMMs are mostly composed of multiple transition-metal ions forming the magnetic core. Transition-metal ions have incomplete 3d orbitals, resulting in a total spin S > 0 for the molecule. These ions couple together with a superexchange interaction providing the molecule a large spin value which, added to the molecule's intrinsic zero-field splitting (ZFS), generate an anisotropy barrier against magnetization reversal. The anisotropy barrier separates different sign projections converting the molecule into a single nanomagnet. All the properties of SMMs are most commonly studied when the molecules are in their crystal form, where they present the same spin magnitude and orientation and intermolecular interactions are small, making easier to study their intrinsic magnetic behavior [2, 15]. Studying only one SMM, however, can make the field to advance in understanding decoherence phenomena and set the basis of quantum computation and information storage [5, 6].

$$\mathcal{H} = -DS_z^2 + E(S_x^2 - S_y^2) + g\mu_B\mu_0 S \cdot H$$
(1.20)

Equation (1.14) shows the usual spin Hamiltonian representing the giant spin of a SMM, which is also known as the giant-spin Hamiltonian. The first term is the uniaxial anisotropy coming from the spinorbit interaction. It corresponds to the easy axis for the magnetic moment of the molecule and divides opposite 2S+1 spin projections by a parabolic anisotropy energy barrier. The second term also results from spin-orbit interaction, and conforms the transversal anisotropy in the perpendicular plane to the easy axis of the molecule. The contribution of this term is small comparing with the first one and it is mainly shaped by molecular symmetry, which modulates the energy separation between opposite projections of the spin. The third term is the Zeeman interaction of the spin with an external magnetic field, *H*. Figure 8 shows the schematic energy diagram for the SMMs double potential well where the first two terms of the Hamiltonian can be founded. The energy separation between the first two levels is sometimes denominated the zero-field splitting (ZFS), which is characteristic of each molecule.

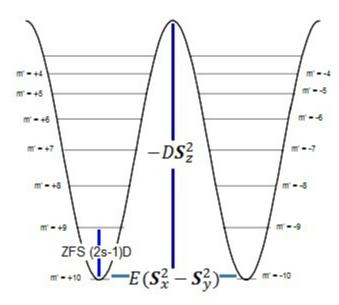


Figure 8: SMMs double potential well energy diagram produced by the 2S+1 energy levels of the molecule. $-DS_z^2$ is the uniaxial anisotropy potential barrier which determines the easy axis for the magnetic moment and is generated by spinorbit coupling. The transverse anisotropy term $E(S_x^2 - S_y^2)$, is determined by the symmetry of the molecule and leads to mixing of m levels and eventual tunneling across the barrier. ZFS (zero-field splitting) is the energy separation between the first two levels and it is an intrinsic property of SMMs.

The anisotropy terms in the spin Hamiltonian are what govern the characteristic quantum properties of SMMs, such as resonant quantum tunneling and Berry-phase interference, and configure the energy landscape of the molecular spin. A good understanding of this physics is important when looking for these characteristic properties through SET experiments, particularly when comparing the spin energies with the transport excitation energies. It is for this reason that SMMs with special properties have to be identified for the future transport experiments to be done with this technique. However, this thesis mainly deals with the technical aspects of the measurements. A more throughout explanation of the interesting properties of SMMs lies beyond the scope of this project, which will likely form the base of a immediate dissertation proposal, where the physics of SMMs and the expected behavior of electrical transport through a SMM will be discussed in detail.

Through this introduction chapter I have reviewed the very basis of SETs and SMMs. In chapter two I explain in detail the fabrication process and the optimization achieved in the SETs that I have developed at University of Central Florida in order to achieve better functional transistors. Moreover, I will present new SMMs (Mn_3 and Mn_4) synthesized by our collaborator George Christou at University of Florida which have been synthesized and adapted to fit my experiments. They have been altered in view of having low ground spin states, spin S = 6 in the case of Mn_3 and spin S = 9/2 in Mn_4 , well isolated from the first excited state, and remain mechanically robust in view of the stress that they undergo when deposited on the SET devices. Finally, I explain the optimization and the improvements in the deposition yield of SMMs on my SETs.

CHAPTER TWO: RESEARCH

Development of Efficient SETs

Building a functional single-electron transistor is not an easy task. Here I present a detailed guide on how to fabricate SETs with a satisfactory yield. First of all, it is required a commercial Si/SiO₂ wafer cut in 1.8 inch squares due to limits in size for the final fabrication steps. The Si wafers used in this guide have ~ 1 μ m of SiO₂ in order to avoid possible conduction with anything outside the final transistor. Also, it is necessary an optical mask made of Fe/Fe₂O₃ with the design of the different fabrication patterns for the optical lithography process. These patterns consist in different steps for the final fabrication of chips. Every chip will have 8 gates, with 5 nanowires lying on top of them, as can be observed in Figure 9a. Figure 9b is a picture example of how the gate looks with nanowires on top of it and Figure 9c is an example of a zoom into one nanowire on top of the gate. A total of 40 nanowires per chip will be in one of my measurements and every fabrication process will give 36 chips adding to a total of 1440 nanowires to achieve the desired results. I reduce the fabrication process down to 4 steps, or 4 layer processes, after which the breaking of the nanowires is produced making the fifth step. These 5 steps are: 1) First and second layer development and deposition, 2) Al layer (Al gate) development and deposition, 3) Al oxidation, 4) Nanowire layer development and deposition, and, 5) Nanowire breaking (Source and Drain electrodes creation).

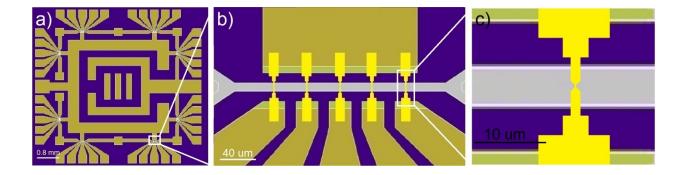


Figure 9: a) Pattern of one of our chips with 8 gates and 40 nanowires on top of the Si/SiO_2 wafer, the whole circuit occupies 6 mm². b) Zoom into one gate electrode (in gray) in the center of the pattern made by the first layer (in dark green) and the second layer (in dark yellow) with the nanowires are on top of it (in yellow). c) Zoom into one nanowire lying on the center of the gate electrode.

Step 1) First and Second Layer (Reservoir for the Source and Drain Electrodes)

I explain the first two layers at once due to their similarities in the fabrication process. The first one is a thin layer of ~ 15 nm thickness which is going set the base of the chips' shape and create a first contact (electric reservoir) between the third and fourth layers with the overall circuit (the second layer), avoiding "shadow effects". This layer was usually made of a combination of two layer deposited on top of each other, the first one of Cr and the second one of Au. Cr was used as sticking layer, but it is magnetic, so for my final magnetic purposes I switched it to Ti (non-magnetic), which is also a good sticking layer and will not give any magnetic noise when an external magnetic field is applied. Moreover, Au which is the metal more often used for this layer is substituted by Pd. The reason is that Pd is cheaper than Au and it is a conducting metal as good as Au for the final performance of the circuit in my experiments.

For the fabrication of the first three layers optical lithography is utilized which I will explain next. Before, in order to get ready for the lithography, the sample needs to be spin-coated with two photoresists: LOR 3A and Shipley S1813. After spin coating the LOR, the sample needs to be baked in a hot plate for 5 minutes at 175°C in order to hardening the photoresist. Right after the LOR baking, the sample is spin coated again with Shipley and baked for 2 minutes at 120°C. The Shipley photoresist will generate a layer of ~ 1.2 μ m thick on top of the sample which is perfect for evaporation and lift off processes. This is a two layer photoresist lithography process that allows for an undercut and produces better edges when working in reduced dimensions. The spin coater specifications for these two photoresists are given in Table 1.

Table 1: LOR 3A and Shipley S1813 photoresists spin coating recipe. After the LOR the sample needs to be baked for 5 minutes at 175°C and after the Shipley for 2 minutes at 120°C.

LOR 3A	Shipley S1813
2s at 500rpm / 30s at 3000rpm / 2s at 0rpm	2s at 500rpm / 30s at 5000rpm / 2s at 0rpm

Once spin coating is done, the sample needs to be aligned for the patterning of first layer using the Fe/Fe₂O₃ mask on top of the photoresist layers. Once the alignment is completed, the sample is exposed to UV light in the optical lithography process. Optical lithography (or photolithography) consists on exposing the photoresists to UV light of a known power per unit area during a specific interval of time. The UV breaks the polymer chains of the photoresists drawing the desired pattern, which has been correspondingly designed on the mask. The exposing relation to UV light in my chips is always: $126 \frac{mJ}{cm^2}$. After the exposition, the sample needs to be developed with CD-26 Developer for 45 seconds in order to remove the photoresists damaged by the UV light (the sample is placed into DI water for stopping the CD-26). If the pattern is well developed, with patterned features showing sharp edges and uniform color all over the chip, then the sample is baked at 130°C for 5 minutes and developed again in CD-26 for 1 more minute. The CD-26 is used a second time in order to undercut the LOR for favoring a better lift off after the deposition. Figure 10 shows optical images for different zoom magnifications of the first layer after the development process.

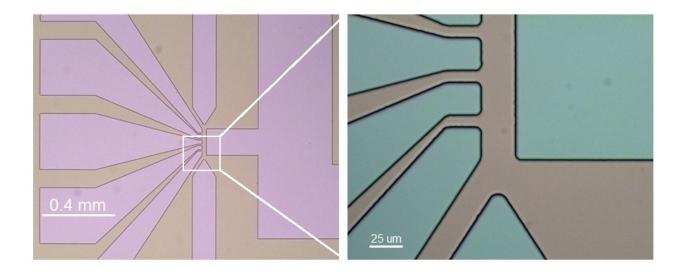


Figure 10: Optical images of the final result in the first layer development process where our transistors will be placed. LOR 3A and Shipley S1813 has been spin coated and then exposed to UV light in the photolithography process. The brown areas are where the photoresist remains after developing, the purple(left) and green(right) areas show the bare wafer with the photoresist removed.

Once the desired pattern is developed on the chip, it is time for the metallic evaporation. The Ti and Pd layers are electron-beam evaporated in high vacuum conditions ($\sim 10^{-7}$ Torr) following the parameters given in Table 2.

Table 2: Evaporation parameters for an electron beam evaporation of a thin layer of Ti (3nm) followed by Pd (12nm) in the first layer of the SETs.

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	Ti	Pd
Density	4.5 g/cm ³	12 g/cm ³
Z-ratio	0.628	0.357
Deposition Rate	1 Å/s	0.4 Å/s
Thickness	3 nm	12 nm
Current	~30 mA	~30 mA

Finished the evaporation, it is necessary to lift off the metals from the sample for the final result in the first layer. For this purpose the sample is introduced in PG Remover for several hours at 80°C. The metals will lift off slowly and it may be possible to have to spray the sample with the PG itself to help in the process. In Figure 11 we can observe the final result of the desired pattern as well as the sharpness achieved thanks to the photolithography followed in this fabrication process.

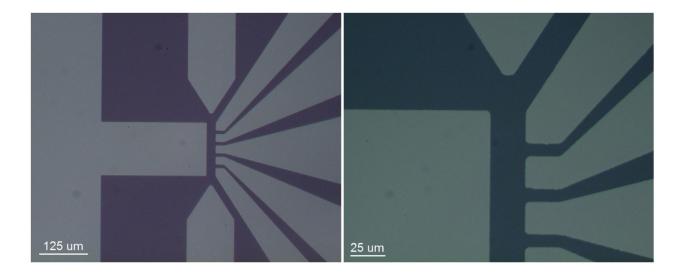


Figure 11: Optical images of final result in the first layer of the SET devices. A thin layer of Pd (12nm) evaporated on top of the Ti (3nm) (light areas) evaporated on the Si/SiO2 wafer (dark areas).

In the past, the second metallic layer consisted on ~ 200 nm thick Au layer on top of a thin Cr adhesive layer which (the second layer) was deposited on top of the first one except in a few micrometers at the edges. Now Pd and Ti are used instead of Au and Cr for the reasons explained below for the case of the first layer. Moreover, the Pd is now evaporated only until reaching a thickness of ~70 nm which works equally well than the previous ~200 nm thick Au layer while it substantially improves the lift off process. The few micrometers left uncovered at the edges of the first layer will make the first contact for the gate and the nanowires (third and fourth layers) with the overall circuit. In Figure 12, optical images of the development of the second layer show these few nanometers left covered with photoresist in the first layer (see arrows in Figure 12). The second layer is particularly important for three reasons: First, it

is a thick layer that reduces the overall resistance of the whole circuit. Second, it facilitates wire bonding of the electrical contacts needed for having access to the final SETs. Third, it creates the thick markers needed for e-beam lithography process in the nanowire layer, therefore the alignment of the gate electrode respect to the second layer is crucial for having the nanowires laying in the center of the gate. As this layer is the only one with the nanowire markers, Cr is evaporated again. The second layer is developed following the same steps as with the first layer, using LOR 3A and Shipley S1813 photoresists for the same UV exposure and baking time. The aligning of the second layer needs to coincide with the center of the first layer, leaving out these few micrometers of the first layer at the edges, for the reason that I mentioned before. The patterned photoresist layer is shown in Figure 11 on top of the first layer.

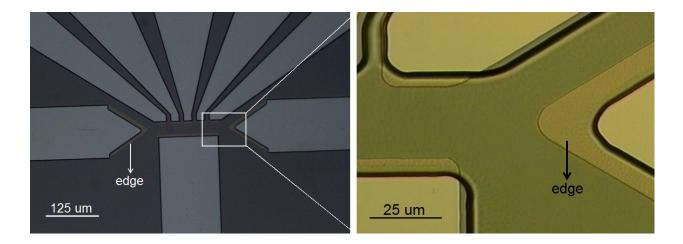


Figure 12: Optical images of the patterned photoresist layer prior to the e-beam evaporation of the second and thicker Ti/Pd layer. The ends of the different electrodes are left covered with the photoresist, such that the thickness of the metal at the edges remains thinner that in the rest of the chip.

Subsequently, the thick Pd layer is deposited by means of electron beam evaporation following the parameters given in Table 3. After the deposition, the lifting off in this layer is done equally than in the previous one with PG Remover at 80°C.

Table 3: Metal e-beam evaporation for the second layer with 8nm of Ti and 72 nm of Pd.

	Ti	Pd
Density	4.5 g/cm^3	12 g/cm ³
Z-ratio	0.628	0.357
Deposition Rate	1 Å/s	1.4 Å/s
Thickness	8 nm	72 nm
Current	~30 mA	~40 mA

Figure 13 shows optical images of the final result in the second layer deposited on top of the first one where we can observe the 15nm thick first layer (dark shadows) protruding out of the edges of the second 80nm thick layer (light areas), as indicated with arrows in Figure 13.

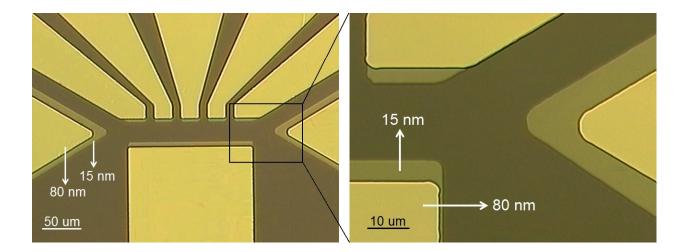


Figure 13: Optical images of the final result in the second layer e-beam evaporation of Ti (8nm) and Pd (72nm). In between the first layer (15nm) and the second layer (80nm) there is an step for favoring a better contact of the following layers (gate layer and nanowire layer).

Step 2) Third Layer / Al Gate

This layer is probably the most difficult to achieve and the one that more troubles can make. This one forms the gate electrode in our SETs, therefore, it needs to display a thin insulating layer at the surface while maintain its high conductivity properties underneath. Moreover, the surface of this layer needs to be smooth in order to minimize the leakage of current into the source and drain electrodes that will come on top of it. Aluminum is chosen for being a good conductor which can be oxidized naturally to create an Al_2O_3 layer of about 2 to 4 nm at its surface. This oxide layer is enough to avoid electric conduction between the source and drain electrodes and the gate. The standard fabrication (including our own group in the past) of this layer is ~15 nm thick deposited at LN₂ temperatures and letting it oxidize itself at ambient conditions. The evaporation is made at low temperatures to avoid excessive heat from the e-beam source and, consequently, avoid cracks on the layer, which can generate leaks to the other electrodes and complicate the conductance of the gate. Typically, this approach led to very low yields, with only 50% of the gates functional, display excessively high resistances ~1.5 k Ω , indicating a much thicker oxide layer than expected. Our group had several problems in the past with this step and I focused in solving them by means of increasing its functionality and yield, achieving better conductance for all the gates.

First of all, I realized that cooling the sample down to LN_2 temperature could be a problem of attracting impurities during the evaporation (like in a diffusion pump) making bad depositions and decreasing the gate functional yield. Recently, our group has switched to a new evaporator where the ebeam evaporator source is far from the sample, so heating is substantially decreased. With this new condition, room temperature deposition produces a final flat and smooth surface without the need of LN_2 . An example of a room temperature Al gate deposition is shown in Figure 14, which shows AFM images and the corresponding roughness analysis. This analysis results that the RMS of the surface roughness in the Al gate is less than 2 nm which does not give any kind of leaking problems neither with the source and drain electrodes nor with the molecule.

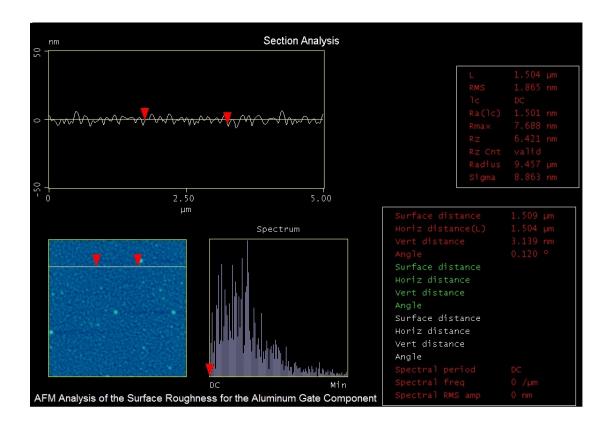


Figure 14: AFM analysis of the surface roughness for the Al/Al₂O₃ gate component deposited at room temperature from an e-beam source. The RMS of the roughness measured is 1.865 nm.

Secondly, having achieved a substantially smoother surface, I focused on improving the conductance through the gates, arriving into the conclusion that making a thicker layer, of around 35 nm, solves the problem. A thicker layer gives a better conductance in all the gates avoiding cracks and decreasing the chances of bad depositions. So now, fabricating this layer thicker with e-beam evaporation at room temperature results in > 90% working gates per chip, with a resistance of around ~ 150 Ω , which is much closer to the expected resistance (~50-100 Ω) for the dimension of our gates assuming that only a 2-4 nm oxide layer is formed at the surface. However, making this layer thicker forced me to make some

changes in the fourth layer, since thin nanowires have to come across the gate layer. The usual nanowire thickness employed in out SETs is ~ 17 nm, and cannot be increased because higher currents would be needed to reach the critical current density required for the electromigration-breaking and formation of the nanogaps. However, such a thin nanowire would break when it jumps over the 35 nm thick edge of the Al gate. I will explain the solution to this in the following section, where the corresponding changes in the nanowires layer are implemented in order to allow working with thick (35nm) Al layers.

The pattern corresponding to the third layer (Al gate) is developed by optical lithography similarly than with the first two layers. However, in this case, the alignment of the gate within the pattern formed by the two first layers is critical and extreme care needs to be placed here, otherwise the fourth layer (the nanowires) will not sit properly on top of the central Al gate line. Figure 15 shows the pattern written on the photoresist layer prior deposition of the Aluminum, which is perfectly aligned with respect to the first and second metallic layers.

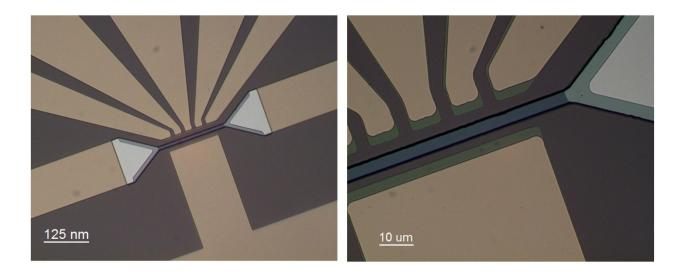


Figure 15: Optical images of the photoresist pattern prior deposition of the Aluminum gate. The aligning of this layer needs to coincide with the middle part of the first two layers, first Ti/Pd (3/12nm) layer in dark green and second Ti/Pd (5/80nm) layer in light brown.

Aluminum is e-beam evaporated according to the parameters given in Table 4.

	Al
Density	2.7 g/cm ³
Z-ratio	1.08
Deposition Rate	0.6 Å/s
Thickness	35 nm
Current	~200 mA

 Table 4: E-beam evaporation parameters at room temperature of the Aluminum layer forming the gate electrode.

Finally, optical images of the final result of the Aluminum gate aligned in the middle of the first two layers are shown in Figure 16.

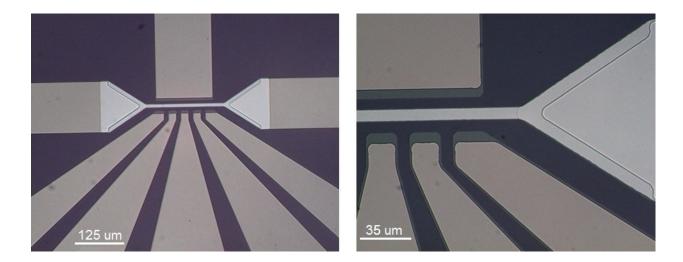


Figure 16: Optical images of the deposited Aluminum gate (35nm) in gray. The gate is situated in the center of the pattern formed by the first two layers, first layer (Ti/Pd 3/12nm) in dark green and second layer (Ti/Pd 5/75nm) in light brown, as seen in the figure on the right.

Step 3) Al Gate Oxidation

This step is based on achieving a more controlled oxidation of the Al gate layer. Typically, this oxidation was made by leaving the sample 24 hours in atmospheric conditions, which, in some occasions, produced conductance leaking between the gate and the source or drain electrodes (the final layer). In order to improve it, first, I decided to introduce O₂ into the chamber right after the Al deposition for 45 minutes at 250 mTorr. Oxidizing the aluminum in the chamber will avoid trapping impurities in the oxidize layer completing a smooth and total oxidation of the layer. The O₂ will oxidize the Al in the chamber before the lift off process instead of after as in the previous procedure. The lift off is another critical part in the process of the gate layer because I detected that the PG Remover, needed for the lift off, partially eats the oxidation producing leaks between the gate and the electrodes. So, a new lift off process needed to be formulated. This new process consists on dipping the sample during 6 hours in Acetone, checking periodically, followed by 1 hour in PG. Although, the PG cannot be avoided from the lift off process, because Acetone does not lift off the LOR resist, at least its use is reduced to the minimum.

Finally, after introducing O_2 right after the deposition and reducing the time of the PG Remover in the lift off process, the sample is forced to a more rigorous oxidation with O_2 plasma. The O_2 plasma finalizes the oxidation of the Al gate in order to make sure that no electric leaking can be produced. For this purpose, the specifications shown in Table 5 are needed to be followed in a plasma oxidation chamber. Table 5: Parameters of the O₂ plasma oxidation for the Aluminum gate. SCCM stands for standard cubic centimeter per minute.

SCCM	Power	Pressure	Time
12.6	50 W	100 mTorr	10 min

The plasma oxidation gives a final resistance for the gates of ~ 200 Ω . Compared to the ~ 1.5 k Ω that our group used to obtain with the old method, the resistance has been reduced by a factor of 10. This shows a better conductance in the gates as well as guarantees making them more efficient because now the oxide layer is thinner and the molecules can be closer to the voltage applied to the Al layer (V_{gate}), resulting in a more efficient gating of the molecules.

Another advance of this oxidation process is that it results in a higher electric breaking point of the oxide layer insulating the gate component from the electrodes, which allows employing higher gate voltages before current starts to leak into the electrodes (i.e. dielectric rupture of the insulating layer). The electric breaking point limits the maximum V_{gate} that can be applied, restringing the tunability degree of the energy levels of the molecule. To characterize the dielectric rupture point, we sweep the V_{gate} while monitoring the current between the gate and one of the electrodes. Note that this is done after depositing the nanowires on top of the gate. Figure 17 shows the process where the current between the gate and one of the electrodes is exponentially small below the breaking point, demonstrating a good insulation between those two (tunnel barrier), while when the breaking point is reached a drastic increase in the conductance is obtained. The breaking point is founded in several different chips lying in the 4.5-5.0 Volts range, constituting an important improvement with respect to the previous gates fabricated in our lab in the recent past, where breaking points in the 2.5-3.0 Volts where typically found.

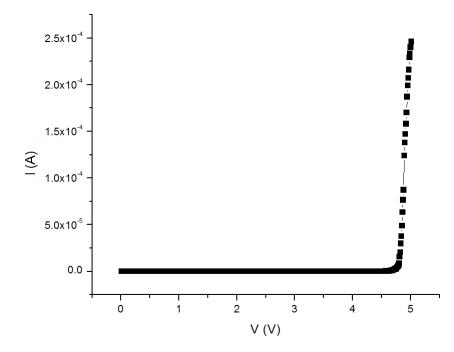


Figure 17: Electric breaking point of the Al_2O_3 layer separating the Al gate from the source and drain electrodes (nanowires). The voltage is applied to the gate while the current between the gate and one of the electrodes (grounded) is monitored. The breaking point of the insulator layer was found to lie in the 4.5-5.0 V range from several different chips.

Step 4) Fourth layer (Nanowires)

The fourth layer is the last layer of the fabrication process and it will eventually form the source and drain electrodes after the electromigration-induced breaking process (Step 5), completing the singleelectron transistors. This layer consists on a set of 5 independent nanowires crossing on top of each of the 8 Al gates in the chip. They are made out of Au, partly due due to the well-known conduction properties of this material at reduced dimensions, since in the narrowest part of the nanowires they are only 50 nm wide. The nanowires layer is ~17 nm thick and partially deposited on top of the gate and connected to the overall circuit (first and second layers), as illustrated in Figure 18a. When they sit over the gate, on top of the insulator Al_2O_3 layer, their dimensions go from 1 µm wide down to 50 nm wide at the center of the gate (see Figure 18b). These reduced dimensions try to minimize the surface area between nanowires and gate and avoid possible conduction leaking between them. The nanoconstiction is practiced at the center of the Al gate in order to form the gap where the gating electric field is maximum. This layer has been usually fabricated in a single deposition step, but now that the Al gate layer is thicker (35 nm) the nanowires need to be redesigned.

With the old Aluminum gates, the nanowire layer consisted on a single e-beam evaporation of Au to form a ~17 nm thick layer. As mentioned earlier, with the new gates 35 nm thick, a 17 nm thick nanowire would disconnect when stepping on top of the gate. One solution could be making the nanowire thicker than the gate and that would solve the problem, however, that would increase the cross-sectional area of the wire and it would unnecessarily impose much larger currents to reach the maximum current density in the electromigration process needed for making Au atoms drift and creating the gap to separate the source from the drain electrodes. In addition, higher breaking voltages would be necessary, causing uncontrolled ruptures of the nanowires and likely damaging the molecules with excessively strong local electric fields. Finally, the molecules could bridge the gap at the top part of a thicker nanowire, being much further away from the gate and feeling an smaller gating electric field, which would in turn reduce the degree of controlling the electrostatic state of the molecule. For these reasons, I decided to divide this layer into two parts: first a ~ 17 nm thick Au layer running across the gate (as in the past), which will be broken by the gate at the edges, and then another layer thicker than the gate which will make the contact of the nanowire on top of the gate with the overall circuit. However, this thicker layer (~50 nm) of Au will be deposited right on top of the thin one without covering the narrowest part of the nanowires, where the breaking will be produced. This second layer makes the connections of the nanowires with the circuit over the gate, keeping the same thickness than in the previous procedure for the central and narrowest part (e.g. the nanowire).

For the fabrication of these two new layers I use e-beam lithography. E-beam lithography works as optical lithography, but, in this case an electron beam source is used instead of a UV lamp. The e-beam

source provides more precision in the written pattern, which in the case of the nanowires need to be 50 nm wide in their thinnest part. The development for e-beam lithography is similar than in the previous layers, but now MMA and PMMA e-beam resists are used instead. Both resists are spin coated on the sample and then baked for 5 minutes at 175°C. The parameters needed for this spin coating are given in Table 6.

Table 6: Parameters for the spin coating of MMA (8.5) EL 6 and 950 PMMA C 2 e-beam resists for the fabrication of the patterned nanowire layer. After each spin coating, the sample is baked for 5 min at 175°C.

MMA (8.5) EL 6	950 PMMA C 2
2s at 500 rpm / 60s at 4000 rpm / 2s at 0 rpm	2s at 500 rpm / 60s at 6000 rpm / 2s at 0 rpm

Once the sample is written by e-beam lithography it needs to be developed in a solution composed of 3 IPA : 1 MIBK for 45 seconds which is stopped by rinsing the sample with IPA. Figure 18 shows optical images of the first thin nanowire pattern written on the e-beam resists layer.

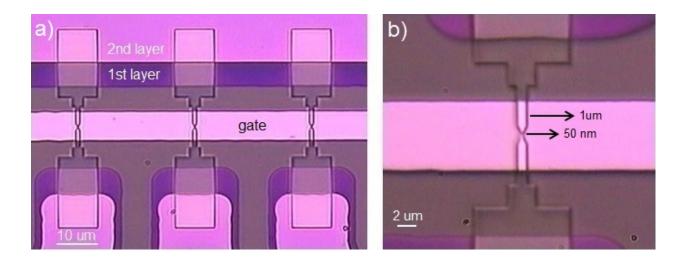


Figure 18: Optical images of the first thin nanowire pattern (thin Au layer) written on the e-beam resists layer. The nanowire gets thinner in the center part of the gate electrode going from 1 µm to 50 nm.

After the e-beam writing and the development, a thin Au layer forming the base of the nanowires is deposited by e-beam evaporation following the parameters shown in Table 7. The nanowire layers have no sticking material underneath because an adhesive layer will make the wire much harder to break in the electromigration process.

Table 7: Parameters for the e-beam evaporation of the thin Au layer forming the basis of the nanowires and creating the narrowest part of it there the breaking will take place.

	Au
Density	19.3 g/cm ³
Z-ratio	0.381
Deposition Rate	1.5 Å/s
Thickness	17 nm
Current	~ 50 mA

For the lift off process it is very important to only use Acetone. PG remover would degrade the oxidize Al layer. This lift off can take a long time and it needs to be gently done, checking it frequently. Figure 19 are optical images of the thin (17 nm) nanowire layer after the lift off process. Figure 19b is a zoom into one single nanowire where in the middle part of it we can appreciate the narrowest part which is not going to be covered by the second thick nanowire layer and where the breaking is going to occur.

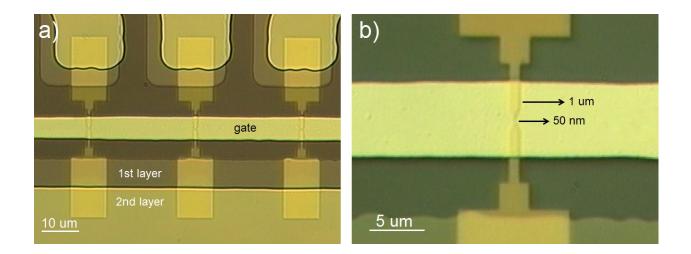


Figure 19: Optical images of the final result of the first nanowire layer (thin nanowire layer). a) Overview of the thin nanowire layer in the circuit. b) Zoon into one single nanowire observing the thinnest part of it (50nm) where the breaking is going to occur.

In order to complete the process, and connect the thin Au nanowire (17 nm), over the Al gate (35 mn) to the overall circuit, a second Au layer is evaporated. This last step consists on evaporating a 50 nm of Au on top of the first nanowire layer without covering the nanowire constriction at the center of the gate. The development is exactly the same as in the before layer. Figure 20 shows the second thick nanowire pattern written on top of the e-beam resists layer.

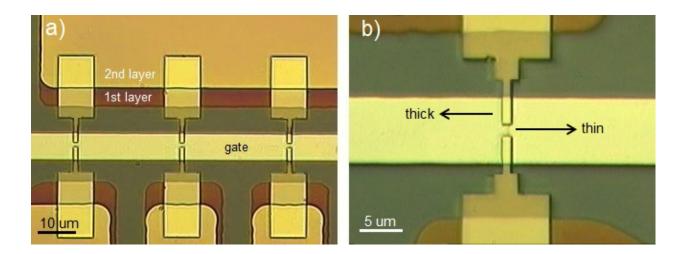


Figure 20: e-beam resist pattern for the second thick nanowire layer on top of the first thin nanowire layer. In b) it can be observed that the narrowest part of the nanowire in the center of the gate is not covered by the resist.

The parameters for the e-beam evaporation of this last layer of Au are given in Table 8.

Table 8: Parameters for the e-beam evaporation of the thick Au nanowire layer which will connect the thin nanowire layer to the overall circuit.

	Au
Density	19.3 g/cm³
Z-ratio	0.381
Deposition Rate	1.5 Å/s
Thickness	50 nm
Current	~ 50 mA

Figure 21 is the final result in the nanowire fabrication process showing the aspect of the two layers of nanowires evaporated across the gate. Figure 21b shows a zoom into one of the wires where the narrowest part of the nanowire is clearly seen.

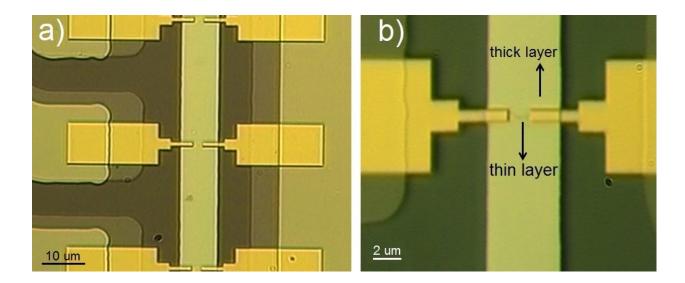


Figure 21: Optical images of the final result in the nanowire fabrication process. a) Nanowires lying on top of the Al gate. b) Zoom into a single wire, where the thinnest central part (nanowire) is left at the center of the gate. Once the nanowires are finished, their resistances are measured in order to determine their quality. Usual resistances found in our devices are ~95 Ω , as expected from the dimensions used in our design. This last step finishes the deposition process and now the nanowire needs to be broken in order to create the source and the drain electrodes. One big note for these last deposition layers is that if in any of the fabrication steps the gates lose conductance it does not mean that they are broken. I figured out that taking the chip into a probe station and situating the probe station tips on top of the ends of the Al gate component (sometimes scratching is needed) the conductance will come back again. I think that this is due to some isolation produced by the polymers in the developing process and rarely occurs.

The nanowires layer has been the last step in our SET evaporation process. Figure 22 shows a SEM image of a finished nanowire on our chips where the step in between the two layers explained in this section can be appreciated.

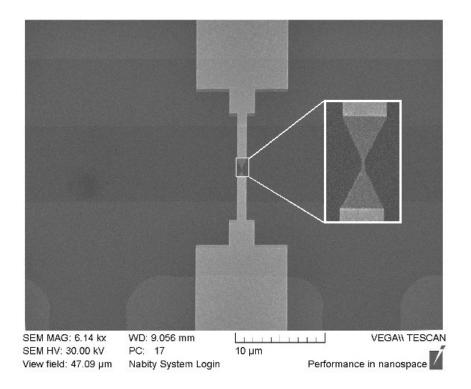


Figure 22: SEM image of the final shape of the Au nanowire on top of the Al gate. The gate is 35 nm thick and the nanowire is composed of two layers: one 50 nm thick and another 17 nm thick.

Step 5) Nonowires Breaking

At this point in the fabrication process, functional SETs are not fabricated yet. We have two layers making the base of the circuit and Au nanowires, 17 nm thick in the narrowest part, on top of a Al/Al₂O₃ gate layer. So, the next step is to break these nanowires and create nanogaps which will separate the source and the drain electrodes. In order to create the gap in the nanowires a feedback-controlled electromigration-induced breaking process is used. The electromigration process consists on applying an electric potential to a nanowire until the Au maximum current density is achieved ($j_b = \sim 5 \cdot 10^{12} \text{A/m}^2$ [16]), forcing the atoms to drift under the action of the strong local electric field until the nanowire breaks. Before the nanowire breaks completely a feedback program reduces the voltage making the nanowire to break only partially. The amount of breaking is controlled by monitoring the percentage of change in current associated to the break. The percentage can be run at will and it is chosen to achieve a complete rupture in the shortest time possible, which has been around 30-40 minutes per wire with the sample placed in our He₃ cryostat. The whole breaking process has been typically performed at 4 K with the molecules already deposited. The main reason for this was to maintain the created gap fixed after the breaking, which is guaranteed at low temperatures. However, the molecules need to be already deposited because driving the Au atoms back to room temperature, in order to deposit the molecules after the break, would move the Au atoms further away increasing the size of the gap. This old process carries two main problems: First, it provides an extremely low yield of getting molecules bridging the gap after the electromigration process and, second, it is an expensive process since it consumes liquid Helium and deprives other experiments to be run in the group while the breaking occurs.

In order to improve this step, first I focused on breaking the nanowires at room temperature. Using the old breaking program would make large gaps in the wires to begin with, and those would keep opening at room temperatures while the rest of the wires are being broken. The new approach consist on a substantially accelerated feedback process in where several parameters can be adjusted attending to the rupture stage, as explained below. However, the main advance is that now we do not use the feedback loop of voltage to completely break the nanowire. Indeed, we break the nanowire until leaving only a few atoms left at the central part and let the surface tension of Au to complete the job and form the nanogap. This is achieved by monitoring the resistance of the wire during the breaking until it grows close to the quantum resistance associated to conduction to a single Au atom or one channel transmission (Landauer formalism):

$$R_0 = \frac{1}{G_0} = \frac{h}{e^2} = 25.8 \, k\Omega \tag{2.1}$$

After stopping the breaking program at this point and motoring the resistance of the nanowire, a gradually increase is appreciated as the nanogap is formed. The resistance finally stabilizes at a few G Ω , which is similar to the resistance obtained with the old process at low temperature, meaning that the formed gap is around 1-3 nm, a perfect size for our molecules. Therefore, this new procedure gives the same gap sizes as the old one does, but now the whole process can be performed at room temperature and, as I show below, in much shorter times. Figure 23 shows a SEM image of a nanowire before and after the feedback-controlled electromigration-induced breaking process at room temperature creating the final source and drain electrodes of our SET.

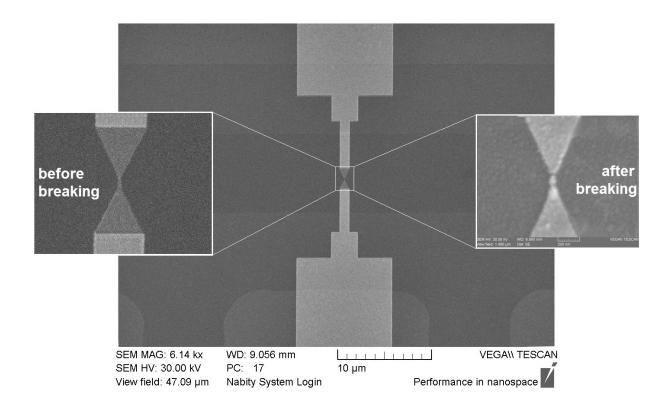


Figure 23: SEM picture of a nanowire before and after the break. A zoom into the thinnest part of the nanowire at the left side shows the point where the nanogap is going to be produced after the feedback-controlled electromigration-induce process. In the right part of the image there is a zoom into the nanowire after the feedback-controlled electromigration-induced breaking process where the nanogap can be appreciated, differentiating the source and the drain electrodes, between which the molecule will be introduced for the final measurements.

After the achievement of breaking nanowires at room temperature, I focused on reducing the breaking time by optimizing the feedback electromigration process. For this purpose, I improved a Labview program to allow the parameters controlling the feedback breaking to be modified at will, and according to the real time measurements of the current obtained during the breaking process. As it was, the program basically increased the electric potential going through the nanowire and measures the current through it. When the current decreased by a certain amount, as the wire starts to break, the program would decrease the potential applied in order to prevent a total rupture of the nanowire in a single step. In order to improve this process, I introduced new steps in the program which will change the parameters of the breaking during the process, according to the absolute value of the current at any instant of time. Figure 24 is an example of the new feedback breaking process at room temperature, using the He_3 cryostat, with the new steps introduced in the program. The main objective of the code modifications is to achieve a controlled formation of the nanogaps in just a few minutes, versus the 30-40 minutes that the process used to take with the old algorithm. These new steps can be resumed as: a) New starting point, b) increase in the voltage increment, c) new breaking percentages and d) new recoil voltage.

a) New starting point: With the old program the electric voltage was swept from zero all the way up until the first breaking point. Now, the code starts with a finite initial voltage (#1 in Figure 24) which is close to the first breaking point (#2 in Figure 24). This saves a substantial amount of time *per se*. Usually, our nanowires start to break in the vicinity of 1 Volt. Consequently, we start the breaking of our wires at an initial voltage of ~0.8 Volts.

b) Increase in the voltage increment: This cannot be appreciated in the Figure 24, but the voltage increment has been increased from 0.001 V in the old program to 0.0025 V in the new one. This translates to a faster sweeping rate of the electric potential and results in a much shorter breaking process (a factor of 2 faster). However, the sweep rate cannot be increased without limit because high increments in voltage may suddenly break the wire, forming larger gaps.

c) New breaking percentages: The program manages the breaking amount by controlling how much decrease in current is allowed at the breaking points before recoiling. However, when the current is very low the same amount of decreased current is achieved sooner and making the breaking less efficient (the wire could be left to break more at low currents). In order to make the same amount of break for low currents a new breaking percentage is needed, which is another step that can be now controlled through the algorithm that I developed. Figure 24 shows this happening when the current decreases below 1.4 mA (#3), where a larger break is appreciable and the wire still does not break completely, making the process get faster and more efficient after that point.

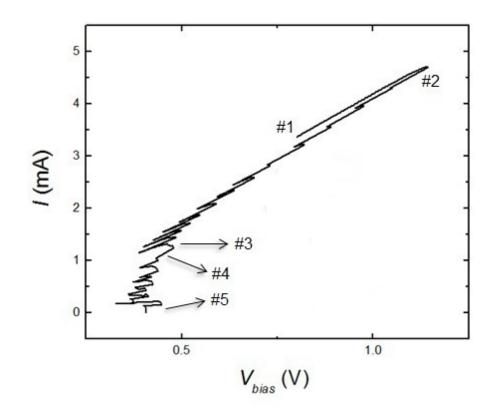


Figure 24: I-V graph of the feedback-controlled electromigration-induced breaking process at room temperature in the He₃ cryostat. #1 shows the point where the program started to apply electric potential. #2 is the first breaking point for the nanowire, where the voltage first recoils. In #3 the recoil voltage is increased. In #4 the breaking percentage is increased. Finally the program stops when it reaches 25 k Ω (#5), a resistance comparable to the one channel quantum resistance (25.8 k Ω).

d) New recoil voltage: As explained before, when the program sees the current decreasing by a given percentage from the previous point, it recoils the voltage back. The smaller the recoil voltage is, the faster it will arrive again to the next breaking point and the faster the process will be. However, if chosen too small the wire may break completely. The amount of recoil voltage needed depends on the absolute value of the current flowing through the wire at any given time. Therefore, I can include several steps at which the recoil voltage is changed according to the current reading. In Figure 24, a change in the recoil voltage from 0.1 Volts to 0.05 Volts is applied once the current has decreased below 1.3 mA (#4). The recoil reduces the voltage applied to a point in where it is not enough to break the wire, but it is very close

to it. Finally, when the resistance of the nanowire reaches a value close to the one channel transition resistance (25.8 k Ω) the program stops as is shown in #5 in Figure 24.

This new process was tested in around 200 nanowires at room temperature decreasing the breaking time down to 4 minutes in average. This is a huge improvement in the breaking process, although in every chip tested a few nanowires need to be scarified in order to optimize the parameters. As a result, the breaking time has been reduced by a factor of 10, from ~40 minutes to ~4 minutes, making possible to break the 40 nanowires in each of our chips in in less than 3 hours. Also, the liquid Helium consumption was completely eliminated by allowing the nanowires to complete the breaking process themselves with help of the surface tension of Au in nanowires that at the edge of the rupture. Most importantly, the breaking at room temperature becomes a fundamental advance of the technique since it allows the deposition of SMMs once the gaps are formed, as it will be explained in the following section. In fact, this new technique allows studying SET based on metallic nanoparticles (i.e. Au), since the particles can be deposited after the breaking process and will not be affected by it. It is known that Au nanoparticles deposited on top of nanowires melt during the breaking process.

In addition to the progress achieved in this chapter, I have built a nanowire breaking box in which I can break the nanowires without the need of using the He₃ cryostat. This breaking box allows me to break nanowires while the cryostat is used for other proposes of my lab and, most importantly, reduce the voltage necessary in order to produce the break. The breaking voltage is reduced since in the high resistance (~150 Ohms) of the cryostat wires, needed to reduce thermal transport into the sample, does not add to that of the nanowires (~80-100 Ohms). Reducing the voltage comes out to be another important factor in the breaking since it reduces the risk of sudden breaking of the nanowires and reduces the violence at which the break takes place. Figure 25 and Figure 26 are two examples of the new breaking process taking place in the new breaking box. Both Figures correspond to room temperature

electromigration breaking using the breaking box, however in the case of Figure 26 the wires were broken while the solution of molecules was present. The characteristic breaking control parameters (indicated by #1, #2, #3, #4, #5) explained before in this section are shown in both Figures 25 and 26. When comparing these to the breaking in the cryostat (Figure 24), one can clearly see that the breaking occurs at the same current (note that the current density to break the nanowire is imposed by its geometry and not by the external resistance of the circuit). This leads to a faster breaking of the wires, since less voltage needs to be applied. Moreover, the new parameters have been optimized in each case improving the breaking time down to $\sim 2 \min (i.e. an increase in the voltage increment and a new breaking percentage)$

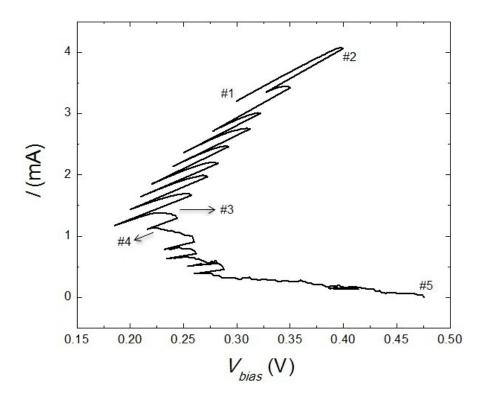


Figure 25: I-V graph of the feedback-controlled electromigration-induced breaking process at room temperature in the nanowire breaking box. #1 shows the point where the program started to apply electric potential. #2 is the first breaking point for the nanowire, where the voltage first recoils. In #3 the recoil voltage is increased. In #4 the breaking percentage is increased. Finally the program stops when it reaches 25 k Ω (#5), a resistance comparable to the one channel quantum resistance (25.8 k Ω).

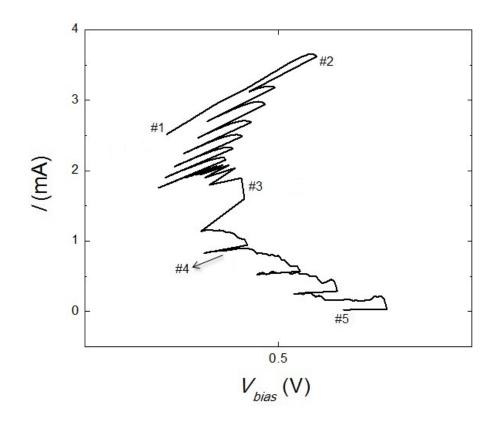


Figure 26: I-V graph of the feedback-controlled electromigration-induced breaking process at room temperature in the nanowire breaking box with the solution of molecules present during the process.

To conclude with this section, Figure 27 shows an SEM image of the final device out of the new fabrication process in where an overall view of the whole system can be appreciated. The Al gate is underneath of 5 broken nanowires which would act as source and drain electrodes if a SMM or any other nanoscale object is placed in the nanogap.

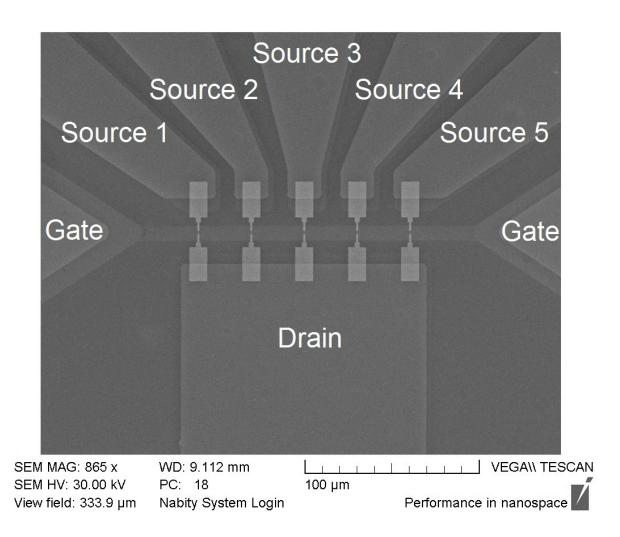


Figure 27: SEM image of a finished SET device. The gate component (Al 35nm) goes underneath of 5 nanowires (Au 17 nm) which have been broken with the improved electromigration process to form 1-3 nm gaps at the center (not appreciable at this scale).

Functionalization of SMMs

Since in 1996 Friedman and coworkers could see the quantum tunneling of the magnetization (QTM) in Mn_{12} [4], SMMs became a very interesting object of study. Their intrinsic bistability produced by the large spin and the uniaxial anisotropy barrier, and their behavior as nanoscale magnets which can reverse their magnetization by quantum tunneling are some of the physics properties that this quantum system can offer. The efforts of the chemists have been focused on functionalizing SMMs to modify their

intrinsic properties to form more interesting molecules from the physics point of view and more suitable for technological applications. Chemist can modify the core of the molecules with different ions and add different ligands to the molecules giving them different magnetic and physical properties. The ligands are usually organic components which can be functionalized and attached to the SMMs protecting them by means of decreasing its fragility and/or increasing its size. Functionalizing SMMs becomes particularly important when studying these molecules at the individual basis, out of their natural crystalline environment. For example, molecules can be functionalized to become more robust, which makes them easier to locate and to manipulate, becoming a clear advantage when considering their use in nanoscale devices. During my thesis research project, I have been working with Mn-based SMMs provided by George Christou at University of Florida. These SMMs have been designed to adequate to the SET experiments that we plan to do in the future. For example, they contain only magnese ions in their low oxidation state, i.e Mn^(III) and Mn^(IV), which are less likely to be reduced when in contact with other metals, such when deposited on the SET chips. They also show low-spin ground states that are well isolated from the first excited state, such that SET transitions can be easily associated to the lowest spin multiplet.

Although our interest in these molecules is driven by the expected SET behavior, within the framework of this thesis, the molecules have only been used to complete the development of our new SET spectroscopy, and to achieve an efficient deposition of the molecules into the nanogaps. Therefore, the remainder of this thesis discusses two Mn-based SMMs from the point of view of the technique, leaving their physics description to a basic description of the molecular system.

Mn_4

We first worked with $Mn_4O_3(OSiMe_3)(OAc)_3(dbm)_3$. This molecule has one $Mn^{(iv)}$ ion (spin 3/2) coupled antiferromagnetically with three $Mn^{(III)}$ ion (spin 2) coupled ferromagnetically with each other in a crystallographic C_3 symmetry giving the molecule a total ground spin state of S = 9/2 at low temperatures. Figure 28a and 28b show a schematic diagram of the Mn_4 molecule and the magnetic configuration of the molecular spins at low temperatures, respectively. The Mn4 molecule can be described by the giant-spin Hamiltonian given in Eqn. (1.14) with the uniaxial anisotropy characterized by the uniaxial anisotropy constant D = 0.72 K (0.062 meV) and the transverse anisotropy constant E = 0.033 K (2.86 µeV) [17, 18], which generate an anisotropy barrier separating opposite projection of the molecular spin (according to Figure 8).

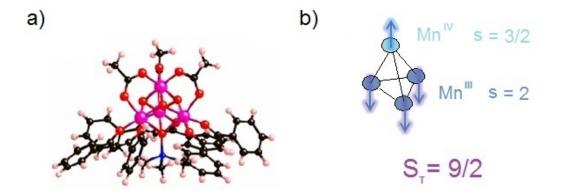


Figure 28: $Mn_4O_3(OSiMe_3)(OAc)_3(dbm)_3$ with total spin S = 9/2. Mn (purple), O (red), Si (blue), C (black), H (white). b) Schematic representation of the magnetic configuration of the molecule at low temperature. The $Mn^{(IV)}$ s = 3/2 couples with the three $Mn^{(III)}$ s = 2 antiferromagnetically, and the $Mn^{(III)}$ couple with each other ferromagnetically giving the molecule a total spin S = 9/2.

One of the characteristics for which this molecule was selected for SET measurements is that its ground spin state is well isolated from its first excited state, by an energy of $k_BT \sim 259$ K (22.3 meV) [19]. Having a big energy separation between the ground and first excited states guarantees that the ground state will not mix with the excited state even when high magnetic fields are applied, and

transitions within different multiples can be well identified, as well as transitions between different spin multiples. In addition, this molecule has been synthesized in order to increase its size and reduce the degradation time once the Mn_4 is deposited on metal surfaces. The total length of Mn_4 molecule is ~2 nm in diameter, which is appropriate when bringing the average gap size of our SETs.

For our experiments, the Mn_4 powder needs to be dissolved in a solution and then deposited by precipitation on our SETs chip. One problem that I encountered is that this system only dissolves in chloroform, and chloroform leaves molecular entities of approximately the same size of the SMMs deposited in the chips. Therefore, the Mn_4 is practically impossible to be distinguished in the deposition process from the chloroform molecules. Figure 29a shows and AFM image of an atomically flat layer of Au on Mica after 60 minutes of the deposition of Mn_4 molecules (0.15 mMol) in chloroform solution. Figure 29b is the same AFM analysis on another Au/Mica surface that has been leaved overnight in only a chloroform solution. This analysis revels that chloroform precipitates molecular entities of approximately the same size as Mn_4 molecule. In principle, these entities would also produce molecular transport characteristics and become indistinguishable from the Mn_4 in a SET experiment, so that we decided not to continue working with them.

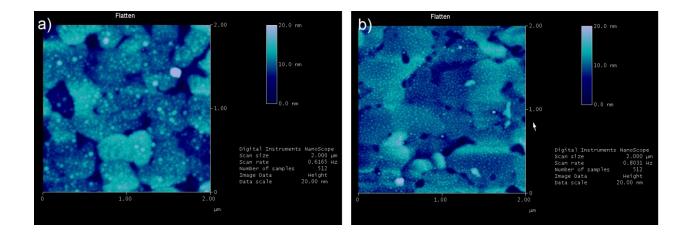


Figure 29: Mn_4 deposition (S = 9/2). a) AFM image after 60 minutes of deposition of Mn_4 molecules (0.15 mMol) dissolved in chloroform on top of a Au/Mica surface. b) AFM of a Au/Mica surface dipped in chloroform overnight, showing the precipitation of molecular entities everywhere.

Mn₃

Most recently, we started to work with Mn₃-benzoate, Mn₃O(C₆H₅COO)₃(mpko)₃]ClO₄. This molecule is composed of three Mn^(III) ions (spin 2) in a triangular shape. The mpko⁻ group (methylpyridinylketone oxime) distorts the triangular structure of the Mn₃ leading it to ferromagnetic super-exchange interactions between the three manganese ions, producing a total spin S = 6 at low temperatures. In Figure 30 there is an schematic diagram of the Mn₃ molecule and the schematic magnetic configuration of the molecule at low temperatures. In this molecule, the anisotropy constant is D = 0.49 K (0.042 mV) and the transverse anisotropy constant E = 0.0215 K (1.86 µeV). Also, the distortion in its triangular shape provides this Mn₃ molecule with two different values for the super-exchange interaction between the ions of J = 26.76 K (2.3 meV) and J² = 9.64 K (0.831 meV) [20]. In addition, the length of this molecule is ~1.4 nm in diameter, resulting from the chemical functionalization.

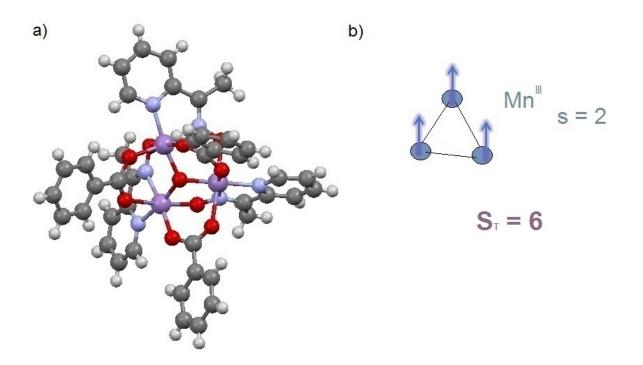


Figure 30: a) $Mn_3O(C_6H_5COO)_3(mpko)_3]CIO_4$. Mn (purple), O (red), N (blue), C (black), H (white). b) Schematic representation of the magnetic configuration of the molecule at low temperature. the $Mn^{(III)}$ ions s = 2 couple ferromagnetically giving the molecule a total spin S = 6.

Differently than with the Mn_4 molecule, the Mn_3 can be dissolved in acetonitrile and dichloromethane, which do not produce sizable residues in the device after deposition and added to its intrinsic properties make this molecule a good candidate for my measurements.

Optimization of the Deposition of SMMs in the Nanogaps

In this final section I present a new efficient method for depositing SMMs into the gaps of the SETs that I have fabricated following the steps of this thesis. This new deposition is achieved at room temperature and I hope it will lead to a substantial enhancement of the yield of the overall SET spectroscopy technique. First I explain the old deposition method reproduced by our group in the past and next the new one with the new advantages that it brings forth to the overall goal.

The goal of the old deposition method was to create a monolayer of SMMs covering completely the surface of SETs device in order to maximize the chances to get a molecule near to the place in the nanowire where the gap is formed, and hope that if falls into it without damage. For this, the chip with the nanowires, still unbroken, had to be immersed into a solvent solution where the molecules were dissolved previously. Note that with this method the feedback electromigration process had to be taken at low temperatures. The solution of molecules was prepared at a fixed dilution parameter, normally around 0.1 mMol, and different attempts depositing the molecules in atomically flat Au/Mika surfaces for different times had to be performed in order to optimize the formation of a monolayer. AFM analysis of the deposited surfaces was then employed to determine the best set of parameters, which were then used to deposit the molecules in the real SETs chips. This method led to several problems that have been mentioned before. Although this technique was very inconvenient and left very low yields (~1%) it was reproduced in most groups in the field, including our own [15].

The biggest advance in the new method is that it takes advantage of the new breaking process explained in step 5) where the nanowires are broken at room temperature. As a consequence, the deposition of the molecules can take place once the gap in already created, contrary to the old method. Moreover, in this new deposition method it is possible to recognize when a molecule has entered into the gap bridging the source and drain electrodes by means of controlling the resistance of the broken nanowire during deposition. As explained above, in the new breaking process the nanowire is first broken until 26 k Ω resistance is reached. The surface tension of Au does the rest, opening the nanogap and raising the resistance to the G Ω range. Once this is achieved in all nanowires of a chip (i.e. 40), the solvent solution with the molecules already dissolved is deposited on top of the chip (i.e. without immersing the chip in the solution), using a flow regulated pipette that allows to maintain the surface of the chip always covered with enough liquid during the deposition. With this method, higher molecular concentrations can be used. In our case we use a ~0.2 mMol concentration. The deposition of the

molecules is prolonged for 2 hours, after which the chip is blown dry and the resistances of all the gaps are checked. If a molecule has entered the gap a drop on the resistance down to $k\Omega$ -M Ω is appreciated. When this is seen for a number of transistors, then the chip is placed in the cryostat for further low temperature experiments.

This new method is a great advance in the deposition technique for three main reasons: a) the cryostat is introduced into liquid He only when the resistance of a good number of broken nanowires has decreased due to the likely presence of a molecule in the gap, guaranteeing molecular SET measurements at low temperature in several nanowires on each run. This, aside of substantially minimizing the liquid He consumption greatly increases the yield of the technique, from ~1% to at least ~15%, i.e. at least 6 working SETs out of the 40 on each chip. b) The chip is completely ready for measurements when the molecule solution is deposited on it, meaning that once the dropping in resistance is noticed the sample can go for low temperature measurements. This avoids possible degradation of the molecules at ambient conditions. c) This method totally avoids the potential damaging effect of strong local electric fields achieved at the breaking point of the nanowire, allowing working with a variety of nanoscale systems, such as molecular magnets or metallic nanoparticles.

CHAPTER THREE: CONCLUSION

In this thesis I have presented the advances achieved in the development of a more efficient molecular single-electron transport spectroscopy by means of improvements in the fabrication of SETs and the optimization in the deposition of SMMs on top of them.

In the fabrication process I illustrated all the advances obtained in every single step, increasing the overall SET spectroscopy technique yield. Dividing the fabrication process down to 5 steps I achieved to: a) Reduce the overall resistance of our circuit and facilitate a better lift off process; b) increase the functional gate component yield up to >90% with an homogenous superficial oxide layer serving as the insulating layer between the molecule and the gate. The latter while maintain thin nanowires for breaking at low currents and bias voltages; and, c) reduce the time needed to form the nanogap the nanowires by a factor of 10 in a new electromigration process at room temperature.

In parallel, we have advanced in identifying properly functionalized SMMs from both physical and magnetic points of view and for their use in SET experiments. In particular, I have presented studies of manipulation and deposition of Mn_4 and Mn_3 -benzoate molecules which show adequate characteristics for our final goals, including a large total spin ground state, well isolated from the first excited state, and a robust mechanical structure for manipulation out of their natural crystalline environment.

Finally, I described a new SMM deposition process at room temperature which avoid degradation of the molecules and increase the deposition yield substantially, at the time of saving time and money with no need of cryogenics during the preparation of the SET samples.

The results exhibited through this thesis provide an optimistic base ground for upcoming studies of the interesting quantum properties of SMMs, such as quantum tunneling of the magnetization and the Berry phase interference, by means of single-electron transport experiments, which until now have been difficult to achieve. Indeed, the new technique will allow transport studies in other nanoscale systems, such as metallic nanoparticles. I expect exciting results coming soon from the new optimized SETs that we are now able to fabricate at the University of Central Florida, combined with the new molecules synthesized by our collaborator at University of Florida. It is my intention to present a dissertation proposal in the Summer 2013 to undertake such studies in the immediate future.

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