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Design, Modeling, And Control Of Three-port Converters For Solar Power Applications

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DESIGN, MODELING, AND CONTROL OF THREE-PORT CONVERTERS FOR SOLAR POWER APPLICATIONS

by

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ABSTRACT

This paper describes the results of research into multi-port converter design and control, specifically a pair of three-port topologies based on the half-bridge and full-bridge topologies. These converters are capable of simultaneous and independent regulation of two out of their three ports, while the third port provides the power balance in the system. A dynamic model was developed for each topology to aid in testing and for designing the control loops. The models were then used to design the control structures, and the results were tested in Simulink. In addition, a basic outline of a system level architecture to control multiple converters working in parallel is presented. To improve the reliability of this system, output current sharing controls were also developed. Finally, one of the topologies is analyzed in detail in order to obtain a set of design equations that can be used to improve the efficiency, weight, and cost of the converter for a specific application.

ACKNOWLEDGMENTS

Thank you to my committee members, Dr. Batarseh, Dr. Shen, and Dr. Klee. Without your support this project would not have been possible.

Thank you also to all of the guys from the SURGE lab of the Florida Power Electronics Center (FPEC), especially Hussam Al-Atrash who supported me throughout the entire process.

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CHAPTER I: INTRODUCTION

With the increasing interest in renewable energy sources, the need for an efficient and cost effective solar power conversion system is greater than ever. The subject of this thesis is a pair of newly developed three-port converter topologies developed by UCF's Florida Power Electronics Center (FPEC) [34,35]. Their purpose is the interfacing of three separate devices, namely a solar array, a storage battery, and the load. With the addition of a storage device to the system, maximum power point tracking can be performed on the solar panel with simultaneous regulation of the load, while the storage device provides the power balance to the system. Normally this amount of regulation requires multiple dual-port converters to interface each of the power flow paths. However, a three-port converter can interface all three devices with a single device, providing significant savings in efficiency and component count, which translates to reductions in cost, space, and weight. Research and development for this project was funded by NASA through their SBIR program, so much of the work was done targeting eventual space applications. However, most of the results can be generalized to apply to any application using solar power.

Two different three-port topologies were developed based on the popular phase-shift full-bridge and duty-cycle shifted half-bridge topologies. Both topologies were modified to allow for the addition of a third port where the storage device would be connected. Figure 1 and Figure 2 below show diagrams of both topologies.

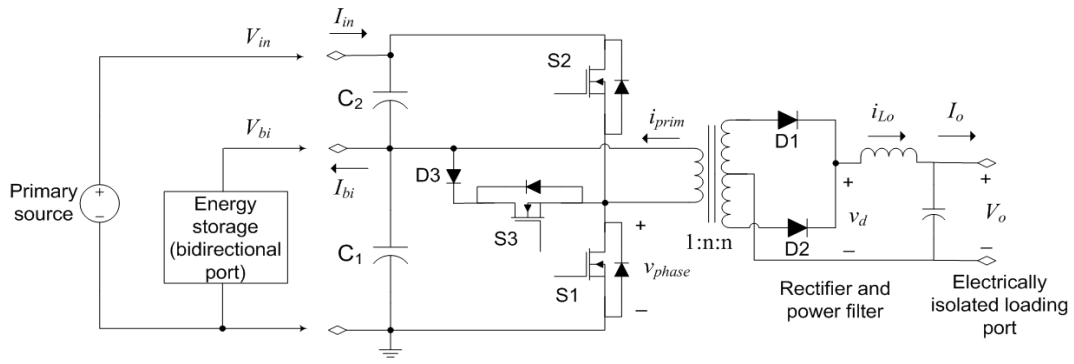

Figure 1: Tri-Modal Half-Bridge Topology

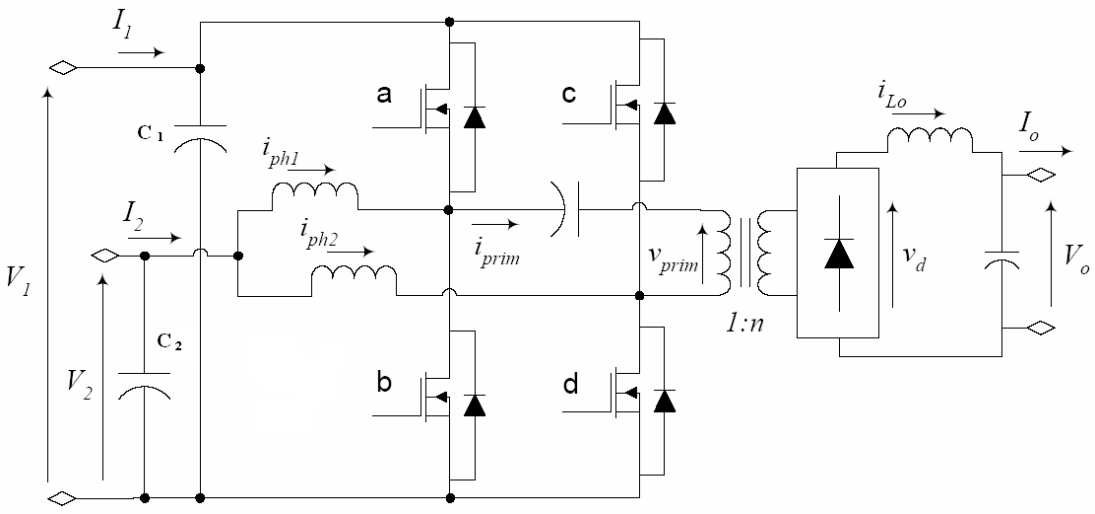

Figure 2: Boost-Integrated Phase-Shift Full-Bridge Topology

Figure 1 illustrates the half-bridge derived topology, hereafter called the tri-modal half-bridge (TM-HB) topology. Figure 2 illustrates the full-bridge derived topology, hereafter called the boost-integrated phase-shift full-bridge (BI-PS-FB) topology. Both topologies are capable of three port operation and simultaneous control of two of the three ports. In the case of the half-bridge converter, since fewer switches are used, there are cost advantages, but only for lower power levels. As the power levels increase, the added benefit of double the voltage gain in a

full-bridge topology and lower losses serve to mitigate the added costs of the additional switching leg. This comparison also holds true for the three port topologies that have been created. Generally the BI-PS-FB topology is better for use in high power applications, while the TM-HB topology is better for low power applications.

Stable system operation requires the maintenance of power balance in the system. That is, in steady-state, the sum of average input power to the converter is required to equal the sum of average output power plus any power losses. This implies that, for a three-port system, the operating point of up to two ports can be tightly regulated, while the third port should be kept "flexible" and would operate at any point that satisfies the power balance constraints. The choice of the flexible power port dictates the feedback control layout. This choice can be fixed, or may dynamically vary with the operating conditions. Both of the topologies can operate in one of three different modes, depending on which of the three ports are being regulated:

1. Battery-balanced operation: the load voltage is tightly regulated, and the solar array is run under MPPT control. In this case, the battery preserves the power balance in the system by storing unconsumed solar power, or providing the deficit during high load intervals.

2. Battery-charge regulation operation: the load is regulated and sinks less power than is available, while the battery charge rate is limited. In this case, the battery current or voltage is regulated, while the solar array is forced to operate in its voltage-source region where it provides less power than it has available.

3. Flexible load operation: the battery charge is regulated, and MPPT controls the solar arrays. This mode is active when the load is able to sink a variable amount of power, while the battery charge rate is limited. This is useful for a grid-tied inverter system.

For the targeted space applications, modes 1 and 2 were concentrated on since load regulation is too important to be left uncontrolled as in mode 3. A top-level system architecture was developed to take advantage of both modes 1 and 2, being able to switch between them as conditions such as battery charge level and light level change. Also, a mathematical model was developed for both modes of each topology, and a basic feedback control scheme was developed using the models. Finally, a series of design equations were developed for the TM-HB topology. The reason for concentrating more strongly on the TM-HB topology in terms of analysis is because other members of the team for this project had already finished the analysis for the BI-PS-FB topology.

CHAPTER II: LITERATURE REVIEW

There has already been a limited amount of study into the idea of multi-port converters. One common method is the use of multiple secondary transformer windings and their associated rectifiers in isolated topologies to provide power to multiple loads at different voltage levels [21]. However, precise regulation of multiple outputs is limited by the amount of available control variables. The use of elaborate control schemes such as simultaneous variation of duty cycle and switching frequency provide this capability, but only for a narrow operating range [17,22].

Other new ideas for multi-port converters have been proposed, such as the multi-input buck [23] and multi-input flyback [24]. Furthermore, isolated multi-input [25], and possibly multi-output [26], configurations are achievable through magnetic coupling to a common flyback transformer. An important part of these topologies is that they can perform independent regulation over a maximum of one output, as long as regulation over one of the inputs is dropped. The main problem with these configurations is the lack of a bi-directional port for power storage.

Some recent publications have focused on load-side control through the utilization of a half-bridge structure magnetically coupled to the source chopper [27, 28]. Still others have preferred the use of multiple converters with centralized control to allow bi-directional power flow [29]. Several publications have proposed the integration of a biphase boost into a full-bridge converter, in order to achieve single-stage power factor correction [30-33]. One method of control that was proposed is simultaneous variation of duty-cycle and phase shift [33] to allow input current shaping, while constraining the amount of energy storage in the bulk capacitor.

However, its application to power factor correction introduced a number of problems that keep the topology from being too useful. There are no such problems in the multi-port dc-dc converters that will be discussed in this thesis.

CHAPTER III: CONVERTER MODELING

The purpose of creating a mathematical model for any topology is to provide an easy means of simulating and analyzing a complex circuit. It is further used to derive the small-signal dynamic characteristics, required for proper design of feedback regulation loops. A pair of models was developed for both the TM-HB and the BI-PS-FB topologies corresponding to the battery-balanced mode and the battery-charge regulation mode. In the battery-balanced mode the solar input voltage is regulated using a MPPT algorithm, while the output voltage is regulated to a certain value. The battery port provides the power balance to the system, either sinking power during periods when the input is providing excess, or sourcing power during periods when the input is insufficient. This mode is useful when the battery does not need regulation so that MPPT can be run on the input in order to extract maximum power. In battery-charge regulation mode the output voltage is again kept tightly regulated, and the voltage or current of the battery is also regulated in order to control the battery charge rate. Meanwhile the input voltage is left unregulated to run at less than maximum power. This mode is useful when battery charge regulation is needed in order to optimize battery usage and extend it lifetime. It is important that in both modes the output remains tightly regulated so that the load remains operational at all times.

Modeling the Tri-Modal Half-Bridge

Creating a mathematical model for a circuit requires finding a series of equations that approximate the operation of the circuit at all ranges of component values and frequencies. To start with, the steady-state equations for each mode were developed. Assuming an ideal lossless converter, the steady-state relations between different port voltages can be determined by

equating the voltage-second product across the converter's two main inductors to zero. First, using the volt-second balance across the magnetizing inductance of the transformer when operating in continuous conduction mode (CCM) we have:

$$-\left(D_1 T\right)\cdot V_{C1}+\left(D_2 T\right)\cdot V_{C2}=0$$

With $V_{in}=V_{C1}+V_{C2}$, and $V_{bi}=V_{C1}$, the voltage at the bidirectional port, V_{bi}, may be given by:

$$V_{bi}=\frac{D_2}{D_1+D_2}V_{in}$$

Where V_{in} is the voltage of the main input source, D_1 and D_2 are the duty cycles of S1 and S2, respectively, and T is the duration of the switching cycle. Assuming CCM operation, the volt-second balance across the load filter inductor yields:

$$D_1\cdot T\cdot\left(n\cdot V_{C1}-V_o\right)+D_2\cdot T\left(n\cdot V_{C2}-V_o\right)-\left(1-D_1-D_2\right)\cdot T\cdot V_o=0$$

$$V_o=D_1\cdot n\cdot V_{C1}+D_2\cdot n\cdot V_{C2}=2\frac{D_1\cdot D_2}{D_1+D_2}n\cdot V_{in}$$

Where n is the turns ratio of the transformer. Assuming a lossless converter, steady-state port currents can be related by applying the power conservation principle as follows:

$$V_{in}\cdot I_{in}=V_{bi}\cdot I_{bi}+V_o\cdot I_o$$

Where I_{in}, I_{bi}, I_o are the average input, bidirectional, and load currents, respectively, and V_o is the load-port voltage.

A dc current flows in the transformer primary winding. It is important to note that this dc current is not associated with any dc voltage. The magnetizing inductance of the transformer is used to

store energy to interface the input and bidirectional ports. The transformer design needs to allow for this dc current flow and becomes similar to an inductor or a flyback transformer design. The average magnetizing current, I_{Lm}, reflected to the primary side satisfies:

$$I_{bi} = D_1 \cdot \left(I_{Lm} - n \cdot I_o \right) + D_2 \cdot \left(I_{Lm} + n \cdot I_o \right)$$

Rearranging:

$$I_{Lm} = \frac{I_{bi} + \left(D_1 - D_2 \right) \cdot n \cdot I_o}{D_1 + D_2}$$

The above equations assume the circuit is in battery-charge regulation mode. If the circuit were in battery-balanced mode, the input and output equations can be rearranged to be:

$$V_{in} = \frac{D_1 + D_2}{D_2} V_{bi}$$

$$V_o = 2 \cdot D_1 \cdot n \cdot V_{bi}$$

Averaged Model of the TM-HB during Battery-Balanced Mode

Since the frequency response of the TM-HB is non-linear, the equations must be linearized around an operating point. A model such as this is called a small-signal model or an averaged model. First, state equations for each energy storage element were developed. These include the input capacitor C_2, the magnetizing inductance L_m, the output inductance L_o, and the output capacitance C_o. Linearizing and converting each equation to the frequency domain gives the following equations:

$$s \cdot v_{C2}(s) = \frac{-v_{C2}(s)}{C_2 \cdot R_s} - \frac{D_2 \cdot \left(n \cdot i_{Lo}(s) + i_{Lm}(s)\right)}{C_2} - \frac{d_2(s) \cdot \left(n \cdot I_{Lo} + I_{Lm}\right)}{C_2}$$

$$s \cdot i_{Lm}(s) = \frac{D_2 \cdot v_{C2}(s) + d_2(s) \cdot V_{C2} - d_1(s) \cdot V_{batt}}{L_m}$$

$$s \cdot i_{Lo}(s) = \frac{n \cdot \left(D_2 \cdot v_{C2}(s) + d_2(s) \cdot V_{C2} + d_1(s) \cdot V_{batt}\right)}{L_o} - \frac{V_o(s)}{L_o}$$

$$s \cdot v_o(s) = \frac{i_{Lo}(s)}{C_o} - \frac{V_o(s)}{C_o \cdot R}$$

Solving for the transfer functions is tedious and ultimately reveals little. Alternatively, the system can be represented in matrix form using a state-space model. The state-space model takes the following form:

$$\frac{dX}{dt} = A \cdot X + B \cdot U$$

$$Y = C \cdot X + D \cdot U$$

Where X is a matrix containing the state variables V_{C2}, I_{Lm}, I_{Lo}, and V_o, U is a matrix containing the system inputs D_1 and D_2, and Y is a matrix containing the system outputs. For this model the four state variables are also the system outputs, so the second equation simplifies to

$$Y = I \cdot X$$

Where I is the identity matrix. Filling in the A and B matrices using the state equations gives:

$$A = \begin{bmatrix} -\frac{1}{R_s C_2} & -\frac{D_2}{C_2} & -\frac{nD_2}{C_2} & 0 \\ \frac{D_2}{L_m} & 0 & 0 & 0 \\ \frac{nD_2}{L_o} & 0 & 0 & -\frac{1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \qquad B = \begin{bmatrix} 0 & -\left(I_{Lm} + nV_o/R\right) \\ -\frac{V_2}{L_m} & \frac{D_1 V_2}{D_2 L_m} \\ \frac{nV_2}{L_o} & \frac{nD_1 V_2}{D_2 L_o} \\ 0 & 0 \end{bmatrix}$$

To test the validity of the mode 1 state-space averaged model, Matlab's Simulink was used to compare the outputs of the model to the actual circuit operation. The circuit was simulated using PLECS and a small-signal perturbation in the form of a small sinusoidal signal was added to one of the duty cycles. The result was then compared to the output of the state-space model. This simulation setup can be seen in Figure 3. This same basic setup was used for all of the simulations in this chapter.

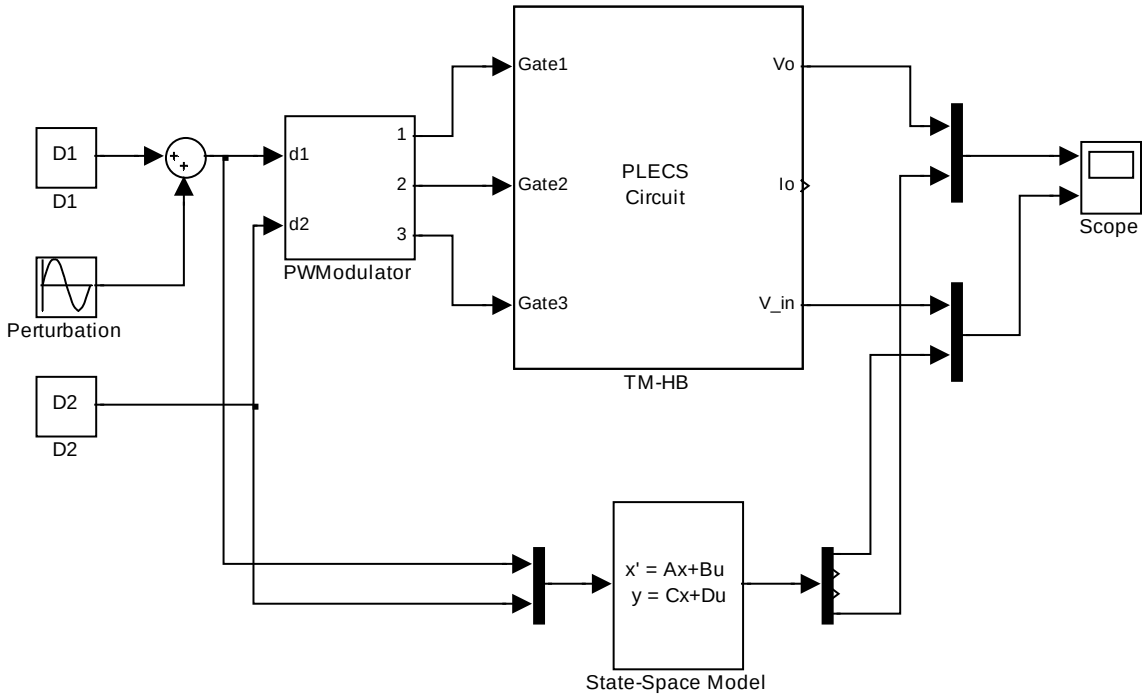

Figure 3: Simulink simulation setup

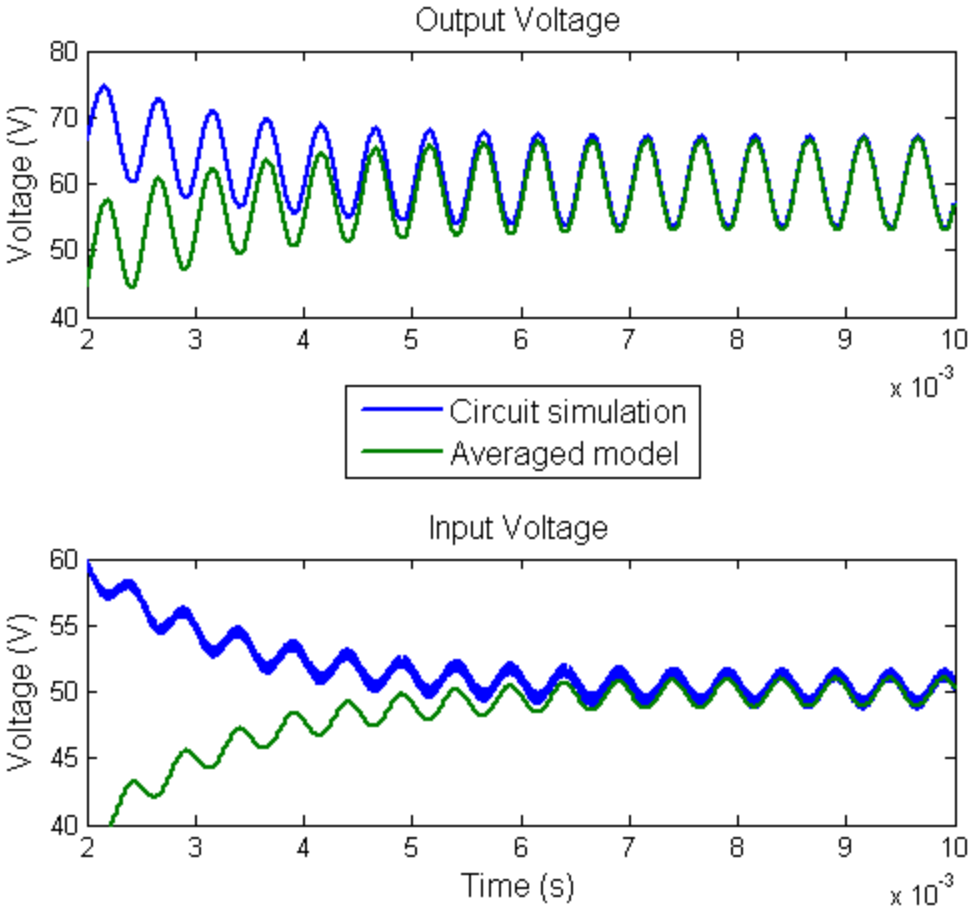

Figure 4: TM-HB mode 1 averaged model simulation

It can be seen that the averaged model correctly approximates the input and output voltages.

Averaged Model of the TM-HB during Battery-Charge Regulation Mode

Next an averaged model for mode 2 (battery-charge regulation mode) operation of the TM-HB was developed. In this case the bi-directional capacitor C_2 was included instead of the input capacitor C_1. The frequency domain state equations for this mode after linearization are:

$$s \cdot v_{C1}(s) = \frac{-v_{C1}(s)}{R_b \cdot C_1} + \frac{i_{Lm}(s) \cdot (D_1 + D_2)}{2 \cdot C_1} + \frac{v_o(s) \cdot n \cdot (D_2 - D_1)}{R \cdot C_1} + \frac{ILm(d_1(s) + d_2(s))}{C_1} + \frac{n \cdot V_o \cdot (d_2(s) - d_1(s))}{R \cdot C_1}$$

$$s \cdot i_{Lm}(s) = \frac{-v_{C1}(s) \cdot (D_1 + D_2)}{L_m} - \frac{(d_1(s) + d_2(s)) \cdot D_2 \cdot V_1}{(D_1 + D_2) \cdot L_m} + d_2(s) \cdot V_1$$

$$s \cdot i_{Lo}(s) = \frac{v_{C1}(s) \cdot n \cdot (D_1 - D_2)}{L_o} - \frac{v_o(s)}{L_o} + \frac{(d_1(s) - d_2(s)) \cdot n \cdot D_2 \cdot V_1}{L_o \cdot (D_1 + D_2)} + \frac{d_2(s) \cdot n \cdot V_1}{L_o}$$

$$s \cdot v_o(s) = \frac{i_{Lo}(s)}{C_o} - \frac{v_o(s)}{R \cdot C_o}$$

A state-space representation was created in the same way as with mode 1. The state matrix X contains the four state variables V_{C1}, I_{Lm}, I_{Lo}, and V_o and the input matrix U contains the two control variables D_1 and D_2. The A and B matrices take the following form:

$$A = \begin{bmatrix} -\frac{1}{R_b C_1} & \frac{(D_1 + D_2)}{2C_1} & 0 & -\frac{n(D_2 - D_1)}{RC_1} \\ -\frac{(D_1 + D_2)}{L_m} & 0 & 0 & 0 \\ \frac{n(D_1 - D_2)}{L_o} & 0 & 0 & -\frac{1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix}$$

$$B = \begin{bmatrix} \dfrac{I_{Lm} - nV_o/R}{C_1} & \dfrac{I_{Lm} + nV_o/R}{C_1} \\ -\dfrac{D_2 V_1}{(D_1 + D_2) L_m} & \dfrac{D_1 V_1}{(D_1 + D_2) L_m} \\ \dfrac{nD_2 V_1}{(D_1 + D_2) L_o} & \dfrac{nD_1 V_1}{(D_1 + D_2) L_o} \\ 0 & 0 \end{bmatrix}$$

The mode 2 state-space model was also tested in Simulink.

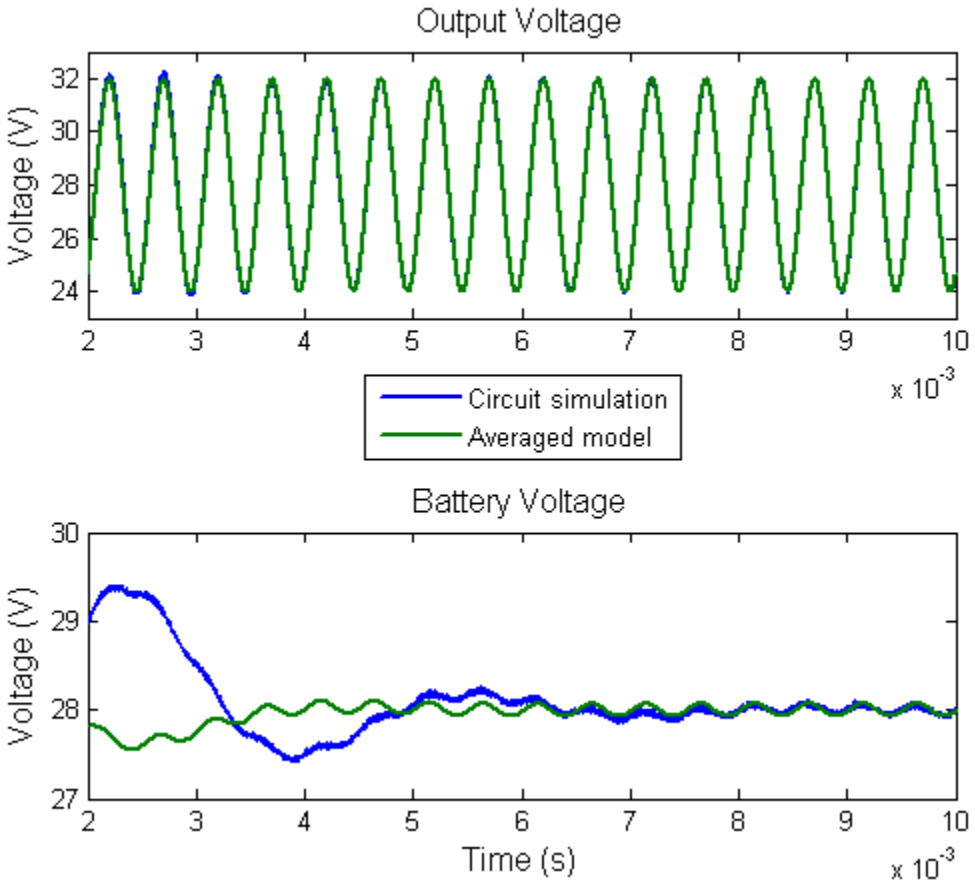

Figure 5: TM-HB mode 2 averaged model simulation

It can be seen once again that the averaged model correctly approximates the output voltage and battery voltage.

Modeling the Boost-Integrated Phase-Shift Full-Bridge

A model was constructed for each mode of operation of the BI-PS-FB topology as well. Steady-state analysis results are presented here for an ideal loss-less converter operating in continuous conduction mode (CCM). Considering volt-second balance across the boost inductors:

$$D \cdot T_s \cdot (V_1 - V_2) - (1 - D) \cdot T_s \cdot V_2 = 0$$

$$V_2 = D \cdot V_1$$

Where V_1, V_2 are the voltages at ports 1 and 2, respectively, D is the duty-cycle of each phase-leg, and T_s is the duration of a switching cycle.

It is notable that this applies to both boost inductors, indicating that the duty-cycle of the two phase-legs is required to be equal to ensure proper operation of the converter. In a practical circuit, small mismatches between the two duty-cycles will produce an imbalance between the currents in the boost inductors. This imbalance is only limited by the parasitic resistances in the current paths. If this resistance is not enough to limit the imbalance to a tolerable value, current-sharing control can be used to enhance the current balance. Considering volt-second balance across the output filter inductor:

$$2 \cdot \Phi_{eff} \cdot T_s \cdot (n \cdot V_1 - V_o) - (1 - 2 \cdot \Phi_{eff}) \cdot T_s \cdot V_o = 0$$

$$V_o = 2 \cdot \Phi_{eff} \cdot n \cdot V_1$$

Where n is the transformer turns' ratio, V_o is the load voltage. Φ_{eff} is the effective value of the phase-shift between the two switching phase-legs. It is related to the phase-leg duty-cycles and the relative phase-shift, Φ, by:

$$\Phi_{eff} = \min(\Phi, D, 1-D)$$

Note that Φ and Φ_{eff} are expressed as dimensionless values in the range [0, 0.5], corresponding to radian phase-shift values [0 , π], or absolute time-shift values of [0 , $T_s/2$].

The load current is reflected to the primary side during power delivery periods, and is held during free-wheeling periods by the transformer leakage inductance. Due to the presence of a dc-blocking capacitor, a limited dc magnetizing current is born that opposes any dc component resulting from the reflected load current. This can be quantified by considering amp-second balance through the dc-blocking capacitor:

$$D \cdot T_s \cdot \left(I_{Lm} - n \cdot I_o\right) + \left(1-D\right) \cdot T_s \cdot \left(I_{Lm} + n \cdot I_o\right) = 0$$

$$I_{Lm} = \left(2 \cdot D - 1\right) \cdot n \cdot I_o$$

Where I_o is the load current, and I_{Lm} is the dc magnetizing transformer current as seen on the primary winding. This dc magnetizing current is small, and is naturally eliminated at 50% duty. The current through either one of the boost inductors is:

$$I_{Bst} = \frac{2 \cdot I_o \cdot \Phi_{eff} \cdot n - I_s}{2 \cdot D}$$

The above equations assume the circuit is in battery-charge regulation mode. If the circuit were in battery-balanced mode, the input and output voltage equations could be rearranged to be:

$$V_1 = \frac{V_2}{D}$$

$$V_o = \frac{2 \cdot \Phi_{eff} \cdot n \cdot V_2}{D}$$

Averaged Model of the BI-PS-FB during Battery Balanced Mode

First, state equations for each energy storage element were developed. These include the input capacitor C_1, the two boost inductors L_{bst1} and L_{bst2}, the output inductor L_o, and the output capacitor C_o. Since in a lossless converter the current through the boost inductors should be equal, only one state equation is needed to represent the boost inductor current. Linearizing and converting each equation to the frequency domain gives the following equations:

$$v_{C1}(s) = \frac{-v_{C1}(s)}{R_s C_1} - \frac{2 \cdot n}{R \cdot C_1}\left(\Phi \cdot v_o(s) + V_o \cdot \Phi(s)\right) + \frac{2}{C1}\left(D \cdot i_{LB}(s) + I_{LB} \cdot d(s)\right)$$

$$i_{LB}(s) = \frac{V_{C1} \cdot d(s) - D \cdot v_{C1}(s)}{L_{Bst}}$$

$$i_{Lo}(s) = \frac{n}{L_o}\left(\Phi \cdot v_{C1}(s) + V_{C1} \cdot \Phi(s)\right) - \frac{v_o(s)}{L_o}$$

$$v_o(s) = \frac{2 \cdot i_{Lo}(s)}{C_o} - \frac{v_o(s)}{R \cdot C_o}$$

The next step is converting the state equations into a state-space representation of the form:

$$\frac{dX}{dt} = A \cdot X + B \cdot U$$

$$Y = C \cdot X + D \cdot U$$

Where X is a matrix containing the state variables, U is a matrix containing the system inputs D and Φ, and Y is a matrix containing the system outputs. As in the case with the TM-HB topology, the system outputs of the state-space representation are equivalent to the state variables themselves, so that the output equation can be simplified to:

$$Y = I \cdot X$$

Where I is the identity matrix. Filling in the A and B matrices using the state equations gives:

$$A = \begin{bmatrix} -\frac{1}{R_s C_1} & \frac{2D}{C_1} & 0 & -\frac{2n\Phi}{RC_1} \\ -\frac{D}{L_b} & 0 & 0 & 0 \\ \frac{n\Phi}{L_o} & 0 & 0 & -\frac{1}{L_o} \\ 0 & 0 & \frac{2}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \quad B = \begin{bmatrix} -\frac{2nV_o}{RC_1} & \frac{2I_{Lb}}{C_1} \\ 0 & \frac{V_2}{DL_b} \\ \frac{nV_2}{DL_o} & 0 \\ 0 & 0 \end{bmatrix}$$

To test the validity of the mode 1 state-space averaged model, Matlab's Simulink was used to compare the outputs of the model to the actual circuit operation. The circuit was simulated using PLECS and a small-signal perturbation in the form of a small sinusoidal signal was added to the phase shift Φ.

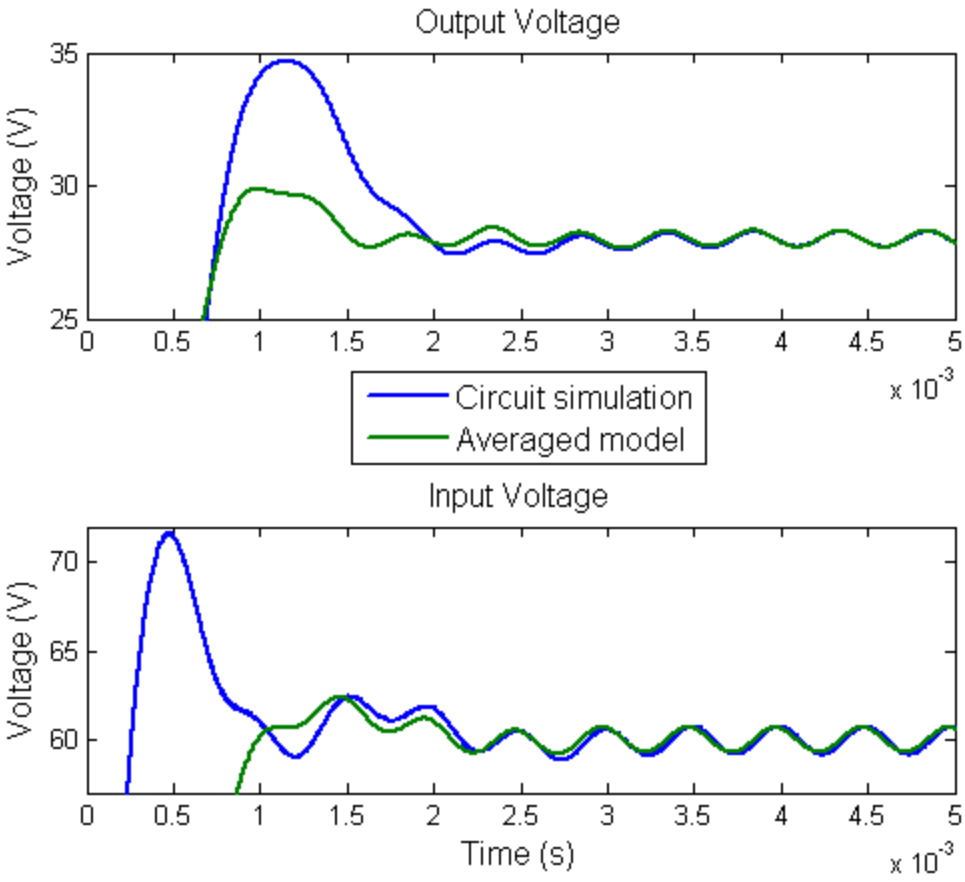

Figure 6: BI-PS-FB mode 1 averaged model simulation

It can be seen that the averaged model correctly approximates the input and output voltages.

Averaged Model of the BI-PS-FB during Battery-Charge Regulation Mode

Next an averaged model for mode 2 operation of the BI-PS-FB was developed. In this case the bi-directional capacitor C_2 was included instead of the input capacitor C_1. This mode is unique in that the input and output voltage equations are entirely independent of each other. This greatly simplifies the transfer functions of the system. It is interesting that these transfer functions are typical of a buck converter operating in CCM. The controller design thus follows the typical design procedures of a voltage-mode buck.

$$\frac{v_o(s)}{\Phi(s)} = \frac{2 \cdot n \cdot V_1}{s^2 \cdot C_o \cdot L_o + s \cdot \frac{L_o}{R} + 1}$$

$$\frac{v_2(s)}{D(s)} = \frac{V_1}{s^2 \cdot C_2 \cdot L_{bst} + s \cdot \frac{L_{bst}}{R_b} + 1}$$

Where L_{bst} is the parallel combination of the two boost inductors. The mode 2 model was also tested in Simulink. A small sinusoidal perturbation was added to the phase shift Φ to simulate a small-signal disturbance.

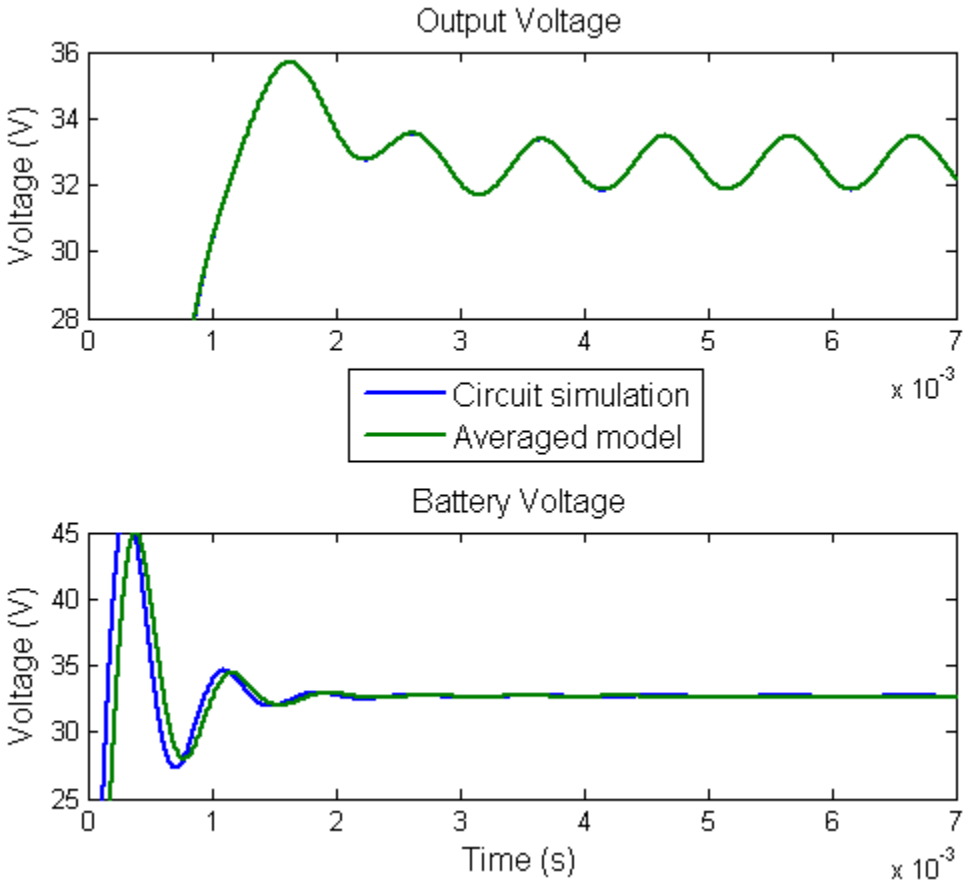

Figure 7: BI-PS-FB mode 2 averaged model simulation

It can be seen once again that the averaged model correctly approximates the battery voltage and output voltage. As expected, the perturbation to Φ has no effect on the battery voltage since it only depends on the duty cycle.

CHAPTER IV: CONTROL AND MODULARITY

It is important for any power processing device to remain under tight control during various kinds of operating conditions. To this end, an overall system architecture was designed with the goal of overseeing many converters working together in parallel. Secondly, a feedback control structure was developed for each operating mode of the two converter topologies. Finally, in order to extend system lifetime and reduce component stress, it is important to make sure that each converter in the system is sharing power equally. To ensure this an output current sharing scheme was developed.

Modular Architecture

The basic outline of the planned modular system architecture was designed and is pictured in Figure 8. The basic system block is a solar channel. Each channel is configured to process power of an individual solar panel. Within that channel, a number of three-port converters are paralleled at all three ports to match the power rating of the corresponding solar panel. A solar group consists of several independently-sourced solar channels whose storage (bidirectional) ports are paralleled and connected to a common battery bank. The output ports of all solar groups are paralleled and connected to a common distribution bus. This system configuration capitalizes on the flexibility of three-port converters. In addition to enhanced efficiency and power density, this configuration offers the following advantages:

1. Standardized building blocks are used to construct scalable power systems. Different panel sizes are accommodated by paralleling several converters within a single channel.

Total system power is expandable by paralleling a larger number of channels within the system.

2. Interfacing a dedicated channel to each solar panel allows it to have an independent MPPT process. The maximization of power output from individual panels is superior to that from a series or parallel combination of those same panels. Ageing, damage, or shading of one or several panels does not affect the operation of others.
3. The utilization of several battery banks with independent charge and discharge control is a very powerful approach. It allows the utilization of banks of different chemistries, voltages, sizes, and age. It further allows the periodic isolation of these battery banks for reconditioning without requiring complete system shutdown.
4. The system architecture is naturally suitable for building N+1 redundancy. This means that there is at least one more converter in the system than is necessary, so that if there is a converter failure it will not affect the system operation.

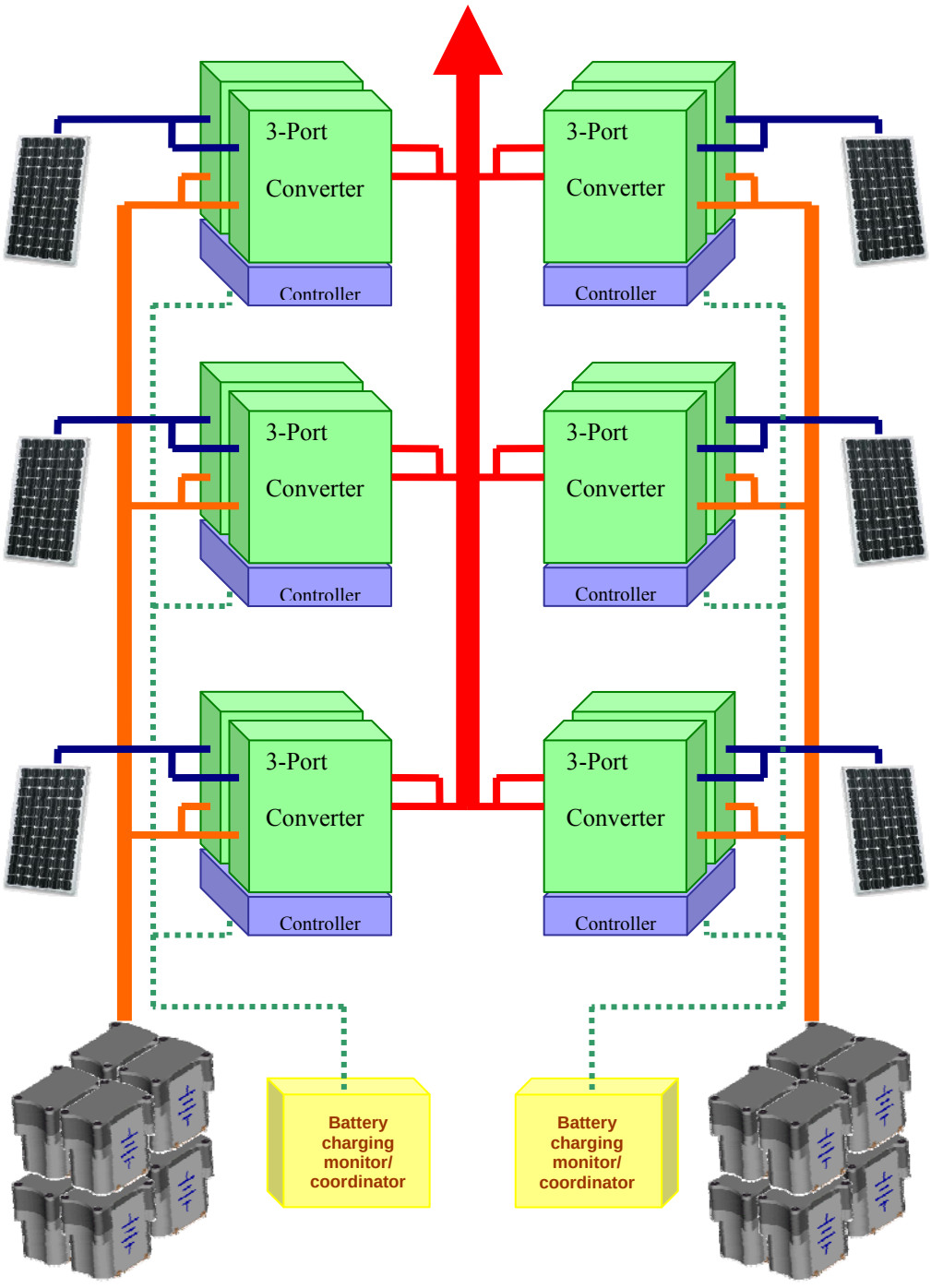

Figure 8: Modular Architecture

Feedback Control Structure

Designing the feedback control structure for a multi-port system is significantly more complex than designing for a traditional two-port system. However, the same control design techniques can be used with some modifications. The control structures for the two three-port topologies were designed based on the averaged models presented in chapter 3. Using the models, transfer functions for both output and input voltage can be extracted using the following equation:

$$G = \left(s \cdot I - A\right)^{-1} \cdot B$$

The G matrix contains transfer functions for each of the state variables in response to the two control variables. While the functions themselves are too long to present here, they can be used to plot the magnitude and phase of the frequency response which is then used to design the feedback control structures for the converters.

TM-HB Battery Balanced Mode Control Structure

During battery-balanced mode for the TM-HB topology, the output voltage is only a function a D_1, while the input voltage is a function of both D_1 and D_2. This implies that d_1 should be used to control the output while d_2 should be used to control the input. The design of the OVR controller is dictated by the frequency response of the output voltage to perturbations in d_1. A perturbation of d_1 induces a perturbation of the input voltage. If the IVR loop is closed, that induces a perturbation in d_2, and has a secondary effect upon the response of the output voltage. These interactions can be seen clearly in Figure 9.

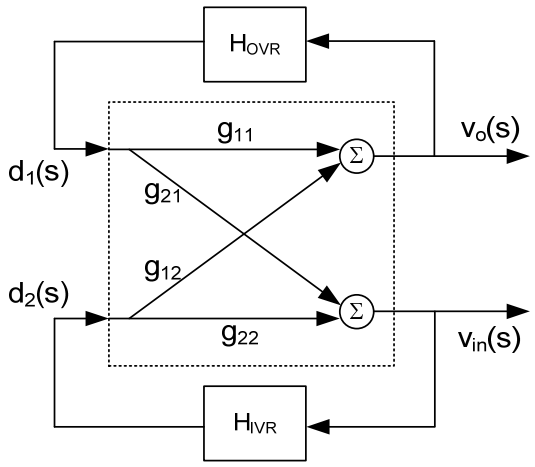

Figure 9: TM-HB small signal model

For the OVR loop, this is described mathematically as:

$$\frac{v_o(s)}{d_1(s)} = \frac{g_{11}}{1 + g_{21} \cdot g_{22} \cdot g_{12} \cdot H_{IVR}}$$

A similar scenario is encountered when designing the IVR loop. The IVR controller design is dictated by the response of the input voltage to perturbations in d_2, which is given by:

$$\frac{v_{in}(s)}{d_2(s)} = \frac{g_{22}}{1 + g_{12} \cdot g_{11} \cdot g_{21} \cdot H_{OVR}}$$

This interdependence of the loops through the power stage complicates the optimization of the controllers. The IVR loop typically has less stringent transient response requirements than the OVR loop. If the IVR loop is designed to have a significantly lower bandwidth, its loop gain can be neglected and it can be considered open around the cross-over frequency of the OVR loop. The OVR controller can then be designed with the approximation:

$$\frac{v_o(s)}{d_1(s)} \approx g_{11}$$

Once the OVR controller is designed, the IVR loop design becomes straightforward utilizing the IVR Equation. The magnitude and phase of $\frac{v_o(s)}{d_1(s)}$ and $\frac{v_{in}(s)}{d_2(s)}$ before compensation are plotted in Figure 10.

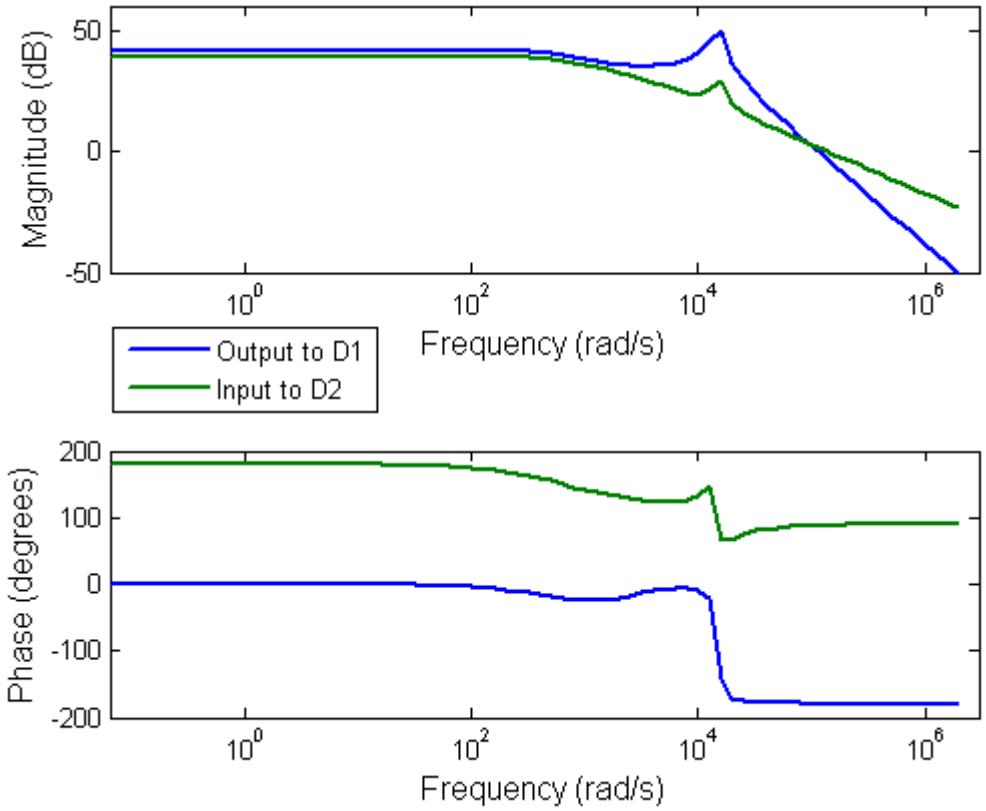

Figure 10: Non-compensated bode plots for TM-HB mode 1

Using these plots, compensators need to be designed to give a high magnitude at low frequencies, a crossover frequency far enough away from the switching frequency, and an acceptable phase margin. All of this will ensure that the signals will be well regulated and also stable. Using the approximations for $\frac{v_o(s)}{d_1(s)}$ and $\frac{v_{in}(s)}{d_2(s)}$ and making sure to keep the crossover

frequency of the input transfer function lower than that of the output, Figure 11 shows the magnitude and phase of the output and input after the addition of lead-lag compensation.

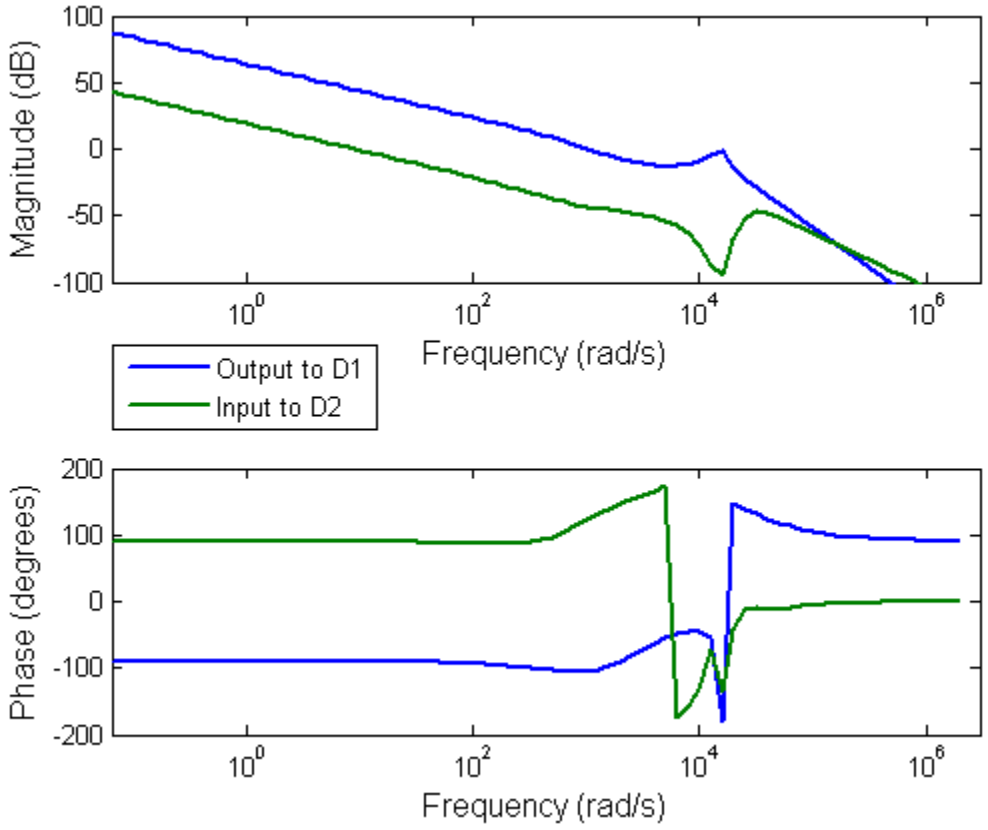

Figure 11: Compensated bode plots for TM-HB mode 1

The control structure was tested in Simulink by adding a small sinusoidal perturbation at 20Hz to d_1. The output voltage was regulated to 60V while the input was regulated to 50V. Figure 12 shows a comparison of the compensated PLECS circuit to the uncompensated averaged model. It can be seen that the oscillations of both the input voltage and output voltage have been reduced by 600% and 1200% respectively. In this way, simultaneous control of both the input and output ports is achieved.

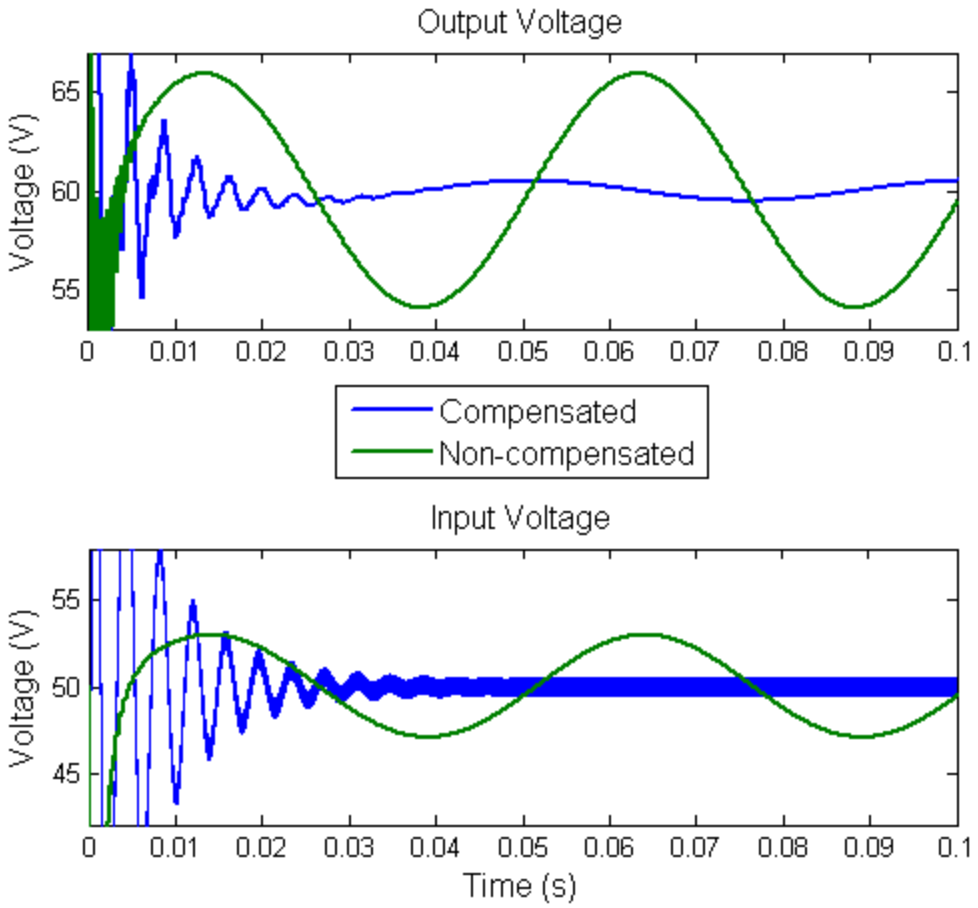

Figure 12: TM-HB mode 1 control simulation

TM-HB Battery-charge Regulation Mode Feedback Control

During mode 2 operation of the TM-HB, both the output and battery voltages are functions of both D_1 and D_2. To stay consistent with the mode 1 connections, D_1 will be used to control the output and D_2 will be used to control the battery voltage. It is again assumed that it is most important to maintain output regulation and so the battery voltage regulation loop is designed to have a lower bandwidth. The uncompensated bode plots of $\frac{v_o(s)}{d_1(s)}$ and $\frac{v_{bi}(s)}{d_2(s)}$ can be seen in Figure 13.

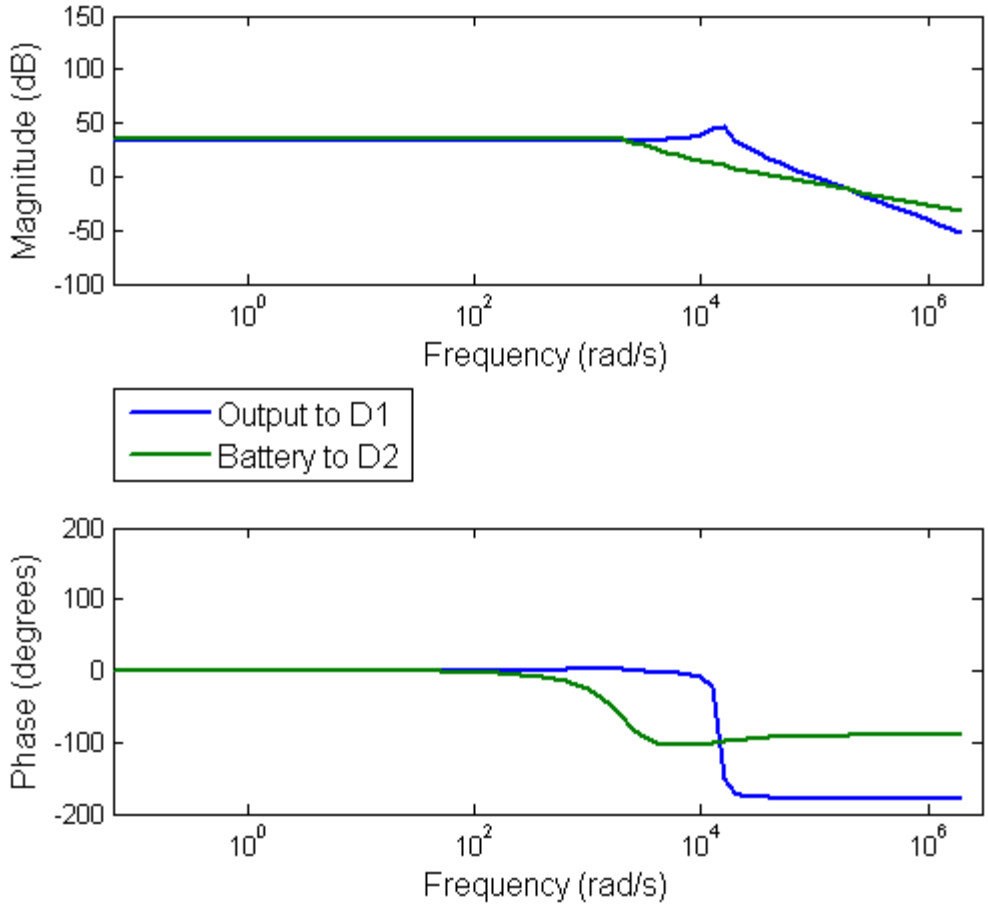

Figure 13: Non-compensated bode plots for TM-HB mode 2

Using the previously mentioned approximation for $\frac{v_o(s)}{d_1(s)}$, the bode plots of the transfer functions after lead-lag compensation can be seen in Figure 14.

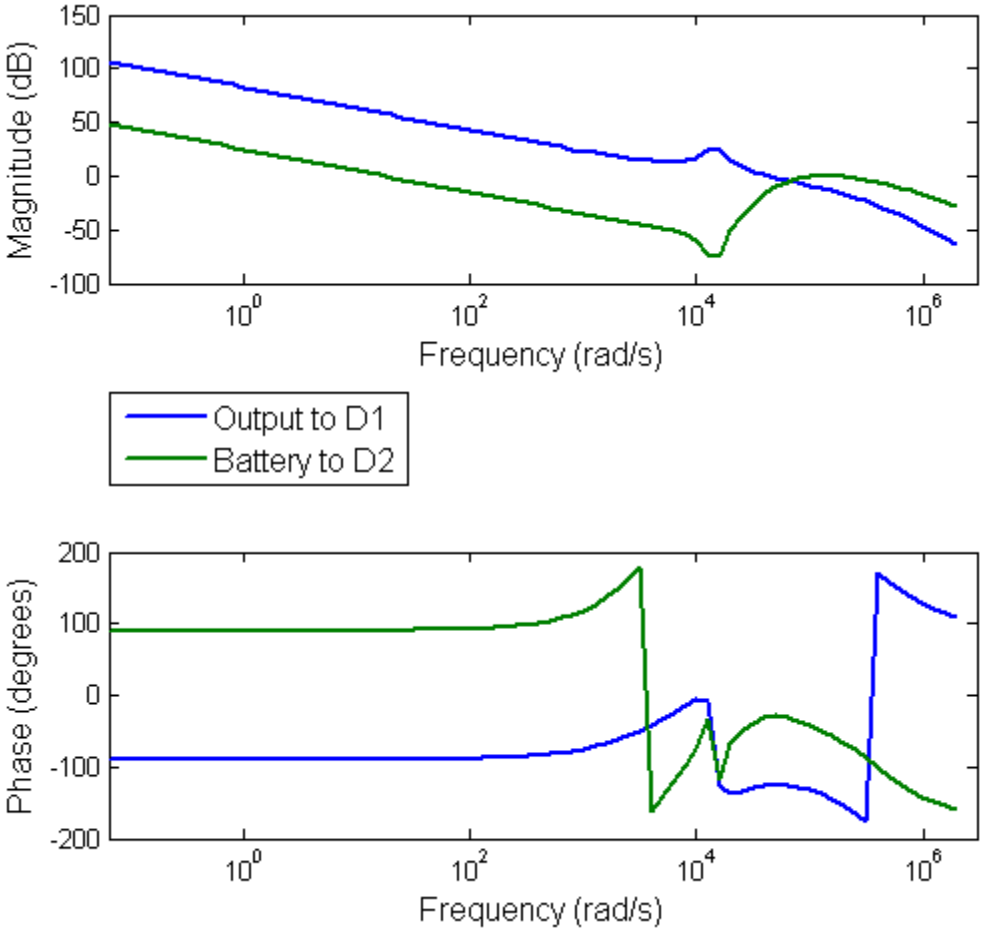

Figure 14: Compensated bode plots for TM-HB mode 2

The control structure was tested in Simulink by adding a small sinusoidal perturbation at 300Hz to d2. The output and battery voltages were both regulated to 28V. Figure 15 shows a comparison of the compensated PLECS simulation to the uncompensated averaged model. It can be seen that the sinusoidal oscillations are almost entirely eliminated by the compensators.

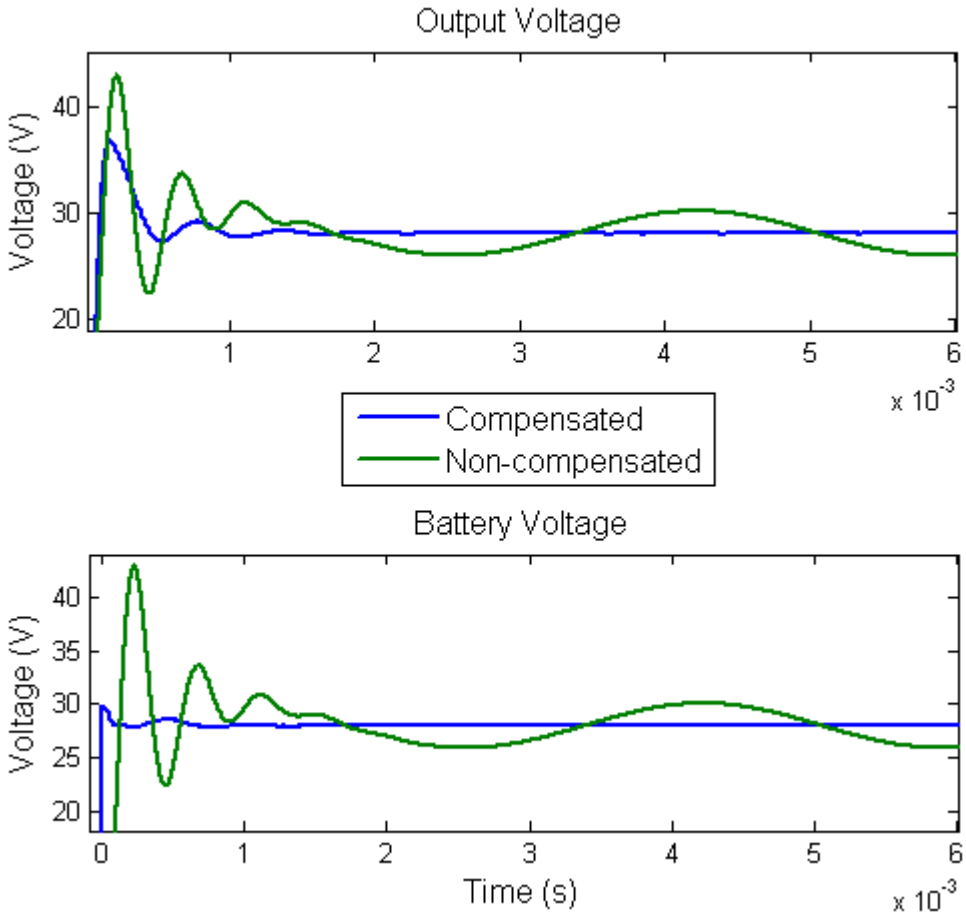

Figure 15: TM-HB mode 2 control simulation

BI-PS-FB Battery Balanced Mode Feedback Control

The BI-PS-FB topology has transfer function interactions similar to that of the TM-HB and these interactions are summarized in Figure 16. During mode 1, the input voltage is dependent only on the duty cycle D while the output voltage is dependent on both the duty cycle and the phase shift. This implies that D should be used to control the input and Φ to control the output. Assuming once again that the input has less stringent transient response requirements, the transfer functions can be simplified to:

$$\frac{v_o(s)}{\Phi(s)} \approx g_{11}$$

$$\frac{v_{in}(s)}{d(s)} = \frac{g_{22}}{1 + g_{12} \cdot g_{11} \cdot g_{21} \cdot H_{OVR}}$$

as long as the bandwidth of the IVR loop is kept significantly lower than that of the OVR loop.

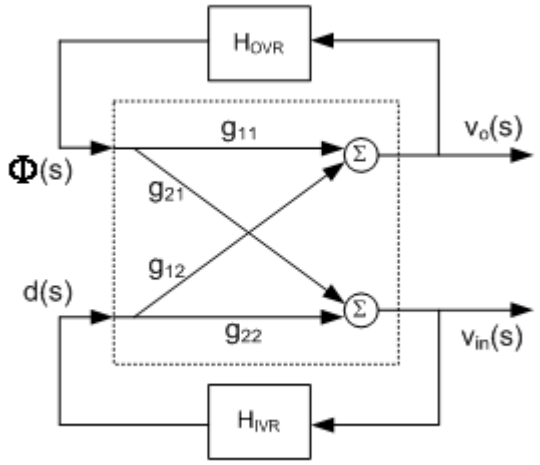

Figure 16: BI-PS-FB small signal model

Figure 17 shows the bode plots of the transfer functions $\frac{v_o(s)}{\Phi(s)}$ and $\frac{v_{bi}(s)}{d(s)}$ before compensation.

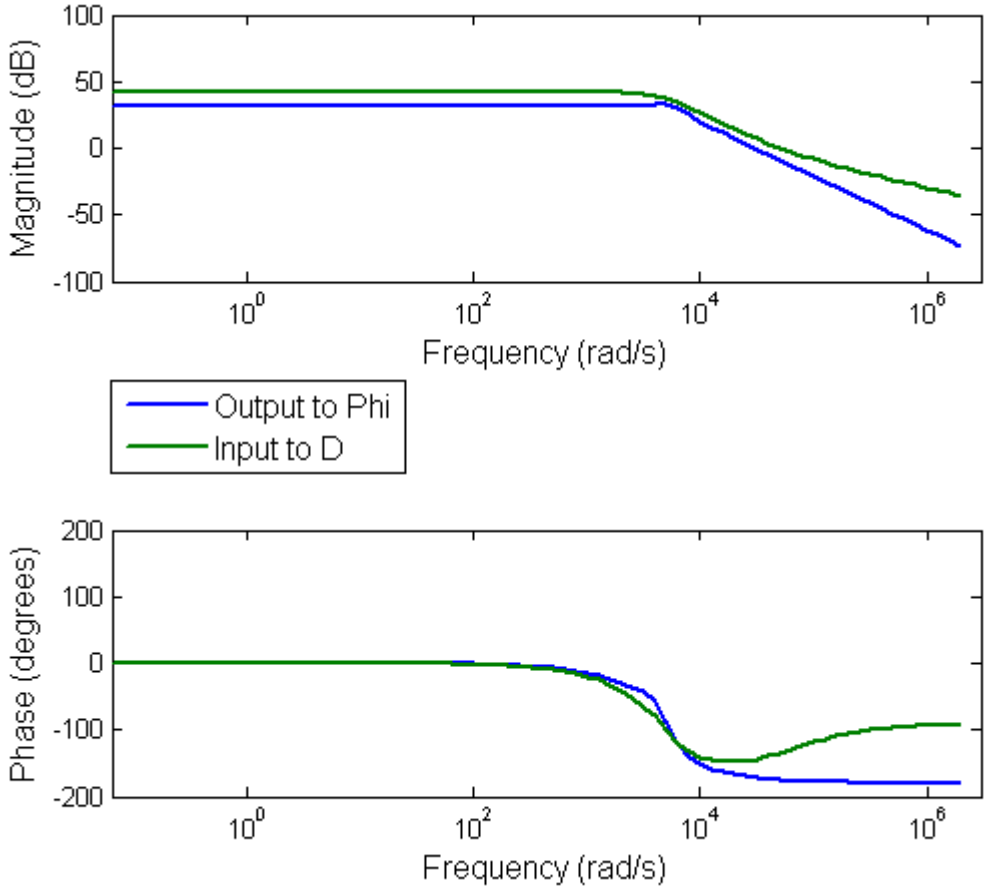

Figure 17: Non-compensated bode plots for BI-PS-FB mode 1

After the addition of a lead-lag compensator to each control loop, the bode plots of the transfer functions can be seen in Figure 18.

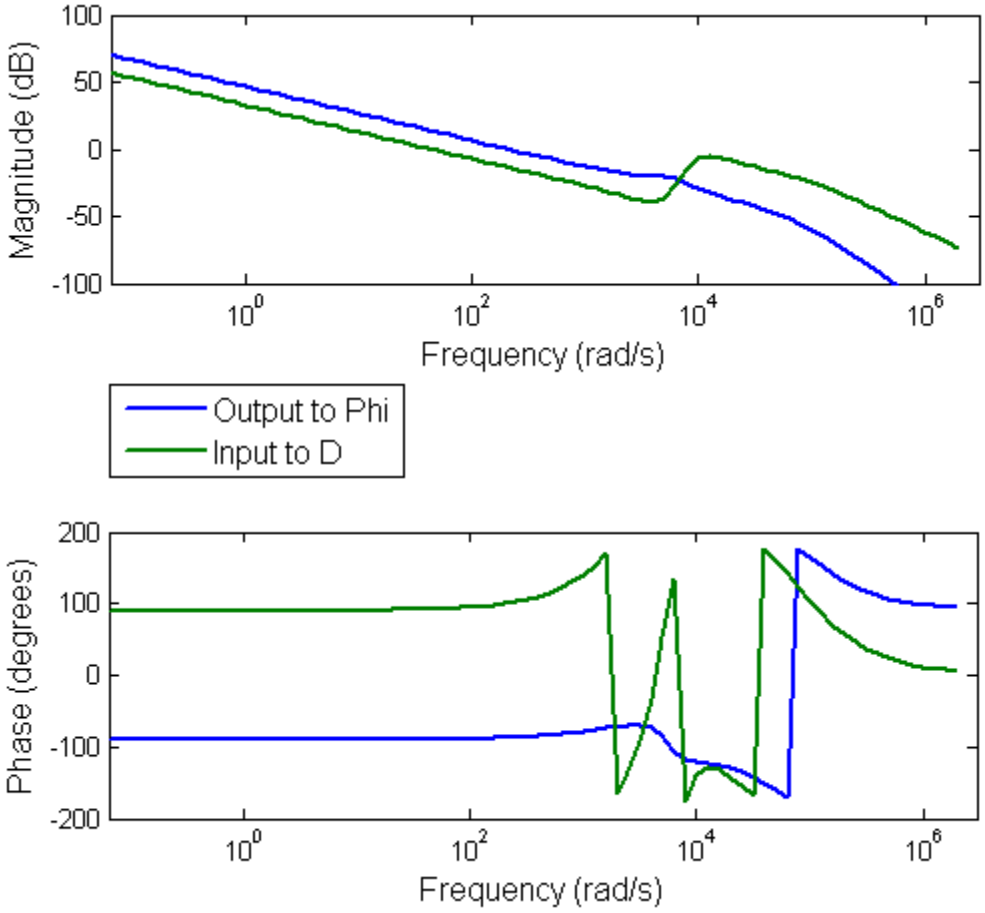

Figure 18: Compensated bode plots for BI-PS-FB mode 1

The control structure was tested in Simulink by adding a small sinusoidal perturbation at 50Hz to D. The output voltage was regulated to 28V and the input voltage was regulated to 50V. Figure 19 shows a comparison of the compensated PLECS simulation to the uncompensated averaged model. It can be seen that the sinusoidal oscillations are almost entirely eliminated by the compensators.

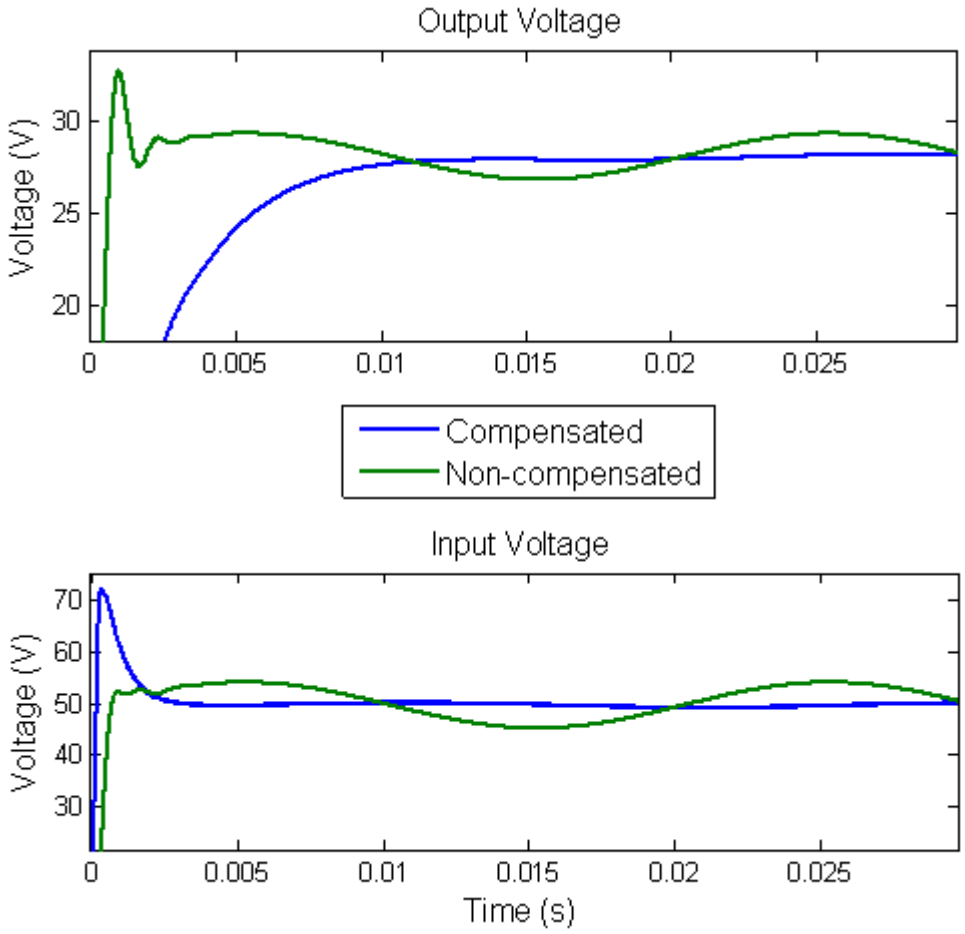

Figure 19: BI-PS-FB mode 1 control simulation

BI-PS-FB Battery-charge Regulation Mode Feedback Control

During mode 2 for the BI-PS-FB, the battery and output voltages are entirely independent of each other. This greatly simplifies the control design, especially since the transfer functions are of the same form as the output of a buck converter. The output voltage will be controlled by Φ while the battery voltage will be controlled by D. Figure 20 below shows the uncompensated transfer functions for $\frac{v_o(s)}{\Phi(s)}$ and $\frac{v_{bi}(s)}{d(s)}$.

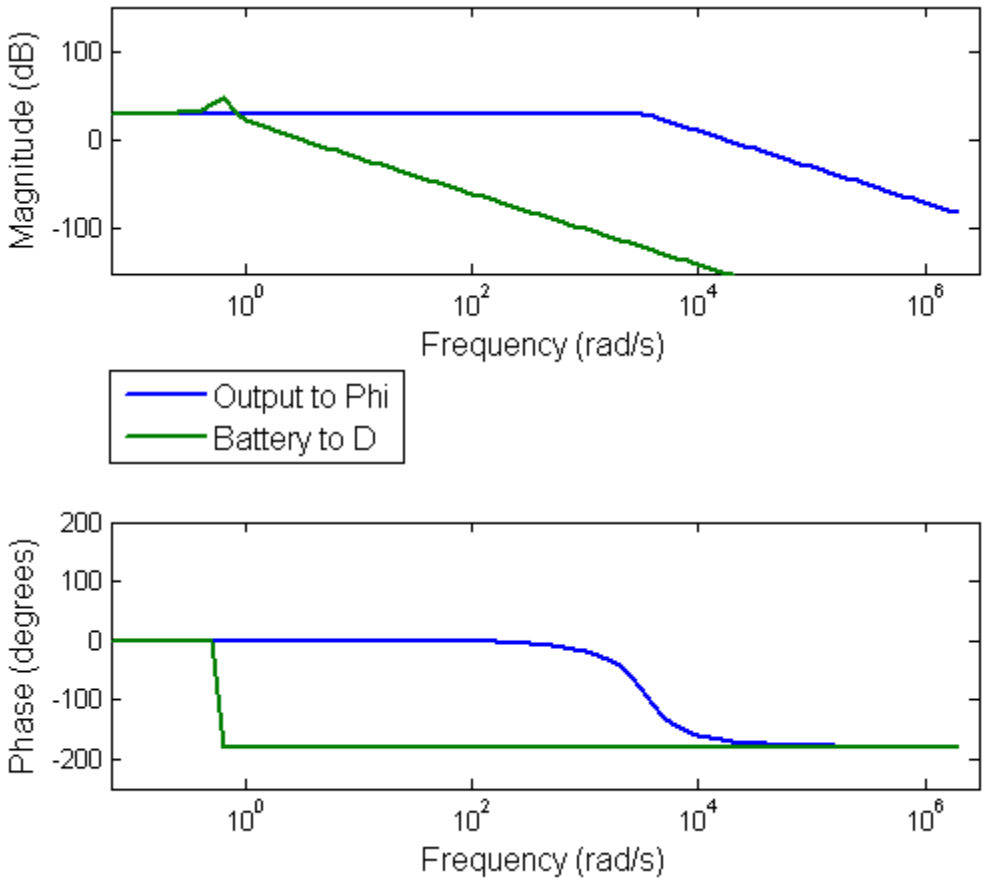

Figure 20: Uncompensated bode plots for BI-PF-FB mode 2

A lead-lag compensator was added to each control loop and the results can be seen in Figure 21.

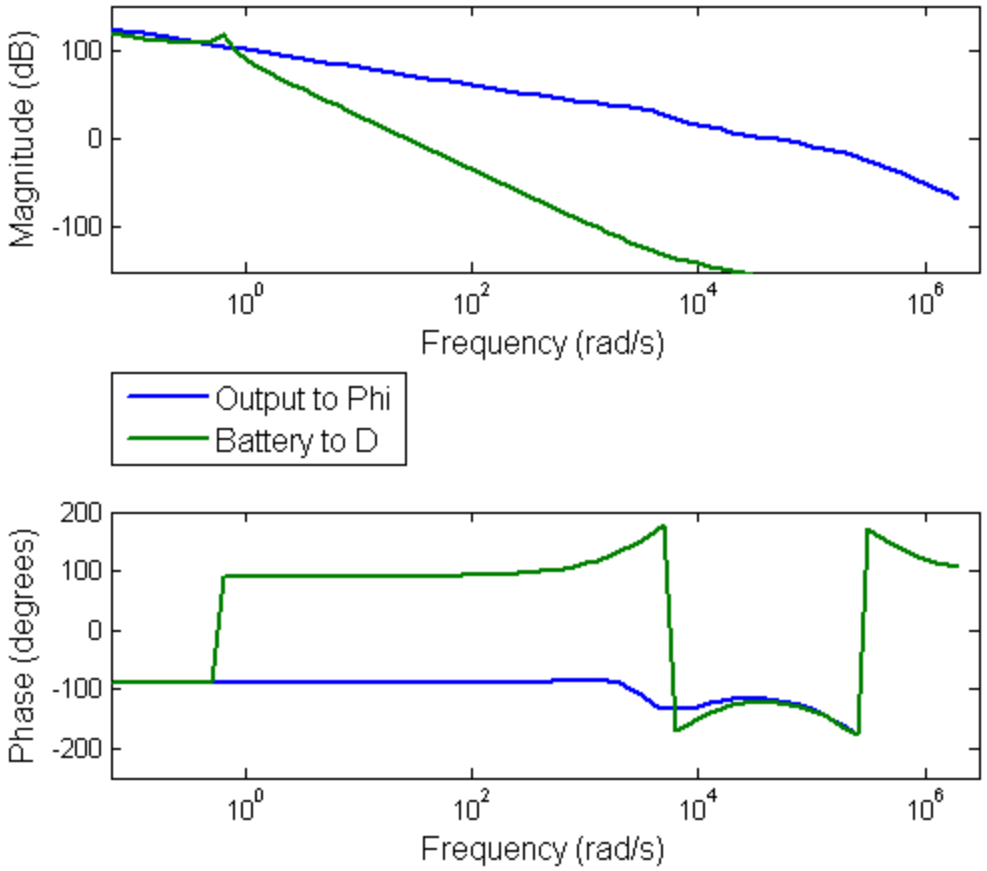

Figure 21: Compensated bode plots for BI-PS-FB mode 2

Figure 22 and Figure 23 show simulations of the compensated circuit compared to the non-compensated averaged model. Both the output and battery were regulated to 28V. Figure 22 is the result of a 500 Hz sinusoidal perturbation added to the phase shift Φ, while Figure 23 is the result of the same perturbation added to the duty cycle D. Each control loop is independent of the other and succeeds in regulating the voltage to the desired level. It can be seen in the results of the output voltage that there is the addition of a significant amount of overshoot. This can be reduced or eliminated with further optimization of the control loops.

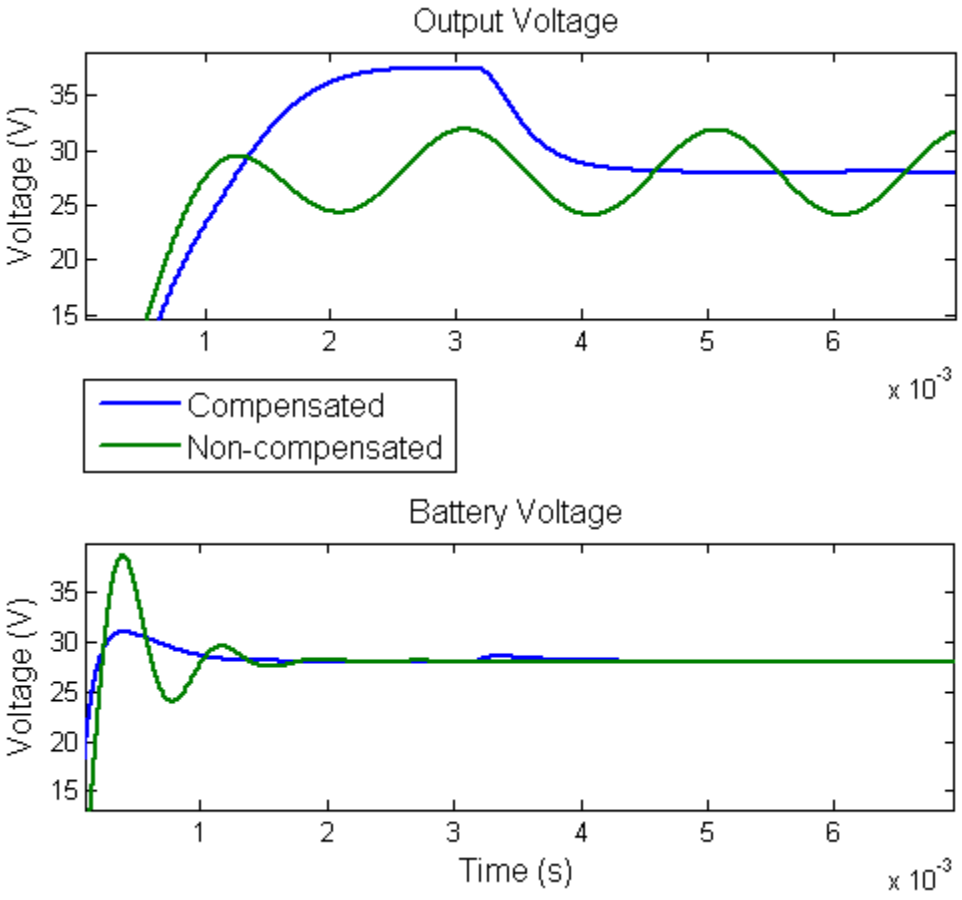

Figure 22: BI-PS-FB mode 2 control simulation with perturbation in Φ

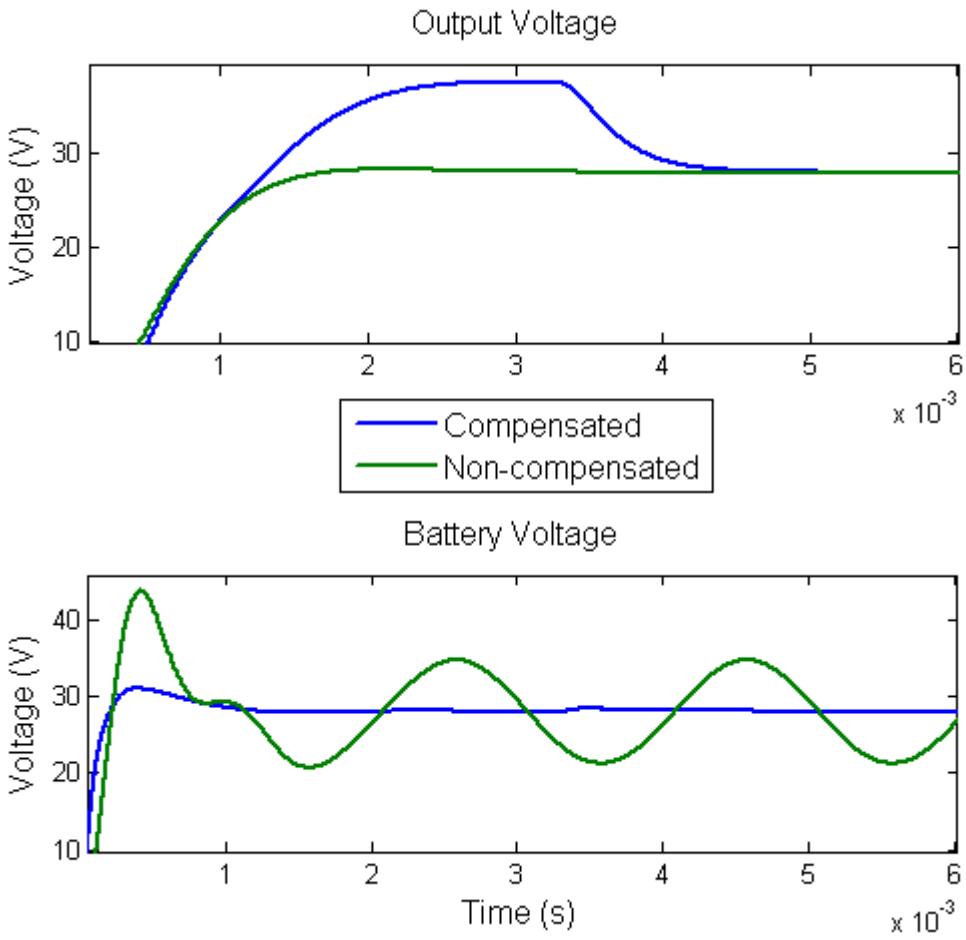

Figure 23: BI-PS-FB mode 2 control simulation with perturbation in D

Current Sharing Control

Current sharing is an essential ingredient in any system that uses multiple converters operating in parallel. This is because the converters will not inherently share the load, and one or more will try to assume a disproportionate amount of the load. Current sharing controls are needed to force each converter to have the same output current. This results in greatly increased reliability, as the component stresses will be evenly distributed among all of the converters. It also results in a faster transient/dynamic response and minimized thermal problems.

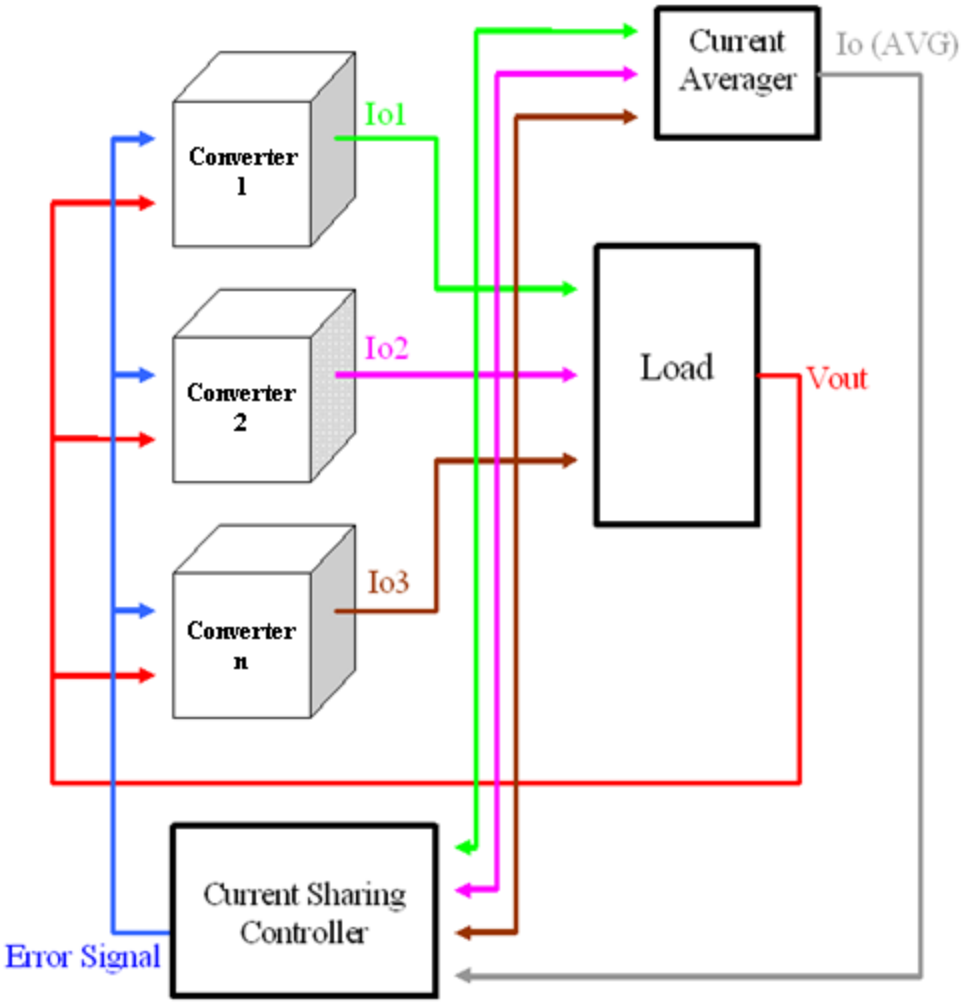

Figure 24: Output current sharing control structure

Figure 24 shows the current sharing control scheme that was designed to work with the system architecture. The output currents of the individual converters are averaged, and each converter compares its current to the average. This difference goes through a controller and the error signal slightly modifies the reference voltage of the output voltage regulation loop. This changes the output current to match the average, and because the change is small the overall output voltage regulation remains unaffected. The current sharing scheme was simulated in Matlab with five buck converters simulating the output of five three-port converters, and the

results are shown in Figure 25 and Figure 26. To simulate uneven current distribution, each channel was given a slightly different reference voltage. The plots show the response of the system to a load transient both with and without the current sharing controls included.

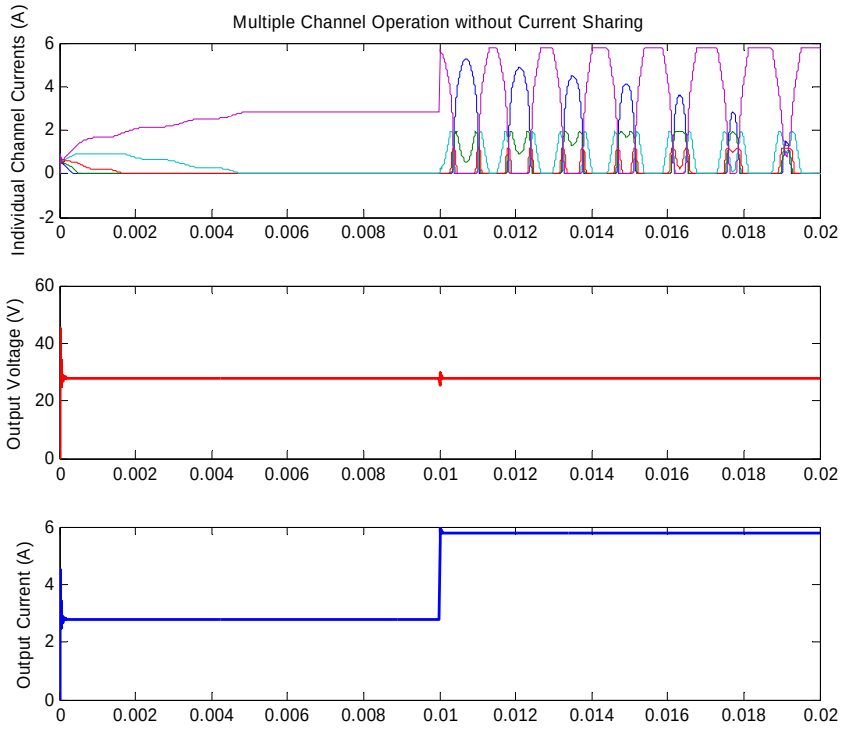

Figure 25: Multiple channel operation without current sharing control

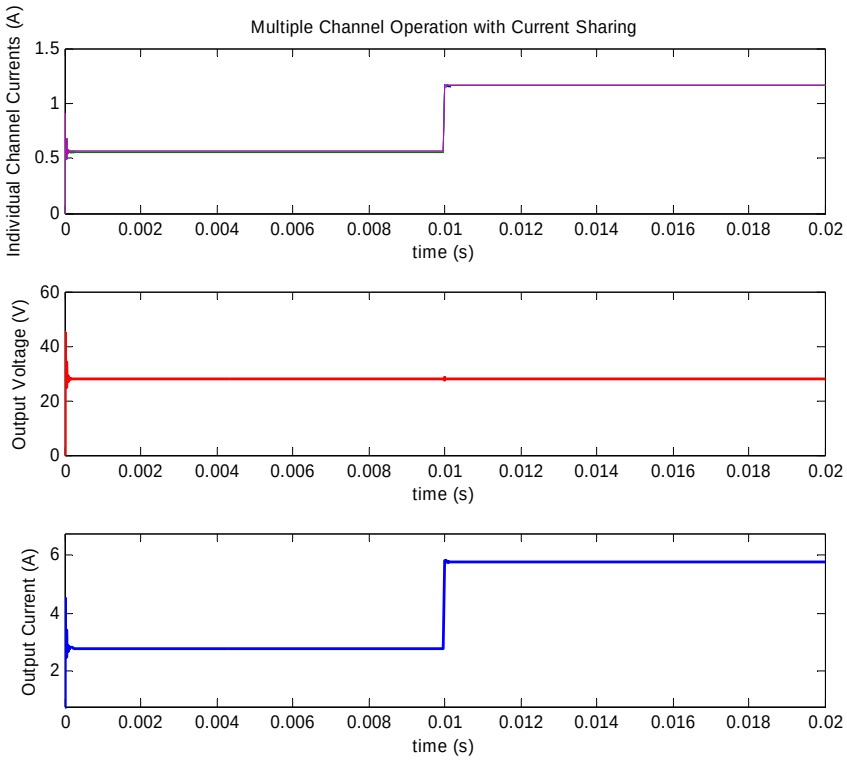

Figure 26: Multiple channel operation with current sharing control

Figure 25 shows a system with no current sharing regulation, and it can be seen that the output currents of each channel vary widely and show some instability. Figure 26 shows the same system with current sharing controls included. When the load is increased, the current of each individual channel remains regulated to the average, while the load remains tightly regulated to the reference voltage of 28V.

CHAPTER V: CONVERTER DESIGN

High-quality converter design leads to higher efficiencies and lower cost and depends directly on having accurate design equations and procedures to work with. This chapter explains all of the design procedures that were developed for the TM-HB topology.

Stress Analysis

Stress analysis for each component in the circuit is required to develop accurate design specifications. Without a proper stress analysis the overall lifetime of the device can be severely lowered, with higher chances of component failure due to overstressing. Knowledge of worst case current and voltage levels on the switches can be used to choose the best switching device for the chosen application, taking into account breakdown voltage, on-resistance, switching speed, and other parameters. Knowledge of current and voltage levels also allows sizing of the magnetic components in the circuit such as the transformer and inductors. Magnetics design will be described in more depth at the end of the chapter.

Current and Voltage Stress

Assuming CCM operation and neglecting inductor current ripple, the rms currents in the switching devices are given by:

$$I_{S1}^{rms} = \sqrt{D_1} \cdot \left| I_M - n \cdot I_o \right|$$

$$I_{S2}^{rms} = \sqrt{D_2} \cdot \left| n \cdot I_o + I_M \right|$$

$$I_{S3}^{rms} = \sqrt{1 - D_1 - D_2} \cdot \left| n \cdot I_o + I_M \right|$$

The ideal maximum voltages stresses seen across the switching devices are:

$$V_{S1} = V_{S2} = V_{in}$$

$$V_{S3} = V_{bi}$$

$$V_{Diode}^{aux} = \frac{D_1}{D_2} \cdot V_{bi}$$

where V_{Diode}^{aux} is the voltage seen across the auxiliary branch diode.

The average currents seen through the rectifier diodes are:

$$I_{D1}^{avg} = (1 - D_1) \cdot I_o$$

$$I_{D2}^{avg} = D_1 \cdot I_o$$

The rms currents through the two input capacitors are given by:

$$I_{C2}^{rms} = \sqrt{{I_{in}}^2 + D_2 \cdot (n \cdot I_o + I_M)^2 - 2 \cdot D_2 \cdot I_{in}(n \cdot I_o + I_M)}$$

$$I_{C1}^{rms} = \sqrt{D_1 \cdot (I_M + I_{in} - n \cdot I_o - I_{bi})^2 + (1 - D_1) \cdot (I_{bi} - I_{in})^2}$$

The rms current through the primary winding of the transformer is:

$$I_{prim}^{rms} = \sqrt{{I_M}^2 + n^2 \cdot {I_o}^2 + 2 \cdot n \cdot I_M \cdot I_o \cdot (1 - 2 \cdot D_1)}$$

assuming the leakage inductance holds the reflected output current constant.

Loss Equations

Power loss equations are also important to the converter design process. Using these equations the efficiency can be predicted based on the chosen operating parameters, the design can be further refined until an acceptable amount of efficiency is achieved. Also, since power loss

translates directly into heating up of the component, these equations are important for sizing any heat sinks that may be required.

The total conduction loss of the three switches can be estimated to be:

$$P_{Switches}^{CondLoss} = R_{ds}^{on} \cdot \left[I_M{}^2 + n^2 \cdot I_o{}^2 + 2 \cdot n \cdot I_o \cdot I_M \cdot (1 - 2 \cdot D_1) \right],$$

assuming equal on-resistance, R_{ds}^{on}, for all three switches.

The total conduction loss of the rectifier diodes can be estimated to be:

$$P_{rectifier}^{CondLoss} = V_D^{on} \cdot I_o$$

where V_D^{on} is the diode forward conduction voltage drop.

The conduction loss of the auxiliary diode can be estimated to be:

$$P_{aux}^{CondLoss} = V_D^{on} \cdot (1 - D_1 - D_2) \cdot (I_M + n \cdot I_o)$$

Soft Switching Design Constraints

Soft switching is an important technique used to improve efficiency by eliminating turn-on and turn-off switching losses. A major advantage of using the half-bridge and full-bridge topologies is the ease of achieving soft switching, and the topologies derived from them maintain this advantage. Zero voltage switching is a soft switching technique involving the elimination of turn-on losses by making sure the series capacitance of the switching device is totally discharged while the switch turns on. Zero voltage switching can be achieved if the combination of the reflected load current and the magnetizing current discharge the parasitic capacitance of each switch to zero voltage during the switching dead time. This forces its anti-parallel diode to conduct until the switch is turned-on. ZVS conditions are discussed next.

Switch 1 ZVS Constraints

The leakage inductance plays an important role in achieving ZVS for switch 1 and 2. By using its stored current during the switching dead time, enough current can be passed through the parasitic capacitance of the switch to discharge it entirely. To help ensure a wide range of ZVS, a large enough leakage inductance must be chosen. ZVS for switch 1 can be achieved if:

$$\left(n \cdot I_o + I_m\right) \cdot \sqrt{L_k} > V_{bi} \cdot \sqrt{2 \cdot C_{ds}^{eff}}$$

Where L_k is the leakage inductance, C_{ds}^{eff} is the effective drain-to-source capacitance of each switch, and V_{bi} is the voltage across the storage port.

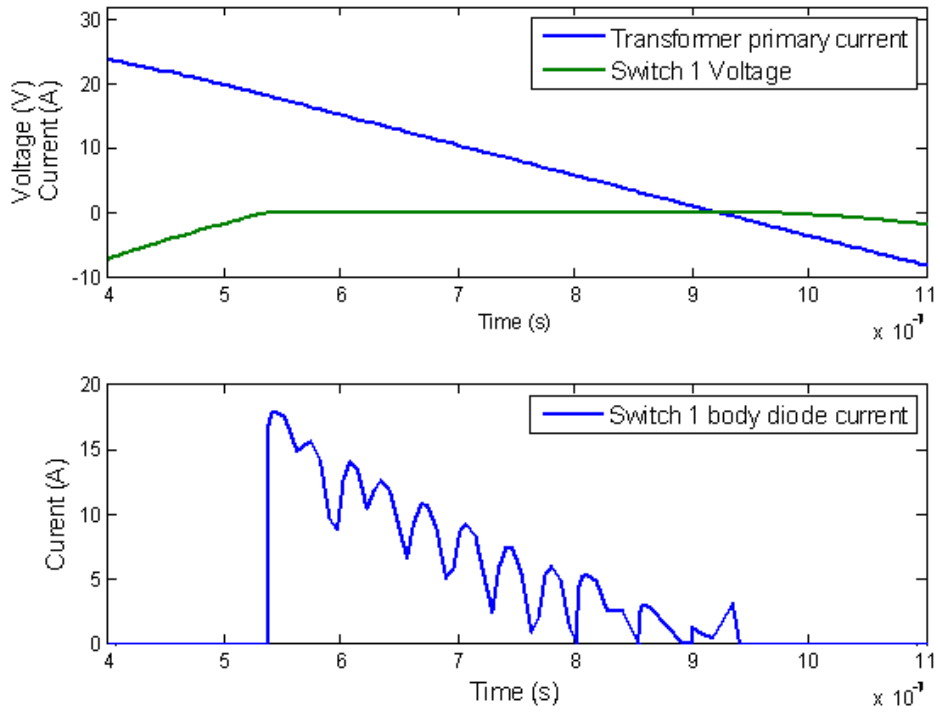

Figure 27: ZVS of switch 1

Figure 27 shows the dead time before switch 1 is turned on. The transformer primary current, which is the sum of the reflected load current and the magnetizing current, is retained by the

leakage inductance. As long as this current discharges the voltage across the switch capacitance to zero before it falls to zero itself, the switch can turn on with ZVS. Figure 27 also shows the current through the body diode of the switch, which starts conducting when the voltage across the switch reaches zero.

Switch 2 ZVS Constraints

Similar to the case for switch 1, switch 2 uses a combination of the reflected load current and the magnetizing current to discharge the parasitic capacitance of the switch. To achieve this, the average reflected load current must be larger than the average magnetizing current in order for the current directions to be correct. For a wide range of ZVS, the leakage inductance can be determined by:

$$\left(n \cdot I_o - I_m\right) \cdot \sqrt{L_k} > V_{C1} \cdot \sqrt{2 \cdot C_{ds}^{eff}}$$

Where V_{C1} is the voltage across the input capacitor, equal to $V_{in} - V_{bi}$. Figure 28 below shows the dead time before switch 2 is turned on. This time the transformer primary current is the reflected load current minus the magnetizing current, hence the requirement that the reflected load current be larger than the magnetizing current during this period. If the transformer primary current can discharge the voltage across the switch capacitance before falling to zero, the switch can turn on with ZVS. Figure 28 also shows the current through the body diode of switch 2, which starts conducting when the voltage across the switch falls to zero.

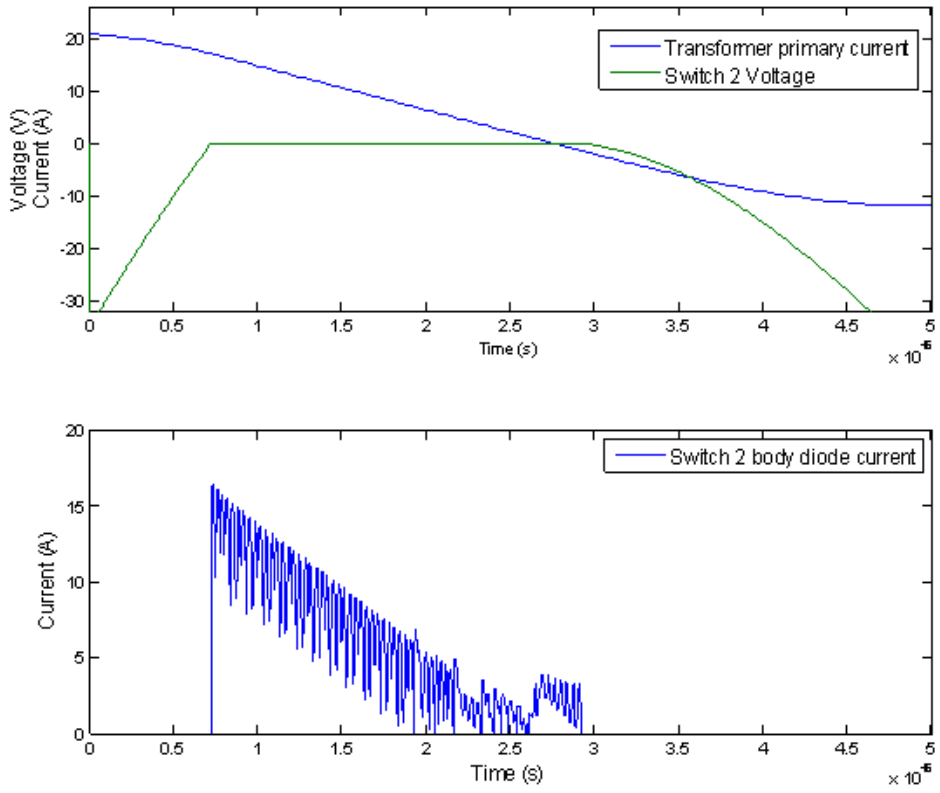

Figure 28: ZVS of switch 2

Switch 3 ZVS Constraints

Concerning the switching behavior of switch S3, by paralleling a capacitor across the auxiliary branch diode such that its capacitance is greater than that of the drain-to-source capacitance of the switch, S3 is easily guaranteed to turn on at zero-current zero-voltage switching (ZCZVS) and turn off at ZVS. In addition to the quantitative constraints presented here, a suitable duration of switching dead-time before each switch is turned on is required to secure proper ZVS operation. This dead time is very small compared to the switching period of the PWM.

Transformer design

The transformer design for the TM-HB topology is similar to designing a flyback transformer, in that it is an inductor-like transformer. Once the desired magnetizing inductance has been chosen, the core material, shape, and size can be chosen to give a low amount of core loss. The window should be as wide as possible to maximize winding breadth and minimize the number of layers. This minimizes ac winding resistance. The wide window also minimizes leakage inductance. With a wider window, less winding height is required, and the window area utilization is usually better. The amount of primary windings can be calculated to give the desired inductance at the expected max flux density swing. Then, the gap size can be calculated based on the amount of primary windings to give the desired inductance. Finally, the amount of secondary windings can be chosen to give the desired turns ratio.

CHAPTER VI: CONCLUSIONS

The results that were presented in this paper are only a part of the overall research that was done with the two three-port topologies, with the rest of the analysis being done by the other members of the research team. It has been shown that a mathematical model can be created to approximate both of the topologies in either of their modes of operation. Further, these models were used to design a control structure that simultaneously regulates two of the three ports, with the regulated ports dictated by the current mode of operation. The basic structure for a system architecture to manage multiple converters operating in parallel was also presented. To improve system reliability, an output current sharing control scheme was developed to force each converter to share the load equally. Finally, a set of design equations was developed for the TM-HB topology which includes stress analysis, power loss estimates, soft-switching design constraints, and transformer design procedures.

As of October 2007, further research into the presented three-port converters will be funded by NASA with the achievement of a phase II SBIR contract. The goals of this contract coincide with the next steps that need to be taken in the research of these topologies. These goals include:

1. Create a detailed converter design based on NASA's specifications that includes snubbers, input and EMI filters, and protection circuits. Using the design equations trade-offs can be analyzed, heat sinks can be sized, and battery chemistry chosen. Knowing the constraints for ZVS operation will aid in achieving high efficiency and low heat sink size and weight.

2. Increase the optimization of the control loops, and add in high level controls such as MPPT and battery-charge control.
3. Control algorithms need to be designed for the system level controller. This controller will manage all of the converters in the system, divided into solar channels and solar groups. It will need to be able to dynamically switch the operating modes of any converter or converter group to match the current conditions of the system.

Achieving these goals will provide a fully functional and redundant solar power system that is ideally suited for use in space applications. However, this system can easily be extended for use in any applications where a steady continuous power source is not available, and where energy storage backup is required to handle the mismatch between source availability and loading patterns.

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