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Transient Response Improvement For Multi-phase Voltage Regulators

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TRANSIENT RESPONSE IMPROVEMENT FOR MULTI-PHASE VOLTAGE REGULATORS

by

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ABSTRACT

Next generation microprocessor (Vcore) requirements for high current slew rates and fast transient response together with low output voltage have posed great challenges on voltage regulator (VR) design [1]. Since the debut of Intel 80X86 series, CPUs have greatly improved in performance with a dramatic increase on power consumption. According to the latest Intel VR11 design guidelines [2], the operational current may ramp up to 140A with typical voltages in the 1.1V to 1.4V range, while the slew rate of the transient current can be as high as 1.9A/ns [1, 2]. Meanwhile, the transient-response requirements are becoming stringer and stringer. This dissertation presents several topics on how to improve transient response for multi-phase voltage regulators.

The Adaptive Modulation Control (AMC) is a type of non-linear control method which has proven to be effective in achieving high bandwidth designs as well as stabilizing the control loop during large load transients. It adaptively adjusts control bandwidth by changing the modulation gain, depending on different load conditions. With the AMC, a multiphase voltage regulator can be designed with an aggressively high bandwidth. When in heavy load transients where the loop could be potentially unstable, the bandwidth is lowered. Therefore, the AMC provides an optimal means for robust high-bandwidth design with excellent transient performance.

The Error Amplifier Voltage Positioning (EAVP) is proposed to improve transient response by removing undesired spikes and dips after initial transient response. The EAVP works only in a

short period of time during transient events without modifying the power stage and changing the control loop gain. It facilitates the error amplifier voltage recovering during transient events, achieving a fast settling time without impact on the whole control loop.

Coupled inductors are an emerging topology for computing power supplies as VRs with coupled inductors show dynamic and steady-state advantages over traditional VRs. This dissertation first covers the coupling mechanism in terms of both electrical and reluctance modeling. Since the magnetizing inductance plays an important role in the coupled-inductor operation, a unified State-Space Averaging model [3] is then built for a two-phase coupled-inductor voltage regulator. The DC solutions of the phase currents are derived in order to show the impact of the magnetizing inductance on phase current balancing. A small signal model is obtained based on the state-space-averaging model. The effects of magnetizing inductance on dynamic performance are presented.

The limitations of conventional DCR current-sensing for coupled inductors are addressed. Traditional inductor DCR current sensing topology and prior arts fail to extract phase currents for coupled inductors. Two new DCR current sensing topologies for coupled inductors are presented in this dissertation. By implementation of simple RC networks, the proposed topologies can preserve the coupling effect between phases. As a result, accurate phase inductor currents and total current can be sensed, resulting in excellent current and voltage regulation.

While coupled-inductor topologies are showing advantages in transient response and are becoming industry practices, they are suffering from low steady-state operating efficiency. Motivated by the challenging transient and efficiency requirements, this dissertation proposes a Full Bridge Coupled Inductor (FBCI) scheme which is able to improve transient response as well as savor high efficiency at (a) steady state. The FBCI can change the circuit configuration under different operational conditions. Its "flexible" topology is able to optimize both transient response and steady-state efficiency. The flexible core configuration makes implementation easy and clear of IP issues.

A novel design methodology for planar magnetics based on numerical analysis of electromagnetic fields is offered and successfully applied to the design of low-voltage high power density dc-dc converters. The design methodology features intense use of FEM simulation. The design issues of planar magnetics, including loss mechanism in copper and core, winding design on PCB, core selections, winding arrangements and so on are first reviewed. After that, FEM simulators are introduced to numerically compute the core loss and winding loss. Consequently, a software platform for magnetics design is established, and optimized magnetics can then be achieved.

Dynamic voltage scaling (DVS) technology is a common industry practice in optimizing power consumption of microprocessors by dynamically altering the supply voltage under different operational modes, while maintaining the performance requirements. During DVS operation, it is desirable to position the output voltage to a new level commanded by the microprocessor (CPU)

with minimum delay. However, voltage deviation and slow settling time usually exist due to large output capacitance and compensation delay in voltage regulators. Although optimal DVS can be achieved by modifying the output capacitance and compensation, this method is limited by constraints from stringent static and dynamic requirements. In this dissertation, the effects of output capacitance and compensation network on DVS operation are discussed in detail. An active compensator scheme is then proposed to ensure smooth transition of the output voltage without change of power stage and compensation during DVS. Simulation and experimental results are included to demonstrate the effectiveness of the proposed scheme.

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With sincere appreciation in my heart, I would first like to thank my advisor, Dr. Thomas X. Wu for his guidance, encouragement and support throughout this work and my studies. It was (he) who first led me into this research area. He changed the direction of my life. I have learned from him not only academic knowledge but also the methods for being a successful researcher. His imagination, integrity, and vast knowledge have been a source of inspiration for me throughout the years.

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CHAPTER 1 INTRODUCTION

1.1 Introduction to Multi-phase Voltage Regulator

Historically, silicon process technology has followed Moore's law, moving to a new silicon process generation every 18 to 24 months, with a corresponding doubling of CPU performance as shown in Fig. 1-1 [3]. Silicon process technology is expected to progress at this rate for the foreseeable future. In theory, this would result in CPUs with enormous processing capabilities. By 2020, a microprocessor could have more than 20 billion transistors, approximately 1 terabyte per second (TB/sec) of bus bandwidth, and frequencies of about 3 terahertz [4]. The continued improvements in silicon processing techniques have resulted in lower supply voltage and higher power.

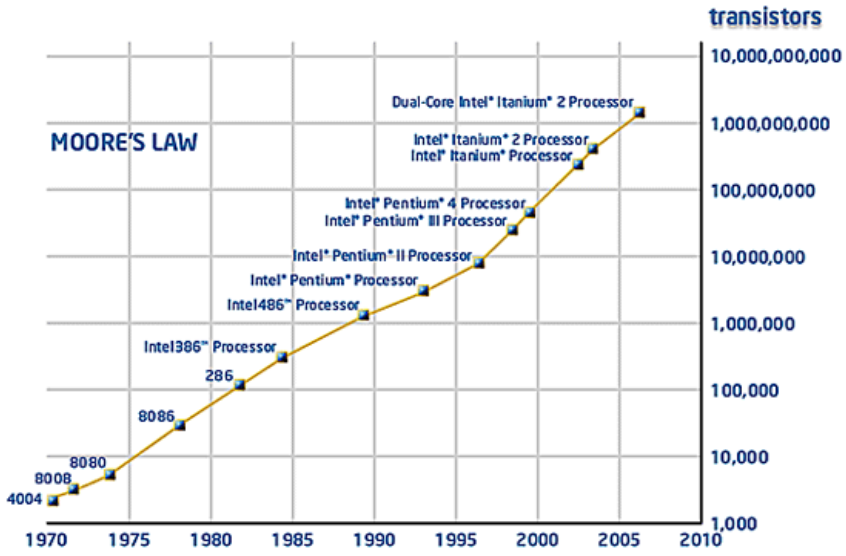


Figure 1-1. Moore's law of number of transistors in one microprocessor [3].

With the ramp-up of the number of transistors, CPUs have greatly improved in performance with a dramatic increase of power consumption since the debut of Intel 80X86 series. In the early days, the CPU was powered from the 5V rail of the silver box directly as shown in Fig. 1-2. As the high-performance Pentium CPU demanded a lower voltage, a dedicated DC-DC converter (voltage regulator) was placed in close proximity to the CPU socket. The topology was typically a single-phase buck converter as shown in Fig. 1-3, since the power delivered to the CPU was low.

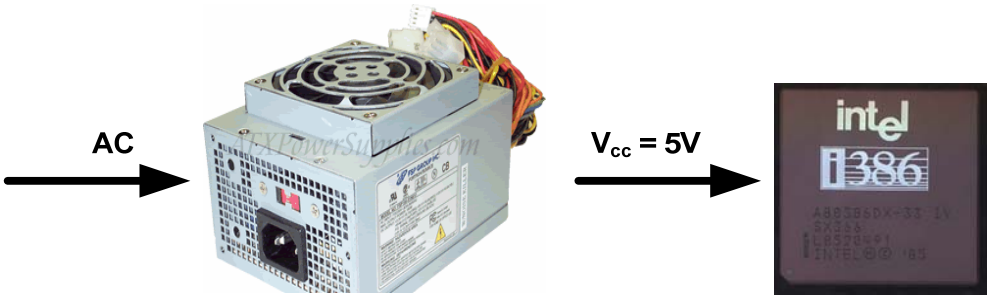


Figure 1-2. Power delivery architecture of early computer systems.

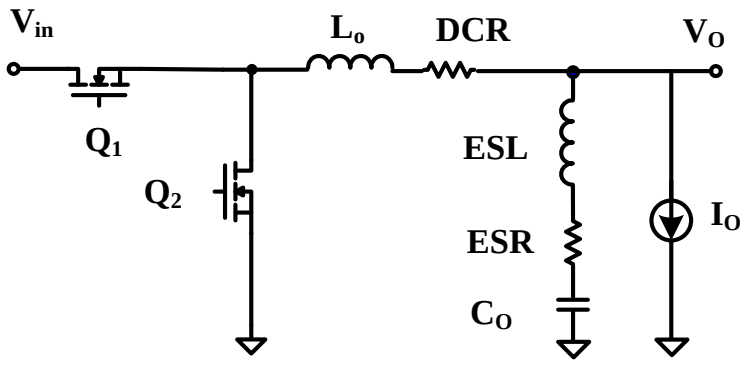


Figure 1-3. Single-phase synchronous buck converter.

As technology advanced, the CPU demanded much more power than ever. The power of the 5V output from the silver box was so high that the distribution loss on the 5V bus became unacceptable. Hooking the VR to the 5V bus was no longer efficient from a system point of view; therefore, VR input voltage was moved to the 12V output of the silver box. Meanwhile, a single-phase buck converter could no longer meet the high-current requirements since handling the high power in a single-phase converter would place high thermal stress on the components such as inductors and metal-oxide semiconductor field-effect transistors (MOSFETs). The technical challenges associated with increased power have forced a change to a both cost-effective and thermally viable solution of multiphase [5] [6] [7] as shown in Fig. 1-4. The interleaved multi-phase buck converter approach has been the most popular way to implement high current core solutions for advance processors.

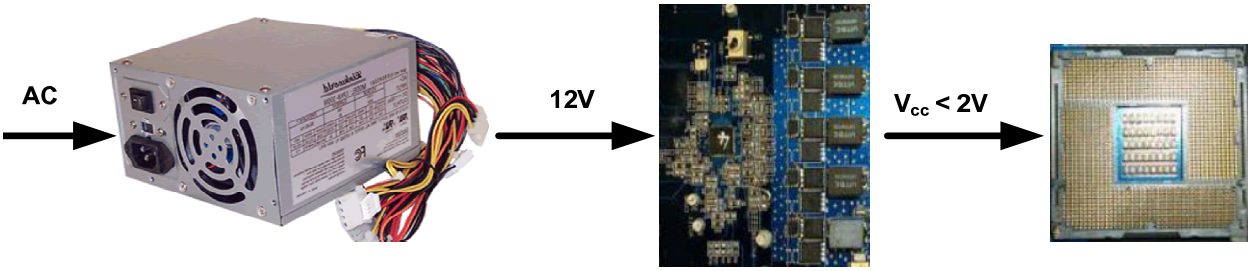


Figure 1-4. CPU power delivery with multiphase buck converter.

Fig. 1-5 shows a simple block diagram of a multi-phase voltage regulator. Multiple phases are paralleled and operated in an interleaved way. If regulated properly, the current can be divided evenly among all phases. As a result, the interleaving buck solution helps spread temperature rise

among multiple phases. Therefore, it reduces thermal stress on a single phase as well as provides flexibility for component selection and board layout.

In a multiphase voltage regulator, the switching of each phase is timed to be symmetrically interleaved with each of the other phases. For example, in an N-phase converter, each channel switches 1/N cycle after the previous phase and 1/N cycle before the following phase. As a result, a multi-phase voltage regulator has an effective switching frequency N times greater than the switching frequency of any single phase. In addition, due to the interleaved operation, the peak-to-peak current ripple of the total current is reduced in proportion to the phase number. The interleaved operational waveforms of a two-phase example in Fig. 1-6 suggest that multiphase voltage regulator is able to reduce the total current ripple and output voltage ripple [8].

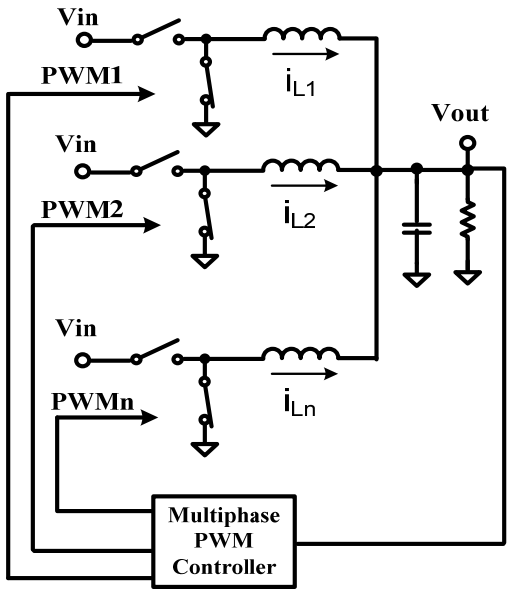


Figure 1-5. Conventional multiphase buck converter.

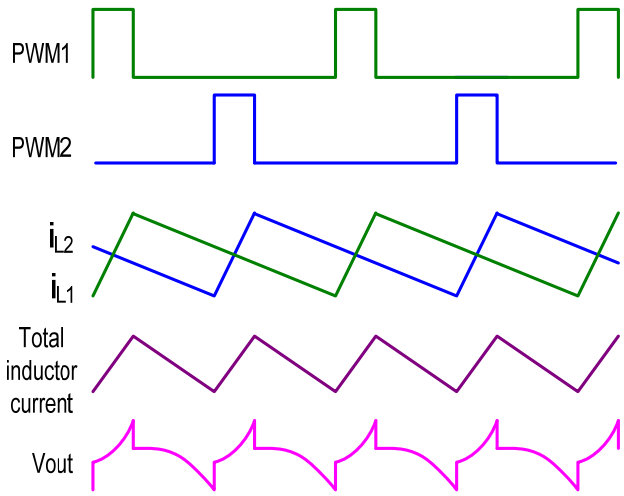


Figure 1-6. Interleaved operational waveforms for multiphase buck converters.

Examination of Equation 1-1 will help understand how a multiphase voltage regulator reduces current ripple. The equation represents a single phase's peak-to-peak inductor current ripple I_{pp}:

$$I_{pp} = \frac{(V_{in} - V_O) \cdot V_O}{L \cdot F_s \cdot V_{in}} \tag{1-1}$$

In above equation, V_{in} is the input voltage and V_O is the output voltage, respectively. L is the inductance value for each phase, and F_s is the switching frequency. Due to the symmetrical output ripple under interleaved operational mode as shown in Fig. 1-6, the actual frequency of the output ripple is the product of phase switching frequency and phase number (N). By summation of N symmetrically phase shifted inductor currents in Equation 1-1, the peak-to-peak output current for an N-phase converter can be expressed by

$$I_{pp} = \frac{(V_{in} - N \cdot V_O) \cdot V_O}{L \cdot F_s \cdot V_{in}} \tag{1-2}$$

It is found from Equation 1-2 that the output current ripple is a function of input voltage, output voltage, output inductance, switching frequency, and phase number. The more the phase number is, the lower the amplitude of the output current ripple will be. Increased overall effective frequency and lower peak-to-peak current ripple enable the designer to use less phase inductance and reduced total output capacitance. Since output inductors and capacitors consume significant footprints and costs on VR, the advantages of reducing output inductance and capacitance of multiphase VR becomes especially attractive to designers.

Another benefit of interleaving is the reduction of input ripple current. The simplified equation for the input RMS current I_{in_rms} of a multiphase buck converter can be expressed as:

$$I_{in\_rms} = \sqrt{I_{ph}{}^2 \cdot (N \cdot D - N^2 \cdot D^2) + \frac{I_{rip}{}^2 \cdot D \cdot N}{12}} \tag{1-3}$$

Where I_{ph} is the averaged phase current, D is the duty cycle, and I_{rip} is the phase ripple current. Assuming the duty cycle for a voltage regulator is 0.1 and the output current is 100A, the input RMS current vs. the phase number can be plotted as shown in Fig. 1-7. It is found that as the phase number increases, the input RMS current decreases. Since the required input capacitance is dictated mostly by the maximum input RMS current, multiphase voltage regulator has the advantages in reducing overall system cost and size by decreasing maximum input RMS current and then reducing the total number of input capacitors.

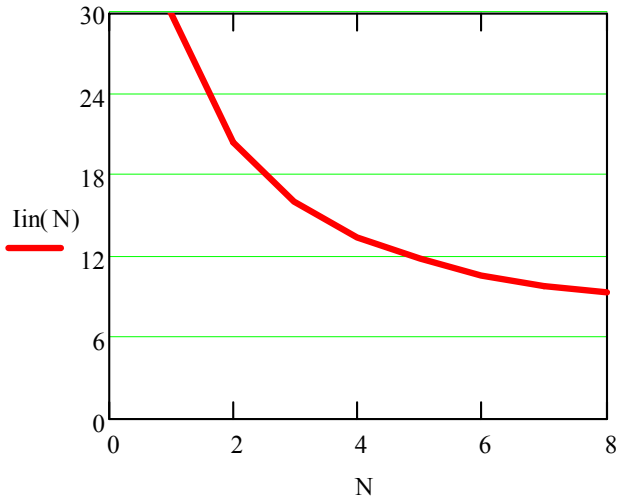


Figure 1-7. Input current vs. phase number.

1.2 Intel Load-line and Droop Control

One of the objectives of voltage regulator design is to maintain the CPU voltage within the allowable voltage window, (V_{max}-V_{min}). The CPU voltage would correspondingly fluctuate as the load current changes during transient. A larger voltage window would allow for a more relaxed voltage regulator design, and, therefore a more cost-effective solution. In a conventional design, the nominal voltage is typically positioned midway between V_{min} and V_{max} as shown in Fig. 1-8, maintaining a current-independent voltage level and leaving only half of the voltage window for either the transient voltage overshoot or undershoot [9]. The load-line and constant output impedance concepts are proposed by Intel in an effort to improve the transient response of voltage regulator [9] [10] [11]. Compared to the half usage of the window shown in Fig. 1-8, the entire voltage specification window is fully utilized, as shown in the transient waveforms for output voltage and current in Fig. 1-9. Load-line keeps V_O high when I_O is low, anticipating a

voltage droop when the current ramps up and thereby leaving the entire window for undershoot. Similarly, load-line maintains voltage low (slightly above V_{min}) at maximum current anticipating a subsequent voltage overshoot. As a result, if the power stage parameters and the control loop response time is the same, with load-line the allowable voltage deviation is effectively twice the amplitude of that without load-line, although the two cases have exactly the same V_{min} and V_{max} specifications. Therefore, load-line can significantly reduce the cost of the voltage regulator solutions by reducing the number of output capacitors. Furthermore, by positioning the CPU voltage close to V_{min} when the load current is high, the CPU's power consumption, which is proportional to $C*V^2*f$, is also reduced, where C is the lumped capacitance of all logic gates of CPU, V is the CPU supply voltage, and f is the clock frequency. To achieve load line, instead of regulating the output voltage constant, the CPU voltage will droop linearly as the load current increases if load-line is applied, as shown in Fig. 1-10, resulting in constant output impedance for the voltage regulator. This voltage-current relationship needs to be satisfied not only at static conditions, but also during transients. As the CPU changes its current during operations, the voltage delivered to the CPU would change accordingly. The equivalent circuit for a voltage with load-line is shown in Fig. 1-11, where R_O is the output impedance in serial with the load. As the load current increase, the voltage drop on output impedance causes the output voltage to droop.

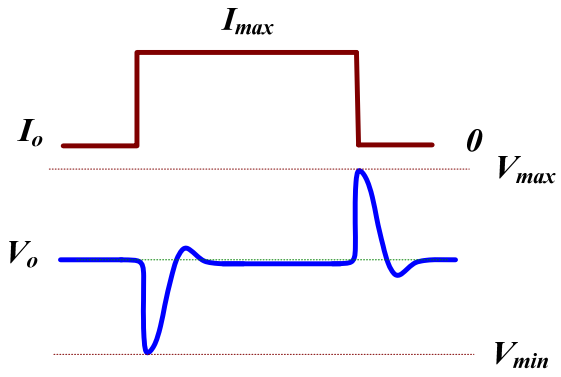


Figure 1-8. Transient waveforms for output voltage and current without load-line.

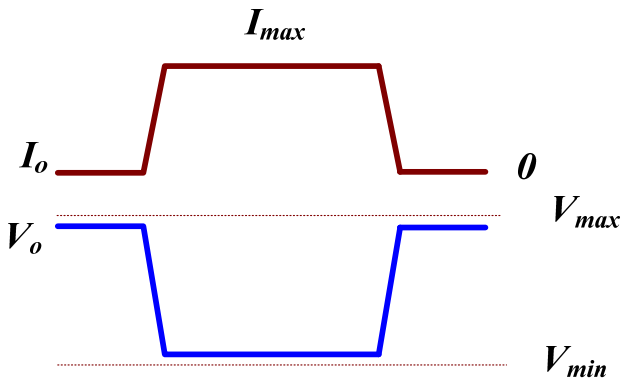


Figure 1-9. Transient waveforms for output voltage and current with load-line.

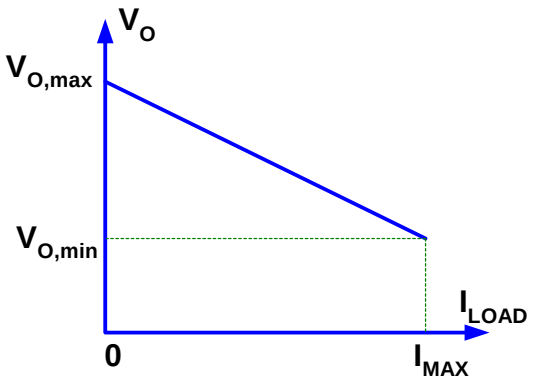


Figure 1-10. Intel load-line.

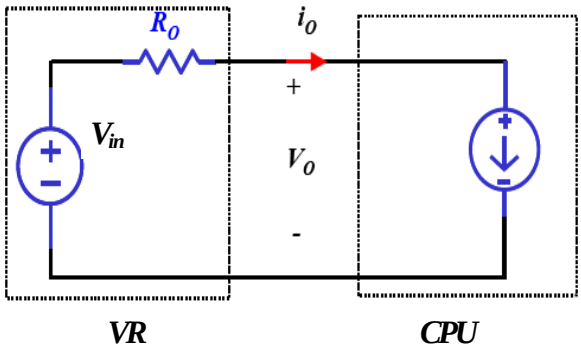


Figure 1-11. Equivalent circuit of VR with load-line.

In order to implement Intel's load-line requirements, droop control, also referred to as adaptive voltage positioning (AVP) in [1-3], is popularly accepted in the V_{core} voltage regulation to achieve a more cost-effective transient-load goal. A basic approach to carry out the droop control is to feed the sensed inductor current to the negative input of the error amplifier and develop a voltage drop across the feedback resistor. The implementation block diagram of droop control is shown in Fig. 1-12. The inductor current, i_L, is sensed and fed to the error amplifier, with K_i

being the current sense gain. This sensed current, K_i*i_L, flows through Z_{FB} and develops a voltage drop across Z_{FB}, resulting in reduced output voltage under increased load current.

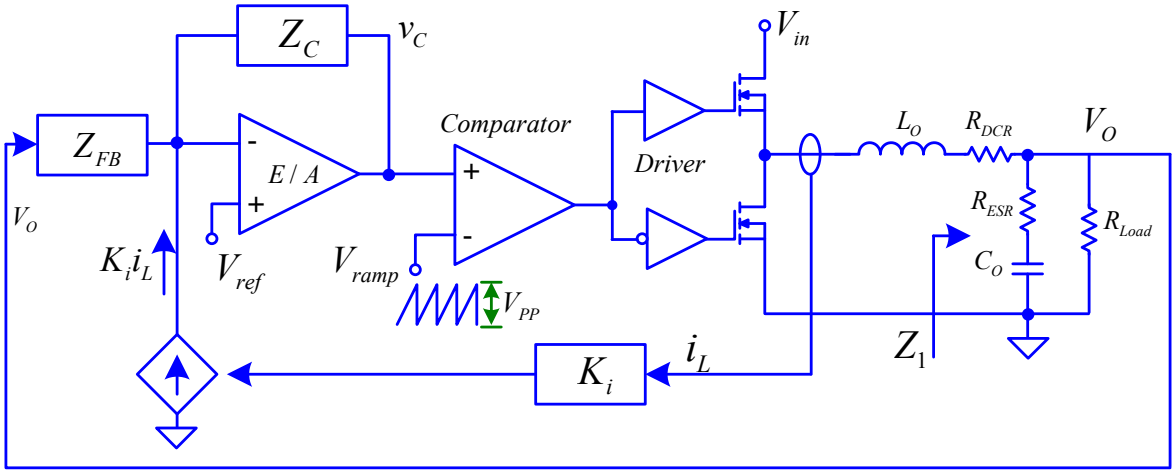


Figure 1-12. Implementation block diagram of VR with droop control.

1.3 Challenges of Transient Response

Next generation microprocessor (V_{core}) requirements for high current slew rates and fast transient response together with low output voltage have posed great challenges on voltage regulator (VR) design. These challenges are mostly resulted from the continued improvements in CPU design and application software. The CPU load current has become faster, unpredictable and more dynamic than ever. According to the latest Intel VR11 design guidelines [2], the operational current may ramp up to 140A with typical voltages in the 1.0V to 1.4V range, while the slew rate of the transient current can be as high as 1.9A/ns as shown in Table 1.1.

Table 1-1. Intel processor current step values for transient socket load line testing [2].

VR Configuration	Starting Current	Ending Current	Dynamic Current Step	Icc Rise Time
775_VR_CONFIG_04A	23 A	78 A	55 A	83 A/µs
775_VR_CONFIG_04B	24 A	119 A	95 A	83 A/µs
775_VR_CONFIG_05A[1]	20 A	85 A	65 A	50 ns
775_VR_CONFIG_05B[1]	30 A	125 A	95 A	50 ns
775_VR_CONFIG_06[1]	25 A	75 A	50 A	50 ns

Meanwhile, the transient-response requirements are becoming stringer and stringer. For VR11 specifications, the output voltage needs to be within the specified window as shown in Fig. 1-13. And the voltage regulator needs to be unconditionally stable under all specified output voltages, load current transients of any duty cycle, and repetition rates of up to 1 MHz as shown in Fig. 1-14. In addition, the maximum overshoot allowed above VID is only 50 mV within 25 uS time duration [2].

If not well managed, the highly dynamic load transients may cause the VR output voltage to go beyond the specified regulation band and manifest the overshoot and undershoot which can ultimately limits the CPU operating speed. It is further compounded by the reduced noise margin in the CMOS logic circuits that result from power supply voltage scaling. While voltage overshoots may cause the CPU's reliability to degrade, undershoots may cause malfunctions of the CPU, often resulting in the "blue screen".

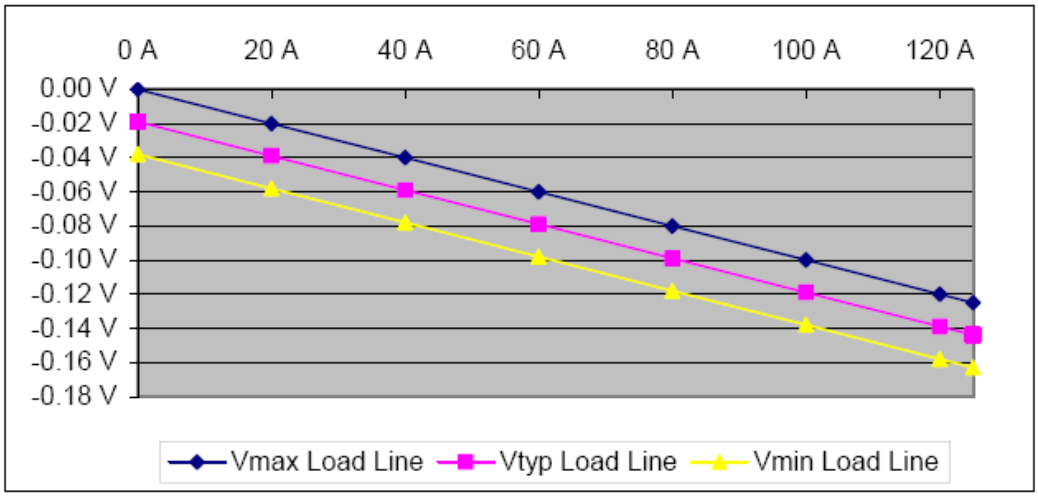


Figure 1-13. Socket Loadline Window for 775_VR_CONFIG_04B, 05A, 05B (0-100 kHz load step rate) [2].

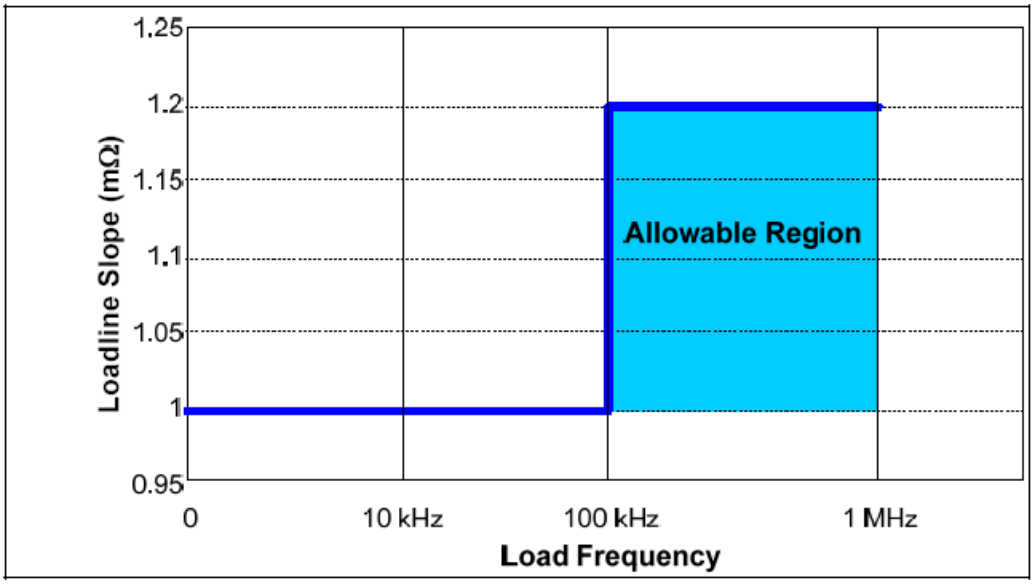


Figure 1-14. Piece-wise Linear Socket Loadline [2].

For an ideal operation of voltage regulator, the output voltage should respond to the changes in load current immediately. However, the delay of the compensation network and output filter may

deteriorate the output voltage waveform. Fig. 1-15 shows the output filter model of multiphase voltage regulators. Both the output bulk capacitors and ceramic capacitors include equivalent series resistance (ESR) and equivalent series inductance (ESL). Fig. 1-16 shows current waveforms of the output filters during load transients. From top to bottom, the waveforms represent load current, current of ceramic capacitors, current of bulk capacitors, and inductor current. When load current steps up at a high slew rate, the compensation loop cannot respond immediately due to control delay. Thanks to their lower ESR and ESL than the bulk capacitors, the ceramic capacitors will be the first supplier of the load current. Following the ceramic capacitors, the bulk capacitors will discharge to meet with the current's demand. As a result of the discharging, voltage undershoot will be seen at the output. The magnitude is dependent on the total number of output capacitance, ESR, and ESL. As soon as the control loop detects this voltage undershoot, it will try to compensate the voltage deviation by turning on the upper MOSFETs. However, since the charging slew rate of the inductor current is limited by the inductance and the input-output voltage difference, it will take a while for the inductor current to reach the demanded load current level. Due to the inductor charging delay, there is a current difference between the inductor current and the load current. The output capacitors will continue discharging in an effort to satisfy the load demand. The discharge process leads to more undershoot of output voltage as shown in Fig. 1-17.

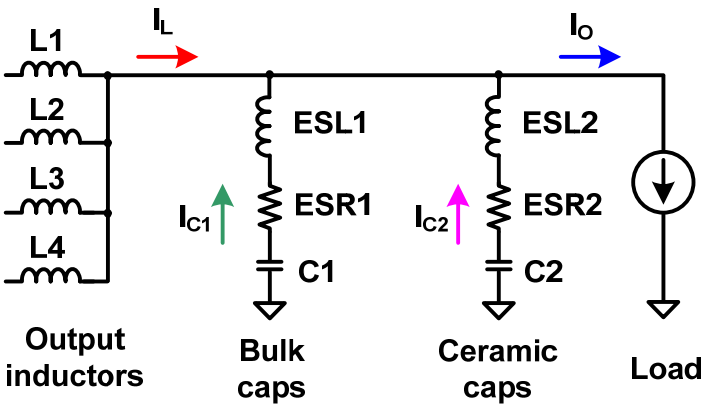


Figure 1-15. Simplified output filter model of multiphase VRs.

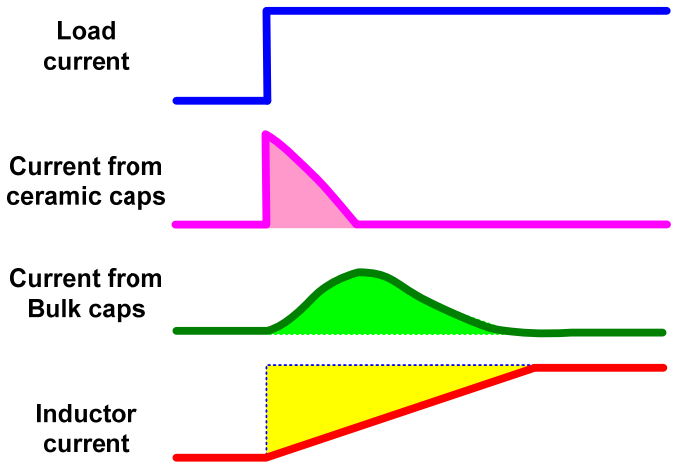


Figure 1-16. Current waveforms of output filters during step-up load transient.

In an opposite way, the output voltage sees overshoot during a load step-down transient. Again, due to the control delay, the upper MOSFETs cannot be turned off immediately. As a result, the inductors continue to charge the output capacitors even though the load step-down is complete. The overcharge of the output capacitors then causes output voltage overshoot. At the time when the control loop responds to the output overshoot, the upper MOSFETs will be shut off.

However, due to the fact that the discharging slew rate of the inductor current is determined by the inductance value and the output voltage, extra energy stored in the output inductors will keep charging the output capacitors. At this moment, the output voltage is dictated by the output filters. The inductor discharging continues to worsen the output voltage deviation as shown in Fig. 1-17.

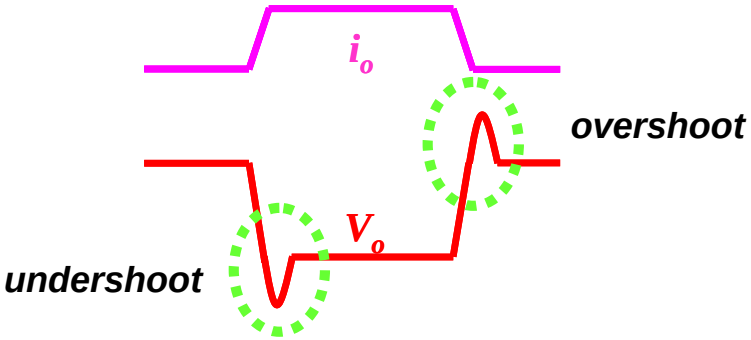


Figure 1-17. Undershoot and overshoot of output voltage during load transients.

From the above discussion, it is concluded that transient response is constrained by output inductance, output capacitance, ESR, ESL, and compensation design.

1.4 Review of Prior Arts

As addressed in the previous chapter, although multiphase converters with droop control have become common practice in VR industry and show advantages in transient response, removing

undesired voltage spikes and dips during large load changes remains a big challenge for VR designers, due to the constraints of transient response.

Much effort has been put forth, such as application of novel topologies, advanced devices and control schemes to meet the stringent V_{core} specifications for transient response. Currently, there are two main solutions to transient voltage spike suppression. One is to reduce the ESR and ESL by paralleling more output capacitors. While the main functions of output capacitors are to filter switching ripple and handle transient response, with multiphase interleaving operation helping to reduce the ripple of the current that flows into the output capacitors, transient response is a more dominant consideration for output capacitors as discussed before. However, this method always suffers from increased system cost and limited footprint, since output capacitors are the most important part in total size and cost. For these reasons, there is a strong incentive to reduce the amount of output capacitors.

The other approach is to extend the bandwidth of VR. Based on the feedback control theory and the investigation in [12] [13] [14], the higher the closed-loop bandwidth in frequency domain, the faster the system will respond to transients in time domain. Therefore, theoretically pushing bandwidth as high as possible is a viable approach to improve transient response. Based on the circuit block diagram shown in Fig. 1-12, a simplified small-signal control block diagram of a multiphase buck with droop control can be obtained as shown in Fig. 1-18, where $Z_O(s)$ is the power stage open-loop output impedance. $G_{vd}(s)$ is the transfer function of output voltage to the duty cycle d. $G_{ii}(s)$ is the transfer function of inductor current to load current. $G_{id}(s)$ is the

transfer function of the inductor current to the duty cycle d. $F_m(s)$ represents the modulation gain. R_{droop} is the targeted load-line resistance, and $A_v(s)$ is the voltage loop compensator transfer function. If the output current variation is neglected, then the current loop can be represented by the red lines and the voltage loop can be represented by the blue lines. According to the block diagram, the current loop gain $T_i(s)$ can be given by:

$$T_i(s) = R_{droop} \cdot A_V(s) \cdot F_m \cdot G_{id}(s) \tag{1-4}$$

With the current loop open, the voltage loop gain $T_v(s)$ is expressed as:

$$T_V(s) = A_V(s) \cdot F_m \cdot G_{vd}(s) \tag{1-5}$$

If the current loop is closed, the voltage loop gain $T_2(s)$ can be given as below:

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)} \tag{1-6}$$

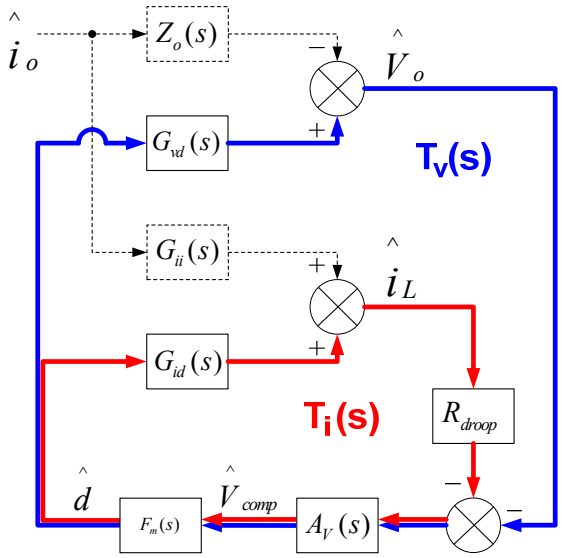


Figure 1-18. Small-signal block diagram of multiphase VR with droop control.

It is found from Fig. 1-18 that the control bandwidth is specifically the bandwidth of voltage loop $T_2(s)$. If the power stage is determined, then by tweaking the compensator $A_v(s)$, the system bandwidth can be extended. Since the transient performance depends on the closed loop bandwidth, the transient response obtained from the system with a higher switching frequency is potentially better than that with a lower switching frequency. Thus, to obtain a high bandwidth design, one has to push the switching frequency high. However, the maximum system bandwidth is limited by the switching frequency F_s: it is hard to push the bandwidth of the closed loop to above half of the switching frequency which is defined by Nyquist Theorem [15]. At the same time, increasing switching frequency posts new trade-offs between performance and overall system cost: higher power loss led by higher switching frequency requires extra heat removal

components and higher-rating devices, which may sacrifice the benefits brought on by increased switching frequency.

While some people seek for solutions to improve the transient performance in terms of linear control, others resort to non-linear control methods. Among the nonlinear solutions, there are two distinguished ways. They include those in which the non-linear control operates all the time like hysteretic control and V^2 control [16], and those in which the non-linear control works in a short period of time [17]. The hysteretic control (or two-state, bang-bang, ripple, free-running regulator, etc.) is a very simple solution that does not require the compensation circuitry and has good dynamic characteristics. Fig. 1-19 shows a buck converter with hysteretic control. Different from other conventional control methods, this controller does not have a conventional compensation loop. Therefore, it is able to respond to the load transient in the switching cycle when the transient occurs. The only delays this control method has during transient are the delay in the hysteretic comparator and the turn-on and turn-off delays in the driver. The high-frequency noise filter in the input of the comparator may add some additional delay. However, those delays depend mostly on the level of the selected technology, so the hysteretic control is theoretically the fastest solution. The other advantage of the hysteretic controller is that its duty cycle covers the entire range from zero to one. The main disadvantages of hysteretic control are its sensitivity to noise and variable frequency control.

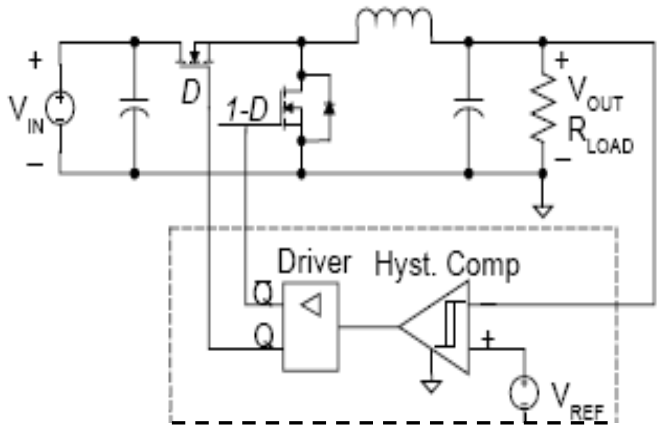


Figure 1-19. Block diagram of hysteretic control [16].

The V^2 mode control, as shown in Fig. 1-20, also has very fast transient-response characteristics, but it has drawbacks in its original implementation. This controller uses the output-voltage ripple as the ramp signal of the modulator. It is assumed that the voltage ripple of the output capacitor depends mostly on the ESR, while the part of ripple caused by the ESL and output capacitance is negligible. In this case the ripple is proportional to the inductor current ripple. At transients, this voltage carries the information about the load-current change directly to the comparator, bypassing the slow main feedback loop. The V^2 mode control actually can be defined as a sort of hysteretic control having an additional error amplifier. This amplifier enables an increase of the hysteresis window of the comparator without degrading the accuracy of the output voltage. On the other hand, the use of output ripple voltage as the ramp signal causes the stability to depend greatly on the output capacitor parasitics. This dependence is especially problematic when using many high-frequency ceramic or film capacitors in parallel as the output filter. In this case, the equivalent output capacitor is almost ideal, because its parasitics are negligible and an output ripple has a parabolic waveform instead of a linear ramp.

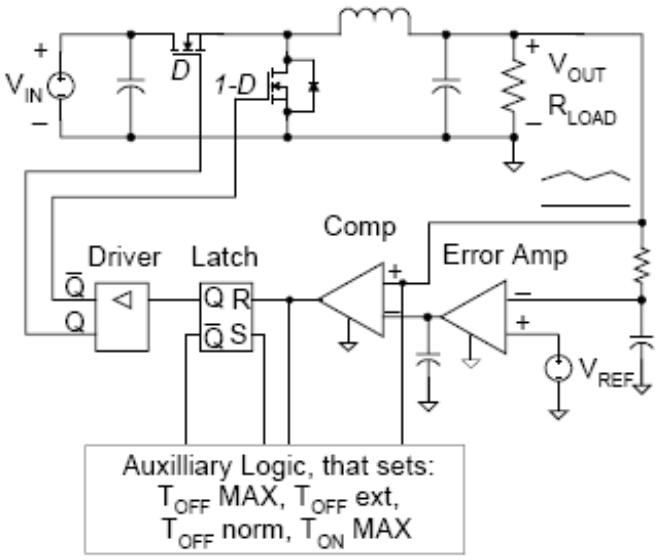


Figure 1-20. One of the implementations of V2 mode control [16].

The Linear-Non-Linear control idea and its operational principle are proposed in [17]. It belongs to those converters in which the Non Linear control works in a short period of time, along the switching period, modifying the control gain of the converter.

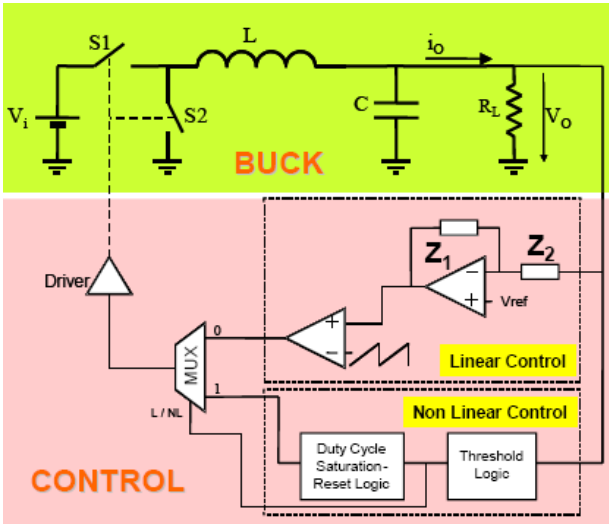


Figure 1-21. Buck converter with Linear and Non-linear control [17].

Fig. 1-21 shows an example of the LnLc control. A threshold logic block will determine if the output voltage is within the specification window or not. When V_O is inside the threshold band the LnLc control works like a linear control, maintaining the converter stability and low output voltage ripple; when the V_O goes out the threshold band, the LnLc control block is triggered and reacts drastically against the perturbation produced by the load current steps, removing it, and, at the same time, improving the stability of the whole converter. At the time when the converter with linear control becomes unstable, the LnLc control is able to stabilize it; if the converter with linear control becomes totally unstable the LnLc control is able to stabilize it as well, operating like a hysteretic control.

For some nonlinear control schemes, an auxiliary circuitry is employed. Fig. 1-22 shows a schematic of the single-shot-transient-suppressor (SSTS) proposed in [18]. The main idea of the

SSTS is to use auxiliary decoupling capacitors, charged to higher voltage, to store the extra charge required by the CPU during the step up transient. The extra charge can then be delivered to the processor in a single shot manner, bypassing the slower VRM. In the same way this circuit can sink the excess of charge that has to be removed during the step down transient.

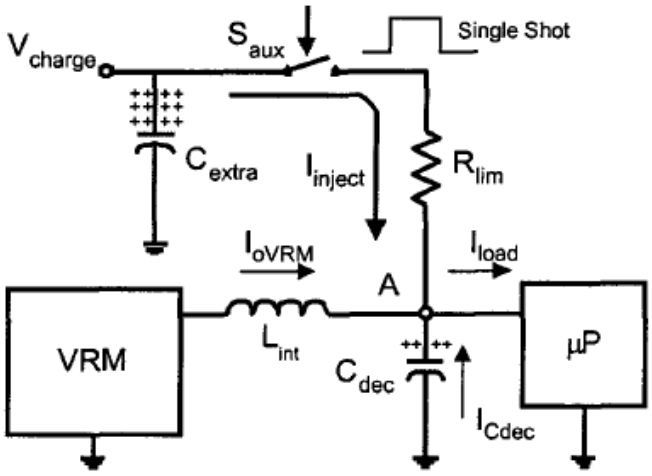


Figure 1-22. Single shot transient suppressor [18].

In [19], a fast-response-double-buck (FRDB) is proposed. The FRDB has an auxiliary buck converter connected in parallel, and controlled by means of the linear-non-linear control [17] as shown in Fig. 1-23. The goal of this converter is to reduce the recovery time of the output voltage during transient, and limit the variation of the output voltage while guaranteeing the stability of the converter. The operation principle is to keep the main switching converter operating at all times, enabling the auxiliary switching converter only at the edges of the load current steps. In this way, the auxiliary converter facilitates the transient events.

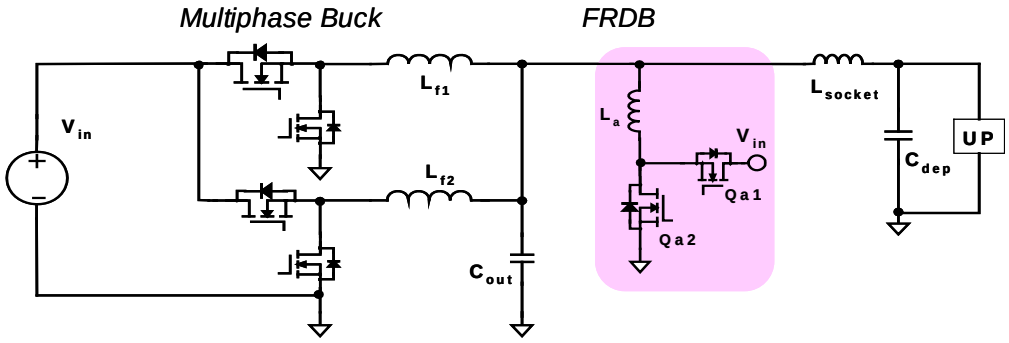


Figure 1-23. Topology of the Fast Response Double Buck [19].

In [20], Consoli proposed a low-inductance-current-path (LICP) topology. It features a quite conventional multiphase section, similar to a multiphase buck converter, parallel connected with an additional switch, providing a very low inductance path, as shown in Fig. 1-24.

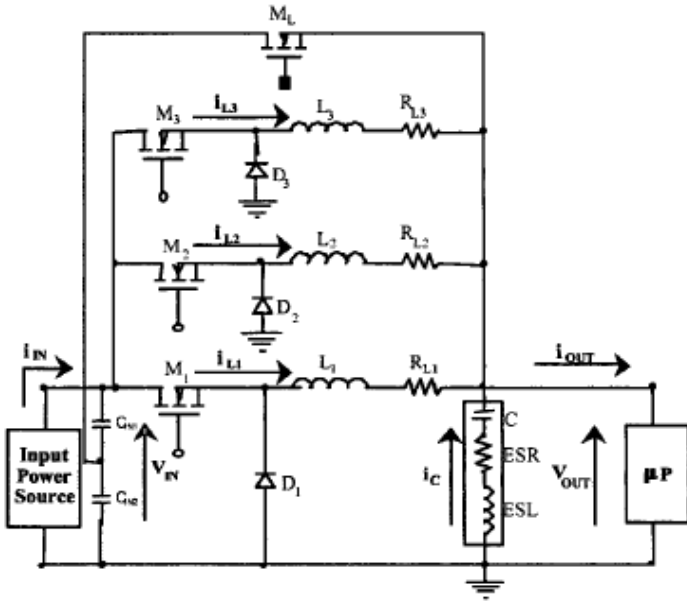


Figure 1-24. Topology of the Low Inductance Current Path [20].

The auxiliary circuitry is activated only if large load variations are detected in order to limit output voltage falls, while the standard multiphase converter is used as the main power processor. The LICP takes advantage of the high efficiency of the main switching converter, and the high slew-rate capability of the additional low inductance current path. Moreover, the additional switch is activated only in case of large current transients, and only slightly affects the efficiency of the whole system. The introduction of the additional low inductance path serves to largely reduce the discharge of the output filter capacitor during load release transients, thus minimizing the effects of capacitor stray impedances.

Poon proposed a stepping inductance scheme in [21]. As shown in Fig. 1-25, two inductors are connected in series to replace the output inductor of a voltage regulator in the stepping inductance method, one inductor with a larger inductance and the other with a smaller inductance. In steady state operation, the inductor with larger inductance is enabled. As a result, the total current ripple as well as the conduction losses is minimized. During load transient, the smaller inductor will take over, in a way to speed up dynamic response.

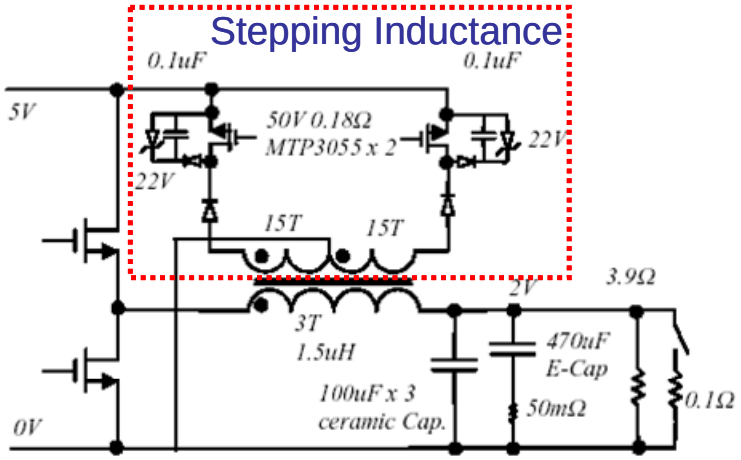


Figure 1-25. Topology of the Stepping Inductance [21].

A transient voltage clamp (TVC) method is presented in [22] to clamp the output voltage variation during step load transient. The typical application circuit of TVC is shown in Fig. 1-26 while the simplified TVC circuit is shown in Fig. 1-27. The TVC works in parallel with a voltage regulator (VR)'s ceramic cap and is claimed to be able to achieve a faster voltage regulation without huge bulk capacitor. TVC is designed based on output impedance analysis. The concept is, if the output impedance of TVC is equal to the bulk capacitor's output impedance, then the proposed TVC works as a solid state replacement of the bulk cap. If TVC has the same output impedance as the bulk capacitor and it covers the frequency range between f_C and f_{ESR}, then the close-loop output impedance can be constant from DC to high frequency.

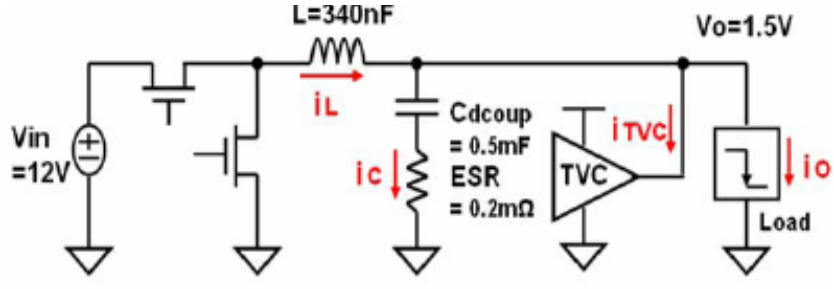


Figure 1-26. Typical application circuit of TVC [22].

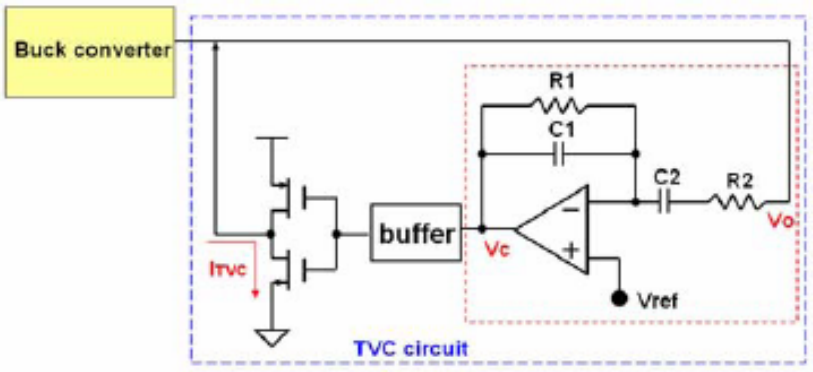


Figure 1-27. Simplified TVC circuit [22].

In [23], a current amplification and absorption technique is proposed to speed up transient response. A buck converter with the proposed current amplification and absorption technique is shown in Fig. 1-28. This technique claims to be less loss, low cost and easy to implement with simple control scheme. The complete application can be modified from a basic buck topology by replacing the output inductor with two magnetically coupled inductors. The two coupled inductors have different inductance values. The inductor with smaller inductance will take over the output inductor during step-up load transient. It speeds up the output current slew rate and reduces the output voltage drop during the step-up load transient. The additional capacitor, which

is parallel connected to the coupled inductor, will suppress the over-shoot of output voltage during the step-down load transient. A diode D1 is used to prevent the reverse current flow at the step-up load transition.

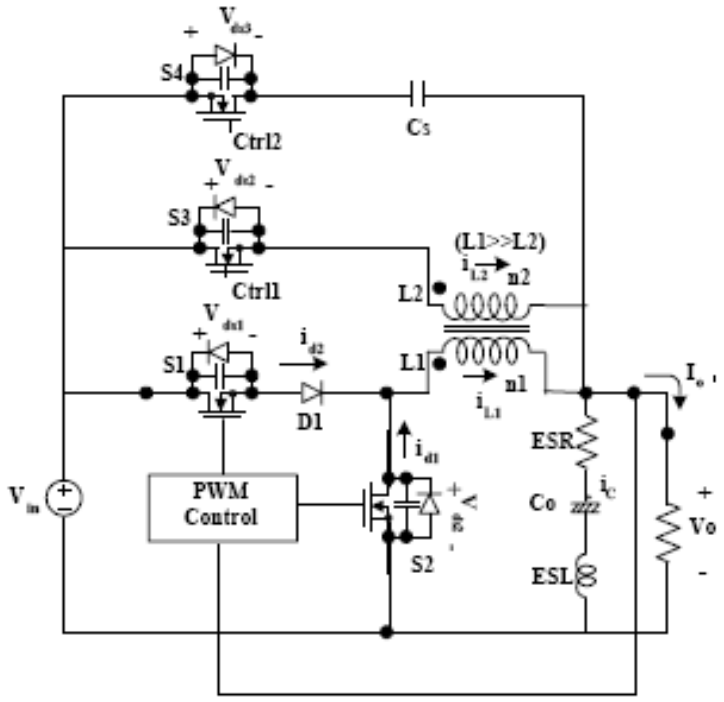


Figure 1-28. Buck converter with current amplification and absorption technique [23].

1.5 Dissertation Outlines

Chapter 1 introduces the background of this work. It first introduces multiphase voltage regulators and Intel load-line as well as droop control. Henceforth, it discusses the challenges of transient response for CPU VR regulation. This chapter concludes with a brief review of the main research work that has been done on transient response improvement.

In Chapter 2, Frequency-domain analysis reveals why high-bandwidth design is hard to achieve in practice. An adaptive modulation control (AMC) scheme is proposed. AMC enables VR designers to design power supplies with extremely high bandwidth in steady state. The bandwidth is lowered while in heavy load transients where the loop could be potentially unstable. Therefore, the AMC provides an optimal means for robust high-bandwidth design with excellent transient performance. Time domain investigation further suggests that AMC is capable of improving transient response by reducing the voltage ringing back. Simulation and experimental results are given in the end.

Chapter 3 offers an error amplifier voltage positioning (EAVP) method. How to remove the voltage-undershoot during load step-up and overshoot during load step-down is always a big challenge for VR designers. With large load transient, the output voltage of the error amplifier is usually driven to saturation level, due to the fact that the R and C in the compensation network will try to hold to their original voltage. While conventional methods struggle to increase the control bandwidth, the EAVP facilitates the error amplifier recover from its saturation status. As a result, the PWM turn-on and turn-off delays are both reduced, achieving a fast transient response. Since it works only during transient, it does not change the circuit configuration nor the control loop gain.

Chapter 4 addresses multiphase voltage regulators with coupled inductors. This chapter starts with the fundamentals of coupled inductors. In most literature, the voltage regulator with coupled

inductors is simplified to the conventional topology with leakage inductor per phase representing the coupled inductors, while the magnetizing inductance is ignored. In order to explore the effects of magnetizing inductance on VR, a unified state-space-averaging model of VR with coupled inductors is built with the magnetizing inductance being taken into account. In terms of the DC solutions, VR with coupled inductors is identical to VR with discrete inductors. The magnetizing inductance has no effect. However, the small-signal solution of the power stage suggests that the magnetizing inductance decreases the LC double-pole frequency if the coupled inductors are not identical. Following the state-space-averaging analysis, the limitations of conventional DCR current sensing method for coupled inductors are addressed. Then, two novel DCR current sensing topologies are presented. Unlike conventional DCR current sensing method, they are able to preserve the coupling effect of multi-phases. As a result, the phase currents as well as the total current can be accurately sensed if the topologies are designed properly. Motivated by the challenging transient and efficiency requirements, this chapter proposes a new voltage regulator with coupled-inductors which is able to improve transient response as well as savor high efficiency. The idea is to change the circuit configuration depending on different operational modes. Detailed operational principles and simulation results are given at the end.

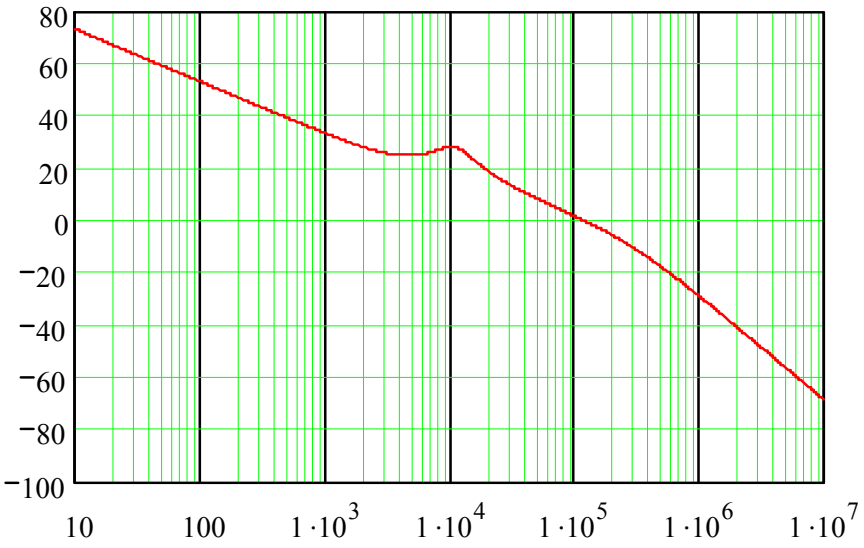
Chapter 5 introduces a new magnetics design methodology. The new methodology features intensive usage of simulation tools Maxwell 2D and 3D. While discrete magnetics components are employed as design examples throughout this chapter, this methodology can be applied to coupled-inductor design.

Chapter 6 presents an active compensator for dynamic voltage scaling. This compensator generates an offset current for the compensation network in an effort to cancel its effects on output voltage deviation during dynamic voltage transition. Since it works only during DVS, no output filter and compensation change is necessary. Simulation and experiment results show that it is a practical and effective solution to the problems encountered in DVS.

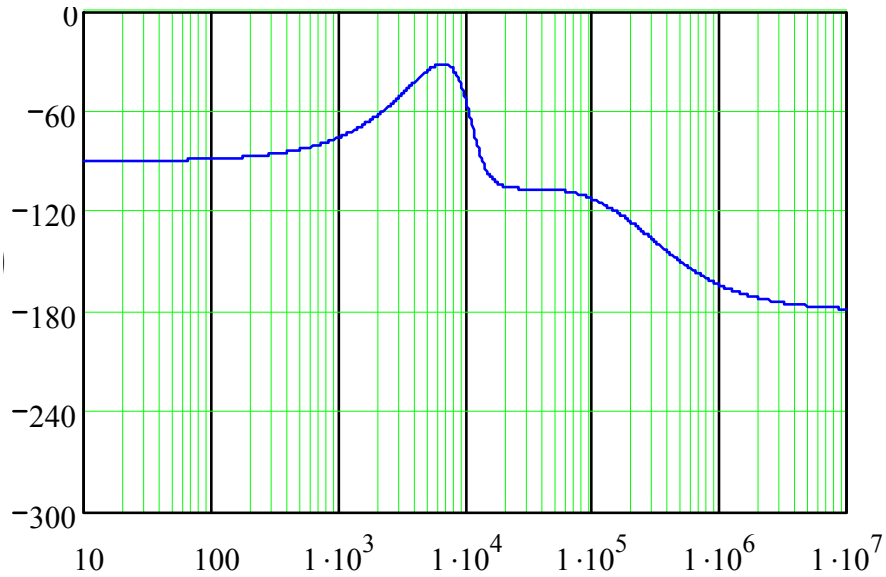
CHAPTER 2 ADAPTIVE MODULATION CONTROL

2.1 Limitations of Conventional Average Model

Traditionally, most of the feedback controller designs have been based on the average model for buck converters [24] [25]. A multiphase buck is simplified to a single-phase buck converter in the average model. However, the switching frequency plays an important role in the loop gain at the high-frequency region [27] [28]. And the highest achievable bandwidth is related to the switching frequency as discussed in Chapter 1. Since the method of the average model is based on the state-space averaging which eliminates the inherent sampling nature of a switching converter, the accuracy of the average model is questionable at frequencies approaching half of the switching frequency [27] [28]. Fig. 2-1 shows the Bode plots of a two-phase buck converter with phase frequency of 300 kHz using average model, while Fig. 2-2 shows the simulated Bode plots by switching model with Simplis simulator. Carefully comparing the results from the average model and switching model, it is found that the average model agrees with the switching model up to the bandwidth which is 100 kHz for both the gain and the phase. However, excessive phase drop is seen beyond the bandwidth from the switching model, which cannot be predicted by the average model. Therefore, for a high bandwidth design, the phase delay may result in a system stability issue if the controller design is based on the average model.

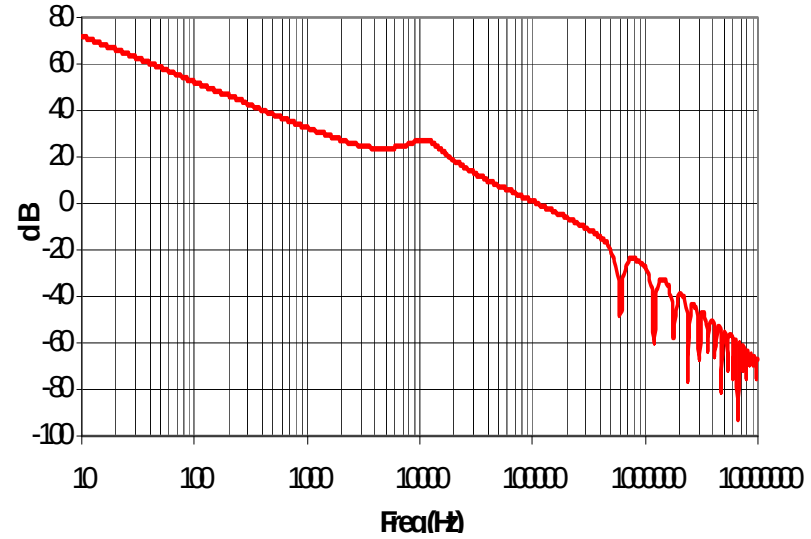


(a) Gain

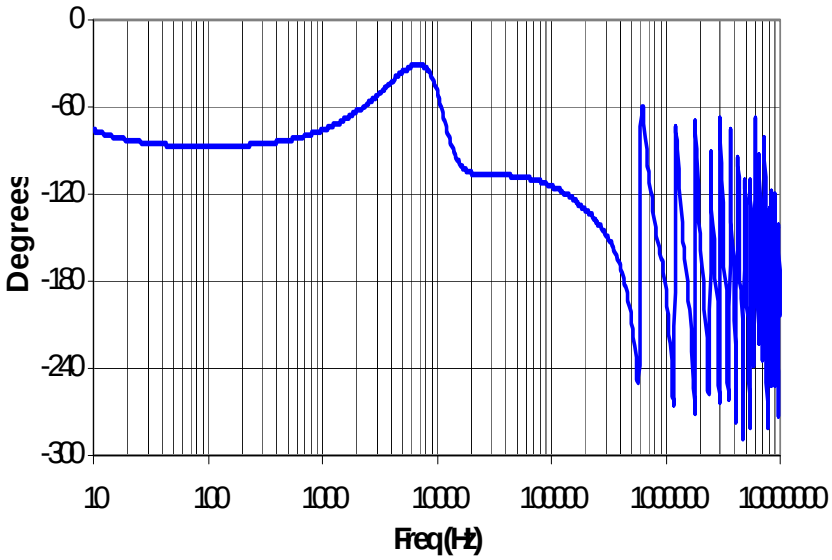


(b) Phase

Figure 2-1. Bode plot for a two-phase buck converter with average model.



(a) Gain



(b) Phase

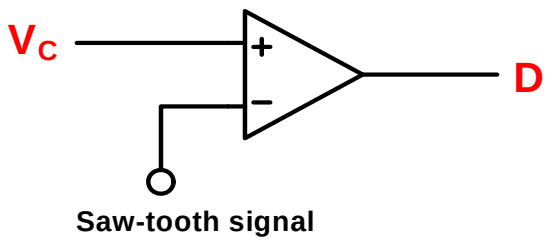
Figure 2-2. Bode plot for a two-phase buck converter with Simplis simulation.

For more than a decade, researchers have been extending small-signal models of switching power converters to predict frequency response at frequencies approaching and beyond half the

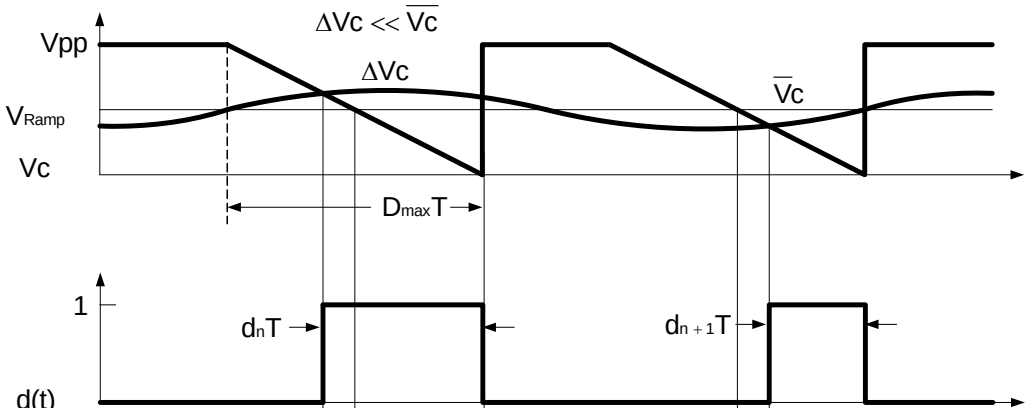
switching frequency [29-34]. Early work [27] in sampled-data modeling involved determining control-to-output frequency responses of pulse width modulated (PWM) converters. Subsequent work [29-34] extended this modeling method to encompass a general range of converters and further allowed determination of input-to-output responses. These efforts have focused on small-signal models for both average and switching characteristics. Reference [33] examined the accuracy of various models for current-mode control, especially considering the effects of time variation on small-signal modeling. The paper reiterated cautions previously risen in [34] regarding the interpretation of frequency response results for the extended frequency range in the presence of aliasing effects.

2.2 Sampling Effects of PWM Modulation

Fig. 2-3 (a) shows a typical PWM modulator diagram and Fig. 2-3 (b) shows its operational waveforms, where V_C is the output voltage of the error amplifier, V_{ramp} is the saw-tooth signal, and D is the duty cycle. The PWM signal is produced when V_C is compared to the saw-tooth signal. Fig. 2-4 shows a conventional small-signal average model. It is found that the modulator is modeled as a proportional gain block G_m in the whole loop as circled by the red dash line. However, by simplifying the modulator into a gain block, its sampling nature, (i.e. high frequency harmonics in the error amplifier output voltage) are neglected. Therefore, the conventional model cannot predict high frequency transient response.



(a) PWM modulator diagram.



(b) Operational waveforms.

Figure 2-3. PWM block diagram and operational waveforms.

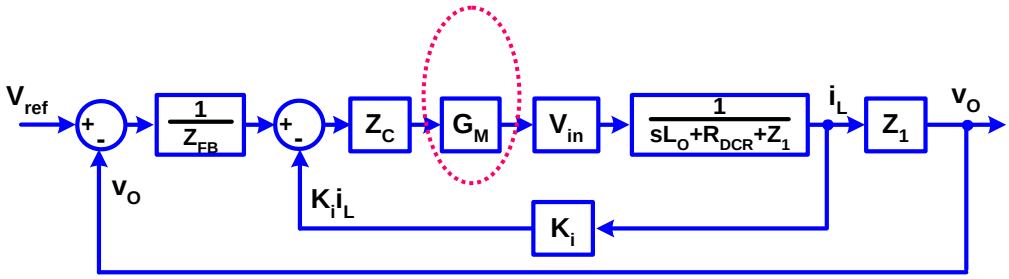


Figure 2-4. Simplified closed-loop diagram of voltage regulator with droop control [1].

If considering the sampling effects of the modulation, the PWM modulator can be modeled as shown in Fig. 2-5.

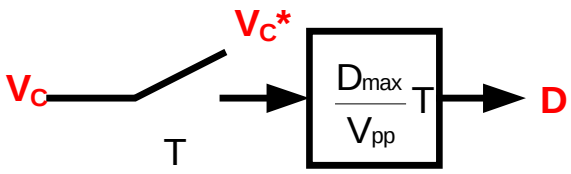


Figure 2-5. PWM modulator with sampling effect.

Where V_C* is the sampled V_C.

To investigate the sampling effects of the PWM modulation, the sampled V_C needs to be reconstructed and approximated in frequency domain for loop analysis purpose. Mathematically, the sampling process can be expressed by

$$Vc^*(t) = Vc(t) \cdot T \cdot \sum_{n=0}^{\infty} \delta(t - nT) = T \cdot \sum_{n=0}^{\infty} Vc(nT) \cdot \delta(t - nT) \tag{2-1}$$

Where T is the switching period and δ is the dirac impulse function. However, this discrete time signal cannot be readily transformed into s-domain for loop analysis purpose. In DSP, outputting a sequence of dirac impulses is decidedly impractical; therefore, most conventional DACs output a voltage proportional to the discrete sampled value and hold that voltage to a constant value for the duration of the sampling interval and then change that voltage rapidly to the value corresponding to the next discrete sample value [15]. Thus, a zero-order hold (ZOH) is the hypothetical filter or LTI system that can convert the ideally sampled signal to the piecewise

constant signal. The sampled output voltage of the error amplifier can be expressed as summation of a train of discrete voltages:

$$Vc_{ZOH}(t) = \sum_{n=0}^{\infty} Vc(nT) \cdot rect(\frac{t-nT}{T} - \frac{1}{2}) \tag{2-2}$$

where rect(x) is the rectangular function. A zero-order hold (ZOH) can be given as:

$$h_{ZOH}(t) = \frac{1}{T} \cdot rect(\frac{t}{T} - \frac{1}{2}) = \begin{cases} \frac{1}{T} & if\ 0 \le t \le T \\ 0 & otherwise \end{cases} \tag{2-3}$$

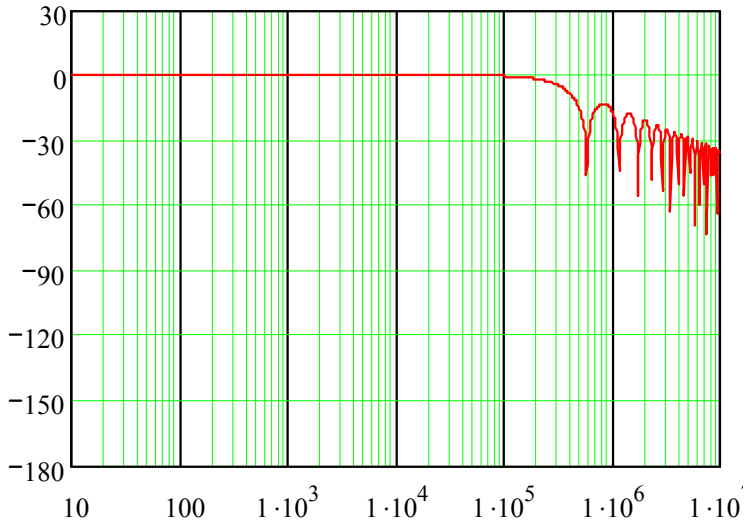
Therefore, the sampled output voltage of the error amplifier contains ZOH effects. In frequency domain, the effective frequency response of the ZOH is the continuous Fourier transform of the impulse response:

$$H_{ZOH}(f) = F\{h_{ZOH}(t)\} = \frac{1-e^{-i2\pi fT}}{i2\pi fT} = e^{-i2\pi fT} \cdot \sin c(fT) \tag{2-4}$$

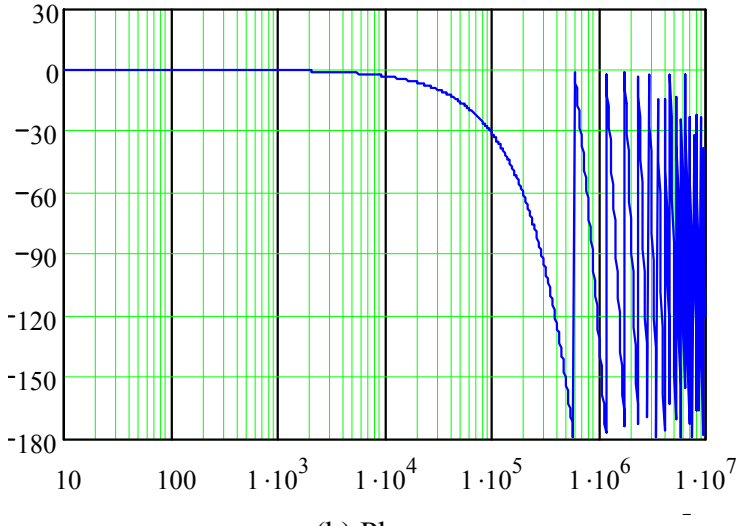
where sinc(x) is the sinc function. Since this form is not readily useful for loop analysis, the ZOH is Laplace-transformed by substituting s = i2πf. The transfer function is found as:

$$H_{ZOH}(s) = L\{h_{ZOH}(t)\} = \frac{1-e^{-sT}}{sT} \tag{2-5}$$

An example of the frequency response of ZOH is given in Fig. 2-6 to illustrate the sampling effects on loop performance. The sampling frequency (switching frequency) is 600 kHz. It is found that both gain and phase dip abruptly beyond the switching frequency, even though they are almost unit at low frequencies. Due to the presence of ZOH effects in PWM modulation, the whole loop bandwidth of a VR will inevitably be constrained by the switching frequency as shown in Fig. 2-2.



(a) Gain.



(b) Phase.

Figure 2-6. Frequency response of Zero-Order-Hold.

Based on the above analysis, it is concluded that the PWM modulation is analogous to a sample-and-reconstruction process. The Nyquist theorem states that if the system bandwidth is less than half of the sampling frequency, the uniformly distributed discrete samples are a complete representation of the signal, just as shown in Fig. 2-6, meaning that the maximum converter

bandwidth is limited by the switching frequency [15]. As a result, the transient response obtained from a VR with higher switching frequency is better than that with lower switching frequency, because theoretically the bandwidth can be designed higher with a higher switching frequency.

For multiphase voltage regulators used in low-voltage applications, the effective frequency of the output voltage ripple is equal to the product of the phase number and phase switching frequency, as shown in Fig. 1-6. Based on loop analysis, the bandwidth of multiphase voltage regulators could be pushed close to the phase-switching frequency. For some advanced control schemes like adaptive phase alignment (APA) in [26], however, all phases are turned on simultaneously to increase the current slew rate during large load-insertion transients. In this case, the effective frequency of the output ripple will be reduced to the phase-switching frequency, as shown in Fig. 2-7.

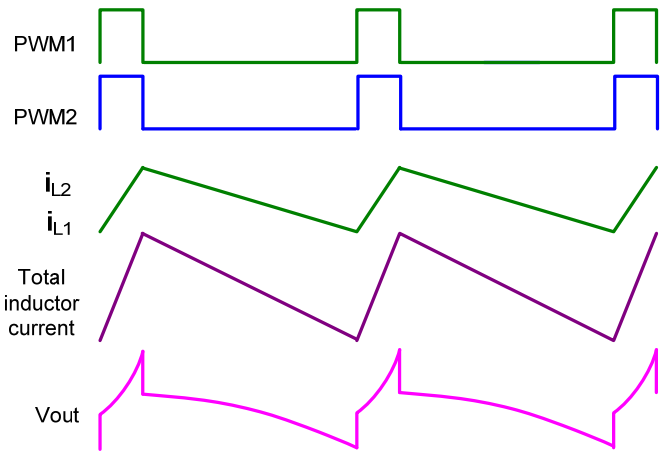
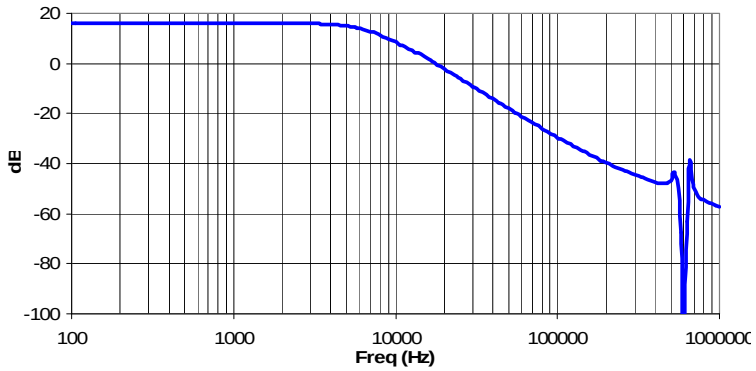


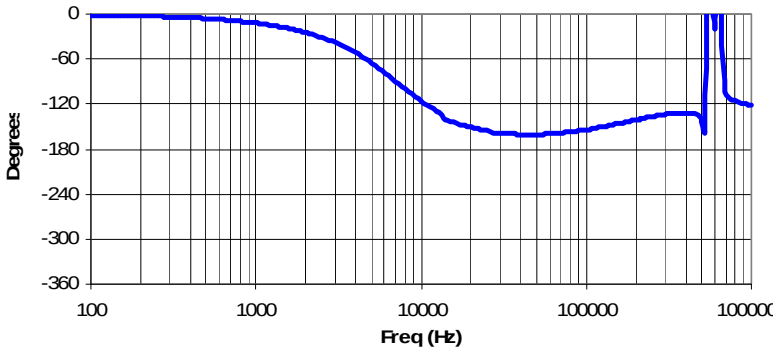
Figure 2-7. Operational waveforms of APP control with simultaneous operation.

In frequency domain, a multiphase VR with APA control during transients shows a different gain-phase relationship from a regular multiphase VR. A 300 kHz two-phase VR is employed as an example to depict the difference in frequency domain for regular operation and APA control. For a regular multiphase VR, the abrupt gain drop and phase delay caused by the aliasing effect [16] occurs at phase number times the phase-switching frequency, i.e. 600 kHz as shown in Fig. 2-8. For a VR in simultaneous operation with APA, however, the gain and phase dips occur at the phase frequency 300 kHz, as shown in Fig. 2-9. It behaves like a single-phase voltage regulator. With a high bandwidth design, this can be disastrous if care is not taken: sideband components induced by the aliasing effect can result in system instability [28].

Motivated by the demand for a control method which is able to facilitate a high-bandwidth design as well as stabilize the loop during large load transients, adaptive modulation control (AMC) is proposed in [8].

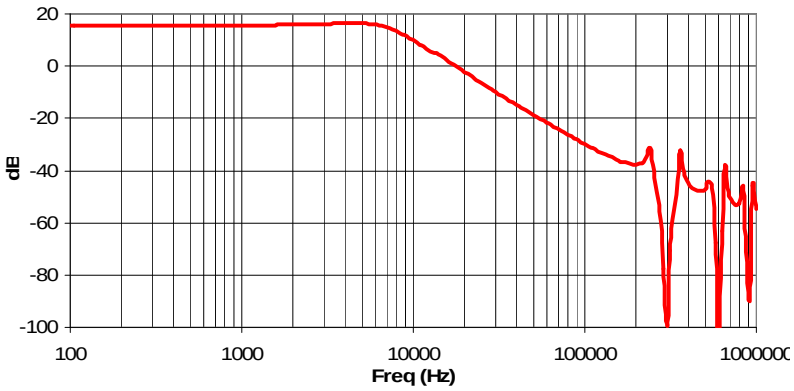


(a) Gain for interleaved operation.

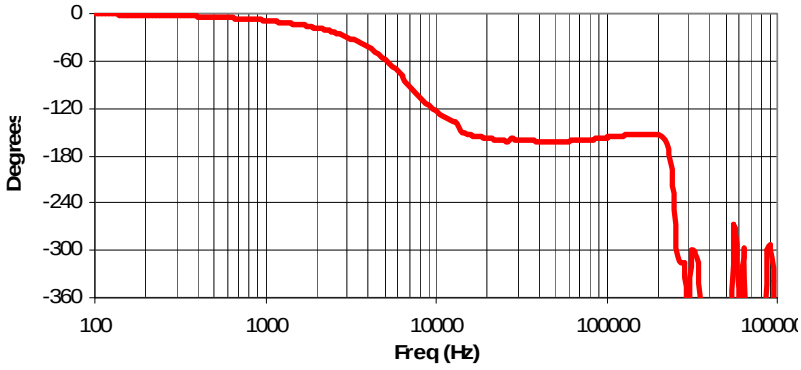


(b) Phase for interleaved operation

Figure 2-8. Power stage transfer function interleaved operation.



(a) Gain for simultaneous operation

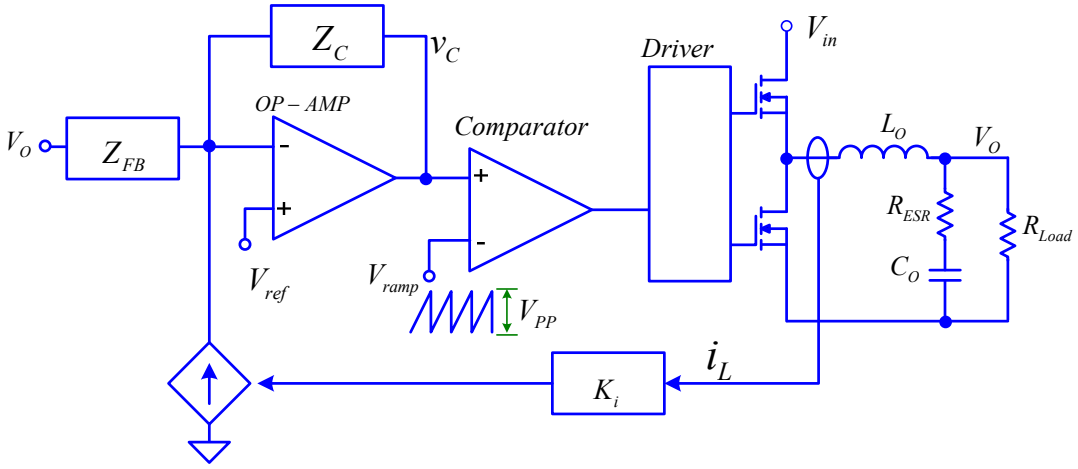


(b) Phase for simultaneous operation

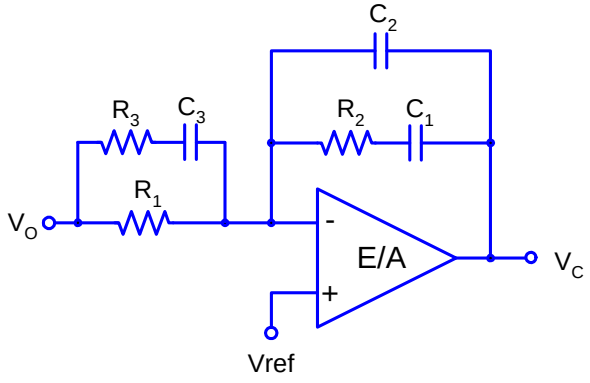
Figure 2-9. Power stage transfer function for simultaneous operation.

2.3 Small-signal Model of VR with Droop Control

The block diagram of a typical voltage regulator with droop control is shown in Fig. 2-10 (a). The inductor current, i_L, is sensed and fed to the error amplifier, with K_i being the current sense gain. This sensed current, $K_i * i_L$, flows through Z_{FB} and develops a voltage drop across Z_{FB}, resulting in reduced output voltage under load.



(a) Simplified voltage regulator circuit with droop control.



(b) Compensation network.

Figure 2-10. Block diagram of a typical voltage regulator with droop control.

Based on the block diagram, the output of the error amplifier is given by:

$$V_C = V_{ref} + \left(\frac{V_{ref} - v_O}{Z_{FB}} - K_i i_L \right) \cdot Z_C \tag{2-6}$$

For a typical compensation circuit, the DC impedance of Z_C is infinite. In order to keep the output of error amplifier in its operational range, the following equation must be satisfied:

$$V_O = V_{ref} - K_i \cdot R_1 \cdot i_L \tag{2-7}$$

where R_1 is the DC resistance of Z_{FB}. Under steady state condition, the load current I_O is equal to the inductor current i_L. Manipulating Equations 2-6 and 2-7 leads to:

$$R_{droop} = K_i \cdot R_1 \tag{2-8}$$

Similar to the modeling of conventional voltage mode buck converter, the small signal average model of the voltage regulator with droop control can be obtained by replacing the PWM comparator and the switching power stage by the DC gain block G_m ($=1/V_{PP}$) and V_{in} respectively, as shown in Fig. 2-4. Based on the small signal block diagram, the transfer function of the inner current loop (G_{IL}) and closed voltage loop (G_{VL}) can be expressed as:

$$G_{iL} = \frac{Z_C G_M V_{in} K_i}{sL_O + R_{DCR} + Z_1} \tag{2-9}$$

$$G_{VL} = \frac{Z_1}{Z_{FB}} \square \frac{Z_C G_M V_{in}}{sL_O + R_{DCR} + Z_1 + Z_C G_M V_{in} K_i} \tag{2-10}$$

Where

$$Z_1 = R_{Load} // \left(R_{ESR} + \frac{1}{sC_O} \right) = \frac{1 + sC_O R_{ESR}}{1 + sC_O (R_{ESR} + R_{Load})} \tag{2-11}$$

When the equivalent droop resistor R_{Droop} is small enough, i.e. the current sense gain K_i is very small, the operation of the voltage regulator with droop control is similar to typical voltage mode buck converter, and conventional design methods can be employed. When droop resistor is not ignorable and the compensation parameters are optimally designed, simplified voltage-loop (G_{VLS}) and current-loop (G_{ILS}) transfer function can be obtained as shown below.

$$G_{iLS} = \frac{G_M V_{in} K_i}{sC_1 R_{Load}} \frac{1 + sC_O R_{Load}}{1 + s\left(\frac{L_O}{R_{Load}} + C_O R_{DCR} + C_O R_{ESR}\right) + s^2 L_O C_O} \tag{2-12}$$

$$G_{VLS} = \frac{R_L}{K_i R_1} \frac{1 + sC_O R_{ESR}}{1 + sC_O\left(R_{ESR} + R_{Load}\right)} \frac{1}{1 + \frac{sL_O}{R_2 G_m V_{in} K_i}} \frac{1}{1 + sC_2 R_2} \frac{1 + sC_3(R_1 + R_3)}{1 + sC_3 R_3} \tag{2-13}$$

where K_i is the current sense gain, V_{in} is the input voltage, L_O, C_O, R_{ESR} and R_L are the power stage parameters, and R_1, R_2, R_3, C_1, C_2, and C_3 are the compensation parameters shown in Fig. 2-10 (b). G_m is the modulation gain, which depends on the peak-peak voltage V_{PP} of the ramp signal:

$$G_m = \frac{1}{V_{pp}} \tag{2-14}$$

2.4 Operational Principles of Adaptive Modulation Control

The simplified bode plot of droop control can be illustrated as shown in Fig. 2-11. It is found that there exists a flat range between the ESR zero and the pole w_{Le} as discussed in [1]. Since the pole w_{Le} is determined by the output inductance, modulation gain and other parameters, a change of

the modulation gain will have a direct impact on the system bandwidth. Adaptive modulation control is proposed by this motivation. The concept is to design an aggressively high bandwidth for steady-state operation, while decreasing the bandwidth by reducing the modulation gain when phases are on simultaneously as shown in Fig. 2-7. This will insure stable operation under all conditions.

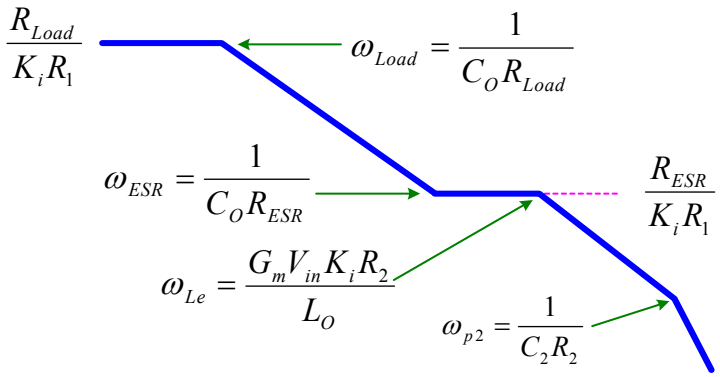


Figure 2-11. Simplified Bode plot of the loop gain for droop control.

Based on the Bode plot in Fig. 2-11, the reduction of modulation gain will push the w_{Le} to a lower frequency, resulting in reduced high frequency gain while keeping the low frequency gain unchanged. For a multiphase VR with droop control, the decrease of high-frequency gain means a decrease of bandwidth and possibly an increase of phase margin. During a large load transient, a corresponding large perturbation will be introduced to the output. This large perturbation in time domain can be transformed into large high-frequency components in the frequency domain. Since the feedback control loop functions as a low-pass filter, these high-frequency components and their associated sideband frequencies can not be damped if the bandwidth is too high [28].

With AMC, the loop gain at a high frequency range is reduced to attenuate the high-frequency components in large load-transient events.

The block diagram for AMC is illustrated in Fig. 2-12. A threshold logic block determines if there is a heavy load transition, based on the dv/dt of the output voltage. With AMC, the optimal slew rate of the ramp signal is adjusted, based on the number of on phases, as shown in the simplified circuit implementation. During load step-up transient, AMC stabilizes the system by increasing the slew rate of the ramp signal, which in turn reduces the modulation gain and the loop bandwidth. Therefore, the high frequency perturbations can be effectively attenuated, resulting in less voltage ring-back during large load transition.

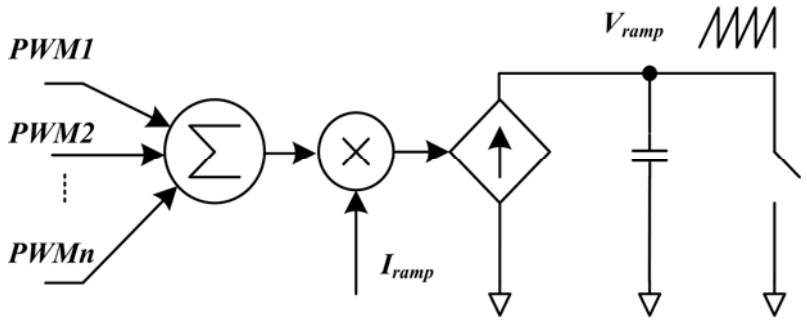


Figure 2-12. Block diagram for adaptive modulation control.

Time-domain investigation of AMC leads to the discovery that AMC shows great advantages in removing undesired voltage spikes during large load-insertion transients. A closer look at the transient voltage waveforms of droop control reveals that the VR output transient voltage drop

contains two main spikes during load step up. The first spike is determined by the output capacitors' ESR and ESL. If the output filters are fixed, there is little that can be done to improve the first spike. The second spike is due to the energy stored in the output filter inductor and the controller design [6] [9]. AMC is effective in removing the second ring-back spike. Fig. 2-13 (a) shows a traditional trailing edge modulation scheme during load step up. The compensation output (COMP) of the error amplifier is typically compared to a fixed ramp signal by a PWM comparator, which generates a PWM signal. The leading-edge (rising edge) of each pulse of the PWM signal depends on the clock (CLK) signal, while the trailing-edge (falling edge) of each pulse of the PWM signal is determined by the RAMP signal compared to the COMP signal. When only one phase of a two-phase voltage regulator is on, the total inductor current is charged at slew rate S_L which can be expressed as

$$S_L = \frac{V_{in} - 2V_O}{L_O} \tag{2-15}$$

where V_O and L_O represents output voltage and phase inductance, respectively. Supposing the step load is ΔI, the total time Δt to charge for the inductors current to the load current is

$$\Delta t = \frac{\Delta I}{S_L} \tag{2-16}$$

When APA [7] is triggered, the system turns on all PWMs simultaneously. The output inductance is equivalent to two inductors in parallel. Therefore, the sum of both inductor currents has approximately twice the slew rate of that of a single inductor, i.e.

$$S_L{}' = \frac{2V_{in} - 2V_O}{L_O} \tag{2-17}$$

where S'_L represents the inductor current slew rate for the simultaneous operation. For low voltage applications where V_O is much less than V_{in}, S'_L is more than twice of S_L. In this case, the effective charging time is given by

$$\Delta t' \approx \frac{1}{2}\Delta t \tag{2-18}$$

Therefore the charging time with simultaneous operation is half of that with the interleaved operation. As a result, the turn-off of the simultaneous operation during a load transition is expected to be sooner. For traditional trailing edge modulation control, PWM pulses are initiated by a clock signal and terminated when the error amplifier output voltage V_{comp} intersects a fixed ramp signal. The duty cycle D is described as

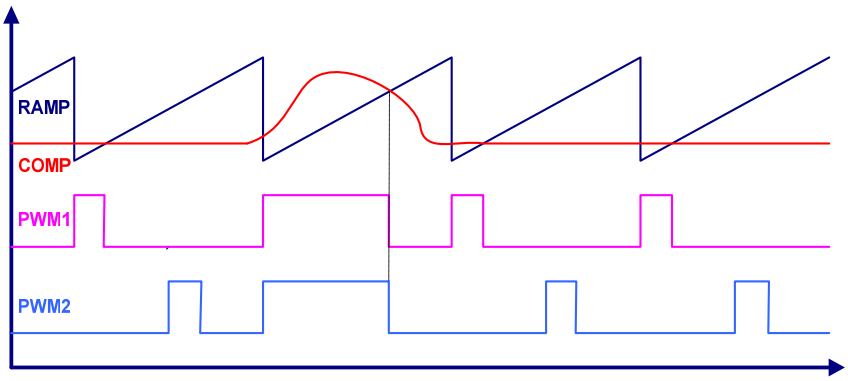
$$D = \frac{V_{comp}}{V_{pp}} \tag{2-19}$$

where V_{PP} is the ramp signal amplitude and is referenced to ground (GND). Assuming that the compensation parameters and the output capacitors are the same for both interleaved and simultaneous operations, the initial voltage drop after a heavy load application is almost the same, resulting in the similar output voltage at the error amplifier. This is valid for most cases. Moreover, the slew rate of the ramp voltage of a traditional modulator remains the same during both steady state and transient operations. Therefore, the duty cycle for each phase is still determined by the COMP signal and the constant ramp signal as shown in Fig. 2-13, even though two phases are on simultaneously under large load application events. With AMC, the slew rate

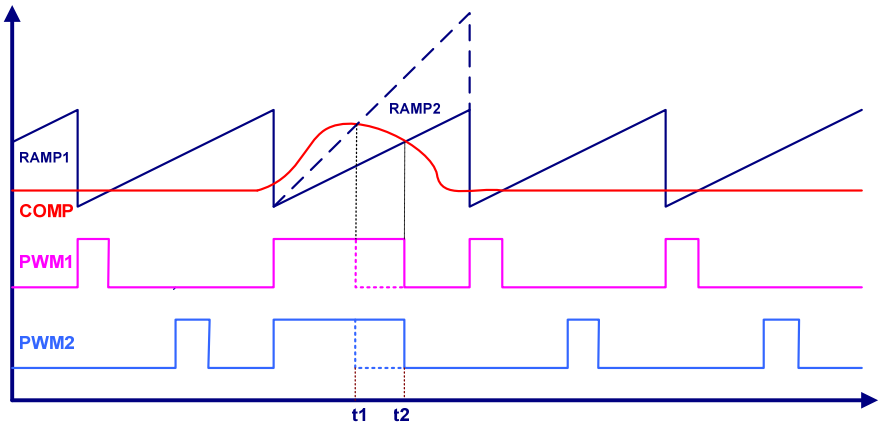
of the ramp signal is adjusted based on how many phases are simultaneously on. If PWM pulses of both phases are on simultaneously, the ramp signal rises with twice the slew rate of the ramp in normal interleaved operation. In this manner, the modulator gain decreases by half under a transient event. Since the ramp signal intersects COMP earlier, the duty cycle is reduced compared to traditional trailing edge modulation. The equation is given by

$$D' = \frac{V_{comp}}{2V_{pp}} \tag{2-20}$$

As shown in Fig. 2-13 (b), the AMC decreases the modulation gain by changing the slew rate of the ramp signal, depending on the active phase number. If PWM pulses of both phases are on simultaneously, the ramp signal rises with twice slew rate of the inductor current. As a result, the modulation gain decreases by half. In this manner, the COMP signal intersects the ramp earlier, resulting in reduced delay time. Thus it outperforms the traditional schemes by partly or totally removing the turn-on or turn-off delay. AMC is in fact a type of nonlinear control since it works only during dynamic load change.



(a) Trailing Edge Modulation

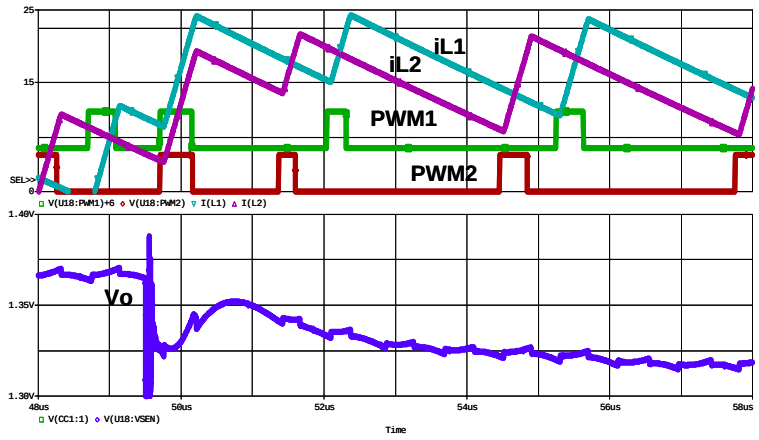


(b) Adaptive Modulation Control scheme

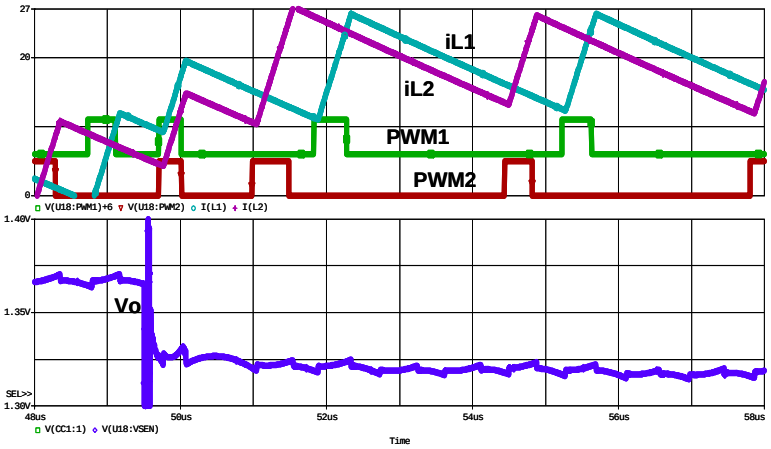
Figure 2-13. Adaptive Modulation Control Scheme for two phase buck converters.

2.5 Simulation and Experiment Results

Fig. 2-14 shows simulation results for a two-phase droop-control voltage regulator with and without the AMC scheme. The blue waveforms represent output voltage, while the red and the green waveforms are PWM signals for phase one and phase two, respectively. The light blue and pink waveforms are inductor current waveforms. During a large load transient, both phases are on simultaneously for fast transient response. The first voltage spike is determined by ESR and ESL. Following the first spike, for traditional trailing-edge PWM modulation control in Fig. 2-14 (a), there is significant voltage ring-back due to extra energy in the inductors during the transient event. AMC removes the turn-off delay by increasing the ramp slew rate; therefore the ring-back voltage is avoided and the system can settle down in a short time, as shown in Fig 2-14 (b).



(a) Output voltage ring-back due to turn-off delay

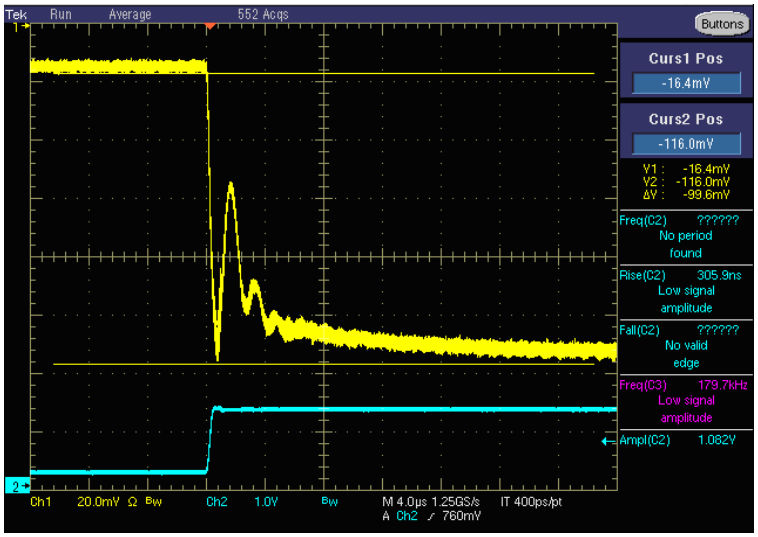


(b) Transient response with AMC

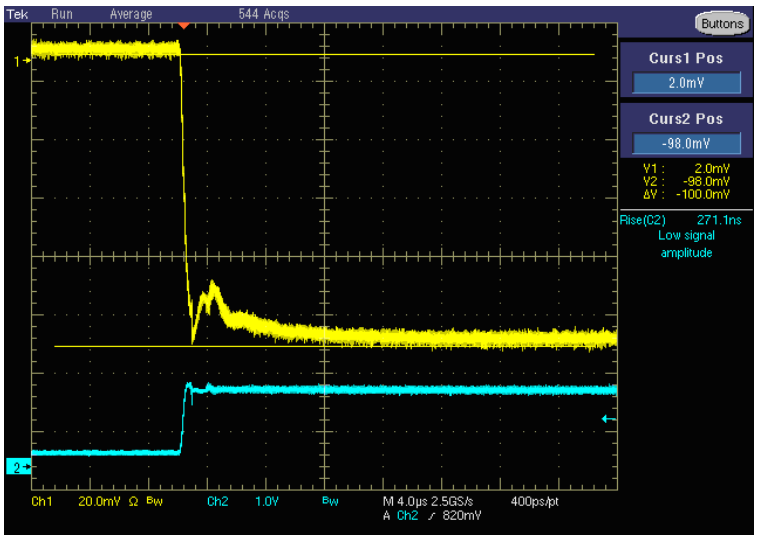
Figure 2-14. Pspice simulations for VRs without and with AMC, using LGA775 Socket & VTT Tool. Simulation model provided by Intel. System parameters: V_{in} = 12V, V_O = 1.2V, I_{Step} = 50A, L_O = 310 nH, C_O = 5 x 680 uF + 12 x 16 uF.

A 300 kHz four-phase VR designed with very high bandwidth and excellent transient response is built to verify AMC. The measured transient responses in time domain for the VRs without and with AMC are shown in Fig 2-15 (a) and (b). The upper waveforms represent the output voltages V_O and the lower waveforms represent load currents I_O. From the experiment comparison, it is

found that excellent transient performance is achieved for the voltage regulator with AMC. The voltage spikes are successfully suppressed under a large load transition.



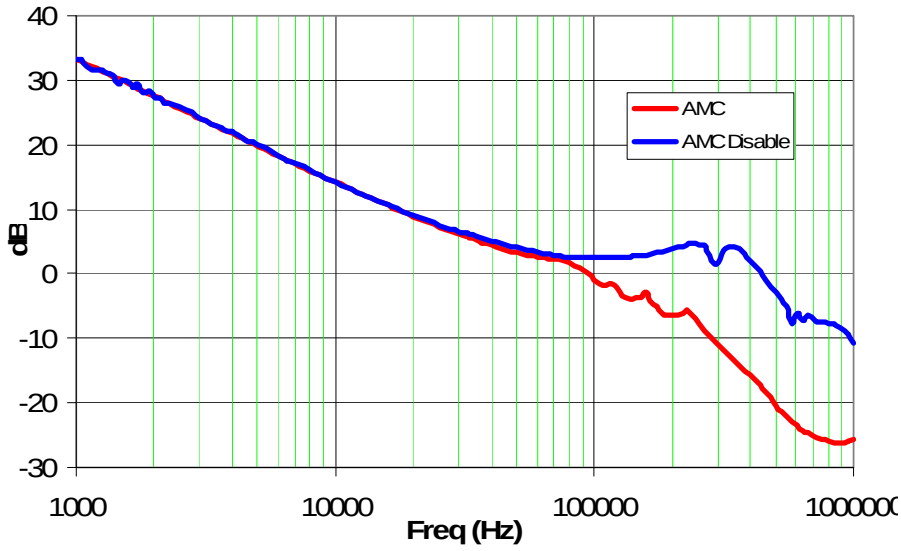
(a) Transient response without AMC.



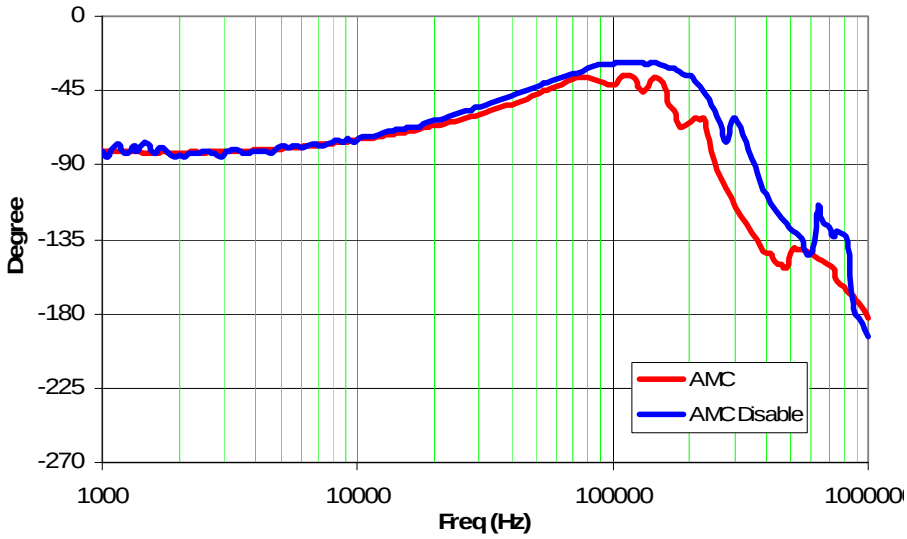
(b) Transient response with AMC

Figure 2-15. Experimental result comparison, using Intel LGA775 VTT tool. System parameters: V_{in} = 12V, V_O = 1.2V, I_{Step} = 95 A, L_O = 315 nH, C_O = 5 x 560 uF OSCON + 12 x 22 uF MLCC + 6 x 10 uF MLCC.

Measured bode plots of the close loop system shown in Fig. 2-16 illustrate how AMC adaptively adjusts the control bandwidth. The blue curves represent gain and phase of the loop during steady state (AMC is effectively disabled). The bandwidth is about 420 kHz and the phase margin is 61 degrees, while the phase switching frequency is 300 kHz. The red curves are gain and phase of the loop with AMC enabled. As shown in Fig. 2-16 (a), AMC changes the modulation gain and drops the bandwidth to 94 kHz. Hence, the phase margin is increased to 139 degree, as shown in solid red curves in Fig. 2-16 (b).



(a) Gain



(b) Phase

Figure 2-16. Experimental measurement of loop gain and phase for VR with AMC enabled and disabled.

2.6 Summary

Traditional PWM modulation schemes fail to achieve a robust high-bandwidth design and remove voltage ring-back during large load transients. The proposed AMC provides an effective solution by adaptively changing the modulation gain during large load transients. With AMC, it is possible to push the bandwidth above the switching frequency for multiphase VR applications with robust operation under all conditions. Simulation and experimental results have verified the proposed AMC scheme and corresponding analysis.

CHAPTER 3 ERROR AMPLIFIER VOLTAGE POSITIONING

3.1 Mechanism of Voltage Spike and Dip

Although multiphase converters with droop control have become common practice in the industry and show advantages in transient response [1], VR designers are facing challenges coming from low settle-down time of output voltage. For an ideal operation of voltage regulator with droop control, the output voltage should respond to the change of the load current immediately. However, the delay of the compensation network and output filter may deteriorate the output voltage waveform. The operational waveforms of droop control shown in Fig. 3-1 reveal how output voltage ring-backs and dips are introduced after the initial transient response. It is found that the output voltage drop contains two main spikes during load insertion. Output capacitors' ESR and ESL determine the first spike. Following the first spike, more power demand by the load drives the error amplifier output higher and higher. As the error amplifier output voltage (V_{COM}) is driven above the peak voltage of the internal ramp signal V_p, the PWM modulator saturates, and the control loop is broken. The capacitor voltages in the compensation network are driven away from their original values by the deviation of the output voltage. Upon the load insertion completion, V_{COM} needs to return to its original value as soon as possible. However time delay associated with the RC in the compensation network will try to hold V_{COM} from changing immediately. As a result, significant turn-off delay is introduced in the load insertion case. Since the output voltage is dictated by the output filters at this moment, the turn-

off delay causes extra energy stored in the output inductors to continue charging the output capacitors, resulting in a second spike (ring-back) [6] [9] [35].

For the load-release case as shown in Fig. 3-1, there usually exist an overshooting spike and a dip at output. The error amplifier output is driven as low as below the bottom tip of the ramp voltage (V_b) to drive the duty cycle to zero. Nevertheless, the inductor continues charging the output capacitors and causes the overshooting spike. The output voltage overshoots will force the error amplifier output voltage V_{COM} to saturate at its minimum limit. And the capacitor voltages in the compensation network are driven far away from their original values also. Only when the output voltage drops close to its reference voltage will the error amplifier start to recover from saturation. Just like in the load insertion case, the compensation network will try to hold V_{COM} due to the reason that voltage across the capacitors cannot be changed immediately. Depending on the compensation design, it may take a few switching cycles to get V_{COM} back to its original value, resulting in turn-on delay. This turn-on delay induces a voltage dip in return, as shown in Fig. 3-1.

Based on the analysis, it is concluded that the second load-insertion ring-back is caused by turn-off delay while the load-release voltage dip is due to the turn-on delay. Both delays are caused by the recovering time of capacitor voltages in the compensation network, which is driven far away from its steady state value during transient events. The secondary ring-back and dip after the initial transient response will deteriorate the performance of the voltage regulator.

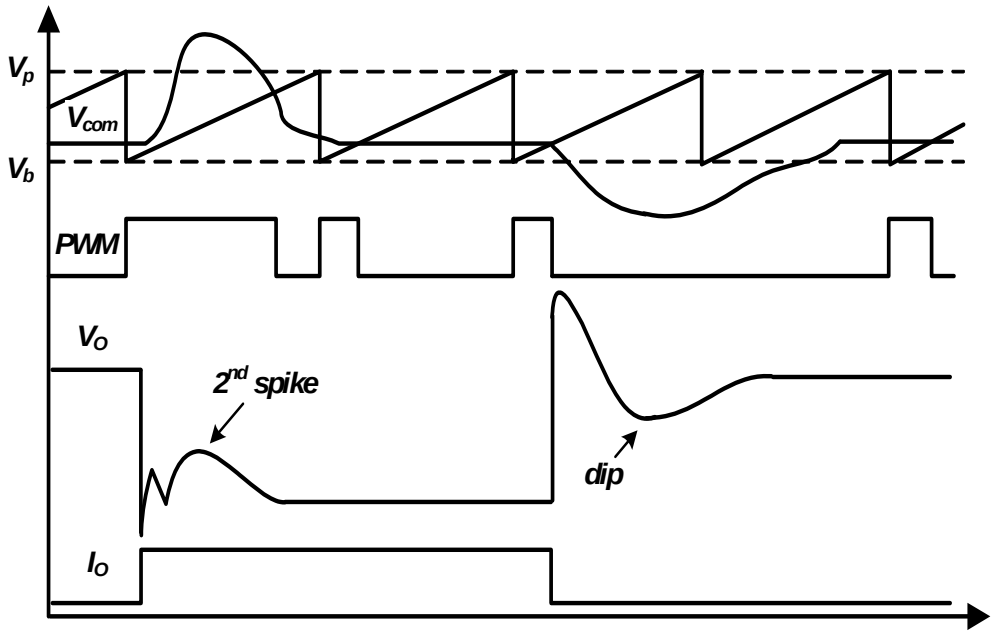


Figure 3-1. Transient response with droop control.

3.2 Operational Principles of the Error Amplifier Voltage Positioning

Much effort, such as applications of novel topologies, advanced devices, and control schemes has been made to meet dynamic requirements. Among these control schemes, some of them are based on the linear control [4-6] and others introduce the non-linear control [17-22], while the nonlinear control solutions can be implemented by either modifying the power block or changing the control gain like linear-non-linear control (LnLc) in [17]. With fast transient response, the first spike and the overshoot can be reduced. So far, however, little research has been done on the secondary spike and dip. In an effort to reduce the turn-on and turn-off delay after PWM saturation, the error amplifier voltage positioning (EAVP) is proposed in [36]. The EAVP is designed to reduce the second load insertion ring-back and the load-release voltage dip. The proposed EAVP can be classified as a non-linear control which works in a short period of time

during transient events. It facilitates the error amplifier voltage recovering processing during transient events, achieving fast settle-down performance. A four-phase buck with droop control will be utilized here to illustrate the mechanism, though EAVP can be applied to other control schemes such as voltage mode and peak current mode control.

Fig. 3-2 shows the simplified implementation diagram of EAVP, in which V_b and V_p represent the valley voltage and peak voltage of the saw-tooth waveform, respectively, and K_i is the amplifying gain of the EAVP once it is triggered. A threshold block determines if there is a transient event or not based on the slew rate dV/dt of the output voltage. Upon load transient events, the EAVP detects whether the error amplifier output V_{COM} is driven beyond the range of the ramp signal voltage. If V_{COM} is higher than the peak voltage of the ramp signal, i.e., V_p, the EAVP will push the error amplifier voltage higher. If V_{COM} is below the valley voltage of the ramp signal, i.e., V_b, the EAVP will pull V_{COM} down to a lower voltage. In short, the EAVP pushes the error amplifier voltage to a level which will drive the PWM saturation deeper for a short interval. Once V_{COM} gets back to within the ramp signal voltage range, the EAVP will hold it at V_b till controller starts to regulate the output voltage, preventing V_{COM} from deviating out of the range.

Fig. 3-3 illustrates the operational waveforms of EAVP during transient. The solid-line of V_{com} represents the error amplifier voltage without EAVP while the dash-line of V_{com} is with EAVP. For the output voltage V_O, the solid line is without EAVP and the dash line is with EAVP active.

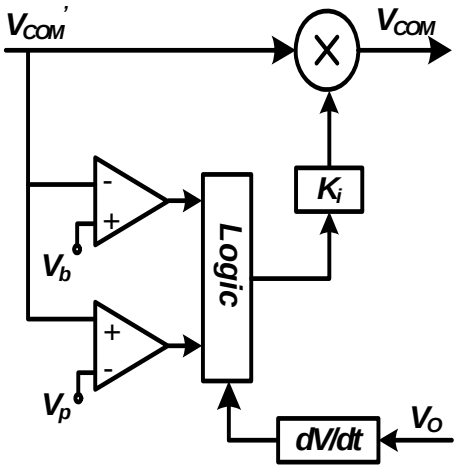


Figure 3-2. Simplified block diagram of EAVP.

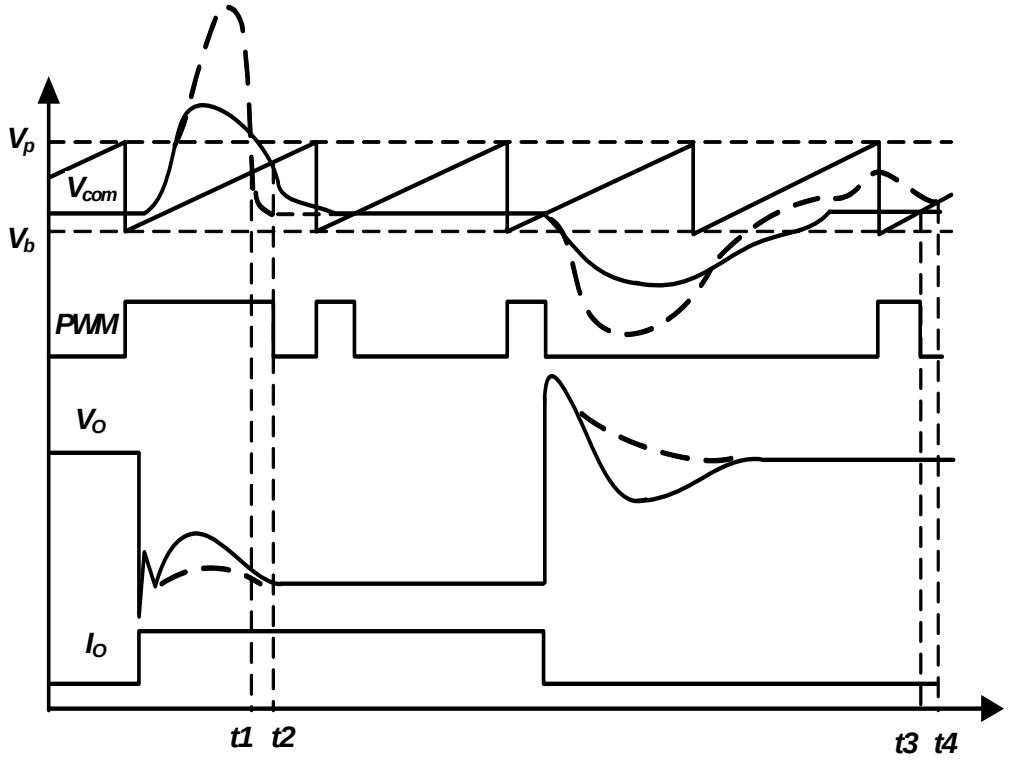


Figure 3-3. Transient operational waveforms for EAVP.

Mathematical analysis of the error amplifier during transient events will give us a better understanding of how the proposed EAVP helps V_{COM} recover from saturation. Fig. 3-4 shows an error amplifier with type III compensation components, in which Z_1 and Z_2 enclosed by dash lines are simplified impedance blocks. Since the control loop is broken during the large transient event, the loop analysis by means of traditional small signal analysis techniques is not applicable here. Instead, classic large-signal circuit analysis techniques are employed for the EAVP analysis.

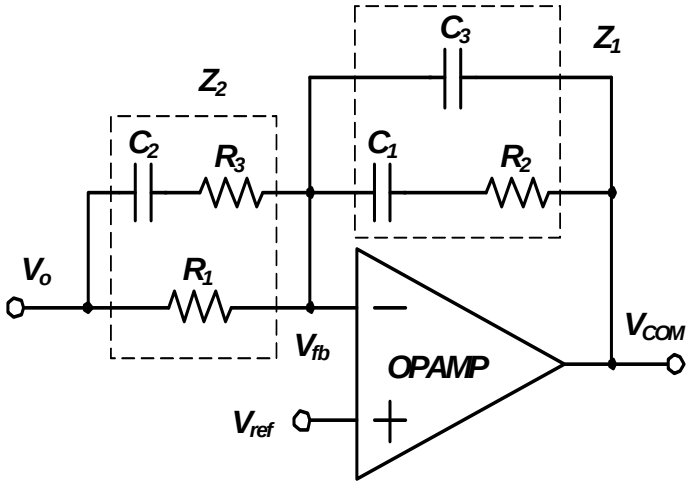


Figure 3-4. Error amplifier with compensation.

As PWM modulator is saturated, the error amplifier output voltage V_{COM} is determined by the output voltage and the compensation network as shown in Fig. 3-4. When the output voltage deviates from its desired value during transient events, the voltage deviation will generate a

current through the compensation network to adjust V_{COM} to correct the error. If the error amplifier open loop gain is A_O, then V_{COM} can be given by

$$V_{com} = A_O \cdot (V_{ref} - V_{fb}) \tag{3-1}$$

where V_{ref} is the reference voltage and V_{fb} is the voltage at the inverting input of the error amplifier. Applying voltage divider theorem, V_{fb} can be obtained in terms of V_{com} and V_O

$$V_{fb} = \frac{Z_2 \times V_{com} + Z_1 \times V_O + I_{droop} \times Z_1 \times Z_2}{Z_1 + Z_2} \tag{3-2}$$

where I_{droop} is the sensed load current for the droop control, Z_1 and Z_2 are the impedances of the compensation network shown in Fig. 3-4. Let the initial V_{com} deviation be ΔV_{com1}, then V_{fb} deviation induced by ΔV_{com1} is given by

$$\Delta V_{fb} = \frac{Z_2 \times \Delta V_{com1} + Z_1 \times V_O + I_{droop} \times Z_1 \times Z_2}{Z_1 + Z_2} \tag{3-3}$$

Assuming V_O and I_{droop} change very slowly during a very short interval and have negligible effect on this equation, which is true for most cases, the net change of V_{fb} will then be fed back to V_{com}. And the resulted change of V_{com} (ΔV_{com2}) can be expressed by insertion of Equation 3-3 into Equation 3-1 and re-arrangement of the equation as:

$$\Delta V_{com2} = -\frac{A_O \times Z_2}{Z_1 + Z_2} \times \Delta V_{com1} \tag{3-4}$$

Since the open loop gain of an op amp A_O is usually very big, the quantity $\frac{A_O \times Z_2}{Z_1 + Z_2}$ becomes much larger than 1. Therefore a small change of V_{com} will result in a significant change of V_{com}, in an opposite direction.

As shown in Fig. 3-3, during a load insertion, the EAVP pushes V_{com} to a higher voltage in a short interval to achieve the maximum duty cycle. Based on the above analysis, the error amplifier output sees a much larger voltage change in an opposite direction; in a way that brings V_{com} back to regulation much quicker than otherwise, resulting in reduced turn-off delay. During a load release transition, the EAVP pulls V_{com} to a lower voltage, in a manner similar to load insertion. Large error amplifier gain feeds the net change of V_{fb} back to V_{com} and gets V_{com} back to within ramp signal level very quickly. Therefore, the turn-on delay is reduced, resulting in reduced voltage dip. The dashed line is V_{com} under the EAVP scheme and the solid line is the V_{com} without EAVP. It should be noted that it could take a long time to stabilize V_{com} after it is back to the original value under some circumstances. EAVP automatically holds V_{com} if it tries to go below the ramp signal valley voltage (V_b), avoiding excess settling time which will worsen transient performance.

3.3 Simulation and Experimental Results

A three-phase VR with droop control schematic is built in Simplis to demonstrate the effectiveness of the EAVP. The switching frequency is 500 kHz. Fig. 3-5 shows the simplified simulation schematic, and Figs. 3-6 shows simulation comparison for this VR with and without the EAVP. The red curves are VO and the pink curves are Vcom for the VR without EAVP, while the blue curves are VO and the green ones represent Vcom with EAVP.

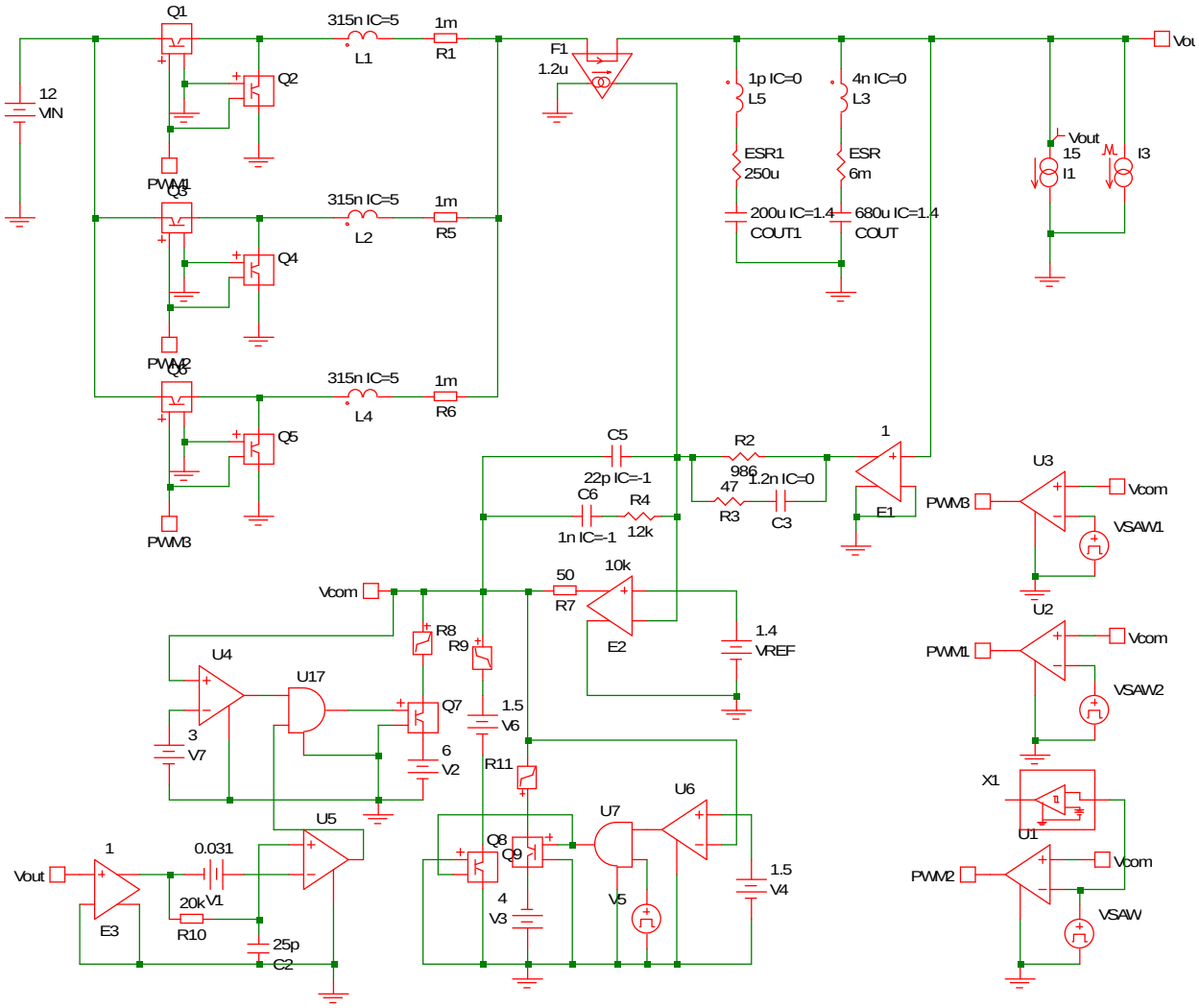
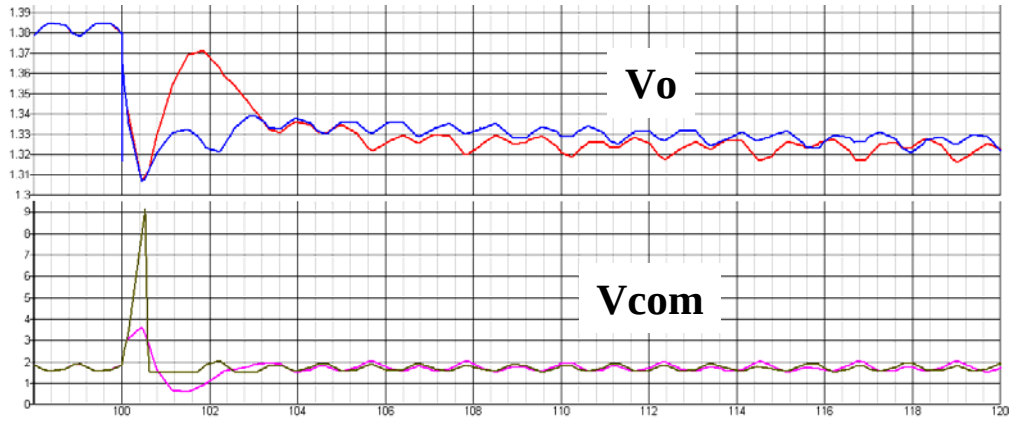
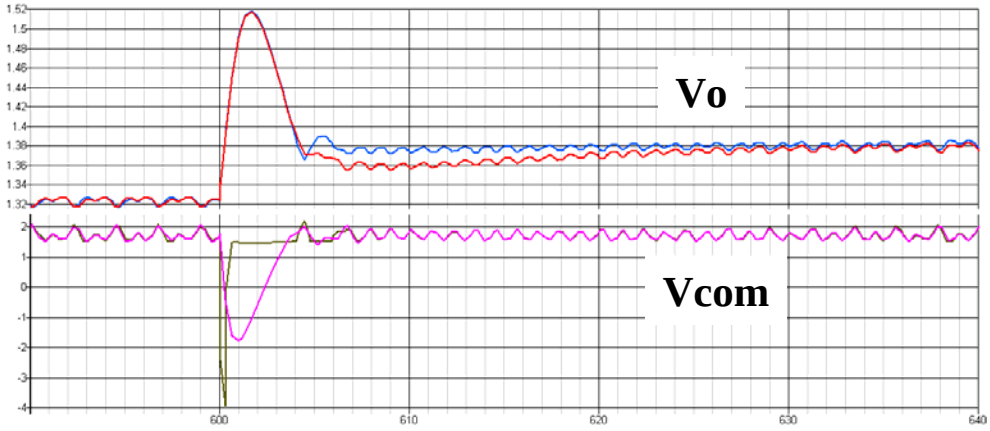


Figure 3-5. Simulation schematic of a VR with EAVP.

It is found from Figs. 3-6 that there is a significant voltage ring-back at load insertion, and a voltage dip at load release, if the EAVP is disabled. When the EAVP is active, V_{com} recovers much quicker, reducing PWM turn-on and turn-off delays. Therefore the output voltage has less ring-back and voltage dip.



(a) Transient response at load insertion.



(b) Transient response at load release

Figure 3-6. Transient response comparison for VRs with and without EAVP.

A four-phase VR prototype with droop control is built to verify the EAVP. The experimental results are shown in Figs. 3-7 to 3-10. The pink curve represents the error amplifier voltage V_{com} while the blue curve represents the output voltage V_O. For traditional control scheme without EAVP as shown in Figs. 3-7 and 3-8, the error amplifier output voltage has larger settling time. The large settling time results in voltage ring-back and dip after initial response.

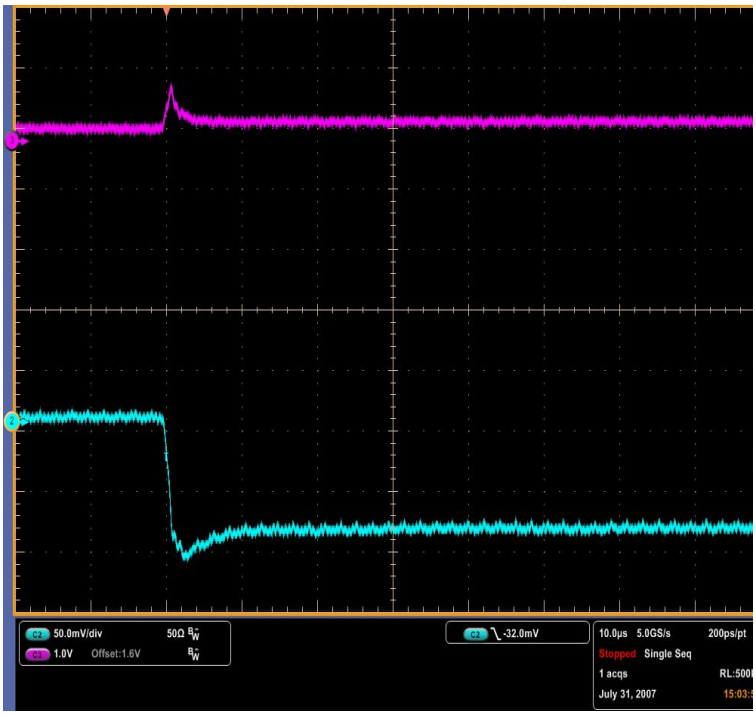


Figure 3-7. Load insertion without EAVP.

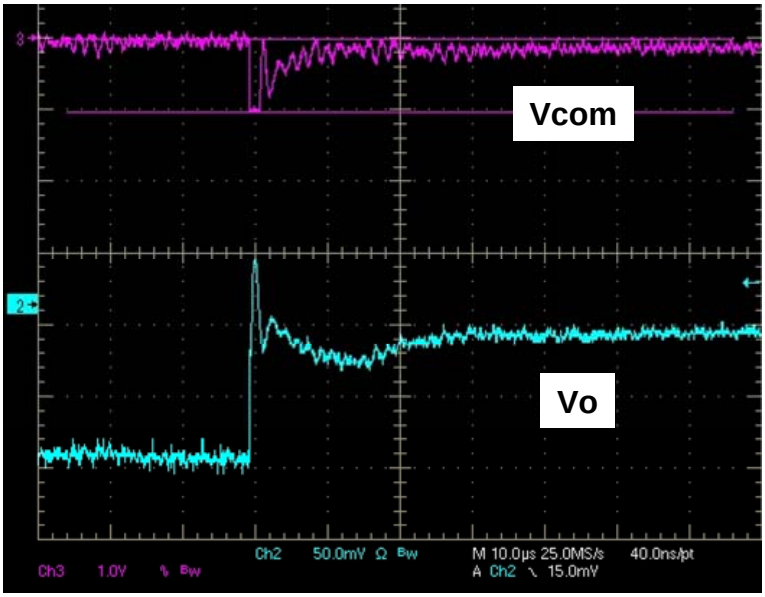


Figure 3-8. Load release without EAVP.

As shown in Figs. 3-9 and 3-10, with the assistance of the EAVP, the error amplifier output voltage is driven up or down very quick and then clamped close to the valley point (about 1.3V) of the ramp signal. As a result, the output voltage settles down to its final value quickly when the proposed EAVP scheme is applied. From the comparison, it can be concluded that the EAVP improves VR transient response significantly.

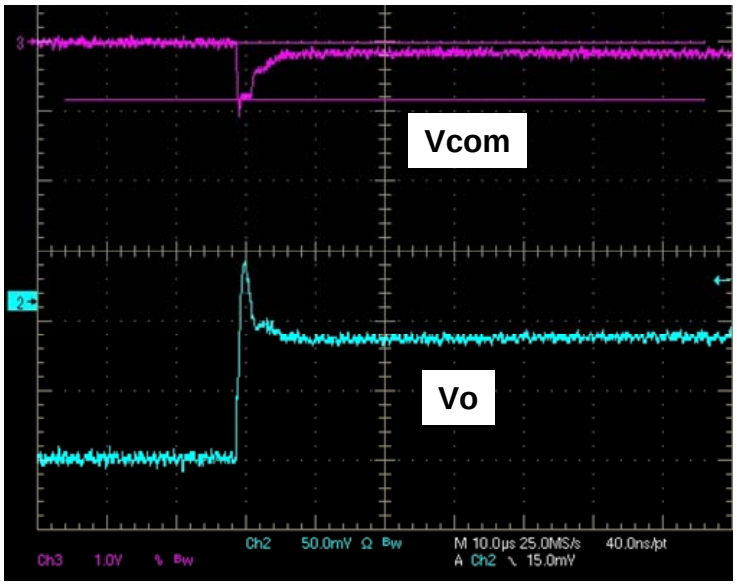


Figure 3-9. Load insertion with EAVP.

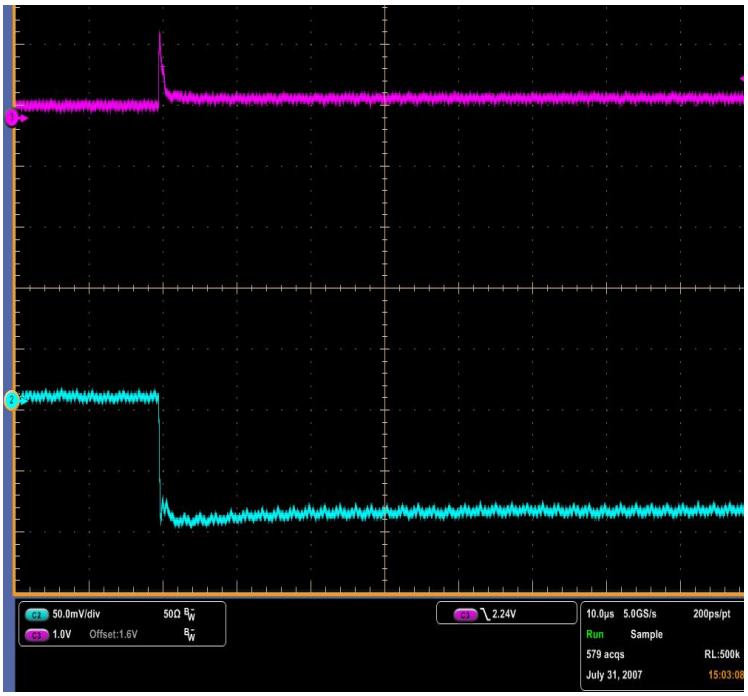


Figure 3-10. Load release with EAVP.

3.4 Summary

The proposed EAVP offers a new solution for fast transient response improvement. With EAVP, the settling time of the error amplifier voltage is reduced significantly. Therefore, both turn-on and turn-off delays of the VR PWM can be reduced. As a result, voltage overshoot and undershoot are suppressed to a large extent. Simulation and experimental results have verified the effectiveness of the EAVP scheme.

CHAPTER 4 INVESTIGATIONS OF COUPLED INDUCTORS

4.1 Fundamentals of Coupled Inductors

Coupled inductors are an emerging topology for power supplies. The concept of coupled inductors is to combine several discrete phase inductors for a given topology into one magnetic core structure. By taking advantage of the electrical and magnetic relationships in the electrical topology and the magnetic circuits of the inductors, the power losses and size of the whole magnetics can be saved. In recent years, multiphase VR with coupled inductors have drawn more and more attention from both industry and academia due to their significant advantages over traditional interleaved buck converters [37-42]. Some work was involved in various coupled-inductor topologies and modeling [37-42]. In [38], [42], [48], [49], and [55], the implementation of multi-phase coupled-inductor VR in which the number of coupled phases is larger than two were explored. The linear structure of a multi-phase coupled inductor is inherently asymmetrical. With coupling phase number more than two, the non-identical magnetic characteristics for different phases may lead to sub-harmonic output ripple [47]. Therefore, two-two coupled-inductor VR is usually preferred in industry. Throughout this chapter, two-two coupled inductors are investigated for general purpose. A typical four-phase VR prototype with two-two coupled inductors is shown in Fig. 4-1, and a physical drawing of two-phase coupled inductors with a single EI core is shown in Fig. 4-2, where L_1 and L_2 denote the phase inductors. The two inductor copper traces are built on the two outer legs of the core and are marked in orange. The

core is in grey color. An air gap is sometimes required on each outer leg to avoid saturation of the core.

Figure 4-1. Prototype of a four-phase VR with two-two coupled inductors.

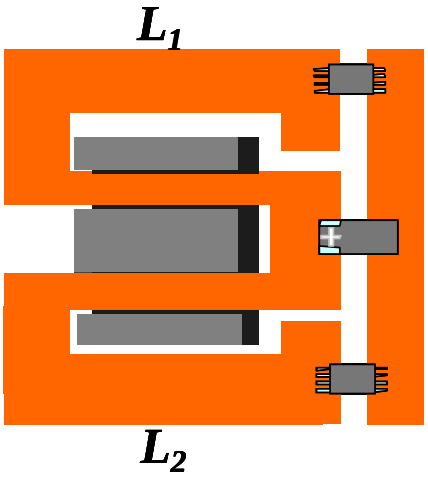


Figure 4-2. Cross-sectional view of coupled inductors with a single EI core.

4.1.1 Design of Coupled Inductors

Coupled inductor design usually involves coupling coefficient and effective inductance determination. In this chapter, the coupling mechanism is explored in terms of both electrical and reluctance modeling. A most widely utilized model of two-two coupled inductors is shown in Fig. 4-3 [38] [48-49]. This circuit model consists of leakage inductances (L_{k1} and L_{k2}) in series with the inductor DCR for two winding and an ideal transformer with a magnetizing inductance (L_M) on one of the windings. V_{P1} and V_{P2} are denoted as the phase voltages for the phase inductors L_1 and L_2, referred to the output voltage V_O.

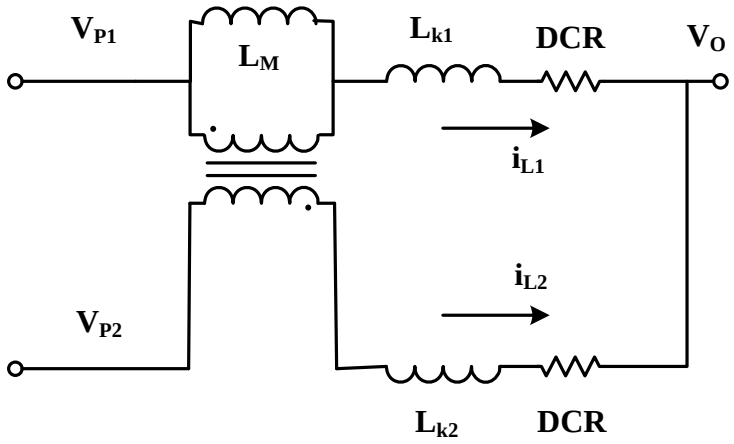


Figure 4-3. Electrical model of two-phase coupled inductors.

Complicated magnetic structures, composed of multiple windings and multiple heterogeneous elements such as cores and air gaps, can be represented using equivalent magnetic circuits, i.e. reluctance model. These magnetic circuits can then be solved using conventional circuit analysis, to determine the various flux, voltage and current relationships. The equivalent reluctance model for two-phase coupled inductors is built as shown in Fig. 4-4, in which ϕ_1 and ϕ_2 are the fluxes passing through the phase inductors, and N_1 N_2 are the inductor turns numbers. The two windings are two sources of magnetomotive force (MMF), of value Ni. The core legs and air gap characteristics can be modeled by reluctances R_1, R_2, R_C, respectively. From Faraday's Law we have

$$V_{P1} = N_1 \cdot \frac{d\phi_1}{dt} \tag{4-1}$$

$$V_{P2} = N_2 \cdot \frac{d\phi_2}{dt} \tag{4-2}$$

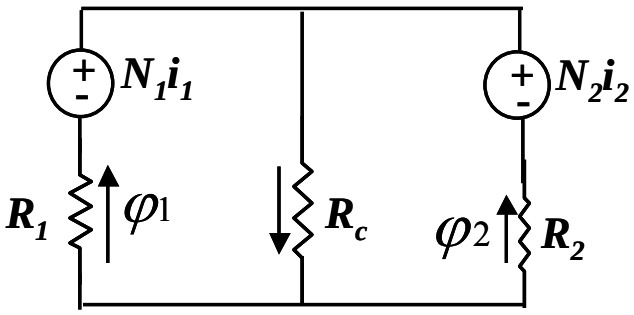


Figure 4-4. Reluctance model of two-phase coupled inductors.

Based on the Ampere's Law and the theory of flux continuity, the following equations are obtained from Fig. 4-4:

$$R_1 \cdot \phi_1 + R_C \cdot (\phi_1 + \phi_2) = N_1 \cdot i_1 \tag{4-3}$$

$$R_2 \cdot \phi_2 + R_C \cdot (\phi_1 + \phi_2) = N_2 \cdot i_2 \tag{4-4}$$

Manipulating the above equations leads to the expressions for flux in the core legs:

$$\phi_1 = \frac{N_1 \cdot i_1}{R_1 + R_C // R_2} - \frac{N_2 \cdot i_2}{R_2 + R_C // R_1} \cdot \frac{R_C}{R_C + R_1} \tag{4-5}$$

$$\phi_2 = \frac{N_2 \cdot i_2}{R_2 + R_C // R_1} - \frac{N_1 \cdot i_1}{R_1 + R_C // R_2} \cdot \frac{R_C}{R_C + R_2} \tag{4-6}$$

$$\phi_C = \frac{N_2 \cdot i_2}{R_2 + R_C // R_1} \cdot \frac{R_1}{R_C + R_1} + \frac{N_1 \cdot i_1}{R_1 + R_C // R_2} \cdot \frac{R_2}{R_C + R_2} \tag{4-7}$$

Hence, the flux density in each leg is given by

$$B_1 = \frac{\phi_1}{A_1} \qquad B_C = \frac{\phi_C}{A_C} \qquad B_2 = \frac{\phi_2}{A_2} \tag{4-8}$$

where A_1, A_2, and A_C are the cross-sectional areas of the core legs, respectively. Those values will be used to determine the saturation point of the cores. From the equations for flux, it is found that

$$V_{P1} = \frac{N_1^{\,2}}{R_1 + R_C // R_2}\frac{di_1}{dt} - \frac{N_1 \cdot N_2}{R_2 + R_C // R_1}\cdot\frac{R_C}{R_C + R_1}\frac{di_2}{dt} \tag{4-9}$$

$$V_{P2} = \frac{N_2^{\,2}}{R_2 + R_C // R_1}\frac{di_2}{dt} - \frac{N_1 \cdot N_2}{R_1 + R_C // R_2}\cdot\frac{R_C}{R_C + R_2}\frac{di_1}{dt} \tag{4-10}$$

Based on the electrical model in Fig. 4-3, we have

$$V_{P1} = L_{k1}\cdot\frac{di_1}{dt} - L_M\cdot\frac{d(i_2 - i_1)}{dt} \tag{4-11}$$

$$V_{P2} = L_{k2}\cdot\frac{di_2}{dt} - L_M\cdot\frac{d(i_1 - i_2)}{dt} \tag{4-12}$$

Manipulating Equations 4-11 and 4-12 yields

$$V_{P1} = (L_{k1} + L_M)\cdot\frac{di_1}{dt} - L_M\cdot\frac{di_2}{dt} \tag{4-13}$$

$$V_{P2} = (L_{k2} + L_M)\cdot\frac{di_2}{dt} - L_M\cdot\frac{di_1}{dt} \tag{4-14}$$

Comparing Equations 4-13 and 4-14 to 4-9 and 4-10, and rearranging the equations it is found that

$$L_M = \frac{N_1 \cdot N_2 \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + R_1 \cdot R_2} \tag{4-15}$$

$$L_{k1} = \frac{(R_2 + R_C)\cdot N_1^{\,2} - N_1 \cdot N_2 \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + R_1 \cdot R_2} \tag{4-16}$$

$$L_{k2} = \frac{(R_1 + R_C) \cdot N_2{}^2 - N_1 \cdot N_2 \cdot R_C}{R_2 \cdot R_C + R_1 \cdot R_C + R_1 \cdot R_2} \tag{4-17}$$

Normally phase inductors have an equal number of turns for multiphase buck converters. And since the reluctance of the high-permeability cores is negligible compared to the reluctance of the low-permeability cores, R_1 and R_2, L_{k1} and L_{k2} can be regarded as being equal. Replacing R_1 and R_2 with R, N_1 and N_2 with N, and L_{k1}, L_{k2} with L_k, we have

$$L_M = \frac{N^2 \cdot R_C}{2R \cdot R_C + R^2} \tag{4-18}$$

$$L_k = \frac{N^2}{R + 2R_C} \tag{4-19}$$

According to the expression for L_l and L_M, we can adjust the reluctance of the low-permeability core or make air gaps to obtain the desired coupling coefficient. This can be realized by changing the geometry or/and changing the permeability u_r of the core since

$$R_C = \frac{l_C}{u_r \mu_0 A_C} \tag{4-20}$$

where l_C is the core length and A_C is the cross-sectional area of the core.

4.1.2 Power Loss Reduction with Coupled Inductors

With coupled inductors, several magnetic components can be constructed in one magnetic core by sharing a common magnetic path. Therefore, the number of magnetic cores is reduced, and the flux ripple may also be suppressed [38-41]. To investigate the core loss reduction

mechanism, let's examine the operational waveforms of two-phase coupled inductors as shown in Fig. 4-5. It is found that there is a phase shift between two phases, usually 180^{o} phase shift for a two-phase voltage regulator.

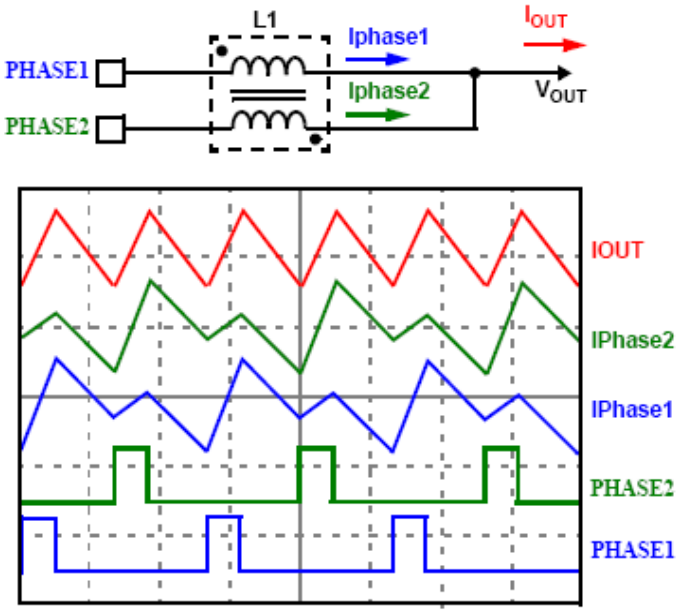


Figure 4-5. Operational waveforms of the coupled inductors.

Based on Equation 4-7 for ϕ_C, phase-shifted currents of the phase inductors will lead to reduced flux in the shared core leg. That is to say, flux cancellation is realized in the center core. Maxwell simulation shown in Fig. 4-6 manifests the cancellation effect in a straightforward way. The blue and red ones are windings of the coupled inductors, and the core set is made up of a ferrite E core and an I core. The color lines inside the core represent flux lines. It is clear that flux lines are reduced in the center leg due to the current phase shift. Since the core loss is a

function of flux density, core volume, and switching frequency, a reduction in flux density will result in reduced power loss.

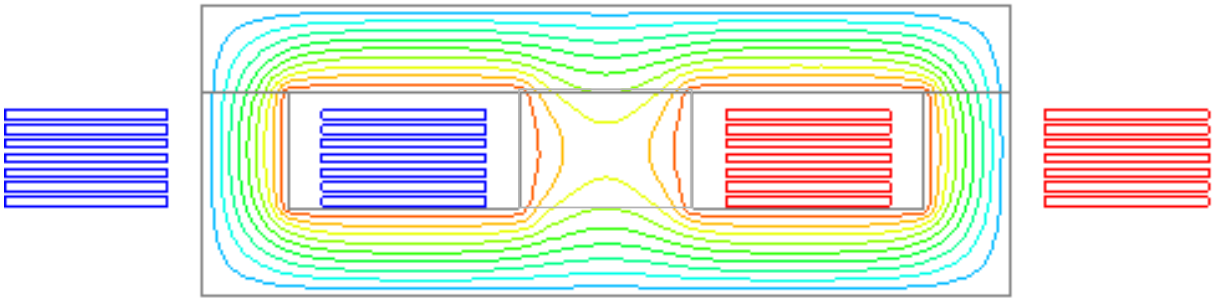


Figure 4-6. Flux cancellation in the core of the coupled inductors.

Some work previously performed on coupled inductors shows that the coupling of inductors is able to reduce the phase RMS current value, even though the total output current remains independent on the coupling coefficient [39] [40]. Fig. 4-5 shows how the phase currents have increased the effective switching frequency, resulting in reduced RMS value of phase currents. A smaller phase RMS current value leads to lower inductor conduction losses. Therefore, coupled inductors help reduce copper losses if the phase leakage inductance is equal to the phase inductance of its non-coupled counterpart.

However, it should be pointed out that the coupling coefficient k, which is defined as the mutual inductance over the phase inductance, can not be made approaching unit. Since for multi-phase buck converters with coupled inductors, only the leakage inductances function as filter inductors,

excessive coupling will lead to insufficient filter inductance, which in return causes high output current ripple.

4.2 Effects of Magnetizing Inductance on VR with Coupled Inductors

Intensive research has been done on various coupled-inductor topologies and modeling [37-42]. The magnetizing inductance plays an important role in the coupled-inductor operation. However, little work has been done on the effects of magnetizing inductance on voltage regulator performance. In most literature, the voltage regulator with coupled inductors is simplified to the conventional topology with leakage inductor per phase representing the coupled inductors, while the magnetizing inductance is ignored. It may be valid for analysis purposes if all phase parameters are identical. In practical applications, however, device parasitics, tolerance, and other non-ideal factors make phases not symmetrical any more. Therefore, it is desired to evaluate the general effects of magnetizing inductance on VR performance. Since two-two coupled-inductor VR is a common industrial practice, a typical two-phase voltage regulator with coupled inductors will be used as an example as shown in Fig. 4-7. And a widely utilized model of coupled inductors is enclosed in the dashed line. A unified State-Space Averaging model [43] will be built for this two-phase coupled-inductor VR. The DC solutions of the phase currents will then be derived in order to show the impact of the magnetizing inductance on phase current balancing. Finally a small signal model can be obtained based on the state-space model. The overall effects of magnetizing inductance on dynamic performance will then be presented.

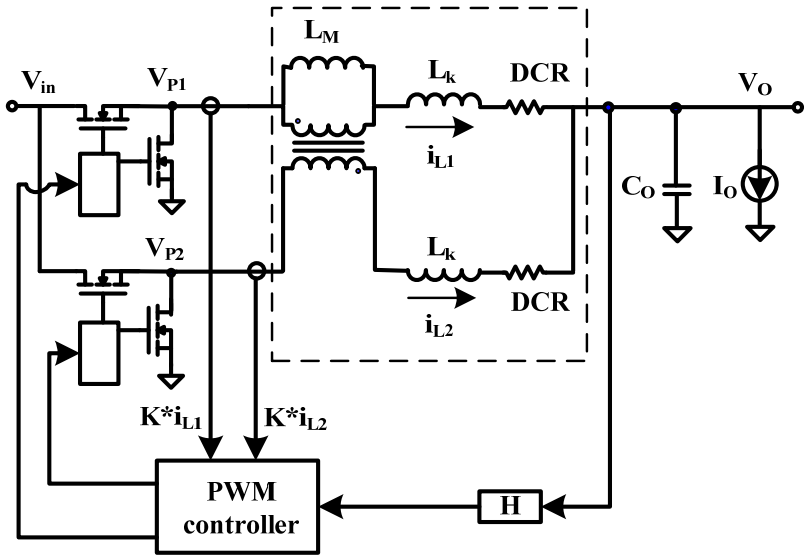


Figure 4-7. Two-phase VR with coupled-inductor model.

4.2.1 State Space Averaging Model and Solutions

To evaluate the effects of magnetizing inductance on VR performance, the power stage of the two-phase VR model with coupled-inductors in Fig. 4-7 is redrawn as shown in Fig. 4-8, with all parasitic parameters, in which R_{ij} is the R_{dson} of each MOSFET, and V_{P1} V_{P2} are voltages across the leakage inductance and magnetizing inductance for respective phases.

The state-space averaging modeling of dynamical systems is a common practice of modern control theory; its state-space description can be employed to derive the small signal averaged equations of VRs with coupled inductors. The advantage of the state-space-averaging modeling is that it can maintain the generality of its result: one can always obtain a small signal averaged model, provided that the state equations of the original voltage regulator can be written. Thus,

compared to previous work done on modeling of VR with coupled inductors, this method provides us with a model without simplifying the effects of magnetizing inductance.

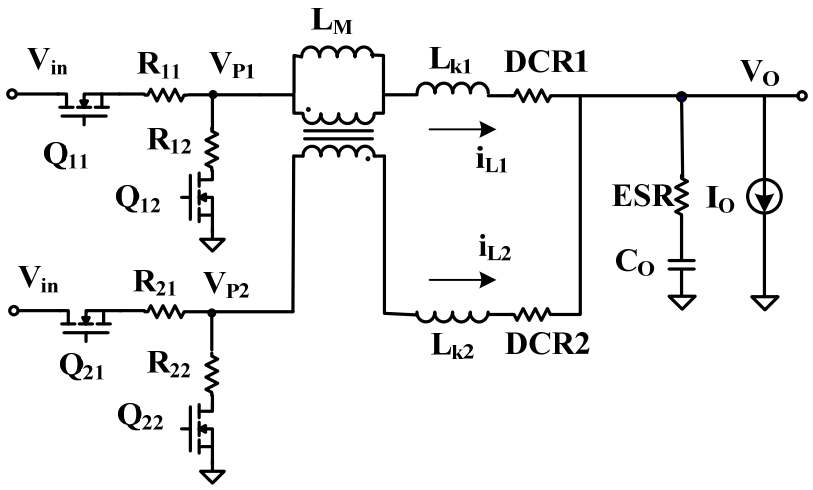


Figure 4-8. Power stage of two-phase VR model with circuit parameters.

The state equations of a VR with coupled-inductors can be written in the compact matrix form of Equation 4-21 [44].

$$K\frac{dx}{dt} = Ax + Bu \qquad Y = Cx + Eu \tag{4-21}$$

where the state vector x contains all the state variables which are the inductor currents and capacitor voltage. The input vector u is the vector containing the independent sources, such as the input voltage and output current. K is a matrix containing the values of capacitance, inductance and magnetizing inductance. The matrices A and B contain constants of proportionality. Based on the circuit model in Fig. 4-8, the following equations can be obtained:

$$V_{P1} = (L_{k1} + L_M)\frac{di_{L1}}{dt} - L_M \frac{di_{L2}}{dt} \tag{4-22}$$

$$V_{P2} = (L_{k2} + L_M)\frac{di_{L2}}{dt} - L_M \frac{di_{L1}}{dt} \tag{4-23}$$

$$C_o \frac{dv_C}{dt} = i_{L1} + i_{L2} - I_o \tag{4-24}$$

Then, the state vectors and matrices can be defined as Equations 4-25:

$$K = \begin{bmatrix} L_{k1} + L_M & -L_M & 0 \\ -L_M & L_{k2} + L_M & 0 \\ 0 & 0 & C_o \end{bmatrix} \quad \frac{dx}{dt} = \begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} \quad x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_C \end{bmatrix} \quad u = \begin{bmatrix} V_{in} \\ I_o \end{bmatrix} \tag{4-25}$$

Assuming the voltage regulator is operating in CCM, there are four subintervals for a two-phase VR with coupled inductors which are shown in Figs. 4-9 through 4-12.

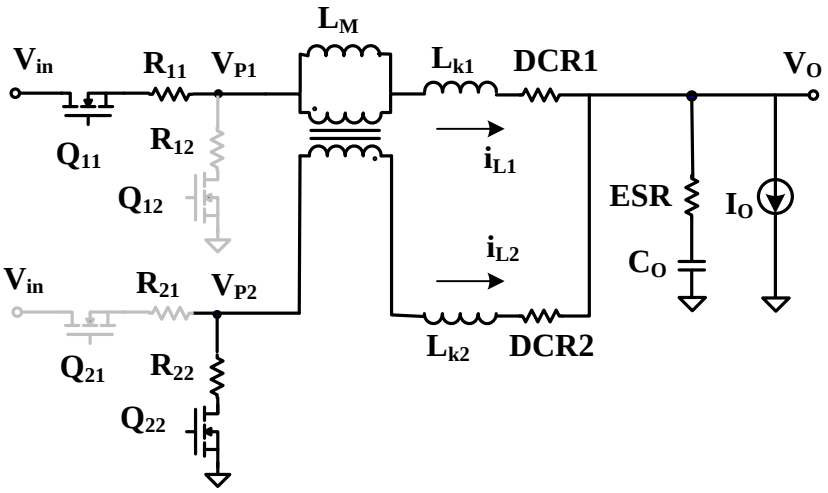


Figure 4-9. Subinterval 1, Q11 and Q22 on, Q12 and Q21 off.

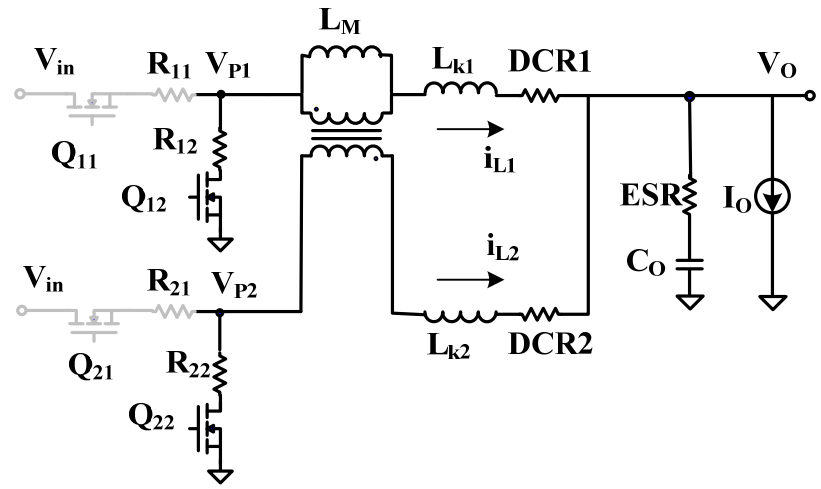


Figure 4-10. Subinterval 2, Q12 and Q22 on, Q11 and Q21 off.

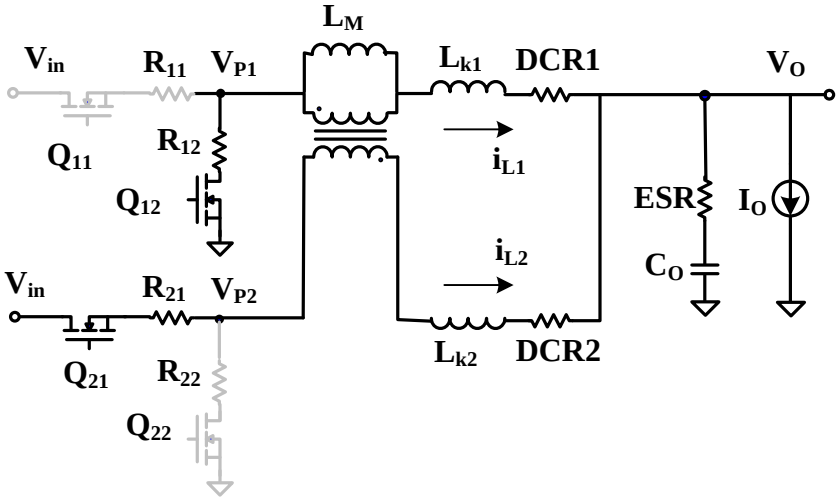


Figure 4-11. Subinterval 3, Q12 and Q21 on, Q11 and Q22 off.

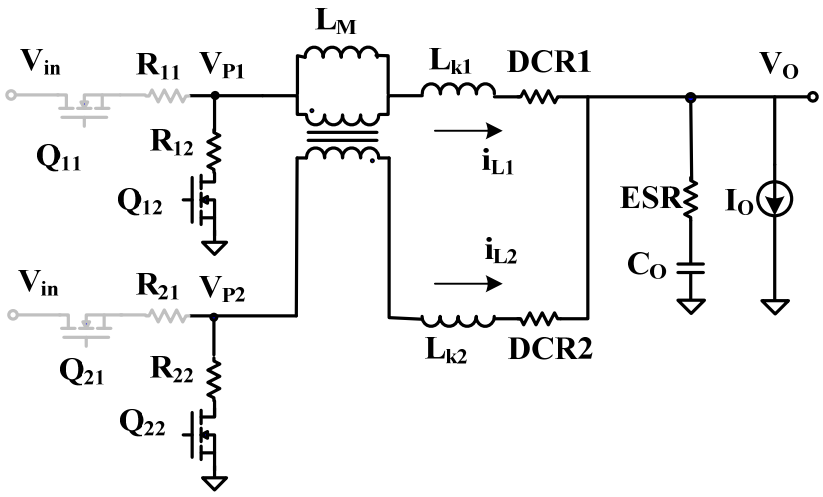


Figure 4-12. Subinterval 4, Q12 and Q22 on, Q11 and Q21 off.

During the four operational modes, the circuit components are connected differently; as a result, the respective state equation matrices A1, B1, A2, B2, A3, B3, A4, and B4 can be derived as the following:

$$A1=\begin{bmatrix} -(R_{11}+DCR_1+ESR) & -ESR & -1 \\ -ESR & -(R_{22}+DCR_2+ESR) & -1 \\ 1 & 1 & 0 \end{bmatrix} \quad B1=\begin{bmatrix} 1 & ESR \\ 0 & ESR \\ 0 & -1 \end{bmatrix} \tag{4-26}$$

$$A2=\begin{bmatrix} -(R_{12}+DCR_1+ESR) & -ESR & -1 \\ -ESR & -(R_{22}+DCR_2+ESR) & -1 \\ 1 & 1 & 0 \end{bmatrix} \quad B2=\begin{bmatrix} 0 & ESR \\ 0 & ESR \\ 0 & -1 \end{bmatrix} \tag{4-27}$$

$$A3=\begin{bmatrix} -(R_{12}+DCR_1+ESR) & -ESR & -1 \\ -ESR & -(R_{21}+DCR_2+ESR) & -1 \\ 1 & 1 & 0 \end{bmatrix} \quad B3=\begin{bmatrix} 0 & ESR \\ 1 & ESR \\ 0 & -1 \end{bmatrix} \tag{4-28}$$

$$A4=\begin{bmatrix} -(R_{12}+DCR_1+ESR) & -ESR & -1 \\ -ESR & -(R_{22}+DCR_2+ESR) & -1 \\ 1 & 1 & 0 \end{bmatrix} \quad B4=\begin{bmatrix} 0 & ESR \\ 0 & ESR \\ 0 & -1 \end{bmatrix} \tag{4-29}$$

And the corresponding matrices C1, D1, C2, D2, C3, D3, C4, and D4 are obtained as:

$$C1=C2=C3=C4=\begin{bmatrix} ESR & ESR & 1 \end{bmatrix} \quad E1=E2=E3=E4=\begin{bmatrix} 0 & -ESR \end{bmatrix} \tag{4-30}$$

Provided that the natural frequencies of the VR and the frequencies of the perturbations are much smaller than the switching frequency, the averaged matrices can be described as:

$$A=A1\cdot D+A2\cdot(\frac{1}{2}-D)+A3\cdot D+A4\cdot(\frac{1}{2}-D) \tag{4-31}$$

$$B=B1\cdot D+B2\cdot(\frac{1}{2}-D)+B3\cdot D+B4\cdot(\frac{1}{2}-D) \tag{4-32}$$

$$C=C1\cdot D+C2\cdot(\frac{1}{2}-D)+C3\cdot D+C4\cdot(\frac{1}{2}-D) \tag{4-33}$$

$$E=E1\cdot D+E2\cdot(\frac{1}{2}-D)+E3\cdot D+E4\cdot(\frac{1}{2}-D) \tag{4-34}$$

where D represents the equilibrium duty cycle. Letting $\frac{dx}{dt}$ be 0, the equilibrium state vector X can be solved by manipulating Equation 4-35:

$$X=-A^{-1}Bu \tag{4-35}$$

Since the state vector X contains the inductor DC currents and capacitor voltage, the DC solutions of the phase currents I_{L1} and I_{L2} can be obtained as:

$$I_{L1}=\frac{DCR_2+R_{21}D+R_{22}(1-D)}{DCR_1+DCR_2+R_{11}D+R_{12}(1-D)+R_{21}D+R_{22}(1-D)}\cdot I_O \tag{4-36}$$

$$I_{L2} = \frac{DCR_1 + R_{11}D + R_{12}(1-D)}{DCR_1 + DCR_2 + R_{11}D + R_{12}(1-D) + R_{21}D + R_{22}(1-D)} \cdot I_O \tag{4-37}$$

It is observed from the above DC solutions for I_{L1} and I_{L2} that:

1) DC solutions of two-phase coupled-inductor VR are exactly the same as that of two-phase non-coupled VR. Neither magnetizing inductance nor leakage inductance has effects on phase DC currents.

2) If the circuit is not symmetric, the phase with smaller R_{dson} and DCR will have a larger DC current.

The equilibrium output vector Y can be solved by substitution of the DC solutions for I_{L1} and I_{L2} into Equation 4-38:

$$Y = -CA^{-1}Bu + Eu \tag{4-38}$$

If the small ripple approximation is satisfied [44], superposition of the AC variations and the DC values leads to the state equation of the output voltage. Dropping out the DC terms and the second-order non-linear terms yields:

$$\hat{y} \cong Cx + [(C_1 - C_2)X + (E_1 - E_2)u]\hat{d} \tag{4-39}$$

where $\hat{y}$, $\hat{x}$ and $\hat{u}$ are the small AC variations of Y, x, u, and D. Let G_{vd} denote the small-signal control-to-output transfer function and neglect all the parameters such as R_{dson} and DCR. Substitution of $\hat{x}$ and manipulation of the terms lead to:

$$G_{vd} = \frac{(1 + s \cdot C_O \cdot ESR) \cdot V_{in}}{s^2 \cdot C_O \cdot (\frac{L_{k1} \cdot L_M + L_{k2} \cdot L_M + L_{k1} \cdot L_{k2}}{L_{k1} + L_{k2} + 4L_M}) + s \cdot C_O \cdot ESR + 1} \tag{4-40}$$

This is the general expression of control-to-output transfer function for VR with coupled inductors. Based on Equation 4-40, it is concluded that:

1) If the coupled inductors are ideal, i.e., L_{k1} is equal to L_{k2}, then L_M will drop out of Equation 4-40, meaning the transfer function is the same as that of a two-phase VR with discrete inductors and magnetizing inductance has no impact on the small signal model.

2) If the coupled inductors are not symmetric, magnetizing inductance L_M will exist in the control-to-output transfer function and affect the dynamic response, specifically, decreasing the LC double-pole frequency. A lower LC double-pole frequency makes compensation design more challenging, especially in computing applications where the effective capacitor equivalent serial resistance (ESR) is very small and the ESR zero is at a high frequency. It needs more effort to boost the phase margin.

3) For some advanced control scheme like APA [7], all phases can be turned on at the same time during large load transients. It behaves as if the magnetizing inductance is shorted. Thus, the transfer function can be modified as:

$$G_{vd} = \frac{(1 + s \cdot C_O \cdot ESR) \cdot V_{in}}{s^2 \cdot C_O \cdot (\frac{L_{k1} \cdot L_{k2}}{L_{k1} + L_{k2}}) + s \cdot C_O \cdot ESR + 1} \tag{4-41}$$

The magnetizing inductance term drops out of this expression and G_{vd} becomes identical to a two-phase non-coupled voltage regulator with phase inductances equal to the leakage inductances of the coupled-inductors.

4.2.2 Experimental Verification

A two-phase voltage regulator with coupled inductors was developed to verify the small-signal model of two-phase VR with coupled inductors. The circuit parameters are as follows:

V_{in} = 12 V;

V_{out} = 1.2 V;

Switching frequency = 400 kHz.

Controller: ISL6266 from Intersil;

Coupled inductors: LC1740-R30R10A from NEC/Tokin (LM = 200 nH, Lk = 110 nH);

Output capacitance: 35 x 22 uF MLCC;

The measured control-to-output transfer function is shown in Fig. 4-13. The top trace is the gain and the bottom trace is the phase. The inductor-capacitor (LC) resonant frequency is about 38 kHz. Since the coupled inductors are almost identical, the magnetizing inductance has no effect on the dynamic response. Now purposely modify the coupled inductors by adding approximately 20 nH wire to phase one. The measured power stage transfer function is shown in Fig. 4-14. The magnetizing inductance then is part of the transfer function due to the unbalance of the coupled inductors. The LC double-pole frequency is about 37 kHz. Therefore, the mathematic analysis is verified even though the effect is not significant.

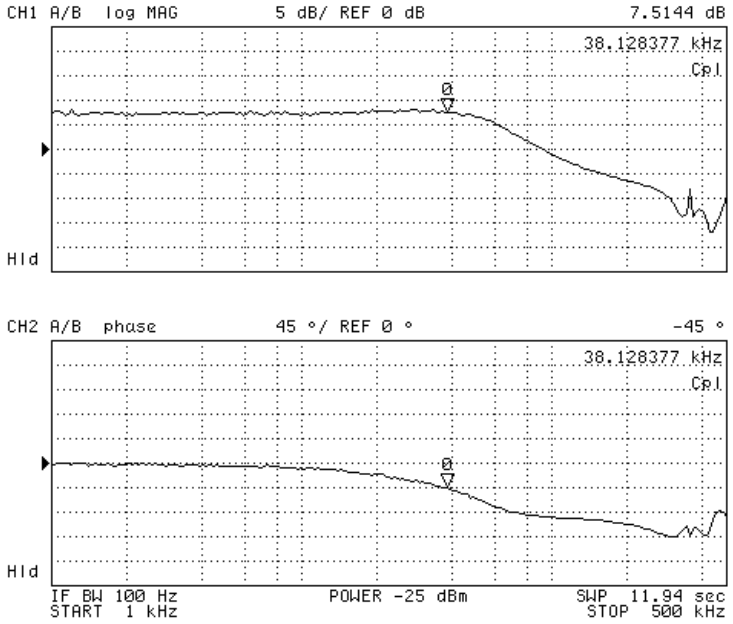


Figure 4-13. Measured power stage transfer function.

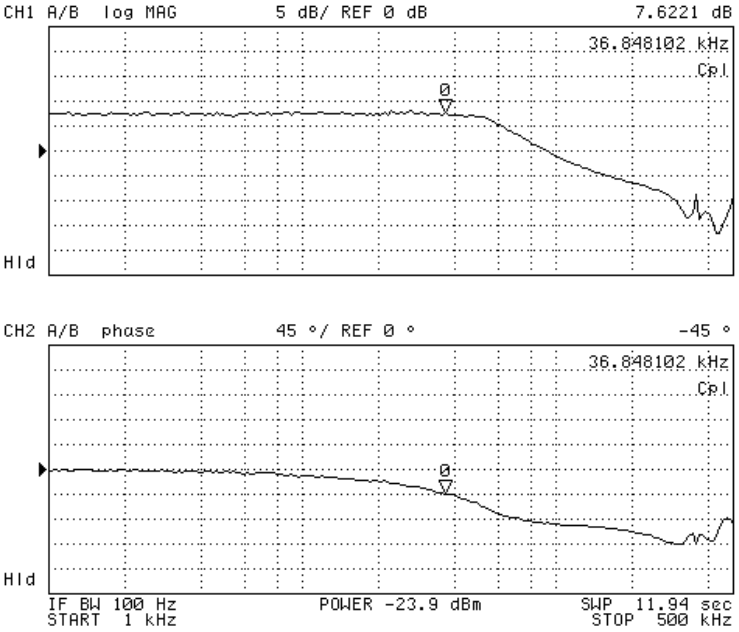


Figure 4-14. Measurement with modified coupled inductors.

4.3 New DCR Current Sensing Topologies for Coupled Inductors

4.3.1 Limitations of Conventional Current Sensing Methodologies

As technologies advance, current mode control, droop control (also referred to AVP), over-current-protection, phase-current limit and other advanced power management features are becoming common industry practices. To implement these technologies, the phase currents need to be sensed and fed back to the PWM controller as shown in Fig. 4-7. As a result, a proper current sensing technique is usually desired. Conventionally, a dedicated sense resistor is placed after the filter inductor to achieve high-accuracy current sensing. As next generation microprocessors demand more power and higher efficiency, this method becomes undesirable since it introduces significant conduction loss. Recently, the MOSFET on-resistance (R_{dson}) current sensing has been utilized in industrial products. Unfortunately the tolerance of MOSFET on-resistance usually falls in the 30% to 40% range [58]. Poor current sensing accuracy leads to phase-to-phase current imbalance. For high-current multiphase VRs, current imbalance leads to stability and thermal issues which could be disastrous. Much research has been done on various current-sensing schemes [56-61]. In recent years, inductor parasitic-resistance current sensing (also referred as DCR current sensing) prevails in the VR industry, although the concept can date back to Maxwell bridge decades ago. The inductor parasitic-resistance (DCR) current sensing method employs a resistor and a capacitor across the inductor to extract the voltage drop on the output inductor parasitic resistance. If the time constant of the resistor-capacitor (RC) network components are designed to match the inductor-DCR time constant, the voltage across the capacitor will be equal to the voltage drop across the inductor DCR, i.e., the phase current is

replicated [56]. Since the tolerance of inductor copper trace can be controlled within up to 5% with state-of-the-art fabrication process [58], the accuracy of DCR current sensing can be significantly improved compared to MOSFET R_{dson} sensing method. Additionally, despite that the RC sensing network has negligible AC losses, the DC loss on it is almost zero. Furthermore, the overall cost of the RC network is even smaller than a sense resistor. Thus, as a cost-effective practice, DCR sensing is widely implemented in VR applications. However, even though DCR current sensing has been well investigated for discrete inductors, little work has been done on current sensing for coupled inductors. In most coupled-inductor applications, the traditional DCR sensing method is simply applied to coupled inductors. The RC network is designed based on the leakage inductance while the magnetizing inductance is neglected. Since, the phase currents of coupled inductors are different than those of discrete inductors due to the presence of magnetizing inductance and coupling effect, the application of conventional DCR current sensing to coupled inductors is questionable. Fig. 4-15 shows a two-phase coupled-inductor VR with traditional DCR current sensing topology, in which V_{P1} and V_{P2} represent the phase voltages (referring to V_O); R_1, C_1, R_2, and C_2 are the RC current-sensing network components. The other components are the same as in Fig. 4-8.

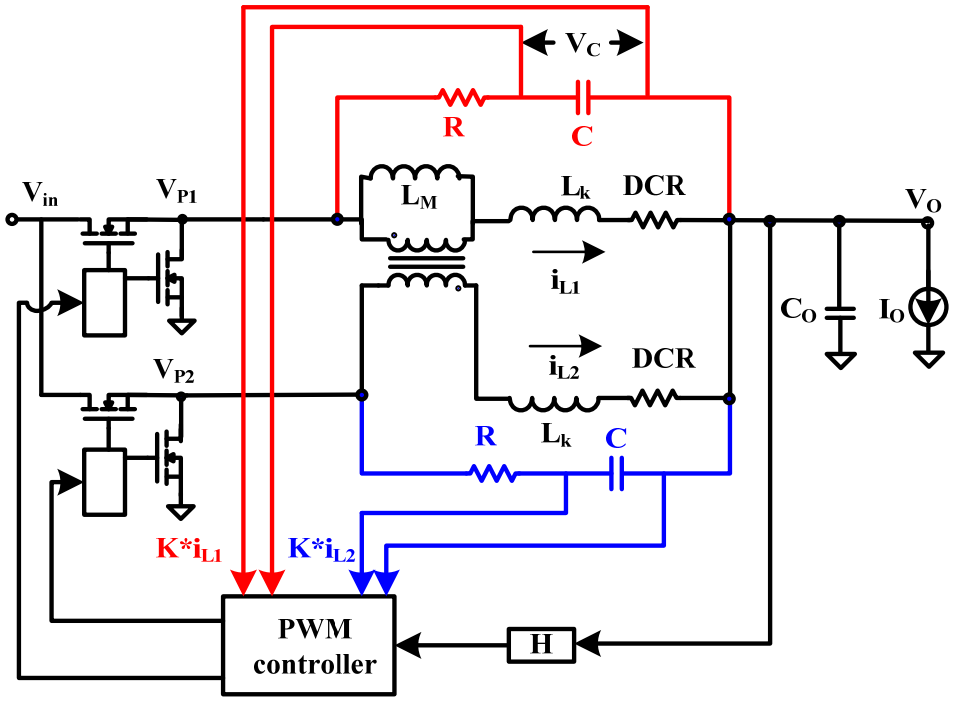


Figure 4-15. Coupled inductors with traditional DCR current sensing topology.

Assuming the coupled inductors are symmetric, the phase voltage V_{P1} can be given in s-domain by:

$$V_{P1} = s(L_k + L_M)\cdot i_{L1} - sL_M \cdot i_{L2} + DCR \cdot i_{L1} \tag{4-42}$$

Since V_{P1} is also the voltage across R and C, the voltage across C for phase 1 can be expressed as:

$$V_{C1} = \frac{s(L_k + L_M)\cdot i_{L1} - sL_M \cdot i_{L2} + DCR \cdot i_{L1}}{1 + sR \cdot C} \tag{4-43}$$

Rearranging the equation, we have:

$$V_{C1} = \left(\frac{1 + s \cdot \frac{L_k}{DCR}}{1 + sR \cdot C}\right) \cdot DCR \cdot i_{L1} + \frac{sL_M \cdot (i_{L1} - i_{L2})}{1 + sR \cdot C} \tag{4-44}$$

For DCR current sensing, the RC time constant has to match the inductor time constant, i.e. RC should be equal to L/DCR. Equation 4-44 can be then simplified as:

$$V_{C1} = DCR \cdot i_{L1} + \frac{sL_M \cdot (i_{L1} - i_{L2})}{1 + sR \cdot C} \tag{4-45}$$

The first term represents the voltage drop across DCR while the second term cannot be cancelled out due to the magnetizing inductance L_M. Careful examination of the second term leads to the discovery that it is a frequency-dependent quantity. Therefore, Equation 4-45 suggests that traditional DCR current sensing scheme cannot extract the correct phase current information. Instead, it is the superposition of the phase current and the additional AC component.

To investigate the total sensed current, phase 2 current is derived in the same manner. Taking the vector sum of the two VCs yields:

$$I_{Total} = DCR \cdot i_{L1} + DCR \cdot i_{L2} + \frac{sL_M \cdot (i_{L1} - i_{L2})}{1 + sR \cdot C} + \frac{sL_M \cdot (i_{L2} - i_{L1})}{1 + sR \cdot C} \tag{4-46}$$

Manipulating the above equation leads to:

$$I_{Total} = DCR \cdot (i_{L1} + i_{L2}) \tag{4-47}$$

It is found in Equation 4-47 that the total sensed current is a replica of the total output current. Thus, the following conclusions can be made based on the above analysis:

1) Even though the DC portion of phase current can be sensed correctly by DCR current-sensing circuit as in the non-coupled inductors case, it fails to represent the total phase current. Instead, it is the total phase current superposed by an extra AC component.

2) The total inductor current can be obtained accurately by the conventional DCR Current Sensing circuit.

Conventional DCR current sensing circuit is built on the board to show its limitations. Measured current waveforms are shown in Fig. 4-16. The top waveform shows the sensed phase current by traditional DCR sensing and the bottom waveform represents the real phase current. It is obvious that the sensed current is distorted. Consequently, wrong phase current information was obtained. This incorrect current may lead to improper phase over-current-protection (OCP) as well as inferior current and voltage regulation.

A current sensing method was proposed in [57] for coupled inductors. It was claimed to be able to sense the total current accurately. Nevertheless, it fails to represent the phase currents as a conventional technique does. Motivated by the demand of a cost-effective current sensing technique for coupled inductors, two new DCR current-sensing topologies are proposed in this paper. By implementation of a simple RC network, the phase currents as well as total current can be extracted. The design equations for the RC sensing network are derived by step-by-step mathematic analysis. These equations are given in terms of leakage inductance and magnetizing inductance since these coefficients are usually provided in the coupled-inductor datasheets by

vendors [24]. Sensitivity and mismatch issues are addressed. A prototype has been built to verify the theoretic results.

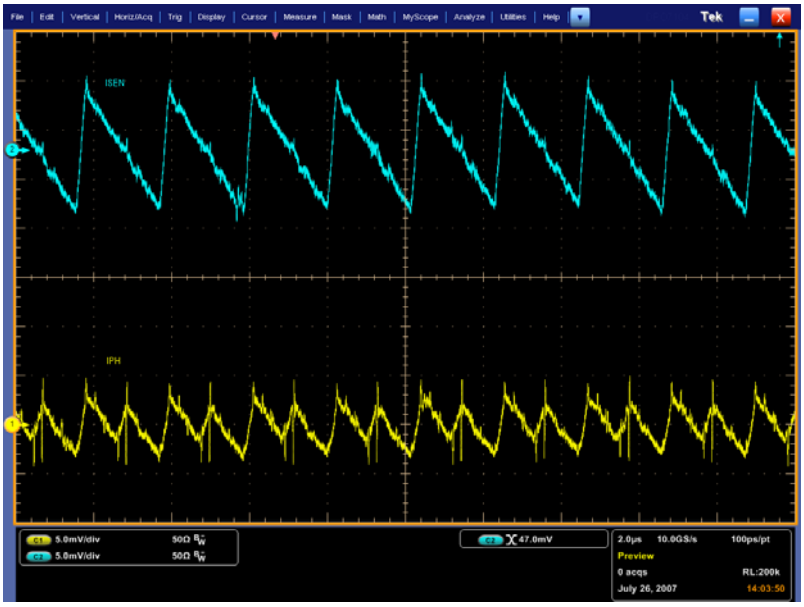


Figure 4-16. Comparison of sensed current and real current by experiments.

4.3.2 Proposed Topology I

Fig. 4-17 shows the first proposed DCR current sensing topology I for two-phase coupled inductors. The coupled-inductor model in Fig. 4-7 is again adopted here. Topology I consists of a resistor R, a capacitor C for each phase, and three other resistors R_1, R_2, R_1 which are shared by the two phases. Under some circumstances, it may be necessary to use a resistor divider to scale down the sensed current or to compensate the temperature variation. This can be accomplished by placing a resistor R_C in parallel with the capacitor C for each phase. By properly sizing the

resistor and capacitor values in this topology, the phase current can be represented by the voltage across C, i.e. V_C. V_C is then sent to a current amplifier inside the PWM controller for current and voltage regulation.

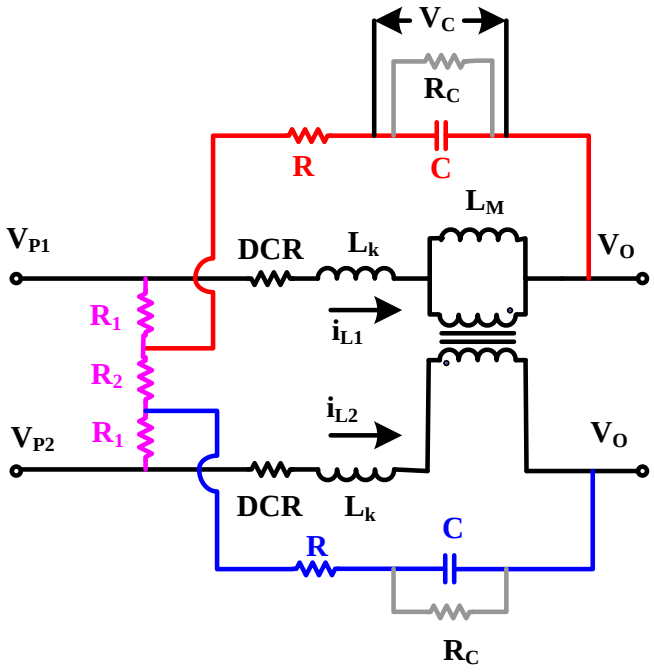


Figure 4-17. Proposed DCR Current Sensing topology I for two-phase coupled inductors.

Mathematical analysis will show how this current sensing topology works and how to design the circuit parameters. Letting V_{P1} and V_{P2} denote the phase voltages (referring to V_O), and assuming the coupled inductors are symmetric, the phase voltages V_{P1} and V_{P2} can be given in s-domain by:

$$V_{P1} = s(L_k + L_M)\cdot i_{L1} - sL_M \cdot i_{L2} + DCR \cdot i_{L1} \tag{4-48}$$

$$V_{P2} = s(L_k + L_M) \cdot i_{L2} - sL_M \cdot i_{L1} + DCR \cdot i_{L2} \tag{4-49}$$

Solving Equation 4-49 for i_{L2} leads to

$$i_{L2} = \frac{V_{P2} + s \cdot L_M \cdot i_{L1}}{s \cdot (L_k + L_M) + DCR} \tag{4-50}$$

Substitution of Equation 4-50 into Equation 4-48 yields:

$$V_{P1} = s \cdot (L_k + L_M) \cdot i_{L1} - s \cdot L_M \cdot \frac{V_{P2} + s \cdot L_M \cdot i_{L1}}{s \cdot (L_k + L_M) + DCR} + DCR \cdot i_{L1} \tag{4-51}$$

Rearranging Equation 4-51 we have:

$$i_{L1} = \frac{V_{P1} \cdot \left[s \cdot (L_k + L_M) + DCR \right] + s \cdot L_M \cdot V_{P2}}{\left[s \cdot (L_k + L_M) + DCR \right]^2 - s^2 \cdot {L_M}^2} \tag{4-52}$$

Assuming the current sensing resistor R is much bigger than R_1 and R_2, and if R_C is not stuffed (in that case the current scale down is not necessary), the voltage across current sensing capacitor C for phase one can be expressed as:

$$V_C = \frac{\frac{V_{P1} \cdot R_1}{2R_1 + R_2} + \frac{V_{P2} \cdot R_2}{2R_1 + R_2}}{1 + s \cdot R \cdot C} \tag{4-53}$$

In order for V_C to represent the voltage drop across DCR, the following equation must be met:

$$i_{L1} \cdot DCR = V_C \tag{4-54}$$

Manipulation of Equations 4-52, 4-53, and 4-54 leads to:

$$\frac{V_{P1} \cdot R_1 + V_{P2} \cdot R_2}{DCR \cdot (2R_1 + R_2) \cdot (1 + sRC)} = \frac{[s(L_k + L_M) + DCR] \cdot V_{P1} + sL_M \cdot V_{P2}}{[s(L_k + L_M) + DCR]^2 - s{L_M}^2)} \tag{4-55}$$

Since the normal switching frequency of VR falls in hundreds of kilohertz range, the term $s(L_k+L_M)$ is usually much greater than DCR, Equation 4-55 can be de-coupled into two equations by dropping off V_{P1} and V_{P2}. The two equations can then be rearranged as:

$$\frac{R_1 \cdot (1 + s\frac{L_k}{DCR})}{(2R_1 + R_2) \cdot (1 + sRC)} = \frac{L_k + L_M}{L_k + 2L_M} \tag{4-56}$$

$$\frac{R_2 \cdot (1 + s\frac{L_k}{DCR})}{(2R_1 + R_2) \cdot (1 + sRC)} = \frac{L_M}{L_k + 2L_M} \tag{4-57}$$

The design equations for topology one are obtained by solving Equations 4-56 and 4-57:

$$\frac{R_1}{2R_1 + R_2} = \frac{L_M}{L_k + 2L_M} \tag{4-58}$$

$$\frac{L_k}{DCR} = RC \tag{4-59}$$

The above analysis suggests that if the resistors and capacitors in topology one are designed properly such that Equations. 4-58 and 4-59 are satisfied, then by reversing the derivation procedure, Equation 4-54 can be obtained, which means that the voltage across C is a replica of the voltage across the inductor DCR, i.e., the phase current is duplicated. Therefore, Equations 4-58 and 59 can serve as the design equations for the proposed current sensing topology. For some applications in which the DCR voltage drop is too high or temperature compensation is desired, a scale-down resistor R_C is usually placed in parallel with C. In this case, V_C is a scaled version of the DCR voltage. Supposing the sensing gain to be K, the following equations can be obtained:

$$i_{L1} \cdot DCR = K \cdot V_C \tag{4-60}$$

$$K = \frac{R_C}{R + R_C} \tag{4-61}$$

It must be noted that two assumptions are made for topology I to work. One is that the current sensing resistor R is much bigger than R_1 and R_2, and the other is that $s(L_k+L_M)$ and sL_M are much greater than DCR. If these two assumptions are not satisfied, the sensed current by this topology will be invalid.

4.3.3 Proposed Topology II

The second proposed topology is shown in Fig. 4-18. It has two resistors and a capacitor C for each phase. R_1, R_2 are for phase one and R_3, R_4 are for phase two, respectively. In a similar manner, the design equations for topology two can be derived. It is found that Equations 4-48 through 4-52 are applicable to topology II.

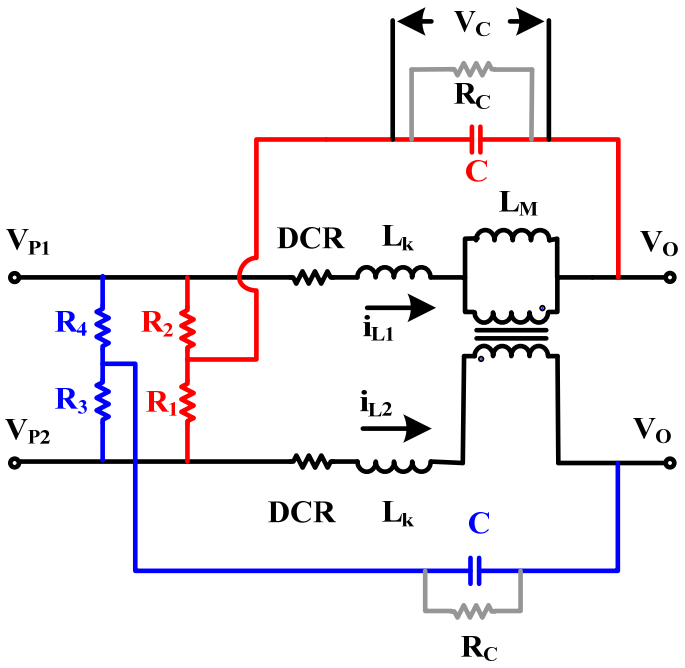


Figure 4-18. Proposed DCR Current Sensing topology II for two-phase coupled inductors.

Let's take a look at the case without scale-down where the voltage across the current sensing capacitor C for phase 1 is:

$$V_C = \frac{\frac{R_1}{1+sR_1 \cdot C_1}}{\frac{R_1}{1+sR_1 \cdot C} + R_2} \cdot V_{P1} + \frac{\frac{R_2}{1+sR_2 \cdot C_1}}{\frac{R_2}{1+sR_2 \cdot C} + R_1} \cdot V_{P2} \tag{4-62}$$

If Equation 4-54 is satisfied, then V_C can represent the phase current. Equation 4-62 becomes:

$$\frac{R_1}{R_1 + R_2 + sR_1 \cdot R_2 \cdot C} \cdot V_{P1} + \frac{R_2}{R_1 + R_2 + sR_1 \cdot R_2 \cdot C} \cdot V_{P2} = \frac{V_{P1} \cdot [s \cdot (L_k + L_M) + DCR] + s \cdot L_M \cdot V_{P2}}{[s \cdot (L_k + L_M) + sL_M + DCR](sL_k + DCR)} \cdot DCR \tag{4-63}$$

For high-current applications, phase inductors usually have small DCR. Therefore, $s(L_k+L_M)$ and sL_M are much greater than DCR. By simplifying Equation 4-63, it can be broken into:

$$\frac{R_1 \cdot (1 + s\frac{L_k}{DCR})}{(R_1 + R_2) \cdot (1 + s\frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C)} = \frac{L_k + L_M}{L_k + 2L_M} \tag{4-64}$$

$$\frac{R_2 \cdot (1 + s\frac{L_k}{DCR})}{(R_1 + R_2) \cdot (1 + s\frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C)} = \frac{L_M}{L_k + 2L_M} \tag{4-65}$$

Thus, the design equations for topology II are obtained as:

$$\frac{R_1}{R_1 + R_2} = \frac{L_k + L_M}{L_k + 2L_M} \tag{4-66}$$

$$\frac{L_k}{DCR} = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C \tag{4-67}$$

Therefore, if the topology II is designed according to Equations 4-66 and 4-67, by reversing the derivation procedure, it is found that the voltage V_C is exactly equal to the phase current. Since topology II has only one assumption made, theoretically it is more accurate than topology I since the latter needs to satisfy two assumptions.

In some cases where scale-down of the sensed voltage is necessary, the resistor R_C is added in parallel with the current sensing capacitor C. With the presence of R_C, the design equations changes to:

$$\frac{L_k}{DCR} = \frac{R_1 \cdot R_2 \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + R_1 \cdot R_2} \cdot C \tag{4-68}$$

$$\frac{R_1}{R_1 + R_2} = \frac{L_k + L_M}{L_k + 2 \cdot L_M} \tag{4-69}$$

$$K = \frac{(R_1 + R_2) \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + R_1 \cdot R_2} \tag{4-70}$$

where K is the scale-down factor.

4.3.4 Multiphase Application of Proposed Topology II

Both topology I and topology II are intended for two-two coupled-inductor applications for their generality. For applications in which multiphase inductors are wound on a single core, topology II can further be modified to a multiphase configuration as shown in Fig. 4-19. Therefore, topology II shows its advantage over topology I. Similar to the topology II for two-phase application, phase N has a resistor R_N, a capacitor C, and an optional R_C for scale-down purpose. The other phase voltage information is obtained by connecting a resistor to each phase. If the phase resistors are designed properly, the phase current can be sensed accurately. With the assumption that $s(L_k+L_M)$ and sL_M are much greater than DCR, the design equations can be given as:

$$\frac{L_k}{DCR} = \frac{R_1 \cdot R_2 \cdots R_N \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + \cdots + R_N \cdot R_C + R_1 \cdot R_2 \cdots R_N} \cdot C \tag{4-71}$$

$$\frac{R_1}{R_1 + R_2 + \cdots + R_N} = \frac{L_k + L_M}{L_k + N \cdot L_M} \tag{4-72}$$

$$K = \frac{(R_1 + R_2 + \cdots + R_N) \cdot R_C}{R_1 \cdot R_C + R_2 \cdot R_C + \cdots + R_N \cdot R_C + R_1 \cdot R_2 \cdots R_N} \tag{4-73}$$

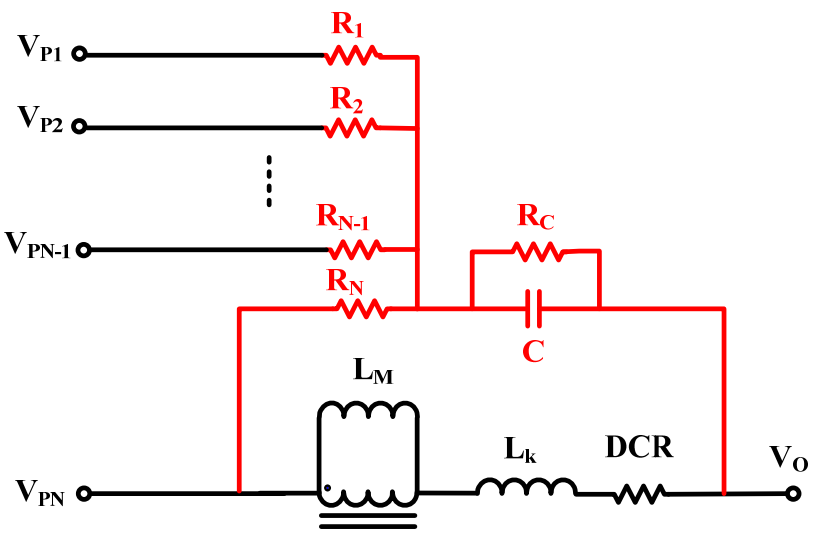


Figure 4-19. Proposed DCR Current Sensing topology for N-phase coupled inductors.

4.3.5 Sensitivity and mismatch analysis

The above analysis has assumed ideal coupled inductors with known, matched coefficients. In practice, it is difficult to obtain accurate values of the parasitic resistance, which varies with frequency, proximity effects (and therefore current), temperature, etc. And it would not be expected to be balanced among windings in a given inductor. The other parameters such as leakage inductance and magnetizing inductance have tolerance up to 30% and can also change with time as magnetic materials cycle and age. With the tolerance and mismatch issues, the sensed current signal may be distorted. Therefore, it is necessary to evaluate the sensitivity and mismatch effects on sensed currents. Since the tolerance of the RC sensing components is typically as low as 1%, the discussion will be focused on the coupled inductor coefficients only.

With proposed topology II as an example and letting the variations of the leakage inductance, magnetizing inductance, DCR to be dL_k, dL_M, dDCR, and the resulted voltage deviation on sensing capacitor C to be dV_C, respevtively, then the effect of each specific coefficient on the sensed current can be analyzed by adding the variations into above equations and solving for dV_C. If the current sensing sensitivity ratio is defined as the sensing deviation dV_C over the correct voltage V_C on the sensing capacitor, then for leakage inductance variation dL_k:

$$\frac{dV_C}{V_C} = \frac{dL_k}{L_k} \frac{1}{(1 + \frac{R_1 + R_2}{s \cdot R_1 \cdot R_2 \cdot C})} \tag{4-74}$$

For magnetizing inductance, the sensitivity ratio is obtained as:

$$\frac{dV_C}{V_C} = \frac{dL_M}{L_M} \cdot \frac{R_2}{R_1 - R_2} \cdot \frac{1}{(1 + \frac{R_1 + R_2}{s \cdot R_1 \cdot R_2 \cdot C})} \tag{4-75}$$

The sensitivity ratio for DCR can be given as:

$$\frac{dV_C}{V_C} = \frac{dDCR}{DCR + dDCR} \cdot \frac{1}{(1 + \frac{s \cdot R_1 \cdot R_2 \cdot C}{R_1 + R_2})} \tag{4-76}$$

Equations 4-74, 4-75 and 4-76 suggest that coefficient variations result in current sensing errors and the errors vary with frequency. To demonstrate sensitivity of each coefficient, the coupled inductor LC1740-R30R10A from NEC/Tokin is employed as an example. According to design equations in Equations 4-66 and 4-67, the current sensing values as well as the inductor coefficient are given in Table 4-1.

Table 4-1. Coefficients of LC1740-R30R10A and current sensing values.

Leakage L (nH)	Magnetizing L (nH)	DCR (mohm)	R_1 (kohm)	R_2 (kohm)	C (uF)
110 +/- 30%	200 +/- 30%	0.4 +/- 5%	3.1	2	0.22

Based on Equations 4-74, 4-75 and 4-76, normalized sensitivity ratio (sensitivity ratio over tolerance) of the coefficients can be plotted versus frequency in Mathcad as shown in Fig. 4-20.

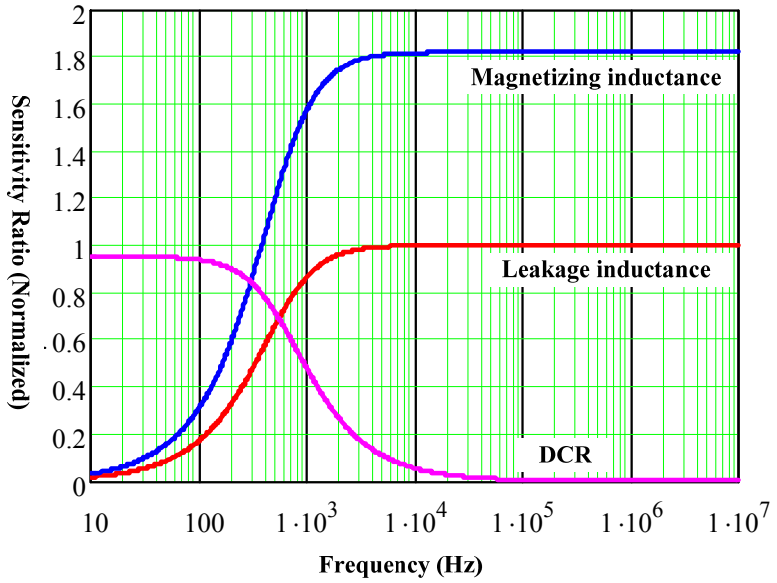


Figure 4-20. Normalized sensitivity ratio for leakage inductance, magnetizing inductance, and DCR.

It can be concluded from Fig. 4-20 that:

1. The tolerance of magnetizing inductance is amplified by around 1.8 times at high frequencies, indicating the AC portion of the sensed current waveform will be distorted if the magnetizing inductance data is not accurate enough. However, it has little effect on the DC level of sensed current.

2. The deviation of sensed current is almost proportional to the leakage inductance tolerance at high frequencies. Similar to the magnetizing inductance, it has limited impact on the DC current level.

3. This topology is sensitive to DCR tolerance at DC (low frequencies), and the sensed current deviation is nearly proportional to the DCR tolerance. At high frequencies, DCR tolerance has negligible effect on sensed current.

As a common industry practice, a thermal resistor R_C as shown in Fig. 4-18 is usually placed close to the inductor to compensate the DCR temperature variation. Therefore, the DC current sensing error can be controlled within acceptable range if the topology is designed properly. The AC portion of sensed current may have errors that stem from leakage and magnetizing inductance tolerance.

4.3.6 Simulation Results

A 500 kHz two-phase coupled-inductor VR with conventional DCR current sensing scheme and proposed topologies are built in Simplis simulator to verify the above mathematical analysis. The component values and coefficients of the topology are listed in Table 4-2, The simulation parameters are as the follows:

V_{in} = 12 V;

V_{out} = 1.2 V;

Switching frequency = 400 kHz;

Coupled inductors: L_M = 500 nH, L_k = 200 nH, DCR = 2 mohm);

Output capacitance: 700 uF.

Table 4-2. Current sensing component values for Simplis simulation.

	R	C	R_1	R_2
Conventional Topology	10 kohm	10 nF	N/A	N/A
Proposed Topology I	10 kohm	10 nF	500 ohm	200 ohm
Proposed Topology II	N/A	10 nF	24 kohm	17 kohm

Figs. 4-21 shows Simplis simulation results for the two-phase coupled-inductor VR with conventional DCR current sensing scheme. It is found that conventional DCR sensing method fails to predict the phase currents. The sensed peak currents are much greater than the real peak currents. The false current information may trigger a wrong protection function and lead to inferior current regulation. Fig. 4-22 and Fig. 4-23 show the Simplis simulation results with

proposed topology I and topology II during steady-state, respectively. Both topologies can sense phase currents accurately. Fig. 4-24 shows dynamic performance of the proposed topology II. It is evident that the sensed current waveforms are almost identical to the real current waveforms during both steady-state and transient. Thus, the proposed topologies are verified to be capable of sensing the phase currents accurately.

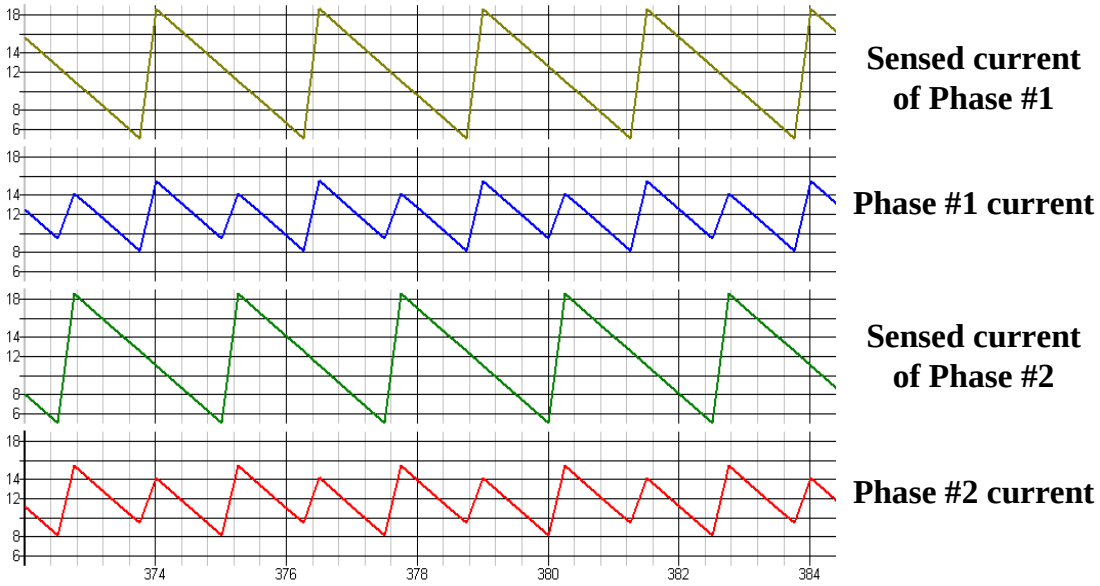


Figure 4-21. Simplis simulations for conventional DCR current sensing. System parameters: V_{in} = 12V, V_O = 1.2V, L_k = 200 nH, L_M = 500 nH, DCR = 2 mohm, C_O = 660 uF.

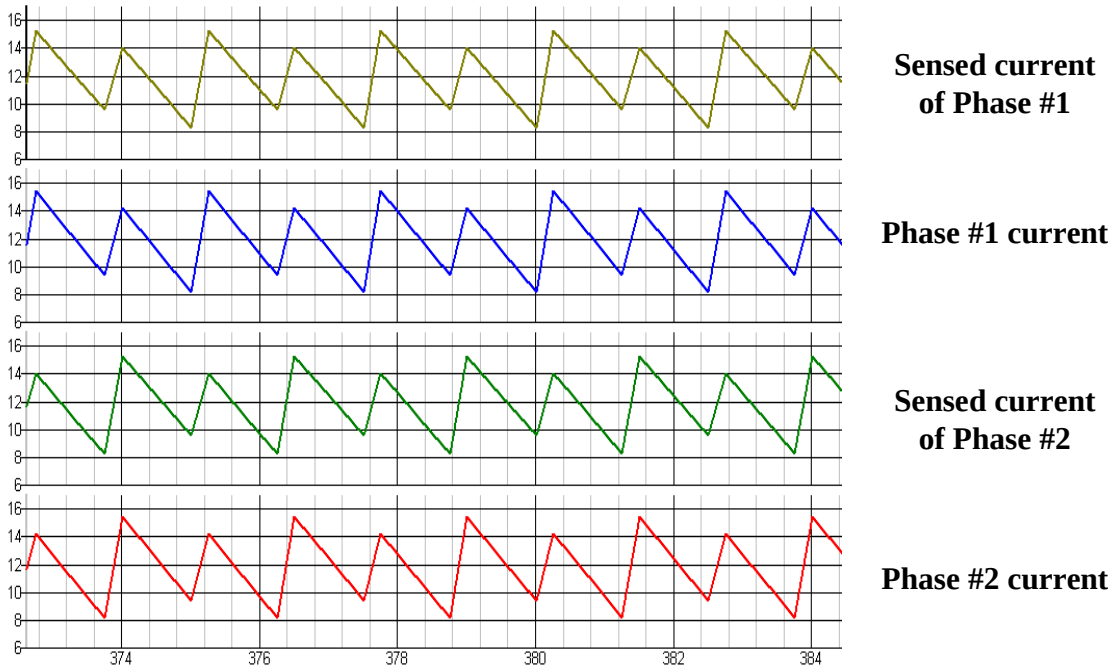


Figure 4-22. Simplis simulations for proposed topology I. System parameters: V_{in} = 12V, V_O = 1.2V, L_k = 200 nH, L_M = 500 nH, C_O = 660 uF.

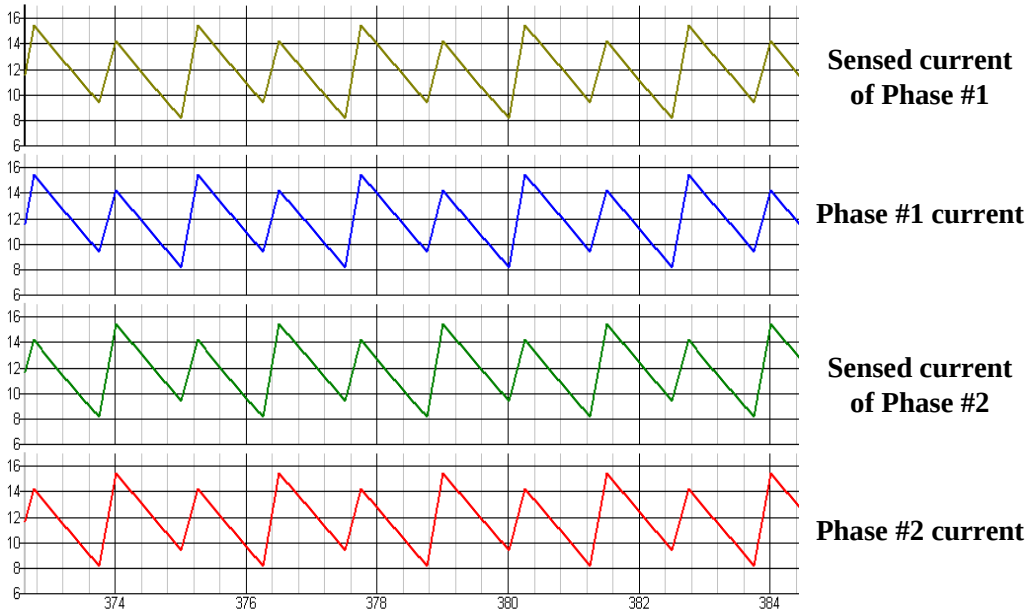


Figure 4-23. Simplis simulations for proposed topology II. System parameters: V_{in} = 12V, V_O = 1.2V, L_k = 200 nH, L_M = 500 nH, C_O = 660 uF.

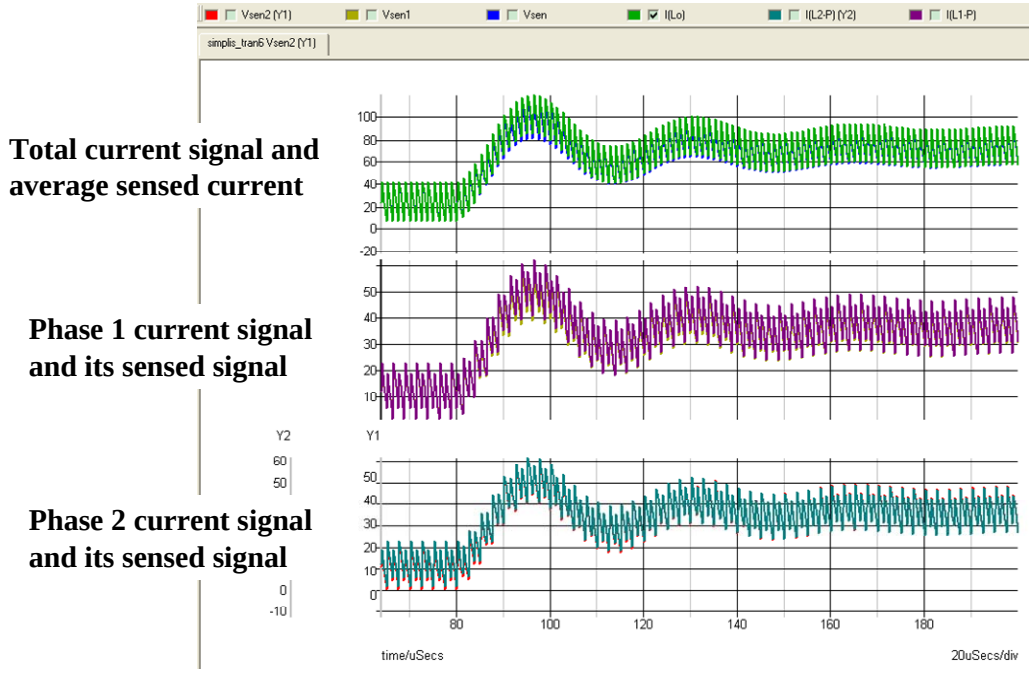


Figure 4-24. Simplis simulations for proposed topology II during transient. System parameters: V_{in} = 12V, V_O = 1.2V, Lk = 200 nH, L_M = 500 nH, C_O = 660 uF. I_{step} = 20A to 70A.

4.3.7 Experimental Verification

A two-phase voltage regulator with coupled inductors has been developed to verify the proposed topologies and mathematical analysis. The system parameters are listed as the follows:

V_{in} = 12 V;

V_{out} = 1.2 V;

Switching frequency = 400 kHz.

Controller: ISL6266 from Intersil;

Coupled inductors: LC1740-R30R10A from NEC/Tokin (LM = 200 nH, Lk = 110 nH, DCR = 0.4 mohm);

Output capacitance: 35 x 22 uF MLCC.

The experimental results for topology I are shown in Fig. 4-25 while Fig. 4-26 shows the experimental results for topology II. The current sensing parameters for topology II are: R_1 = 3.1 kohm, R_2 = 2 kohm, C = 0.22 uF. From top to bottom, the first waveforms represent the sensed current by the proposed topologies and the second waveforms are captured by a current probe, respectively. The other waveforms are the PWM switching waveforms. Based on the experimental results, it is found that the sensed currents agree with the real currents in terms of DC level. The AC portion (valley current) is distorted a little because of the tolerance of leakage and magnetizing inductance. The high-frequency jitters on the sensed waveforms are random noise resulting from measurement.

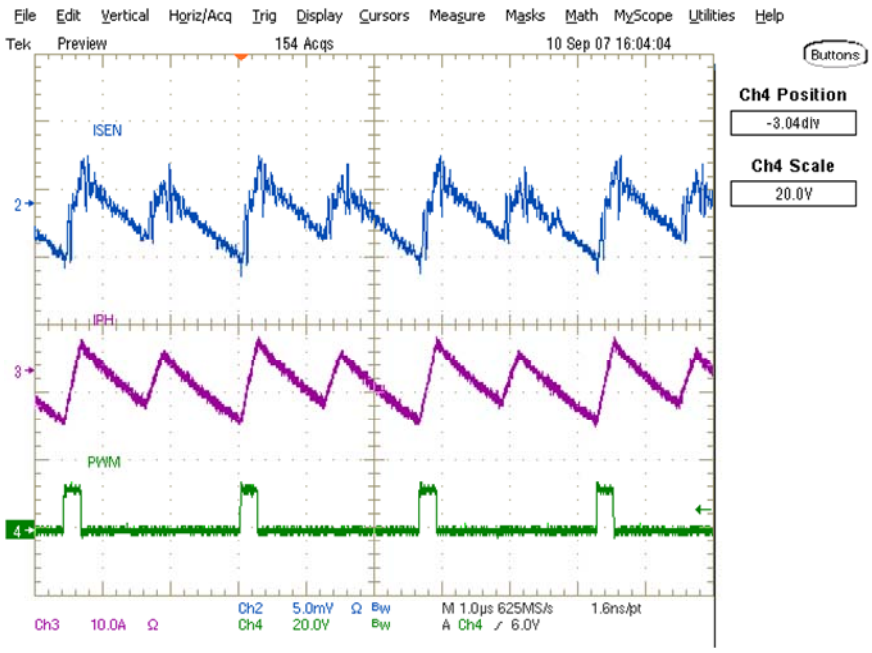


Figure 4-25. Experimental current waveforms for proposed topology I.

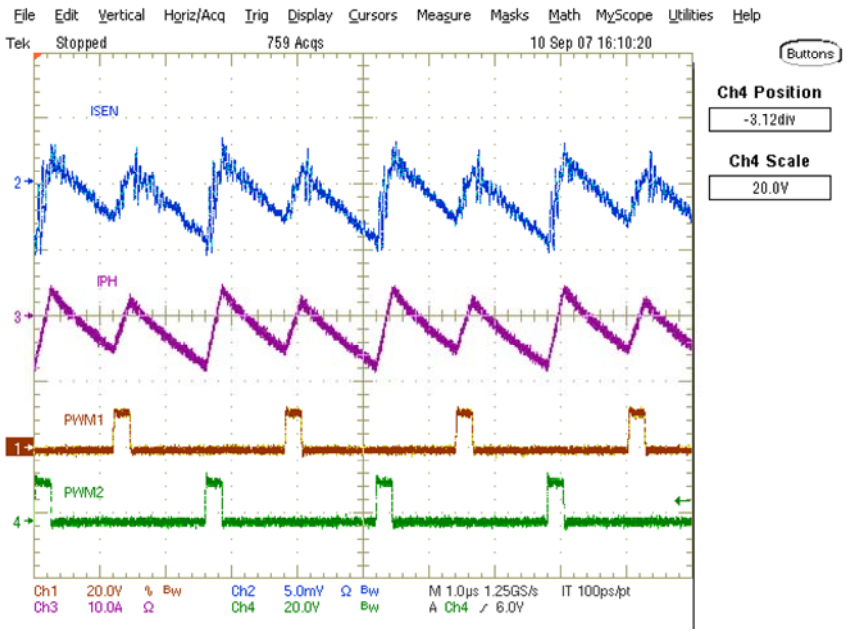


Figure 4-26. Experimental current waveforms for proposed topology II.

4.3.8 Summary

Two current sensing topologies for coupled inductors have been proposed in this dissertation. By implementation of simple RC networks, the phase coupling information can be preserved. Therefore, they are capable of sensing phase currents and total current accurately and efficiently for VRs with coupled inductors. Mathematic analysis and design formula were presented in detail. Simulation and experimental results were also included to verify the proposed topologies.

4.4 New Topologies of VR with Coupled Inductors

The ever-stringent requirements of CPU regulation impose a harsh challenge for voltage regulator designers on how to further improve both dynamic and steady state performance. It is well known that there is a dilemma for the output inductance expectation for both fast transient response and low steady-state current ripple [37]. A low inductance allows a high current slew rate to respond to the load demand quickly. Therefore, it is more preferable to reduce the equivalent phase inductor to achieve a fast current slew rate during transient events. However, a small inductance also leads to large ripple currents and associated large root-mean-square (RMS) currents [37-39]. High RMS current associated with the large current ripple results in high power losses and high-rating device requirements. As a result, VR designers have to deal with increased power losses and higher-rating device requirements. One way to reduce the ripple current is to increase the switching frequency. However, as the switching frequency increases, the switching and driving losses will increase as well. Furthermore, higher switching frequency imposes new

requirements for magnetic materials capable of operating with low loss at high frequencies and thermal management [37].

As one of the benefits, coupled inductors can increase the equivalent switching frequency on each phase. Assuming the phase inductance in the non-coupled inductor configuration is equal to the equivalent leakage inductance in the coupled inductor configuration, the phase ripple current of coupled-inductor VR is much smaller than the conventional non-coupled configuration [39] [40], although the total output current ripple in the coupled inductor configuration is almost the same as that in the conventional non-coupled inductor configuration. As a result, the inductor copper loss, MOSFET conduction loss, and switching loss are less with coupled inductors. On the other hand, the core losses of the inductors can also be reduced due to the flux cancellation effect as shown in previous analysis. Therefore, significant power losses are saved with coupled inductors. A typical topology of a two-phase voltage regulator with coupled inductors is illustrated in Fig. 4-27.

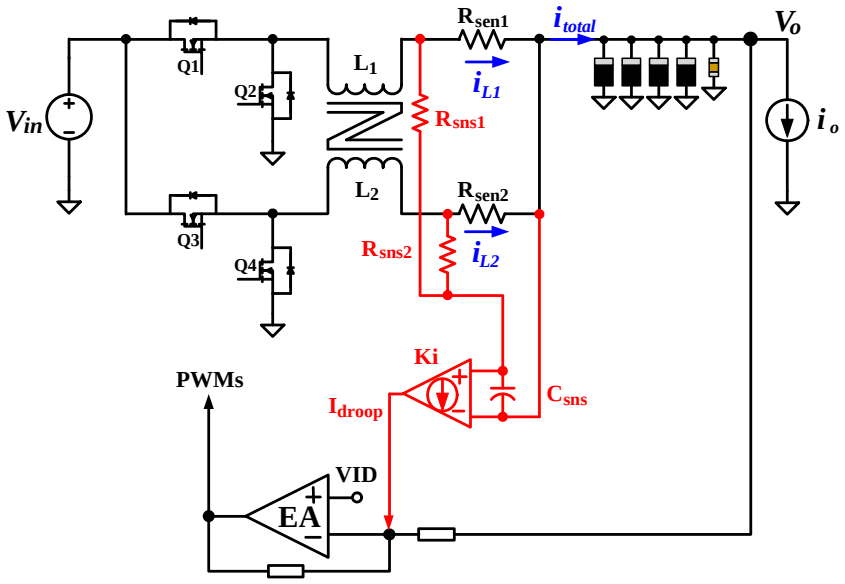


Figure 4-27. Two-phase voltage regulator with coupled inductors.

4.4.1 Review of Prior Arts for Coupled-inductor Topologies

Much work has been done on various coupled-inductor topologies. A coupled-inductor topology is presented in [38] [48] [49] as shown in Fig. 4-28. In this topology, all phases are coupled on a single “ladder core”, in a way that results in significant space saving. Since all phases share a low reluctance common path, it ensures good coupling. In addition, the orientation of windings yields DC flux cancellation to allow high current without saturation. Moreover, each phase has a high reluctance path giving small leakage inductance per phase. While this feature makes the transient response faster, it suffers from high power loss induced by high peak to peak phase current due to asymmetric coupling and reduced phase inductance. To reduce the ripple current, the leakage inductance as well as the core size has to be increased. Thus, a tradeoff has to be

made between leakage inductance and overall device footprint. Meanwhile, the centralized core structure also sacrifices the flexibility of layout.

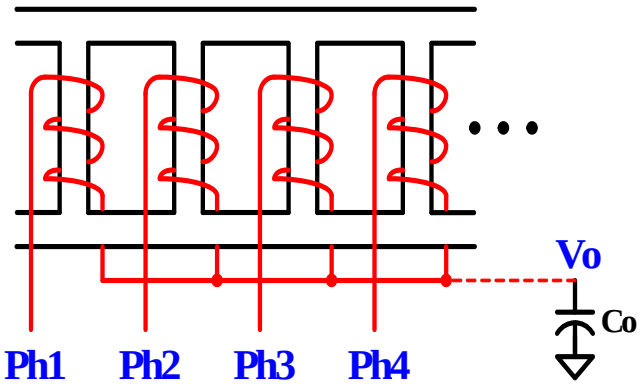


Figure 4-28. Multiphase coupled inductors with a ladder core.

A series coupled-inductor is shown in Fig. 4-29 [42]. From a circuit point of view, this topology is essentially equivalent to the "ladder core" coupled-inductor version. The main difference lies in that, compared to the ladder core structure, the series coupled-inductor topology employs distributed cores. This feature makes it suitable for VR applications in which all phases need to be distributed far away from one another. Another advantage of this topology is that the coupling between phases is symmetrical. Therefore, the current ripple as well as the output voltage ripple is even. Nevertheless, long windings are needed for this topology. As a result, the DC losses are increased. Again, due to the coupling between phases, only phase leakage inductances function as the filter inductances. For the same reason, it suffers low steady-state efficiency as the "ladder core" topology does.

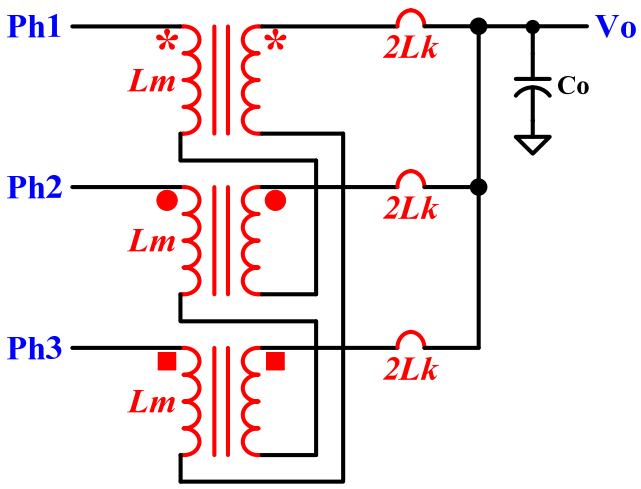


Figure 4-29. A series coupled-inductor topology.

Virginia Tech (CPES) proposes a secondary-loop coupled-inductor topology as shown in Fig. 4-30 [55]. In this topology, a secondary winding is utilized to couple all phases together. Compared to the above two topologies, it offers both layout flexibility and symmetric coupling. However, an extra secondary winding consumes significant power. Further more, the DCM self-turn-on problem [55] is left unresolved.

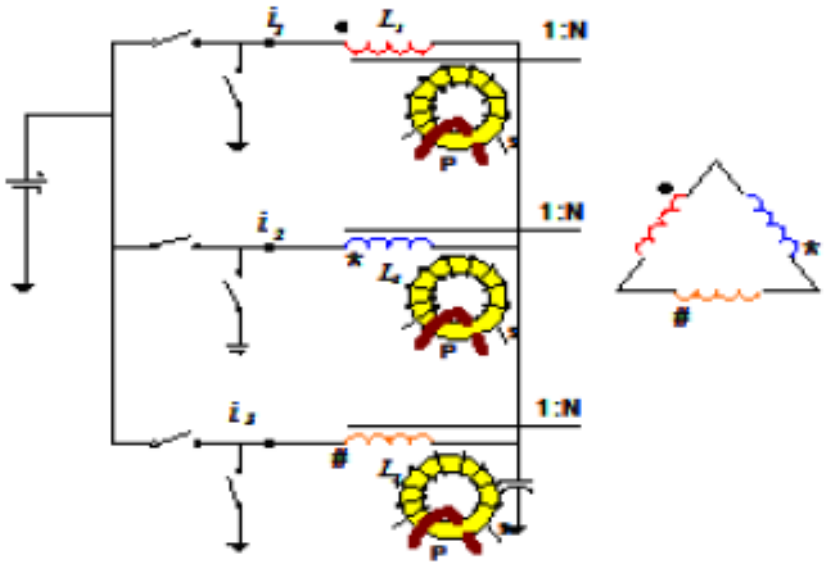
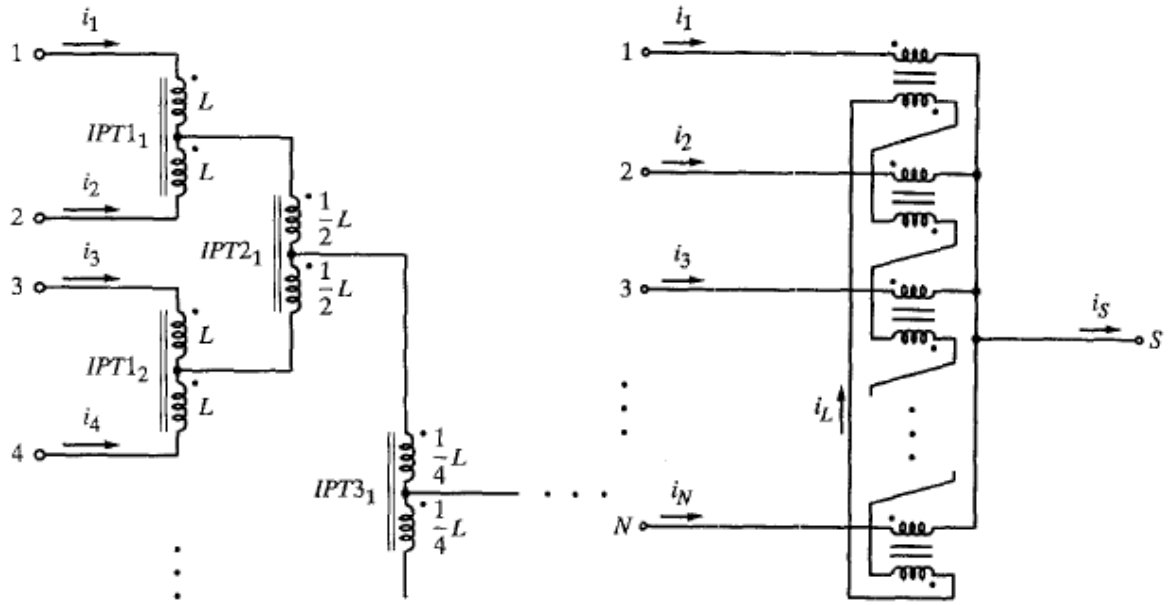


Figure 4-30. Coupled-inductor topology with secondary winding [55].

There are various other coupled-inductor investigations as shown in Fig. 4-31 [62]. They differ from one another in topologies, but could achieve the same performance if proper specifications are satisfied. Again, due to the "fixed" topologies, they struggle with low steady-state efficiency.



(a) Center-tapped coupling inductors (b) Secondary coupled inductors

Figure 4-31. Various topologies on coupled inductors [62].

4.4.2 A New Full Bridge Coupled-inductor Topology

As mentioned above, while coupled-inductor topologies are showing advantages in transient response and are becoming industry practices, they are suffering from low steady-state operating efficiency due to their "fixed" topologies. In steady state operation, it is preferred to reduce the total inductor current ripple with larger phase inductance; during transient operation, a smaller phase inductance is desired to achieve a fast current slew rate. Motivated by the challenging transient and efficiency requirements, this chapter proposes a new full-bridge coupled-inductor (FBCI) scheme which is able to change its topology in different operational environments. For coupled inductors, since the self inductance is usually much larger than the equivalent leakage inductance, the idea is to uncouple the phase inductors in a steady state condition while coupling

all phases together during transient events. Its “flexible” topology thus can improve transient response as well as savor high efficiency.

Fig. 4-32 shows a two-phase example of FBCI. There is an auxiliary coupling phase (Phase #3) connecting all secondary windings of other phases in series. Four switches A, B, C, and D are employed to control the operational modes of the auxiliary phase. By changing the states of the four switches, the auxiliary phase can either couple or decouple the other two phases. Therefore, this topology is flexible compared to prior arts of coupled inductors. In steady state, the auxiliary phase turns off all switches such that the other phases can operate independently in non-coupled status. Without coupling between phases, large phase magnetizing inductance can result in high operating efficiency. When load transitions occur, the auxiliary phase controls turn-on and turn-off of the four switches, such that the other two phases can be coupled when necessary. Since the phase inductors are reversely coupled, the leakage inductance functions as the effective phase inductance. Small leakage inductance lead to high current slew rate which results in a fast transient response. The detailed operational modes will be addressed.

The FBCI can be further extended to a multiphase configuration as shown in Fig. 4-33. In this multiphase configuration, phase N serves as the auxiliary phase. Similar to the two-phase example, four switches are employed to control the operational modes of the auxiliary phase.

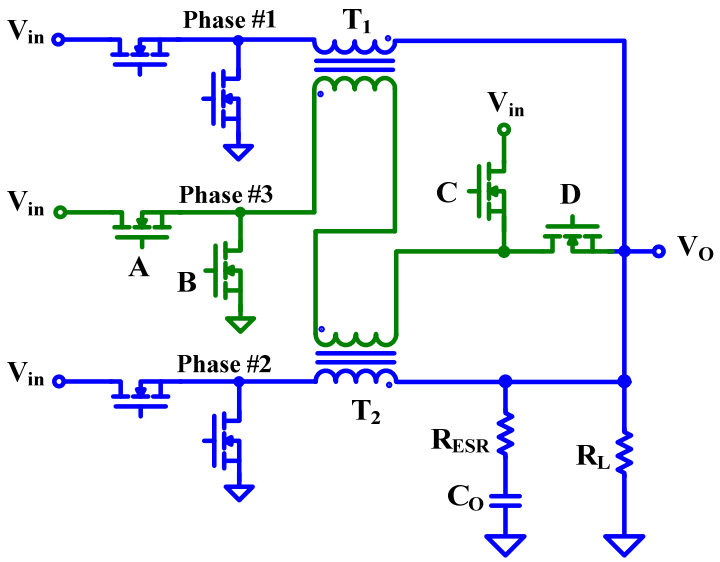


Figure 4-32. Two-phase voltage regulators with an auxiliary coupling phase.

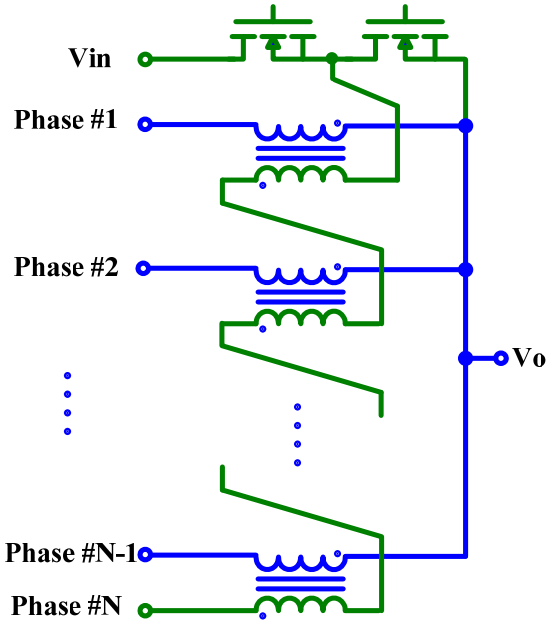


Figure 4-33. Multiphase voltage regulators with an auxiliary coupling phase.

Besides the flexible topology, “flexible” core structures can be implemented to FBCI. For distributed application, the phase inductors can be wound on discrete cores as shown in Fig. 4-34. For applications with all phases centralized, all phase windings can be built on a single core as shown in Fig. 4-35. Therefore, it overcomes the layout drawbacks of the prior arts.

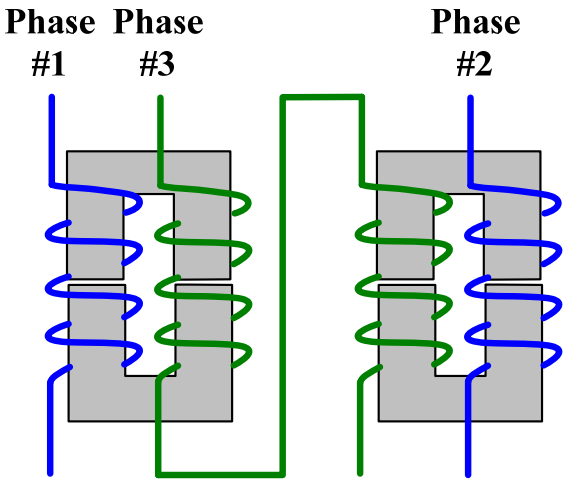


Figure 4-34. Distributed core configuration of FBCI.

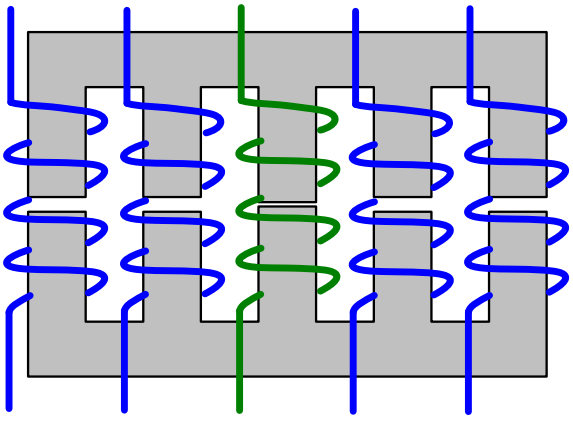


Figure 4-35. Centralized core configuration.

4.4.3 Operational Modes of FBCI

With the proposed FBCI, optimal performance can be achieved by both the flexible topology and the flexible core configurations. The statuses of the four switches of the auxiliary phase determine the operational modes of FBCI. The operational modes will be covered in detail. Simplis simulation will show how these modes work and their features. The simulation parameters are shown in Table 4-3.

Table 4-3. Simulation parameters for FBCI operations.

Input voltage (V)	12
Output voltage (V)	1.4
Switching frequency (kHz)	300
Magnetizing inductance (nH)	200
Leakage inductance (nH)	100
Output capacitance (uF)	880
ESR (mohm)	4

4.4.3.1 Operational Mode 1

The topology of operational mode 1 is shown in Fig. 4-36. For mode 1, switch D is always on and C is off, while switches A and B are controlled by PWM signals. In this mode, the FBCI operates similar to a three-phase coupled-inductor buck converter. All the other phases are coupled through the auxiliary phase all the time.

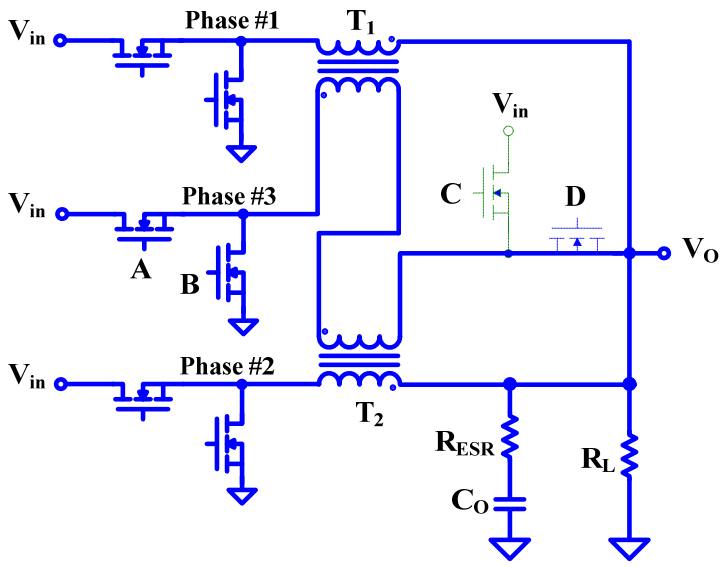


Figure 4-36. Operational mode 1.

The Simplis simulation results are shown in Fig. 4-37. The traces from top to bottom are phase-node voltage, voltage on the phase leakage inductance, current of phase 1, current of phase 2, and total output current, respectively. It is evident from the simulation results that due to the coupling, the total current ripple is high in steady state. Nevertheless, the phase current ripple is reduced. This mode is desired in high-current application where more phases are desired to reduce the average phase current and thermal stresses on each single phase.

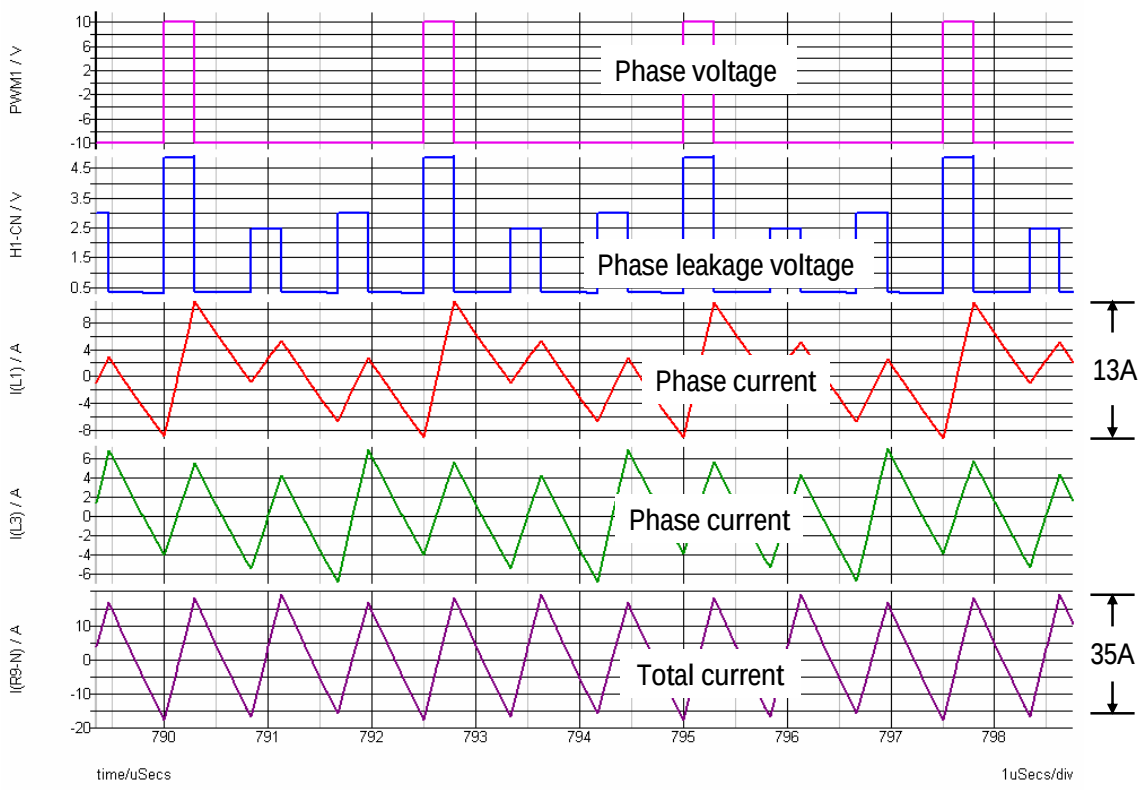


Figure 4-37. Simulation results for operational mode 1.

4.4.3.2 Operational Mode 2

The FBCI runs in operational mode 2 when all four switches are off as shown in Fig. 4-38. Mode 2 is preferred when the VR is operating in light-load conditions. With all the switches off, the other phases are decoupled and FBCI operates as a non-coupled multiphase voltage regulator. In this case, both switching losses and conduction losses are decreased, since dropping the auxiliary phase saves extra energy which will be consumed by this phase otherwise. Moreover, due to increased effective phase inductance, the phase current ripple in phase 1 and phase 2 is small, further reducing the phase conduction losses.

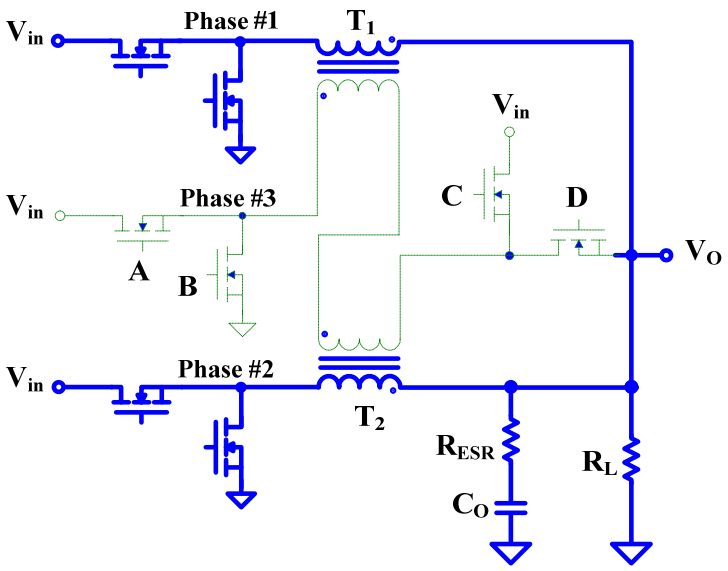


Figure 4-38. Operational mode 2.

The simulation results are shown in Fig. 4-39. The traces from top to bottom are PWM waveforms, currents of phase 1 and phase 2, and total current, respectively. Observed from the simulation, it is found that the total output current ripple is reduced dramatically compared to mode 1. Therefore, light-load efficiency is improved.

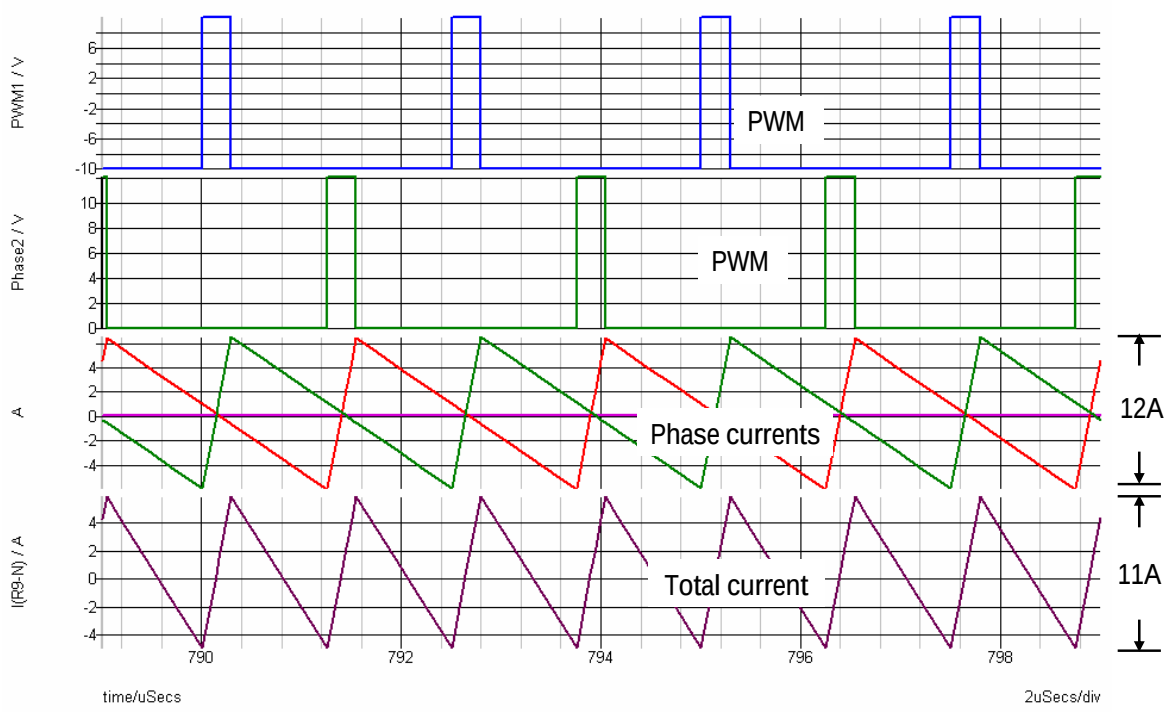


Figure 4-39. Simulation results for operational mode 2.

4.4.3.3 Operational Mode 3:

When a large load-insertion occurs, a high slew-rate current is desired to reduce the output voltage undershoot. In this case, operational mode 3 will kick in to satisfy the load current demands. In this mode, switches B and C are off while A and D are on as shown in Fig. 4-40. The input voltage is applied to the auxiliary phase, and all phases are coupled together through the auxiliary phase. The coupling effect leads to a small effective phase inductance. As a result, the total inductor current will ramp up very fast, with the slew rate determined mainly by the input voltage and the leakage inductance.

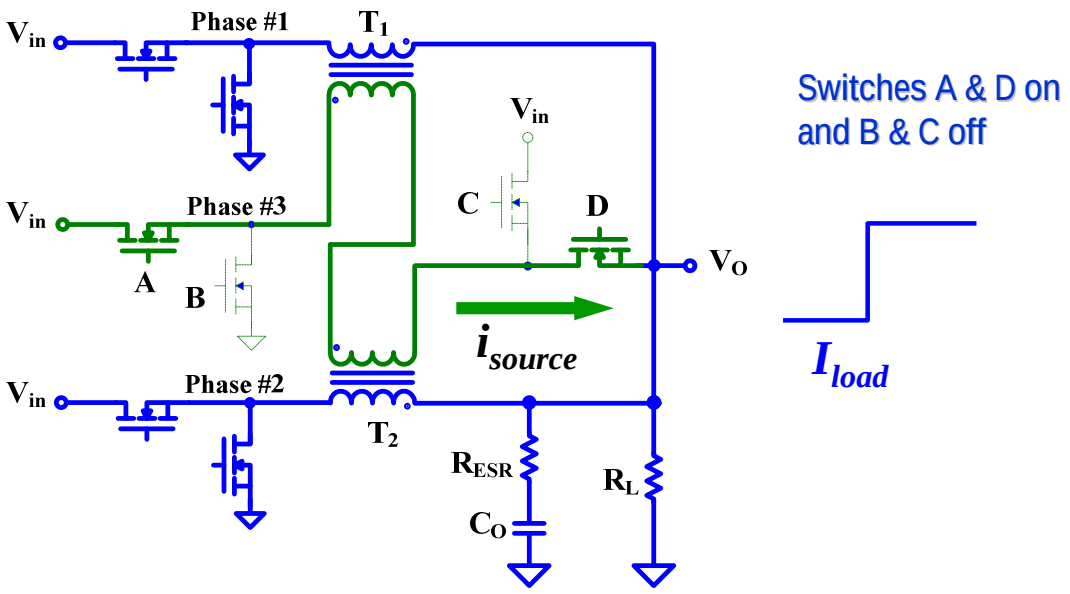


Figure 4-40. Operational mode 3.

Simulation has proven that mode 3 is effective in reducing the undershooting spike during a load application event. Fig. 4-41 shows simulation result comparison for a multi-phase buck converter with and without the proposed FBCI. The red waveform is the output voltage of the VR without the proposed FBCI, while the blue one represents the output voltage of the VR with the FBCI. Without FBCI, due to the inductor delay, VR cannot catch up with the load requirement during transient. The red waveform sees significant voltage undershoot at the edge of the transient. On the contrary, the FBCI couples all the other phases together by turning on switches A and D, resulting in a fast transient response. The voltage undershoot are reduced to a large degree.

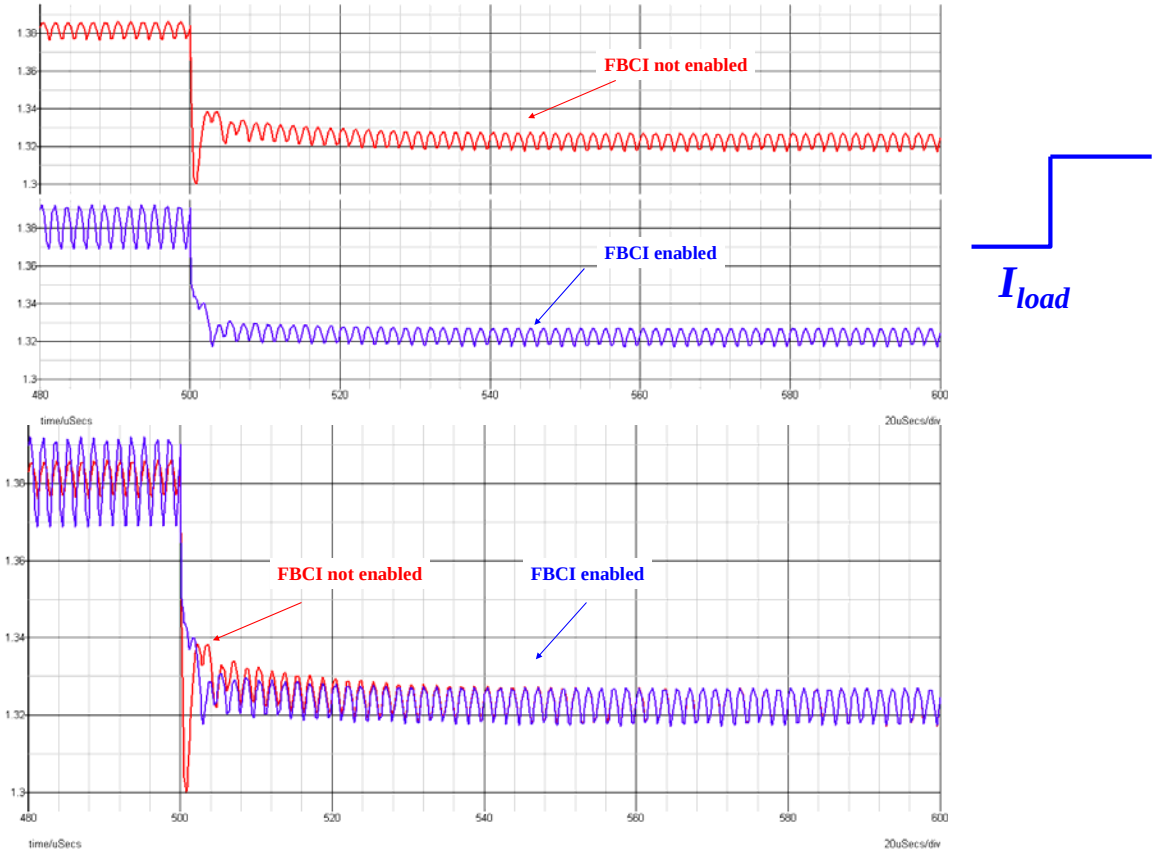


Figure 4-41. Simulation results for operational mode 3.

4.4.3.4 Operational Mode 4

In operational mode 4, switches A and D are always off while B and C are turned on by the control signal upon a load-release transient event. The input voltage is applied to the auxiliary phase in an inverting direction while all phases are coupled together. The output current is sunk very quickly through the coupling, releasing the extra energy stored in the inductors to the input. As a result, the overshooting spike is suppressed during load release events. The equivalent circuit of mode 4 is shown in Fig. 4-42.

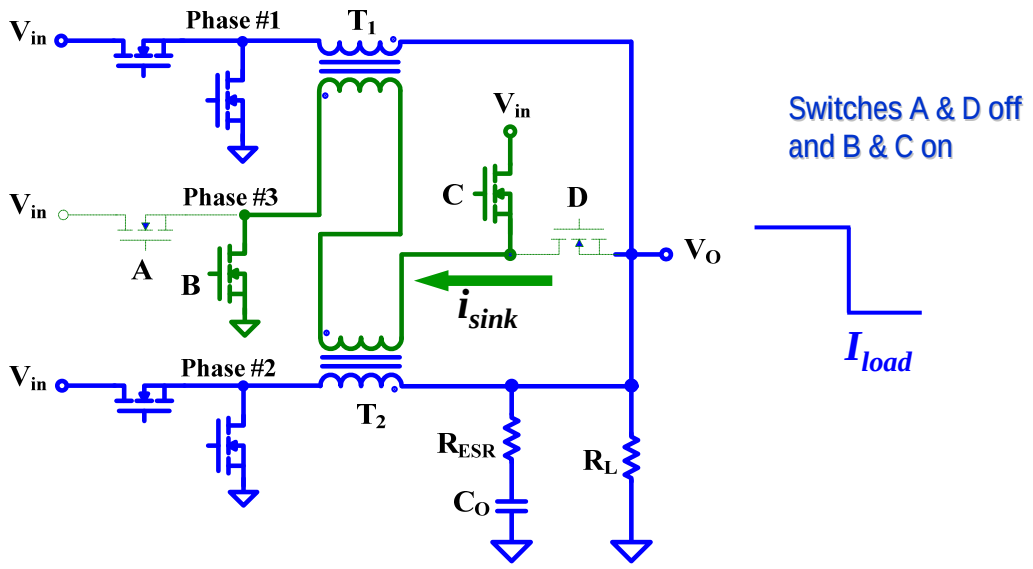


Figure 4-42. Operational mode 4.

The effectiveness of mode 4 is shown in Fig. 4-43 by Simplis simulation. The red waveform is the output voltage of the VR without the proposed topology, while the blue one represents the output voltage of the VR with an auxiliary coupling phase. Without FBCI, the surplus current keeps charging the output capacitors and causes extra voltage overshoots as the red waveform shown in Fig. 4-43. The FBCI couples all the other phases together. The input voltage applied inversely to the auxiliary phase helps sink the current to the input with a high slew rate. Thus, the extra energy is recycled rather than overcharging the output capacitors. And the transient performance has improved.

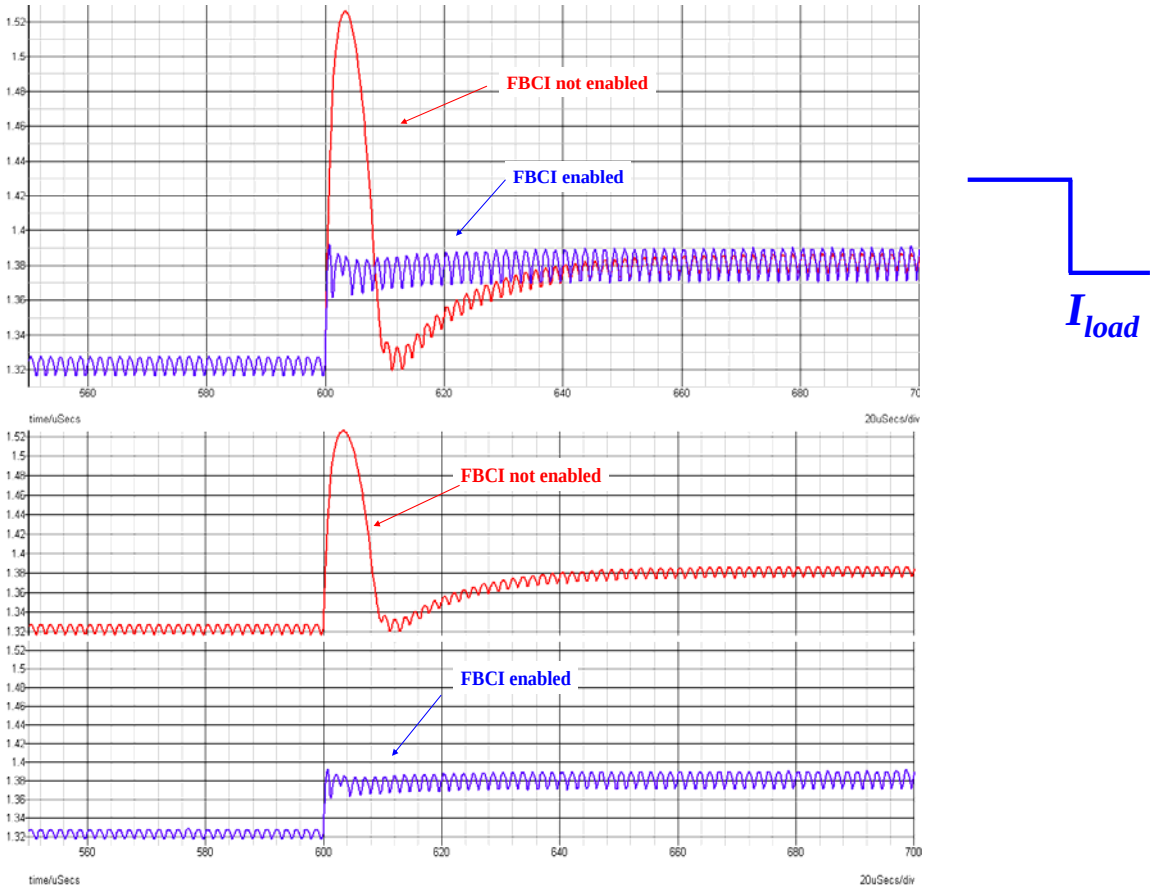


Figure 4-43. Simulation results for operational mode 4.

4.4.3.5 Operational Mode 5

In operational mode 5, switches B and D are always off, and switches A and D are always on as shown in Fig. 4-44. This mode behaves similar to CPES's topology since the auxiliary phase acts as a secondary winding coupling the other phases together. It is desired in a distributed application when all phases have to be dispatched separately. As discussed previously, this topology has circulating current in the secondary winding, which decreases the overall

efficiency. Nevertheless, with the flexibility of FBCI, the circulating current can be released to the load when necessary.

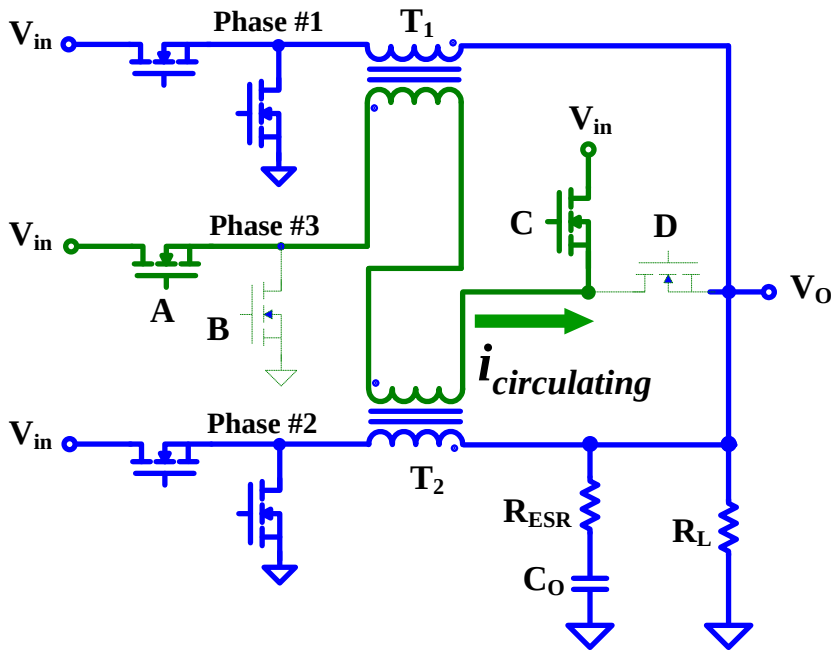


Figure 4-44. Operational mode 5.

Simulation results for mode 5 are shown in Fig. 4-45. Because of the coupling between two phases, the leakage inductance acts as the output filter. The small output filtering inductance leads to high phase ripple current as well as high output ripple current. Compared to operational mode 2, the phase ripple current increases to 16 A while the total current ripple increases to 17A. Nevertheless, this mode shows its advantage in achieving fast transient response and flexible layout.

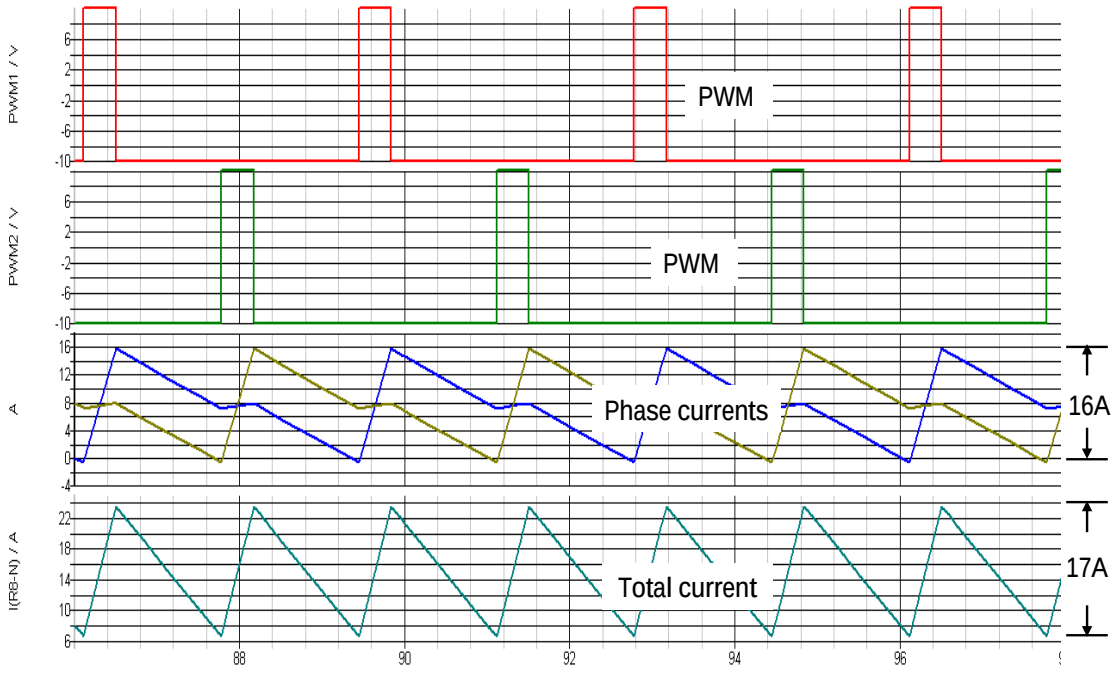


Figure 4-45. Simulation results for operational mode 5.

4.4.3.6 Operational Modes for large Repetitive Transition

During large repetitive transition, FBCI is able to combine several modes together to optimize the transient performance. The operational modes for large repetitive transition is illustrated in Fig. 4-46. Supposing a load-release transition occurs first, mode 4 comes into work with switches B, C on, and A, D off. The extra current stored in output inductors is dumped with a high slew-rate caused by the coupling of the other phases, resulting in reduced voltage overshoot. Following the operational mode 4, switches A and C are on, and B and D are off, i.e. mode 5 is active, in a way that keeps the magnetizing current circulating in the auxiliary phase. As the load application event comes, the circulating current can be released to the load by turning on switches A and D, as the operation of mode 3. The high slew-rate current is sourced to the output

very quickly, preventing the output voltage from undershooting. By properly controlling the operational modes, the FBCI can optimize the transient response.

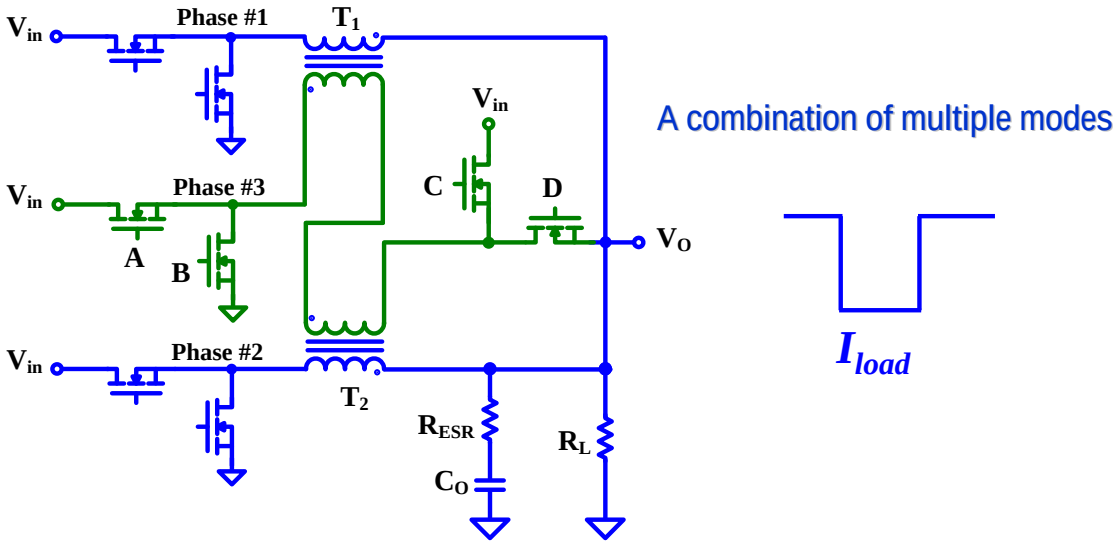


Figure 4-46. Operational modes for large repetitive load transition.

Detailed performance comparison can be seen in Fig. 4-47 by simulation. The red waveform is the output voltage of the VR without the proposed topology, while the blue one represents the output voltage of the VR with an auxiliary coupling phase. It is found that the FBCI is capable of both sourcing and sinking currents with a fairly high slew rate. Both undershoot and overshoot of the output voltage are reduced during large repetitive load transient events, compared with topologies without FBCI. Therefore, it shows advantages over most other topologies in terms of transient performance.

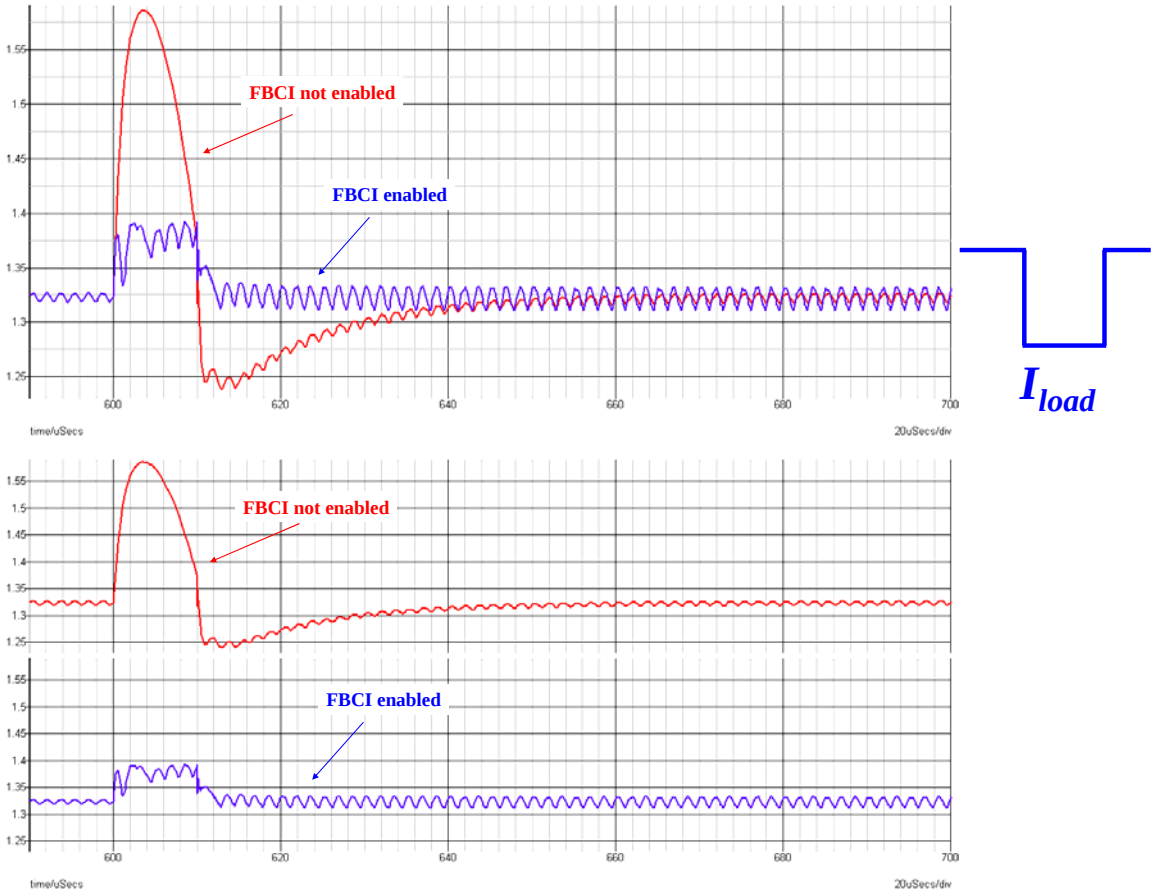


Figure 4-47. Simulation results for large repetitive load transient.

4.4.4 Summary

Coupled inductors are attracting more and more attention from voltage regulator designers. Although they show advantages on transient response improvement, they are potentially suffering from low steady-state operating efficiency. The proposed full-bridge coupled-inductor topology provides a promising solution to this common problem. Simulation results show that the FBCI improves transient response as well as increase steady-state efficiency.

CHAPTER 5 A NEW MAGNETICS DESIGN METHODOLOGY

Motivated by ever increasing demand for multi-phase buck converters with coupled inductors, a new magnetics design is presented based on FEM simulation. This chapter will limit the discussion to planar power inductor design for simplicity purposes. This method can, however, be extended to other non-planar discrete and coupled inductors.

5.1 Review of Magnetics Design

The increasing demand of smaller-size and cost-effective DC/DC converters has expected design engineers to develop power converters capable of operating at higher switching frequencies with high efficiency. However, even with modern advanced topologies, magnetics is still one of the biggest challenges for achieving higher power density and higher efficiency due to the significant portion of magnetics in the whole power system [63].

In recent years, there have been two distinct trends in magnetics design in power electronics systems. The first trend concerns the use of planar structures [63-68], with which much closer board spacing and lower profile can be achieved. Easier manufacturability due to simpler conductor assembly methods makes planar structures the prevailing method in the power converter industry. The second trend is to move continuously toward higher frequencies in order to reduce the size of magnetic components [63-78]. However, the design of transformers and inductors is usually a limiting technology for higher frequencies.

Since magnetic components usually occupy a large portion of size in a power converter, an optimal design of transformers and inductors thus becomes critical to miniaturize the system profile and further increase its power density. For conventional approaches, magnetic components are often designed based on magnetic-circuit models. Core loss and conduction loss in magnetic devices are roughly estimated. However, with the increase of switching frequency driven by continuously lower profile and higher power density, traditional analysis makes it very difficult to evaluate the loss due to skin effect and proximity effect. Therefore an innovative methodology based on numerical analysis of electromagnetic fields is desired.

So far there is little research work done in modeling magnetics in a wider frequency range for power converters based on the analysis of electromagnetic fields. As one of the most popular tools for electromagnetic design in industry, Ansoft Maxwell Field Simulators (Maxwell 2D and 3D) have shown their powerful capability of electromagnetic computations with excellent accuracy and ease of use, which stimulates their prevalence in magnetics design.

In this chapter, design issues of planar magnetics, including loss mechanism in copper and core, winding design on PCB, core selections, winding arrangements and so on will be reviewed first. Afterwards, FEM simulators are introduced to numerically compute the core loss and winding loss. Consequently, a software platform for magnetics design is established, and optimized magnetics can then be achieved.

5.2 Loss Mechanism in Magnetics Design

The total power loss in magnetic devices usually consists of core loss in magnetic materials and copper loss in windings. The core loss has two portions, which are hysteresis loss and eddy current loss while the copper loss is often explained by DC or AC power loss dissipated in the windings in the form of heat.

5.2.1 Core Losses

Consider an *n*-turn inductor excited by periodic waveforms *v(t)* and *i(t)* having frequency *f*, the net energy that flows into the inductor over one cycle is [44]

$$\begin{aligned} W &= \int_{onecycle} v(t)i(t)dt \\ &= \int_{onecycle} \left(nA_C \frac{dB(t)}{dt} \right) \left(\frac{H(t) \cdot l_m}{n} \right) dt \\ &= \left(A_C l_m \right) \int_{onecycle} HdB \end{aligned} \tag{5-1}$$

and the hysteresis loss is

$$P_H = (f)(A_C l_m) \int_{onecycle} HdB \tag{5-2}$$

On the other hand, ferrites, as widely used magnetic core materials in power electronics systems, usually are good electrical conductors. Consequently ac magnetic fields can cause electrical eddy currents to flow within the core material itself, as shown in Fig. 5-1. Eddy current losses contribute significantly in the total core losses at high frequencies.

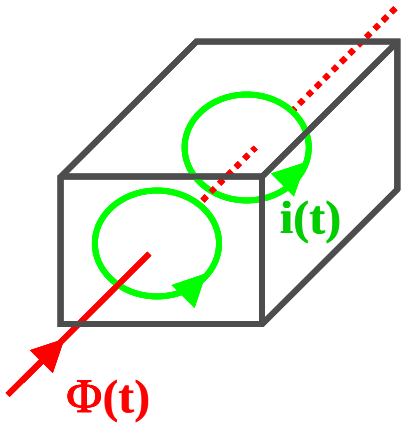


Figure 5-1. Eddy currents in a magnetic core.

At a given frequency *f,* the core loss P_{core} can be approximately expressed by an empirical function of the form [69]

$$P_{core} = K_{fe}(\Delta B)^{\beta} A_C l_m = P_V V_e \tag{5-3}$$

where P_v is obtained from Philips software and V_e is specified by vendors. The AC flux density ΔB of the inductor is given by

$$\Delta B = \frac{V_0 \cdot (1 - D)}{2 \cdot N \cdot A_e \cdot f} \tag{5-4}$$

where A_e is the core cross-sectional area, N is the inductor turns number, f is the switching frequency, Vo is the output voltage, and D is the duty cycle. To accurately evaluate the core loss resulting from hysteresis loss and eddy-current loss in magnetic cores, Philips has developed software that can give core loss density P_V at different temperatures for arbitrary flux waveforms of inputs. Fig. 5-2 contains core loss data samples for Ferroxcube 3C96 ferrite material.

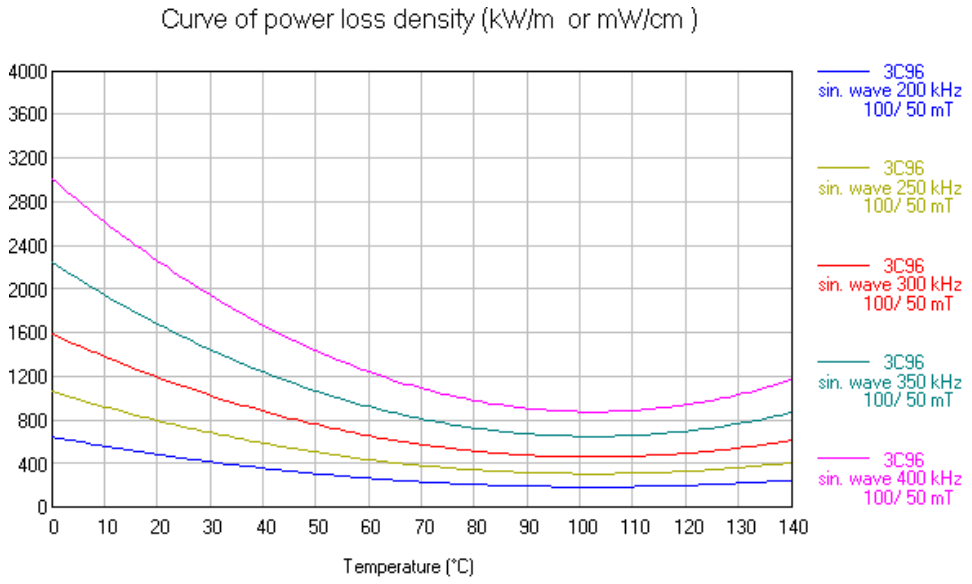


Figure 5-2. Core loss data samples for 3C96 ferrite material.

It is obvious that core loss is proportional to core size and increases as frequency goes higher. However, the relationship between core loss and temperature is not uni-directional. As shown in Fig. 5-2**,** there exists a minimum core loss point at a specific temperature.

5.2.2 Copper Losses

The DC or low-frequency copper loss in the windings can be estimated by

$$P_{Cu} = I_{rms}^2 R_{DC} \tag{5-5}$$

where I_{rms} is the RMS value of the current flowing through the windings, and the dc resistance can be expressed as

$$R_{DC} = \rho \frac{l_b}{A_W} \tag{5-6}$$

where A_W is the copper trace cross-sectional area, l_b is the length of the trace, and ρ is the resistivity of copper.

Therefore, to obtain the DC resistance of the copper, we need to determine the dimensions of the PCB trace. The number of turns per layer and the spacing between the turns are denoted by the symbols N_L and S respectively as shown in Fig. 5-3.

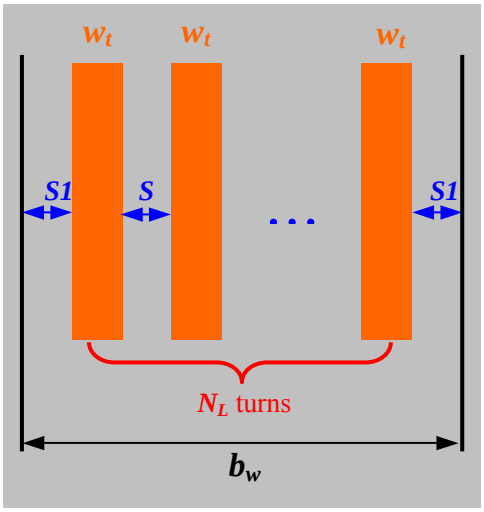


Figure 5-3. Trace width W_t, spacing S and core space b_W.

For an available core window width b_W, the trace width W_t can be calculated from [65]:

$$w_t = \frac{b_w - (N_L - 1) \cdot S - 2 \times S_1}{N_L} \tag{5-7}$$

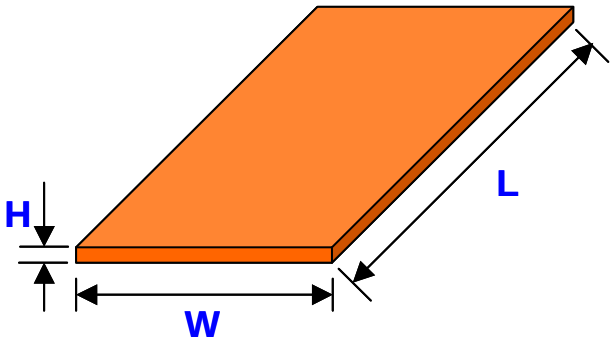
where S_1 and S are specified by the safety rules and fabrication tolerance of industry practice. Usually the copper thickness H_c is also specified upon prototype layout. After the trace width is obtained, the trace cross-sectional area can be given by

$$A_w = W_t \cdot H_c \tag{5-8}$$

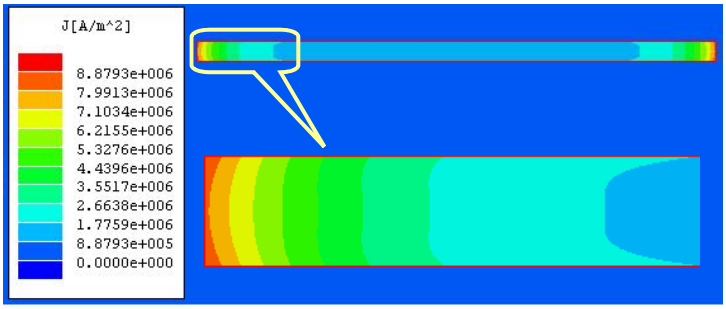
Hence, the DC resistance is determined.

At high frequencies, eddy currents in the windings due to skin effect and proximity effect also cause power losses, and may lead to copper loss even in excess of DC or low-frequency loss expressed above [71-78].

One way to reduce the high-frequency loss due to skin effect is to decrease the thickness of conductor to the order of one skin depth such that the ac current can be assumed to be uniformly distributed in the cross-sectional area of the winding. For a planar magnetic structure, since the thickness of the conductor is usually comparable to one skin depth, the skin effect can be suppressed. For example, the thickness of 4-oz PCB is about 140 μm while the penetration depth (or skin depth) for the copper at 400 kHz is about 104 μm. From a circuit point of view, it is usually reasonable to ignore the skin effect when the thickness of copper is less than twice of the skin depth. For most of planar copper structures, however, the currents are distributed dominantly in the two ends rather than on the surface evenly. Fig. 5-4 illustrates an example of skin effect from electromagnetic simulation.



(a)



(b)

Figure 5-4. Skin effect in a 4-oz PCB copper trace (H=140 um, W/H=25): (a) Copper configuration, and (b) current distribution.

On the other hand, proximity effect also contributes much to the total high-frequency loss as shown in Figs. 5-5 and 5-6. From Figs. 5-5 to 5-6, it is obvious that the distribution of ac currents is no longer uniform in the planar windings. Therefore the accurate ac resistances can be computed only from EM simulation (like FEA). Table 5-1 lists the ratio of ac resistance to dc resistance for each case above at frequency of 400 kHz.

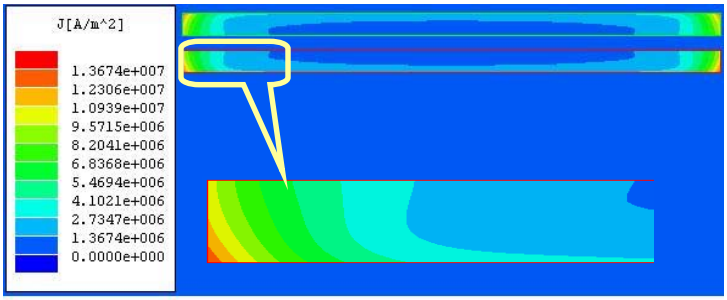


Figure 5-5. Proximity effect (two layers in parallel).

Figure 5-6. Proximity effect (three layers in parallel).

Table 5-1. AC resistances due to skin effect and proximity effect.

	Rac/Rdc
One single copper layer	1.59
Two layers	2.24
Three layers	2.22

One way to reduce the copper losses due to the proximity effect is to interleave the windings (for transformer design). Figs. 5-7 and 5-8 explain how to improve current distribution and therefore reduce total ac loss by interleaving primary and secondary windings in power transformers.

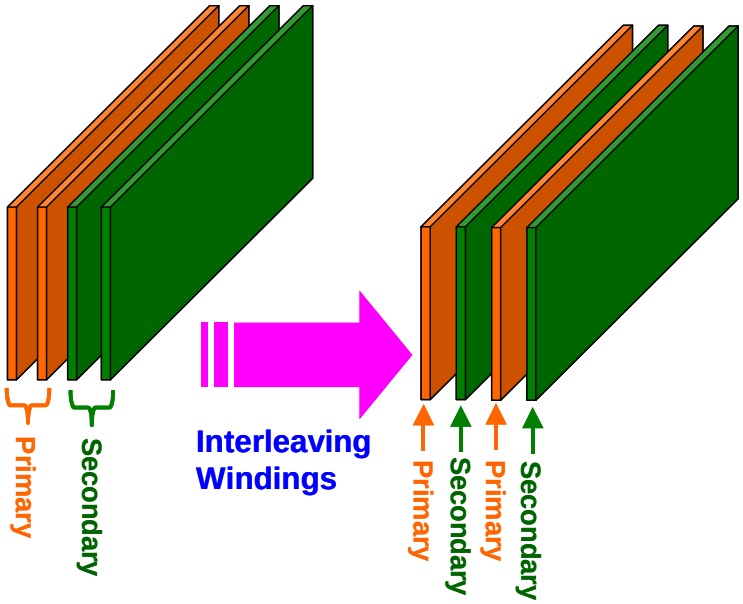


Figure 5-7. Interleaved windings.

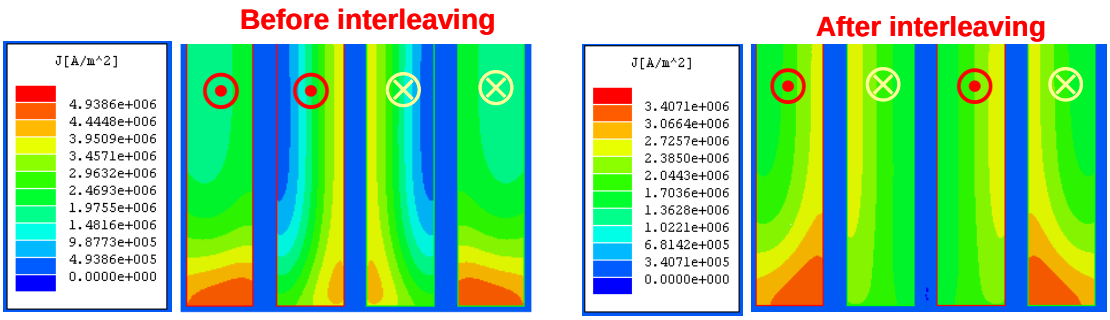


Figure 5-8. Current distributions before and after interleaving.

Apparently the current is distributed more uniformly after interleaving the primary and secondary windings. As a result, the ac loss can be reduced.

5.3 Design of Planar Power Inductors

Power inductors play an increasing important role in CPU core regulation. The design methodologies usually fall in two categories. The first category is inductors where the ripple current is a small percentage of the average dc current component (say, less than 5% on an RMS basis). The other category is where the ripple current is large relative to the dc component (say, greater than 20%) [72-78]. Of course, many applications are somewhere in between and tradeoffs are required.

In the case of small ripple, we can assume that the current is a dc current and that skin effect and core losses can be ignored. The design of the planar inductor then reduces to choosing the lowest resistance winding possible based on the constraints of the core size and gap. Minimizing the number of turns on the inductor is the first step towards achieving a low winding resistance. The next and, probably, more difficult challenge is to maximize the copper utilization of the core window.

For inductors where the ac ripple content is high, the design of the winding has issues very similar to that of transformer winding design with one more difficulty. There is usually no secondary winding that can be used to reduce proximity effects through interleaving.

With regard to core design, there is now a significant ac flux component causing core losses and potentially contributing to eddy-current losses if the gap and the winding are in close-proximity. This is not an unreasonable assumption in planar devices as two of the primary goals are small

size and high power density. In these cases, a lumped gap may result in unacceptably high losses in the winding and alternative-gapping strategies (e.g. distributed gaps) may merit consideration.

As an example, we will design planar inductors using 8-layer PCB for a half-bridge converter with low profile of 0.22 inch, output power of 60 W as shown in Fig. 5-9. The specifications are given in Table 5-2.

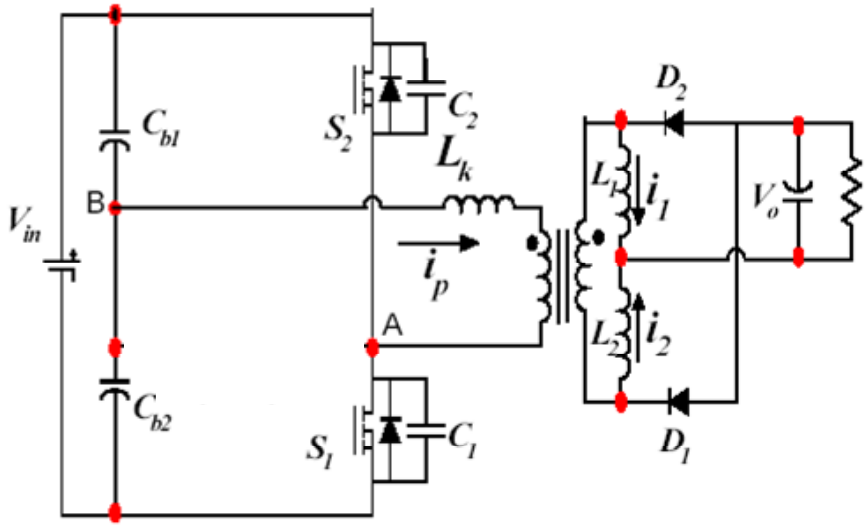


Figure 5-9. Half-bridge converter topology.

Table 5-2. Specifications of the inductors.

Input voltage (V)	36~75
Output voltage (V)	1.2
Output power (W)	60
Switching frequency (kHz)	400
Inductor height (inch)	0.22
Inductor current (A)	25+ripple
PCB layers	8
Copper thickness (mm)	0.14
Insulation thickness (mm)	0.11

The design platform can be described as shown in Fig. 5-10. The core materials and core shapes are first selected. Maxwell 3D FEM simulator is used to calculate the core losses. For copper loss calculation, converter-dependent excitations are used as inputs. After determining the window partition, Maxwell simulators are introduced to obtain the winding layouts, as well as copper loss. Consequently, total design goal is achieved.

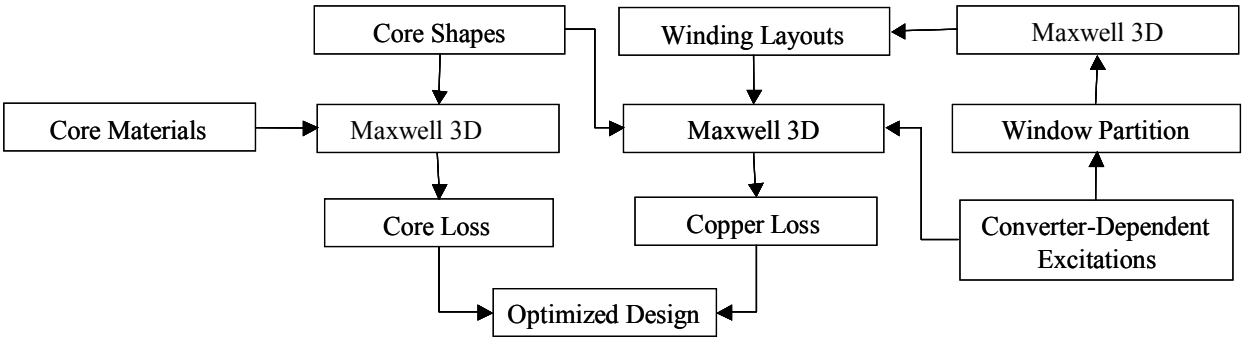
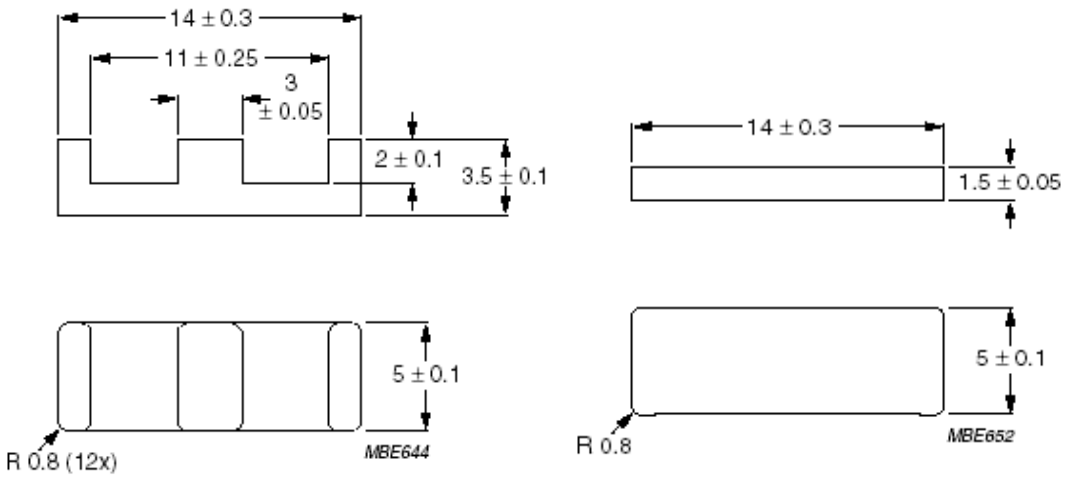


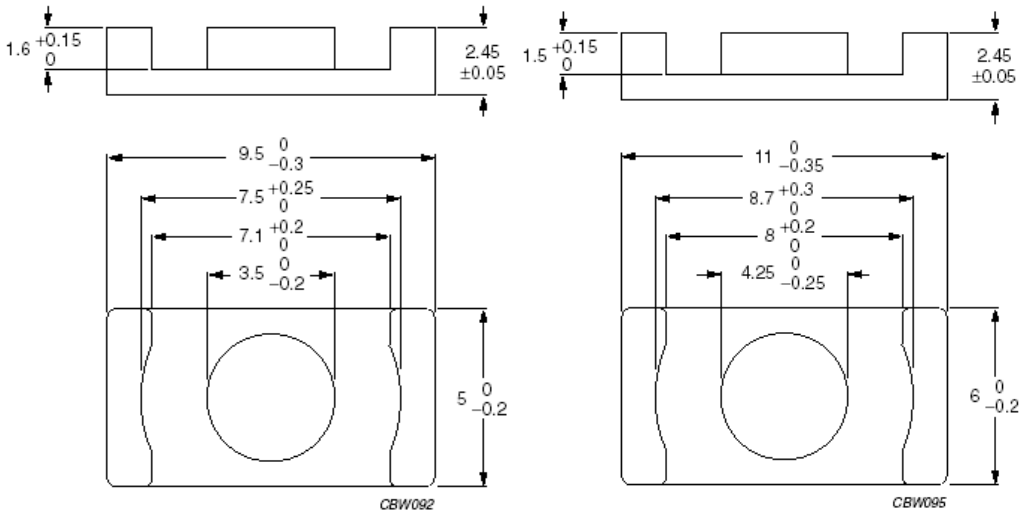
Figure 5-10. Power inductor design platform.

5.3.1 Selections of Core Shape and Material

Since the profile of the magnetics is strictly required to be no more than 0.22 inch, we first look into commercially available planar ferrite cores satisfying such low profile requirement. Three core combinations with less than 0.22 inch profile, as shown in Figs. 5-11(a) through (d), can be options for the transformer. Although a little bit higher than 0.22" in height, EQ13 can handle larger energy than above cores because of its bigger cross-sectional area. Therefore it is still a candidate core for the inductors. Since the height requirement is mandatory, custom work must be done on EQ13 to satisfy the 0.2" profile. Fig. 5-12 shows the core parameters of EQ13.

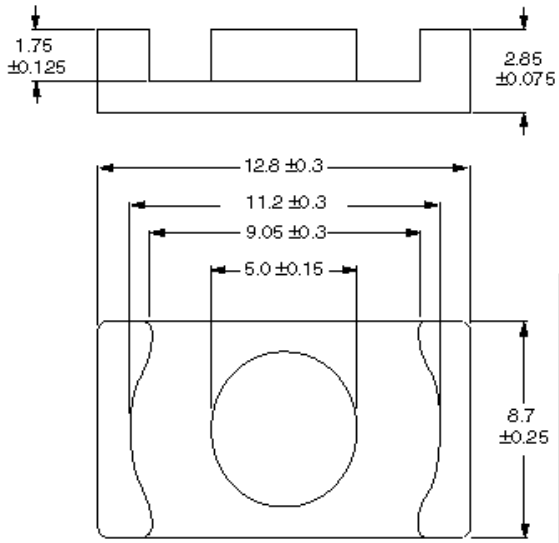


(a) (b)



(c) (d)

Figure 5-11. Core shapes: (a) E14/3.5/5, (b) PLT14/5/1.5, (c) ER9.5, and (d) ER11.



SYMBOL	PARAMETER	VALUE	UNIT
Σ(l/A)	core factor (C1)	0.911	mm^{-1}
V_e	effective volume	348	mm^3
l_e	effective length	17.5	mm
A_e	effective area	19.9	mm^2
A_{min}	minimum area	19.2	mm^2
m	mass of core set	≈ 0.9	g

Figure 5-12. EQ13 parameters.

Comparisons for the candidate cores are presented in Table 5-3.

Table 5-3. Core shape specifications.

	ER95	ER11	E14	EQ13
Height (mm)	5	4.9	4.9	N/A
Ae (mm2)	8.47	11.9	14.5	19.9
Footprint (mm2)	47.5	66	70	111.36

A half-bridge topology has two inductors which are combined to serve as a current doubler to achieve the required 50 A output current, therefore average current for a single inductor is as high as 25 A. To prevent saturation, it is critical to select core materials that have high saturation flux densities. Nevertheless, air-gaps are needed for inductors to prevent saturation. The air-gap length is given by

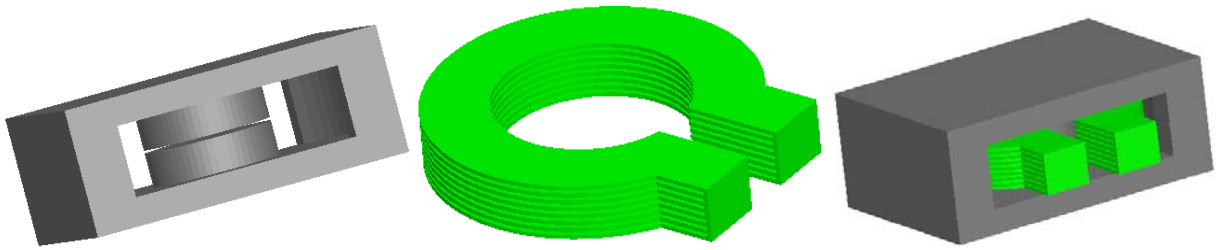
$$l_g = \frac{\mu_0 \cdot A_c \cdot N^2}{L} \tag{5-9}$$

where A_c is the cross-sectional area of the core, N is the turn number of the winding, and L represents the inductance value.

Carefully investigating main core material vendors, we choose 3F35 and 3F3 as our desired core materials. Although 3F35 has relatively smaller loss density, it is not suitable for operation at frequencies lower than 400 kHz. Therefore, 3F3 is employed for our preliminary design at frequencies below 400 kHz. Just like the transformer, there are four core shapes ER95, ER11, E14, and EQ13 available that meet the height requirement. The specifications for these cores are given in previous sections.

5.3.2 FEM Simulation and Loss Evaluation

In order to accurately determine the core loss and high-frequency conduction losses in inductor windings, both core loss and copper loss will be evaluated by Ansoft EM simulation tools, such that optimal inductor design can be obtained. Based on the equation for the air-gap length, the airgap can be determined if the phase inductance, turns number, and core geometry are given. Maxwell 3D models are built based on the selected candidate core shapes as shown in Fig. 5-13. The phase inductance is specified by the converter specifications. One turn is assumed for layout purpose.



(a) (b) (c)

Figure 5-13. 3-D models of the inductor. (a) Core; (b) winding; and (c) overall structure.

The simulated core losses with different core shapes are shown in Fig. 5-14 (The curve drops are due to different materials we adopted for frequencies below and above 400 kHz). The curves suggest that core loss increases with frequency, core size, and flux density increasing.

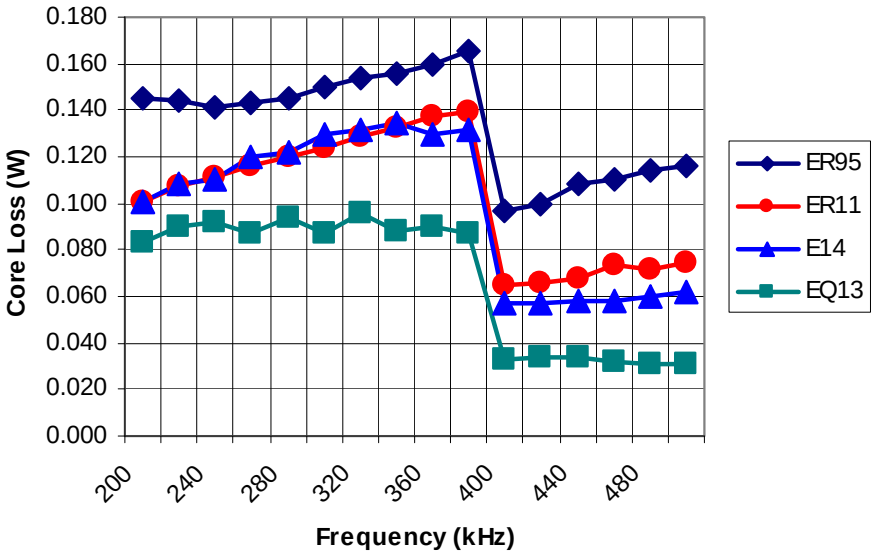


Figure 5-14. Effects of core materials, shapes, and frequency on inductor core loss.

Usually, magnetic component design involves a compromise between the reduction of losses and the expense of increased footprint or vice versa. EQ13 has the smallest core loss but the largest footprint among the candidate cores (see Table 5-3). Therefore, a tradeoff always exists in the core selection. Due to layout constraints, E14 and ER95 will not be evaluated for copper losses.

To evaluate the overall copper losses, we choose an ER11 and an EQ13 ferrite structures with air-gaps. Maxwell 3D models are built just as shown in Fig. 5-13. The simulated losses are shown in Fig. 5-15.

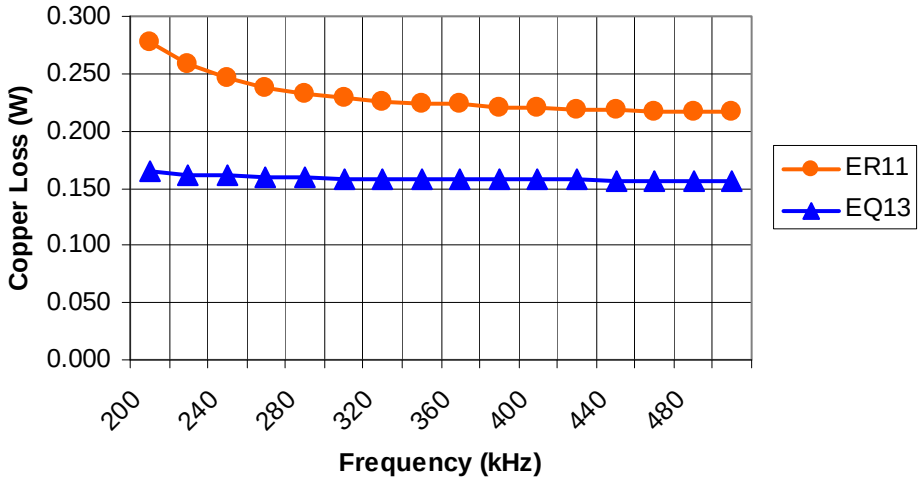


Figure 5-15. Copper losses for ER11 and EQ13.

According to Fig. 5-15, change of frequency leads to a little change of copper loss. This can be explained from circuit and magnetic points of view. Generally, as frequency increases, the output current ripple is reduced if the phase inductance value is given. As a result, the RMS value of the output current is reduced, which causes the decrease of the copper loss. However, the increase of the frequency causes extra ac losses due to skin effect and proximity effect. Consequently, two tendencies compromise to contribute to the total copper loss of the inductor. Combined with the core losses shown in Fig. 5-14, the total losses for ER11 and EQ13 are illustrated in Fig. 5-16:

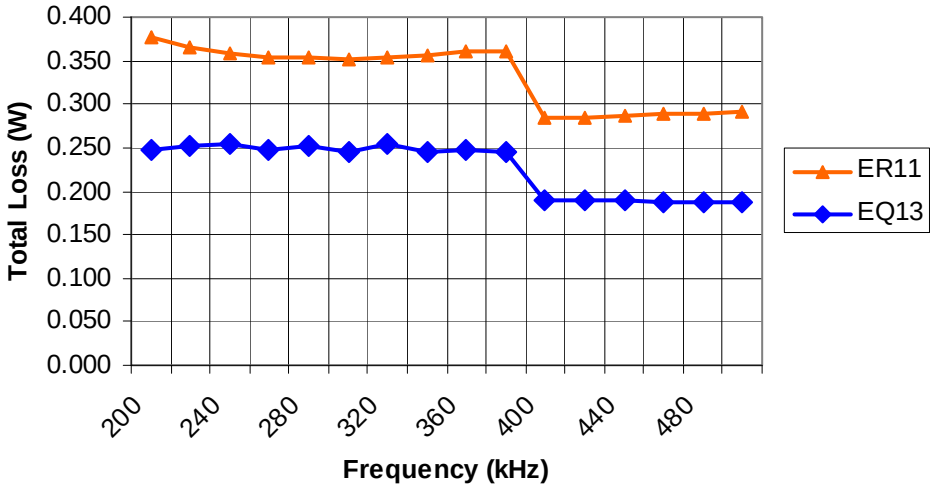


Figure 5-16. Total losses for ER11 and EQ13.

Fig. 5-16 suggests that frequency change doesn't affect total loss significantly for a given core shape with a specific material. And within a range of frequencies, the larger the core is, the smaller the total loss will be. Also due to different loss density of 3F3 and 3F35, significant curve drops can be found around frequency of 400 kHz.

The inductor design will not be complete without a look into the effect of input voltage on the power losses. We first look at the equation for the duty cycle

$$D(V_{in}) = \frac{2 \cdot V_o \cdot N_p}{N_s \cdot V_{in}} \tag{5-10}$$

from which we found that the duty cycle $D(V_{in})$ decreases with the increase of input voltage. Therefore, the current ripple

$$\Delta I = \frac{Vo \cdot (1 - D(V_{in}))}{2 \cdot L \cdot f} \tag{5-11}$$

will increase as the input voltage increases for a given switching frequency. However, the ripple is so small that a significant change of RMS current value is not expected according to equation (41), which leads to negligible change of copper losses. The simulated copper losses are shown in Fig. 5-17.

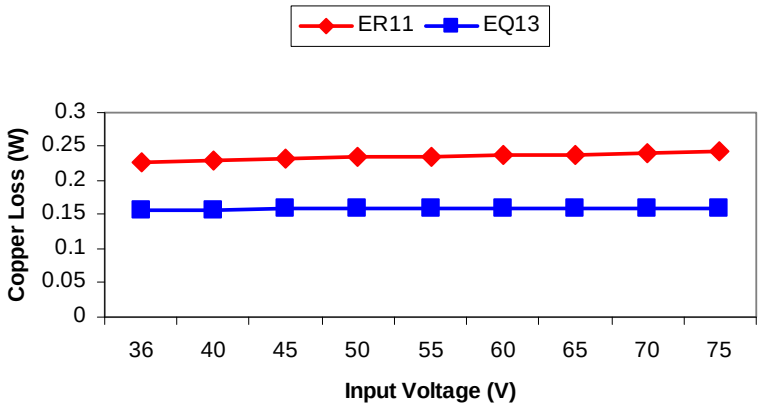


Figure 5-17. Copper loss vs input voltage.

Let's also investigate the effect of input voltage on the core losses. According to Equation 5-4, an increase of the input voltage results in increased AC flux density, which leads to the increment of core loss as shown in Fig. 5-18. The input voltage is set to be from 36 V to 75 V.

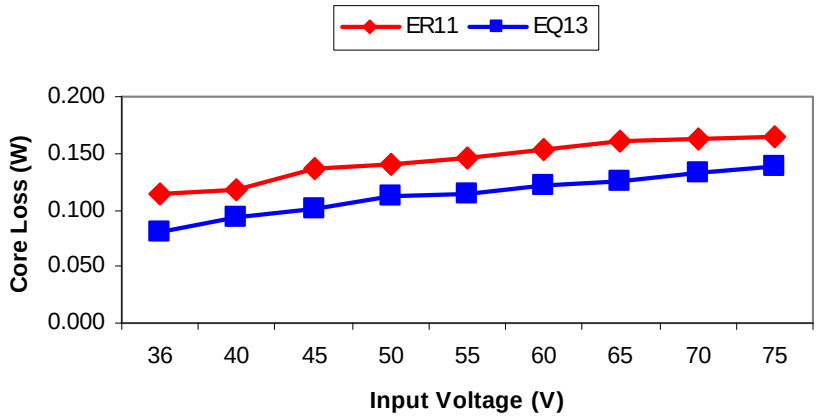


Figure 5-18. Core loss vs input voltage.

The overall power losses are obtained as shown in Fig. 5-19. Notice that the inductor has the smallest loss at the 36V input voltage, and the total loss increase as the voltage goes higher.

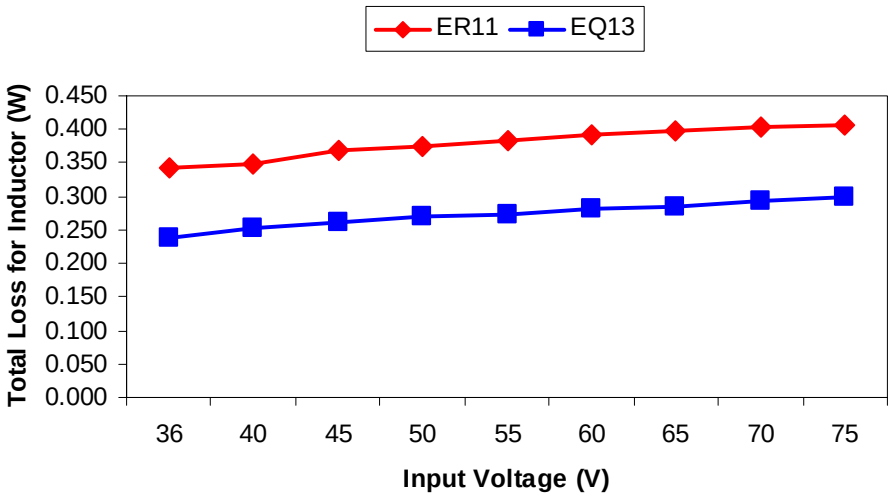


Figure 5-19. Total loss for the inductor at different input voltages.

Carefully budgeting layout and power loss by evaluation of the total topology, we decided the core shape for the inductors to be ER11. The core material is 3F35. Then the preliminary design results of the inductors on 8-layer PCB can be finalized.

5.4 Summary

A novel design methodology of planar magnetics based on numerical analysis of electromagnetic fields is proposed and successfully applied to the design of low-voltage high power density dc-dc converters. The design methodology features intense use of FEM simulation. As a powerful simulation software for electromagnetic analysis, Maxwell 2D delivers virtual prototypes of magnetics quickly and accurately. Maxwell 3D can simulate frequency and time domain electromagnetic fields in complex 3D structures with unsurpassed accuracy and ease of use. It is therefore employed throughout the design for magnetics in this thesis.

Effects of input voltage, core shape, and frequency on magnetics are investigated. While the inductor copper loss is reluctant to change with the input voltage at a given frequency, the worst case for the total losses of the inductors is at the highest input voltage. In terms of core shape, it is found that larger cores have smaller losses for inductors. In a given frequency range, losses for the transformer and inductor are reduced with the increase of the frequency. Through the study, it is demonstrated that ac losses play important roles in magnetics design at high frequencies.

CHAPTER 6 AN ACTIVE COMPENSATOR FOR DYNAMIC VOLTAGE SCALING

6.1 Introduction

The ever-stringent transient and efficiency requirements of recent microprocessors have posed great challenges on voltage regulator (VR) design. As the microprocessor clock frequency becomes faster and faster, the power consumption and thermal dissipation soar dramatically and have an adverse impact on system performance. Provided that the power dissipation is proportional to the square of the supply voltage, the efficiency can be improved significantly by dynamically varying the supply voltage without affecting perceived performance. This dynamic voltage scaling (DVS) technology has been well investigated in [79-89] which date back to years ago. Also referred to as dynamic voltage identification (VID) in [2], it has been widely implemented in microprocessor (CPU) voltage regulation to achieve a higher efficiency. With the dynamic VID technology, a microprocessor is able to dynamically determine an optimal operating voltage based on its load condition and send VID command to the voltage regulator. Upon receiving the VID command, the voltage regulator will then position its reference voltage to targeted operating voltage.

It is desired for a voltage regulator to respond to VID command immediately and settle its output voltage to a new level with minimum delay to expedite power reduction and processor cooling [91-94]. For example, in Intel's specifications [2], the VR must regulate the maximum output voltage to recover within the specified voltage VID window within 50 microseconds of the final

VID command, and react on a low VID to high VID transition by adjusting the output voltage to the range defined by the new VID command within 50 microseconds. However, output capacitors of a voltage regulator will try to hold the output voltage from transitioning, since any output voltage change will result in charging or discharging of the output capacitors. Due to the fact that the output inductor current can only ramp up at a fixed slew rate, it takes a certain amount of time for a regulator to supply the load current as well as the charging/discharging current, resulting in DVS transition delay. A large number of bulk capacitors then become a heavy burden for a fast DVS operation. The resulted time delay can cause output voltage deviate from the reference voltage, or even out of Intel VR design specifications [2]. While reducing output capacitors can speed up DVS transition, it is vital to maintain enough output capacitance to meet both static ripple voltage and transient response requirements. Investigation in this dissertation discovers that the compensation network of the voltage regulator also has a big impact on DVS operation. Thus, an alternative way to improve DVS operation could be achieved by modifying the compensation network.

In this dissertation, the operational principles of DVS and impacts of the output capacitors on DVS are addressed first. Then an active compensator scheme is proposed to improve the DVS performance. Simulation data and experimental results are demonstrated to verify the proposed scheme.

6.2 Effects of Output Filters and Compensation on Dynamic Voltage Scaling

A simple block diagram of a voltage regulator with voltage-mode control in Fig. 6-1 is employed to demonstrate the operation of DVS. There is a VID interface between the CPU and the pulse-wide-modulation (PWM) controller. A digital-analog converter (DAC) integrated in the controller decodes the logic signals into a discrete analog voltage which is the reference voltage VREF. As receiving VIDs from CPU, the reference voltage is adjusted and the output voltage V_O will be regulated to the desired VID voltage. As mentioned in the first section, output capacitors have big impact on DVS operation. When the VID is transitioned from high to low, output capacitors need to discharge current to the load. If the load demand of the processor is less than the output capacitor discharging current, reverse current may flow into the regulator's input filter, potentially charging the input filter to a voltage above the over voltage value. In another case when the VID increases from low to high, the voltage regulator will charge output capacitors to increase the output voltage. The VR may experience a large inrush current due to charging of output capacitors. Therefore, the reference voltage of VR usually ramps up or decreases to the targeted VID at a specified slew rate such that the output voltage will alter smoothly. For example, according to the specifications in [2], the microprocessor transitions to its desired operating voltage in a 12.5mV step every five microseconds.

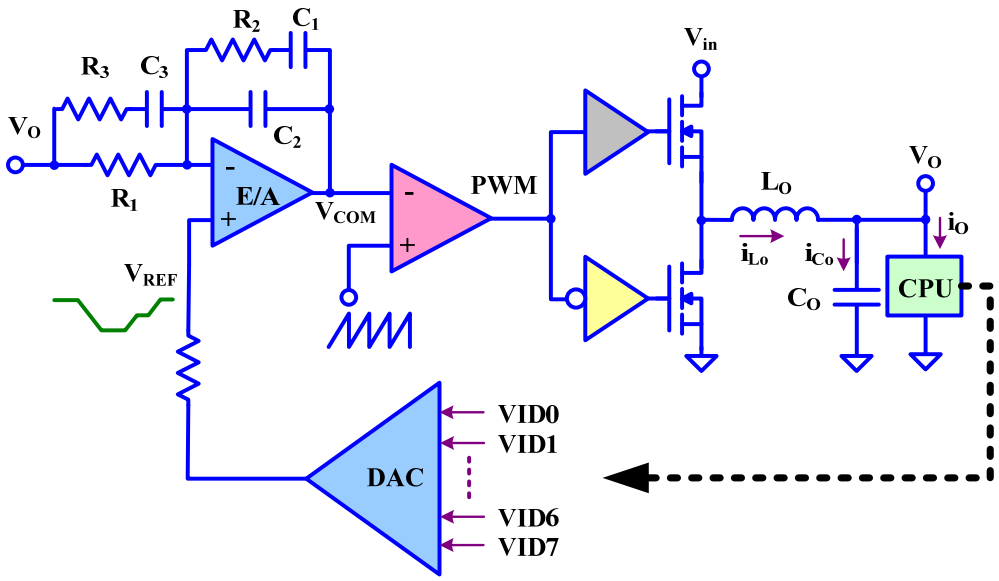


Figure 6-1. Typical voltage regulator with voltage mode control.

Given the total output capacitance, the relationship between the charging/discharging current and DVS slew rate can be expressed by:

$$I_{charge} = C_O \cdot \frac{dV}{dt} \tag{6-1}$$

where I_{charge} is the charging/discharging current during DVS, C_O is the total output capacitance, and dV/dt is the DVS slew rate. It is found that if the DVS slew rate is specified, the total current drawn during DVS is proportional to the output capacitance. Due to the fact that the output inductor cannot change its current immediately, it usually takes a few cycles for the VR to reach the required total current at DVS operation. This time delay results in output voltage deviation or distortion from the reference voltage. Fig. 6-2 shows experimental waveforms of DVS operation of a multiphase voltage regulator. During voltage transitioning, the inductor current is ramping up since extra current is drawn to charge the output capacitors. After the reference voltage

reaches its final value, the inductor current returns to the load current slowly. The extra current will be dumped to the output capacitors and cause voltage deviation. Depending on compensation, there is a considerable settling time of the output voltage at the end of the VID transition.

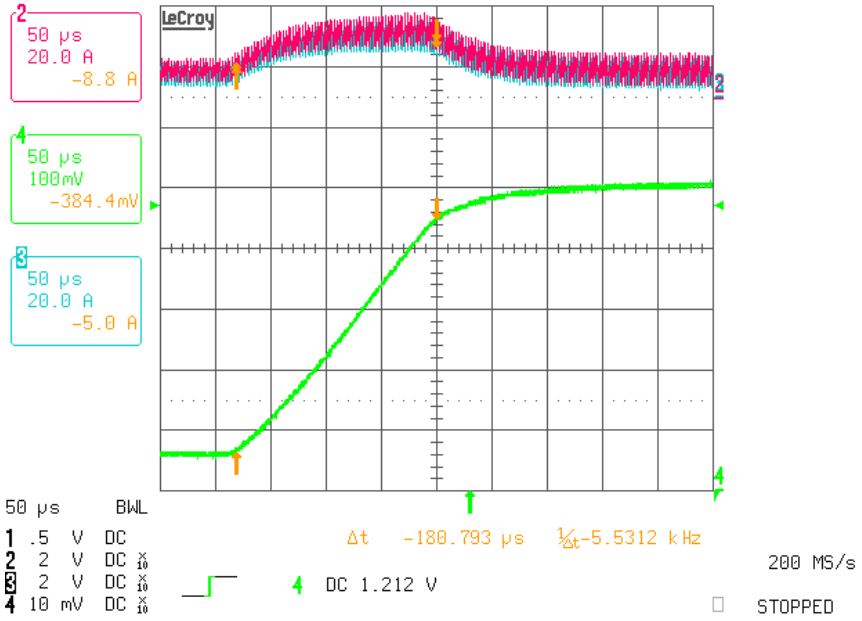


Figure 6-2. Experimental data of DVS operation. (Top traces: output inductor current of two phases, bottom traces: output voltage).

The investigation of DVS would not be complete without the inclusion of adaptive voltage positioning (AVP) control [2] since it has become a common industry practice for microprocessor voltage regulation. AVP adjusts the output voltage based on the load current. A typical method to achieve AVP control is to inject the sensed inductor current to the inverted

input of the error amplifier (Fig. 6-1). This current will flow through R_1 to develop a voltage drop proportional to the load current. During DVS, the inductor current includes both the load current and the charging/discharging current of the output capacitors as derived in Equation 6-1. As a result, the sensed inductor current is different than the real load current, and the output voltage may be regulated to a wrong value due to the extra charging/discharging current of the output capacitors.

Based on the above discussions, it is noted that reducing the output capacitance can bring down the total charging or discharging current for DVS. However, a minimum number of capacitors are usually required to meet both static and dynamic requirements of VR operation. As a result, a method that can optimize DVS operation without change of the VR power stage is desired. In the following discussion, the effect of the compensation network on DVS is studied. Mathematical and simulation analysis show that the compensation network plays an important role in settling the output voltage during DVS operation.

The average model of a typical voltage regulator with voltage mode control shown in Fig. 6-3 is employed to study the effects of compensation on DVS operation. Compared to Fig. 6-1, a block G_m replaces the PWM modulator and it represents the modulation gain, while the block V_{in} is the input voltage gain of the power stage.

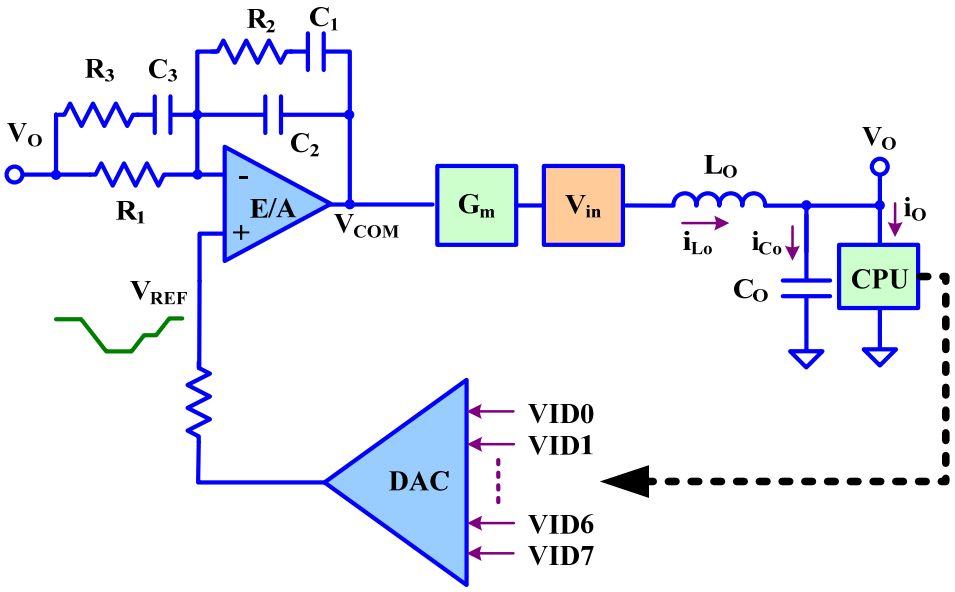


Figure 6-3. Average model of voltage regulator in DVS operation.

During DVS operation, V_{REF} is varied when receiving the VID codes from the microprocessor. Since the VID transitioning slew rate is limited, i.e V_{REF} is moved smoothly, steady-state condition can be approximately assumed during DVS operation. The high gain of the error amplifier then causes the error amplifier output voltage V_{COM} to adjust rapidly to a new level. The V_{COM} can be calculated by the reference voltage V_{REF}, input voltage V_{in}, and the modulation gain G_m:

$$V_{COM} = \frac{D}{G_m} = \frac{1}{G_m V_{in}} V_{REF} \tag{6-2}$$

where D is the duty cycle. Since the voltage at inverted input pin of the error amplifier is equal to the reference voltage V_{REF}, the voltage across C_1 and R_2 in steady state can then be obtained by:

$$V_{COM} - V_{REF} = \frac{G_m V_{in} - 1}{G_m V_{in}} V_{REF} \tag{6-3}$$

According to Equation 6-3, while the reference voltage is changing during DVS, the voltage across C_1 will also adjust to a new level to regulate the output voltage. The change of V_{C1} can be expressed by:

$$dV_{C1} = dV_{COM} - dV_{REF} = \frac{G_m V_{in} \text{-} 1}{G_m V_{in}} \cdot dV_{REF} \tag{6-4}$$

where dV_{COM} and dV_{REF} are the change of error amplifier output voltage and reference voltage, respectively. dV_{C1} then generates charging/discharging current flowing through R_2 and C_1. This current can be given in s-domain by:

$$i_C(s) = \frac{1}{R_2 + \frac{1}{sC_1}} \cdot \left[V_{COM}(s) - V_{REF}(s)\right] = \frac{1}{R_2 + \frac{1}{sC_1}} \frac{G_m V_{in} \text{-} 1}{G_m V_{in}} \cdot V_{REF}(s) \tag{6-5}$$

For a VR with AVP, Equation 6-5 is still valid since the sensed inductor current will mainly flow through R_1 and adjust the output voltage. From Equation 6-5, it is found that if the dynamic VID change is specified, the charging/discharging current is related to the capacitor C_1 and resistor R_2. This charging/discharging current will eventually flow through compensation components R_1, R_3, and C_3 and develop a voltage deviation between output voltage V_O and reference voltage V_{REF} during the DVS voltage transition, resulting in settling time. Thus, both the voltage deviation and settling time depend largely on the R_2C_1 time constant. If the R_2C_1 time constant is too large, it will cause a long settling time and large voltage deviation during DVS operation.

6.3 Proposed Active Compensator for Dynamic Voltage Scaling

The above analysis suggests that both voltage deviation and settling time of DVS depends on the operating voltage across C_1. With a short R_2C_1 time constant, the voltage deviation and settling time in DVS operation can be reduced. However R_2C_1 is typically determined by the whole control loop. Once the power stage and compensation have been optimized, any change of the RC network may result in overall loop gain and phase margin drift which may lead to system instability. Therefore, a method that can improve DVS without impact on loop stability is desired.

Careful analysis discovers that if a specific current can be generated to compensate the charging and discharging current provided for the voltage change of the capacitor C_1, as given in Equation 6-5, the output voltage deviation will be minimized during DVS operation. Based on this observation, an active compensator scheme is proposed. This scheme consists of a voltage doubler in series with a RC network R_D and C_D. The voltage doubler is connected to the V_{REF} pin (positive input of the error amplifier) while the RC network is connected to the inverting input of the error amplifier as shown in Fig. 6-4.

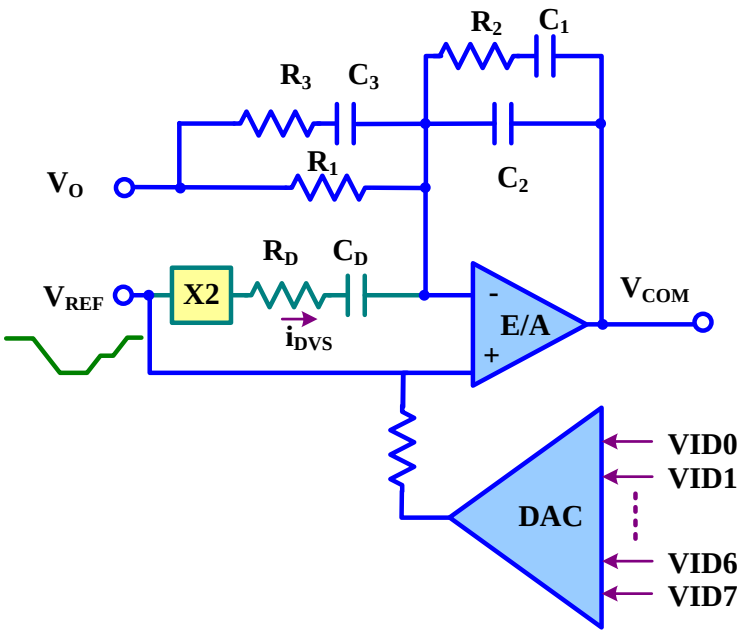


Figure 6-4. Block diagram of the proposed active compensator.

Since the inverting pin voltage is equal to the reference voltage, a voltage equal to the reference voltage is generated across the RC network due to the voltage doubler. In normal operation where the reference voltage is stable, the voltage across the RC network is DC and no current will be generated. During DVS operation, a changing voltage equal to the reference voltage is developed across the R_D and C_D. As a result, a current is generated and will offset the charging/discharging current flowing through the compensation capacitor C_1. The current flowing through the active compensator network can be written as:

$$i_{DVS}(s) = \frac{1}{R_D + \frac{1}{sC_D}} \cdot V_{REF}(s) \tag{6-6}$$

In order for i_{DVS} to counter the charging/discharging current i_C from C_1, Equation 6-5 must be equal to Equation 6-6. Manipulating these two equations leads to the design formula for R_D and C_D:

$$R_D = K_D R_2 \tag{6-7}$$

$$C_D = \frac{C_1}{K_D} \tag{6-8}$$

where,

$$K_D = \frac{G_m V_{in}}{G_m V_{in} - 1} \tag{6-9}$$

It suggests that if R_D and C_D are designed such that Equations 6-7, 6-8, and 6-9 are met, then the active compensator will provide a current i_{DVS} which is equal to the required current to charge or discharge the capacitor C_1 during DVS. As a result, there will be less voltage deviation and shorter settling time on output voltage during DVS. Since the proposed active compensator comes into play only during DVS, and the VID transitioning slew rate is fairly slow as mentioned in last section, steady-state operation can be assumed during DVS operation. Therefore, the proposed active compensator scheme has no impact on system small-signal performance, e.g. closed-loop gain and output impedance. Pspice simulation results in Fig. 6-5 are provided to verify this proposed scheme. Without the active compensator, there is a significant deviation between V_O and V_{REF} while this deviation is reduced to a large extent by applying the proposed active compensator.

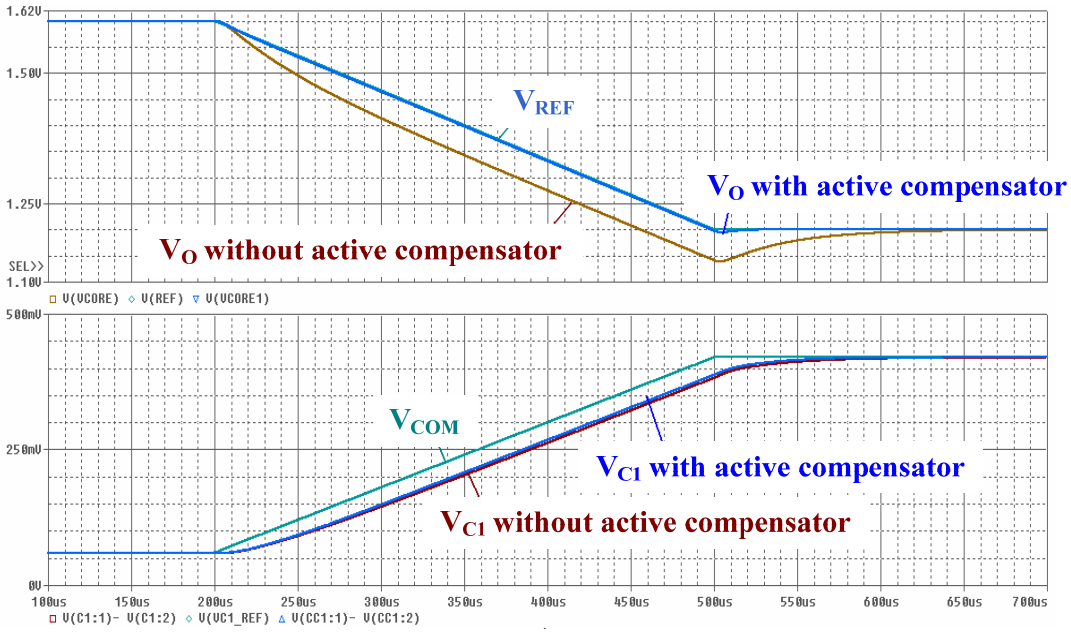


Figure 6-5. Simulation comparison of DVS operation with and without the active compensator.

6.4 Experimental Results

A voltage regulator prototype was developed to verify the proposed active compensator scheme. The circuit parameters are as the following:

V_{in} = 12 V;

V_O = 1.1 V – 1.4 V;

Switching frequency = 500 kHz.

Controller: ISL6333 from Intersil;

Output inductors: THCBR1290-221-R from Delta (L = 220 nH);

Output capacitance: 5 x 560 uF polymer capacitors + 18 x 22 uF MLCC;

The voltage doubler of the active compensator is integrated in the controller ISL6333 [17], where a pin "DVC" is designated for the active compensator design. The compensation components R_2, C_1, and designed active compensator values are given as:

R_2 = 12.1 kohm;

C_1 = 1000 pF;

R_D = 14 kohm;

C_D = 820 pF.

where the components are chosen based on standard industry values. Fig. 6-6 shows experimental results of DVS operation without the proposed scheme. The top trace is the VID voltage V_{REF} and the bottom trace is the output voltage V_O. When the VID voltage V_{REF} changes from 1.1 V to 1.4 V within 120 uS, the output voltage V_O sees about 29mV voltage overshoot and undershoot during each DVS transition. Also, V_O settles down to its final value fairly slow due to the large R_2C_1 time constant. With the proposed active compensator, the experimental results are shown in Fig. 6-7. It is found that the proposed active compensator scheme significantly improves the DVS performance with much less voltage deviation and settling time, even though the same compensation and power stage parameters are implemented.

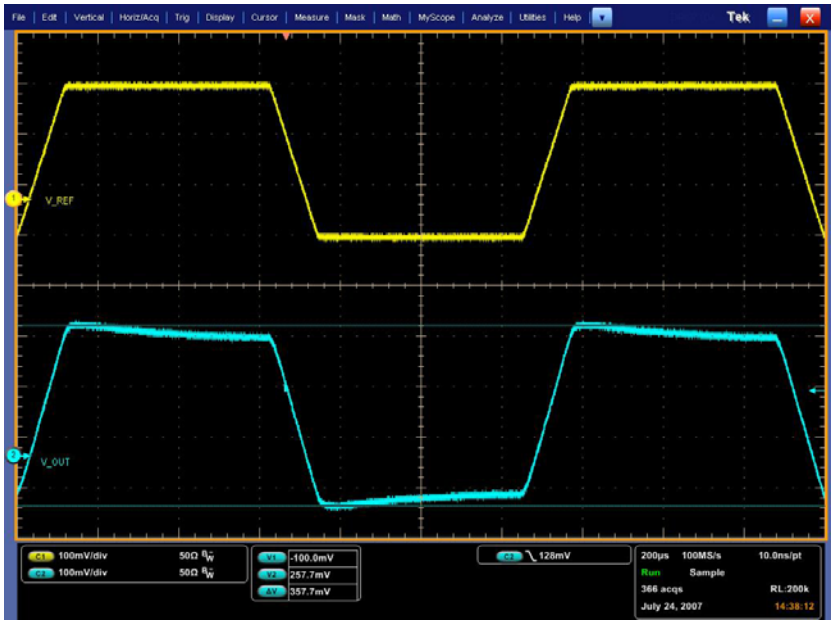


Figure 6-6. Experimental results for VR without active compensator during DVS.

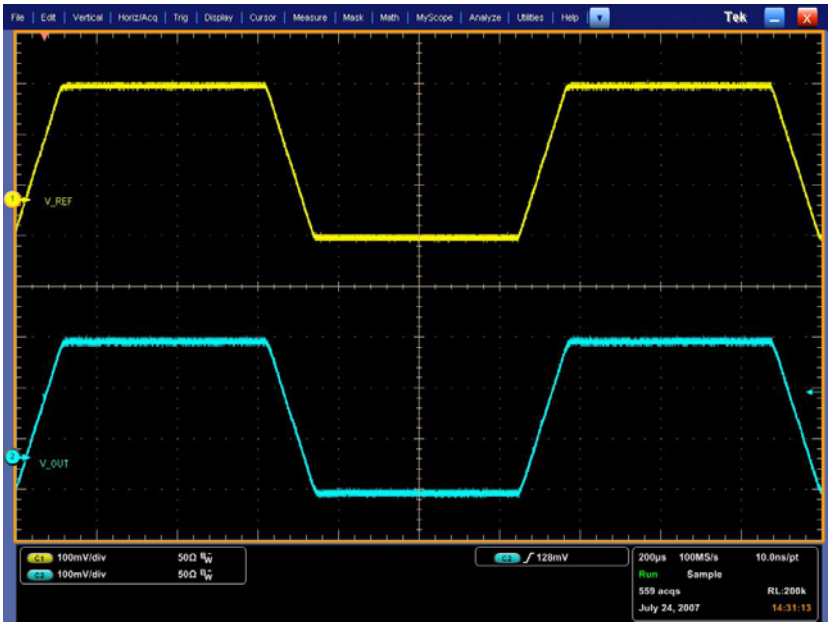


Figure 6-7. Experimental results for VR with active compensator during DVS.

6.5 Summary

Although dynamic voltage scaling (DVS) technique is a common industry practice to improve the efficiency of microprocessor operation, VR designers are facing challenges such as output voltage deviation and slow settling time. While reducing output capacitance and changing compensation may help improve DVS, the improvement comes at the cost of sacrificing static and dynamic performance. In this paper, an active compensator is proposed to improve the DVS operation without changing the power stage and compensation. Simulation data and experimental results have verified the effectiveness of this new scheme.

CHAPTER 7 CONCLUSIONS

VR is a dedicated DC-DC converter to power the microprocessor. The real challenges for VR design for the future microprocessors are to address fast transient, high current, and extremely low output voltage. Multi-phase VR is becoming an industry practice. Nevertheless, to meet the transient requirements, a huge number of output decoupling capacitors are usually needed to keep the voltage within the specified window, which is undesired from both the cost and the motherboard real estate aspects. One way to save the output bulk capacitors is to increase the control-loop bandwidth. However, the bandwidth is limited in the practical design. Running the converter at a higher frequency appears to be an ultimate solution to reducing the cost and size of those expensive capacitors. However, when the converter switching frequency increases, the switching-frequency-related power losses of the converter increase as well. Meanwhile, due to the increasing current demand, conduction losses also increase. All of this loss poses severe thermal problems to the VRM designers. This dissertation is engaged in exploring novel solutions for transient improvement of multi-phase voltage regulators.

Starting from the introduction of multi-phase VR with droop control, a novel adaptive modulation control (AMC) scheme is proposed. AMC enables multi-phase VR to operate with an extremely high bandwidth during steady-state. The key is AMC is able to adaptively adjust the bandwidth in different operating states. Aided with AMC, multi-phase VR design can achieve fast transient response without sacrificing system stability. Simulation and experimental results have verified AMC and related analysis.

The error amplifier plays an important role in VR closed-loop performance. During large load transitions, the error amplifier is usually driven to saturation and the PWM output becomes zero or one. The slow recovery time of the error amplifier deteriorates transient response since it causes turn-on and turn-off delays. The introduction of the error amplifier voltage positioning (EAVP) gives a feasible solution to the turn-on and turn-off delays resulted from the error amplifier saturation. The EAVP facilitates the recovery time by applying extra voltage to the output of the error amplifier. This extra voltage is fed back to the input and amplified by the amplifier toward an inverse direction. Therefore, the output voltage is expected to recover sooner. Compared with regular multi-phase VR by simulation and experiments, the EAVP yields much better transient performance.

As an alternative solution to transient response and efficiency of VR design, coupled inductors are drawing more and more attention from both industry and academia. This dissertation investigates the fundamental theories, operational principles, and design of coupled inductors. A state-space-averaging model is built for a two-phase VR with coupled inductors. The DC solutions of the phase currents indicate that a two-phase coupled-inductor VR has exactly the same phase currents as that of a two-phase non-coupled VR. Neither magnetizing inductance nor leakage inductance has any effect on phase DC currents. If the circuit is not symmetric, the phase with smaller R_{dson} and DCR will have larger DC current. In terms of AC solutions, however, if the coupled inductors are not symmetric, the magnetizing inductance L_M will affect the dynamic response, specifically, decreasing the LC double-pole frequency.

New DCR current sensing topologies are proposed. Compared to their conventional counterparts, the proposed topologies cannot only sense the total current, but also the exact phase currents, leading to accurate phase current limit and excellent current regulation. Meanwhile, the proposed topologies feature ease of implementation and can be extended for multi-phase application.

A Full Bridge Coupled-Inductor (FBCI) topology is offered in this dissertation. The impressive features of the FBCI are its flexibility in terms of both topology and core implementation. By turning on or off the well-controlled switches, FBCI is able to optimize its topology upon different operational environments. As a result, both high steady-state efficiency and fast transient response can be achieved. As for the core implementation aspect, all inductor windings can be implemented on a single core structure for centralized application or on discrete cores when distributed application is desired. Simulation results suggest that FBCI show great advantages over conventional coupled-inductor topologies.

To complete the exploration of the coupled inductors, a new magnetics design methodology is introduced. This methodology features intensive use of simulation tools. Throughout this chapter, Maxwell 2D and 3D are employed to compute the magnetic copper losses and core losses. By varying the winding structure, core shape, and core material, an optimal magnetics design can be achieved. This design platform can be applied to coupled-inductor design successfully.

Dynamic Voltage Scaling (DVS) is a technique that dramatically reduces energy consumption in high performance computing systems. In the DVS, energy savings are achieved by adjusting the supply voltage to the workload demands as receiving the VID commands from the microprocessor. As a result from the constraints of output filters and compensation, the output voltage usually deviates from the VID voltage. An active compensator is presented to target this problem without change of output filters and compensation design. During DVS, this compensator generates a current to offset the charging/discharging current of the compensation network which will otherwise cause output voltage deviation. Therefore, it provides an effective way to optimize DVS operation.

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