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DESIGN AND IMPLEMENTATION OF A DIGITAL CONTROLLER WITH DSP FOR HALF-BRIDGE DC-DC CONVERTERS

by

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M.S. University of Central Florida, 2004

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the Department of Electrical & Computer Engineering
in the College of Electrical and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2004

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ABSTRACT

DC-DC power converters play an important role in powering telecom and computing systems. With the speed improvement and cost reduction of digital control, digital controller is becoming a trend for DC-DC converters in addition to existed digital monitoring and management technology. In this thesis, digital control is investigated for DC-DC converters applications.

To deeply understand the whole control systems, DC-DC converter models are investigated based on averaged state-space modeling. Considering half-bridge isolated DC-DC converter with a current doublers rectifier has advantages over other topologies especially in the application of low-voltage and high-current DC-DC converters, the thesis take it as an example for digital control modeling and implementation.

In Chapter 2, unified steady-state DC models and small-signal models are developed for both symmetric and asymmetric controlled half-bridge DC-DC converters. Based on the models, digital controller design is implemented. In Chapter 3, digital modeling platforms are established based on Matlab, Digital PID design and corresponding simulation results are provided. Also some critical issues and practical requirements are discussed. In Chapter 4, a DSP-based digital controller is implemented with the TI's DSP chip TMS320F2812. Related implementation methods and technologies are discussed. Finally the experimental results of a DSP-based close-loop of HB converter are provided and analyzed in Chapter 5, and thesis conclusions are given in Chapter 6.

This document is dedicated to God, my parents and my husband Hong Mao

ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Issa Batarseh for his constant encouragement and thought provoking ideas that had helped me in this thesis work. I would also like to thank Dr. Jaber AbuQahouq and Dr. Thomas X. Wu for their suggestions and for being on my thesis committee. I would also like to thank my husband Hong Mao, my parents and friends for giving me the necessary impetus towards the development of this thesis work.

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CHAPTER ONE: INTRODUCTION

Power control schemes have been revolutionized over the past few decades. Compared with analog controller, digital controller is receiving much attention because of its stable performance, flexibility and ability of more complicated control techniques.

The advent of programmable digital signal processors (DSPs) in recent years is creating thriving opportunities in power electronics. The special architecture and high performance of DSPs make it possible to implement a wide variety of control and measurement algorithms at a high sampling rate and reasonable cost. Power electronics systems are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics. Real-time power electronics systems, therefore, demand the use of high-speed data-acquisition and control. High performance DSPs meet the processing requirements imposed by such systems.

1.1 DC-DC Converter

DC-DC converters are used in power electronics circuits to convert an unregulated DC input voltage to a regulated or variable DC output voltage. The circuit's main commercial application is in systems that require a stable and regulated DC output voltage. Switching devices are normally operated at very high frequency reaching as high as a few hundred kilohertz.

Switching converters use power semiconductor devices to operate in either the on state or the off state. Since the recent advances in semiconductor technology allow the capabilities of very high switching speed and high power handling, it is possible to convert DC to DC with higher efficiency using a switching regulator [1].

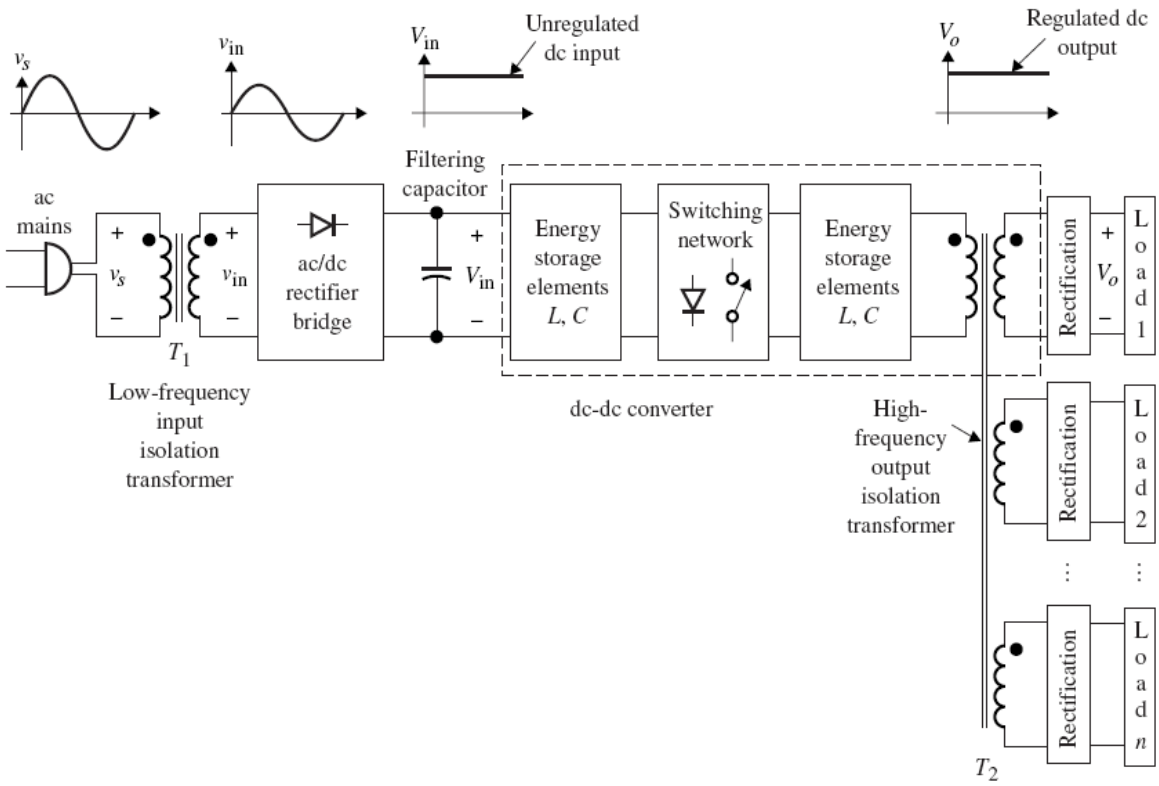


Figure1.1 Block diagram of a switch mode power supply with multiple output [1]

Figure 1.1 shows a typical block diagram for a switched mode AC-DC power converter with multiple output application. The front end of the DC-DC converter is a low-frequency transformer, used to provide input electrical isolation and to step up or step down the voltage,

which is followed by a full wave bridge rectifier to converter the AC to DC This DC input to the DC-DC converter, V_{in}, is unregulated DC and can't be used to drive the load directly. DC-DC converter provides a stable DC output, V_o.

DC-DC converters store energy in an inductor, capacitor or both during operation. This energy is then distributed to the load over a period of time. This distribution of the stored energy is accomplished efficiently by varying the charging time for the energy storage device, depending on the load, for every time period. The charging time period corresponds to the switching action of the power converter, which is controlled by an external circuitry.

Depending on whether or not an output transformer is used, high-frequency DC-DC switching converters are classified as isolated or nonisolated. For isolated DC-DC converters, the main types of converters are as follows: buck, boost, buck-boost and Cuk. However, in most of the practical applications, isolation is required for the DC-DC converters, which include some widely used topologies, such as the flyback, forward, push-pull, half-bridge and full bridge converters.

1.2 Controller for DC-DC Converter

In a DC-DC converter application, it is desired to obtain a constant output voltage in spite of disturbances in input voltage and load current. Therefore, the idea behind the use of negative feedback for control is to build a circuit that automatically adjusts the duty cycle as needed to obtain the desired output voltage with high accuracy, regardless of disturbances in input and load.

A block diagram of a feedback system is shown in Figure 1.2. The output voltage $v(t)$ is measured using a "sensor" with transfer function of $H(s)$ [9]. The sensor output $H(s)v(s)$ is compared with a voltage reference $V_{ref}(s)$. The error between $H(s)v(s)$ and $V_{ref}(s)$ is feed to compensator that amplifies error signal and makes the output voltage regulated around reference voltage. In practice, the error is usually nonzero and nonetheless small enough. A compensator gain $G_c(s)$ helps to obtain a small error and improve the stability and performance of the system. The PWM (pulse width modulator) modulator is used to generate "digital" pulse width feed into the switch of converter. The pulse width changes with the comparator output voltage $V_c(t)$.

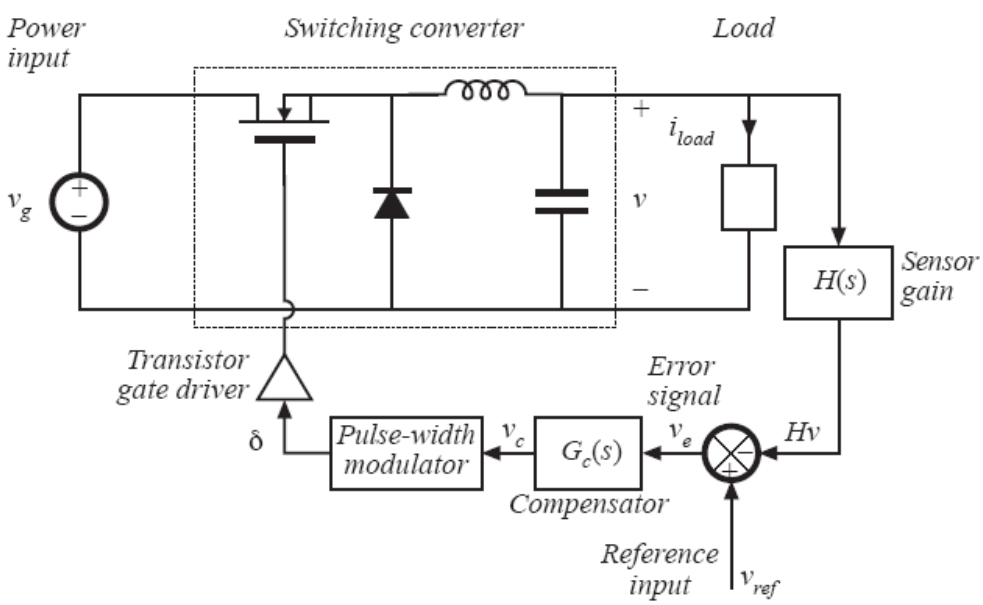


Figure1.2 Feedback loop for switching converter [9]

The traditional approaches for controllers of DC-DC converters based on duty ratio adjustment have relied on analog implementation schemes. The above mentioned control strategies based on analog techniques offer robust control, but suffer from serious limitations such as sensitivity to noise and temperature change. Hence, this trend has moved towards digital control schemes, which offer multitudinous benefits. Digital controllers for switching power supplies offer a number of advantages including a reduction of the number of passive components, programmability, implementation of more advanced control algorithms and additional processing options, as well as reduced sensitivity to parameter variations.

Generally, there are several implementation approaches for digital controllers today, which include Microprocessor/DSP's (Digital Signal Processors), FPGA (Field Programmed Gates Array) and Custom IC Design. The features of these approaches are compared in the following list.

DSP:

- DSP chips can be reprogrammed;
- The speed is generally slower than ICs;
- Implementation is exceedingly complex for the intended application;
- DSP is costly over custom IC design;
- High frequency power converters have to use high performance DSPs;

FPGA:

- FPGA can be programmed on site;
- The processing is faster than a general purpose DSP;
- For FPGA design there is no physical manufacturing step, which results in very short design time;
- FPGA's typical price is higher than DSPs;

Custom IC Design:

- Due to physical design consideration the typically better performance than FPGA;
- However it results in much longer design time than FPGA since there is a layout step;
- Custom IC design has lower price than FPGA and DSP.

In this thesis, the features that make DSPs effective computational engines for high frequency switching power converters are presented. A case study is introduced in which a DSP-based solution was developed as a controller for a half-bridge DC-DC converter with a current doubler, which is widely used in low voltage applications. The design, implementation and testing of a DSP-based system are illustrated, and the techniques and challenges in system design based on DSPs are also addressed. DSP designs are optimized to handle real-time applications with high bandwidth requirements.

1.3 Limitations of Digital Controller

Over analog controller for power converters digital controller has some limitations. Due to digital controller's inevitable involving of ADC, the system's performance must be affected by the ADC. A complete analog system is simpler than a high speed and high resolution ADC. Moreover, available microcontroller or DSP now are still too slow and too costly for the power converters. A high speed and high resolution of DPWM is also too costly for the power application. Furthermore, digital controller increases the complexity of the system due to ADC and digital processing.

1.4 Thesis Chapter Synopses

Chapter two focuses on analyzing the topology and operation of the half-bridge DC-DC converter with current doublers. The modeling of the topology, including steady state average model and small-signal dynamic model, are established and the related controller compensation design issues are addressed based on the models and analysis.

Chapter Three discusses digital control, which includes the theory, methodology and critical issues of a digital controller. As a case study, a digital PID compensator is designed based on the specifications of the given power stage. Also, this chapter explores the modeling and simulation of a digital controller with an 8-bits microprocessor in Matlab/Smulink. Finally, digital controller design issues are addressed.

Chapter Four explores DSP implementation of a digital controller, which brings in the introduction of DSP chips, to be specific, TI C24X and TMS320F2812. Then, the PWM generators and ADC of TMS320F2812 are emphasized as the important devices in the controller. Controller implementation based on the TMS320F2812 is described as one of the important part of the thesis.

Chapter Five provides and analyzes the experimental results of closed-loop DSP controlled half-bridge DC-DC converter. Also Practical issues for DSP-based controller design on the platform are discussed. Finally the conclusion of future work will be presented in chapter six.

CHAPTER TWO: HALF-BRIDGE CONVERTERS WITH CURRENT DOUBLERS

The half-bridge (HB) DC-DC converter is an attractive topology for middle-power level applications due to its simplicity. There are two conventional control schemes for the HB DC-DC converter, namely symmetric control and asymmetric (complimentary) control. A HB DC-DC converter with a Current Doubler Rectifier (CDR) is suitable for high-current low-voltage applications, since the CDR structure has lower conduction loss compared to the center-tap rectifier.

In this chapter, an average space-state model is established for the half-bridge DC-DC converter with current doubler rectifier while taking into consideration the parasitic DC parameters. Based on the DC model, a unified small-signal model is established, and design issues are provided with both symmetric HB and asymmetric HB DC-DC converters. Also, utilizing the small-signal model, some design guidelines and issues of close loop design are discussed and investigated.

2.1 Topology and Operation

The half-bridge DC-DC converter with a current doubler rectifier (CDR) is shown in Figure 2.1, which can be controlled symmetrically or asymmetrically. Neglecting the leakage inductance and transient commutation, and considering the converter operating at CCM mode

due to the synchronous rectifier, the converter has three typical modes as shown in Figure. 2.2 (a)(b)(c). The operation modes are well known and readers can refer to [2] for more details.

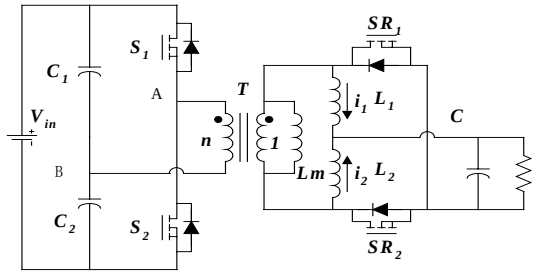
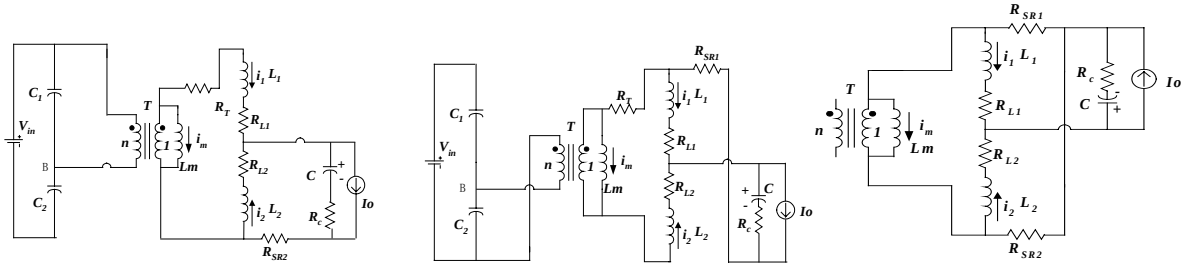


Figure 2.1 CDR half-bridge DC-DC converter



(a) Mode 1: S1 is on (b) Mode 2: S2 is on (c) Mode 3: Both S1 and S2 are off

Figure 2.2 Operation modes

2.2 State-Space Model and DC Bias Analysis for Symmetrical and Asymmetrical HB Converters with Current Doublers

In the operation modes, the load is assumed as a constant current source, since the voltage ripple is ignorable. In a switching cycle, the converter can be denoted using three linear state-space equations, respectively. The three corresponding space-state equations can be expressed as:

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \quad y = Cx + Eu \tag{2-1}$$

where $x = [v_{c1} \;\; i_{L1} \;\; i_{L2} \;\; v_{co} \;\; i_m]^T$ $\quad \dot{x} = \frac{dx}{dt}$ $\quad u = [V_{in} \;\; I_o]^T$ $\quad y = v_o$

During the on time of switch S_1, the corresponding matrices are A_1 and B_1; during the on time of switch S_2, the corresponding matrices are A_2 and B_2; during the off time of both switch S_1 and S_2, the corresponding matrices are A_3 and B_3. All matrixes above are as follows:

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{n} & 0 & 0 & -\frac{1}{n} \\ \frac{1}{n} & -(R_{L1}+R_C+R_{SR2}+R_T) & -(R_C+R_{SR2}) & -1 & 0 \\ 0 & -(R_C+R_{SR2}) & -(R_{L2}+R_C+R_{SR2}) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -(R_C+R_{SR1}) & -1 & 0 \\ -\frac{1}{n} & -(R_C+R_{SR1}) & -(R_{L2}+R_C+R_{SR1}+R_T) & -1 & 0 \\ 0 & 1 & 1 & 0 & 0 \\ \frac{1}{n} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -(R_{L1}+R_C+R_{SR1}) & -R_C & -1 & -R_{SR1} \\ 0 & -R_C & -(R_{L2}+R_C+R_{SR2}) & -1 & R_{SR2} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & -R_{SR1} & R_{SR2} & 0 & -(R_{SR1}+R_{SR2}) \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T \quad B_2 = \begin{bmatrix} 0 & 0 & \frac{1}{n} & 0 & -\frac{1}{n} \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T \quad B_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & R_c & R_c & -1 & 0 \end{bmatrix}^T$$

$$C = [0 \quad R_c \quad R_c \quad 1 \quad 0] \quad E = [0 \quad -R_c]$$

Assuming the switch S_1 on-time is D_1T and switch S_2 on-time is D_2T, the switching cycle is T. The key concept in state-space averaging is the replacement of the above three sets of state-space equations by a single equivalent set:

$$\dot{x} = Ax + Bu \qquad y = Cx + Eu \tag{3-2}$$

where the equivalent matrices are defined by:

$$A = D_1A_1 + D_2A_2 + (1 - D_1 - D_2)A_3 \qquad B = D_1B_1 + D_2B_2 + (1 - D_1 - D_2)B_3$$

The steady-state solution, with DC values indicated by capital letters, is obtained by setting:

$$\dot{x} = 0 : X = -A^{-1}BU \tag{3-3}$$

From Equation 3-3, the steady-state DC quiescent point can be obtained, where the inductor and magnetizing average currents are as follows:

$$I_{L1} = \frac{d_2R_T + R_{L2}}{(d_1+d_2)R_T + R_{L1} + R_{L2}} I_o$$

$$I_{L2} = \frac{d_1R_T + R_{L1}}{(d_1+d_2)R_T + R_{L1} + R_{L2}} I_o$$

$$I_M = \frac{d_2R_{L1} - d_1R_{L2}}{(d_1+d_2)(R_{L1}+R_{L2}) + (d1+d2)^2 R_T} I_o \tag{3-4}$$

The equations derived above are general solutions for both symmetric and asymmetric half-bridge DC-DC converters. From the equations above, it can be observed that:

(1) Only DC resistances and duty cycles, other than capacitance and inductance, have an effect on the DC current's distribution.

(2) Unbalanced inductor average currents and DC bias of a magnetizing current exist due to either asymmetry of equivalent DC resistance (DCR) or duty cycles.

(3) On-resistance of synchronous rectifiers has no effect on the DC current's distribution and averaged magnetizing current.

For the HB converter, peak-current-mode control cannot be applied. The natural current sharing between the two inductors is needed. However, the DC current sharing cannot be achieved due to unbalanced DC resistive parameters $R_{L1} \neq R_{L2}$ or unbalanced duty cycle $D_1 \neq D_2$. The PCB layout of two-channel inductors should be as symmetric as possible, and both the driving channel and switch should match to achieve symmetric duty cycles. If the PCB layout has to be asymmetric, synchronous rectifiers can be asymmetric instead of inductors. As a result of asymmetry, there is a DC magnetizing current bias in the transformer, which should be estimated when designing the transformer [2].

For an asymmetric HB converter, DC solutions can be obtained by substituting $D_2 = 1 - D_1$ into the DC solutions. From the solution, one may conclude:

(1) The current sharing between two inductors is uneven because of the asymmetric duty cycle.

(2) The transformer has DC bias of magnetizing current due to asymmetric duty cycle, and an air gap has to be added to avoid the transformer saturation.

2.3 Unified Small-Signal Model for Half-Bridge DC-DC Converter

The unified small-signal model of the half-bridge converter with a current doubler can be derived based on the unified model shown in Equation 2-3 and a small-signal assumption. Disturbing the unified state-space average Equation 2-2 as follows:

$$y = Y + \hat{y} \quad x = X + \hat{x} \quad u = U + \hat{u} \quad d_1 = D_1 + \hat{d}_1 \quad d_2 = D_2 + \hat{d}_2 \tag{2-5}$$

Substituting Equation 2-5 into Equation 2-2 and removing the DC bias from the obtained equation and ignoring high-order terms, one can derive the unified small-signal linear models for both symmetrical and asymmetrical HB converters:

$$\hat{x}(s) = (sI - A)^{-1} B\hat{u}(s) + (sI - A)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)]X + (sI - A)^{-1}[\hat{d}_1(s)(B_1 - B_3) + \hat{d}_2(s)(B_2 - B_3)]U \tag{2-6}$$

$$\hat{y}(s) = C(sI - A)^{-1} B\hat{u}(s) + C(sI - A)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)]X + (sI - A)^{-1}[\hat{d}_1(s)(B_1 - B_2) + \hat{d}_2(s)(B_2 - B_3)]U + E\hat{u}(s) \tag{2-7}$$

The unified output-to-control transfer function can be obtained:

$$\begin{aligned}\frac{\hat{y}(s)}{\hat{d}(s)}\Big|_{\hat{u}(s)=0} = {} & C(sI - D_1A_1 - D_2A_2 - (1-D_1-D_2)A_3)^{-1}[\hat{d}_1(s)(A_1 - A_3) + \hat{d}_2(s)(A_2 - A_3)][D_1A_1 + D_2A_2 + (1-D_1-D_2)A_3]^{-1}[D_1B_1 + D_2B_2 + (1-D_1-D_2)B_3]\frac{-U}{\hat{d}(s)} \\ & + (sI - D_1A_1 - D_2A_2 - (1-D_1-D_2)A_3)^{-1}[\hat{d}_1(s)(B_1 - B_2) + \hat{d}_2(s)(B_2 - B_3)]\frac{U}{\hat{d}(s)}\end{aligned} \tag{2-8}$$

The open-loop output impedance of the half-bridge converter can be derived as:

$$Z_{output} = \frac{\hat{V}_o}{\hat{i}_o}\Big|_{\hat{d}(s)=0} = [C(sI - A)^{-1} B + E]_{12} \tag{2-9}$$

Even the symmetric HB and asymmetric HB have different average matrixes A and B. They have identical open-loop output impedance.

For symmetrical HB, the two switches operate at the same steady-state duty cycle D1 = D2 = D, and the duty cycles of the two switches disturbance are $\hat{d}_1(s) = \hat{d}(s)$ and $\hat{d}_2(s) = \hat{d}(s)$. Substituting the two conditions into Equation 2-6, the linearized small-signal state-space equation of symmetric HB is obtained:

$$\hat{x}(s) = \left[sI - D(A_1 + A_2) - (1-2D)A_3\right]^{-1}\left[D(B_1 + B2) + (1-2D)B3\right]\hat{u}(s) + (sI - A)^{-1}[(A_1 + A_2 - 2A_3)X + (B_1 + B_2 - 2B_3)U]\hat{d}(s)$$

(2-10)

The output-to-control transfer function of symmetric HB is:

$$\hat{y}(s) = C(sI - A)^{-1}B\hat{u}(s) + C(sI - A)^{-1}[(A_1 + A_2 - 2A_3)X + (B_1 + B_2 - 2B_3)U]\hat{d}(s) + E\hat{u}(s) \quad (2\text{-}11)$$

If the HB converter has half-bridge circuits balanced, it means $L_1 = L_2 = L$, $R_{L1} = R_{L2} = R_L$, from Equation 2-11 yields the output-to-control transfer function:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{(V_{in} - R_T I_o n)(sC_o R_c + 1)}{n(s^2 C_o L + sC_o D R_T + sC_o R_L + 2sC_o R_c + 2)} \quad (2\text{-}12)$$

From Equation 2-12, we can see that symmetric HB is a second-order system. Due to the symmetric control, the magnetizing inductance and input capacitance has no impact on the dynamic system model. From a control point of view, this is a advantage over asymmetric HB, because it makes the system design easier. The output impedance is given in Equation 2-13, and the bode diagram and output impedance is plotted in Figure 3-13.

$$Z_{output} = \frac{\hat{V}_o}{\hat{i}_o}\bigg|_{\hat{d}(s)=0} = \frac{s^2 L C_o R_c + sL + sdR_T C_o R_c + sR_L C_o R_c + dR_T + R_L}{s^2 C_o L + sC_o dR_T + sC_o R_L + 2sC_o R} \quad (2\text{-}13)$$

For asymmetric HB, the two switches operate at duty cycle D and 1-D, so we set the steady-state values D_1 = D and D_2 = 1-D. Substituting them into Equation 2:

$$A = D(A_1 - A_2) + A_2 \qquad B = D(B_1 - B_2) + B_2 \quad (2\text{-}14)$$

Setting the disturbance $\hat{d}_1 = \hat{d}$, $\hat{d}_2 = -\hat{d}$ and substituting them into Equation 2-7 yields:

$$\hat{y}(s) = C(sI - A)^{-1} B\hat{u}(s) + C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}(s) + E\hat{u}(s) \tag{2-15}$$

$$\frac{\hat{y}(s)}{\hat{d}(s)}\Big|_{\hat{u}(s)=0} = C(sI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)U] \tag{2-16}$$

The bode diagram has been calculated and plotted for the following set of parameters and is shown in the following figures from Figure 2.3~Figure 2.5.

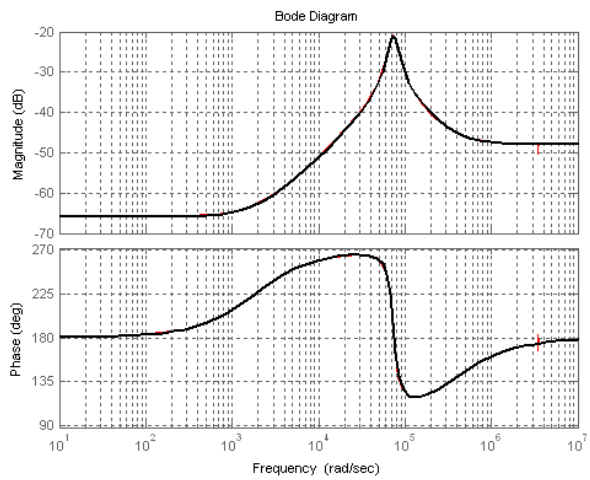


Figure 2.3: Symmetric and asymmetric HB output impedance

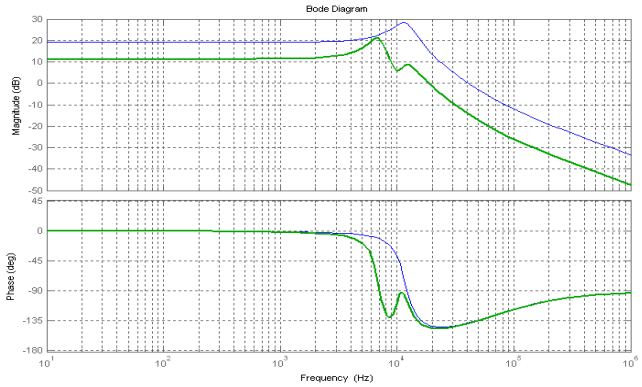


Figure 2.4: Bode diagram of symmetric and asymmetric HB converters (blue: symmetric HB, green: asymmetric)

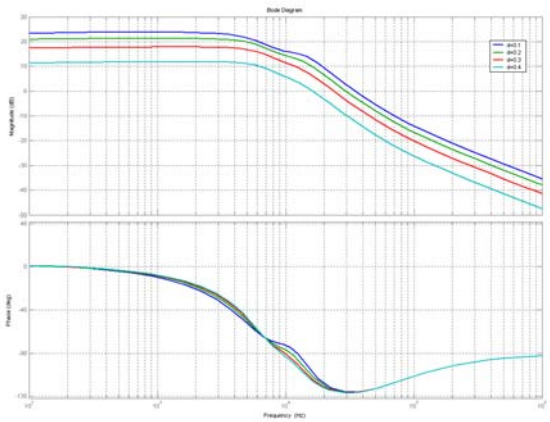


Figure 2.5: Asymmetric HB bode diagram with changing duty cycle

The asymmetric HB bode diagram is illustrated in Figure 2.3. Compared with symmetric HB, the asymmetrical HB is a fourth-order system. It has two pairs of LC poles. A LC pole is

constituted of transformer magnetizing inductance L_m and the input equivalent capacitance $2C_1$. Another LC pole is determined by equivalent output inductance $L/2$ and output capacitor Co.

2.4 Analysis and Controller Design Issues

Utilizing the described small-signal model, close loop could be designed. Generally, the criteria for a feedback loop design is [9]:

- Provide the gain slope at crossover –20db/dec.
- Provide maximum possible open loop gain at DC for good static regulation.
- Provide maximum possible gain at low frequencies for good ripple rejection.
- The switching frequency is at least 10 to 15 times higher than the open loop crossover frequency.

  For the asymmetrical HB, some close loop design issues have to be considered:

- In order to get wider bandwidth, the resonant frequency $f_2 = \frac{1}{2\pi\sqrt{LC_o/2}}$ should be much larger than the resonant frequency of the input LC network, which is $f_1 = \frac{1}{2\pi\sqrt{2L_mC_p}}$.

  Therefore, high input capacitance and large magnetizing inductance are good for the close loop design.

- When the input fitter LC pole appears in the low-frequency band, the system is close to symmetric HB, which is good for the control loop compensation.

With decreasing duty cycle, the gain increases and results in lower phase margin. Therefore, when doing the feedback loop design, the worst case must be considered first.

CHAPTER THREE: DIGITAL CONTROLLER DESIGN

Digital controllers offer a number of advantages in DC-DC power converters, and various analysis, design and implementation aspects of this emerging area are receiving increasing attention. A digital controller system is one or more silicon chips that combine ADC conversion with control law processing, PWM and communication elements operating entirely (or mostly) in digital mode.

From what has been demonstrated so far, it is clear that benefits will be derived from digital control. With digital controller, compensator and protection features can be programmable, reducing or eliminating the need for passive components for tuning. Digital controllers have inherently lower sensitivity to process and parameter variations. Furthermore, digital controllers allow the system to have communications and data management, such as storing data for operational purposes. Also, it is possible to implement control schemes that are considered impractical for analog realizations. For example, a what-if process can be made easily available for a digital controller versus an analog controller. In transformer-isolated DC-DC converters, digital signal transmission through isolation can be used to address limited bandwidth and/or large gain variations associated with standard analog approaches. In general, more sophisticated control methods can be applied to achieve improved dynamic responses.

3.1 Theory and Methodology

As the Shannon sampling theorem shown in Figure 3.1, a function $e(t)$ that contains no frequency components greater than f_o is uniquely determined by the values of $e(t)$ at any set of sampling points spaced $\frac{1}{2f_0}$ seconds apart. This means that when choosing the sampling rate for a control system, the sampling frequency should be greater than twice the highest-frequency component of the significant amplitude of the signal being sampled [4].

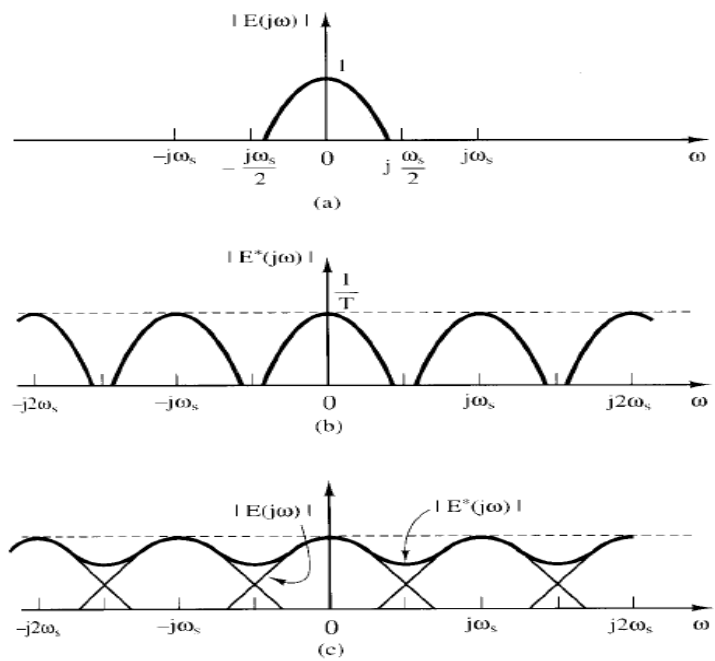


Figure 3.1 Shannon sampling theorem [4]

A typical digital control system is shown in Figure 3.2. The system contains a sampler to detect continuous analog signal at discrete instances of time. Before a data hold is employed to

reconstruct the original signal, a digital compensator block is added to improve system performance.

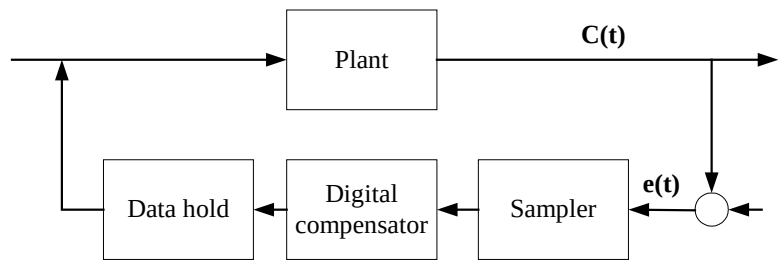


Figure 3.2. Typical digital control system

A commonly used method of data reconstruction is polynomial extrapolation. Using a Taylor's series expansion, one can express $e(t)$ as:

$$e(t) = e(nT) + e'(nT)(t - nT) + \frac{e''(nT)}{2!}(t - nT)^2 + ... \tag{3-1}$$

If the first term above is used, the data hold is called a zero-order hold, which is expressed as $e_0(t) = u(t) - u(t - T)$. The corresponding transfer function is $G_{h0}(s) = \frac{1 - e^{-Ts}}{s}$, so the frequency response of the zero-order hold can be obtained as $G_{h0}(j\omega) = T\frac{\sin(\pi\omega / \omega_s)}{\pi\omega / \omega_s} e^{-j(\pi\omega/\omega_s)}$, and the bode diagram in frequency domain is shown in Figure 3.3.

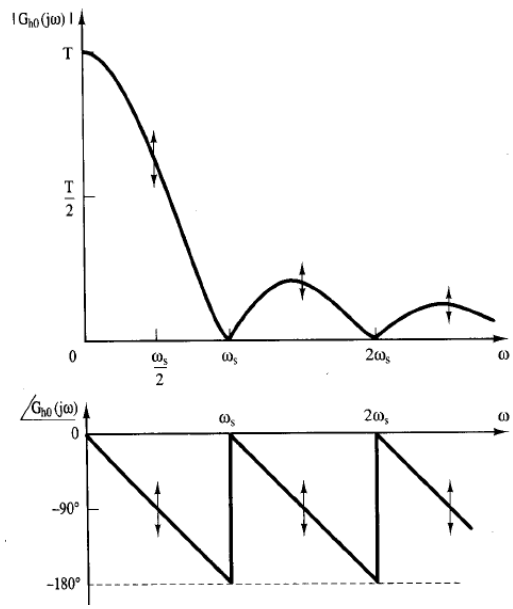


Figure 3.3 Frequency responses bode diagram [4]

According to the Shannon sampling theorem, when the input signal is reconstructed, any frequencies $\omega > \omega_s / 2$ will reflect into the frequency range $0 < \omega < \omega_s / 2$. This effect is called frequency aliasing. The frequency aliasing can be prevented either by increasing ω_s or by placing an analog antialiasing filter in front of the sampler. The antialiasing filter is a low pass filter that removes any frequency components in $e(t)$ that is greater than $\omega_s / 2$, since the low pass filters introduce phase lag. However, the cutoff freuqency of the antialiasing filter cannot be made so low as to destablilize the control system.

From the phase plot of zero-order hold, we can see that the zero-order hold introduces the phase lag into the system. When the bandwidth of the system is equal to the sampling frequency, the phase delay goes to 180^0. Generally, in order to make the phase delay of the zero-order hold

as small as possible, the sampling frequency should be greater than the system bandwidth by at least 10 times, which means the phase delay goes to $\omega_s / 10 = 18^0$.

3.2 Digital Compensator Design

The analog controller design procedure generally includes following steps:

- Develop an average small-signal model of a switching converter at the quiescent operating points.
- Solve the uncompensated loop gain $T_H(s)$.
- Design the compensator to shape $T(s)$ in frequency domain to achieve the desired stability margin and performance.

For the buck converter closed-loop system shown in Figure 3.4, the loop gain is

$$T(s) = \frac{H(s)G_c(s)G_{vd}(s)}{V_M} \tag{3-2}$$

Analog controller design has many benefits. The analog large- and small-signal models of the system blocks are readily available and well understood. The design can be completely implemented in frequency domain.

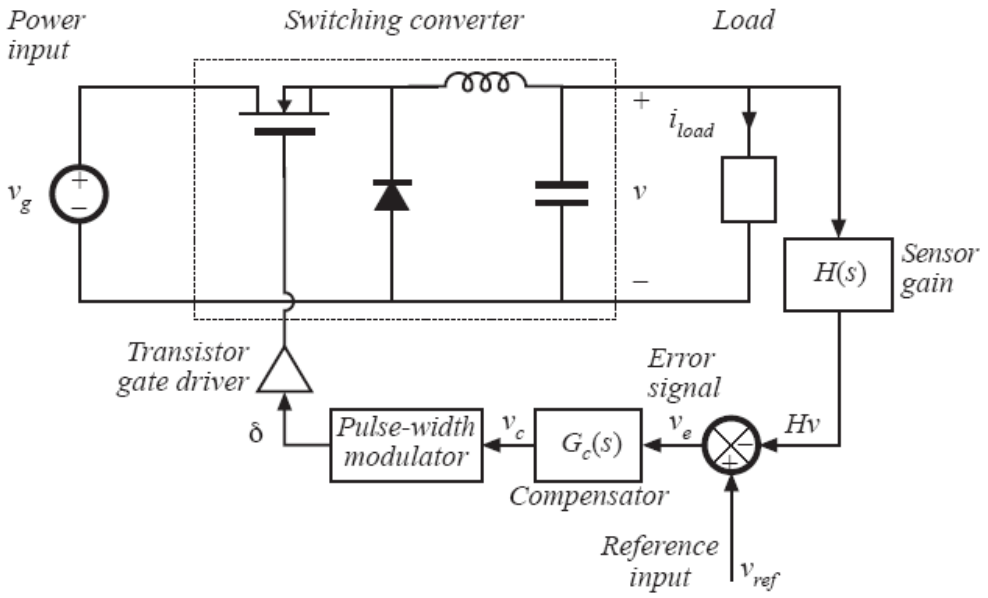


Figure 3.4 Buck converter closed-loop system [9]

Compared with analog controller, the digital controller shown in Figure 3.5 consists of AD, digital compensator and PWM. The output signal is sensed and sampled by AD and is compared with the reference signal and generate an error signal. The digital compensator generates the duty cycle control signal according to the input error signal and feeds the control signals into PWM to get the drive signal to power stage.

For the digital controller design, generally there is two design methods: Digital redesign approach and direct digital design approach. Digital redesign assumes the sampling frequency is much greater than the system crossover frequency, so the design equivalent approach is accurate. This approach first models the discrete components as analog components approximately, and then designs the analog controller with standard analog control technique. Finally, it maps the analog compensator into digital with some equivalent mapping methods.

For direct design approach, first a discrete model of sampled analog components is modeled. Then, the compensator design is directly in Z-domain including the accurate models of sampling functions. In the direct design, the frequency response techniques, like gain margin and phase margin, can be used also.

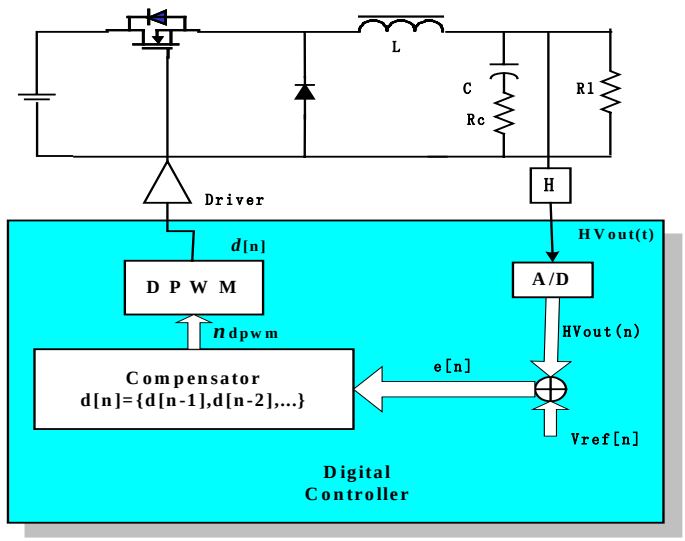


Figure3.5 Digital controller

Taking the buck converter shown in Figure 3.5 as an example, we start redesign with the small-signal model of the buck converter in Equation 3-3. With specified parameters, the bode diagram of the model is shown in Figure 3.6.

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \left(\frac{V_o}{D}\right)\left[\frac{1+sR_CC}{1+s\left(R_CC+[R//R_L]C+\frac{L}{R+R_L}\right)+s^2LC\left(\frac{R+R_C}{R+R_L}\right)}\right] \tag{3-3}$$

Assuming the feedback gain is unit, bode plot of the power stage is the same as loop gain and it indicates that this system has a very small phase margin. A compensator must be designed to ensure that the gain at low frequencies is high enough to minimize the steady-state error and that the crossover frequency is as high as possible under stability condition with enough phase margin and gain margin. The phase margin of the compensated system should be in the range of 45° to 60° to meet the transient response requirements.

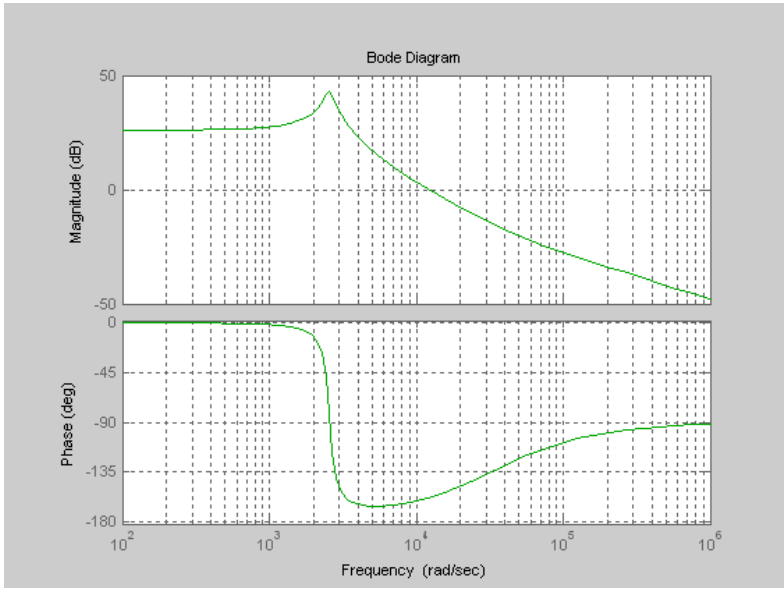


Figure 3.6 Bode plot of the buck converter

The compensator is a PID controller, which is described by the following transfer function:

$$G_C(s) = K_P + \frac{K_I}{s} + K_D s \tag{3-4}$$

where K_P is the proportional coefficient, K_I is the integral coefficient and K_D is the derivative coefficient. This PID controller has one pole and two zeros. The PID controller was designed in the continuous time domain and then converted to the discrete time domain using bilinear mapping method. The frequency response of the compensator in continues time domain and discrete time domain are shown in figure 3.7. The figure indicates that the two frequency responses are very similar except for the region close to the sampling frequency. Generally, the bandwidth of the system is much less than sampling frequency, so the error around the sampling frequency can be ignored.

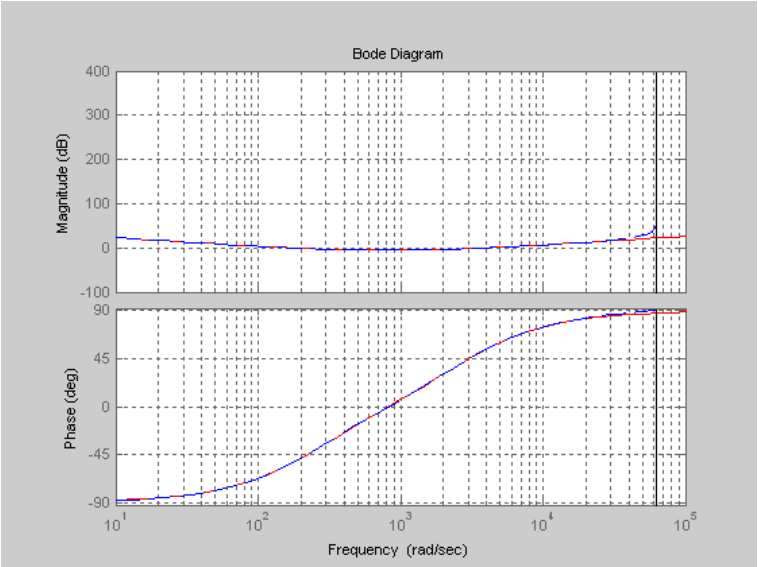


Figure 3.7 Compensator frequency responses of continuous-time (red) and discrete-time (blue)

Regarding the discretization methods, there are several methods listed in Table 3.1. The different discretization methods have advantages and disadvantages respectively, which are not going to be discussed in this thesis.

Converting the PID controller in the continuous s-domain to the discrete z-domain using the backward integration method (Euler rule), the following difference equation can be derived from the discrete time transfer function [5].

$$U(k) = K_P e(k) + K_I T \sum_{i=0}^{k} e(i) + \frac{K_D}{T}[e(k) - e(k-1)] \tag{3-5}$$

where, u(k) is the new duty cycle calculated from the kth sample, and e(k) is the error of the kth sample. The error e(k) is calculated as e(k) = Ref-ADC(k), where ADC(k) is the converted digital value of the kth sample, and Ref is the digital value corresponding to the desired output voltage. The second term in the equation is the sum of the errors and e(k)-e(k-1) is the difference between the error of the kth sample and the error of the (k-1)th sample [13].

Transformation Method	s-Domain	z-Domain
Backward Euler	s	$\frac{1-z^{-1}}{T_s}$
Bilinear	s	$\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$
Step Invariant	$G_c(s)$	$Z(\frac{1-e^{-T_s s}}{s}G_c(s))$
Pole/Zero Match	$s+a$	$1-z^{-1}e^{-aT_s}$
	$s+a\pm jb$	$1-2z^{-1}e^{-aT_s}\cos bT_s + z^{-2}e^{-2aT_s}$

Figure 3.8 Transfer methods from s-domain to z-domain

The closed-loop bode diagram is shown in Figure 3.9. With PID compensator, the close loop phase margin is improved up to 50 degree. The red line is the curve of continuous-time PID and the green line is the discrete-time PID compensator.

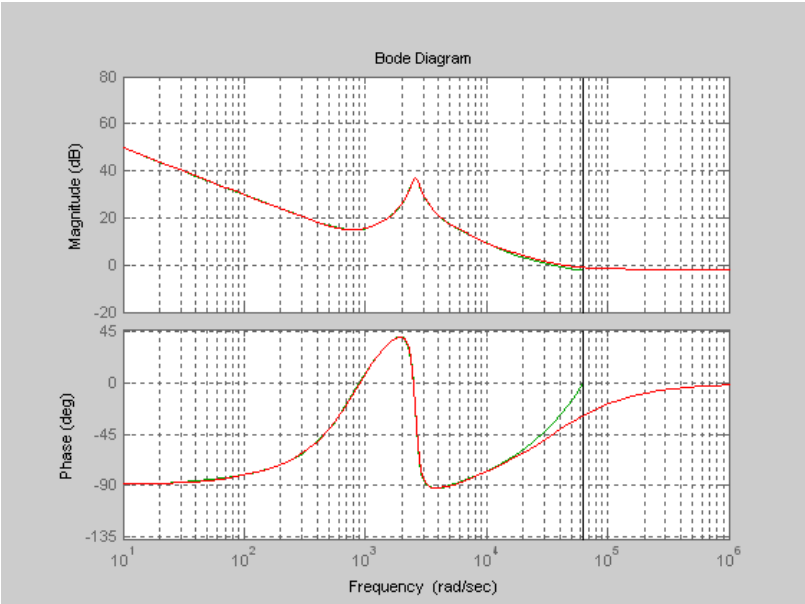


Figure 3.9 Closed-loop bode diagram

3.3 Digital Controller Design Issues

For the digital controller, the sensitivity of the ADC converter, inherent time delay of the calculation/sampling and the precision of the numerical value degrade the performance of the system. Therefore, some practical issues should be considered when designing a digital controller, including:

- ADC sampling frequency and resolution.
- PWM resolution.

- Computational delay time.
- Quantization/word length effects and calculation precision.

3.3.1 ADC Requirement

For the ADC of a digital system, generally, the dynamic voltage regulation requires that output voltage Vo must always follow reference voltage Vref during load or input voltage transients. As matter of fact, only a small window around Vref is needed to sample. Therefore, ADC converter can be used to sample the error signal instead of output voltage and the resolution can be improved and less bits of ADC converter is required [5]-[7][10].

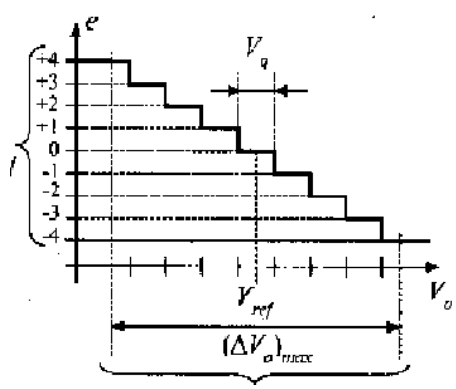


Figure 3.10. A/D conversion characteristic [10]

Figure 3.10 shows the A/D conversion characteristic, which indicates that the output voltage is sampled by an A/D converter and produces the digital error signal. Vq is the smallest difference corresponding to the least level of A/D analog equivalent voltage difference of LSB. In order to meet the requirement that A/D can sense the smallest change of the output voltage,

the Vq should not be greater than the smallest change of output, which means $V_q < \Delta V_o$. So the smallest output change that can be distinguished determinates the resolution of ADC.

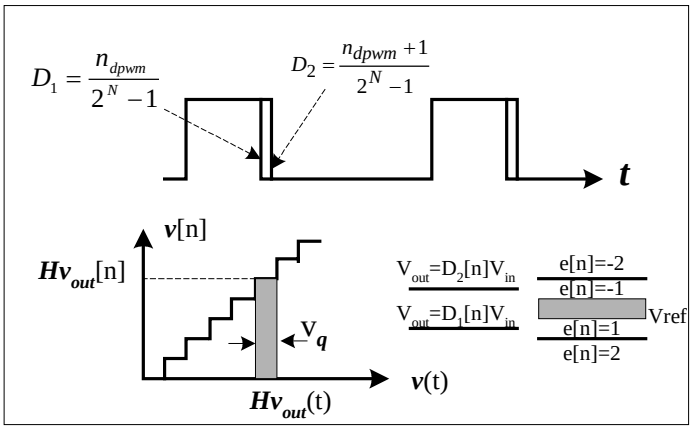


Figure 3.11 Resolution requirement of the DPWM [10]

Another important issue for ADC is to determine the sampling frequency. Theoretically, higher the sampling frequency is better for the system due to less time delay. However, in practice, the cost of hardware implementation and the calculation capability have to be considered. In the discussion of the zero-order hold in the early chapter, we recognize that a sampling frequency must be two times greater than the bandwidth of the system to reconstruct the input without errors. Even at this case, the zero-order hold still introduces significant phase lag into the system. Generally, in order to make the phase delay as small as possible, we pick up the sampling frequency at least 10 times greater than the system bandwidth, which means the phase delay goes to $w_s / 10 = 18^0$. For a switching power system, one option is to sample at the switching frequency [4].

3.3.2 DPWM Requirement

In a digital controller, a DPWM acts as a DA conversion, which is used to generate pulse width for a switch. Obviously, the minimal time increment of duty ratio depends on N, which is the resolution of DPWM. Because the discrete change of duty ratio causes the discrete change of output voltage, if the smallest change of V_{out} caused by the discrete change of duty cycle is greater than the smallest difference of V_{out}, AD can be distinguished. This means the DPWM resolution is too low, and in this case, a so-called limit cycle can occur. The basic requirement of the DPWM is that the resolution of DPWM should be greater than the resolution of ADC [5][6][7][10].

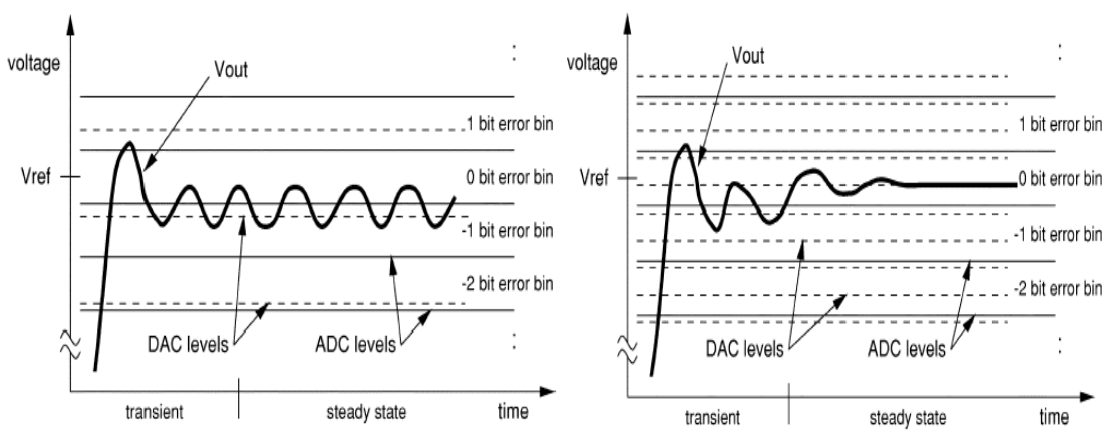


Figure 3.12 “Limit cycle” happens when the resolution of the DPWM is too coarse

3.3.3 Quantization and Finite Word Effect

In a practical implementation, the digital controller is implemented with the hardware, so the values of signal variables and filter coefficients are restricted to a finite set of discrete magnitude values, which is called quantization or finite word effect. The quantization and finite word length in the controller require consideration in following areas [4].

Fixed-point numbers could cause round-off or truncation errors for the coefficients of the calculation, which can be modeled as the worst case bound or random noise input. Those round-off effects also can be reduced by choosing a suitable filter structure, since different filter structures have different sensitivity for the given coefficients. Furthermore, coefficient round off can perform differentiation to derive sensitivity equations for poles and zeros to coefficients variations.

Overflow has been shown to impose disastrous consequences on the digital filter so the overflow oscillations must be avoided. By scaling the input to the filter so that only small signal levels exist in the filter, the overflow can be avoided. Or a digital filter structure, which is free of overflow oscillation, can be used [4].

3.4 Modeling and Simulation of Digital Controller with an 8-bits Microprocessor

In the early chapters, we discussed how to design a digital compensator based on the given specifications of power stage theoretically and the critical issues for a digital controller in the practice. In this chapter, we investigate the modeling and simulation of a DC-DC converter controlled by an 8-bit microcontroller, and many of these critical issues have been modeled using Matlab/Simulink [12].

The figure 3.13 shows the closed-loop system of a buck converter with an 8-bit digital controller, which includes the ADC, digital compensator and DPWM simulation models with quantization effect respectively.

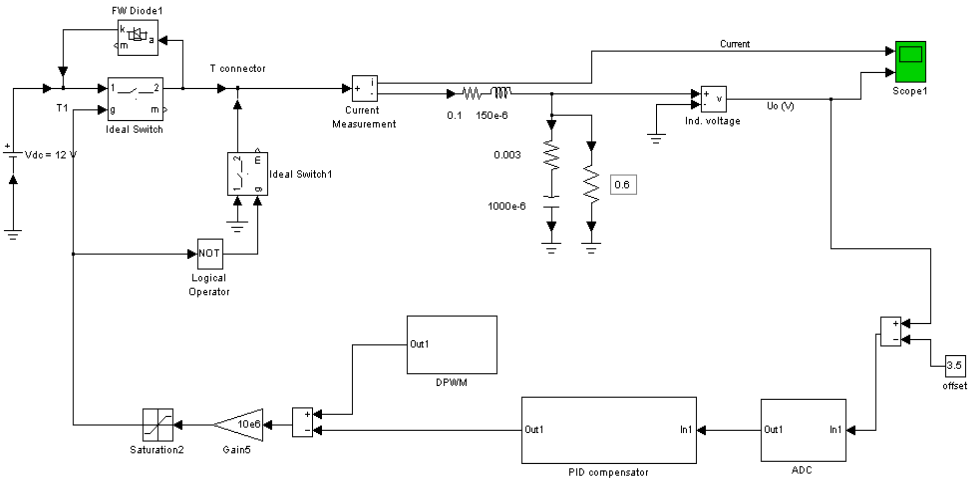


Figure 3.13: The close loop of buck converter with an 8-bit digital controller

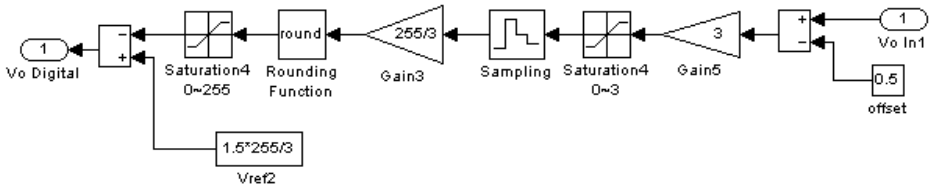


Figure 3.14: ADC simulation model with quantization effect

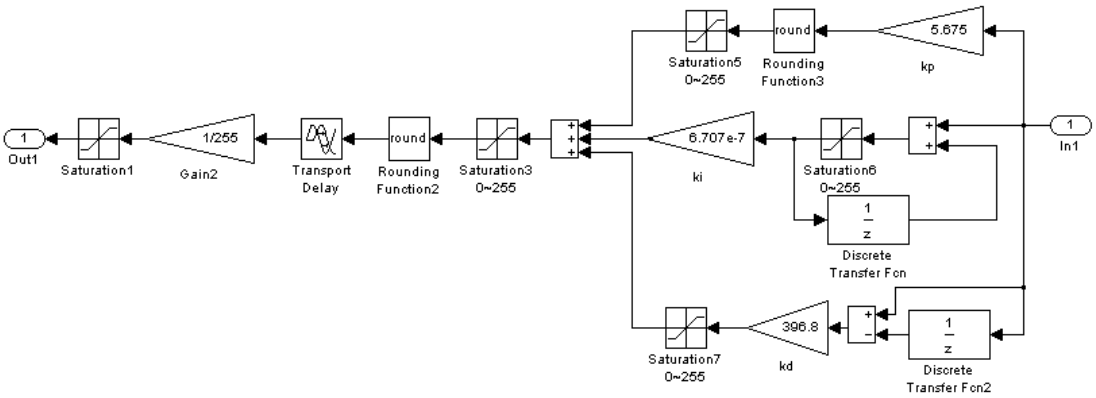


Figure 3.15: 8-bits digital compensator simulation models with quantization effect

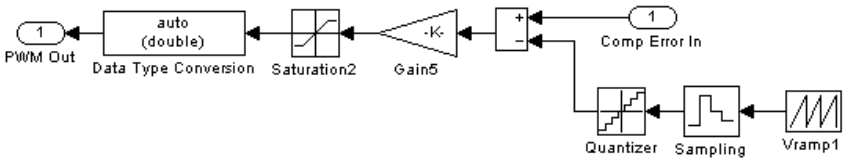


Figure 3.16: DPWM simulation model with quantization effect

The objective of this model is to include non-ideal effects such as ADC conversion range, time delay, calculation delay, quantization and numerical precision. The digital controller is basically a PID compensator, which is designed by the procedures mentioned in the chapter 3.2. In order to simulate the non-ideal effects, some delay blocks and limiter blocks are added. Note the limiters in both the proportional and integral paths of the controller, which impose bounds on the intermediate numerical calculations similar to that in the actual software. Since the microcontroller is 8-bits, the duty cycle, which is the output of the block, must be limited to between 0-255. It is rounded up to the nearest integer and then converted to a number between 0-1. Figure 3-17 through Figure 3-21 show the simulation results.

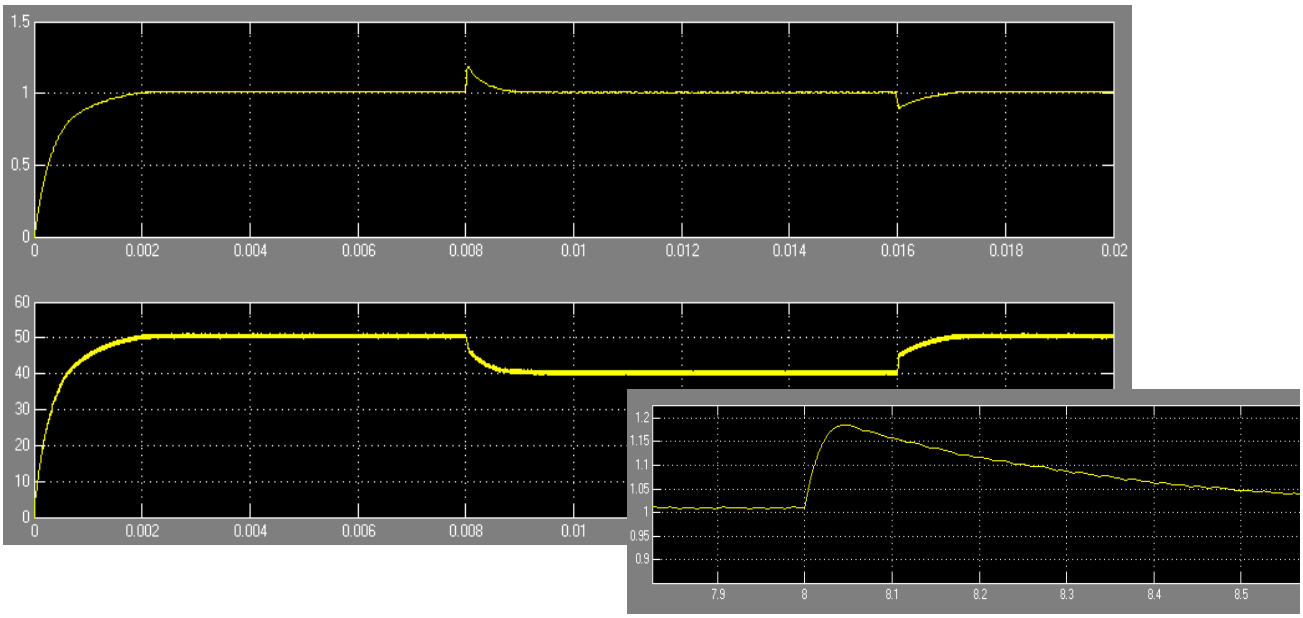


Figure 3.17: Output voltage and inductor current with a step-changed load in the ideal simulation case without the resolution issues and quantization effects

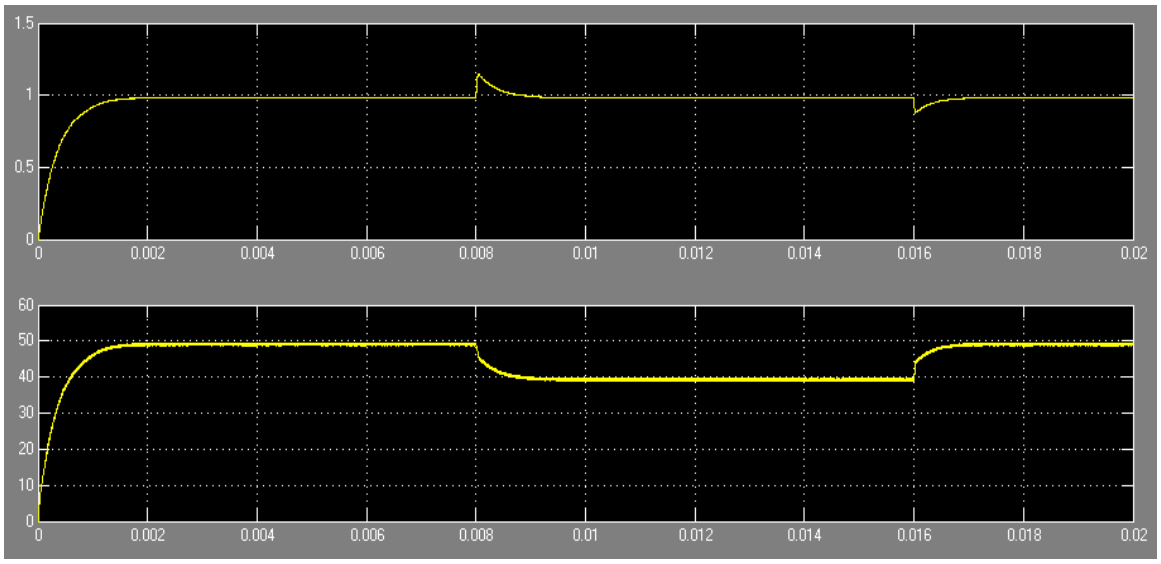


Figure 3.18: The sampling frequency of ADC is twice that of the switching frequency; the speed of transient response is increased and without any effects on the steady state because the bandwidth of the system is low

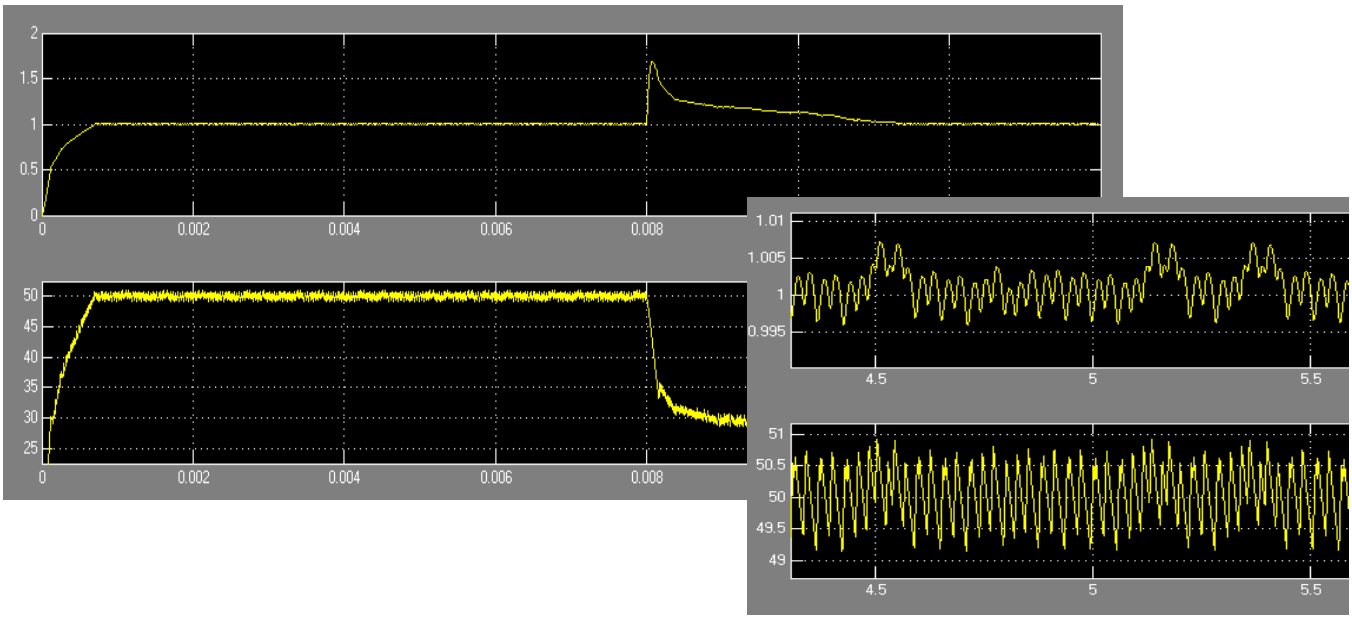


Figure 3.19; Resolution issues of ADC and DPWM result in limit cycles

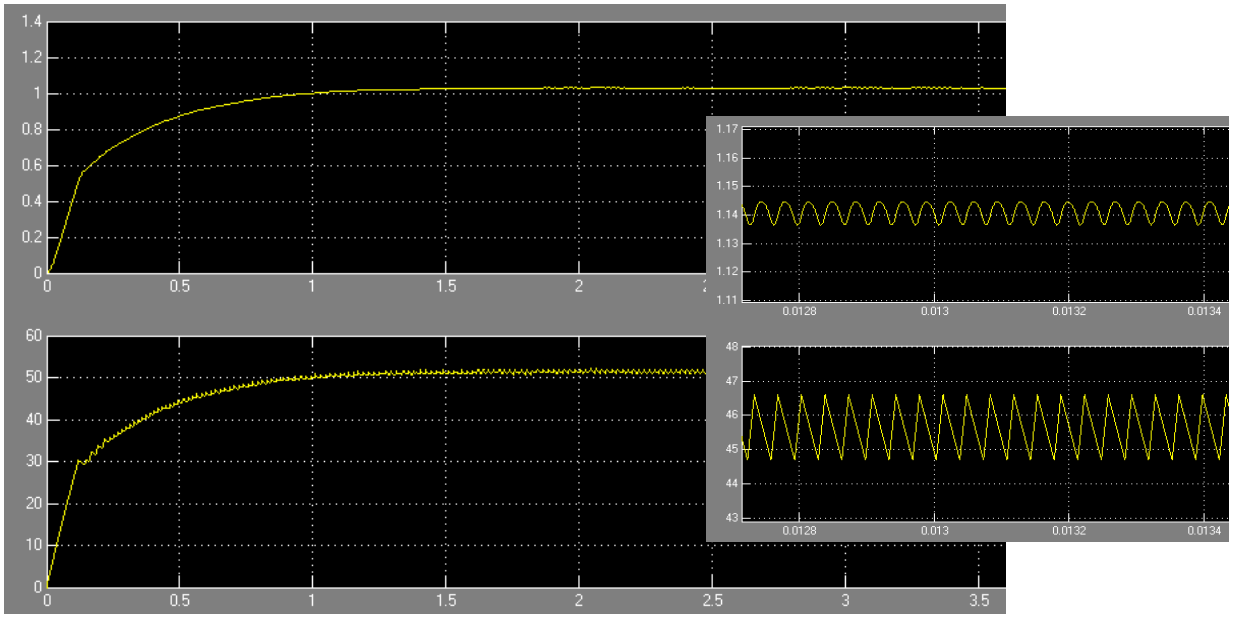


Figure 3.20: Simulation results with non-ideal ADC and DPWM

(resolution of ADC: 8 bits; resolution of DPWM: 12 bits)

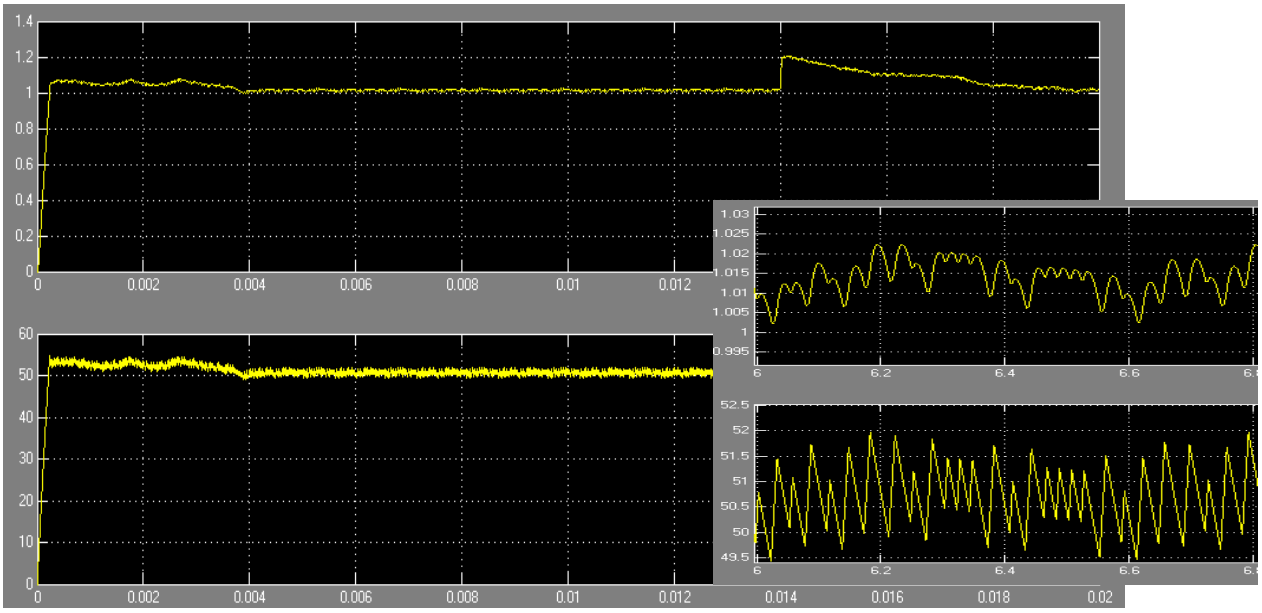


Figure 3.21: Simulation results based on the 8-bits PID controller with finite precision effects including finite word length, round off and quantization effect

From the simulation platform, we can summarize the following conclusion based on the above results and waveforms:

- A digital simulation platform is established and provides the platform to try an advanced control algorithm and more practical issues.
- The offset circuit increases ADC resolution resulting in smaller steady-state error. In addition, reducing the resolution increases the magnitude of the limit cycles.
- The simulation results are not affected by the delay within one switching cycle, but lower sampling frequency degrades transient response due to the sampling delay.
- If the resolution of DPWM is smaller than ADC, limit cycle occurs.

- Quantization and finite word length effects will cause the limit cycles and also result in larger steady-state error.

CHAPTER FOUR: DSP IMPLEMETATION FOR DIGITAL CONTROLLERS

Power electronics systems are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics. Real-time power electronics systems, therefore, demand the use of high-speed data acquisition and control. DSPs (Digital Signal Processors) meet the processing requirements posed by such systems. DSPs are used in multiple applications in power electronics including AC motor drives, high-frequency converter control, motion control, robotics and real-time testing and monitoring.

4.1 Introduction of DSPs

Because of the DSP's special architecture, it is more useful than a general-purpose microprocessor for the high-speed processing applications and real-time systems such as control system. DSPs are built with Harvard architecture, and this configuration employs separate program and data buses [14]-[17]. The benefit of this arrangement is the increased speed because instructions and data can move in parallel instead of sequentially. DSPs, like many advanced microprocessors, use pipelining to operate on several instructions simultaneously.

1) Hard-Wired Logic: In DSPs, most instructions execute in one machine cycle because all functions are performed internally in hard-wired logic. Hardware multipliers in DSPs perform multiplication in a single cycle.

2) Scaling: Hardware shifters allow the scaling of data used in computations. This helps prevent overflows and keep the required precision.

3) Saturation: In DSPs, the accumulator handles overflow by saturating to the most positive or least negative value, thus eliminating rolling over.

4) Word Length: Some DSPs support a large word length, thus reducing the quantization error. They also support a larger intermediate word length for intermediate computational results.

5) Other Features: Many DSP chips include input/output (I/O) functionality, timing circuitry, direct memory access (DMA) controllers and high-speed memories on-chip.

DSPs resemble reduced instruction set computers (RISCs), in that a small set of frequently used instructions are optimized for numerical processing at the expense of less frequently used general-purpose operations. DSP instruction sets efficiently handle mathematical operations common to many algorithms that are repeatedly executed in time-critical loops. For example, digital filters, which are often used in signal processing and control applications, are implemented using recursive difference equations of the form:

$$y(n) = \sum_{i=0}^{N} a(i)x(n-i) + \sum_{j=1}^{M} b(j)y(n-j) \tag{4-1}$$

The equation states that any output can be computed as a weighted sum of the input at the present time, past inputs and past outputs. Each step in this computation involves a multiplication and addition. The multiply and accumulate (MAC) instruction in DSPs performs this in a single instruction cycle. In contrast, in a typical fixed-point microprocessor, a “multiply” and “add” typically executes in 15 to 20 machine cycles. MAC is the one instruction that most distinguishes DSPs from other micros.

DSPs also significantly increase execution speed by performing multiple operations in parallel. For instance, in the same instruction cycle that a MAC operation is being performed, a

parallel data move can be carried out. Thus, the special DSP instructions supplement the computational speed of DSPs and make them ideal for high-performance real-time applications.

4.2 Architecture of TI C2000 and TMS320F2812

TI has developed the DSP solutions that are driving digital control by providing the industry's high performing and code efficient DSPs. The TMS320C2000 family of DSP controllers set the standard for performance and peripheral integration by offering a unique combination of on-chip peripherals such as flash memory, ultra-fast A/D converters, PWM modules and robust CAN modules.

TMS320C2812 is a member of the TMS320C28x DSP generation, which is a highly integrated, high-performance solution for demanding control applications [16]-[17]. These devices are based on a 32-bits DSP core delivering 150 MIPS of performance on a flash process and an impressive 32x32bit MAC in a single 6.67ns cycle. These DSPs also uniquely feature a large amount of fast-access on-chip flash memory so that code can be executed internally without adding costly external flash memories. Furthermore, these devices incorporate a high-precision ultra-fast ADC together with many control and communication peripherals for truly single-chip designs. Figure 4.1 is the architecture of the TMS320C2812.

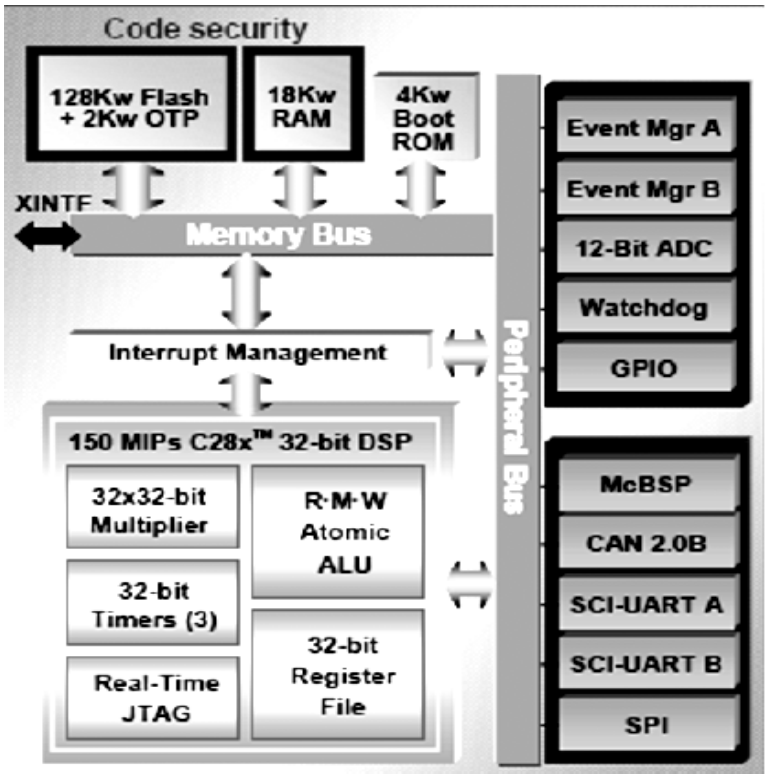


Figure 4.1: Architecture of TMS320C2812

Due to its architecture, which is specially optimized for C/C++, these devices offer good code efficiency, and give customers the ability to develop their algorithms entirely in high-level languages. Further, these devices uniquely enable customers to develop their code in virtual floating point via the IQ math capability.

The TMS320C2812 supports multiple bus architecture, whose memory bus architecture contains a program read bus, and data read bus and data write bus. The 32-bit-wide data busses enable single cycle 32-bit operations. The F281x and C281x implement the standard IEEE 1149.1 JTAG interface. Additionally, the TMS320C2812 supports the real-time JTAG mode of operation including the contents of memory, peripheral and register locations; that is to say, the

real time analysis is allowed. It contains 128K x 16 of embedded Flash memory and 128K x 16 of ROM, and two blocks of single access memory, each 1K x 16 in size. The TMS320C2812 supports the 32-bits CPU timers and several serial communication peripherals including CAN, McBSP, SPI and SCI. Further, it supports the event managers and ADC as peripherals, which are used for embedded control and communication.

4.3 PWM Generators and ADC of TMS320F2812

With digital power applications, ADC and PWM modules are the most important peripheral devices inside the DSPs. TMS320F2812 provides high performance ADC and PWM generators and makes it possible to meet the high requirement of DC-DC converters.

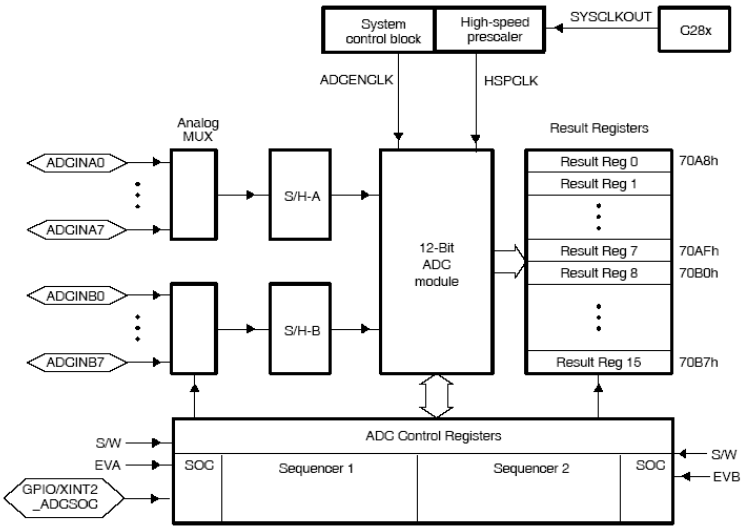


Figure 4.2: Structure of ADC in TMS320F2812

The ADC of TMS320F2812 provides 12-bit core with built-in dual sample-and-hold (S/H), simultaneous sampling or sequential sampling modes, very fast conversion time (running at 25 MHz), ADC clock, or 12.5 MSPS, and 16-channel, multiplexed inputs and 16 result registers to store conversion values. The sequencer of ADC can be operated as two independent 8-state sequencers or as one large 16-state sequencer. The ADC interrupts can be triggered by multiple sources for the start-of-conversion (SOC) sequence, such as S/W — software immediate start, event manager A/B or the external pins.

The PWM modules of TMS320F2812 are designed to generate pulse width modulated waveforms used in motor control and motion control applications. The PWM waveform generation capability of each event manager module (A and B) is summarized as follows.

There are five independent PWM outputs — three of which are generated by the compare units, while the other two are generated by the GP timer compares — plus three additional PWM outputs, dependent on the three compare unit PWM outputs. TMS320F2812 provides programmable dead-band for the PWM output pairs, and the minimum dead-band duration of one device clock cycle (6.67ns). The minimum PWM pulse width and pulse width increment/decrement is one clock cycle. The PWM supports 16-bit maximum PWM resolution and programmable generation of asymmetric, symmetric and space vector PWM waveforms. Figure 4.3 is an example of generating the PWM waveform with the controlled dead time based on the given PWM period and initial values.

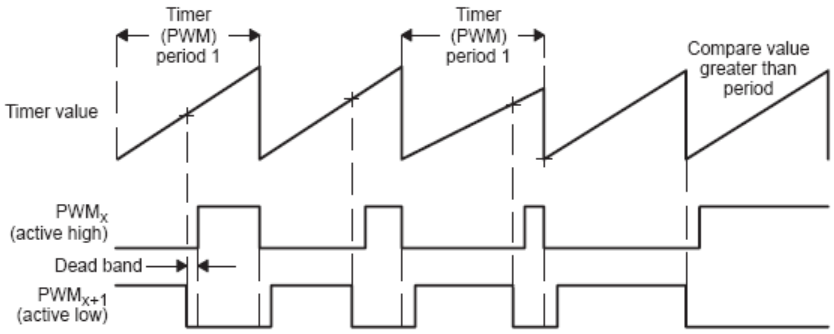


Figure 4.3: Generating the PWM waveform in TMS320F2812

4.4 Controller Implementation with TMS320F2812

4.4.1 ADC Implementation

The ADC of TMS320F2812 could be triggered by the software, EVA/B or the external pins. In our DSP platform, we set up the ADC triggered by the Event Timer A, whose frequency is suppose to be equal to the sampling frequency of ADC, since the SOC (start of conversion) of ADC is designed to be triggered by the underflow of the timer ramp signal, as shown in Figure 4.4.

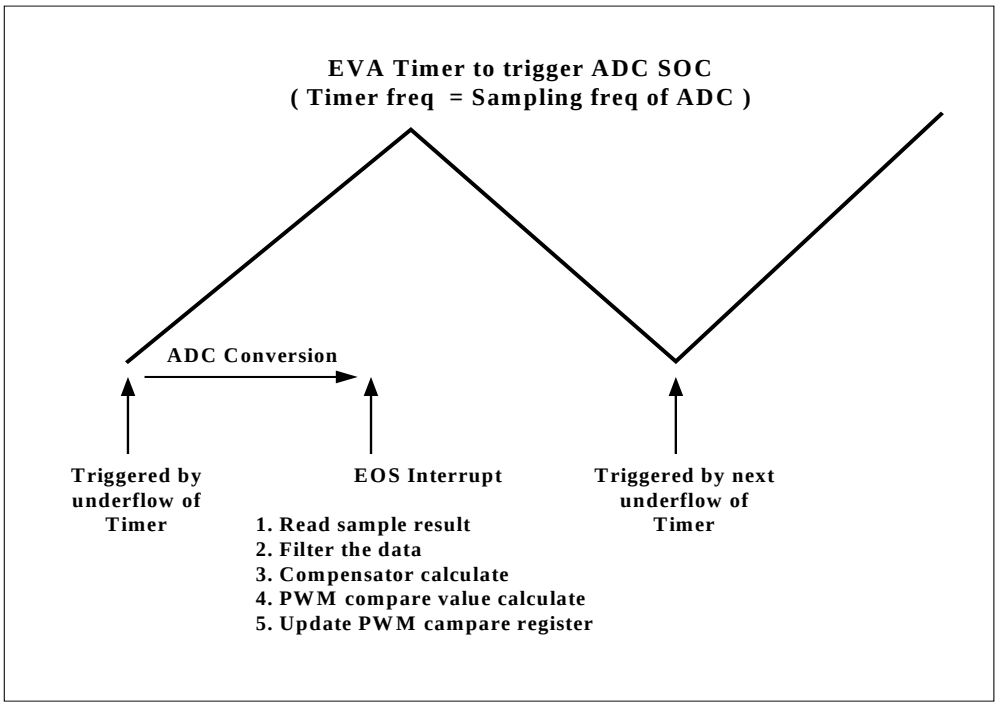


Figure 4.4: Set-up of ADC

The SOC is started by the Timer A, and once the conversion is finished, the EOC (end of conversion) interrupt is triggered, and then the ADC interrupt routine is called in the program. In ADC interrupt routine, DSP first reads the sample result from the ADC result registers and then processes the data, such as filtering or averaging the data. After that, DSP calculates the compensator and gets the result, which is supposed to be the new value of the duty cycle. Finally, the PWM modulated value is calculated in terms of the new duty cycle, and then the registers are updated before the next trigger of the ADC conversion.

The resolution of ADC in chip TMS320F2812 is 12 bits, which means the minimum value ADC can distinguish is around $\frac{1}{2^{12}-1} = 0.24\%$ of the input, which is small enough over the power system's precision requirement of 1%.

As mentioned in the early chapters, the sampling frequency should be greater than the bandwidth of the system by 10 to 20 times in order to reduce the sampling delay. In our experiment, the switching frequency is 400kHz, so we pick up the sampling frequency as 2MHz, which is sufficient for the system requirement.

4.4.2 PWM Implementation

The PWM modules of TMS320F2812 can set up the period register TxPR and configure register TxCON to initialize the frequency and configuration of PWM. To generate the gate driver signals for the DC-DC converter, the PWM frequency is designed to be equal to the switching frequency, which is 400kHz for our experiment case. As mentioned in Chapter 2, to avoid the limit cycle, the resolution PWM must be greater than the resolution of ADC. The PWM signal of TMS320F2812 has 16-bits resolution, while the resolution ADC is 12 bits. Therefore, TMS320F2812 provides the most reasonable resolution for the digital controller implementation.

The power stage we are using for the digital control investigation is the half-bridge DC-DC converter with a current doubler. There are two kinds of cases for the converter, which includes symmetrical and asymmetrical cases. For the symmetrical case, the gate signals of primary side have the same duty cycle ratio but with 180-degree phase shift, while for the asymmetrical case, the gate signals of the primary side are complimentary signals with dead time. Further, we should generate the complementary signals with controlled dead time for the secondary side signals. TMS320F2812 can provide the minimum increment of PWM signal or

the minimum dead time as one clock cycle 6.67ns, which is supposed to be sufficient for the HB converters requirement.

The figure 4.5 and 4.6 show how to generate the primary and secondary PWM signals with PWM generator of TMS320F2812. To get the accurate dead time and phase shift of the signals, we generate the signals based on the same timer, which is set up in Event Manager A. The symmetrical ramp signals are achieved by using Event Manager A timer in a PWM module. Using given duty cycle values from the compensator calculation, the four compare values are calculated to get responding values, and then the compare registers are set up respectively.

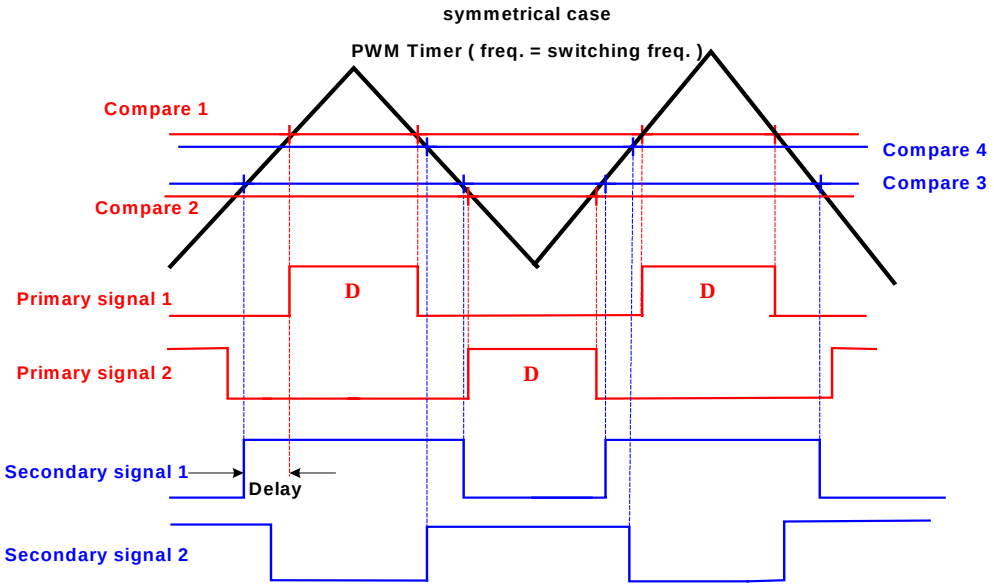


Figure 4.5: Symmetrical PWM signals generating

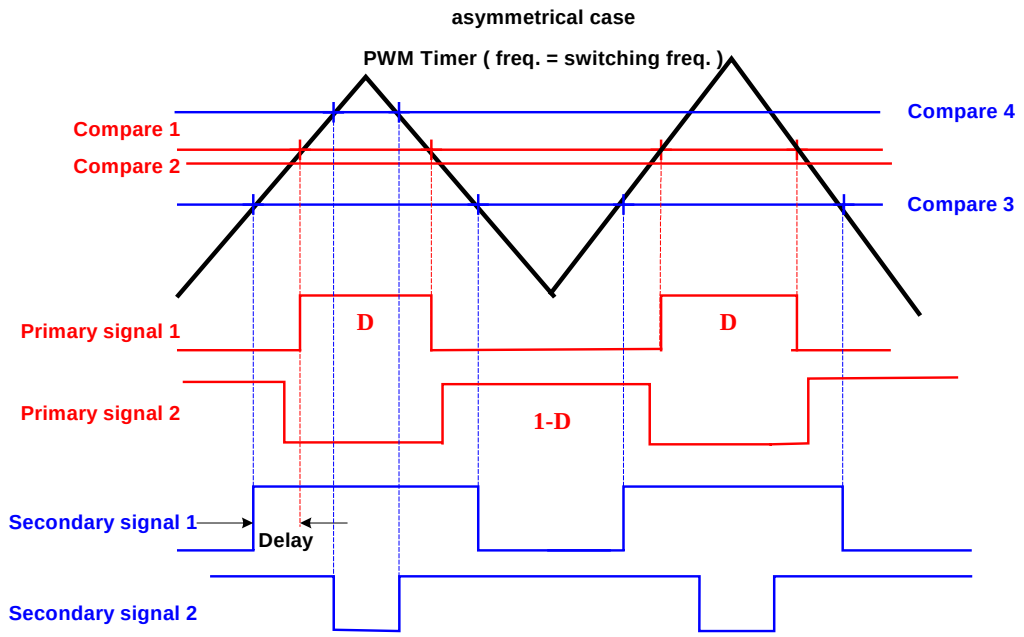


Figure 4.6: Asymmetrical PWM signals generating

PWM modules are designed to update the duty cycle every switching cycle, meaning that before the next switching cycle begins, the compare values are stored in the buffer and then are updated once the new switching cycle comes.

4.4.3 Controller Implementation

The specifications of a half-bridge converter with current doublers are as follows:

Vin=48V, n=6, Vo=1V, Io= 50A, fsw= 400kHz, Co=500 uF, Lo= 270 nH

With the small signal model we derived in Chapter 2, we can plot the "output to duty cycle" frequency response, which the compensator designed is based upon. We design the digital controller with redesign method, which means designing the analog controller first, based

on the specifications of power stage, and then transferring it to the digital controller. Using 2 Poles 2 Zeros Controller Transfer Function, we can get the analog controller transfer function:

fs=2e6Hz ts=1/fsSec c1=780e-12F c2=0.02e-6F c3=0.01e-6F R1=1000ohm R2=499ohm R3=39ohm

$$\omega_{z1} := \frac{1}{R_2 \cdot C_2} \quad \omega_{p1} := \frac{1}{R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \omega_{p2} := \frac{1}{R_3 \cdot C_3} \quad \omega_{z2} := \frac{1}{(R_1 + R_3) \cdot C_3} \quad G_o := \frac{1}{R_1 \cdot (C_1 + C_2)}$$

$$H_c(s) := G_o \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{s \cdot \left(\frac{s}{\omega_{p1}} + 1\right) \cdot \left(\frac{s}{\omega_{p2}} + 1\right)}$$

$$Hc = \frac{7.221 \times 10^{-7} s^2 + 0.9981 s + 9.276 \times 10^4}{1.461 \times 10^{-13} s^3 + 7.646 \times 10^{-7} s^2 + s}$$

Then with Bilinear method, the Z-transform of the controller is achieved.

$$Hc(z) = \frac{0.6113 z^3 - 0.2847 z^2 - 0.5968 z + 0.2992}{z^3 - 1.418 z^2 + 0.4619 z - 0.04364}$$

For practical reasons, we need the model order reduction for the digital controller, from three orders to second order, and then we transform it to the difference function:

D [n] =1.418 D [n-1] - 0.4619 D [n-2] +0.0436 D [n-3] +

0.6113 e[n] -0.2847e [n-1]-0.5968 e [n-2]+0.2992e[n-3]

Figure 4.7 is the frequency response of the compensator. The red curve is the continuous domain response, and the blue curve is the discrete domain response. Figure 4.8 shows frequency response of the converter, compensator and open loop

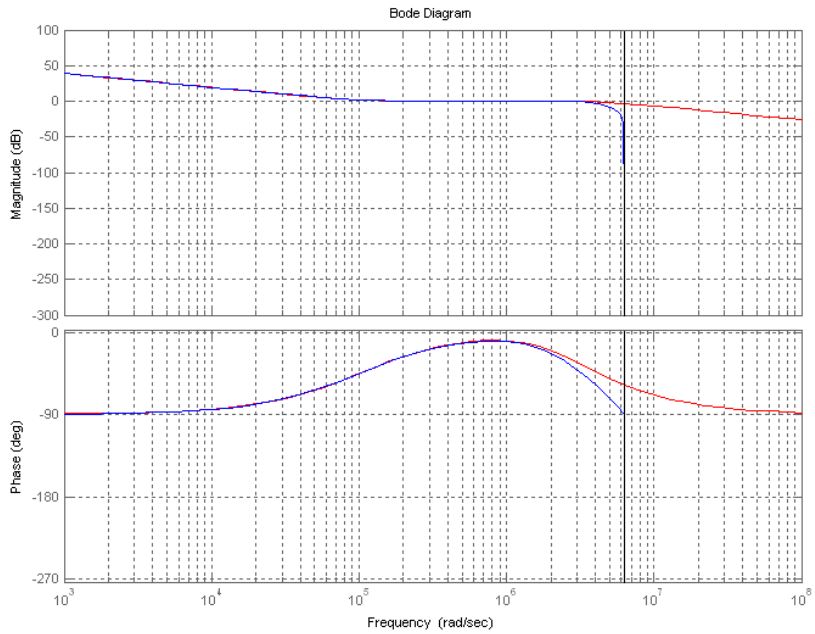


Figure 4.7: Frequency response of the compensator

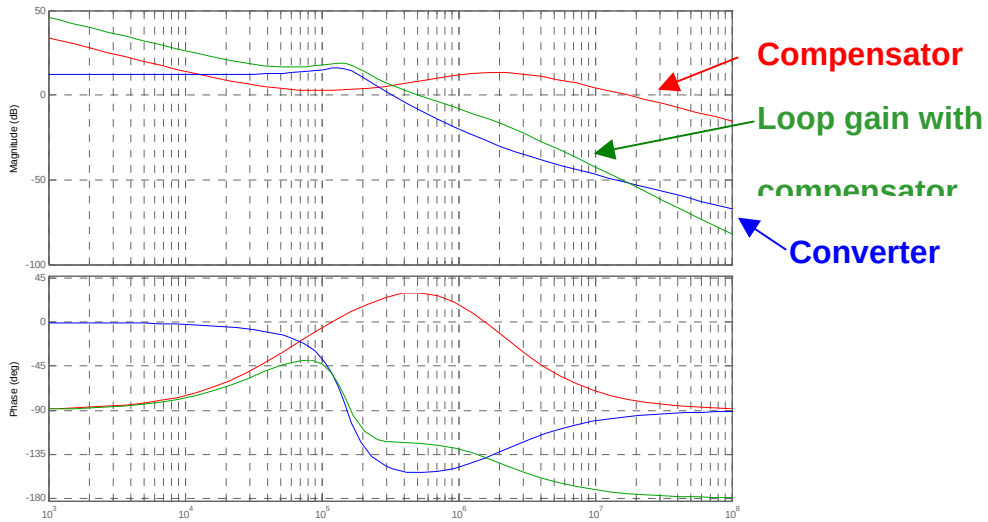


Figure 4.8: Frequency response of the converter, compensator and open loop

To achieve a controller suitable for the implementation, it is decided to limit the control law to the second-order equation. Based on the derived small signal model of HB converter in Chapter 2, we easily can get the “output to duty cycle” frequency response. The frequency response of the converter is not constant value, and it depends on the operating point.

The complete real-time controller implementation is interrupt driven. The PWM module loads the new value of the duty cycle at the beginning of every switching cycle. All calculations regarding the duty cycle are implemented in the ADC interrupt routine. Given the ADC sampling frequency of 1.4MHz, the interrupts are 700ns. Taking into account the interrupt response time, the time available for the processor to compute the new value of the duty cycle is about 700ns or 100 instructions. A flow chart of the controller implementation is shown in Figure 4-9.

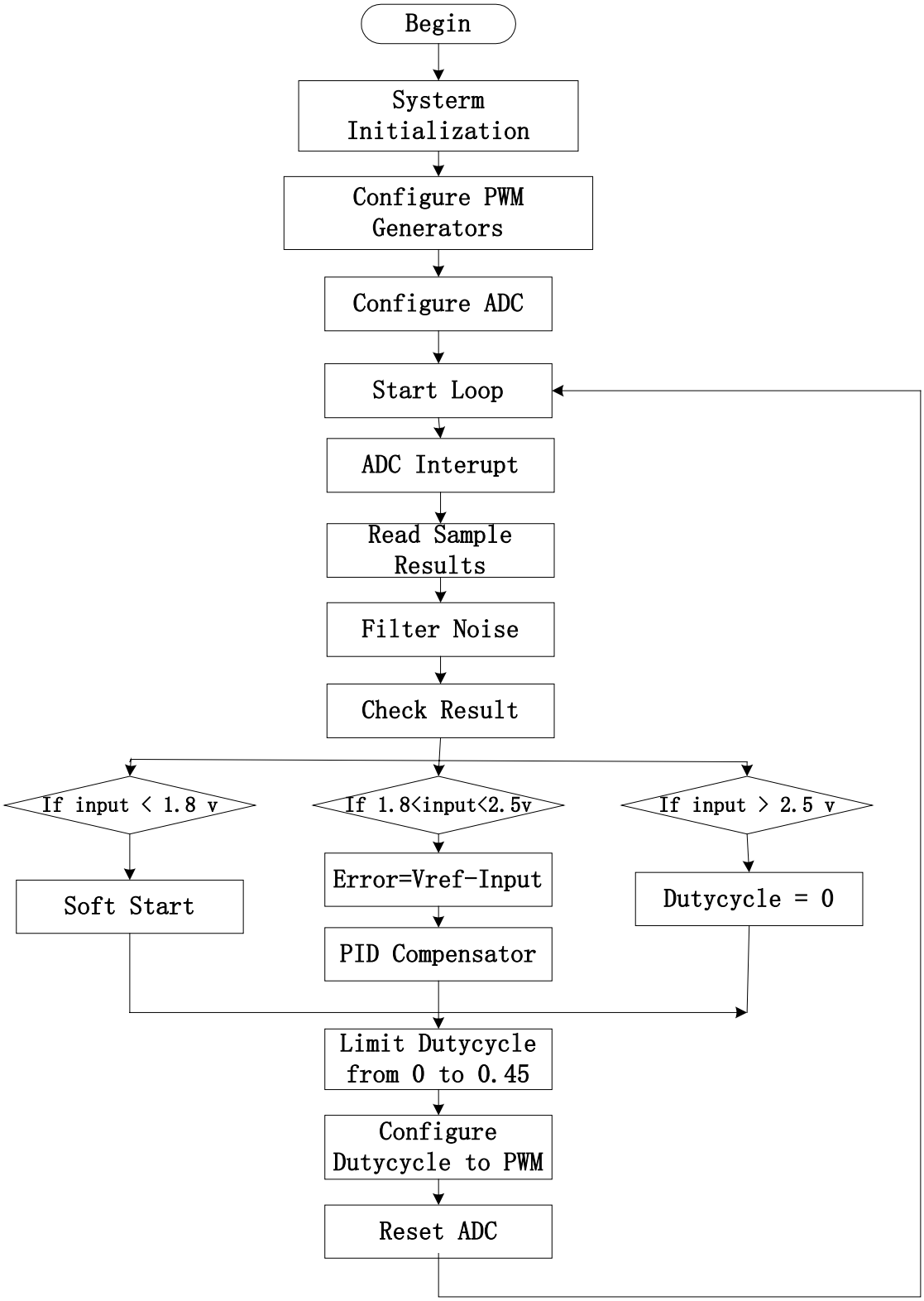


Figure 4.9: Flow chart of controller implementation in DSP

After the ADC interrupt is recognized, the latest sampled value of the output signal is read and pre-processed. If the output signal is less than 1.8 volt, soft starter module is called for to avoid the transient overshoot. If the signal is greater than 2.5 volts, the duty cycle is shut down. Otherwise, the signal is subtracted from the reference, and the new value of the error signal is formed. The error is fed into the PID calculation module, and then the new duty cycle value is generated. The duty cycle is limited from 0 to 0.45 as a protection objective, and at the end of the ADC interrupt, the ADC is reset to be ready for the start of the next conversion.

The PID calculation flow chart is shown in Figure 4.10:

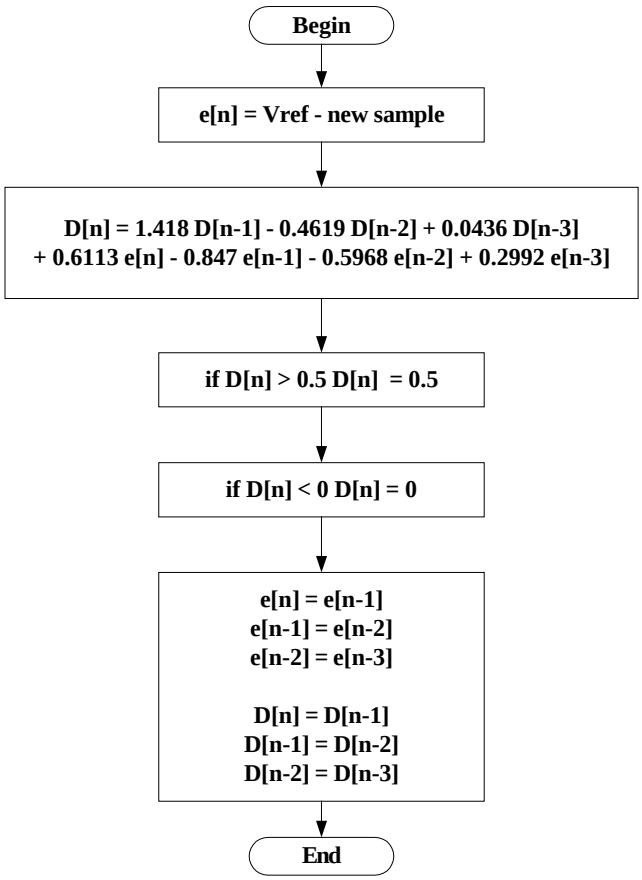


Figure 4.10: PID calculation flow chart

In the practical implementation of a controller in DSP, the following critical issues have to be considered:

- The input signals are sampled, and then the signal is filtered by a low-pass filter to reduce the noise. Since the bandwidth of the low-pass filter is going to affect the whole bandwidth of the loop, that bandwidth should be considered carefully.
- The soft start is used to avoid the transient overshoot when a system is started up. In the soft start module, the duty cycle is increased with a small step to avoid a sharp ascend of the output signal.
- The duty cycle is limited from 0 to 0.45 as a protection objective.

CHAPTER FIVE: TESTING RESULTS AND ANALYSIS

5.1 Experimental Results

The specifications of a DSP-controlled half-bridge DC-DC converter with a current doubler are as follows:

Vin=48V, n=6, Vo=1V, Io= 50A, fsw= 400kHz, Co=500 uF, Lo= 270 nH

Based on the small signal model of HB DC-DC converter and digital controller design theory, the digital controller is designed in chapter four as follows:

$$Hc(z) = \frac{0.6113z^3 - 0.2847z^2 - 0.5968z + 0.2992}{z^3 - 1.418z^2 + 0.4619z - 0.04364} \quad (5\text{-}1)$$

The corresponding difference equation is

D [n] =1.418 D [n-1] - 0.4619 D [n-2] +0.0436 D [n-3]

+0.6113 e[n] -0.2847e [n-1]-0.5968 e [n-2]+0.2992e[n-3]. (5-2)

The digital compensator is implemented with DSP program with C language and the flow chart is shown in chapter four. A 12 bits ADC with 80 ns conversion time is setup for the digital controller in TMS320F2812 DSP chip. And the PWM generator in the chip generates symmetrical, asymmetrical and DCS PWM signals for the power stage.

Figure 5.1 shows the primary and secondary gate signals with 100ns dead time in a symmetrical case, which is generated by DSP chip, TMA320F2812. The two primary signals have the same duty cyle with a 180-degree phase shift, and the secondary signals are the

complementary signals of the primary signals with a controller dead time. In Figure 5.2, the asymmetrical primary-side gate signals are shown with 100ns dead time. Actually, the deadtime mentioned above is adjustable with the program.

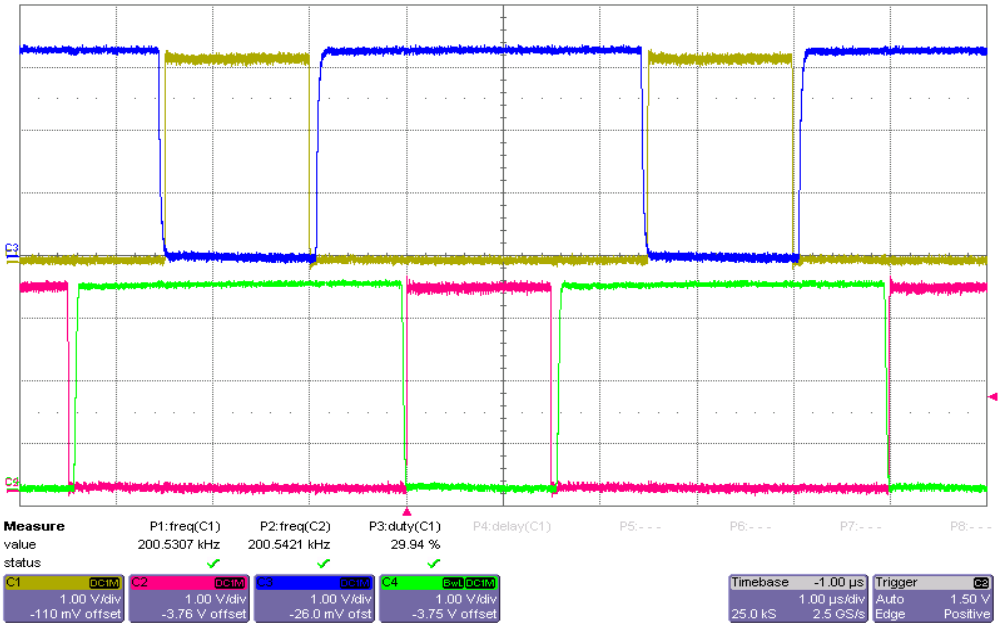


Figure 5.1: The primary and secondary gate signals with 100ns dead time in a symmetrical case

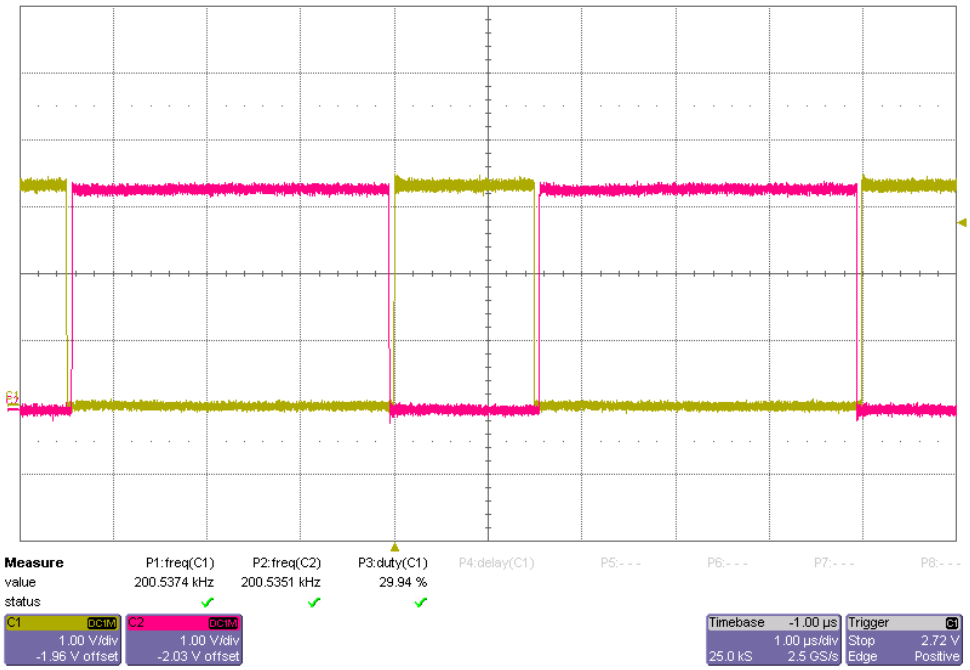


Figure 5.2: The gate signals with 100ns dead time in an asymmetrical case, the signals are complementary signals with controlled dead time.

Figure 5.3 shows the primary signals with 100ns dead time in a DCS (Duty Cycle Shift) case. DCS control technology is used to reduce primary ringing of the signals [3]. In a DCS case, the two primary signals have the same duty cycle but with a fixed dead time, which is independent of the duty cycle and SR dead time. Figure 5.4 shows the output voltage with the significant noise and in this case the output is hard to regulate.

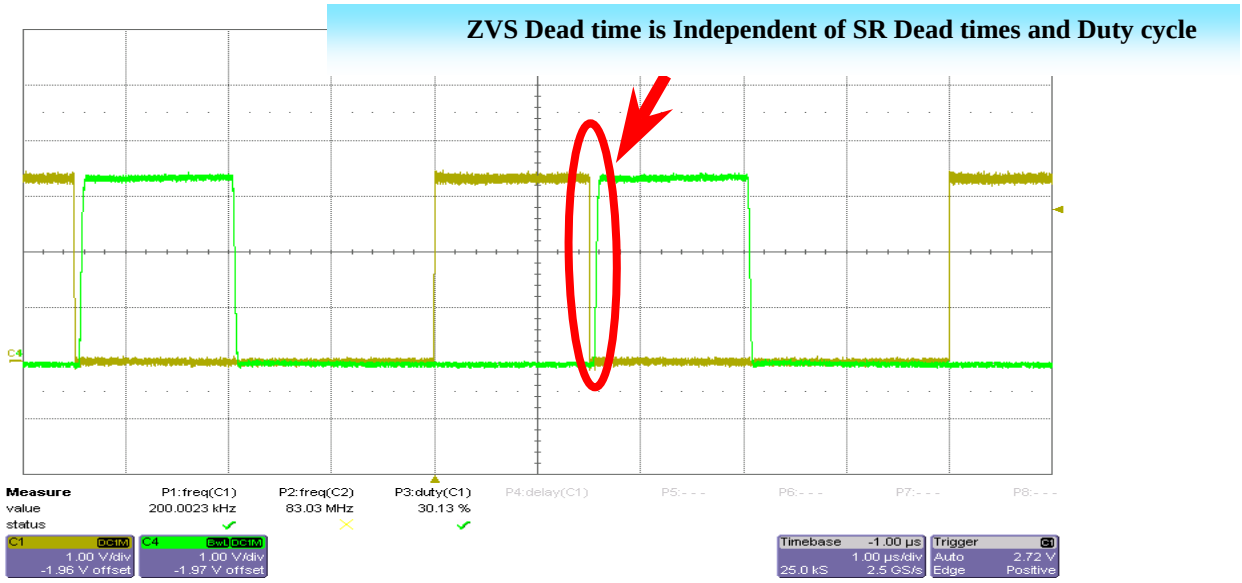


Figure 5.3: The primary signals with 100ns dead time in a DCS case

In the actual experiments, we set up the close loop system with DSP-controlled HB power train as shown in Figure 5.5. We use the low-pass filter before DSP board to filter the switching noise and this filter behaves as an anti-liaising filter for the sampling of the ADC. The protection circuit is used to give a voltage limit from 0 volts to 3 volts for the input signal of the DSP since that is the range DSP can accept.

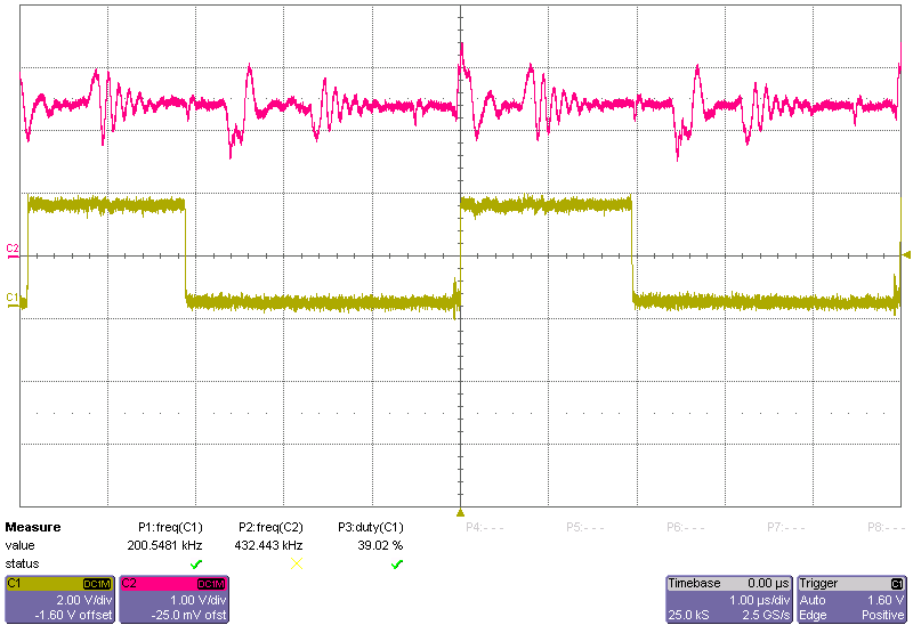


Figure 5.4: The output voltage with significant noise

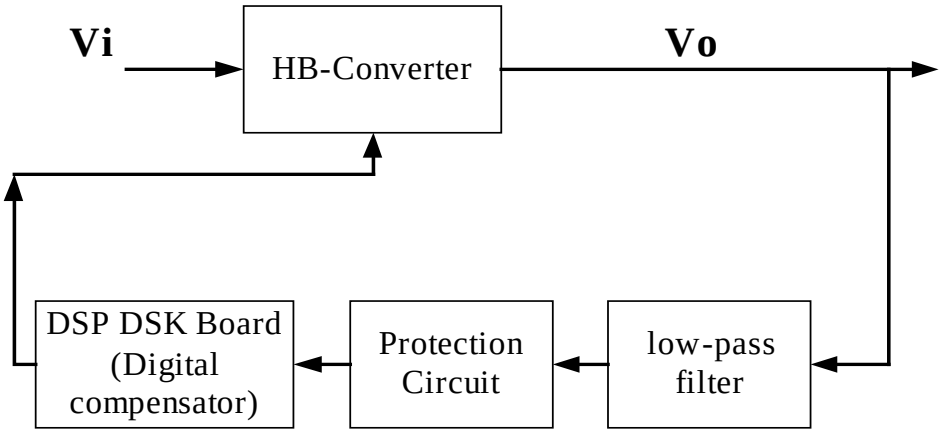


Figure 5.5: Close loop diagram with power stage and DSP controller

Figure 5.6 shows the output voltage and the gate signal for the closed-loop DSP controller. In this case, the input voltage is 48 volts. We can see the output voltage is regulated to the reference voltage of 1.5 volts, which is actually set up in the DSP program. The duty cycle is regulated at D=0.26, which is the calculation result of a digital PI compensator based on the error difference compared with the reference voltage. And Figure 5.7 and 5.8 are showing the transformer current at steady state.

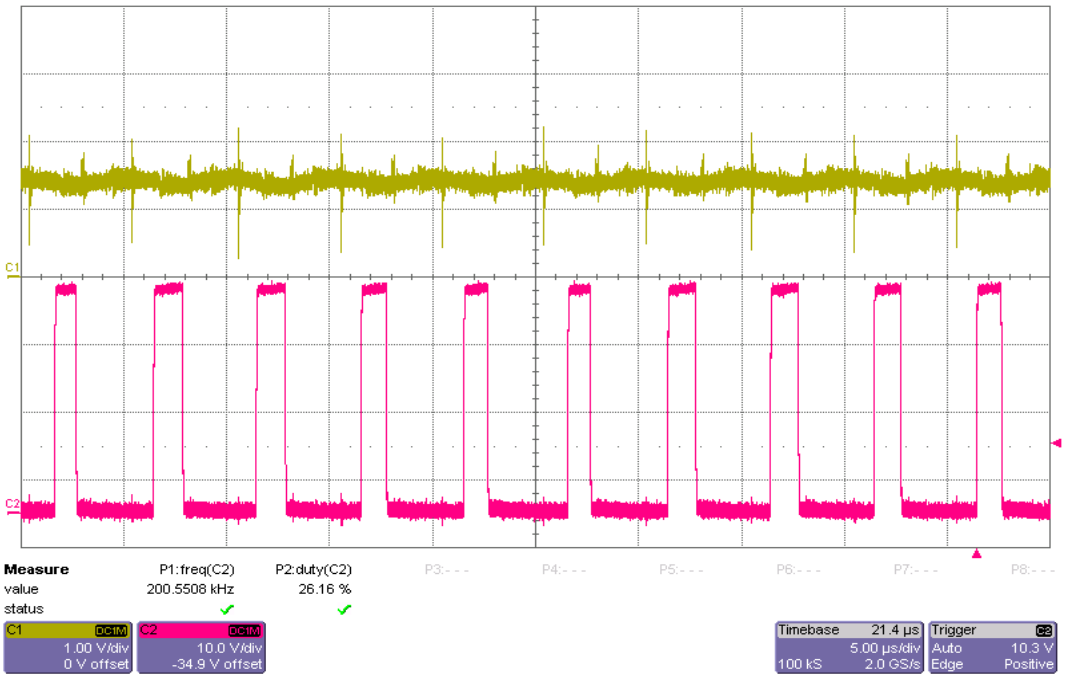


Figure 5.6: The output voltage 1.5 volt and gate signal with 0.26 duty cycle at steady state With a DSP controller (digital PI compensator) in symmetrical case

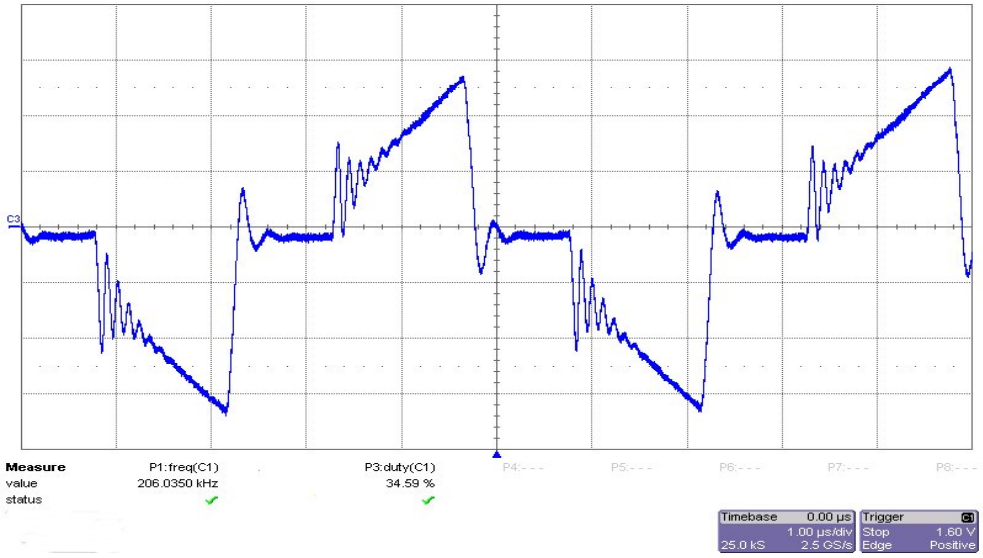


Figure 5.7: The transform primary current

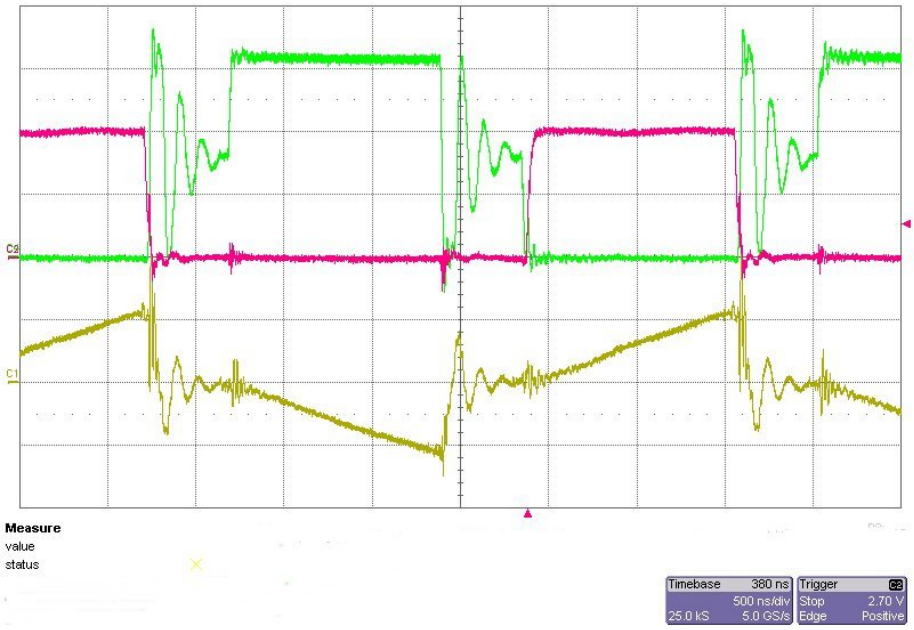


Figure 5.8: The transform primary current, gate and drain-source signals of the low-side switch

5.2 Consideration and Analysis

5.2.1 Noise Issue

Due to the switching noise and connection noise in the experiment, the low-pass filter is necessary for stability of the system. But the bandwidth of the low-pass filter obviously will affect the entire bandwidth of the system. This means that if the bandwidth of the low-pass filter is too low, the dynamic performance of the system is going to be affected. Therefore, the tradeoff should be considered before choosing the bandwidth of the low-pass filter when a system has considerable noise.

One of the approaches to reduce the switching noise is to make the sampling happen after the switching noise, which is supposed to appear at the beginning of each switching cycle. This approach needs to synchronize the sampling cycle and PWM cycle with fixed phase shift inside DSP, which will be discussed in the synchronization section of this chapter.

5.2.2 Frequency Limitations

The sampling frequency of the ADC of the TMS320F2812 can reach 12.5MHz theoretically. However, the maximum switching frequency at which the converter can be operated is dependent upon the time required by the processor to complete all instructions as well as the performance requirement. Let τ be the time required to complete one instruction, N be the number of instructions to be computed, η be the time required for ADC conversions and other delays and f be the sampling frequency. Then, we must have: $\tau N + \eta < \frac{1}{f}$.

In the interrupt routine of the ADC, dealing with the data and calculation of the compensator will consume considerable instructions, which makes it impossible to reach the maximum sampling frequency of 12.5MHz for the ADC. In our experiment, the interrupt routine consumes about 100 instructions, which is around 700ns, so that the sampling frequency we can reach is around 1.4MHz. Therefore, optimizing and reducing the number of the instructions for the compensator calculation and digital filtering is an important issue.

5.2.3 Synchronization

Synchronization is an important requirement in any digital controller. Signals must be sampled at the same relative position in each period, and failing to do so will cause the calculated duty cycle to be meaningless — especially when the ripple amplitudes are significant. For simplicity and ease of implementation, the processor will take control of: all signals that determine the start of a period, the sampling time for the input signals and the time needed to issue the duty cycle signal. Furthermore, to minimize the effect of noise, sampling of the input signals is scheduled to take place at the instant before the power MOSFET is switched off.

In short, the period starts when a triggering signal is sent out to sample all the necessary inputs. Immediately after this, the power MOSFET is turned off, and the processor commences to calculate the required value of the duty cycle.

In our experiment, this synchronization has not been achieved yet, so the low-pass filter is used to deal with the switching noise.

5.2.4 Software

Generally, there are two main considerations in the design of the software, namely accuracy and speed. TMS320F2812 supports the 32-bits fixed-point format, and, based on this, the C28** IQ math library will provide sufficient accuracy for the arithmetic operations. The IQ math library allows the customer to code the algorithms in such a way that it seems like they are coding with the ease of floating point, even though this DSP is a cost effective fixed-point machine. Numeric precision and dynamic range requirement will vary considerably from one application to another, and higher precision results in a lower dynamic range. Hence, the system designer must trade off between the range and the resolution before choosing an IQ format. In our experiments, we choose IQ18 as the default IQ format for most of the arithmetic operations with the considerations of sufficient precision and dynamic range for our application.

Of vital importance are the choice of the algorithm and the way in which it is executed. Care must be taken to avoid redundant calculations at all costs, which eat up computation time.

CHAPTER SIX: CONCLUSION

6.1 Summary

The thesis presents the DC state space model and unified small signal model of half-bridge converters with current doubler both for symmetrical and asymmetrical case. Based on the small signal models of HB converters, a digital compensator is designed to stabilize and optimize the system. The digital controller with ADC and PWM generators is implemented with a DSP chip, which is a high performance DSP chip especially for digital control applications.

Based on the small-signal models, the digital controller design method and some important practical design issues and considerations are discussed in this thesis. Experimental work shows that a digital compensator that is implemented in a DSP program can regulate the output voltage by adjusting the duty cycle with desired performance.

As power-processing equipment becomes more complicated, more sophisticated control algorithms will be required. The microprocessors will certainly play an important role in controlling such equipments. In addition, as the price of a digital signal processor decreases and the performance is expected to be higher in coming years, the use of DSP in processing electrical power will become increasingly popular. The high frequency low voltage HB DC-DC converter reported in this thesis represents an attempt to control DC-DC converter digitally through a DSP.

6.2 Future Work

In future work, the system will focus on how to optimize the digital controller, which includes: reducing the number of the instructions to increase the achievable sampling frequency, implementing the synchronization of the sampling and switching cycle, tuning up the coefficients of the compensator and increasing the bandwidth of the low-pass filter to improve the transient response of the system.

A more complicated and nonlinear algorithm will be attempted in DSP to improve system performance, which is generally difficult to implement in analog circuits. This algorithm may include adaptive and predictive control or a control based upon efficiency peaking, thermal management and other factors.

The DSP can also play an important role in managing, monitoring and testing of the power system. DSP can be used to execute data acquisition, signal conditioning, filtering, spectral analysis and transient capture, and it has the capability to monitor and control systems concurrently. This is particularly useful in adaptive control because the controller can dynamically change the structure or parameters in real time in response to variations in system behavior. Testing capabilities built into power electronics systems are used to identify system parameters for automatic tuning of controller gains and to locate faults in the event of a failure. Such systems facilitate testing by performing a selected acquisition of data and recording the stimulated system responses.

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