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Adaptive Efficiency Optimization For Digitally Controlled Dc-dc Converters

Wisam Al-Hoor
University of Central Florida

ADAPTIVE EFFICIENCY OPTIMIZATION FOR DIGITALLY CONTROLLED DC-DC CONVERTERS

by

WISAM M. AL-HOOR

B.S. Princess Sumaya University for Technology, 2002
M.S. University of Central Florida, 2006

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Major Professor: Issa Batarseh

ABSTRACT

The design optimization of DC-DC converters requires the optimum selection of several parameters to achieve improved efficiency and performance. Some of these parameters are load dependent, line dependent, components dependent, and/or temperature dependent. Designing such parameters for a specific load, input and output, components, and temperature may improve single design point efficiency but will not result in maximum efficiency at different conditions, and will not guarantee improvement at that design point because of the components, temperature, and operating point variations.

The ability of digital controllers to perform sophisticated algorithms makes it easy to apply adaptive control, where system parameters can be adaptively adjusted in response to system behavior in order to achieve better performance and stability. The use of adaptive control for power electronics is first applied with the Adaptive Frequency Optimization (AFO) method, which presents an auto-tuning adaptive digital controller with maximum efficiency point tracking to optimize DC-DC converter switching frequency. The AFO controller adjusts the DC-DC converter switching frequency while tracking the converter minimum input power point, under variable operating conditions, to find the optimum switching frequency that will result in minimum total loss and thus the maximum efficiency.

Implementing variable switching frequencies in digital controllers introduces two main issues, namely, limit cycle oscillation and system instability. Dynamic Limit Cycle

Algorithms (DLCA) is a dynamic technique tailored to improve system stability and to reduce limit cycle oscillation under variable switching frequency operation.

The convergence speed and stability of AFO algorithm is further improved by presenting the analysis and design of a digital controller with adaptive auto-tuning algorithm that has a variable step size to track and detect the optimum switching frequency for a DC-DC converter. The Variable-Step-Size (VSS) algorithm is theoretically analyzed and developed based on buck DC-DC converter loss model and directed towered improving the convergence speed and accuracy of AFO adaptive loop by adjusting the converter switching frequency with variable step size.

Finally, the efficiency of DC-DC converters is a function of several variables. Optimizing single variable alone may not result in maximum or global efficiency point. The issue of adjusting more than one variable at the same time is addressed by the Multivariable Adaptive digital Controller (MVAC). The MVAC is an adaptive method that continuously adjusts the DC-DC converter switching frequency and dead-time at the same time, while tracking the converter minimum input power, to find the maximum global efficiency point under variable conditions.

In this research work, all adaptive methods were discussed, theoretically analyzed and its digital control algorithm along with experimental implementations were presented.

To my parents with love and gratitude.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER ONE
INTRODUCTION

1.1 Background and Motivation

The ever increasing demand for power converter systems with smaller size, higher efficiency and more tight output regulation place many challenges over the traditional analog control approach. Digital control is a new promising direction that offers many advantages over analog controllers [1-26]. One of the most important advantages is the ability to apply advanced non-linear control algorithms. Newer power converter systems may have two or more control loops that interact with each other to: control output variables, enhance dynamic response, and optimize certain system parameters. Building such control schemes using analog controllers is a very difficult and time consuming task, where it can be easily programmed using a digital controller. Reliability is another important advantage; digital controller's needs few passive components compared to analog controllers which make them less sensitive to components tolerances, aging and temperature variations. Finally digital controllers offers flexibility, where all the control laws and monitoring schemes can be programmed in a single digital controller, and can be easily changed in case of new design requirements [9].

Fig. 1.1 shows typical digitally controlled synchronous buck DC-DC converter. The closed loop in Fig. 1.1 starts by measuring output voltage using a signal conditioning circuit that attenuates noise levels and convert the measured signal to a level appropriate for the Analog to Digital Converter (ADC). The measured signal is then sampled using the ADC and compared to a programmable reference inside the digital controller. The resultant error signal is then processed by the digital PID compensator that will calculate the required duty-cycle. Digital pulse width modulation (DPWM) unit works on the compensated error signal from the PID and generates a PWM signals with the correct frequency and duty cycle to the driver of the DC-DC converter. The sensed output voltage is not only used for voltage regulation, but can be also used to protect the DC-DC converter by shutting down the PWM signals when a faulty condition occurs [12].

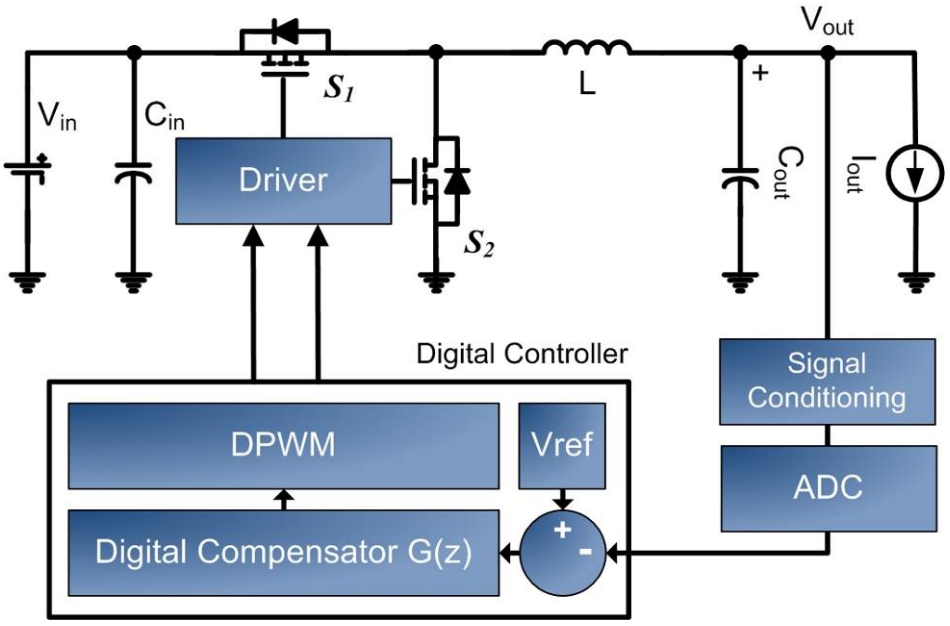


Fig. 1.1: General block diagram for a digitally controlled power converter

According to control theory, there are two ways to design a digital controller [15]. The first method is the direct digital design, where a discrete time model of the system is first obtained then the controller is directly designed in the z-domain using traditional methods like frequency response bode plots, or root locus method. Direct digital design offers the advantages of better system response and the ability to achieve better phase and gain margins [15,16,19]. The other design method is the digital redesign, where the controller is first designed in continuous time domain (s-domain) then transformed to z-domain using well known discretization methods [15,16]. Digital redesign has the advantages of easier design process and the ability to apply known analog controller design techniques [15,22].

This work focuses on moving with power converters digital control beyond the conventional closed loop design into more advanced control schemes that will take the full advantage of digital controllers to harvest the benefits of improved efficiency and better converter dynamics. The following is the literature review and introduction of the work covered in this dissertation.

1.2 Adaptive Efficiency Optimization

Design optimization of the DC-DC converters requires the optimum selection of several parameters to achieve improved efficiency and performance. Some of these parameters are load dependent, input/output voltage dependent, components dependent, and/or temperature dependent. Designing such parameters for a specific load, input and output, components, and temperature may improve single design point efficiency but will

not result in maximum efficiency at different load and line conditions and will not guarantee improvement at that design point because of the components, temperature, and operating point variations [27-32]. As the processing power of digital controllers is becoming better at lower cost and lower power consumption, the ability to implement complex control law becomes easier and more practical for power conversion applications. One interesting type of control is adaptive control, where system parameters are dynamically adjusted in response to system changes in order to achieve better efficiency and dynamics [27,28].

One important parameter to be optimized for power converters is the switching frequency, in order to improve efficiency over wide range of operating conditions such as load conditions [31]. For example, for a wide load range low-output voltage DC-DC converter, selecting the optimized switching frequency is an important design parameter. Usually lower switching frequency means lower switching losses. Switching losses increase at higher switching frequencies while conduction losses become higher at heavier load currents [31,32]. Higher efficiencies are important at all operating conditions and at light load conditions to achieve energy savings and to extend battery life [27-44].

Variable switching frequency schemes have been used at light load in conjunction with DCM (Discontinuous Conduction Mode) to improve light load efficiency. For example, in [31], a synchronous buck converter is used to operate in the DCM with variable switching frequency that change according to the load current. Operating in DCM at light loads prevents the inductor current from going negative, which helps in reducing the conduction losses since there will be no circulating energy in the synchronous

converter [31]. This will also result in lower switching losses since the synchronous rectifier is turned off at zero current. Moreover, operating at lower switching frequency reduces the switching losses. Operating in DCM with a lower switching frequency results in a converter that has higher efficiency at lighter loads. Since the converter operates in DCM and the switching frequency is reduced, a larger output capacitor may be needed to filter out the resulting large ripple current [35,38].

A peak current control method is used in [31], which may cause converter instability [35]. A modified approach to solve this issue was proposed in [32] and named hybrid control, where the DC-DC converter operates in the CCM (Continuous Conduction Mode) with fixed frequency at heavy loads, and in DCM with variable switching frequency that is also a function of the load current at light loads. In [39,40] and [43], a method is proposed that varies the switching frequency non-linearly, by tracking the peak inductor current in order to achieve efficiency at lighter loads while keeping maintained performance.

On the other hand, the optimum switching frequency value for the highest efficiency even in CCM fixed frequency operation is determined in conjunction with other design variables and assumptions. Usually, this optimum frequency is selected at nominal converter operating conditions (nominal input voltage, load range, temperature, inductor value, …etc.) and for assumed components and parasitic values. Operating far from these nominal conditions and assumed design variables will result in not operating at the optimum switching frequency value for maximum conversion efficiency.

The Adaptive Frequency Optimization (AFO) method starts by presenting an adaptive digital closed loop controller, with lower bandwidth than the output voltage regulation loop, to optimize and auto-tune the converter switching frequency on-the-fly under variable operating conditions. The proposed controller adaptively chooses the best switching frequency for the DC-DC converter, as operating conditions vary, by tracking the maximum efficiency point [28]. The Adaptive-Frequency-Optimization (AFO) changes the switching frequency to achieve lower combined switching and conduction losses, and as a result, achieves higher power conversion efficiency.

In the second part of the AFO method, design considerations that are related to variable switching frequency power digital controllers are summarized, and a dynamic technique that adjusts the system resolution to avoid the limit cycle oscillation problem is proposed [49-59]. This proposed dynamic technique alleviates some issues that result in digitally controlled variable frequency converters, which affect stability and dynamics. AFO algorithm along with improved controller designed is roughly studied and analyzed and simulation and experimental results to prove the concept are presented.

1.3 Variable Step Size Auto-Tuning Algorithm

It is known that the power conversion efficiency of a DC-DC converters is typically a function of several design variables such as switching frequency, output inductance, switching devices characteristics, and dead-time and is a function of several other surrounding factors such as temperature and component aging [28,31-42].

Switching power converters designer optimize the efficiency based on given and assumed components characteristics and parasitics under a given set of pre-defined operating conditions and design specifications [31-42]. Usually, the efficiency-based design optimizations target at achieving the best tradeoff between different types of power losses including conduction losses, switching losses and gate drive losses at a certain load [37-40]. Such designs will only result in achieving the maximum efficiency for one set of operating conditions, which may result in conversion efficiency degradation under different sets of operating conditions. This is true for on-board power converters that use discrete components and also true for on-chip integrated power converters [41, 42].

Digital controllers allow flexibility in realizing adaptive and advanced control schemes [27-29, 52-54]. Adaptive auto-tuning power controllers can adjust power converter parameters for maximized efficiency is under variable conditions [35,40,27-29]. However, the convergence stability, convergence speed, convergence error and simplicity/complexity are among the important characteristics of an adaptive auto-tuning controller, which need to be carefully studied and improved.

The switching frequency and Synchronous Rectifiers (SR) dead-time are two of the parameters which need to be optimized under variable conditions for maximum efficiency during the life time of the converter [27-29]. The SR dead-time can be optimized based on either the input current/power value minimization or based on the duty cycle value minimization as discussed in [28, 29]. In general, the method that is based on the duty cycle is suitable and accurate only for some of the non-isolated type converters, while the method that is based on the input current/power can be applied to both isolated

and non-isolated converters. The later method can be used to auto-tune converter parameters such as switching frequency in addition to SR dead-time.

In previous work [27-29], the proposed algorithms were implemented using fixed-step-size (fixed increment and decrement of the variable value being auto-tuned). In fixed setp size algorithms, the designer has to choose either a small step-size (limited by the hardware resolution) that will result in longer controller convergence time to reach the optimum parameter value but with better accuracy, or he has to choose a large step-size that will result in shorter controller convergence time to the optimum parameter value but with lower accuracy.

In this work, the effect of variable conditions on conversion efficiency is considered and a Variable Step Size (VSS) algorithm and the corresponding controller with good tradeoff between conversion speed, stability, and accuracy are proposed. The VSS control loop is theoretically analyzed and its design and stability criteria are developed. The developed algorithm and its theory are verified by a proof of concept experimental prototype results. While chapter three focus on analyzing and implementing the VSS to auto-tune the switching frequency of a power converter, the approach can be also extended to auto-tune the SR dead-time.

1.4 Multivariable Adaptive Digital Controller

Optimizing the efficiency of DC-DC converters is one of top priorities for power electronics design engineer. Power converter losses, and the resultant power efficiency for

a given design varies at different loading conditions, line conditions, and it is impacted by the variations of temperature and aging effect [27-44]. From studying the power loss in DC-DC converter, it can be noted that there are two main kinds of losses, DC-DC converter switching losses and DC-DC converter conduction losses [31-38]. Switching losses are function of the switching frequency and conduction losses are function of the load current. Optimizing DC-DC converter switching frequency is one way to reduced switching losses [27,31,35]. While optimizing DC-DC converter dead time value can reduce conduction losses [31-38].

The ability of a digital controller to perform sophisticated algorithms makes it easy to apply adaptive control laws where system parameters can be dynamically adjusted in response to system behaviors in order to achieve better efficiency [28]. An adaptive controller and algorithm to optimize switching frequency of DC-DC converter is presented in [27] based on the efficiency tracking concept discussed in [28]. However, the controller in [27] optimizes one parameter: the switching frequency, while the controller in [28] optimizes another parameter only: the SR dead-time. Optimizing one parameter at a time may not result in maximum or global efficiency point and combined efficiency improvement.

Since the input power/current used in both [27] and [28] as the function to minimize, a single controller that optimize both variables and exhibits multivariable behavior can be used. In chapter 4, the analysis and experimental results for a multivariable adaptive controller that optimize DC-DC converter switching frequency and dead-time together is presented.

CHAPTER TWO
ADAPTIVE DIGITAL CONTROLLER AND DESIGN CONSIDERATIONS FOR A VARIABLE SWITCHING FREQUENCY VOLTAGE REGULATORS

2.1 Introduction

Power converter efficiency improvement is a major concern for power electronics design engineers. Higher efficiency values reveal better utilization of the available input power, and less stresses, and thus better reliability for the power converter system on hand. While the common approach for conversion efficiency improvement is using more optimized hardware components, a new approach, that utilize advanced control theory, to optimize converter operating parameters, proved to be effective in tackling the efficiency problems.

In this chapter an adaptive digital controller with maximum efficiency point tracking to optimize DC-DC converter switching frequency is presented. The Adaptive-Frequency-Optimization (AFO) controller adjusts the DC-DC converter switching frequency while tracking the converter minimum input power (maximum efficiency) point under variable conditions including variable load and variable input voltage. The AFO digital controller continuously finds the optimum switching frequency that will result in the minimum total loss while converter parameters and conditions vary. Moreover, the presented controller addresses issues that are associated with implementing variable switching frequencies in digital controllers, such as limit cycle oscillation and system

instability, using a dynamic algorithm to improve system stability under variable switching frequency operation.

Next section briefly discusses the switching frequency effects on losses. Section 2.3 presents the adaptive-frequency optimization controller and its algorithm to optimize the switching frequency to improve converter efficiency. Section 2.4 discusses the gain and phase considerations when designing a variable frequency digital controller. The limit cycle issue and the proposed dynamic algorithm to avoid it are discussed in Section 2.5. The experimental work is discussed in Section 2.6 while the conclusion is given in Section 2.7.

2.2 Switching Frequency Effect on Losses

Fig. 2.1 shows a non-isolated buck DC-DC converter with synchronous rectification to be taken as a converter example to present the AFO and the Dynamic Limit Cycle Algorithms (DLCA) of this chapter. As stated earlier, switching losses are due to many reasons including the control and synchrnous MOSFETs output capacitances charge and discharge, the control and synchrnous MOSFET input capacitance charge and discharge (gate drive losses) and voltage-current turn off overlapping. Where as, conduction losses are mainly due to the components' parasitic resistances; which include the lower and upper MOSFET ON-resistance, the inductor winding DC resistance (DCR), the capacitor equivalent series resistance (ESR) and the sensing resistances [30-44]. Fig. 2.2 shows typical switching and conduction losses for the synchnous buck coverter discussed in section 2.6 at different load conditions with fixed switching frequency: it is

clear that the switching losses are dominant at light loads while conduction losses are dominant at heavy loads. A complete list of equations that summarizes the switching and conduction losses for a synchronous buck converter in both Discontinuous Conduction Mode (DCM) and continuous Conduction Mode (CCM) are discussed in [35,36,38].

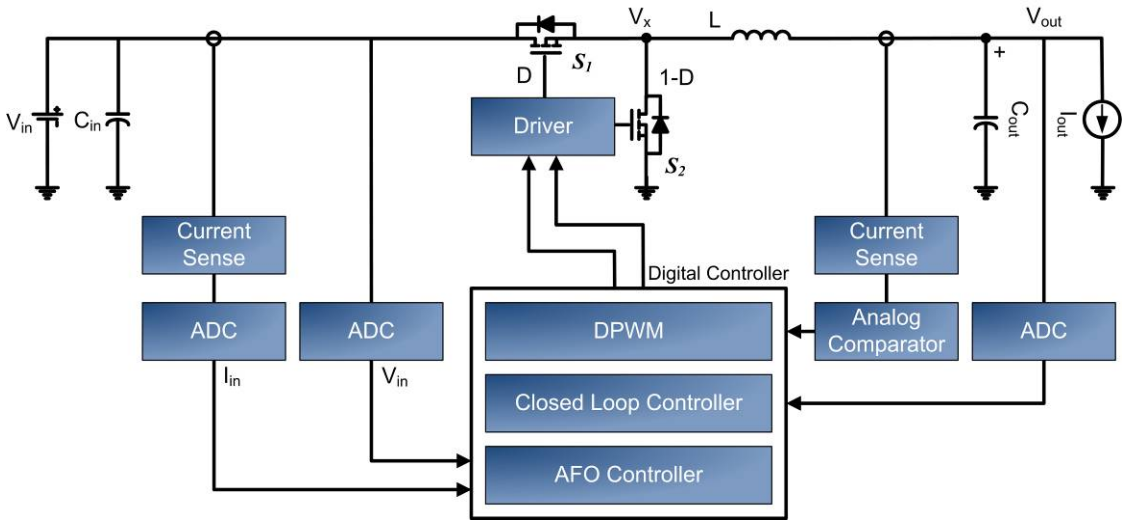


Fig. 2.1: Non-isolated buck DC-DC converter with synchronous rectification.

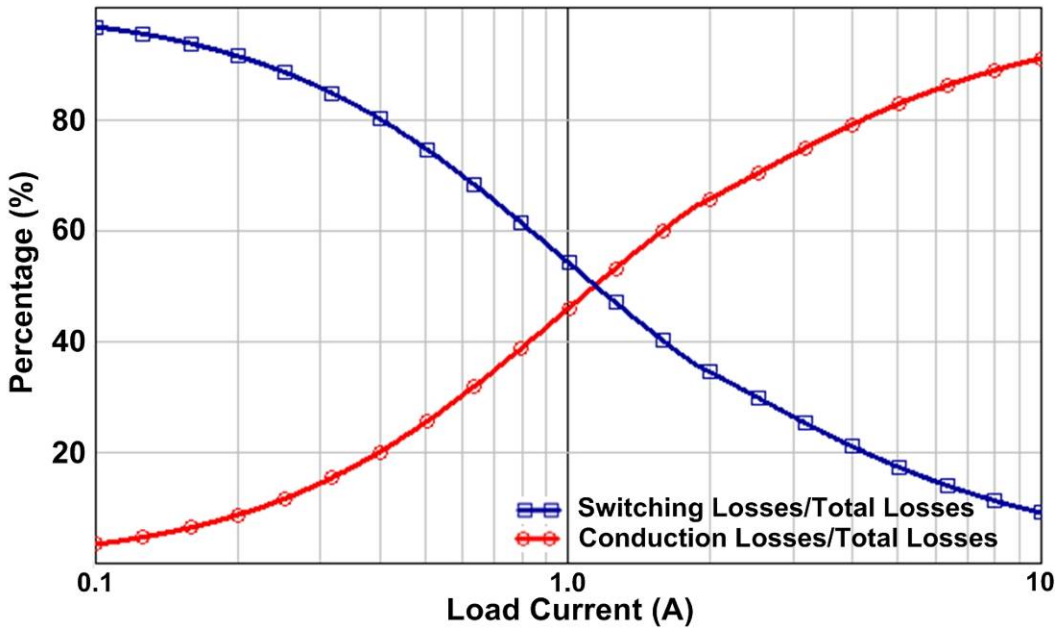
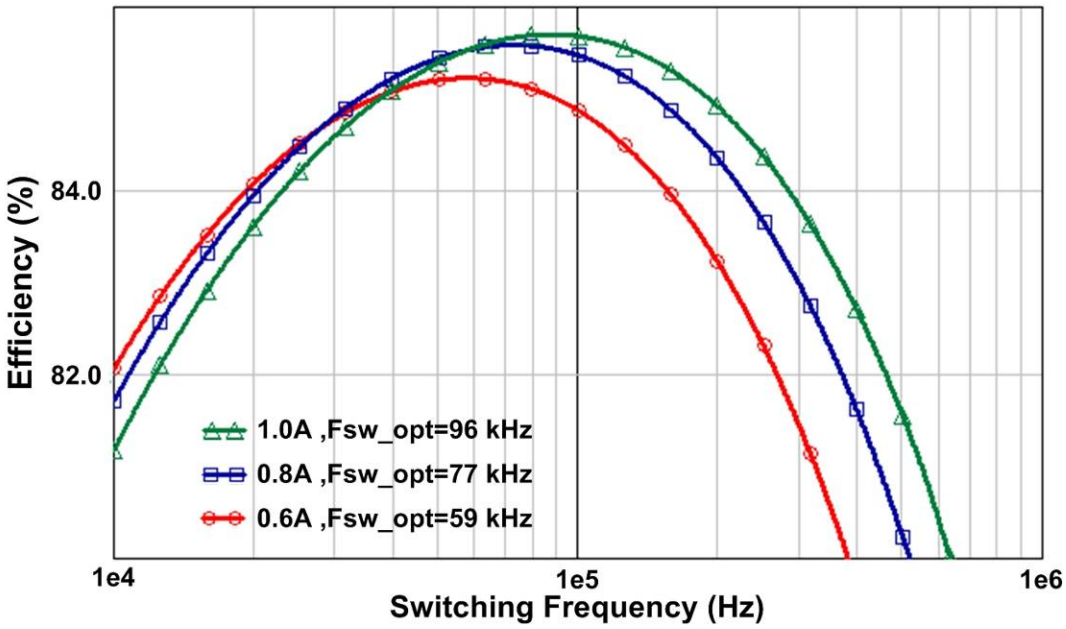


Fig. 2.2: Switching and conduction power losses normalized to the total power loss vs. load current under fixed switching frequency operation for a given design.

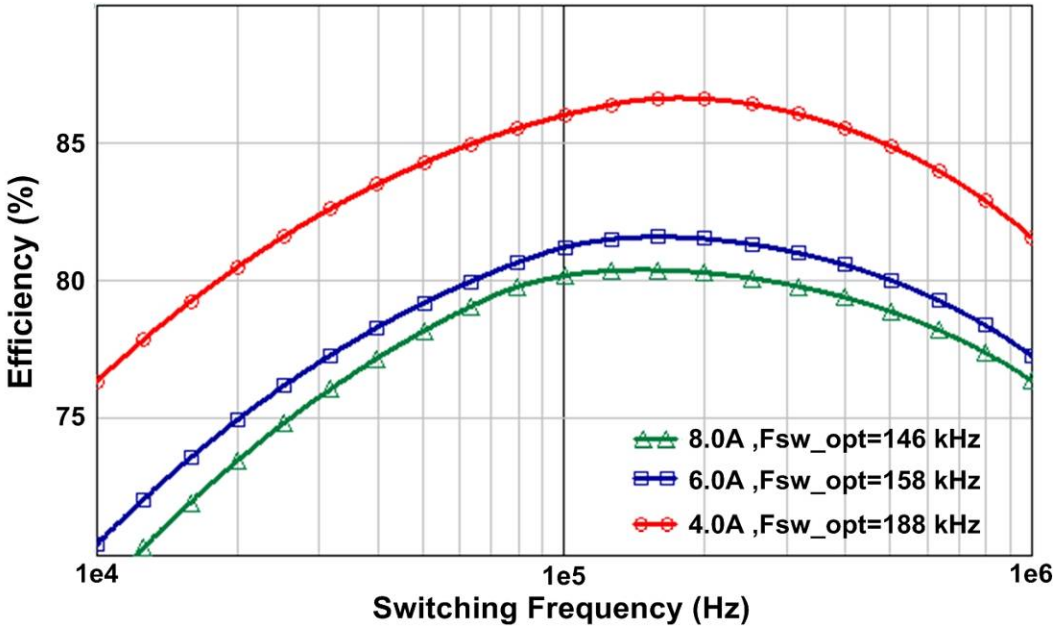
Lower switching frequency means lower switching and driving losses. Moreover, the switching and driving losses increase with the switching frequency while the conduction losses decrease because of lower ripple and *rms* currents. Also, the conduction losses increase with the load current increase. The optimized switching frequency that achieves the lowest total switching and conduction losses is related to many nonlinear parameters that makes the optimized switching frequency (f_{swO}) different at different conditions. An adaptive controller that adaptively adjusts f_{sw} within a range depending on such nonlinear parameters variation can be used to achieve the optimum switching frequency. Fig. 2.3 shows efficiency simulation results curves at different load currents for synchronous buck converter discussed in section 2.6. From Fig. 2.6 it can be noted that there is a different optimized switching frequency where the efficiency is maximum for

both DCM and CCM operation. Fig. 2.3 (a) shows the simulation results when DCM operation is allowed and Fig. 2.3 (b) shows the simulation results when DCM is not allowed at all conditions (or in other words, while operating in CCM at all conditions). These curves shows that even in CCM, the optimum switching frequency is not necessarily fixed and it can vary. Moreover, as stated earlier, the optimum switching frequency will vary based on components parasitic variations resulted for example from aging and temperature variations.

Next section presents the Adaptive-Frequency-Optimization (AFO) method that tracks the optimum switching frequency (f_{swO}) to achieve peak efficiencies under variable conditions. Even though the discussion of this chapter is based on a low power design example for the sake of concept demonstration, the method is applicable to higher power levels where its implementation is more justifiable and the power savings are larger.



(a)



(b)

Fig. 2.3: Simulation efficiency curves vs. switching frequency: (a) DCM operation is allowed, and (b) DCM operation is not allowed (CCM only)

2.3 Adaptive Frequency Optimization (AFO) Digital Controller

Fig. 2.4 shows an implementation flowchart for the AFO algorithm. The algorithm can be activated periodically or it can run in continuous manner with appropriate delay between iterations. N samples of P_{in} (converter sensed input power, or input current at a fixed input voltage) are taken by the ADC (Analog-to-Digital Converter) and averaged to generate $P_{in}(n)$. $P_{in}(n)$ is used as an indication of the converter efficiency since the maximum efficiency occurs at the minimum input power. It is proved theoretically and experimentally that the switching frequency versus input power at a certain load current, has one local minimum [27]. So P_{in} can be used in the adaptive loop to decide the value of the digital controller switching frequency. Next, the AFO algorithm calculates the difference between the present and the previous values of P_{in} and the difference between the present and the previous values of f_{sw} as follows:

$$\Delta P_{in} = P_{in}(n) - P_{in}(n-1) \tag{2.1}$$

$$\Delta f_{sw} = f_{sw}(n) - f_{sw}(n-1) \tag{2.2}$$

Next, a check is performed to see if ΔP_{in} has sufficient difference (p_e) to update f_{sw} or not. If this difference is sufficient, the program will proceed to the next step. Otherwise, it will start from the beginning by sampling P_{in} again. If the signs (positive or negative) of

Equations (2.1) and (2.2) are similar, this means f_{sw} should be incremented by f_{sw_step} to move toward the maximum efficiency point (or minimum input power). Otherwise, if the signs of Equations (2.1) and (2.2) are not similar, this means f_{sw} should be decremented by f_{sw_step} to move toward the maximum efficiency point. Increasing the converter efficiency by decreasing the input power indicates a reduction in the total losses to the minimum possible value (optimal switching frequency value). After storing the current values of P_{in} and f_{sw}, the program will decrement or increment f_{sw} and update it. Then, after several (M) switching cycles (enough to reach steady-state), P_{in} is sampled again and the AFO process is repeated. It must be noted that the compensated control signal D_c that regulates the converter output voltage is generated by a digital controller that also contains the AFO algorithm.

At a fixed input voltage, or with relatively very slow changing input voltage, it is sufficient to track the minimum input current value as discussed in [28]. The following discussion in this chapter will base in tracking the minimum input current rather than tracking the minimum input power.

Finally, it should be noted that the AFO loop bandwidth is much smaller than the output voltage regulation loop bandwidth. In practical implementation of the AFO algorithm in a digital controller, the following consideration should be taken into account:

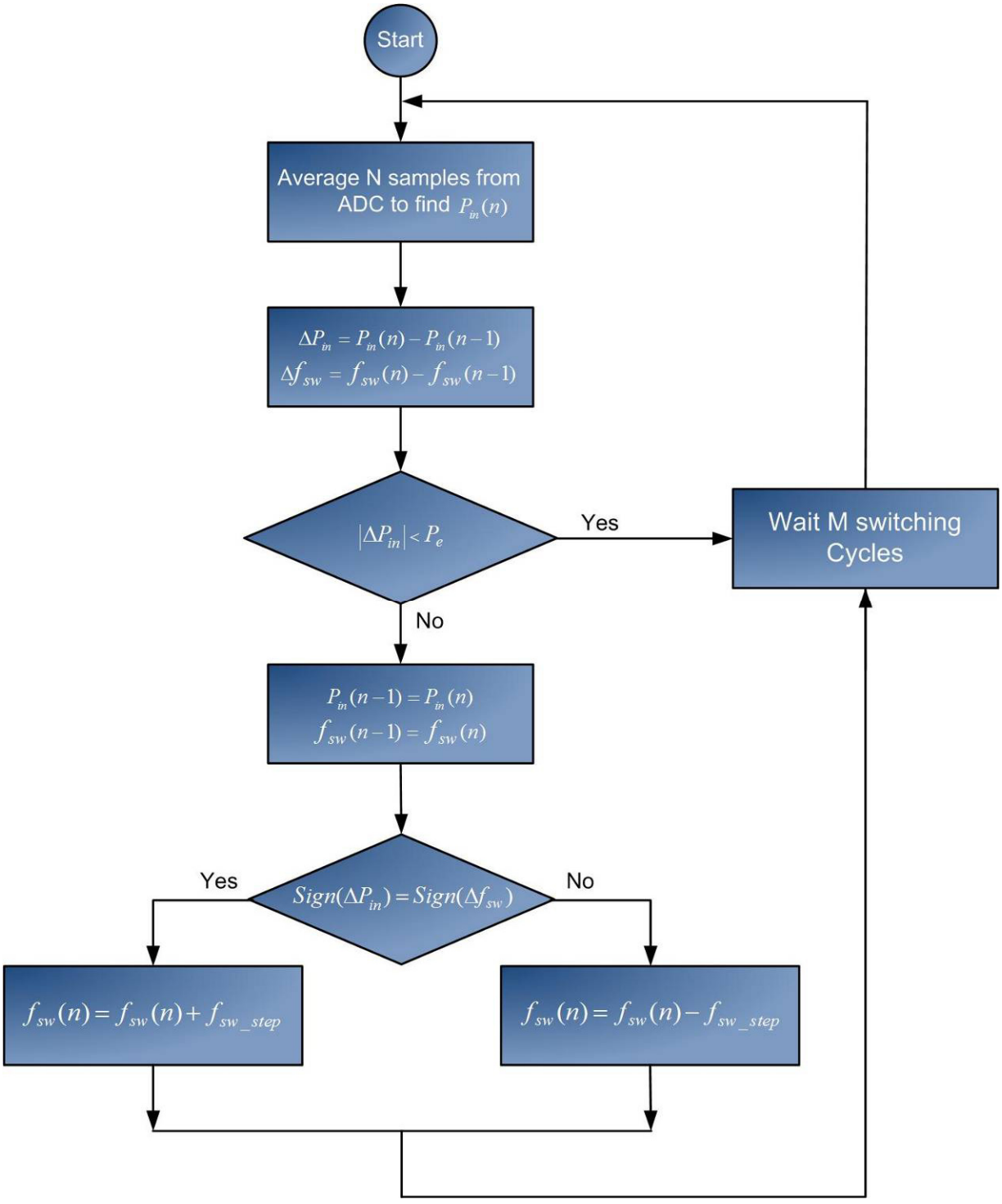


Fig. 2.4: The Adaptive-Frequency-Optimization (AFO) digital controller flowchart

2.3.1 Switching Frequency Minimum step size f_{sw_step} Selection

Selecting the switching frequency increment/decrement step size (f_{sw_step}) depends on many parameters. This includes the minimum/maximum change in switching frequency that the DPWM can generate, the ADC resolution and the minimum change in switching frequency that will generate a descent and sufficient change in input current (or input power) that can be sensed. In the following, a detailed analysis for the effect of changing the switching frequency on input current is first introduced and then this analysis is used to design for the minimum f_{sw_step} based on a given converter system design parameters.

The sensitivity of the input current, I_{in}, with constant input voltage (assuming the voltage is either constant or slow changing), to a change in switching frequency f_{sw} can be defined as the normalized change in I_{in} over the normalized change in f_{sw}:

$$S_{f_{sw}}^{I_{in}} = \frac{\frac{\Delta I_{in}}{I_{in}}}{\frac{\Delta f_{sw}}{f_{sw}}} = \frac{\Delta I_{in}}{\Delta f_{sw}} \cdot \frac{f_{sw}}{I_{in}} \tag{2.3}$$

For AFO process, where the switching frequency f_{sw} is varied in successive iterations, the sensitivity can be approximated as:

$$S_{f_{sw}}^{I_{in}} = \frac{\partial I_{in}}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} \tag{2.4}$$

Equation (2.4) can also be rewritten as:

$$S_{f_{sw}}^{I_{in}} = \nabla I_{in} \cdot \frac{f_{sw}}{I_{in}}$$

(2.5)

Where ∇I_{in} is the gradient of the input current. The expression for the input current gradient function ∇I_{in} can be obtained as follows:

$$P_{in} = P_{out} + P_{Losses} = V_{out} I_{out} + P_{Losses}$$

(2.6)

The resulting expression for Iin,

$$I_{in} = \frac{V_{out} I_{out}}{V_{in}} + \frac{P_{Losses}}{V_{in}}$$

$$\nabla I_{in} = \frac{\partial I_{in}}{\partial f_{sw}} = \frac{\partial\left(\frac{V_{out} I_{out}}{V_{in}}\right)}{\partial f_{sw}} + \frac{\partial\left(\frac{P_{Losses}}{V_{in}}\right)}{\partial f_{sw}} = \frac{\partial\left(\frac{P_{Losses}}{V_{in}}\right)}{\partial f_{sw}}$$

(2.7)

The sensitivity for each power loss type can be calculated using the gradient function and the total input current sensitivity as follows:

2.3.1.1 Sensitivity for Conduction Losses in CCM Mode:

The conduction losses in synchronous buck converter are the result of the *rms* current passing through the parasitic resistances of the different components. By computing the conduction losses and taking the derivative with respect to the switching frequency, the

sensitivity for conduction losses in Continuous Conduction Mode (CCM) using the gradient function can be given by:

$$S_{f_{sw}}^{I_{\Phi 1}} = S_{f_{sw}}^{I_{\alpha}} + S_{f_{sw}}^{I_{\beta}} + S_{f_{sw}}^{I_{\chi}} + S_{f_{sw}}^{I_{\delta}}$$

(2.8)

Where $S_{f_{sw}}^{I_{\Phi 1}}$: is the change in the input current as a result of all conduction losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_{\alpha}}$: is the change in the input current as a result of control MOSFET conduction losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_{\beta}}$: is the change in the input current as a result of synchronous MOSFET conduction losses in CCM mode under one f_{sw} step. $S_{f_{sw}}^{I_{\chi}}$: is the change in the input current as a result of Inductor conduction losses in CCM mode under one f_{sw} step. $S_{f_{sw}}^{I_{\delta}}$: is the change in the input current as a result of the sense resistor conduction losses in CCM mode under one f_{sw} step. The sensitivity for each conduction loss using the gradient is computed as:

$$S_{f_{sw}}^{I_{\alpha}} = \frac{\partial(\frac{P_{\alpha}}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{1}{6} \cdot \frac{V_{out}^3}{V_{in}^4} \cdot \frac{(V_{in}-V_{out})^2}{L^2 {f_{sw}}^2} \cdot \frac{R_{sw}}{I_{in}}$$

(2.9)

$$S_{f_{sw}}^{I_{\beta}} = \frac{\partial(\frac{P_{\beta}}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^4} \cdot \frac{(V_{in}-V_{out})^3}{L^2 {f_{sw}}^2} \cdot \frac{R_{sr}}{I_{in}}$$

(2.10)

$$S_{f_{sw}}^{I_\chi} = \frac{\partial(\frac{P_\chi}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^3} \cdot \frac{(V_{in} - V_{out})^2}{L^2 {f_{sw}}^2} \cdot \frac{R_{DCR}}{I_{in}}$$

(2.11)

$$S_{f_{sw}}^{I_\delta} = \frac{\partial(\frac{P_\delta}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^3} \cdot \frac{(V_{in} - V_{out})^2}{L^2 {f_{sw}}^2} \cdot \frac{R_{sense}}{I_{in}}$$

(2.12)

Where P_α : is the control MOSFET conduction power losses in CCM mode, P_β : is the synchronous MOSFET conduction power losses in CCM mode, P_χ : is the inductor conduction power losses in CCM mode, P_δ : is the sense resistor conduction power losses in CCM mode, R_{sw} is the ON resistance of a main switch, R_{sr} is the ON resistance of a synchronous switch, R_{DCR} is the inductor parasitic resistance, and R_{sense} is the sensing resistance.

2.3.1.2 Sensitivity for Switching (and Driving) Losses in CCM Mode

Switching losses (including driving losses) in synchronous buck converter are combinations of the turn ON and turn OFF losses of the main and synchronous switch, losses to charge the MOSFETs output capacitance and the driving losses. By computing the switching losses and taking the derivative with respect to the switching frequency, the gradient function for the switching losses in CCM can be given by:

$$S_{f_{sw}}^{I\Phi_2} = S_{f_{sw}}^{I_\varepsilon} + S_{f_{sw}}^{I_\phi} + S_{f_{sw}}^{I_\varphi} + S_{f_{sw}}^{I_\gamma} + S_{f_{sw}}^{I_\kappa} + S_{f_{sw}}^{I_\lambda}$$

(2.13)

Where $S_{f_{sw}}^{I_{\Phi_2}}$: is the change in the input current as a result of all switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\varepsilon}$: is the change in the input current as a result of control MOSFET turn ON switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\phi}$: is the change in the input current as a result of control MOSFET turn OFF switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\varphi}$: is the change in the input current as a result of synchronous MOSFET turn ON switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\gamma}$: is the change in the input current as a result of synchronous MOSFET turn OFF switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\kappa}$: is the change in the input current as a result of MOSFET output capacitance switching losses in CCM under one f_{sw} step. $S_{f_{sw}}^{I_\lambda}$: is the change in the input current as a result of driving losses in CCM under one f_{sw} step. The sensitivity for each conduction loss using the gradient is computed as:

$$S_{f_{sw}}^{I_\varepsilon} = \frac{\partial(\frac{P_\varepsilon}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{2} \cdot \frac{I_{out}}{I_{g_{on}}} \cdot \frac{f_{sw}}{I_{in}} \cdot Q_{sw}$$

(2.14)

$$S_{f_{sw}}^{I_\phi} = \frac{\partial(\frac{P_\phi}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{2} \cdot \frac{I_{out}}{I_{g_{off}}} \cdot \frac{f_{sw}}{I_{in}} \cdot Q_{sw}$$

(2.15)

$$S_{f_{sw}}^{I_\varphi} = \frac{\partial(\frac{P_\varphi}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{1}{4} \cdot \frac{V_{out}}{V_{in}^2} \cdot \frac{(V_{in} - V_{out})}{L} \cdot \frac{t_{rise\_sr} \cdot V_D}{I_{in}}$$

(2.16)

$$S_{f_{sw}}^{I_\gamma} = \frac{\partial(\frac{P_\gamma}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{4} \cdot t_{fall\_sr} \cdot \frac{V_{out}}{V_{in}^2} \cdot \frac{(V_{in} - V_{out})}{L} \cdot \frac{V_D}{I_{in}}$$

(2.17)

$$S_{f_{sw}}^{I_\kappa} = \frac{\partial(\frac{P_\kappa}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{2}(Q_{oss\_sw} + Q_{oss\_sr}) \cdot \frac{f_{sw}}{I_{in}}$$

(2.18)

$$S_{f_{sw}}^{I_\lambda} = \frac{\partial(\frac{P_\lambda}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{2Q_{gsw}V_g}{V_{in}} \cdot \frac{f_{sw}}{I_{in}}$$

(2.19)

Where P_ε : is the control MOSFET turn ON switching power losses in CCM, P_ϕ : is the control MOSFET turn OFF switching power losses in CCM, P_φ : is the synchronous MOSFET turn ON switching power losses in CCM, P_γ : is the synchronous MOSFET turn

OFF switching power losses in CCM, P_{κ} : is the MOSFET output capacitance switching power losses in CCM, P_{λ} : is the driving power losses in CCM. Q_{sw} is the main switch charge, $I_{g_{on}}$ is the Driver ON current, $I_{g_{off}}$ is the Driver OFF current, V_D is the forward voltage drop of the switch body diode, t_{rise_sr} is the turn ON rise time of the synchronous switch, t_{fall_sr} is the turn OFF fall time of the synchronous switch, and Q_{oss} is MOSFET output charge. From the above, the input current sensitivity for total losses in CCM is:

$$S_{f_{sw}}^{I_{\Phi_{total}}} = S_{f_{sw}}^{I_{\Phi_1}} + S_{f_{sw}}^{I_{\Phi_2}}$$

(2.20)

Where $S_{f_{sw}}^{I_{\Phi_{total}}}$: is the change in the input current as a result of all switching and conduction losses in CCM under one f_{sw} step

2.3.1.3 Sensitivity for Conduction Losses in DCM Mode

Following the same procedure in CCM analysis above, start by computing the gradient for the conduction losses in Discontinuous Conduction Mode (DCM) , by taking the derivative with respect to the switching frequency, the sensitivity for conduction losses in DCM can be given by:

$$S_{f_{sw}}^{I_{\Psi_1}} = S_{f_{sw}}^{I_{\mu}} + S_{f_{sw}}^{I_{\nu}} + S_{f_{sw}}^{I_{o}} + S_{f_{sw}}^{I_{\varpi}}$$

(2.21)

Where $S^{I_{\Psi_1}}_{f_{sw}}$: is the change in the input current as a result of all conduction losses in DCM under one f_{sw} step. $S^{I_\mu}_{f_{sw}}$: is the change in the input current as a result of control MOSFET conduction losses in DCM under one f_{sw} step. $S^{I_\nu}_{f_{sw}}$: is the change in the input current as a result of synchronous MOSFET conduction losses in DCM mode under one f_{sw} step. $S^{I_o}_{f_{sw}}$: is the change in the input current as a result of Inductor conduction losses in DCM mode under one f_{sw} step. $S^{I_\varpi}_{f_{sw}}$: is the change in the input current as a result of the sense resistor conduction losses in DCM mode under one f_{sw} step. The sensitivity for each conduction loss using the gradient is computed as:

$$S^{I_\mu}_{f_{sw}} = \frac{\partial(\frac{P_\mu}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{\sqrt{2}}{3I_{in}} \cdot \frac{I_{out}^2 V_{out} R_{sw}}{\sqrt{\frac{I_{out} V_{in}^5 L f_{sw}}{V_{out}(V_{in}-V_{out})}}} \tag{2.22}$$

$$S^{I_\nu}_{f_{sw}} = \frac{\partial(\frac{P_\nu}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{\sqrt{2}}{3I_{in}} \cdot \frac{I_{out}^2 (V_{in}-V_{out}) R_{sr}}{\sqrt{\frac{I_{out} V_{in}^5 L f_{sw}}{V_{out}(V_{in}-V_{out})}}} \tag{2.23}$$

$$S_{f_{sw}}^{I_o} = \frac{\partial(\frac{P_o}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{\sqrt{2}}{3I_{in}} \cdot \frac{I_{out}^2 R_L}{\sqrt{\frac{I_{out} V_{in}^3 L f_{sw}}{V_{out}(V_{in}-V_{out})}}}$$

(2.24)

$$S_{f_{sw}}^{I_\varpi} = \frac{\partial(\frac{P_\varpi}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = -\frac{\sqrt{2}}{3I_{in}} \cdot \frac{I_{out}^2 R_{sense}}{\sqrt{\frac{I_{out} V_{in}^3 L f_{sw}}{V_{out}(V_{in}-V_{out})}}}$$

(2.25)

Where P_μ : is the control MOSFET conduction power losses in DCM mode, P_ν : is the synchronous MOSFET conduction power losses in DCM mode, P_o : is the inductor conduction power losses in DCM mode, P_ϖ : is the sense resistor conduction power losses in DCM mode.

2.3.1.4 Sensitivity for Switching Losses in DCM Mode

By computing the gradient for the switching losses in DCM mode, the sensitivity for switching losses in DCM can be given by:

$$S_{f_{sw}}^{I_{\Psi_2}} = S_{f_{sw}}^{I_\vartheta} + S_{f_{sw}}^{I_\rho} + S_{f_{sw}}^{I_\sigma} + S_{f_{sw}}^{I_\varsigma}$$

(2.26)

Where $S_{f_{sw}}^{I_{\Psi_2}}$: is the change in the input current as a result of all switching losses in DCM under one f_{sw} step. $S_{f_{sw}}^{I_\vartheta}$: is the change in the input current as a result of control

MOSFET turn OFF switching losses in DCM under one f_{sw} step. $S_{f_{sw}}^{I_\rho}$: Is the change in the input current as a result of synchronous MOSFET turn ON switching losses in DCM under one f_{sw} step. $S_{f_{sw}}^{I_\sigma}$: Is the change in the input current as a result of MOSFET output capacitance switching losses in DCM under one f_{sw} step. $S_{f_{sw}}^{I_\varsigma}$: is the change in the input current as a result of driving losses in DCM under one f_{sw} step. The sensitivity for each conduction loss using the gradient is computed as:

$$S_{f_{sw}}^{I_\vartheta} = \frac{\partial(\frac{P_\vartheta}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{2\sqrt{2}I_{in}Ig_{off}} \sqrt{\frac{Q_{sw}^2 I_{out} f_{sw} V_{out}(V_{in}-V_{out})}{V_{in}L}} \tag{2.27}$$

$$S_{f_{sw}}^{I_\rho} = \frac{\partial(\frac{P_\rho}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{t_{rise\_sr}}{2\sqrt{2}I_{in}} \cdot \sqrt{\frac{V_D^2 I_{out} f_{sw} V_{out}(V_{in}-V_{out})}{V_{in}^3 L}} \tag{2.28}$$

$$S_{f_{sw}}^{I_\sigma} = \frac{\partial(\frac{P_\sigma}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{1}{2}(Q_{oss\_sw} + Q_{oss\_sr}) \cdot \frac{f_{sw}}{I_{in}} \tag{2.29}$$

$$S_{f_{sw}}^{I_\varsigma} = \frac{\partial(\frac{P_\varsigma}{V_{in}})}{\partial f_{sw}} \cdot \frac{f_{sw}}{I_{in}} = \frac{2Q_{gsw}V_g f_{sw}}{V_{in}I_{in}}$$

(2.30)

Where P_ϑ: is the control MOSFET turn OFF switching power losses in DCM, P_ρ: is the synchronous MOSFET turn ON switching power losses in DCM, P_σ: is the MOSFET output capacitance switching power losses in DCM, P_ς: is the driving power losses in DCM . From the above, the input current sensitivity for total losses in DCM is:

$$S_{f_{sw}}^{I_{\Psi total}} = S_{f_{sw}}^{I_{\Psi 1}} + S_{f_{sw}}^{I_{\Psi 2}}$$

(2.31)

Where $S_{f_{sw}}^{I_{\Psi total}}$: is the change in the input current as a result of all switching and conduction losses in DCM under one f_{sw} step.

From the above analysis, the synchronous buck DC-DC converter, input current sensitivity to changes in input current can be calculated as:

$$S_{f_{sw}}^{I_{in}} = \begin{Bmatrix} S_{f_{sw}}^{I_{\Phi total}}, & CCM \\ S_{f_{sw}}^{I_{\Psi total}}, & DCM \end{Bmatrix}$$

(2.32)

The minimum frequency change that can be used given certain hardware limitations can be calculated as follows: First, the minimum change the ADC can sense is given in Equation (2.33) as follow:

$$ADC_{LSB} = \frac{V_{ADC\_MAX}}{2^{N_{ADC}}} \tag{2.33}$$

Where ADC_{LSB} is the minimum voltage change the ADC can sense, V_{ADC_MAX} is the ADC maximum sensed voltage and N_{ADC} is the ADC number of bits. For the AFO experimental step of this chapter presented in Section 2.6, the input current is sensed using a 12 bits ADC with $V_{ADC\_MAX} = 3.3\text{V}$:

$$ADC_{LSB} = \frac{3.3}{2^{12}} = 0.806 \times 10^{-3} V$$

If the current sensing circuitry is using a 5mΩ sensing resistor with current sensing op-amp gain set to 100 V/V, the minimum input current change that cause a 0.806mV change can be calculated as:

$$I_{in\_min} \times R_{sense} \times Gain = ADC_{LSB}$$
$$I_{in\_min} \times (5 \times 10^{-3}) \times 100 = 0.806 \times 10^{-3}$$
$$I_{in\_min} = 1.6 \times 10^{-3} A$$

The minimum switching frequency change that cause the minimum input current change I_{in_min} can be calculated using Equation (2.34):

$$f_{sw\_min} = \frac{I_{in\_min}}{\nabla I_{in}} \tag{2.34}$$

Using Equation (2.34) and based on the power stage specifications that are given in the experimental work of Section 2.6, the minimum change in switching frequency is calculated to be 6.380 kHz. Therefore, the step size should be selected to be larger than 6.380 kHz. This value was selected to be 10 kHz for the experimental prototype.

2.3.2 P_e Selection

P_e is defined as the minimum input power change required to activate the AFO loop. As shown in Fig. 2.4, the difference in input power between two samples is first compared if this difference is greater than a certain threshold P_e the AFO adaptive loop is activated, else, the AFO algorithm will just wait and do nothing. This condition is optional and can be replaced by a delay time that periodically activates the AFO. This threshold comparison serves two purposes [26]: First it reduces oscillation between two values when there is no descent change in input power, and second, it minimizes the noise effect [2]. The selection of P_e depends on the selected step size: f_{sw_step} and can be calculated from equation (2.35) as follow:

$$P_e = \nabla I_{in} \cdot f_{in\_\min} \cdot V_{in}$$

(2.35)

Using the power stage specification, and assuming that the input voltage $V_{in} = 10V$ and that the switching frequency step-size is $f_{sw\_step} = 10\ kHz$, the input power threshold P_e can be calculated from Equation (2.35) and is equal to 3.1 mW or 0.31mA at 10V fixed input voltage. It should be noted that the design equations discussed above are used as a guide line to find an initial value for the step size and Pe, more exact values was found through out the experiment.

2.3.3 M Selection

A delay of *M* switching cycles between each increment/decrement of the switching frequency is required to ensure that the new input power/input current is sampled after the frequency change transient effect has passed. The closed loop compensator takes some time, the settling time, to settle the system to it new steady state condition. This transient settling time value is very negligible especially when the step size is small, however, it should be taken into account. The delay time (*M* switching cycles) is usually selected to be much larger than the settling time value. For the experimental setup described in Section 2.6, the settling time was selected to be $M = 5$ switching cycles, which was sufficient based on this chapter loop design (see Section 2.4 for bode-plots of the closed loop design). One important note here is that AFO algorithm will only work when the load is

changing at frequency less than M. In other words, AFO will work with slowly varying loads. It should be noted also that since the adaptive loop is running at much slower bandwidth than the closed loop, this means that the AFO effect on system stability is minimal.

2.4 Loop Gain-Phase Design Considerations

Fig. 2.5 shows the block diagram of a digitally controlled synchronous Buck DC-DC converter. For a digitally controlled converter the output voltage is sampled using an ADC and compared to a programmable reference internal to the digital controller [12-26]. This is done before it is applied to the digital PID compensator that will generate the required duty-cycle to the digital pulse width modulation (DPWM) unit. The DPWM unit generates the PWM signals with the correct frequency and duty cycle to the driver of the DC-DC converter. The sensed output voltage can also be used to protect the DC-DC converter by shutting down the PWM signals when an over voltage condition occurs.

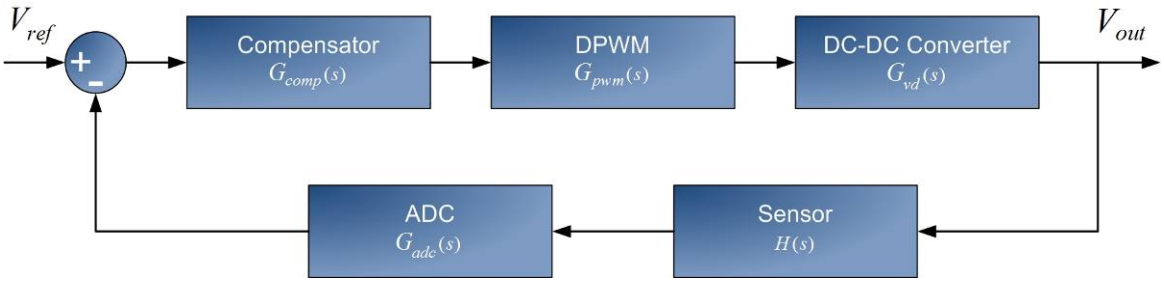


Fig. 2.5: Block-diagram of a digitally controlled closed loop synchronous buck converter.

According to control theory, there are two closed loop design methods that can be used to design the digital controller [15]: The first method is the direct digital design, where a discrete time model of the system is first obtained then the controller is directly designed in the z-domain using famous methods like frequency response bode plots, or root locus method. Direct digital design has the advantages of better system response and the ability to achieve better phase and gain margins [15,16,19]. The other design method is the digital redesign where the controller is first designed in continuous time domain (s-domain) then transformed to z-domain using well known discretization methods [15,16]. Digital redesign has the advantages of easier design process and the ability to apply known analog controller design techniques [15]. For both design methods an accurate model for the different systems blocks must be first obtained [14, 22].

Table 2.1 shows a summary of continuous time models for different blocks of digitally controlled buck converter, where V_{in} is the input voltage, R_o is the load resistance which equals to V_o / I_o, L is the output inductor, R_L is the output inductor equivalent series resistance (DCR), C_o is the output capacitance, R_C is the output capacitor equivalent series resistance (ESR), T_{samp} is the sampling time, K_{adc} is the ADC gain, T_{adc} is the delay caused by the ADC conversion time, $V_{\max_{adc}}$ is the maximum voltage range that the ADC can sense, N_{adc} is the ADC resolution or number of bits, K_{pwm} is the DPWM gain, T_{pwm} is the delay caused by the DPWM, N_{pwm} is the DPWM resolution or number of bits, $H(s)$ is the output voltage sensor gain, $L(s)$ is

the system open loop gain, $C(s)$ is the closed loop voltage reference to output voltage transfer function, and $G_{comp}(s)$ is the conventional PID compensator transfer function. Matched Z transform [15] was used to get the discrete time model of the complete system. The equations summarized in Table 2.1 are used next in the discussion design example.

Table 2.1: A summary of continuous time models for different blocks of digitally controlled buck converter

Buck DC-DC converter model working CCM	$G_{vd}(s) = \frac{\hat{V}_o}{\hat{d}}(s) = \frac{(\frac{V_{in}R}{R+R_L})(1+s\cdot R_C\cdot C)}{1+s\left[C(R_C+\frac{R\cdot R_L}{R+R_L})+\frac{L}{R+R_L}\right]+s^2\left[\frac{LC(R+R_C)}{R+R_L}\right]}$	(2.36)
Buck DC-DC converter model working DCM	$G_{vd}(s) = \frac{\hat{V}_o}{\hat{d}}(s) = \frac{2V_o}{\sqrt{\frac{2\cdot L\cdot f_s\cdot M^2}{R\cdot(1-M)}}}\cdot\frac{(1-M)}{(2-M)+s\cdot R\cdot C\cdot(1-M)}$	(2.37)
Analog to Digital converter ADC model	$G_{adc}(s) = K_{adc}e^{-sTadc} = \frac{1}{LSB}\cdot e^{-sTadc}$	(2.38)
Pulse width modulation PWM model	$G_{pwm}(s) = K_{pwm}e^{-sTpwm} = \frac{1}{2^{N_{pwm}}-1}\cdot e^{-sTpwm}$	(2.39)
Zero Order Hold	$\frac{1-e^{-sT_{samp}}}{sT_{samp}}$	(2.39.a)
Dealy	$e^{-sT_{samp}}$	(2.39.b)
output voltage V_o sensor gain	$H(s) = \frac{V_{ref}}{V_{out}}$	(2.40)
System Open loop	$L(s) = G_{adc}(s)\cdot G_{vd}(s)\cdot G_{pwm}(s)\cdot H(s)$	(2.41)
System closed loop reference to output	$C(s) = \frac{G_{comp}(s)\cdot G_{pwm}(s)\cdot G_{vd}(s)}{1+G_{comp}(s)\cdot G_{pwm}(s)\cdot G_{vd}(s)\cdot G_{adc}(s)\cdot H(s)}$	(2.42)

Fig. 2.6 shows a conceptual block diagram for a digital pulse width modulator (DPWM), in which an internal oscillator feeds a quantizer block where the oscillator frequency f_s or time T_s is divided into a discrete number of time slots each of length t_d. The selection of a particular time slot is made through the control word $d[n]$ [45-49]. Changing the switching frequency of the DPWM can be performed by dividing the oscillator frequency by a number programmed in a register in the digital controller. This number also determines the total number of duty cycle steps over one switching cycle. The new switching frequency can be given by Equation (2.43) as follows [46]:

$$f_{PWM} = \frac{f_{osc}}{\text{Register}[0{:}\text{N}_{\text{steps}}]+1} \tag{2.43}$$

Where f_{PWM} is the DPWM switching frequency ($f_{PWM} = f_{sw}$), f_{osc} is the DPWM oscillator clock frequency, N_{steps} is the number programmed the divider register. Note that it is assumed here that the DPWM is implemented in a counter-based architecture [45], for discussion purposes Other possible architectures are such as delay-line and hybrid architectures [23, 45-48].

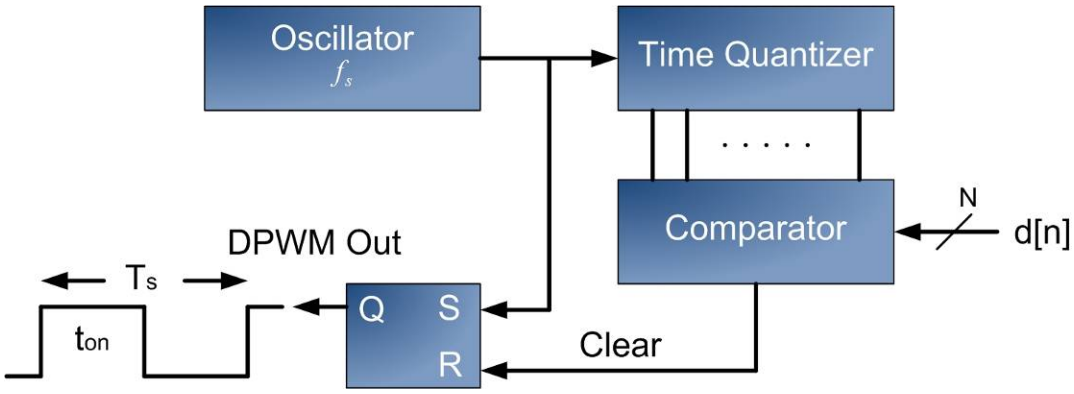


Fig. 2.6: Conceptual block diagram of the DPWM unit [32].

Based on the Equation (2.43), in order to achieve higher switching frequencies, the total number of steps need to be reduced and hence the effective resolution of the DPWM, N_{pwm}, is reduced. Reducing the effective DPWM resolution increases the DPWM gain as given by Equation (2.39) in Table 2.1. Changing the DPWM gain, K_{pwm}, changes the total system gain, which results in performance change in the closed loop system, which may cause the system to run into instability. This effect does not exist in analog controllers since the PWM resolution does not change with switching frequency.

A synchronous buck converter closed loop is simulated (using Table 2.1 equations and Fig. 2.5 models), which has the same hardware specifications as in Section 2.6, to investigate the effect of variable switching frequency. The switching frequency is varied from 100 kHz to 700 kHz in digitally controlled buck converter. Fig. 2.7 shows the effect of changing the switching frequency in CCM and Fig. 2.8 shows the effect of changing the switching frequency in DCM. From Fig. 2.7, it can be noticed that varying the switching frequency in CCM using digitally controlled converter has changed the crossover

frequency (from 18 kHz at f_{sw}=100 kHz to 106 kHz at f_{sw} =700 kHz for this design example) and also has changed the phase margin (from 48.5^o at f_{sw} =100 kHz to 40.5^o at f_{sw} =700 kHz).

From the above discussion, when designing a compensator for the variable switching frequency digital controller, the controller should also be designed to have a good phase margins that ensures stability over the entire switching frequency range, in addition to having a good phase and gain margins for different input voltages and loads. Next section discusses another issue resulting from varying the switching frequency digitally, the limit cycle oscillation issue, and an adaptive technique to alleviate these issues is presented.

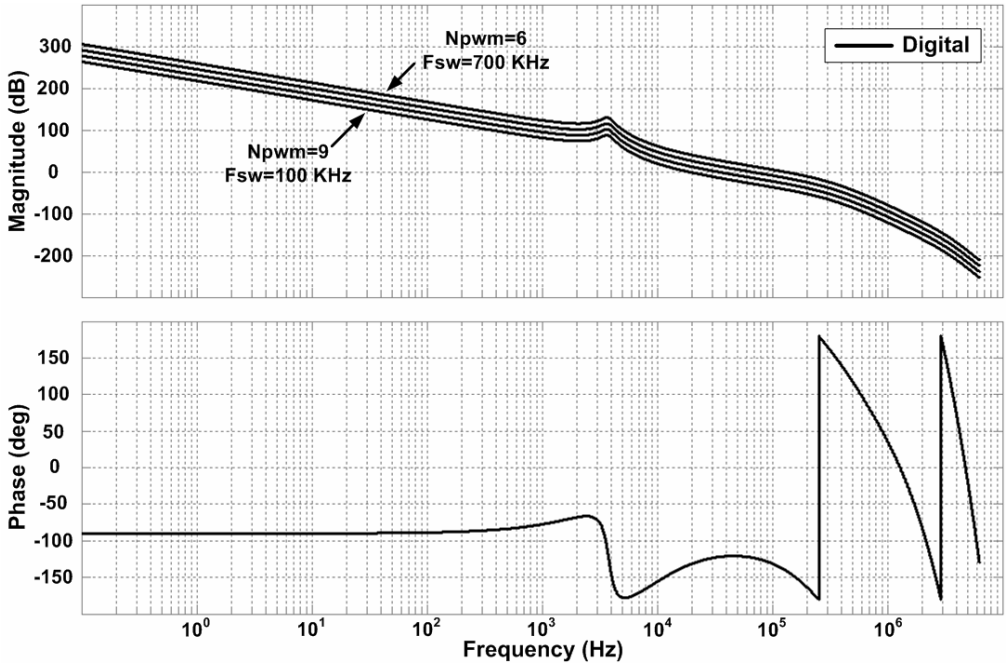


Fig. 2.7: Digital variable switching frequency (by varying DPWM number of steps) effect in CCM mode

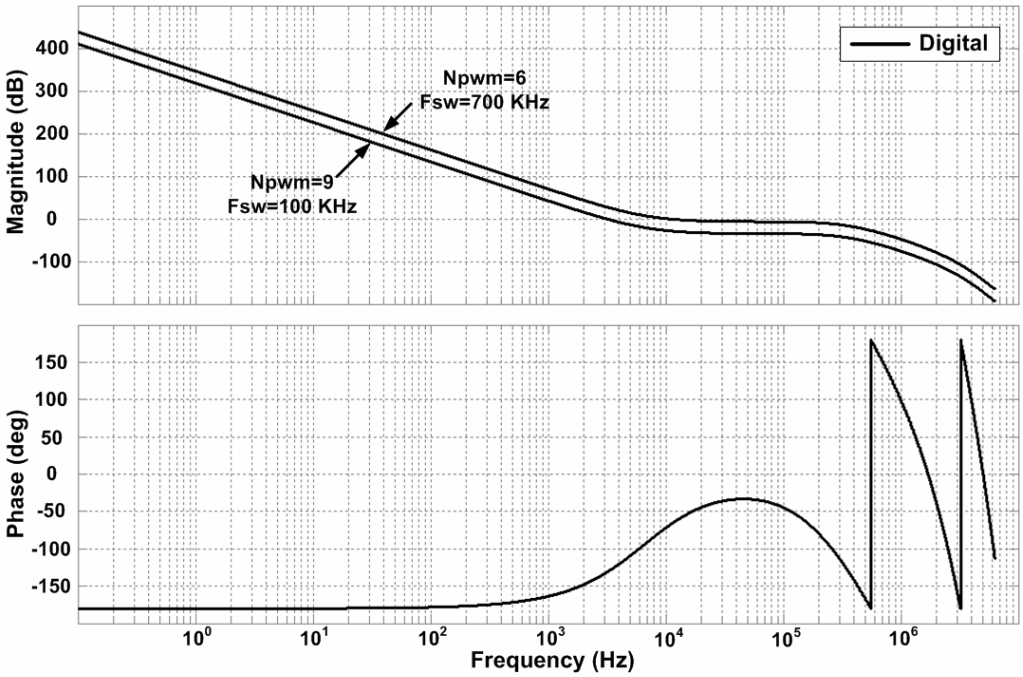


Fig. 2.8: Digital variable switching frequency (by varying DPWM number of steps) effect in DCM mode

2.5 Limit-Cycle Considerations and Proposed Dynamic Algorithm

Limit-cycle is undesired oscillation at the output of the DC-DC converter V_{out} at frequencies lower than the converter's switching frequency f_{sw} [19, 49-59]. The DPWM block generates a discrete number of duty cycle values, and if the output voltage does not correspond to one of those values, the feedback controller will oscillate between two or more discrete duty cycle values, which cause the output voltage to oscillate in what is known as limit cycle oscillation. For a fixed frequency DPWM, the limit cycle oscillation can be avoided by making sure that the output voltage change resulted from one LSB change in the duty cycle of the DPWM is smaller than the analog equivalent of the LSB of

the ADC [19]. In other words, the resolution of the DPWM should be always higher than the resolution of the ADC [53]. An exact relation for the minimum required resolution for the DPWM unit for a buck converter is given in Equation (2.44) [19]:

$$N_{PWM} \geq \text{int}\left[N_{adc} + \log_2\left(\frac{V_{ref}}{V_{\max_{adc}} \cdot D} \right) \right] \tag{2.44}$$

Where V_{ref} is the closed loop reference voltage and the rest of parameters where defined earlier in the chapter. To achieve the output voltage regulation requirement, the ADC must sense voltage changes smaller than the variation in the output voltage ΔV_o. The resolution of the ADC is given in Equation (2.45) [19]:

$$N_{adc} \geq \text{int}\left[\log_2\left(\frac{V_{\max_{adc}}}{V_{ref}} \cdot \frac{V_o}{\Delta V_o} \right) \right] \tag{2.45}$$

For a variable frequency digital controller that varies the switching frequency to achieve the optimum efficiency, the DPWM resolution will also vary since the total number of DPWM steps that controls the switching frequency changes. For example, when changing the switching frequency from 100 kHz to 800 kHz in a digital controller that uses a 50 MHz DPWM oscillator and a 9 bit DPWM register, the DPWM resolution changes from 9 bits to 6 bits. Therefore, optimizing the system resolution at switching frequency of 100 kHz to avoid limit cycle does not guarantee the elimination of limit cycle oscillation at all other switching frequencies.

The need arises for adding another functionality to the AFO, and therefore, the Dynamic Limit Cycle Algorithm (DLCA) is presented in this section. The DLCA is a simple control algorithm that dynamically varies the ADC resolution as the switching frequency changes to avoid limit cycle oscillation, and at the same time, reduces the gain and phase changes discussed in the previous section [25]. Fig. 2.9 shows the dynamic limit cycle controller flowchart. Note that the algorithms of Fig. 2.4 and Fig. 2.9 form one completed algorithm as shown next in this chapter and in Fig. 2.13.

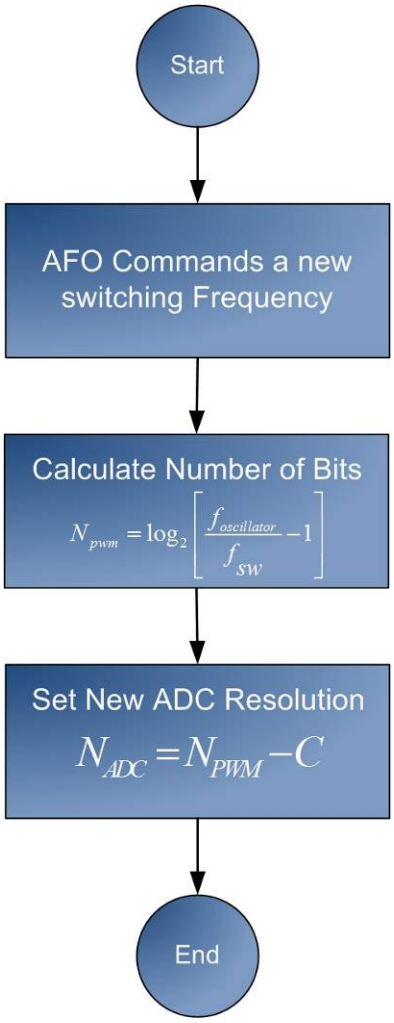


Fig. 2.9: Dynamic limit cycle controller algorithm flowchart.

The DLCA algorithm starts by taking the new required switching frequency value from the AFO adaptive loop that determines the best switching frequency to optimize the efficiency. The first step is calculating the required number of steps and the DPWM resolution N_{PWM} to achieve the new commanded frequency at a certain PWM oscillator. From this value the algorithm calculates the new ADC resolution value to avoid the limit cycle as shown in Fig. 2.10 (a). Fig. 2.10 (b) shows the required ADC resolution to avoid

the limit cycle problem at different input voltages and Fig. 2.10 (c) shows a surface plot of the switching frequency vs. the input voltage vs. the ADC required number of bits in order to avoid limit cycle. It can be noted from Fig. 2.10 that the required change in ADC resolution to avoid limit cycle over a wide frequency range is small, Maximum 2 bits in the frequency range 100 kHz to 500 kHz, and thus the effect of DLCA on dynamic behavior is minimal.

The ADC resolution is adjusted by changing the threshold voltage between neighboring ADC output states so that the ADC resolution is lower than the DPWM resolution. The threshold voltage is adjusted by controlling the ADC reference voltage which is controlled by a DAC (Digital to Analog Converter). The ADC reference voltage can be changed by adjusting the DAC output by changing the digital word controlling the DAC. For example for a 10 bits ADC, if the DLCA calculated that the ADC required number of bits to avoid limit cycle is 8 bits, the digital controller, commanded by the DLCA, will write a new digital word to the DAC so that the ADC threshold voltage is adjusted to the appropriate new value. These DAC digital words are stored in a look-up table with their corresponding resulted number of bits for the ADC.

This will result in eliminating the limit cycle oscillation. It will not affect the steady-state output voltage ripple since it is a function of the switching frequency, output filter, the input voltage, and the output voltage and not a function of the ADC resolution. However, lower ADC resolution may have an impact on the dynamic output voltage deviation. Note that, using the DLCA, lower ADC resolution is used at higher switching

frequencies while higher ADC resolution is used at lower switching frequencies. Therefore, the dynamic response requirements can be satisfied with appropriate design.

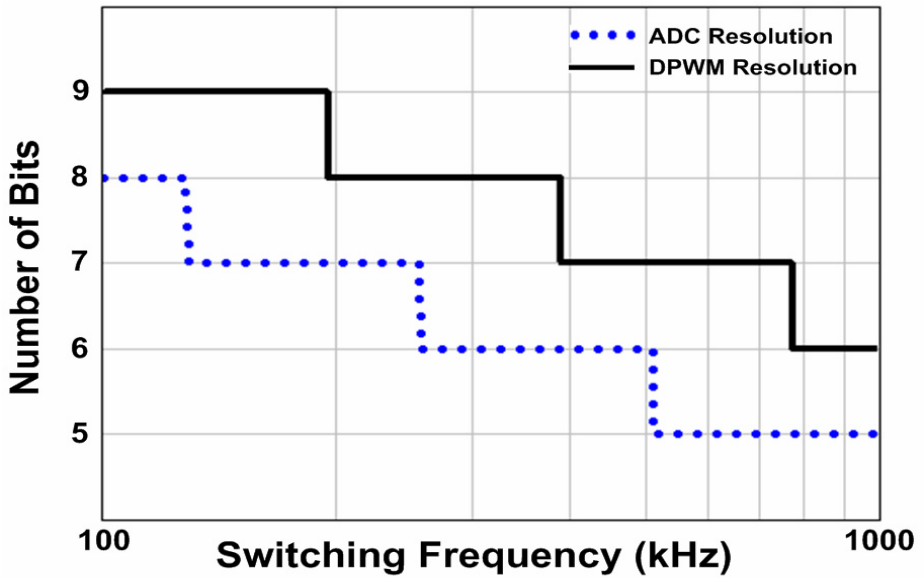


Fig. 2.10 (a): DPWM and ADC required resolution to avoid limit-cycle at different switching frequencies with nominal input voltage of 10V.

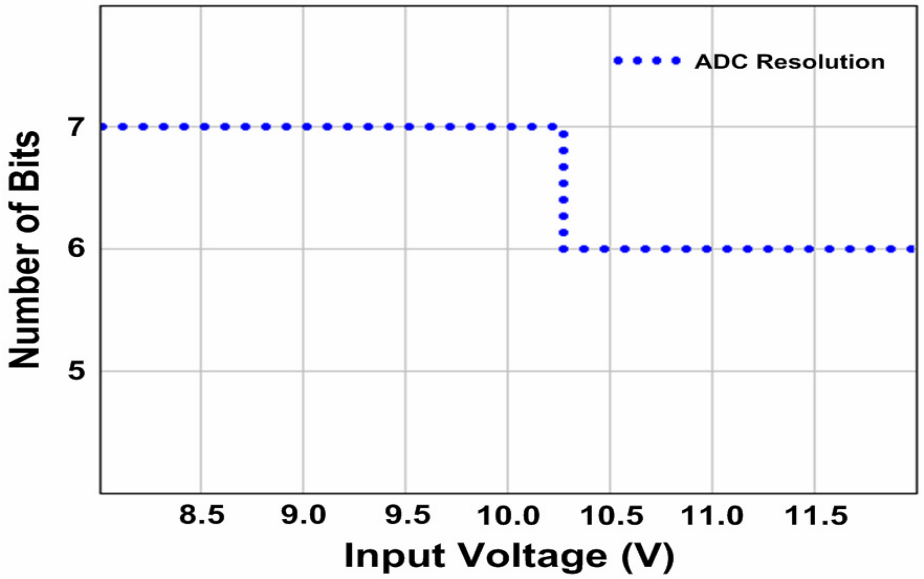


Fig. 2.10 (b): ADC required resolution to avoid limit-cycle at different input voltages with switching frequency = 250 kHz.

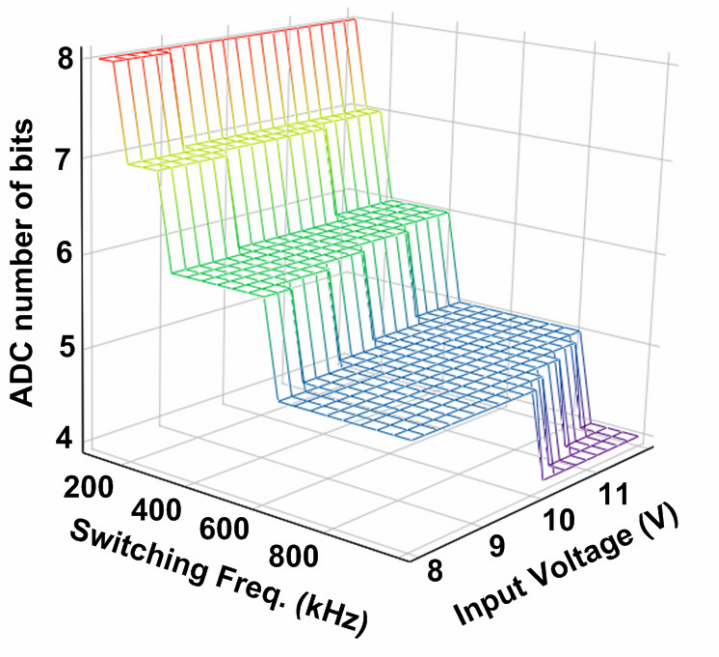


Fig. 2.10 (c): ADC required resolution to avoid limit-cycle at different frequencies and input voltages

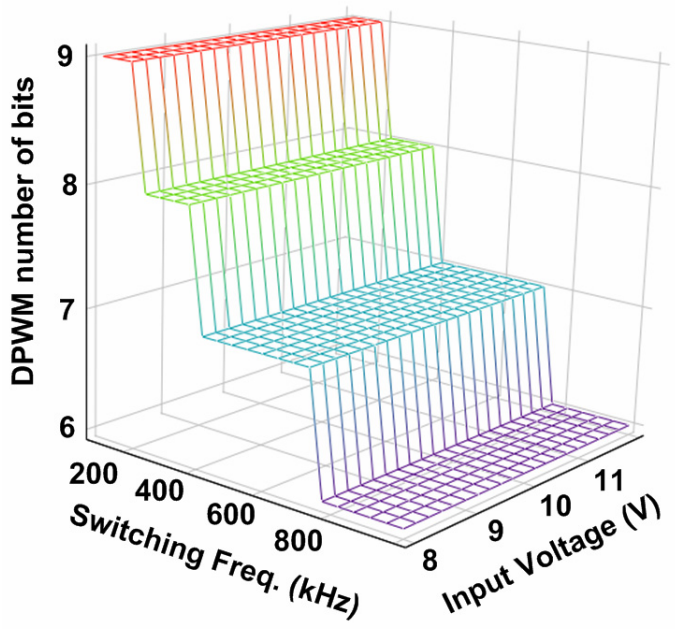


Fig. 2.10 (d): DPWM required resolution to avoid limit-cycle at different frequencies and input voltages

The constant C in Fig. 2.9 is calculated using Equation (2.46) with the knowledge of the duty cycle D which is available internally to the digital controller, as follows:

$$C \geq \log_2\left(\frac{V_{ref}}{V_{\max_{adc}} \cdot D}\right) \tag{2.46}$$

Note that Equation (2.46) does account for any change in the conversion ratio or input voltage. Hence, there are two choices for calculating C, the first is calculating C once at worst case condition such as minimum input voltage value, and the second is continuously calculating C base on the new D value.

Another major advantage of the DLCA controller is reducing the crossover frequency variations when varying the switching frequency, which makes the compensator design much easier and helps in achieving more stable system. For the same design that is simulated in Fig. 2.7 and Fig. 2.8, Fig. 2.11 and Fig. 2.12 show the simulated results when the DLCA is used, respectively. It can be noted from the figures that the crossover frequency variation is much more less with the DLCA especially at high switching frequencies, for both CCM and DCM operations.

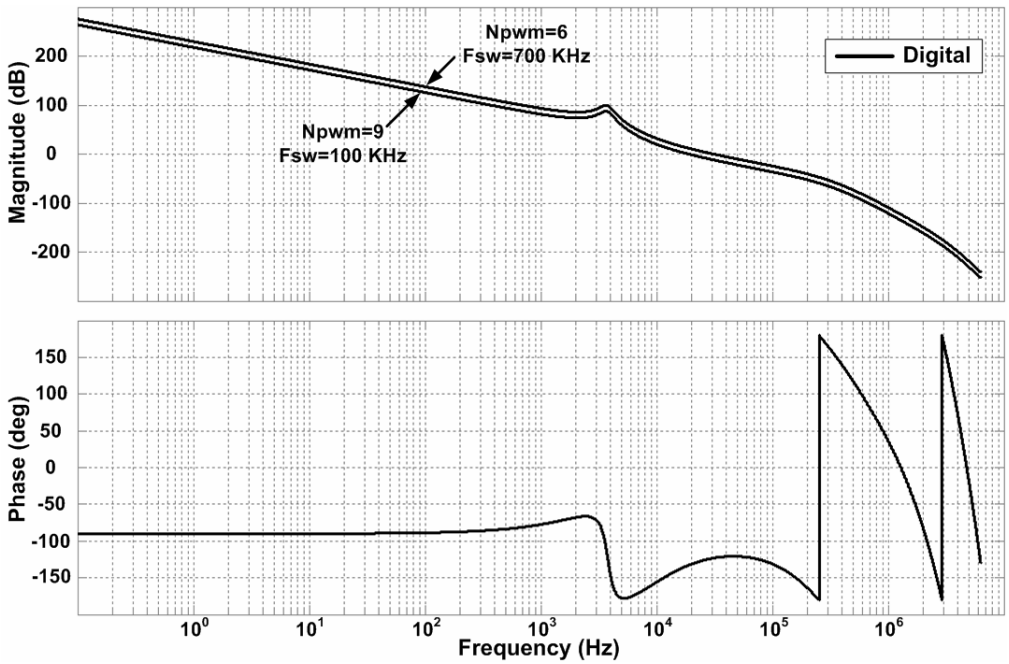


Fig. 2.11: Bode-Plots in CCM with the DLCA controller

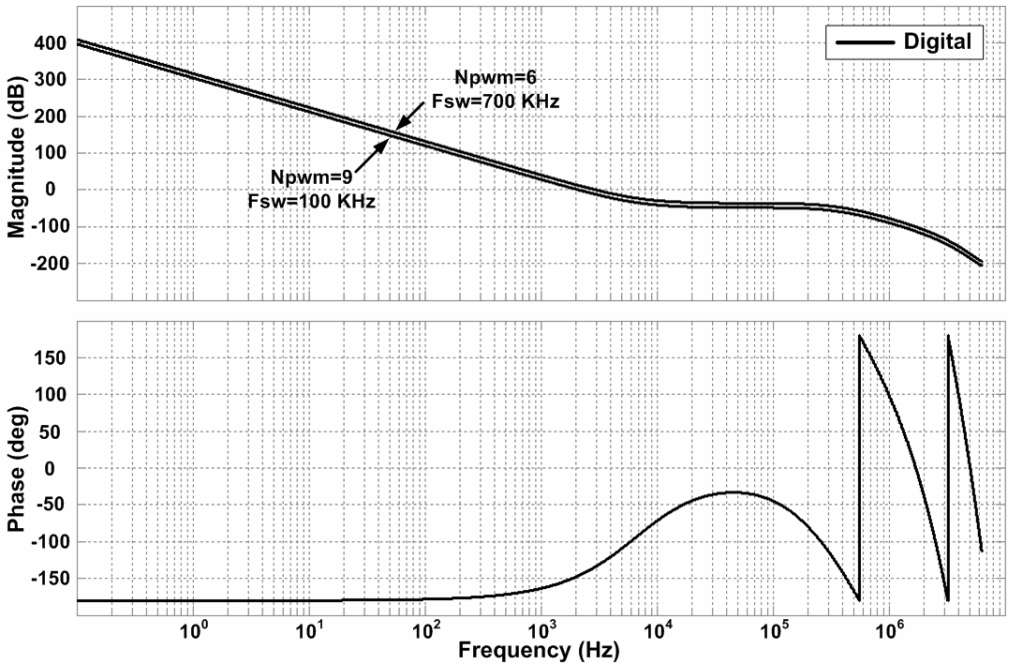


Fig. 2.12: Bode-Plots in DCM with the DLCA controller

2.6 Experimental Work

The AFO and DLCA methods are prototyped in a digital controller for a proof of concept purposes. The complete algorithm flowchart that includes both techniques is shown in Fig. 2.13. The experimental power stage setup is a single phase synchronous buck DC-DC converter with $V_{in} = 10V$, $V_o = 3.3V$, output Inductor: $L_o = 2.6\mu H$ with $DCR = 1m\Omega$, input capacitors $940\mu F$,output capacitors $991\mu F$, synchrnous FET: IRFR5305, two in parallel [60], control FET: IRFR2905, two in parallel [61], and FETs Driver: TC428COA [62]. The digital microcontroller is used to implement both the AFO with DLCA and the output voltage regulation closed loop.

The input power is sensed using two 12-bit ADC's. The converted data is then processed by the digital controller and utilized by the AFO algorithm. Another 12-bit ADC is used to convert the sensed output voltage and then used by a conventional digital PID compensator to regulate the output voltage. Both ADC's has maximum input voltage of 3.3V.

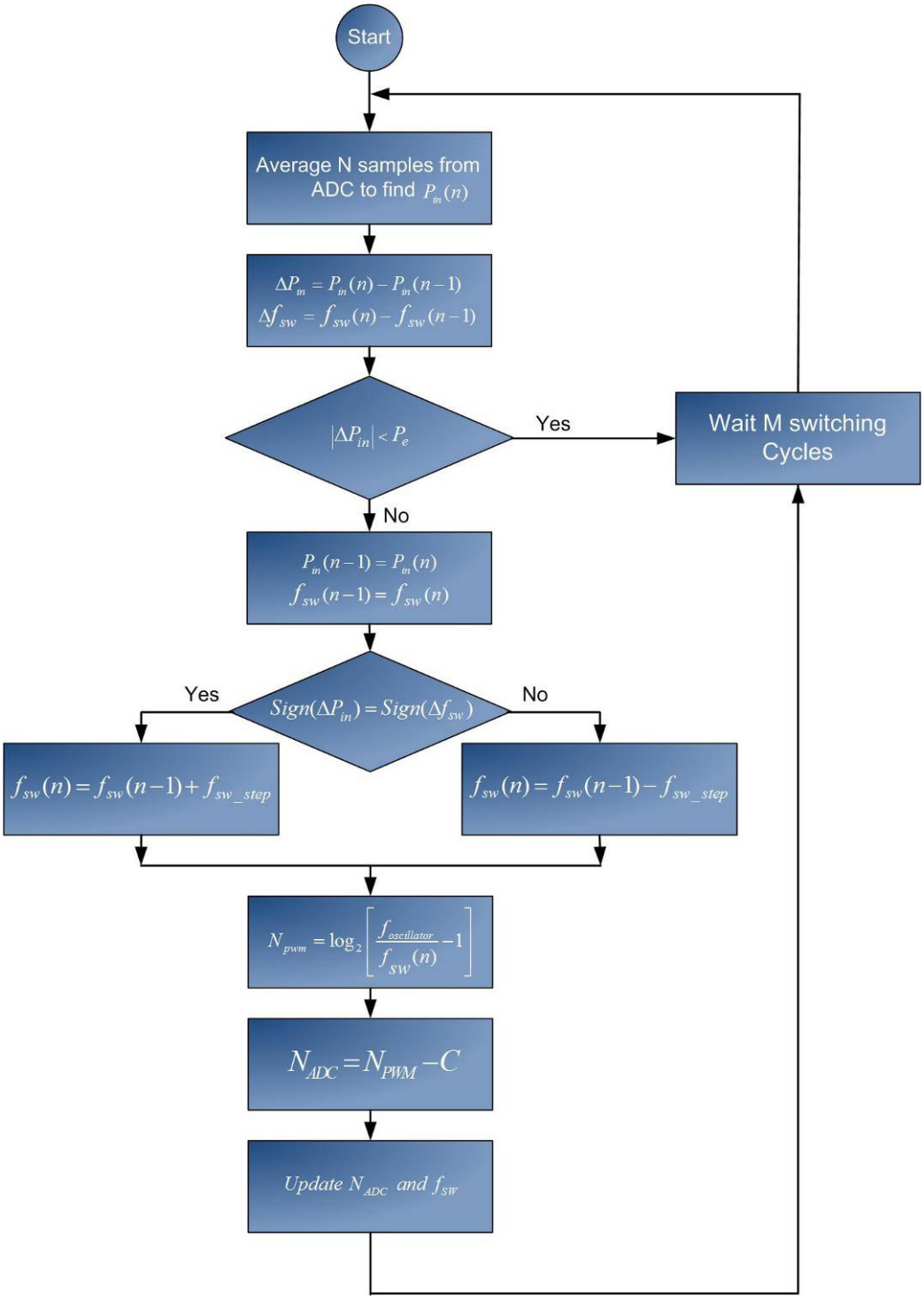
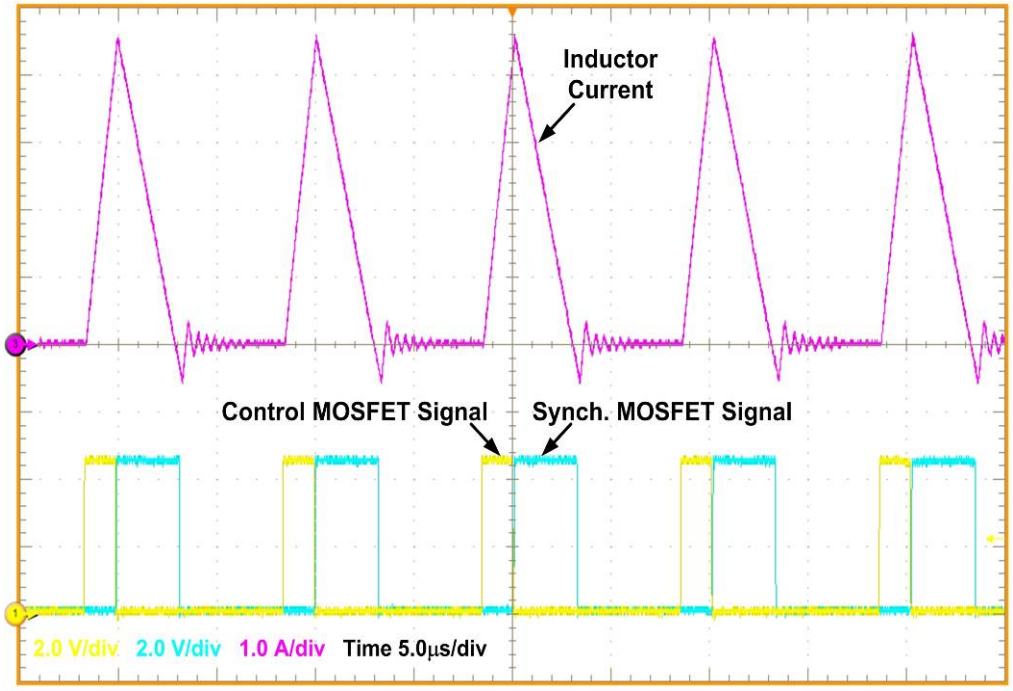
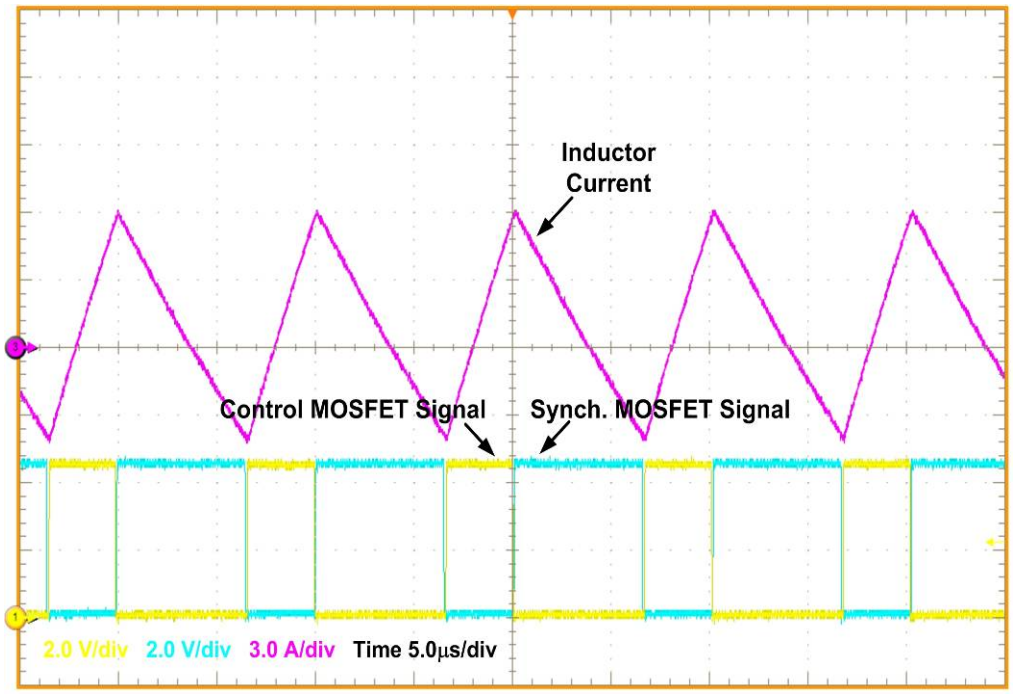


Fig. 2.13: Complete proposed controller algorithm flowchart.

To further improve the efficiency, the system is designed to be able to switch between CCM and DCM modes of operation depending on the load. For this purpose, a current sense circuit that sense inductor current is used. The current sense circuit feeds its measurement to the microcontroller analog comparator, when the inductor current approaches zero, an interrupt signal is generated and the lower side MOSFET signal is disabled to operate in DCM. Fig. 2.14 (a) shows the experimental waveforms for the synchronous buck converter operating in DCM, and Fig. 2.14 (b) shows experimental waveforms for the buck converter operating in CCM.



(a)



(b)

Fig. 2.14: Experimental switching waveforms: (a) in DCM and (b) in CCM.

Fig. 2.15 shows the efficiency versus switching frequency curves obtained from the experimental setup at different loading conditions where the switching frequency is swept across a range at each given load. Fig. 2.16 shows a comparison between efficiency improvements resulted from fixed switching frequency versus the proposed AFO algorithm, as can be noted from the figure, adaptive efficiency optimization achieves the highest efficiency improvement compared to the fixed frequency approach. Now, for each switching frequency, the efficiency is measured by dividing the output power to the input power. The controller power loss is included since it is powered from the same input power source. Table 2.2 demonstrates how the proposed controller detects the new

optimum switching frequency and adjusts it when the input voltage varies from 8V to 10V to 12V. for load currents 0.6A, 1A, 4A and 6A. As the input voltage increases, the optimum switching frequency may go lower or higher depending on the trade off between conduction losses and switching losses. Fig. 2.17 shows the experimental results of the DCLA part of the proposed controller. The experimental waveforms demonstrate how the DCLA eliminated the limit cycle oscillation at different switching frequencies.

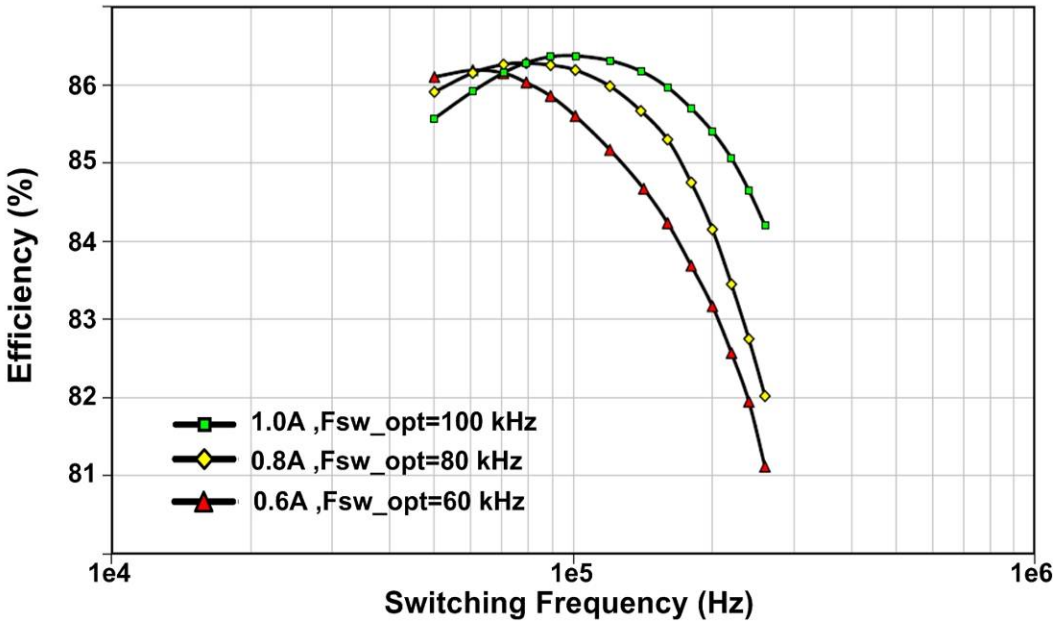


Fig.2.15 (a): Efficiency vs. switching frequency at different loads when DCM is allowed at input voltage of 10V

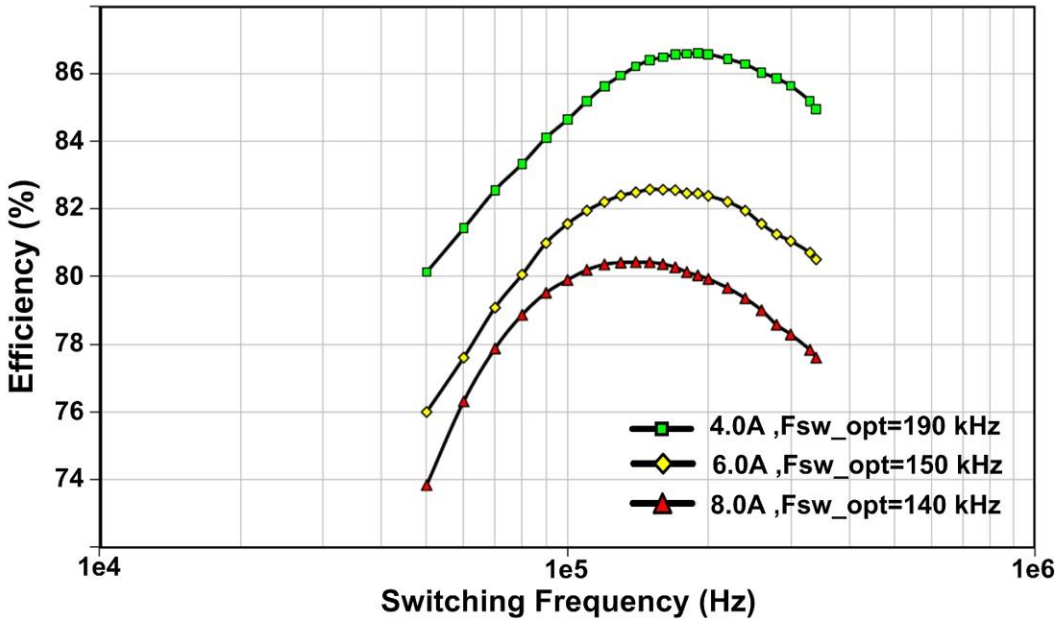
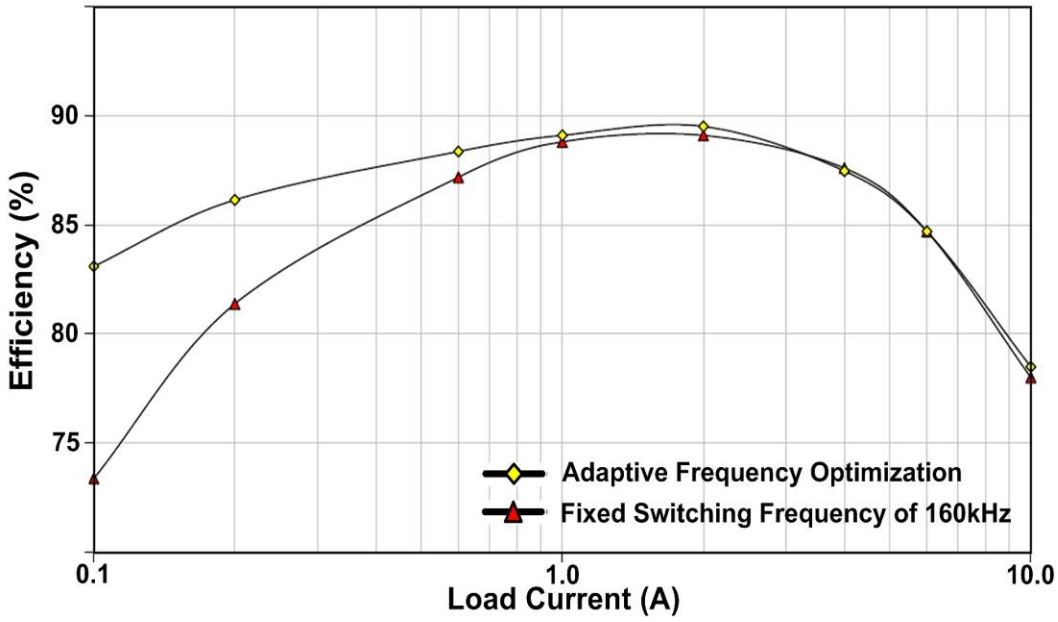
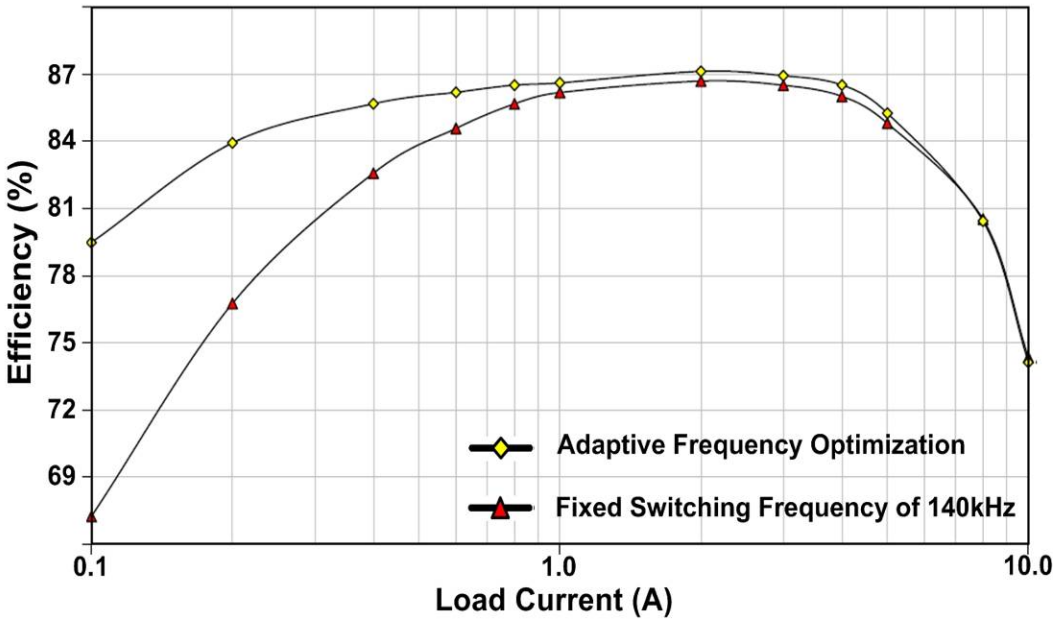


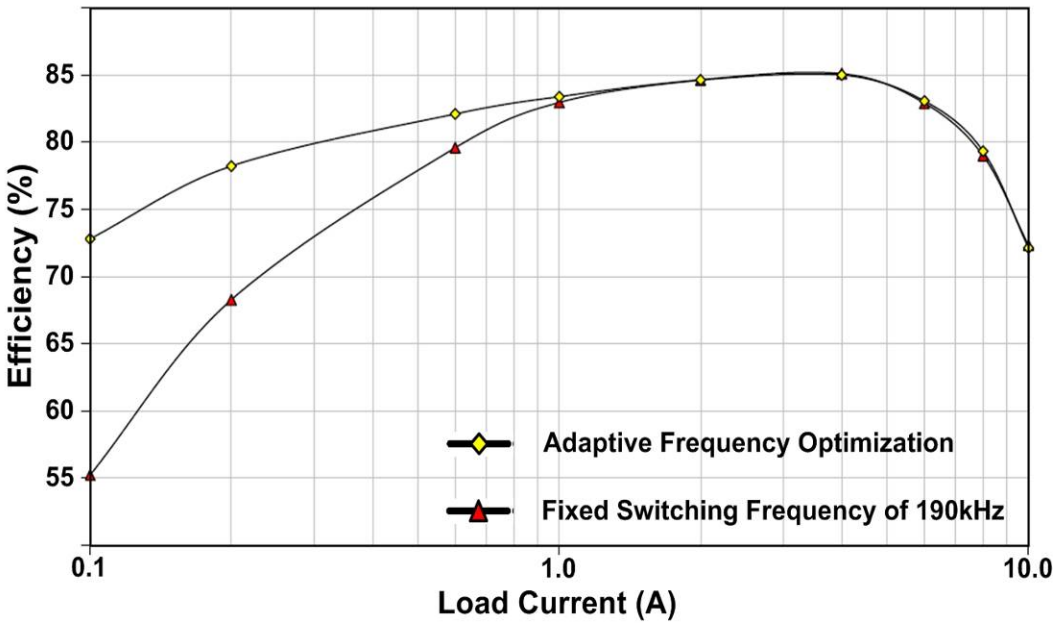
Fig.2.15 (b): Efficiency vs. switching frequency at different loads in CCM when DCM is not allowed at input voltage of 10V



(a)



(b)



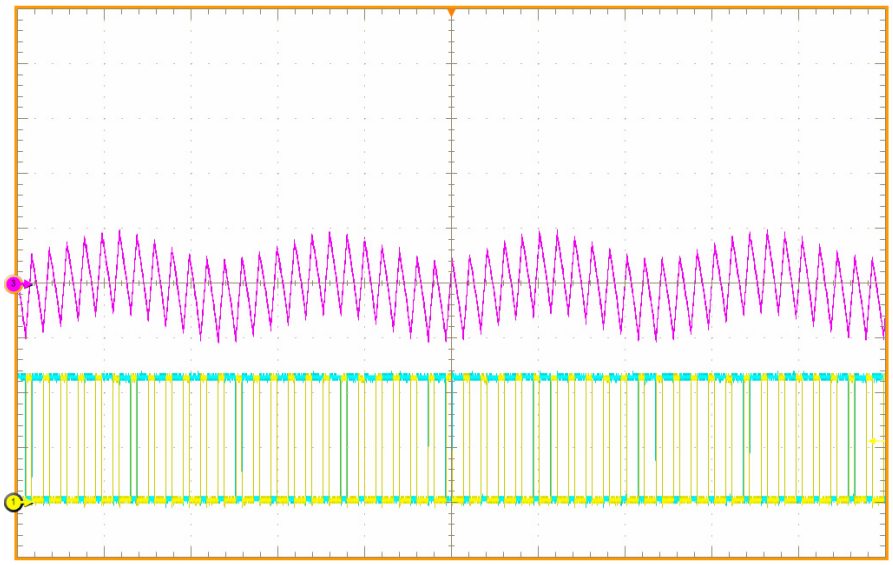
(c)

Fig. 2.16 : Efficiency vs. Load using adaptive frequency Optimization (AFO) algorithm compared to operating at fixed switching frequency with CCM/DCM enabled at input voltage of (a) 8V (b) 10V (c) 12V

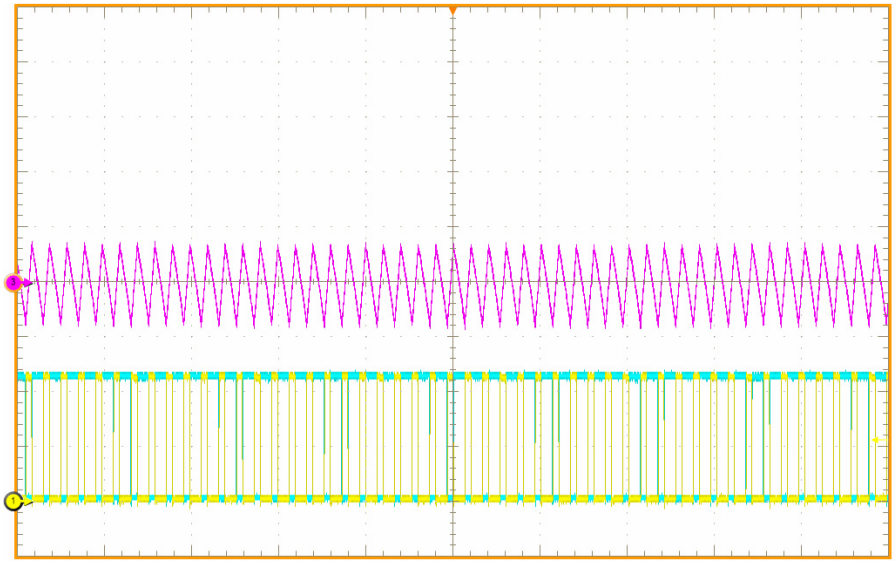
Table 2.2: Optimum switching frequency and efficiency at different input voltages and different load currents

Load	**0.6A**		**1.0A**		**4.0A**		**6.0A**	
Vin	$\mathbf{f_{optimum}}$	**Efficiency**	$\mathbf{f_{optimum}}$	**Efficiency**	$\mathbf{f_{optimum}}$	**Efficiency**	$\mathbf{f_{optimum}}$	**Efficiency**
8.0V	90 kHz	88.36 %	150 kHz	89.10 %	190 kHz	87.47 %	160 kHz	84.70 %
10.0V	60 kHz	86.19 %	100 kHz	86.61 %	190 kHz	86.51 %	150 kHz	82.58 %
12.0V	70 kHz	82.10 %	100 kHz	83.38 %	190 kHz	85.00 %	160 kHz	83.06 %

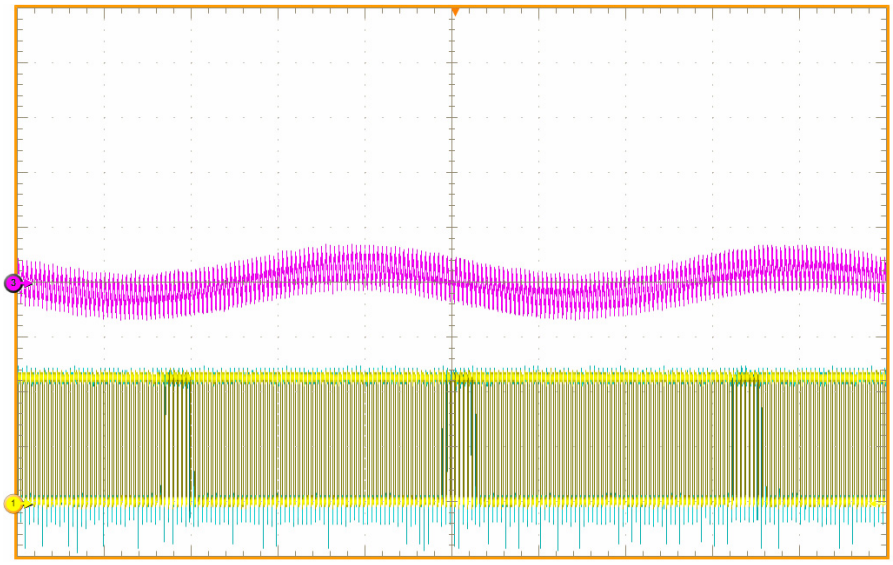
The experimental proof of concept results of this section verified the theoretical and simulation results presented earlier in this chapter. As stated previously, even though the experimental results was for relatively low power converter, more significant improvement is expected in higher power converters.



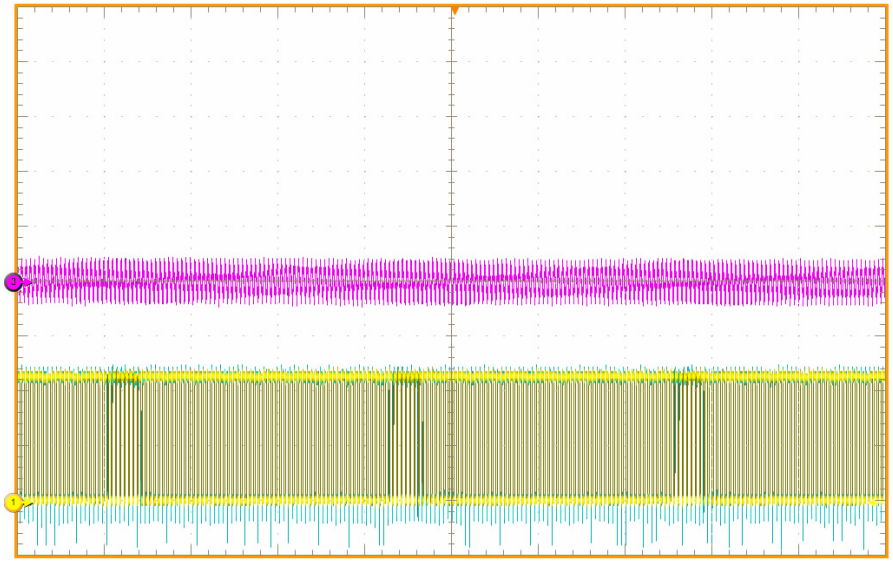
(a) Figure scale $(50\mu s / div.,\ 50mV / div.top,\ 2V / div.bottom)$



(b) Figure scale $(50\mu s / div.,\ 50mV / div.top,\ 2V / div.bottom)$



(c) Figure scale $(100\mu s\,/\,div.,\ 50mV\,/\,div.top,\ 2V\,/\,div.bottom)$



(d) Figure scale $(100\mu s\,/\,div.,\ 50mV\,/\,div.top,\ 2V\,/\,div.bottom)$

Fig. 2.17: (a) Limit cycle oscillation at 100 kHz without the proposed DCLA, (b) No limit cycle oscillation at 100 kHz because of activating the DCLA part of the controller, (c) Limit cycle oscillation at 200 kHz without the proposed DCLA, and (c) No limit cycle oscillation at 200 kHz because of activating the DCLA part of the controller

2.7 Conclusion

Adaptive digital control methods to maximize the converter efficiency and improve its stability under variable switching frequency operation are presented in this chapter. The presented AFO digital controller tracks the minimum input power point, by adjusting the switching frequency f_{sw}. The optimum f_{sw} value results in the lowest converter total losses (maximum converter efficiency). Moreover, a dynamic technique to avoid limit cycle oscillation problem and to reduce cross over frequency variation when operating at different switching frequencies is presented in this chapter.

The need for a controller that tracks the optimum switching frequency under variable conditions is discussed. These conditions include components variations and aging, temperature variations, input voltage variations, and load variations. Even though such conditions are assumed and approximated at the time of converter design, they may vary significantly such that the conversion efficiency is compromised. Moreover, two issues which are associated with variable switching frequency operation in digital controllers, that do not exist in analog controllers, are reviewed. These are the limit cycle oscillation and the closed loop gain and phase variations as a result of the switching frequency variations.

While the AFO part of the proposed digital controller tracks the optimum switching frequency under variable operating conditions to result in high conversion efficiency, the DLCA part of the digital controller alleviates the issues of limit cycle oscillation and gain-phase variation associated with variable switching frequency in digital controllers. The AFO-DLCA concepts and controller algorithms are discussed and

analyzed in this chapter. The design theory and guidelines of the presented AFO-DLCA controller are presented and used to design for the proof of concept experimental prototype. The proof of concept experimental results is in good agreement with the theoretical results.

CHAPTER THREE
ANALYSIS AND DESIGN OF A VARIABLE STEP SIZE AUTO-TUNING ALGORITHM FOR DIGITAL POWER CONVERTER WITH A VARIABLE SWITCHING FREQUENCY

3.1 Introduction

As stated earlier, the the switching frequency of DC-DC converters is one of the variables that determine the converter power efficiency among many others. For a different operating condition and mode of operation, the switching frequency may be different for a highest efficiency [31]. The ability of a digital controller to perform sophisticated algorithms makes it easy to apply adaptive control algorithms where system parameters can be adaptively adjusted in response to system behaviors in order to achieve better performance [27,28]. An auto-tuning algorithm to adaptively optimize switching frequency is presented in [27] based on the efficiency tracking concept discussed in [28]. However, the controller in [27] utilizes a fixed step size algorithm which may not result in the best trade off between the speed and the accuracy (convergence error) of the converter's adaptive loop. This chapter presents the analysis and experimental results for an adaptive step-size variable switching frequency algorithm. The developed technique addresses the adaptive-step-size controller speed, convergence, accuracy, and sensitivity. The work is supported by experimental results obtained for a design example and a proof of concept hardware.

Next section discusses the variable switching frequency adaptive step size algorithm and its analysis. Section 3.3 presents the convergence stability and speed analysis for the variable step size adaptive controller. Section 3.4 presents the variable step size (VSS) adaptive controller flowchart. The VSS adaptive loop theoretical design and guidelines are discussed in Section 3.5. The experimental work is discussed in Section 3.6 while the conclusion is given in Section 3.7.

3.2 Variable Frequency Adaptive-Step-Size Algorithm

The analysis of the variable-step-size variable-switching-frequency algorithm is developed in this section based on the steepest descent algorithm [63,64] and the power loss model of DC-DC buck converter [31,35]. As discussed in [27], the main goal from the algorithm is to maximize the conversion efficiency under variable conditions and designs. This is achieved by adaptively tracking the optimum switching frequency, and dynamically minimizing the input power or input current under a fixed input voltage. In the previous chapter, such algorithm is implemented with a fixed increment/decrement step size of a certain control parameter during the optimization or auto-tuning, which may results in large delay in the convergence speed and/or a large convergence error or instability. In this section, the control algorithm is based on variable step size to improve speed and accuracy trade off. Fig. 3.1 shows the DC-DC synchronous buck converter considered in the analysis while Fig. 3.2 shows the input power curve resulting from varying the switching frequency.

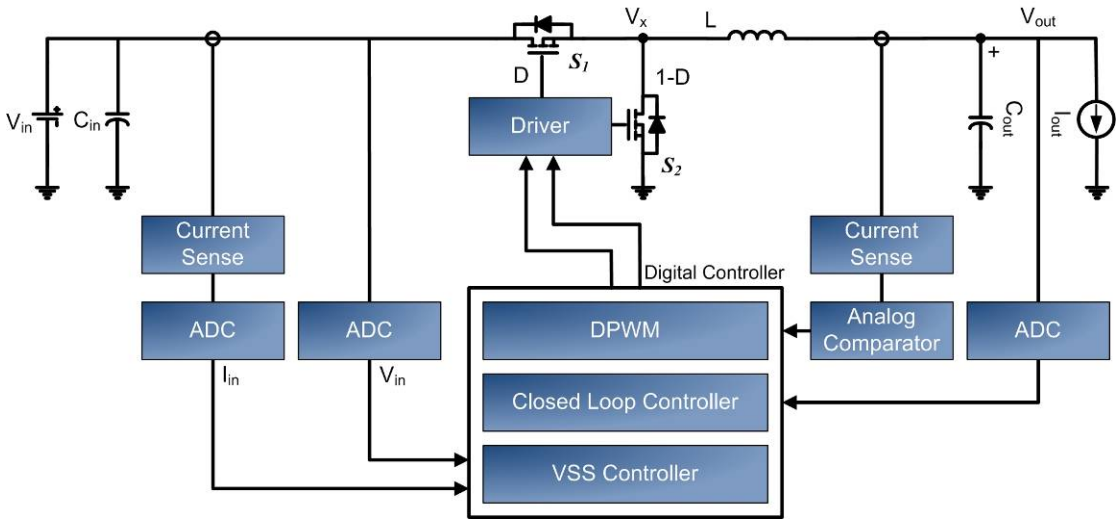


Fig. 3.1: Non-isolated synchronous buck DC-DC converter with VSS controller.

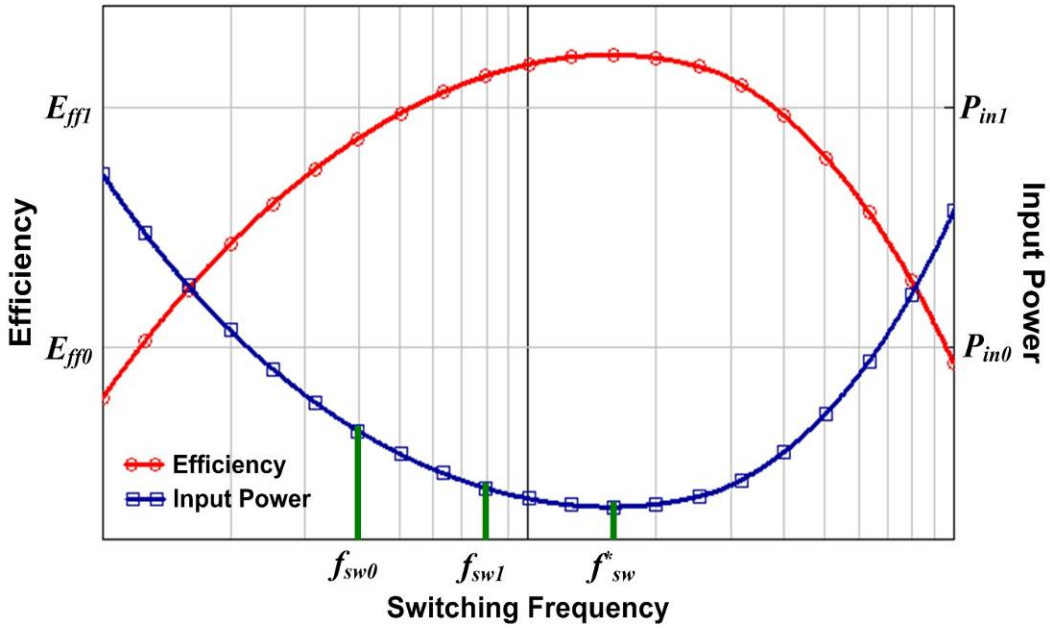


Fig. 3.2: Typical Input power and efficiency curves when varying the switching frequency with fixed input voltage

The following analysis is developed for the input power but similarly it can be developed for the input current (at fixed input voltage). Using the steepest descent algorithm [64], the switching frequency is varied according to the input current gradient function as follows:

$$f_{sw_{k+1}} = f_{sw_k} + \mu \cdot (\nabla P_{in_k})$$

(3.1)

where, $f_{sw_{k+1}}$ is the switching frequency at the next time interval, f_{sw_k} is the current switching frequency, μ is a constant that determines the step size, ∇P_{in} is the gradient function of the input power and the sign of the signal ∇P_{in} (positive or negative) determines the direction of the movement. The gradient function is given by:

$$\nabla P_{in} = \partial P_{in} / \partial f_{sw}$$

(3.2)

The expression for the input power gradient function ∇P_{in} can be found as follows:

$$P_{in} = P_{out} + P_{Losses} = V_{out} I_{out} + P_{Losses}$$

Yielding,

$$\nabla P_{in} = \frac{\partial P_{in}}{\partial f_{sw}} = \frac{\partial (V_{out} I_{out})}{\partial f_{sw}} + \frac{\partial P_{Losses}}{\partial f_{sw}} = \frac{\partial P_{Losses}}{\partial f_{sw}}$$

(3.3)

In the following, the gradient for each power loss type is calculated and the total input power gradient is found.

3.2.1 Gradient for Conduction Losses in CCM Mode:

The conduction losses in synchronous buck converter are the result of the RMS current passing through the parasitic resistances of the different components. By computing the conduction losses and taking the derivative with respect to the switching frequency, the gradient function for conduction losses in Continuous Conduction Mode (CCM) can be given by:

$$\nabla P_{\Phi_1} = \nabla P_{\alpha} + \nabla P_{\beta} + \nabla P_{\chi} + \nabla P_{\delta} \tag{3.4}$$

Where ∇P_{Φ_1} : is the input power gradient as a result of all conduction losses in CCM. ∇P_{α} : is the input power gradient as a result of control MOSFET conduction losses in CCM. ∇P_{β} : is the input power gradient as a result of synchronous MOSFET conduction losses in CCM. ∇P_{χ} : is the input power gradient as a result of Inductor conduction losses in CCM. ∇P_{δ} : is the input power gradient as a result of the sense resistor conduction losses in CCM.

The gradient for each conduction loss is computed as:

$$\nabla P_{\alpha} = \frac{\partial(P_{\alpha})}{\partial f_{sw}} = -\frac{1}{6} \cdot \frac{V_{out}^3}{V_{in}^3} \cdot \frac{(V_{in} - V_{out})^2}{L^2 f_{sw}^3} \cdot R_{sw} \tag{3.5}$$

$$\nabla P_{\beta} = \frac{\partial(P_{\beta})}{\partial f_{sw}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^3} \cdot \frac{(V_{in} - V_{out})^3}{L^2 f_{sw}^3} \cdot R_{sr} \tag{3.6}$$

$$\nabla P_{\chi} = \frac{\partial(P_{\chi})}{\partial f_{sw}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^2} \cdot \frac{(V_{in} - V_{out})^2}{L^2 f_{sw}^3} \cdot R_{DCR} \tag{3.7}$$

$$\nabla P_{\delta} = \frac{\partial(P_{\delta})}{\partial f_{sw}} = -\frac{1}{6} \cdot \frac{V_{out}^2}{V_{in}^2} \cdot \frac{(V_{in} - V_{out})^2}{L^2 f_{sw}^3} \cdot R_{sense} \tag{3.8}$$

Where P_{α} : is the control MOSFET conduction power losses in CCM mode, P_{β} : is the synchronous MOSFET conduction power losses in CCM mode, P_{χ} : is the inductor conduction power losses in CCM mode, P_{δ} : is the sense resistor conduction power losses in CCM mode, R_{sw} is the ON resistance of a main switch, R_{sr} is the ON resistance of a synchronous switch, R_{DCR} is the inductor parasitic resistance, and R_{sense} is the sensing resistance.

3.2.2 Gradient for Switching Losses in CCM Mode:

Switching losses (including driving losses) in synchronous buck converter are combinations of the turn ON and turn OFF losses of the main and synchronous switch, losses to charge the MOSFETs output capacitance and the driving losses. By computing the switching losses and taking the derivative with respect to switching frequency, the gradient function for switching losses in CCM can be given by:

$$\nabla P_{\Phi_2} = \nabla P_{\varepsilon} + \nabla P_{\phi} + \nabla P_{\varphi} + \nabla P_{\gamma} + \nabla P_{\kappa} + \nabla P_{\lambda} \tag{3.9}$$

Where ∇P_{Φ_2} : is the input power gradient as a result of all switching losses in CCM. ∇P_{ε} : is the input power gradient as a result of control MOSFET turn ON switching losses in CCM. ∇P_{ϕ} : is the input power gradient as a result of control MOSFET turn OFF switching losses in CCM. ∇P_{φ} : is the input power gradient as a result of synchronous MOSFET turn ON switching losses in CCM. ∇P_{γ} : is the input power gradient as a result of synchronous MOSFET turn OFF switching losses in CCM. ∇P_{κ} : is the input power gradient as a result of MOSFET output capacitance switching losses in CCM. ∇P_{λ} : is the input power gradient as a result of driving losses in CCM.

The gradient for each switching loss is computed by:

$$\nabla P_{\varepsilon} = \frac{\partial(P_{\varepsilon})}{\partial f_{sw}} = \frac{1}{2} Q_{sw} \frac{I_{out} V_{in}}{I g_{on}}$$

(3.10)

$$\nabla P_{\phi} = \frac{\partial(P_{\phi})}{\partial f_{sw}} = \frac{1}{2} Q_{sw} \frac{I_{out} V_{in}}{I g_{off}}$$

(3.11)

$$\nabla P_{\varphi} = \frac{\partial(P_{\varphi})}{\partial f_{sw}} = -\frac{1}{4} t_{rise\_sr} \cdot V_D \frac{V_{out}}{V_{in}} \cdot \frac{(V_{in} - V_{out})}{L f_{sw}}$$

(3.12)

$$\nabla P_{\gamma} = \frac{\partial(P_{\gamma})}{\partial f_{sw}} = \frac{1}{4} t_{fall\_sr} \cdot V_D \frac{V_{out}}{V_{in}} \cdot \frac{(V_{in} - V_{out})}{L f_{sw}}$$

(3.13)

$$\nabla P_{\kappa} = \frac{\partial(P_{\kappa})}{\partial f_{sw}} = \frac{1}{2} V_{in} (Q_{oss\_sw} + Q_{oss\_sr})$$

(3.14)

$$\nabla P_{\lambda} = \frac{\partial(P_{\lambda})}{\partial f_{sw}} = 2 Q_{gsw} V_g$$

(3.15)

Where P_{ε} : is the control MOSFET turn ON switching power losses in CCM, P_{ϕ} : is the control MOSFET turn OFF switching power losses in CCM, P_{φ} : is the synchronous MOSFET turn ON switching power losses in CCM, P_{γ} : is the synchronous MOSFET turn OFF switching power losses in CCM, P_{κ} : is the MOSFET output capacitance switching power losses in CCM, P_{λ} : is the driving power losses in CCM. Q_{sw} is the main switch charge, $I_{g_{on}}$ is the Driver ON current, $I_{g_{off}}$ is the Driver OFF current, V_D is the forward voltage drop of the switch body diode, t_{rise_sr} is the turn ON rise time of the synchronous switch, t_{fall_sr} is the turn OFF fall time of the synchronous switch, and Q_{oss} is MOSFET output charge. From the above, the gradient function for the total losses in CCM is:

$$\nabla P_{\Phi_{total}} = \nabla P_{\Phi_1} + \nabla P_{\Phi_2} \tag{3.16}$$

Where $\nabla P_{\Phi_{total}}$: is the input power gradient as a result of all switching and conduction losses in CCM.

3.2.3 Gradient for Conduction Losses in DCM Mode:

Following the same way used in CCM analysis above, and by computing the conduction losses in Discontinuous Conduction Mode (DCM) mode and taking the derivative with

respect to the switching frequency, the gradient function for conduction losses in DCM can be given by:

$$\nabla P_{\Psi_1} = \nabla P_{\mu} + \nabla P_{\nu} + \nabla P_{o} + \nabla P_{\varpi}$$

(3.17)

Where ∇P_{Ψ_1} : is the input power gradient as a result of all conduction losses in DCM. ∇P_{μ}: is the input power gradient as a result of control MOSFET conduction losses in DCM. ∇P_{ν} : is the input power gradient as a result of synchronous MOSFET conduction losses in DCM. ∇P_{o} : is the input power gradient as a result of Inductor conduction losses in DCM. ∇P_{ϖ} : is the input power gradient as a result of the sense resistor conduction losses in DCM. The gradient for each conduction loss is computed by:

$$\nabla P_{\mu} = \frac{\partial (P_{\mu})}{\partial f_{sw}} = -\frac{\sqrt{2}}{3} \cdot \frac{I_{out}^2 V_{out} R_{sw}}{\sqrt{\frac{I_{out} V_{in}^3 L f_{sw}^3}{V_{out}(V_{in} - V_{out})}}}$$

(3.18)

$$\nabla P_{\nu} = \frac{\partial (P_{\nu})}{\partial f_{sw}} = -\frac{\sqrt{2}}{3} \cdot \frac{I_{out}^2 (V_{in} - V_{out}) R_{sr}}{\sqrt{\frac{I_{out} V_{in}^3 L f_{sw}^3}{V_{out}(V_{in} - V_{out})}}}$$

(3.19)

$$\nabla P_{o} = \frac{\partial (P_{o})}{\partial f_{sw}} = -\frac{\sqrt{2}}{3} \cdot \frac{I_{out}^{2} R_{L}}{\sqrt{\frac{I_{out} V_{in} L f_{sw}^{\ 3}}{V_{out}(V_{in} - V_{out})}}}$$

(3.20)

$$\nabla P_{\varpi} = \frac{\partial (P_{\varpi})}{\partial f_{sw}} = -\frac{\sqrt{2}}{3} \cdot \frac{I_{out}^{2} R_{sense}}{\sqrt{\frac{I_{out} V_{in} L f_{sw}^{\ 3}}{V_{out}(V_{in} - V_{out})}}}$$

(3.21)

Where P_{μ} : is the control MOSFET conduction power losses in DCM mode, P_{ν} : is the synchronous MOSFET conduction power losses in DCM mode, P_{o} : is the inductor conduction power losses in DCM mode, P_{ϖ} : is the sense resistor conduction power losses in DCM mode.

3.2.4 Gradient for Switching Losses in DCM Mode:

By computing the switching losses in DCM mode and taking the derivative with respect to the switching frequency, the gradient function for switching losses in DCM can be given by:

$$\nabla P_{\Psi_{2}} = \nabla P_{\vartheta} + \nabla P_{\rho} + \nabla P_{\sigma} + \nabla P_{\varsigma}$$

(3.22)

Where ∇P_{Ψ_2} : is the input power gradient as a result of all switching losses in DCM. ∇P_{ϑ}: is the input power gradient as a result of control MOSFET turn OFF switching losses in DCM. ∇P_{ρ}: is the input power gradient as a result of synchronous MOSFET turn ON switching losses in DCM. ∇P_{σ}: is the input power gradient as a result of MOSFET output capacitance switching losses in DCM. ∇P_{ς}: is the input power gradient as a result of driving losses in DCM. The gradient for each switching loss is computed by:

$$\nabla P_{\vartheta} = \frac{\partial(P_{\vartheta})}{\partial f_{sw}} = \frac{1}{2\sqrt{2}} \frac{Q_{sw} I_{out} V_{in}}{I_{g_{off}} \sqrt{\frac{I_{out} V_{in} L f_{sw}}{V_{out}(V_{in} - V_{out})}}} \tag{3.23}$$

$$\nabla P_{\rho} = \frac{\partial(P_{\rho})}{\partial f_{sw}} = \frac{t_{rise\_sr}}{2\sqrt{2}} \frac{V_D I_{out}}{\sqrt{\frac{I_{out} V_{in} L f_{sw}}{V_{out}(V_{in} - V_{out})}}} \tag{3.24}$$

$$\nabla P_{\sigma} = \frac{\partial(P_{\sigma})}{\partial f_{sw}} = \frac{1}{2} V_{in} (Q_{oss\_sw} + Q_{oss\_sr}) \tag{3.25}$$

$$\nabla P_{\varsigma} = \frac{\partial(P_{\varsigma})}{\partial f_{sw}} = 2Q_{gsw}V_g$$

(3.26)

Where P_{ϑ}: is the control MOSFET turn OFF switching power losses in DCM, P_{ρ}: is the synchronous MOSFET turn ON switching power losses in DCM, P_{σ}: is the MOSFET output capacitance switching power losses in DCM, P_{ς}: is the driving power losses in DCM .

From the above, the input current sensitivity for total losses in DCM is:

$$\nabla P_{\Psi_{total}} = \nabla P_{\Psi_1} + \nabla P_{\Psi_2}$$

(3.27)

Where $\nabla P_{\Psi_{total}}$: is the change in the input power gradient as a result of all switching and conduction losses in DCM. Finally, the total input power gradient at any load can be calculated as:

$$\nabla P_{in\_Total} = \begin{Bmatrix} \nabla P_{\Phi_{total}}, & CCM \\ \nabla P_{\Psi_{total}}, & DCM \end{Bmatrix}$$

(3.28)

3.3 Convergence Stability and Speed Analysis for VSS Adaptive Controller

Before presenting the experimental results of the proposed adaptive-step-size optimization controller in this chapter, a detailed controller algorithm convergence stability and speed analysis is discussed. The cost function [63,64] of the proposed adaptive step-size variable switching frequency controller is the input current/power, which is used to track the optimum switching frequency for a maximum efficiency. Referring to Fig. 3.2, the minimum input power corresponds to the maximum efficiency point. A good approximation for such curve is a second order parabola which can be represented as in Eq. (3.29):

$$P_{in} = P_{in_{\min}} + \lambda \cdot (f_{sw} - f_{sw}^{*})^{2} \tag{3.29}$$

Where P_{in} is the input power, $P_{in_{\min}}$ is the minimum input power, f_{sw} is the current switching frequency, f_{sw}^{*} is the optimum switching frequency that gives the minimum input power and λ is a proportionality constant. Taking the first derivative of equation (3.29) to yeild :

$$\frac{dP_{in}}{df_{sw}} = 2\lambda \cdot (f_{sw} - f_{sw}^{*}) \tag{3.30}$$

The second derivative is a constant value over the entire input current curve give by:

$$\frac{d^2 P_{in}}{df_{sw}^2} = 2\lambda$$

(3.31)

The main goal of the analysis is to find the optimum switching frequency f_{sw}^* that minimizes the input power to its lowest value. At different loads and system parameters the exact input power curve is not known, so a search algorithm to find the optimum point is needed. The search algorithm starts with an initial value for the switching frequency f_{sw_0}, then measures the slope of the input power curve at that point. After that the algorithm calculates a new switching frequency value f_{sw_1}, which equals to the old switching frequency plus/minus an incremental value. The iterative process repeats till the optimum switching frequency f_{sw}^* is found.

3.3.1 Gradient Search Using Steepest Descent Method

There are many algorithms used for gradients search, a simple and practical one is the steepest descent algorithm [64]. Steepest Descent algorithm follows the search method described above and can be represented by (3.1) as:

$$f_{sw_{k+1}} = f_{sw_k} + \mu \cdot (-\nabla_k)$$

Where k is the iteration number, $f_{sw_{k+1}}$ is the new switching frequency value, f_{sw_k} is the present switching frequency value, μ is a constant that controls stability and convergence of the adaptive loop and ∇_k is the gradient at $f_{sw}=f_{sw_k}$, using Equation (3.30) the gradient ∇_k can be expressed as :

$$\nabla_k = \left.\frac{dP_{in}}{df_{sw}}\right|_{f_{sw}=f_{sw_k}} = 2\lambda \cdot (f_{sw_k} - f_{sw}^*)$$

(3.32)

The steepest descent adaptive loop dynamics from the initial switching frequency iteration f_{sw_0} to the optimum switching frequency f_{sw}^* can be studied by substituting Equation (3.32) into Equation (3.1) as:

$$f_{sw_{k+1}} = f_{sw_k} - 2\mu\lambda \cdot (f_{sw_k} - f_{sw}^*)$$

(3.33)

Rearranging the equation:

$$f_{sw_{k+1}} = (1-2\mu\lambda) \cdot f_{sw_k} + 2\mu\lambda \cdot f_{sw}^*$$

(3.34)

Taking the first four iterations of Equation (3.34) gives

$$f_{sw_1} = (1-2\mu\lambda)\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*$$

(3.35)

$$f_{sw_2} = (1-2\mu\lambda)^2\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*\cdot\left[(1-2\mu\lambda)+1\right]$$

(3.36)

$$f_{sw_3} = (1-2\mu\lambda)^3\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*\cdot\left[(1-2\mu\lambda)^2+(1-2\mu\lambda)+1\right]$$

(3.37)

$$f_{sw_4} = (1-2\mu\lambda)^4\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*\cdot\left[(1-2\mu\lambda)^3+(1-2\mu\lambda)^2+(1-2\mu\lambda)+1\right]$$

(3.38)

From those equations, a general expression for f_{sw_k} at any iteration can be given as:

$$f_{sw_k} = (1-2\mu\lambda)^k\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*\cdot\sum_{n=0}^{k-1}(1-2\mu\lambda)^n$$

(3.39)

$$f_{sw_k} = (1-2\mu\lambda)^k\cdot f_{sw_0} + 2\mu\lambda\cdot f_{sw}^*\cdot\frac{1-(1-2\mu\lambda)^k}{1-(1-2\mu\lambda)}$$

(3.40)

$$f_{sw_k} = f_{sw}^{*} + (1-2\mu\lambda)^k \cdot (f_{sw_0} - f_{sw}^{*})$$

(3.41)

3.3.2 Gradient Stability and Convergence

The ratio between successive terms in the summation in Equation (3.41) can be defined as $r = 1-2\mu\lambda$, the ratio r is the most important parameter that determine the stability of the adaptive loop. From Equation (3.41) it is clear that the iterative process will be stable if :

$$|r| = |1-2\mu\lambda| < 1$$

(3.42)

This condition can be expressed also as

$$\frac{1}{\lambda} > \mu > 0$$

(3.43)

If the condition in Equation (3.42) or (3.43) is satisfied, the adaptive loop will be stable and will converge to the optimum switching frequency:

$$\lim_{k\to\infty}\left[f_{sw_k} \right] = f_{sw}^{*}$$

(3.44)

It can be noted also that the ratio r plays an important role in determining the convergence speed to the optimum solution. Fig. 3.3 shows weight adjustment behavior

for AFO loop at different values of r, the adaptive loop starts with initial switching frequency of 600 kHz and tries to reach the optimum switching frequency of 180 kHz. From the figure it can be noted that the rate of convergence increase as r value decrease reach to its maximum at r=0. Also it can be noted also that for positive values of r (Overdamped) there is no oscillation while for negative values (Underdamped) there is an overshoot which decays eventually to the optimum point finally at r=0 the system is called critically damped.

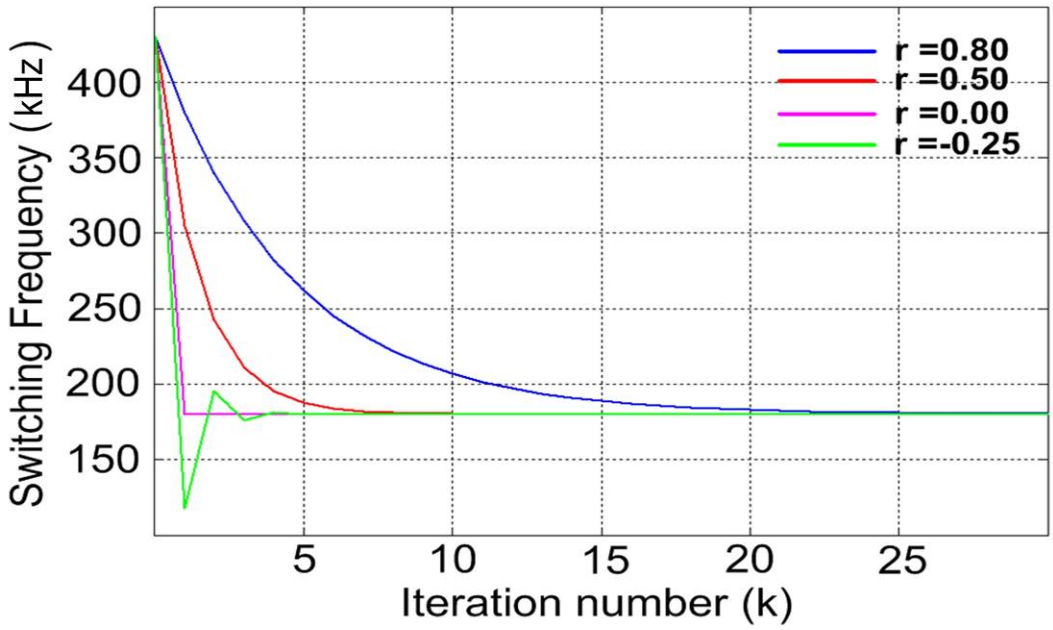


Fig. 3.3 Weight adjustment behavior for AFO loop at different values of r

3.4 Variable Step-Size Adaptive Controller Flowchart

Fig. 3.4 shows an implementation flowchart for the Variable-Step-Size Switching Frequency Optimization controller algorithm. The algorithm can be activated periodically or run in continuous manner with appropriate delay. N samples of P_{in} (converter sensed input power) are taken by two ADC's (one for input current and the other is for input voltage) and are stored and averaged to generate $P_{in}(n)$. $P_{in}(n)$ is used as an indication of the converter efficiency since the maximum efficiency point occurs at the minimum input current point. P_{in} is used to decide the value of the variable step size digital controller switching frequency. Next, the AFO program will calculate the difference between the previous value and the new value of P_{in} and the difference between the current value and the previous value of f_{sw} as follows:

$$\Delta P_{in} = P_{in}(n) - P_{in}(n-1) \tag{3.45}$$

$$\Delta f_{sw} = f_{sw}(n) - f_{sw}(n-1) \tag{3.46}$$

A check will be performed to see if ΔP_{in} has sufficient difference (P_e) to update f_{sw} or not. If this difference is sufficient, the program will proceed to the next step. Otherwise, it will start from the beginning by sampling P_{in} again. If the signs (positive or negative) of Equations (3.45) and (3.46) are similar, this means f_{sw} should be incremented by f_{sw_step} to move toward the maximum efficiency point (or minimum input power).

Otherwise, if the signs of Equations (3.45) and (3.46) are not similar, this means f_{sw} should be decremented by f_{sw_step} to move toward the maximum efficiency point. f_{sw_step} is calculated using equation (3.47):

$$f_{sw\_step} = \left| \xi \cdot \mu_{max} \cdot \nabla P_{in} \right| \tag{3.47}$$

Where μ_{max} is the maximum step size which can be calculated using equation (3.43), ξ a constant less than 1 used to make sure that the maximum step size μ_{max} is not exceeded. And ∇P_{in} is the gradient of the input power or the input current with fixed input voltage. Increasing the converter efficiency by decreasing the input power indicates a reduction in the total losses to the minimum possible value (optimal switching frequency value). After storing the current values of P_{in} and f_{sw}, the program will decrement or increment f_{sw} and update it. Then, after several (M) switching cycles (enough to reach steady-state), P_{in} is sampled again and the AFO process is repeated. It must be noted that the compensated control signal D_c that regulates the converter output voltage is generated by a digital controller that also contains the AFO algorithm. Finally, note that the AFO loop bandwidth is much smaller than the output voltage regulation loop bandwidth.

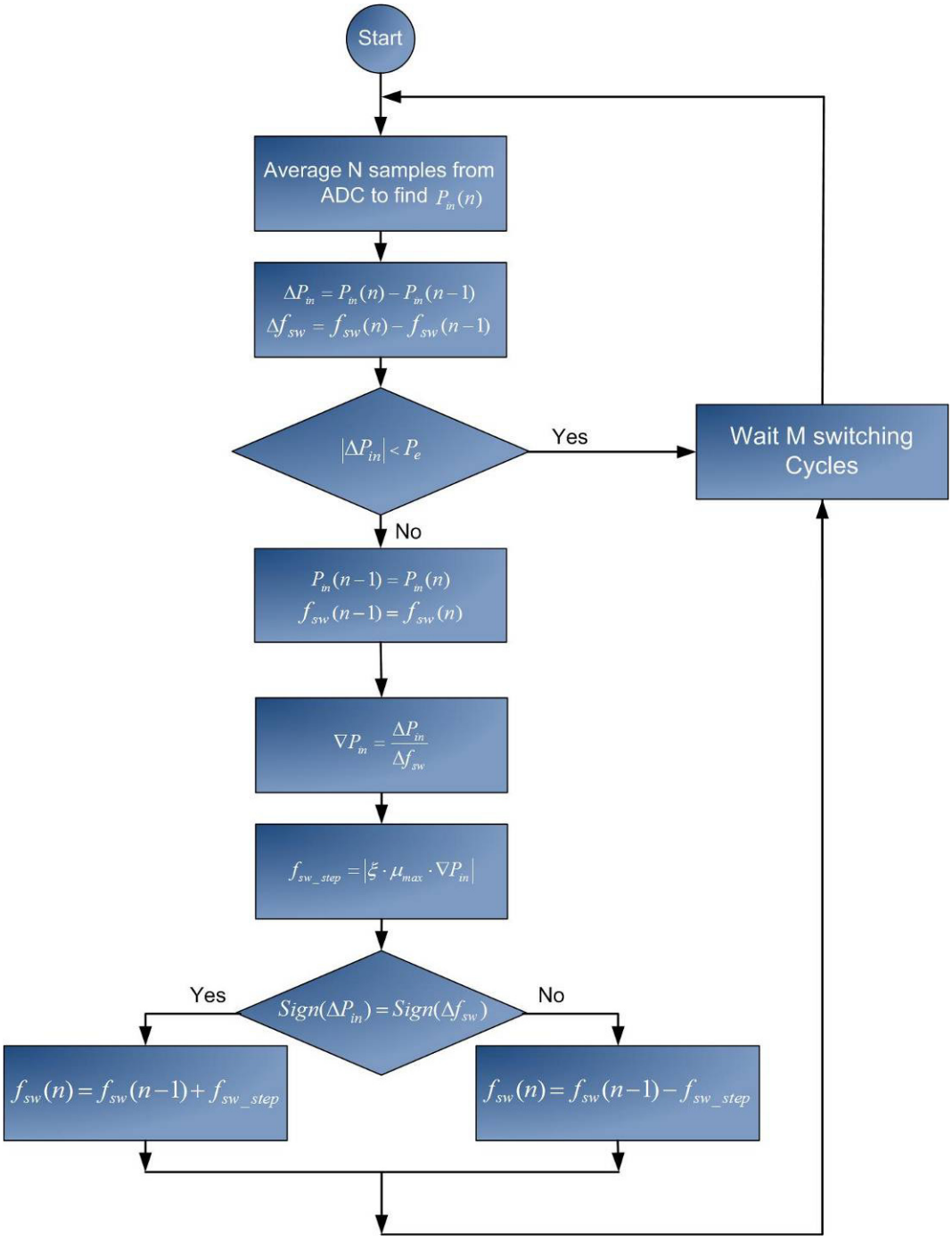


Fig. 3.4: Variable-Step-Size (VSS) digital controller flowchart

3.5 Adaptive Loop Theoretical Design and Guidelines

This section describes how the analysis developed in Section 3.3 can be used to design and predict the behavior and stability of the proposed variable step size controller. The design used in this section is the same design used in the experimental work and simulation of the next section. The experimental setup is a single phase DC-DC buck converter with V_{in}=12V , V_o=1V , Output Inductor: L_o=400nH , Output Capacitors $5mF$, Synchronus FET: NTD40N03R, two in parallel., Control FET: NTD85N02R, two in parallel, FETs Driver: ADI3418K - 12V, The controller is a digital controller implemented in FPGA part: Xilinx Virtex 4, Output Voltage ADC: ADI9215 - 10-bit - 30M sample/sec, Input Current ADC: 12-bit 100k sample/sec, and 13-bit DPWM. From the above specs and for 10A load current. The step size for each iteration can be calculated from Equation (3.47). For example, assume that the adaptive loop is at switching frequency of 420 kHz and that it converged to this frequency from an initial switching frequency of 455 kHz. Using Equation (3.47), the input power gradient ∇P_{in} can be calculated as follow: First, the average input power $P_{in}(n) = 9.31W$ at $f_{sw}(n) = 420kHz$ and the previous average input power $P_{in}(n-1) = 9.41W$ at $f_{sw}(n-1) = 455kHz$, the gradient $\nabla P_{in}(n)$ can be approximated as:

$$\nabla I_{in}(n) = \frac{I_{in}(n) - I_{in}(n-1)}{f_{sw}(n) - f_{sw}(n-1)} = \frac{0.931 - 0.941}{420\times10^3 - 455\times10^3} = 2.8571\times10^{-6}$$

Second, the maximum $\mu(n)$ for any step size can be calculated from Equation (3.31) by taking the derivative of the gradient with respect to the switching frequency as follows:

$$\frac{d\nabla_k}{df_{sw}} = \frac{d(2\lambda \cdot (f_{sw_k} - f_{sw}^*))}{df_{sw}} = 2\lambda$$

From the power stage specs:

$$\frac{d\nabla_k}{df_{sw}} = 2\lambda = 8.202 \times 10^{-12}$$

From Equation (3.43), and to ensure over damped response at the maximum step-size:

$$0 < \mu < \frac{1}{2\lambda} \Rightarrow \mu < \frac{1}{2 \times 4.101 \times 10^{-13}} \Rightarrow \mu < 1.219 \times 10^{11}$$

This value represents the absolute maximum value for μ_{max} above which, the system become unstable. Finally selecting $\xi = 0.1$ the step size $\mu(n)$ is:

$$f_{sw\_step} = \left| \xi \cdot \mu_{\max} \cdot \nabla P_{in} \right| = \left| 0.1 \times 1.219 \times 10^{11} \times 2.8571 \times 10^{-6} \right| = 3.4829 \times 10^{4} \text{ Hz}$$

3.6 Experimental Results

To verify the proposed concept, the block diagram of the prototype shown in Fig. 3.1 was built with the specifications presented in Section 3.5. Table 3.1 shows a sample comparison data obtained from the experimental prototype for fixed step-size algorithms and for the proposed adaptive step-size algorithm at different ξ values that affects the convergence speed and the accuracy. Fig. 3.5 shows comparison of the required number of iteration between a fixed step-size algorithm with step size equals to 10 kHz and variable step size algorithm at different load currents. Fig. 3.6 shows a comparison of the VSS algorithm switching frequency at different iterations using different zetas at

different load currents and Fig. 3.7 shows a comparison of the input current resulting from changing the switching frequency at different iterations using different zetas at different load currents.

Table 3.1. VSS Experimental Results

Load	Criteria	**Fixed Step Size**			**Variable Step Size**		
		5 kHz	10 kHz	30 kHz	$\xi = 0.05$	$\xi = 0.1$	$\xi = 0.15$
		Exp.	Exp.	Exp.	Exp.	Exp.	Exp.
5A	Iterations	84	41	18	33	19	12
	% Error	0	0.061	6.550	1.938	3.416	6.946
10A	Iterations	83	41	12	31	16	12
	% Error	0	2.209	2.210	2.021	3.322	4.111
15A	Iterations	81	39	12	23	12	8
	%Error	0	0.640	6.711	0.134	2.260	3.578

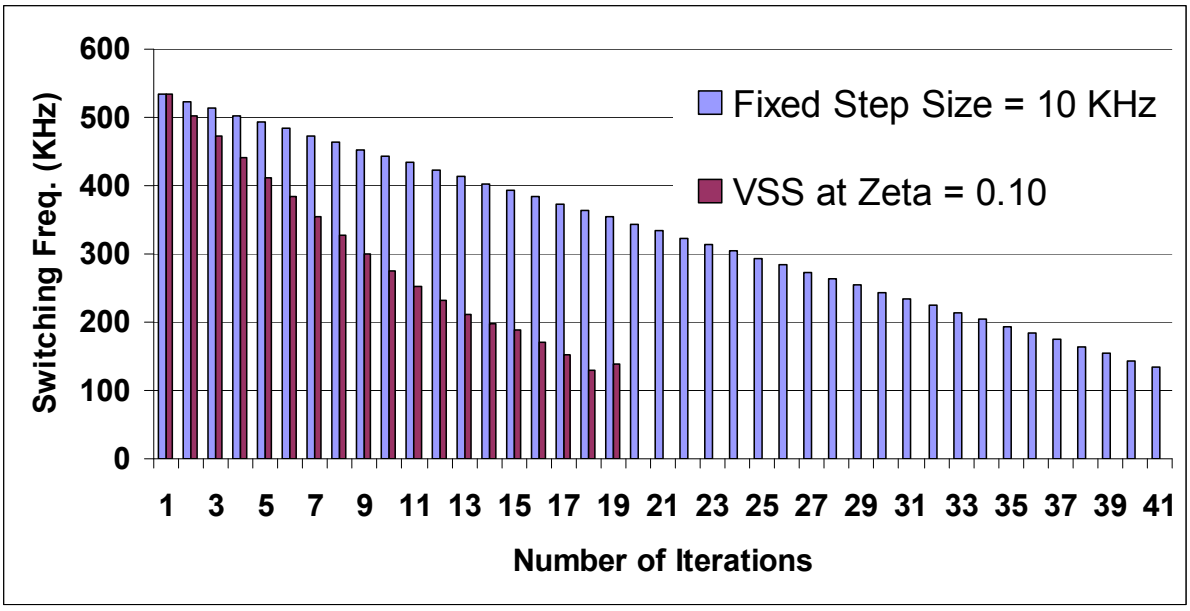


Fig. 3.5 (a) Comparing variable step size with fixed step size at 5A load (start up frequency 533 KHz)

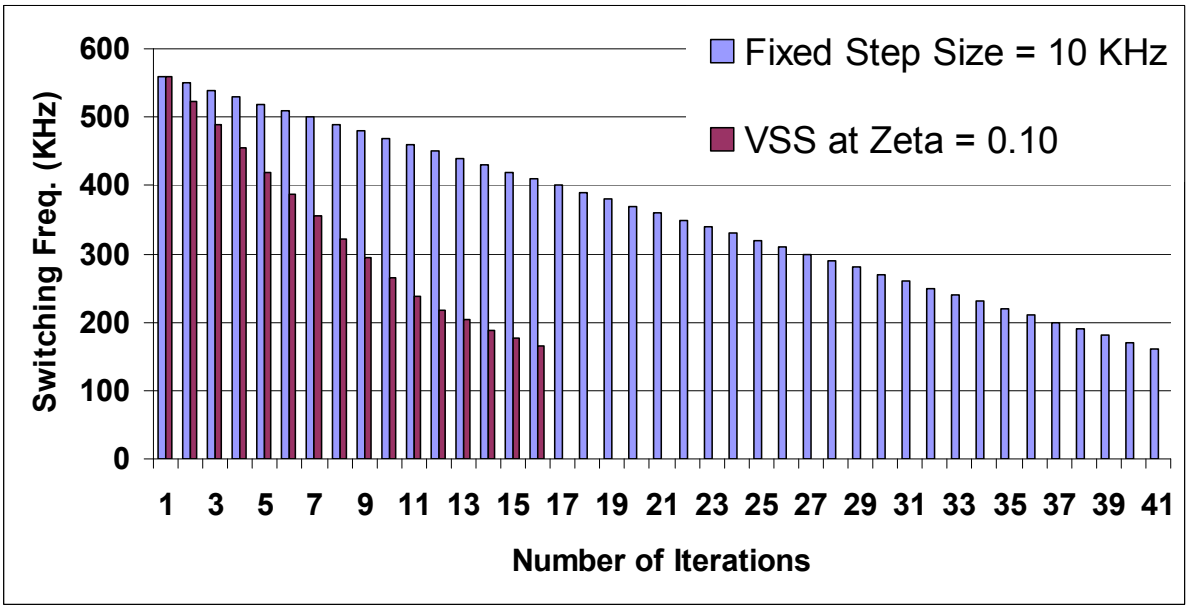


Fig. 3.5 (b) Comparing variable step size with fixed step size at 10A load (start up frequency 560 KHz)

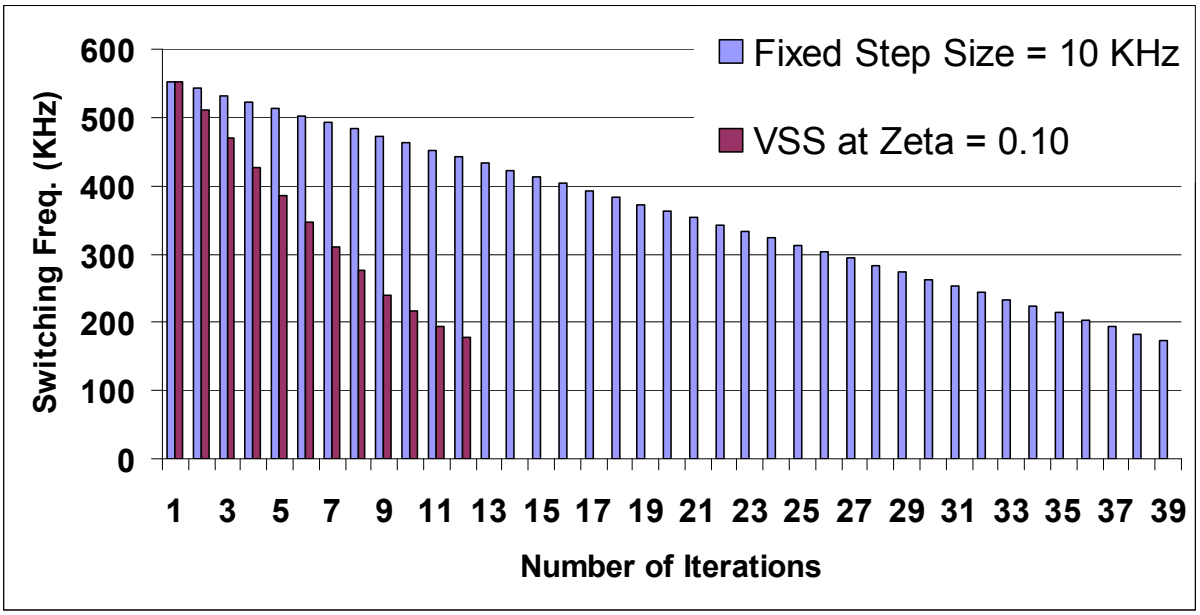


Fig. 3.5 (c) Comparing variable step size with fixed step size at 15A load (start up frequency 552 KHz)

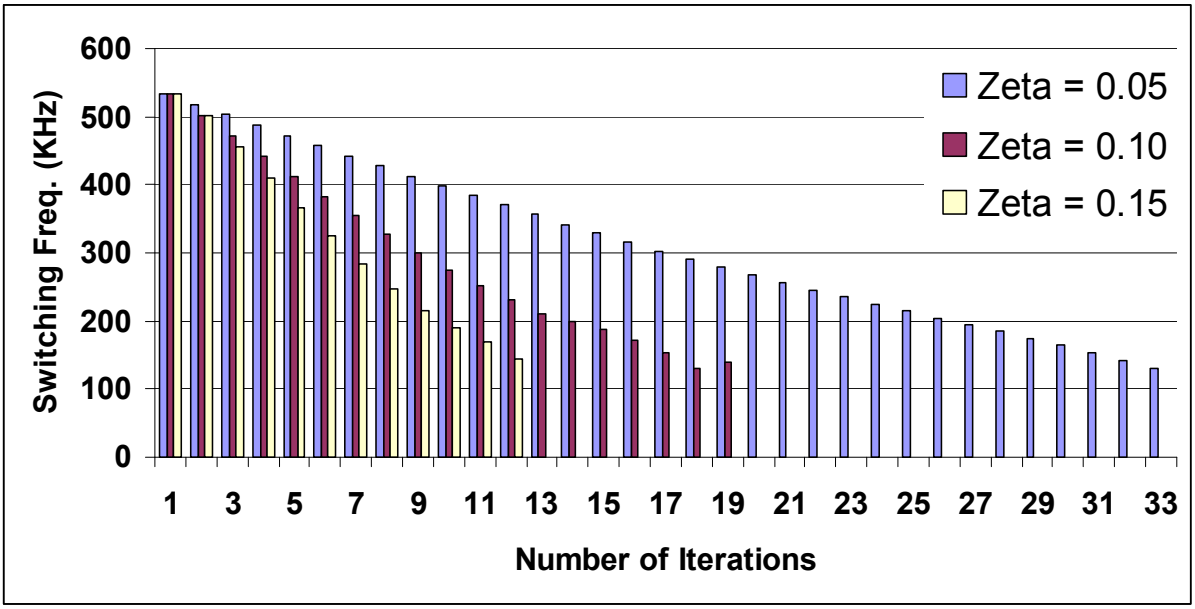


Fig. 3.6 (a) Switching frequency at different iterations using different Zetas at 5A load

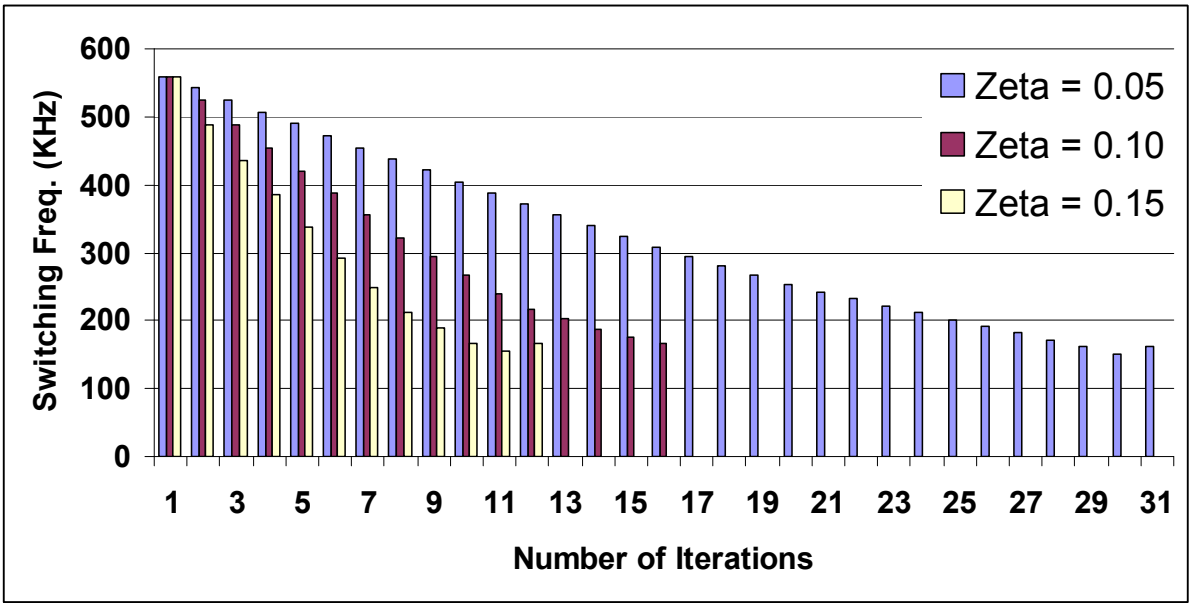


Fig. 3.6 (b) Switching frequency at different iterations using different Zetas at 10A load

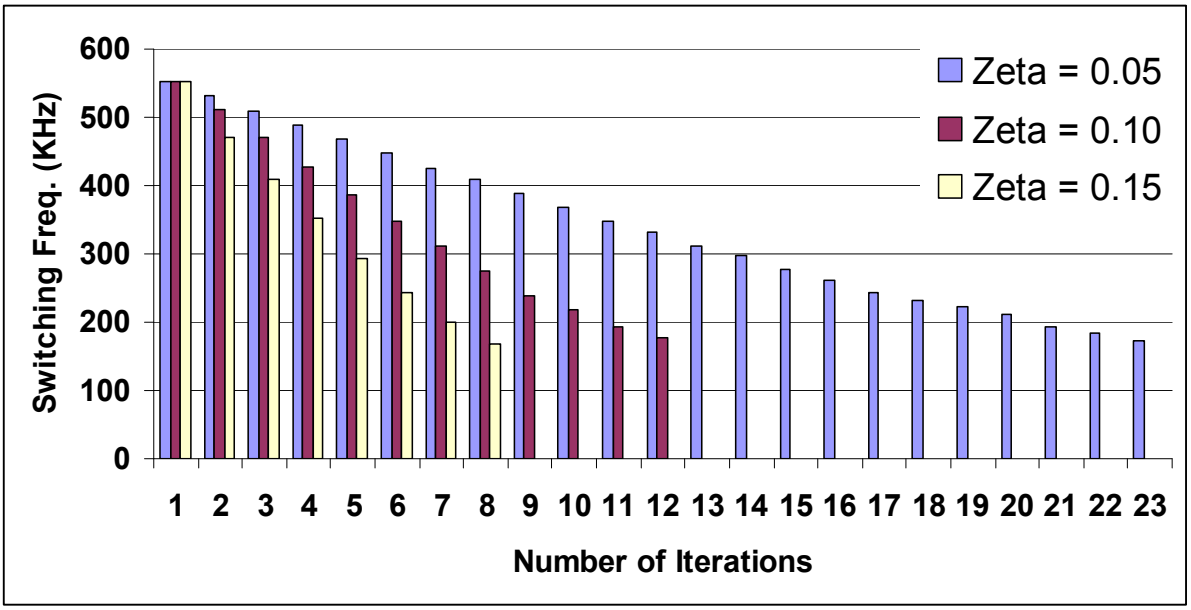


Fig. 3.6 (c) Switching frequency at different iterations using different Zetas at 15A load

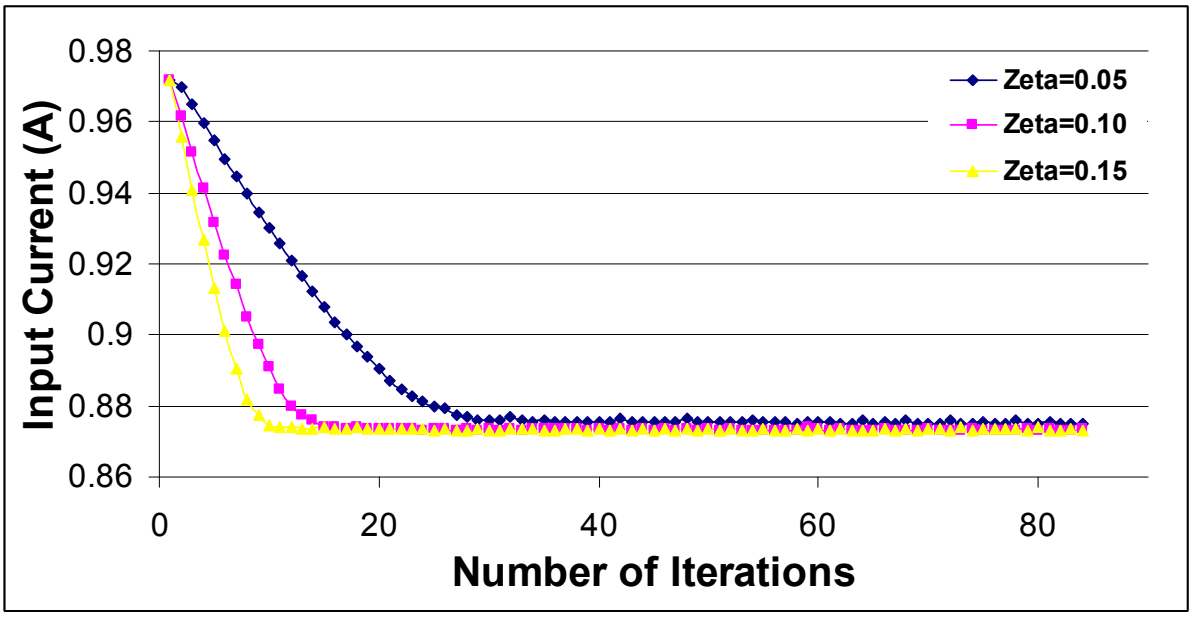


Fig. 3.7 (a): Input current at different iterations using different Zetas at 10A load

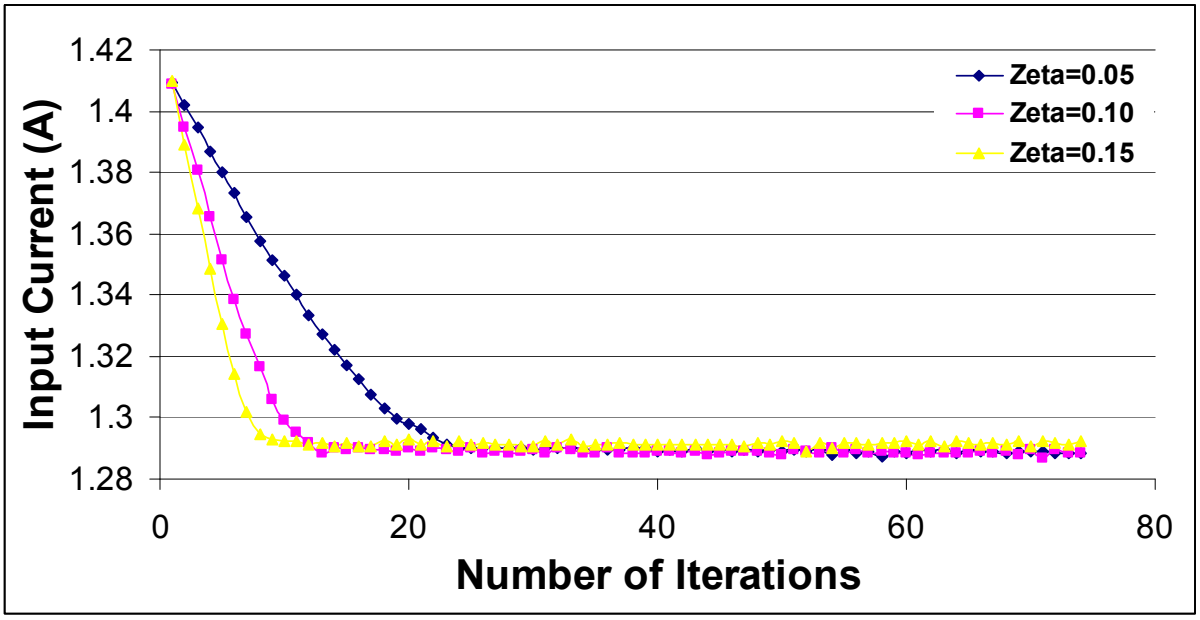


Fig. 3.7 (b): Input current at different iterations using different Zetas at 15A load

3.7 Conclusion

This chapter presents a self auto-tuning algorithm with adaptive variable-step-size to track and detect the optimum switching frequency of DC-DC converter under variable operating conditions such as load variations, voltage variations, components variations, aging effects, and temperature effects. The Variable-Step-Size (VSS) algorithm was theoretically developed and analyzed based on buck DC-DC converter loss model, and a general expression for the gradient function that describes the VSS algorithm was given. The experimental results were compared for both fixed step size algorithm and the adaptive variable step size algorithm. It is shown that the proposed Variable-Step-Size adaptive algorithm achieves better trade off between speed and accuracy compared to the fixed step size algorithm. The convergence stability and speed are analyzed to give the design guidelines for the adaptive loop response.

CHAPTER FOUR
MULTIVARIABLE ADAPTIVE EFFICIENCY OPTIMIZATION DIGITAL CONTROLLER

4.1 Introduction

Optimizing the efficiency of DC-DC converters is one of top priorities for power electronics design engineer. Power converter losses, and the corresponding power efficiency for a given design varies at different loading conditions, line conditions, and it is impacted by the variations of temperature and aging effect [27-44]. From studying the power loss in DC-DC converter, it can be noted that there are two main kinds of losses, DC-DC converter switching losses and DC-DC converter conduction losses [31-38]. Switching losses are function of the switching frequency and conduction losses are function of the load current. Optimizing DC-DC converter switching frequency is one way to reduced switching losses [27,31,35]. While optimizing DC-DC converter dead time value can reduce conduction losses [31-38].

The ability of a digital controller to perform sophisticated algorithms makes it easy to apply adaptive control laws where system parameters can be dynamically adjusted in response to system behaviors in order to achieve better efficiency [28]. An adaptive controller and algorithm to optimize switching frequency of DC-DC converter is presented in [27] based on the efficiency tracking concept discussed in [28]. However, the controller in [27] optimizes one parameter only which is the “switching frequency” while the controller in [28] optimizes another parameter which is the “SR dead-time”, which may

not result in maximum or global efficiency point and combined efficiency improvement. Since the input power/current used in both [27] and [28] as the function to minimize, a single controller that optimize both variables at the same time that exhibits multivariable behavior can be used.

In this chapter, the analysis, simulation and experimental results for a multivariable adaptive controller (MVAC) that optimize DC-DC converter switching frequency and dead-time together is presented. Next section discusses the effect of switching frequency and dead-time on losses. Section 4.3 presents the multivariable adaptive controller algorithm. Section 4.4 presents a mathematical treatment for the MVAC algorithm stability and sensitivity. Experimental results are discussed in Section 4.5 and finally conclusion is given in Section 4.6.

4.2 Effect of Different PWM Parameters on Losses

In this section a study of the effect dead-time on total system losses and thus its effect on efficiency is presented. The effect of switching frequency on losses was studied in details in Section 2.2. Fig. 4.1 shows a non-isolated buck DC-DC converter with synchronous rectification to be taken as a converter example to present the MVAC of this chapter.

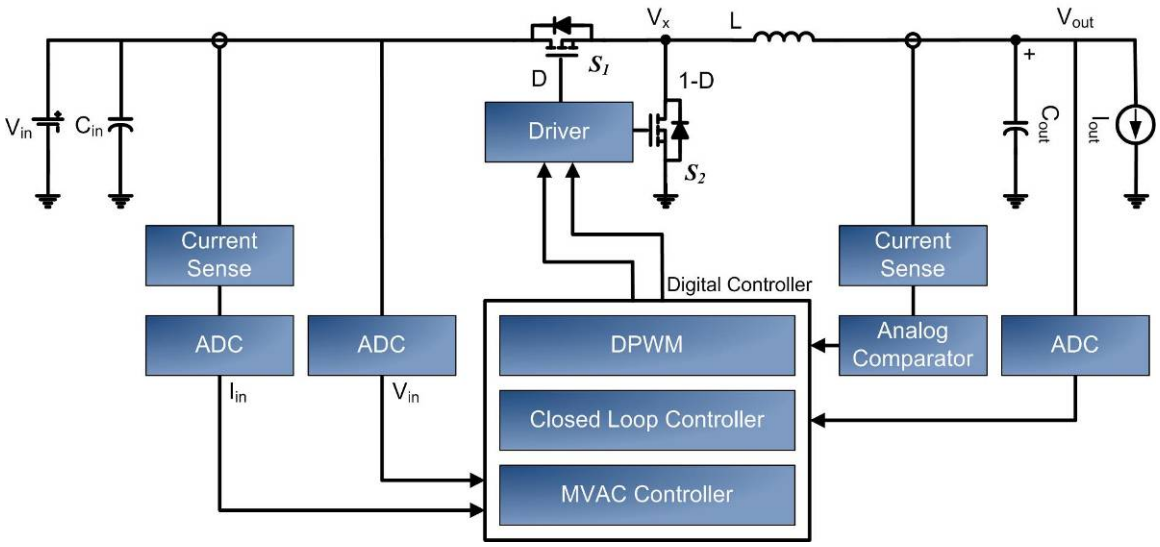


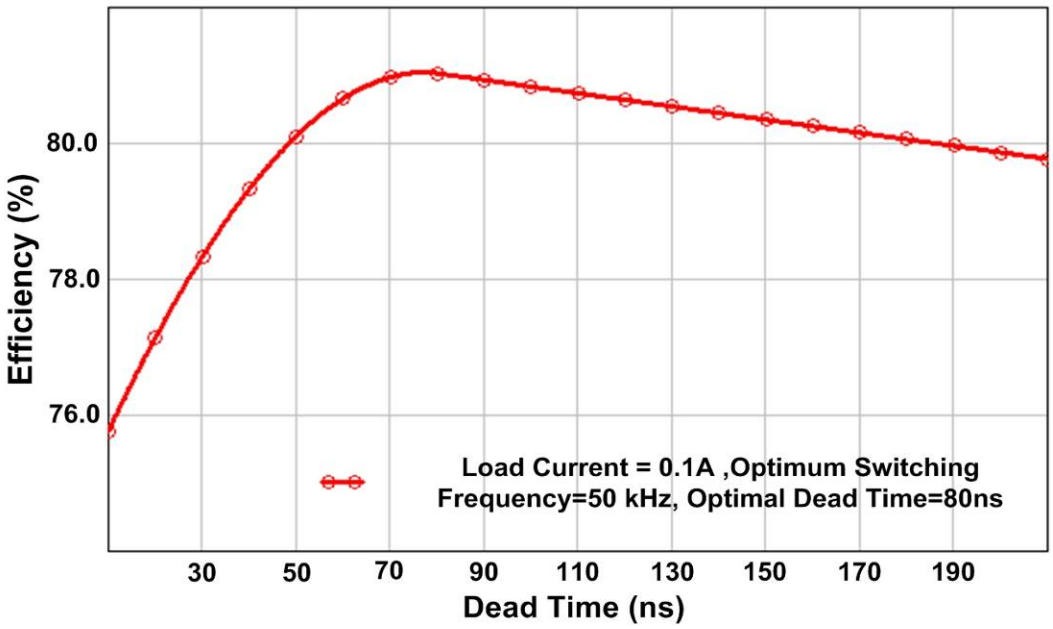
Fig. 4.1: Non-isolated synchronous buck DC-DC converter with MVAC controller

For synchronous rectifiers there are two main types of dead-time losses: switching losses that depends on the switching frequency and the body diode conduction losses that are function of the load current and body diode forward voltage drop. Dead-Time switching losses occur when turning the MOSFET ON/OFF while its parasitic capacitances are not fully discharged causing hard switching losses. The magnitude of hard switching losses depends on the parasitic capacitance value, the voltage across the capacitance and the switching frequency [29].

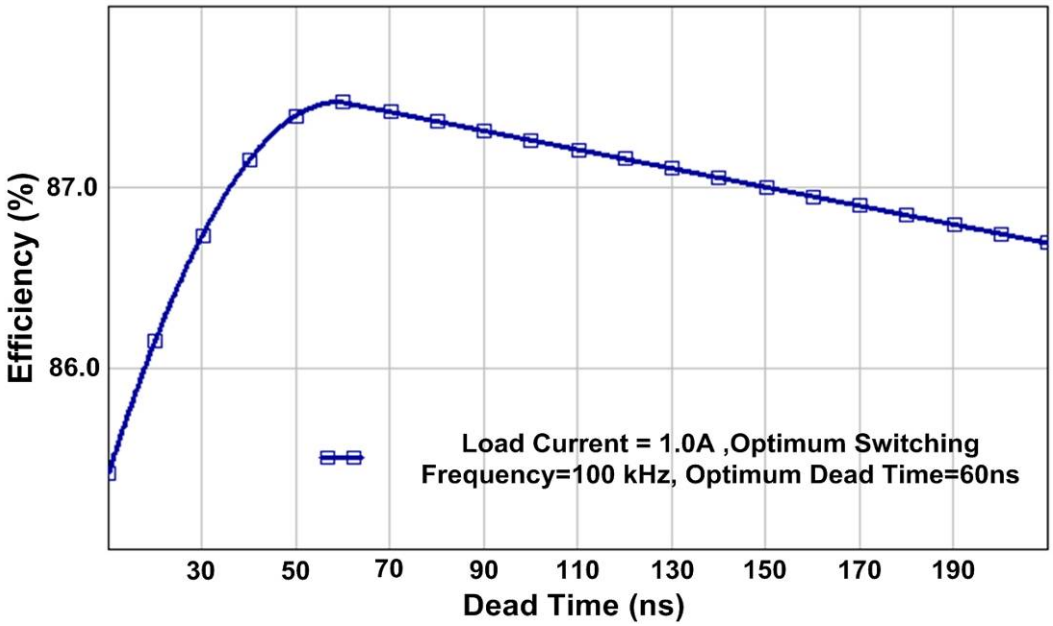
The second type of dead-time losses is the body diode conduction losses, which are mainly the result of the MOSFET parasitic diode. When the parasitic capacitance is fully discharged the body diode starts conduction and contributes a conduction loss that depends on the body diode forward voltage drop, and the RMS current passing through it. Finally, the body diode reverse recovery loss is another considerable loss that is generated

when the body-diode turns off. Reverse recovery losses depends on the charge stored on parasitic capacitor, the voltage across the body diode and the switching frequency [29].

Smaller dead-time means lower MOSFET's body-diode switching and conduction losses. Moreover, the body-diode switching and conduction losses increase with the load. The optimized dead-time that achieves the lowest total body-diode switching and conduction losses is related to many nonlinear parameters that makes the optimized dead-time (t_{dO}) different at different conditions. An adaptive controller that adaptively adjusts the dead-time , t_d, within a range depending on such nonlinear parameters variation can be used to achieve the optimum dead-time t_{dO}. Fig. 4.2 shows that at given load condition there exist an optimized dead-time value where the efficiency is maximum.



(a)



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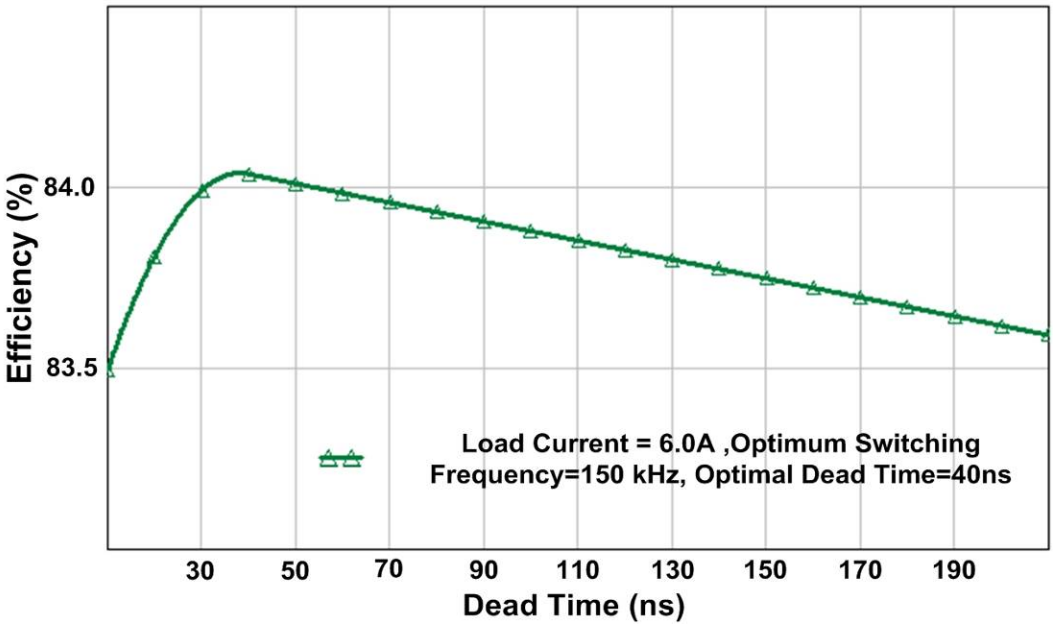

(c)

Fig. 4.2: Efficiency vs. Dead-Time at (a) 0.1A, (b) 1.0A and (c) 6.0A. At different loads there is an optimized Dead-Time value at which the efficiency is maximum.

From the above discussion, it can be noted that there is an optimized switching frequency, dead-time value for each load where the switching and conduction losses are minimum [31]. Fig. 4.3 shows a three dimensional surface plot for frequency, dead-time and efficiency at different load conditions for a typical synchronous buck DC-DC converter design. Fig. 4.3 surface plots are obtained from a comprehensive multivariable loss model built in MathCad®. From Fig. 4.3 it can be noted that for each load there is an optimum (frequency, dead-time) pair points where efficiency is maximum. The multivariable controller presented in the next section aims at finding the optimum pair for frequency and dead-time at variable loads and other conditions.

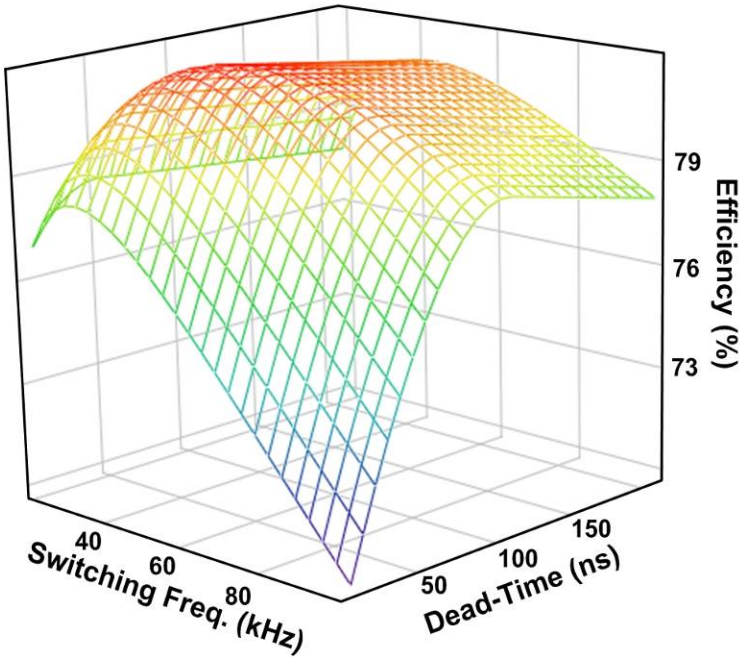

Fig. 4.3: (a) 3D surface plot for the switching frequency, dead-time and efficiency at load current = 0.1A, optimum F_{sw} = 50 kHz, optimum Dead-Time = 80ns

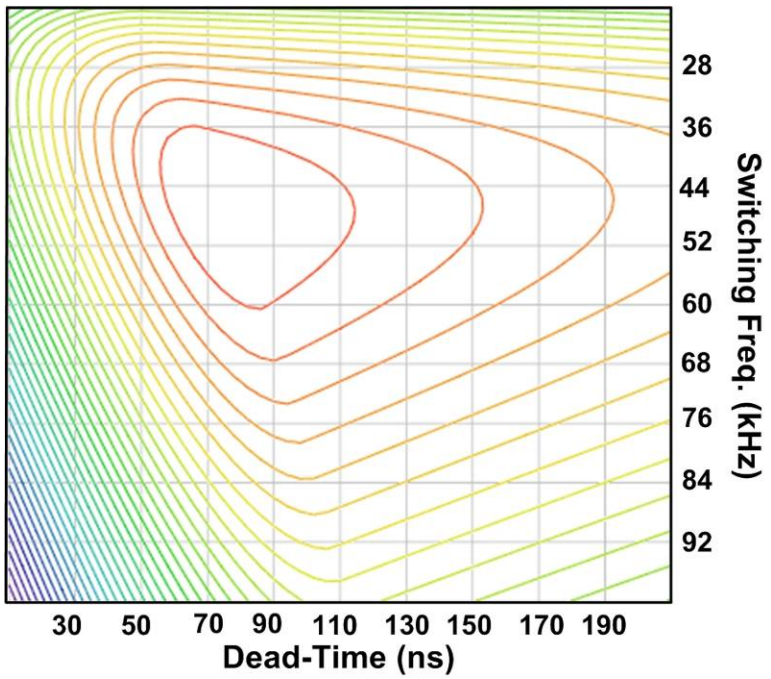

Fig. 4.3 (b): Contour plot for the switching frequency, dead-time and efficiency at load current = 0.1A, optimum F_{sw} = 50 kHz, optimum dead-time = 80ns

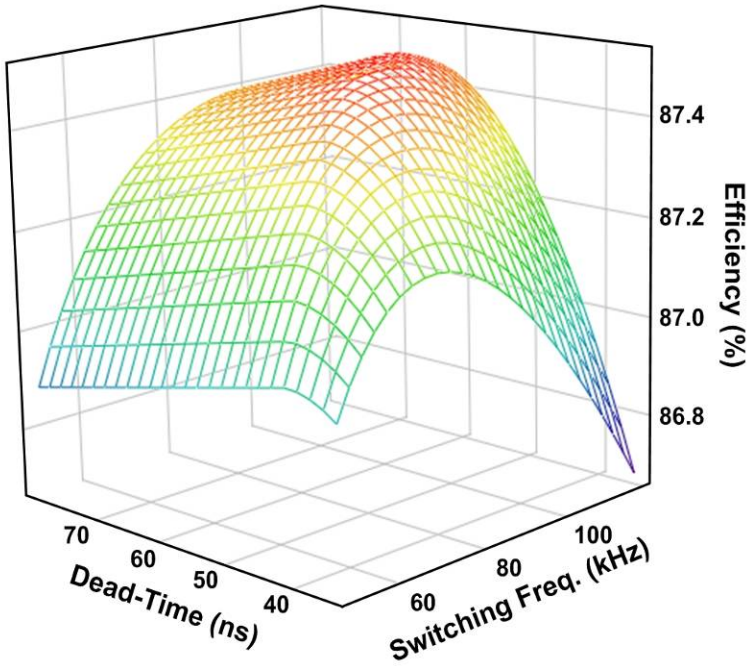

Fig. 4.3 (c): 3D surface plot for the switching frequency, dead-time and efficiency at load current = 1.0A, optimum F_{sw} = 100 kHz, optimum dead-time = 60ns

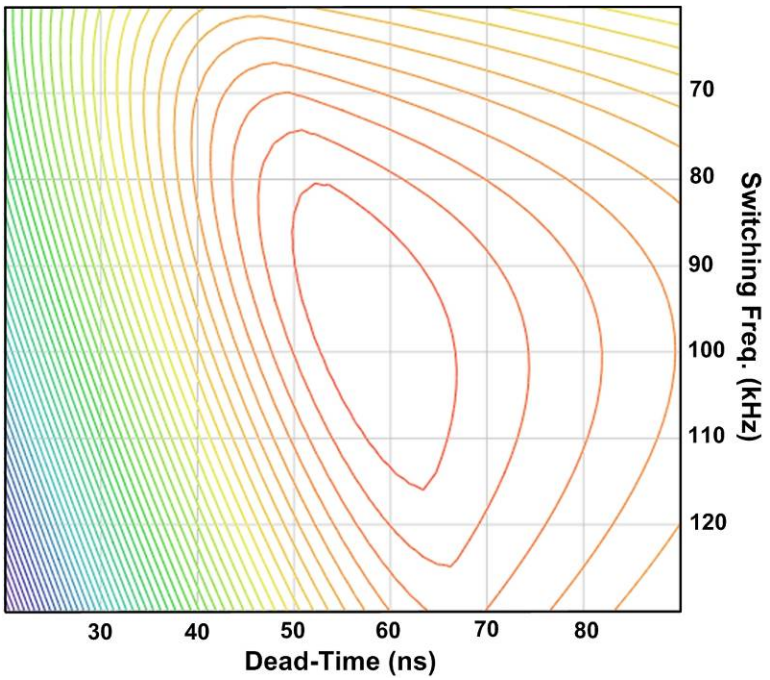

Fig. 4.3 (d): Contour plot for the switching frequency, dead-time and efficiency at load current = 1.0A, optimum F_{sw} = 100 kHz, optimum dead-time = 60ns

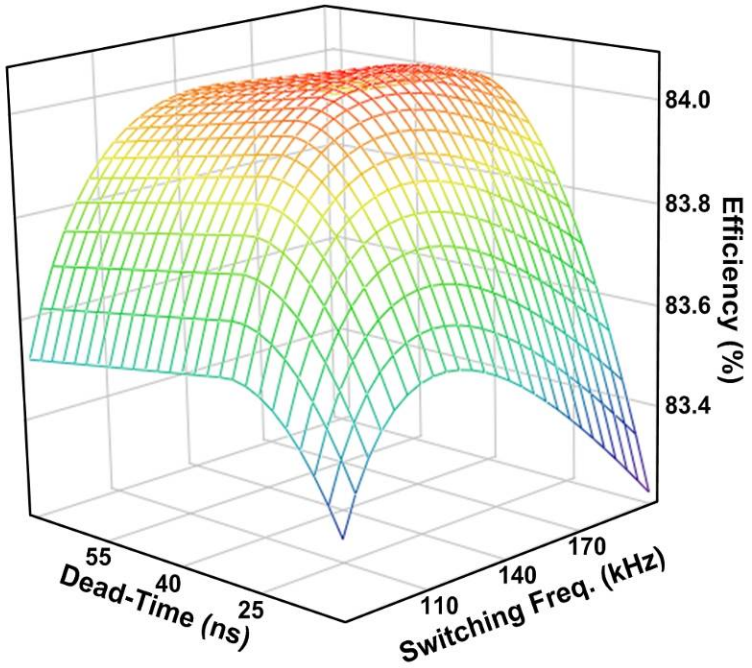

Fig. 4.3 (e): 3D surface plot for the switching frequency, dead-time and efficiency at load current = 6.0A, optimum F_{sw} = 150 kHz, optimum dead-time = 40ns

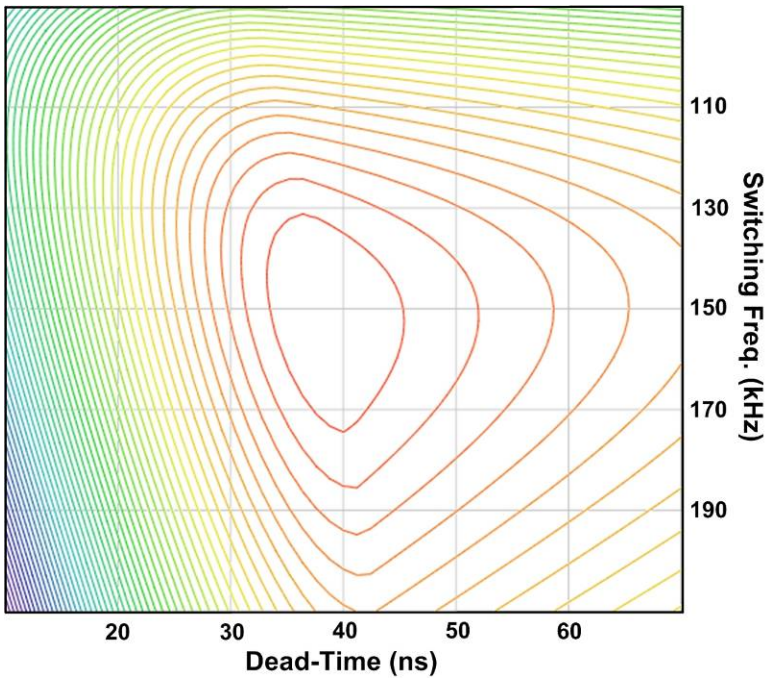

Fig. 4.3 (f): Contour plot for the switching frequency, dead-time and efficiency at load current = 6.0A, optimum F_{sw} = 150 kHz, optimum Dead-Time = 40ns

4.3 Multivariable Adaptive Digital Controller

Fig. 4.4 shows an implementation flowchart for the Multivariable adaptive controller algorithm. From the flowchart, N samples of P_{in} (converter sensed input power) using the ADC and are stored and averaged to generate $P_{in}(n)$. $P_{in}(n)$ is used as an indication of the converter efficiency since the maximum efficiency point occurs at the minimum input power point. P_{in} is used at a later stage to decide the value of the digital controller switching frequency and dead-time values. Next, the Multivariable Adaptive Controller (MVAC) starts optimizing the switching frequency as shown in Fig. 4.4. Switching frequency optimization starts by calculating the difference between the previous value and the new value of P_{in} and the difference between the current value and the previous value of f_{sw} as follows:

$$\Delta P_{in} = P_{in}(n) - P_{in}(n-1) \tag{4.1}$$

$$\Delta f_{sw} = f_{sw}(n) - f_{sw}(n-1) \tag{4.2}$$

After that, a sign comparison between ΔP_{in} and Δf_{sw} is made. If the signs (positive or negative) of Equations (4.1) and (4.2) are similar, this means f_{sw} should be incremented by f_{sw_step} to move toward the maximum efficiency point (or minimum

input power). Otherwise, if the signs of Equations (4.1) and (4.2) are not similar, this means f_{sw} should be decremented by f_{sw_step} to move toward the maximum efficiency point. Increasing the converter efficiency by decreasing the input power indicates a reduction in the total losses to the minimum possible value (optimal switching frequency value). After storing the current values of P_{in} and f_{sw}, the program will decrement or increment f_{sw} and update it. Then, after several (M) switching cycles (enough to reach steady-state), P_{in} is sampled again and the MVAC algorithm starts optimizing the Dead-Time. Dead-Time optimization is done in a similar way to the frequency optimization; first the difference between the previous value and the new value of P_{in} is found, then the difference between the current value and the previous value of d_t is calculated as follows:

$$\Delta d_t = d_t(n) - d_t(n-1) \tag{4.3}$$

After that, a sign comparison between ΔP_{in} and Δd_t is made. If the signs (positive or negative) of Equations (4.1) and (4.3) are similar, this means d_t should be incremented by d_{t_step} to move toward the maximum efficiency point (or minimum input power). Otherwise, if the signs of Equations (4.1) and (4.3) are not similar, this means d_t should be decremented by d_{t_step} to move toward the maximum efficiency point. Increasing the converter efficiency by decreasing the input power indicates a reduction in the total losses

to the minimum value (optimal dead-time value). After storing the current values of P_{in} and d_t, the program will decrement or increment d_t and update it. Then, after several (M) switching cycles (enough to reach steady-state) MVAC algorithm starts optimizing the switching frequency again. The MVAC keep optimizing the switching frequency and the dead-time one step at a time till the global maximum efficiency point is reached.

It must be noted that the compensated control signal D_c that regulates the converter output voltage is generated by a digital controller that also contains the MVAC algorithm. In addition, the MVAC loop bandwidth is much smaller than the output voltage regulation loop bandwidth. Finally it should be noted that the performance curve has a global maximum with respect to the controlling parameter [27,28], consequently the initial values of the controlling parameters and the strategy used in adjusting the parameter will not affect the convergence to the global maximum efficiency.

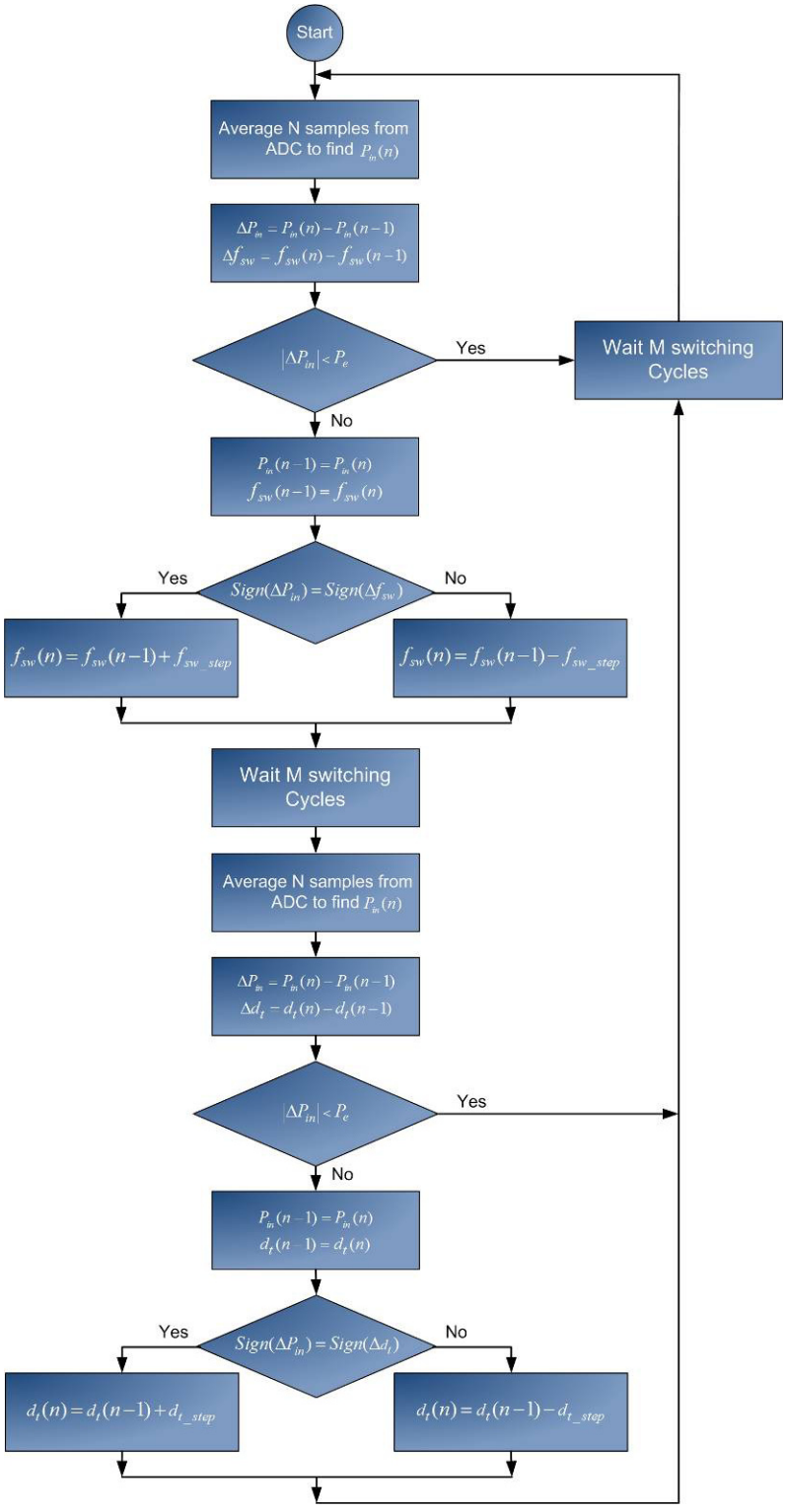

Fig. 4.4: Multivariable adaptive controller (MVAC) flowcharts

4.4 The MVAC Algorithm and its Analysis

Determining the stability and sensitivity for adaptive systems is of great importance since it determines the stable region of operation for the adaptive controller. Multivariable adaptive controller adaptively perturbs DC-DC converter switching frequency and the dead-time to track the optimum system efficiency. In this section theoretical analysis for the stability and sensitivity for multivariable adaptive controller applied to synchronous buck DC-DC converter is discussed and analyzed. The stability and sensitivity analysis for frequency perturbation was discussed in details in Section 2.3.1, the following analysis focus on stability and sensitivity for dead-time perturbation.

4.4.1 Adaptive Dead-Time Optimization

The input power is to be used as a cost function to track the maximum efficiency. Fig. 4.5 shows the input power resulting from perturbing the dead-time. The curve is continuous with one local minimum. It can be noted also from the curve that the minimum input power corresponds to the maximum efficiency. Approximating input current curve as a parabola, which can be represented in Equation (4.4) [64]:

$$P_{in} = P_{in\_\min} + \lambda \cdot (d_t - d_t^*)^2 \tag{4.4}$$

where P_{in} is the input power which is the cost function to be minimized, $P_{in\_\min}$ is the minimum input power, d_t is the dead-time, d_t^* is the optimum dead-time that gives the

minimum input power. λ is proportionality constant. Taking the first derivative of Equation (4.4):

$$\frac{dP_{in}}{d(d_t)} = 2\lambda \cdot (d_t - d_t^*)$$

(4.5)

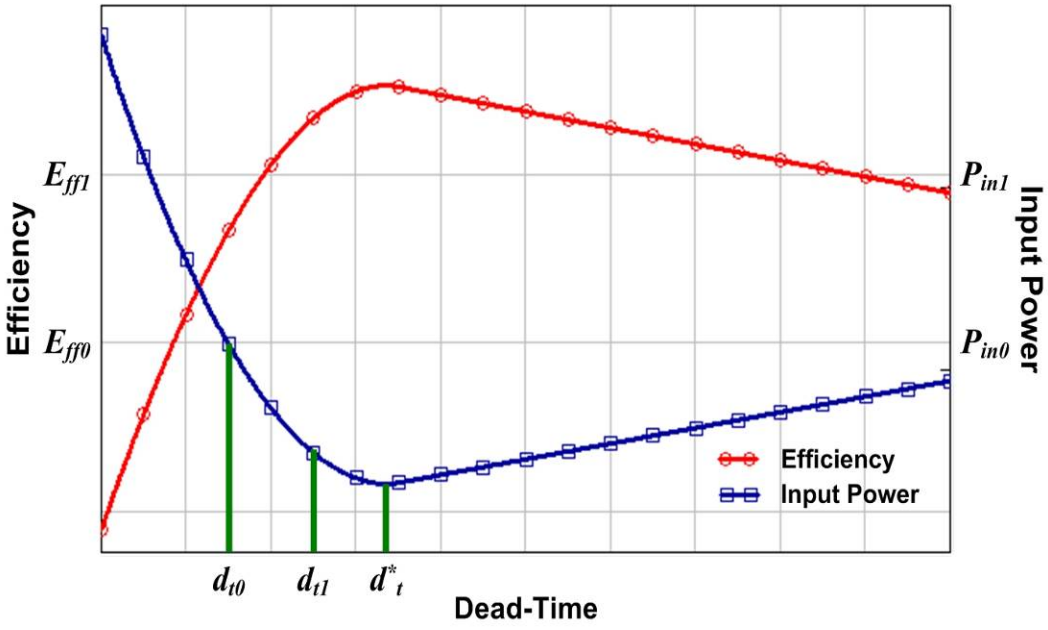

Fig. 4.5 Input current as function of dead-time

The second derivative is a constant value over the entire input current curve:

$$\frac{d^2 P_{in}}{d(d_t)^2} = 2\lambda$$

(4.6)

The main goal of the analysis is to find the optimum dead-time value d_t^* that minimizes the input power/current to its lowest value. At different loads and system parameters the exact input power/current curve is not known, so a search algorithm to find the optimum point is needed. The search algorithm starts with an initial value for the dead-time d_{t0}, then measures the slope of the input power curve at that point. Next the algorithm calculates a new dead-time value d_{t1}, which equals to the old dead-time plus/minus an incremental value. The iterative process repeats until the optimum dead-time d_t^* is found.

4.4.2 Gradient Search Using Steepest Descent Method

There are many algorithms used for gradients search, a simple and practical one is the steepest descent algorithm. This algorithm follows the search method described above and can be represented by Equation (4.7) as [64] :

$$d_{t_{k+1}} = d_{t_k} + \mu \cdot (-\nabla_k) \tag{4.7}$$

where k is the iteration number, $d_{t_{k+1}}$ is the new dead-time value, d_{t_k} is the present dead-time value, μ is a constant that controls stability and convergence of the adaptive loop and ∇_k is the gradient of the cost function at $d_t = d_{t_k}$, using equation (4.5) the gradient ∇_k can be expressed as :

$$\nabla_k = \left.\frac{dP_{in}}{d(d_t)}\right|_{d_t = d_{t_k}} = 2\lambda \cdot (d_{t_k} - d_t^*)$$

(4.8)

The steepest descent adaptive loop dynamics from the initial dead-time iteration d_{t0} to the optimum dead-time value d_t^* can be studied by substituting equation (4.8) into equation (4.7) as [64]:

$$d_{t_{k+1}} = d_{t_k} - 2\mu\lambda \cdot (d_{t_k} - d_t^*)$$

(4.9)

Rearranging the equation:

$$d_{t_{k+1}} = (1 - 2\mu\lambda) \cdot d_{t_k} + 2\mu\lambda \cdot d_t^*$$

(4.10)

Taking the first four iterations of (4.10) gives

$$d_{t_1} = (1 - 2\mu\lambda) \cdot d_{t_0} + 2\mu\lambda \cdot d_t^*$$

(4.11)

$$d_{t_2} = (1 - 2\mu\lambda)^2 \cdot d_{t_0} + 2\mu\lambda \cdot d_t^* \cdot \left[(1 - 2\mu\lambda) + 1\right]$$

(4.12)

$$d_{t_3} = (1 - 2\mu\lambda)^3 \cdot d_{t_0} + 2\mu\lambda \cdot d_t^* \cdot \left[(1 - 2\mu\lambda)^2 + (1 - 2\mu\lambda) + 1\right]$$

(4.13)

$$d_{t_4} = (1-2\mu\lambda)^4 \cdot d_{t_0} + 2\mu\lambda \cdot d_t^* \cdot \left[(1-2\mu\lambda)^3 + (1-2\mu\lambda)^2 + (1-2\mu\lambda) + 1 \right]$$

(4.14)

From those equations, a general expression for d_{t_k} at any iteration can be given as [64]:

$$d_{t_k} = (1-2\mu\lambda)^k \cdot d_{t_0} + 2\mu\lambda \cdot d_t^* \cdot \sum_{n=0}^{k-1} (1-2\mu\lambda)^n$$

(4.15)

$$d_{t_k} = (1-2\mu\lambda)^k \cdot d_{t_0} + 2\mu\lambda \cdot d_t^* \cdot \frac{1-(1-2\mu\lambda)^k}{1-(1-2\mu\lambda)}$$

(4.16)

$$d_{t_k} = d_t^* + (1-2\mu\lambda)^k \cdot (d_{t_0} - d_t^*)$$

(4.17)

4.4.3 Gradient Stability and Convergence

The ratio between successive terms in the summation in equation (4.17) can be defined as $r = 1-2\mu\lambda$, the ratio r is the most important parameter that determine the stability of the adaptive loop. From equation (4.17) it is clear that the iterative process will be stable if

$$|r| = |1-2\mu\lambda| < 1$$

(4.18)

This condition can be expressed also as [64]

$$\frac{1}{\lambda} > \mu > 0$$

(4.19)

If the condition in equation (4.18) or (4.19) is satisfied, the adaptive loop will be stable and will converge to the optimum dead time value [64]:

$$\lim_{k \to \infty} \left[d_{t_k} \right] = d_t^*$$

(4.20)

It can be noted also that the ratio r plays an important role in determining the convergence speed to the optimum solution. Fig. 4.6 shows weight adjustment behavior for the dead-time adaptive loop at different values of r, the adaptive loop starts with initial dead-time of 200ns and tries to reach the optimum dead-time of 50ns. From the figure, it can be noted that the rate of convergence increase as r value decrease reach to its maximum at r=0. Also it can be noted that for positive values of r (Overdamped) there is no oscillation while for negative values (Underdamped) there is an overshoot which decays eventually to the optimum point. Finally at r=0 the system is called critically damped which theoretically yields the fastest convergence [64].

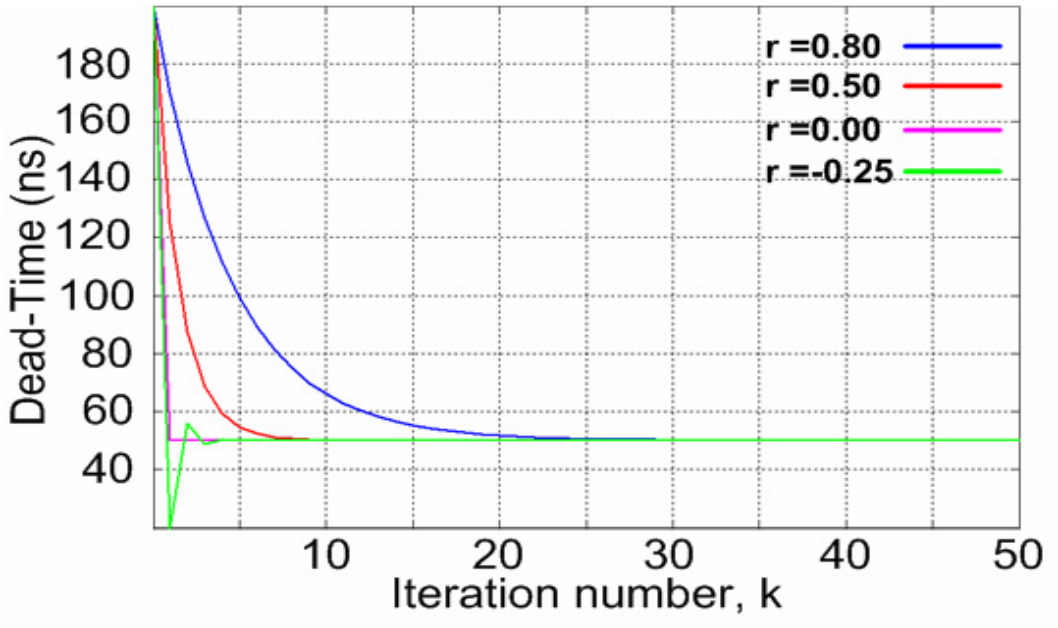

Fig. 4.6 Weight adjustment behavior for dead-time adaptive loop at different values of r

4.4.4 Adaptive Dead-Time Sensitivity Analysis

The sensitivity of the input power P_{in} (or input current assuming the input voltage is either constant or slow changing) to a change in dead-time d_t can be defined as the normalized change in P_{in} over the normalized change in d_t:

$$S_{d_t}^{P_{in}} = \frac{\frac{\Delta P_{in}}{P_{in}}}{\frac{\Delta dt}{dt}} = \frac{\Delta P_{in}}{\Delta dt} \cdot \frac{dt}{P_{in}} \tag{4.21}$$

For MVAC process, where the dead-time dt is changing in successive iterations, the sensitivity can be approximated as:

$$S_{d_t}^{P_{in}} = \frac{\partial P_{in}}{\partial d_t} \cdot \frac{d_t}{P_{in}}$$

(4.22)

Equation (4.22) can also be defined as:

$$S_{d_t}^{P_{in}} = \nabla P_{in} \cdot \frac{d_t}{P_{in}}$$

(4.23)

The expression for the input current gradient function ∇I_{in} can be found as follows:

$$P_{in} = P_{out} + P_{Losses} = V_{out} I_{out} + (P_{Conduction} + P_{Switching} + P_{DeadTime})$$

(4.24)

Yielding,

$$\nabla P_{in} = \frac{\partial P_{in}}{\partial d_t} = \frac{\partial V_{out} I_{out}}{\partial d_t} + \frac{\partial P_{Conduction}}{\partial d_t} + \frac{\partial P_{Switching}}{\partial d_t} + \frac{\partial P_{DeadTime}}{\partial d_t} = \frac{\partial P_{DeadTime}}{\partial d_t}$$

(4.25)

Dead-Time losses can be approximated by

$$P_{DeadTime} = d_t \cdot f_{sw} \cdot V_D \cdot I_{out}$$

(4.26)

This mean the input power gradient for perturbation in dead-time is:

$$\nabla P_{in} = \frac{\partial P_{in}}{\partial d_t} = \frac{\partial P_{DeadTime}}{\partial d_t} = \frac{\partial d_t \cdot f_{sw} \cdot V_D \cdot I_{out}}{\partial d_t} = f_{sw} \cdot V_D \cdot I_{out}$$

(4.27)

Substituting equation (4.27) into equation (4.23), the input power sensitivity due to perturbation in dead-time is give by:

$$S_{d_t}^{P_{in}} = \nabla P_{in} \cdot \frac{d_t}{I_{in}} = \frac{f_{sw} \cdot V_D \cdot I_{out} \cdot d_t}{I_{in}}$$

(4.28)

It should be noted that for the sake of simplicity the first order equation in (4.26) was used to derive the sensitivity analysis. Future research will include deriving a more exact relation which has the 2nd order dependency as in equation (4.4).

4.5 Experimental Results

The MVAC method was prototyped using a digital microcontroller. The experimental power stage is a single phase synchronous buck DC-DC converter with $V_{in} = 10V$, $V_o = 3.3V$, input capacitors $940\mu F$,output capacitors $991\mu F$, output Inductor: $L_o = 2.6\mu H$ with $DCR = 1m\Omega$, upper FET: IRFR5305 [60], two in parallel, lower FET: IRFR2905 [61], two in parallel, and TC428COA FET Driver [62]. The digital microcontroller is used to implement both the MVAC and the output voltage regulation closed loop. The experimental setup uses three 12-bit ADC's with maximum input voltage

of 3.3V to convert the measured parameters. One ADC is used to convert the sensed output voltage; the converted output voltage data is used at a later stage by a digital PID compensator to regulate the output voltage. The second and third ADC's are used for input current sensing and input voltage sensing respectively; the converted data is then processed by the digital controller and utilized by the MVAC algorithm. The synchronous buck converter was designed to be able to switch between CCM and DCM modes of operation depending on the load using the scheme described in AFO experimental result section 1.6.

Fig. 4.7 shows the efficiency versus switching frequency curves obtained from the experimental setup at different loading currents where the switching frequency is varied within a range at each given load.

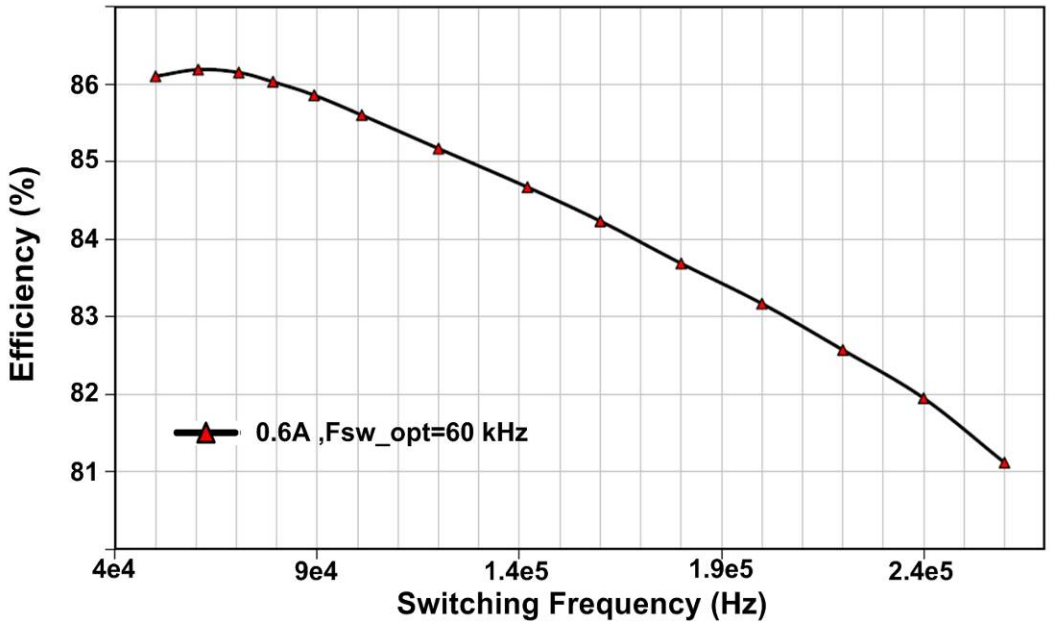

Fig. 4.7 (a): Experimental efficiency vs. switching frequency at 0.6A load at DCM mode.

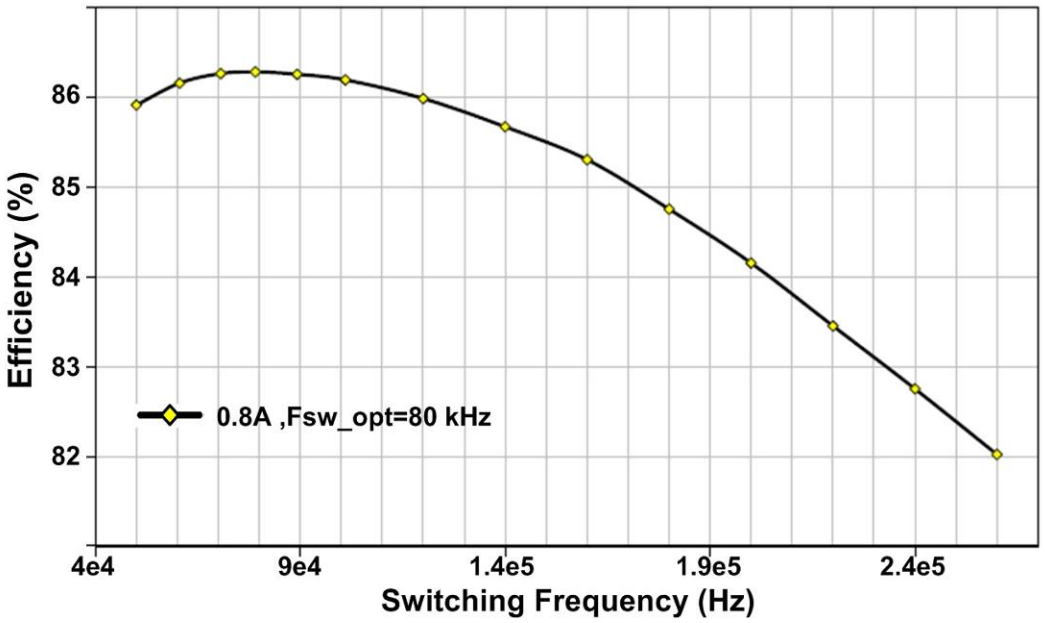

Fig. 4.7 (b): Experimental efficiency vs. switching frequency at 0.8A load at DCM mode.

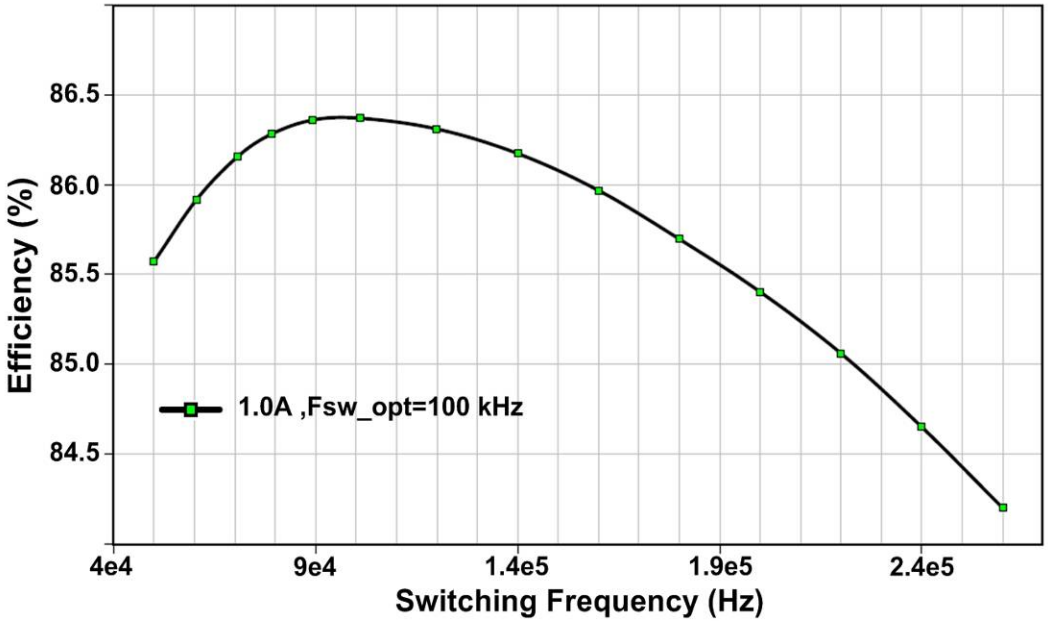

Fig. 4.7 (c): Experimental efficiency vs. switching frequency at 1.0A load at DCM mode.

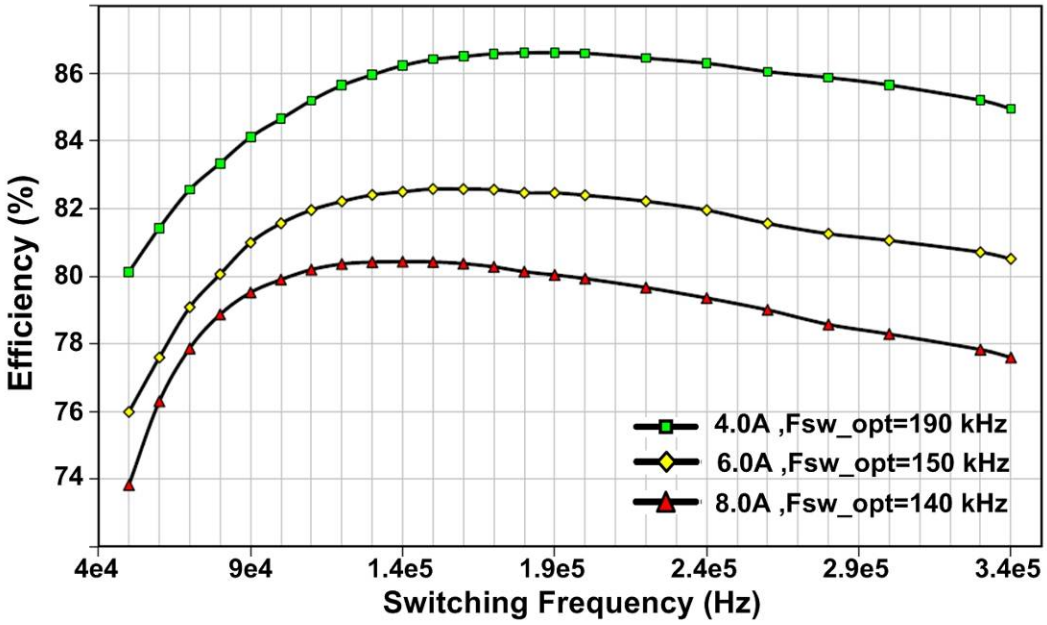

Fig. 4.7 (d): Experimental efficiency vs. switching frequency at different loads at CCM mode.

Fig. 4.8 shows the efficiency versus dead-time curves obtained from the same experimental setup at different loading currents where the dead-time is varied within a range at each given load. From Fig. 4.8, it is clear again that for each load there is an optimized Dead-Time value at which the total switching and conduction losses are minimum and thus efficiency is maximum. It can be noted also from Fig. 4.8 that as the load current increase the optimum Dead-Time value decreased as discussed in section 4.2 dead time effect on losses.

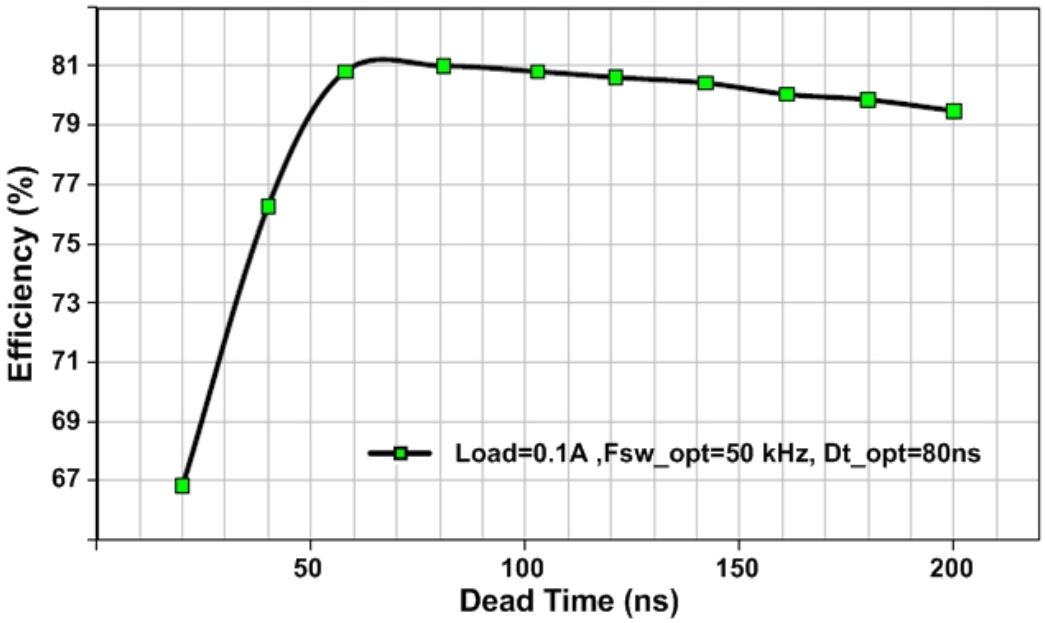

Fig. 4.8 (a): Experimental efficiency vs. dead-time at 0.1A load at DCM mode.

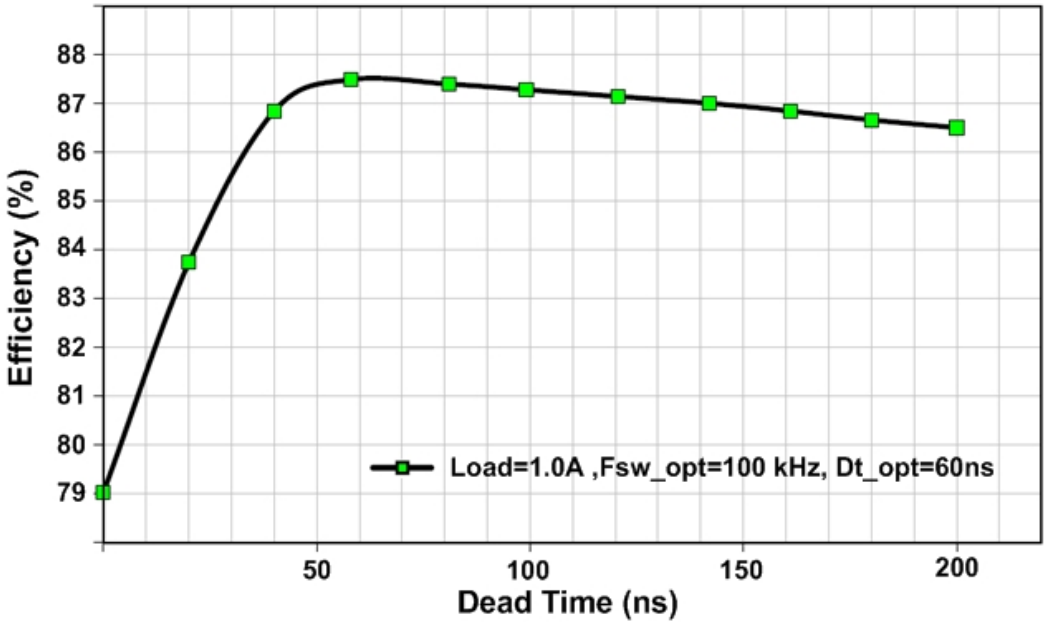

Fig. 4.8 (b): Experimental efficiency vs. dead-time at 1.0A load at DCM mode.

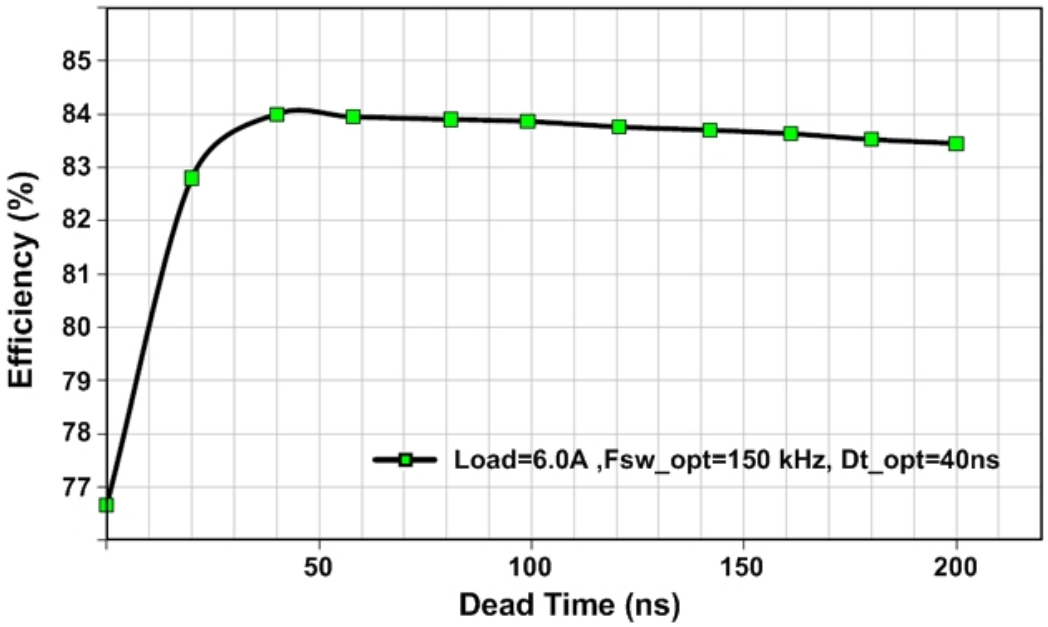

Fig. 4.8 (c): Experimental efficiency vs. dead-time at 6.0A load at CCM mode.

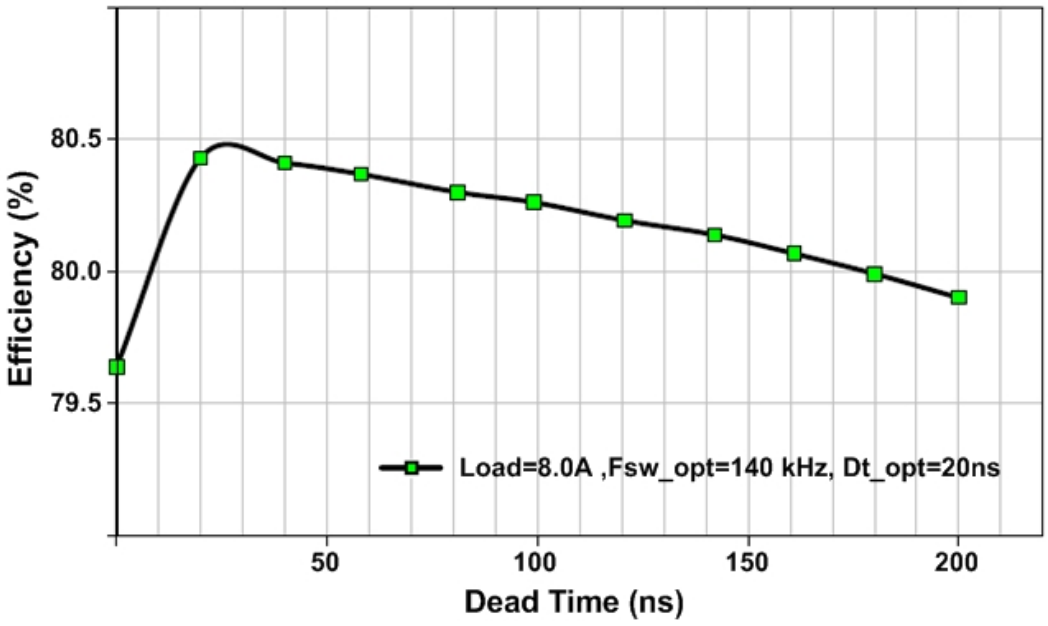

Fig. 4.8 (d): Experimental efficiency vs. dead-time at 8.0A load at CCM mode.

Fig. 4.9 shows a comparison between efficiency improvements resulted from fixed switching frequency with CCM/DCM enabled versus Adaptive Frequency Optimization (AFO) algorithm versus the new Multivariable Adaptive Controller (MVAC) algorithm, as can be noted from the figures, Multivariable adaptive efficiency optimization (MVAC) achieves the highest efficiency improvement compared to AFO or the fixed frequency approach.

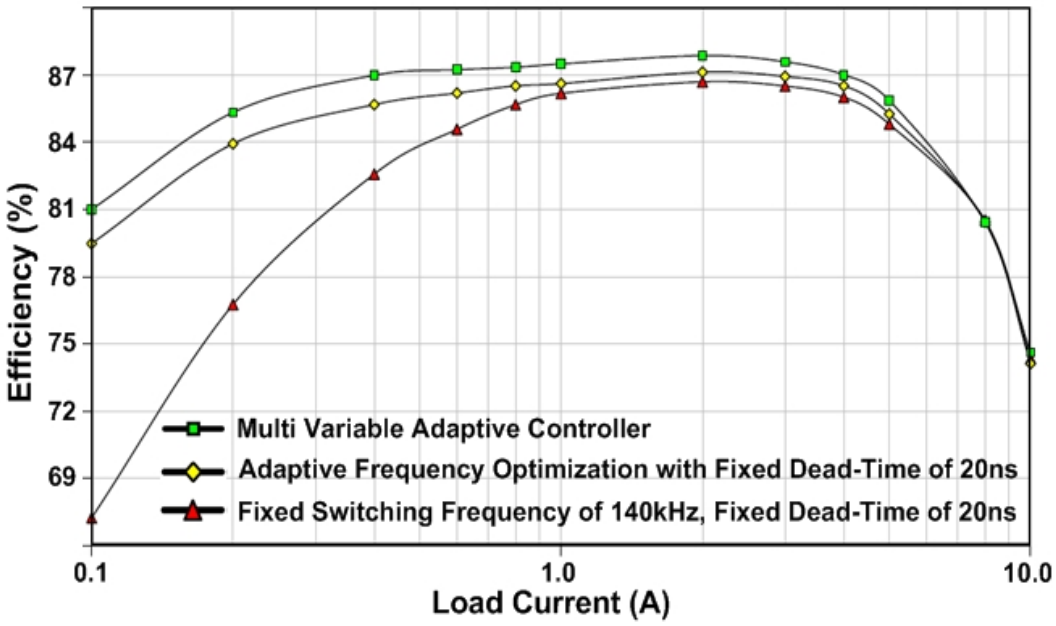

Fig. 4.9 (a): Efficiency comparison between different schemes working at Vin=10V.

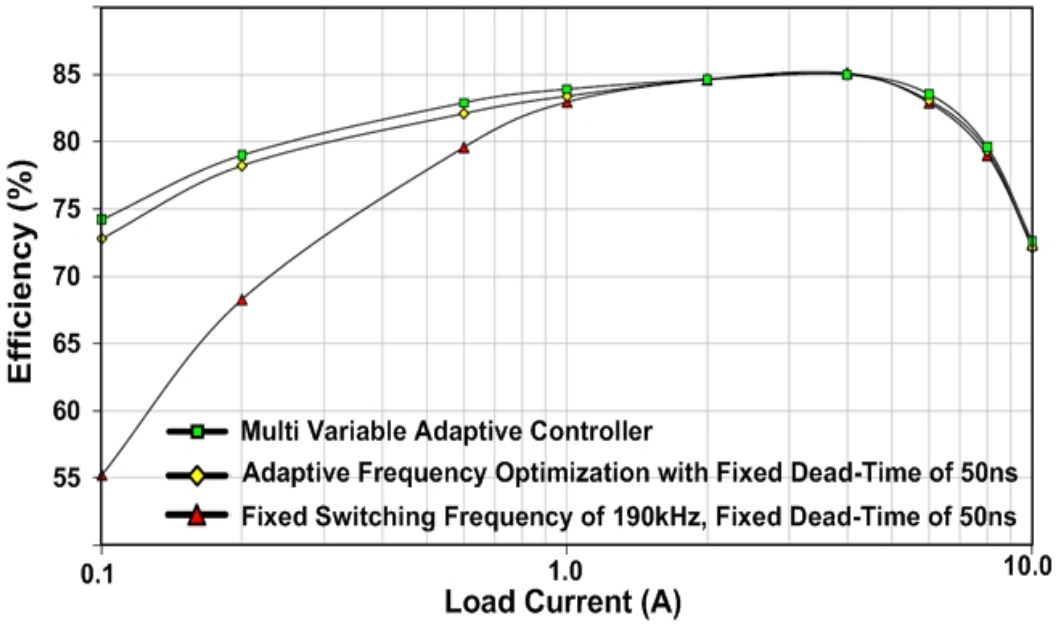

Fig. 4.9 (b): Efficiency comparison between different schemes working at Vin=12V.

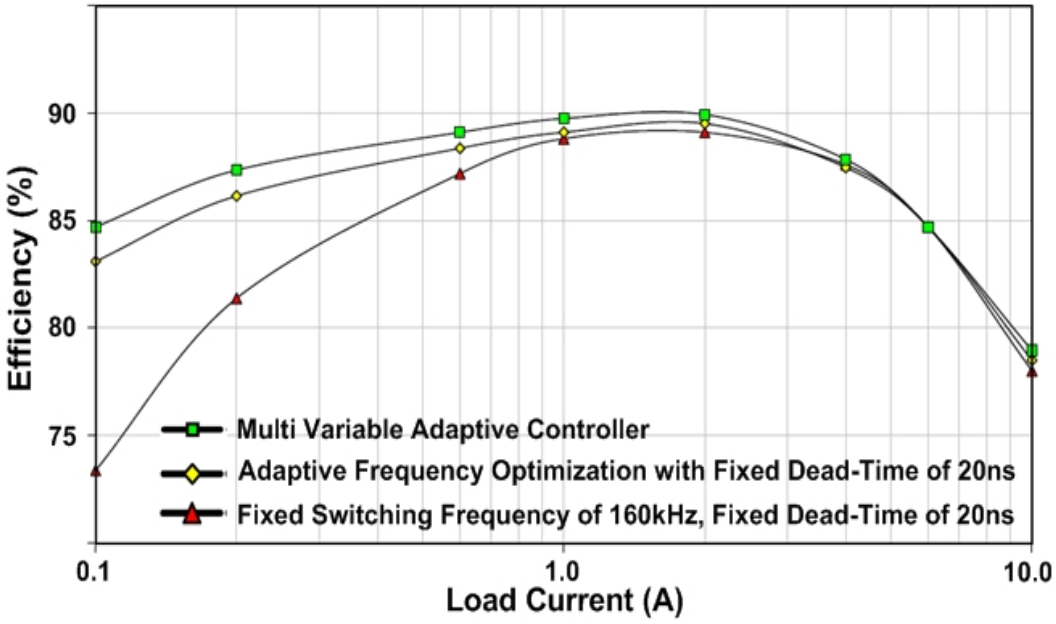

Fig. 4.9 (c): Efficiency comparison between different schemes working at Vin=8V.

Table 4.1 shows efficiency comparison at different input voltages. It can be noticed from Table 4.1 how MVAC controller detects the new optimum (switching frequency, Dead-Time) values and adjusts both variables when the input voltage varies from 8V to 10V to 12V. As the input voltage increases, the optimum (switching frequency Dead-Time) values may be lower or higher depending on the trade off between conduction losses and switching losses.

Table 4.1: Optimum switching frequency and Dead-Time and the resulted efficiency at different input voltages and different load currents

Vin	**8.0V**			**10.0V**			**12.0V**		
Load	$f_{optimum}$ (kHz)	$Dt_{optimum}$ (ns)	Eff (%)	$f_{optimum}$ (kHz)	$Dt_{optimum}$ (ns)	Eff (%)	$f_{optimum}$ (kHz)	$Dt_{optimum}$ (ns)	Eff (%)
0.1A	50.00	40.00	84.70	50.00	80.00	80.99	50.00	80.00	74.20
1.0A	150.00	30.00	89.74	100.00	60.00	87.49	100.00	60.00	83.90
6.0A	160.00	20.00	84.70	150.00	40.00	84.00	160.00	50.00	83.53
8.0A	140.00	10.00	80.43	140.00	20.00	80.43	150.00	40.00	79.61

Finally, Fig. 4.10 shows how the MVAC algorithm moves toward the optimum switching frequency and Dead-Time values in different loading conditions. In Fig 4.10 (a) and the related contour plot 4.10 (b) the MVAC algorithm tries to find the optimum operating points for 1A load current working at 12V input voltage. The algorithm starts with switching frequency of 50 kHz and Dead-Time value of 150ns. MVAC iterates 10 times with switching frequency step size of 10 kHz and Dead-Time step size of 20ns to

reach the optimum points of switching frequency of 100 kHz and Dead-Time value of 60ns. After finding the optimum working points, the algorithm keep moving between two or more points around the optimum values as shown in Fig. 4.11 (a) which shows number iteration vs. switching frequency and Fig. 4.11 (b) which shows number of iteration vs. the Dead-Time value.

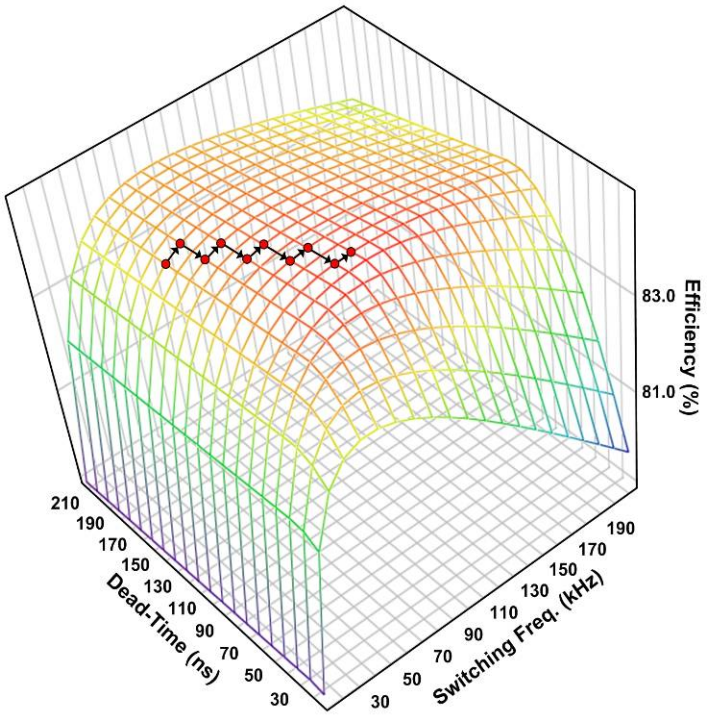

Fig. 4.10 (a): 3D surface plot that shows how the MVAC algorithm approaches the optimum efficiency point (fsw_opt = 100 kHz, Dt_opt=60ns) for 1.0A load current.

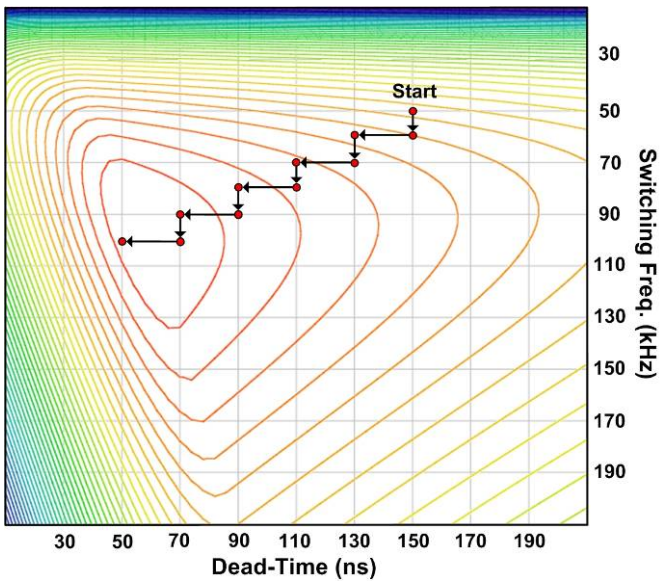

Fig. 4.10 (b): Contour plot that shows how the MVAC algorithm approaches the optimum efficiency point (fsw_opt = 100 kHz, Dt_opt=60ns) for 1.0A load current.

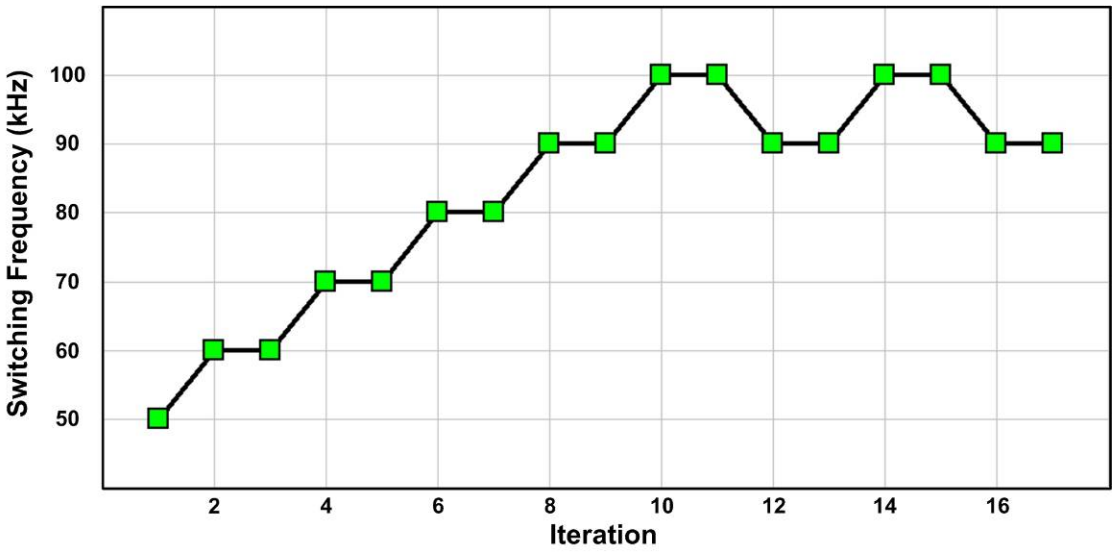

Fig.4.11 (a): Iteration vs. switching frequency for 1.0A load current example.

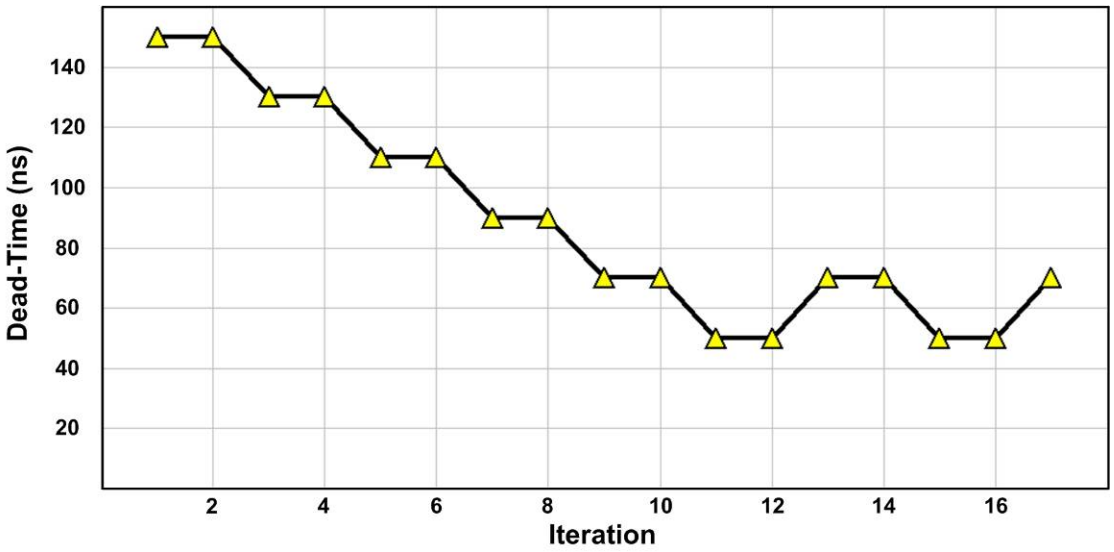

Fig.4.11 (b): Iteration vs. dead-time for 1.0A load current example

In Fig 4.12 (a) and 4.12 (b) the MVAC algorithm tries to find the optimum operating points for 4A load current working at 12V input voltage. The algorithm starts with switching frequency of 300 kHz and Dead-Time value of 10ns. MVAC iterates 22 times with switching frequency step size of 10 kHz and Dead-Time step size of 20ns to reach the optimum points of switching frequency of 190 kHz and Dead-Time value of 50ns. After finding the optimum working points, the algorithm keep moving between two or more points around the optimum values as shown in Fig. 4.13 (a) which shows number iteration vs. switching frequency and Fig. 4.13 (b) which shows number of iteration vs. the Dead-Time value.

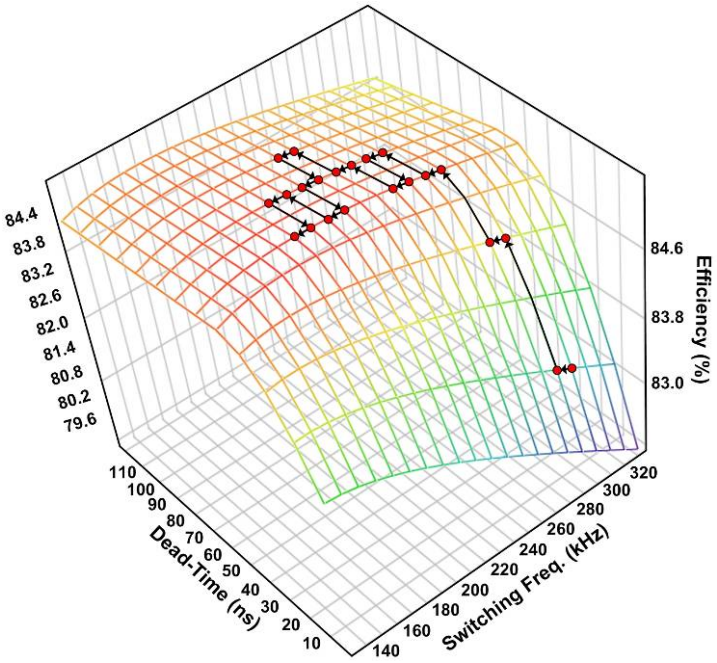

Fig. 4.12 (a): 3D surface plot that shows how the MVAC algorithm approaches the optimum efficiency point (fsw_opt = 190 kHz, Dt_opt=50ns) for 4.0A load current.

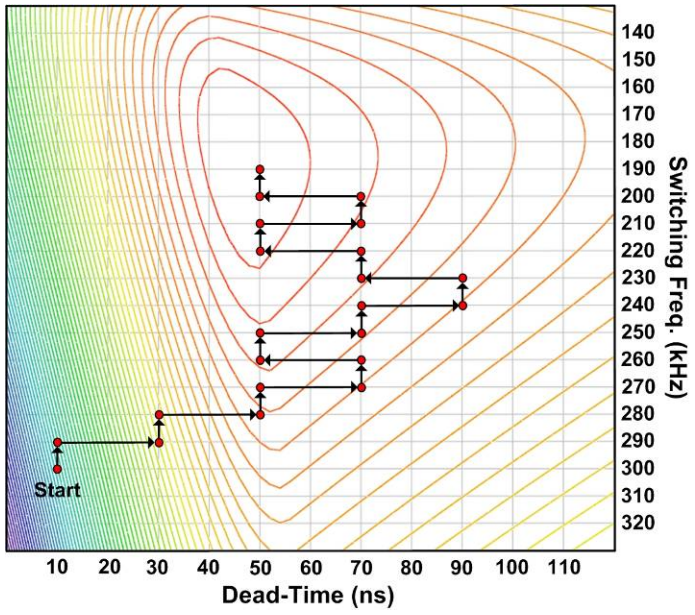

Fig. 4.12 (b): Contour plot that shows how the MVAC algorithm approaches the optimum efficiency point (fsw_opt = 190 kHz, Dt_opt=50ns) for 4.0A load current.

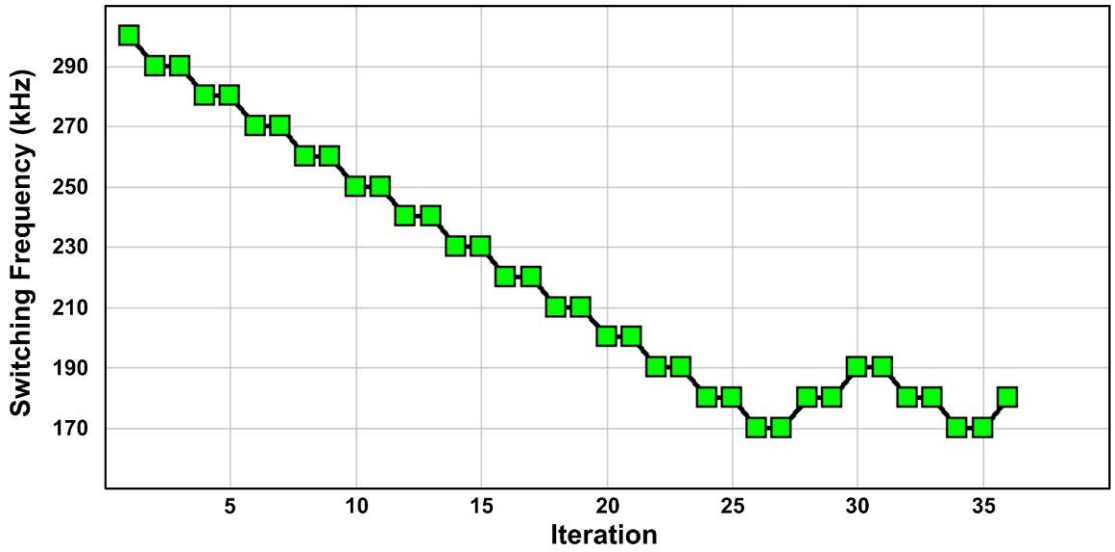

Fig.4.13 (a) Iteration vs. switching frequency for 4.0A load current example

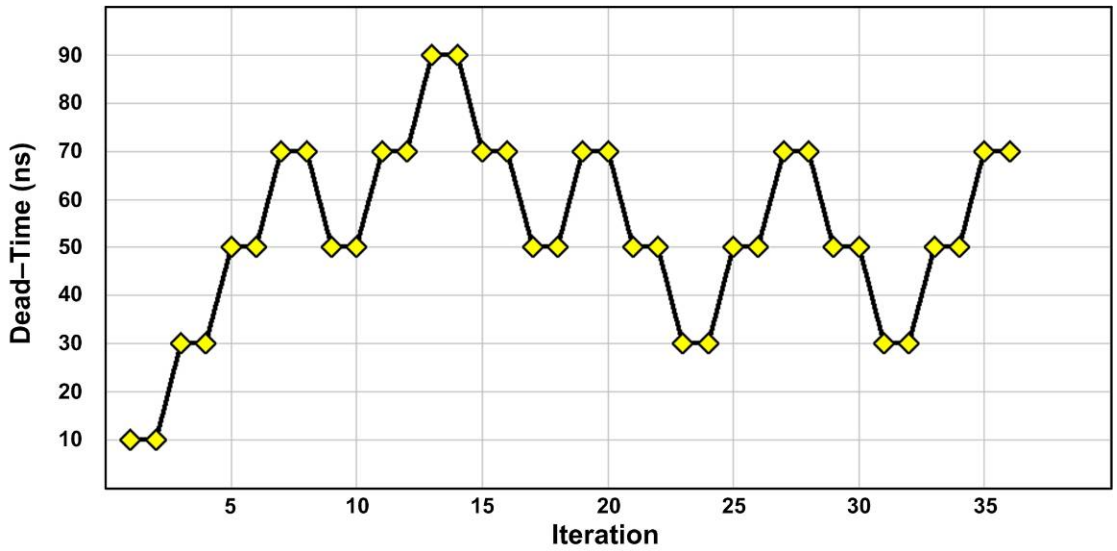

Fig.4.13 (b) Iteration vs. dead-time for 4.0A load current example

4.6 Conclusion

An adaptive digital control method to maximize the converter efficiency is presented in this chapter. The Multivariable Adaptive Controller (MVAC) tracks the minimum input power point, by changing the switching frequency f_{sw} and dead-time values under variable operating conditions such as load variations, voltage variations, components variations, aging effects, and temperature effects. The optimum switching frequency and dead-time values results in the lowest converter total losses (maximum converter efficiency). The MVAC was verified experimentally and compared to other adaptive schemes. From the experimental results, it can be shown that the proposed MVAC algorithm converges to the optimal efficiency points. Also that the proposed multivariable adaptive controller (MVAC) achieves better efficiency compared to adaptive frequency optimization (AFO) or dead-time optimization alone.

CHAPTER FIVE
SUMMARY AND FUTURE WORK

5.1 Summary

Digital control is a new promising direction that offers many advantages over analog controllers. The ability of digital controllers to apply advanced non-linear control algorithms opens the door for more exciting control opportunities. This work focuses on moving with power converters digital control design beyond the conventional closed loop practice, into more advanced control schemes that will take the full advantage of digital controller's capabilities to harvest the benefits of improved efficiency, and enhanced dynamics. The following is a summary of the work covered in this dissertation.

In Chapter 2, an adaptive digital control method to maximize the converter efficiency and to improve its stability under variable switching frequency operation was presented. The proposed AFO digital controller tracks the minimum input power point, by adjusting the switching frequency f_{sw}. The optimum f_{sw} value results in the lowest converter total losses (maximum converter efficiency).

The need for a controller that tracks the optimum switching frequency under variable conditions is discussed. These conditions include components variations and aging, input voltage variations, and load variations. Even though such conditions are assumed and approximated at the time of converter design, they may vary significantly such that the conversion efficiency is compromised. Moreover, two issues which are

associated with variable switching frequency operation in digital controllers that do not exist in analog controllers, are reviewed. These are the limit cycle oscillation and the closed loop gain and phase variations as a result of the switching frequency variations.

While the AFO part of the proposed digital controller tracks the optimum switching frequency under variable operating conditions to result in high conversion efficiency, the DLCA part of the digital controller alleviates the issues of limit cycle oscillation and gain-phase variation associated with variable switching frequency in digital controllers. The AFO-DLCA concepts and controller algorithms are discussed and analyzed in this chapter. The design theory and guidelines of the presented AFO-DLCA controller are presented and used to design for the proof of concept experimental prototype. The proof of concept experimental results is in good agreement with the theoretical results.

In Chapter 3, a self auto-tuning algorithm with adaptive variable-step-size to track and detect the optimum switching frequency of DC-DC converter under variable operating conditions such as load variations, voltage variations, components variations and aging effects. The Variable-Step-Size (VSS) algorithm was theoretically developed and analyzed based on buck DC-DC converter loss model, and a general expression for the gradient function that describes the VSS algorithm was given. The experimental results were compared for both fixed step size algorithm and the adaptive variable step size algorithm. It is shown that the proposed Variable-Step-Size adaptive algorithm achieves better trade off between speed and accuracy compared to the fixed step size algorithm.

In Chapter 4, an adaptive digital control method to maximize the converter efficiency is presented in this chapter. The Multivariable Adaptive Controller (MVAC) tracks the minimum input power point, by changing the switching frequency and dead-time values under variable operating. The optimum switching frequency and dead-time values results in the lowest converter total losses (maximum converter efficiency). The MVAC was verified experimentally and compared to other adaptive schemes. From the experimental results, it can be shown that the proposed MVAC algorithm converges to the optimal efficiency points. Also that the proposed multivariable adaptive controller (MVAC) achieves better efficiency compared to adaptive frequency optimization (AFO) or dead-time optimization alone.

5.2 Future Work

Adaptive efficiency optimization for digitally controlled power converter is a new topic that tries to utilize exiting adaptive signal processing techniques for the benefits of power electronics industry. In this work, different adaptive techniques were proposed and experimentally verified. However, this work is still in its early stages, and much more can be done, the following summarize suggested future research work.

In Chapter 2, an adaptive method to optimize the efficiency of DC-DC converter and to improve the dynamic response was presented. Steepest descent algorithm was used to find the optimum switching frequency, future work will include studying and investigating more advanced adaptive techniques to find the optimum frequency and comparing those different techniques in terms of accuracy and speed. Also, the work done so far was for DC-DC converters, future work will include studying other candidate topologies that can benefit from applying the AFO technique such as PFC and DC-AC.

In Chapter 3, a self auto-tuning algorithm with adaptive variable-step-size to track and detect the optimum switching frequency of DC-DC converter under variable operating conditions was presented. The algorithm was developed using Taylor series first order approximation. Future work will investigate using higher order approximation that could benefit in further reduction in the total number of steps, and/or hitting the optimum switching frequency more precisely.

In Chapter 4, an adaptive digital control method to maximize the converter efficiency by optimizing two variables at the same time (switching frequency and dead-time) was presented. The Multivariable Adaptive Controller (MVAC) optimizes one

variable at a time (single step perturbation) to reach to global efficiency point. Future research work will include studying more advanced techniques to perturb two variables at the same time. Also, The MVAC algorithm used fixed step size to reach the optimum point, future work will investigate utilizing the knowledge gained in chapter 3 to benefit in reducing the number of steps and/or hitting the optimum efficiency points more precisely. Finally, in this research only two variables were used, future work will study how to perturb three or more variable to hit even greater efficiency numbers.

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