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CLASS F AND INVERSE CLASS F POWER AMPLIFIER SUBJECT TO ELECTRICAL STRESS EFFECT

by

GIJI SKARIA
B.S. University of Madras, 2000

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
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Summer Term
2011

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ABSTRACT

This study investigated the Class F and inverse Class F RF power amplifier operating at 5.8 GHz. The major challenging issue in design and implementation of CMOS power transistor is the breakdown voltage especially in sub-micron CMOS technologies. In order to eliminate this problem a Cascode topologies were implemented to reduce the Drain-to-Source voltage (stress). A Cascode Class F & Inverse Class F RF power amplifier were designed, and optimized in order to improve efficiency and reliability using 0.18μm CMOS technology process. A 50% decrease in the stress has been achieved in the Cascode class-F and Inverse class F amplifiers.

The sensitivity and temperature effect were investigated using BSIM-4 model. Such an amplifier was designed and optimized for a good sensitivity. A substrate bias circuit was implemented to achieve a good sensitivity.

Recommendations were made for future advancements for modification and optimization of the class F and inverse class F circuit by the application of other stress reduction strategies, and improvement of the substrate bias circuit for a better sensitivity.

To my Parents

ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Jiann S. Yuan, for his continuous commitment to help and support me through my graduate career. His advice, technical and otherwise, has been valuable to my experience as a graduate student and a person. I would also like to thank my committee members, Dr. Kalpathy Sundaram and Dr. Lee Chow, for their support throughout my years at UCF.

My heartfelt gratitude goes out to all of my colleagues at the lab – Jason Steighner, Divya Narasimha Raju, Shuyu Chen, Yiheng Wang, Ms. Yuying Zhang, Mr. Karan S Kutty, Mr. Chengcheng Xiao, and Gabriel Vazquez. Especially, I discussed lots of issues with Shuyu and Karan about the analysis, design, implementation, and optimization of RF circuit.

Last, but not least, I would like to thank my wife Seena Thomas for her support, understanding and love during the past few years. Her support and encouragement was in the end what made this thesis possible. My parents –Mr. Skaria and Mrs.Annakutty, parent-in-law – Mr.Thomas and Mrs.Chinnamma, and my brothers, sisters and friends receive my deepest gratitude and love for their dedication, prayer, love and support during my studies.

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LIST OF ACRONYMS/ABBREVIATIONS

ADS	Advance Design System
CMOS	Complementary Metal Oxide Semiconductor
TSMC	Taiwan Semiconductor Manufacturing Company
BSIM	Berkeley Short-Channel IGFET model
IGFET	Insulated Gate field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
LPF	Low Pass Filter
HPF	High Pass Filter
LO	Local Oscillator
LNA	Low Noise Amplifier
DC	Direct Current
PA	Power Amplifier
PAE	Power Added Efficiency
DE	Drain Efficency

V_{DS}	Drain to Source Voltage
I_{DS}	Drain to Source Current
P_{out}	Power Output
RF	Radio Frequency

CHAPTER ONE: INTRODUCTION

Now a day the wireless technology is growing as well as scaling consistently, high efficiency and good reliability is the most spoken component in the RF technology. The main power consumption in a RF system is the power amplifier. The design of an acceptable power level, efficiency and gain remains one of the major challenges in today's pursuit of single chip integrated power amplifiers. There are different type of classes of power amplifier already implemented according to the efficiency, power output, linearity and method of operation.

An introduction to RF communication

In a modern wireless communication where the mobile phones and other wireless communication devices are used, there has been significant improvement is the processing technology, and as a result there has been an increase in circuit performance as well as scaling. These circuits provide even more efficiency and power output compared to the older technology. A basic block diagram of a transceiver is show in Figure 1.

Let's take a look at the receiving section of the transceiver. The signal is received by an antenna, in a cell phone it will be patch antenna or a parabolic, sector antenna etc. in the case of a base station. Since this signal has travelled a very large distance, there is a significant attenuation and noise added to the fundamental signal. In order to condition this noise signal, the signal is

sent to a Low-Noise Amplifier (LNA). The amplified signal sent to a mixer in order to shift it to a lower frequency. This could be in GHz range. The output of the mixer is send to an analog-to-digital (ADC) in order to convert the analog signal to the digital. The converted digital signal then sends to the Micro Processor for further processing.

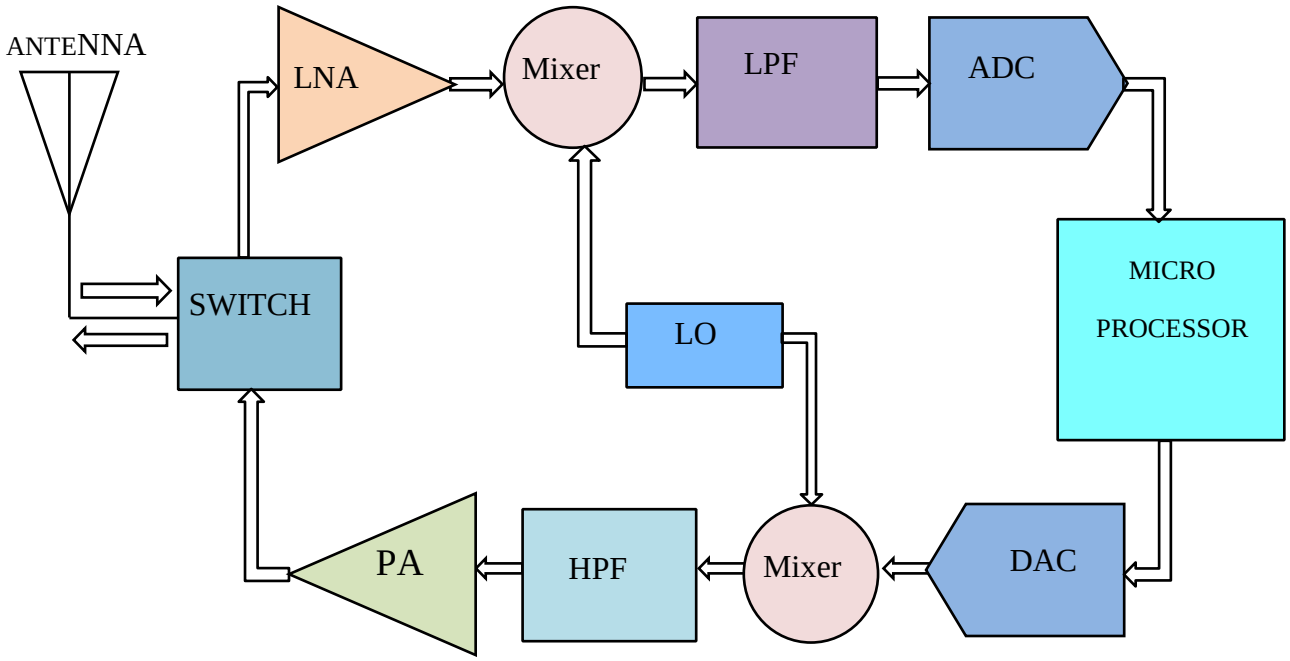

Figure 1: Basic block diagram of transceiver circuit

On the transmission side, the digital data coming from the micro processor are converted to an analog signal using a digital-to-analog converted (DAC). This analog signal sends to a mixer to shift the signal frequency to higher frequency. The reason for the frequency shifting to higher is the frequency which is using for transmission is much higher than the digital signal output. The resulting signal is now amplified using a RF power amplifier and transmitted using

an antenna. The power amplifiers are used just before the antenna because the signal needs to be amplified in order to travel large distance from the antenna.

Back in the early days of wireless communication, the class A and Class AB are predominantly the choices of PA design. However the increasing demand for longer battery life and smaller wireless mobile devices, the CMOS class F power amplifier has become very popular due to its high efficiency and high output power capability. The class –F approach has been developed in the frequency domain as a means of increasing the efficiency over class-A and class-AB. The class –F power amplifier uses the multiple harmonics resonator output filter to control the harmonic content of it drain-to source voltage and drain current waveforms, thereby shaping them to reduce the power dissipation by the transistor and thus to increase the efficiency of the power amplifier.

A high efficiency CMOS C-band class F- power amplifier with 42.8% PAE at a low supply voltage of 1.9 V V_{DD} has been established in [7]. As far as electrical stress effect concerned, a single stage class F- power amplifier on 65 nm CMOS at 60GHz have been studied and established in [6]. Fully integrated single stage classes F- power amplifier using CMOS technology at 2.4 GHz with P_{out} of 21.8dBm and *PAE* of 43.95% have been established in [4]. A 29 dBm P_{out}, 900MHz single stage class F- power amplifier with high efficiency of 56% *PAE* using 0.18 µm TSMC CMOS technology have been established in [2].

Study of reliability and hot carrier stress has been already established for the single stage class –F power amplifier earlier. The Cascode class F amplifier and its reliability and stress study have been investigated the first time in this paper. We designed the Cascode both class F and inverse-class F power amplifier and evaluate the result with conventional class-F and inverse class F power amplifier in terms of *PAE, P_{out}, DE,* in domain of power input and gate-to-drain resistance and also did the analysis of V_{DS} (stress effect) of the main transistor in time domain.

CHAPTER TWO: IDEAL CLASS-F POWER AMPLIFIER

When the RF power amplifier comes to the practical application, there are different types of amplifiers can be applied Different amplifiers classes can be achieve depend on the application and its requirements. Table 1 shows the different types of all well known classes of amplifiers.

Class	Conduction Angle (%)	Drain Efficiency (%)	Mode of operation
A	100%	50%	Current source
B	50%	78.5%	Current source
AB	50%-100%	50%-78.5%	Current source
C	<50%	100%	Current source
D	50%	100%	Switch
E	50%	100%	Switch
F	50%	100%	Switch

Table 1 Power amplifiers class Comparison

There are mainly two mode of operation in switching transistor either current source or as a switch. The drain efficiency is depends on the conduction angel. Since the class A amplifier is on the entire conduction angle the power dissipation is more and the efficiency is capped at 50%. In order to increase the efficiency, the conduction angle must reduce as much as possible. Since

the switching mode will reduce the overlapping of the voltage and current waveforms which will help to increase the efficiency. Ideally C, D, E and F are most efficient amplifiers. Especially D, E and F are 100% efficient amplifier since the mode of operation is in switched mode. C, D, E, and F are ideally most efficient power amplifiers. Class C power amplifier provides less P_{out} but class D power amplifiers provides undesired harmonics, requiring higher order filters. Class E power amplifiers the transistor under more stress about 3.6 times V_{DD} but Class F power amplifiers transistor stress about 2 times V_{DD} . There is a trade-off between efficiency and circuit complexity. The circuit diagram of Class F Power Amplifier is complex. The output harmonic tuning circuit also serves as the output matching

Class F power amplifier

Figure 2 shows the ideal class F RF power amplifier circuit with tuned circuit.

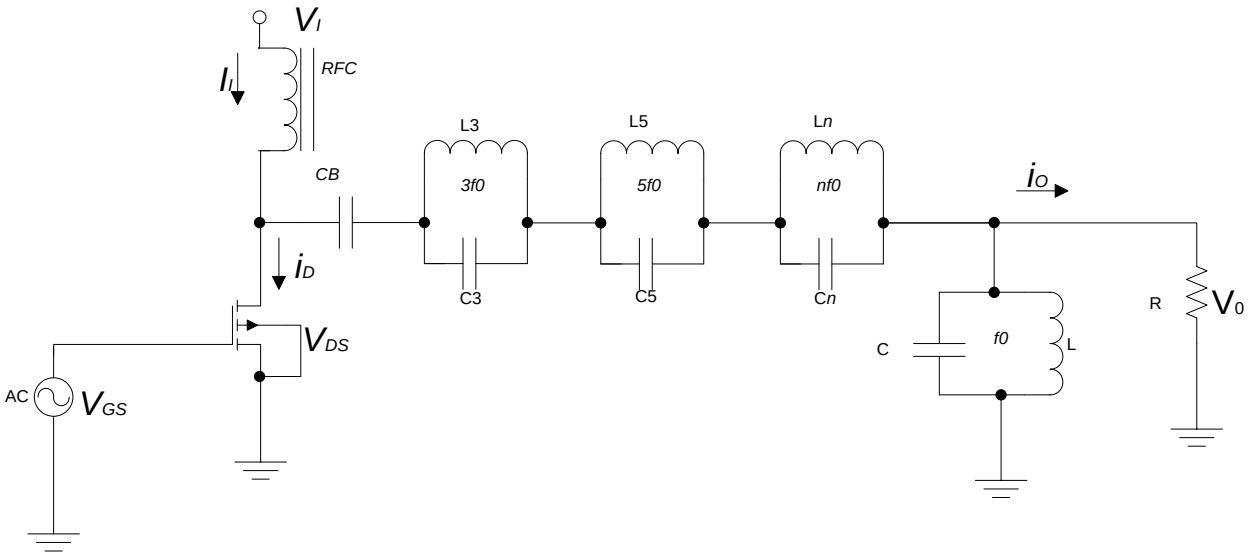

Figure 2: Ideal class F power amplifier

Mainly there are two types of class F power amplifier, such as class F power amplifiers and inverse class F amplifier. The Class F RF Power Amplifiers utilize multiple harmonic resonators in the output network to shape the drain to source voltage (V_{DS}) such that the transistor switching loss is reduced and the efficiency is increased. The drain current flows when the drain to source voltage is low, and the drain to source voltage is high when the drain current is zero. Therefore the result of drain current and drain to source voltage is low is reducing the power dissipation in the transistor. In a class F amplifier with odd harmonics, the drain to source voltage contains only odd harmonics and the drain current contains only even harmonics. Therefore the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics.

The drain to source voltage V_{DS} of class F amplifiers with odd harmonics is symmetrical for the lower and upper half of the cycle.

The V_{DS} of odd harmonics is given by

$$V_{DS} = V_I - V_m \cos \omega_0 \, t + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos n \, \omega_0 \, t \quad (1)$$

The drain current i_D given by

$$i_D = I_I - I_m \cos \omega_0 \, t + \sum_{n=2,4,6,\ldots}^{\infty} I_{mn} \cos n \, \omega_0 \, t \quad (2)$$

Inverse class F power amplifier

Figure 3 shows the inverse class F power amplifier circuit with n number of tuned harmonic tank circuit.

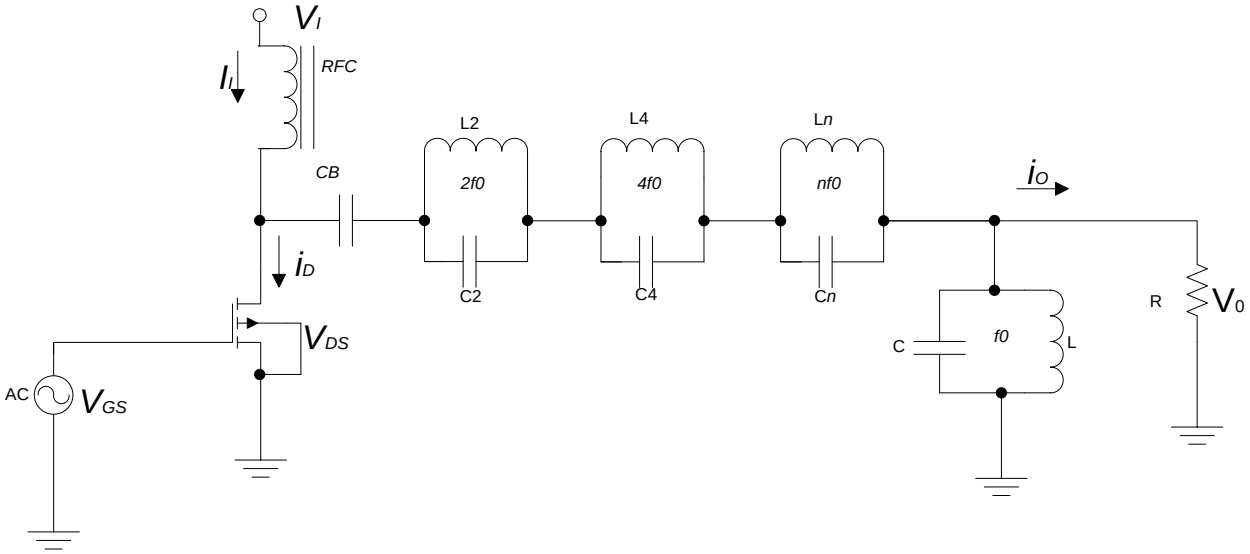

Figure 3: Ideal inverse class F power amplifier

In a class F amplifier with even harmonics, the drain to source voltage contains only even harmonics and the drain current contains only odd harmonics. Therefore the load network represents an open circuit at even harmonics and a short circuit at odd harmonics. The drain to source voltage V_{DS} of class F amplifiers with odd harmonics is not symmetrical for the lower and upper half of the cycle.

Since high efficiency is one of the most required components in the class F power amplifier, we are going for inverse-class F power amplifier which giving more efficiency than the traditional class F power amplifier. The main difference of the inverse-class F amplifier from the traditional class F amplifier is the output harmonic tuning method. In inverse-class F amplifier the even harmonics is tuning instead odd to shape the drain current to be a square and the drain-to – source voltage will be a sine wave form.

This circuit contain the output tuning circuit with even harmonic and fundamental harmonics frequencies, by tuning this we can achieve the drain current is in square wave form and the drain-to-source voltage is in sine waveform, this will raise the efficiency and output power of the amplifier. The even harmonic treatment circuit has 1 pole point at $2f_0$ and 4 f_0 zero point at $3f_0$. The fundamental harmonic tunic circuit has pole at f_0 and zero point at $3f_0$.

The V_{DS} of odd harmonics is given by

$$V_{DS} = V_I - V_m \cos \omega_0 \, t + \sum_{n=2,4,6,\ldots}^{\infty} V_{mn} \cos n \, \omega_0 \, t \tag{3}$$

The drain current i_D given by

$$i_D = I_I - I_m \cos \omega_0 \, t + \sum_{n=3,5,7,\ldots}^{\infty} I_{mn} \cos n \, \omega_0 \, t \tag{4}$$

Figure 4 shows the ideal waveform of a class F power amplifier. From the figure the drain-to-source voltage is square wave form and drain current is in sign wave form. The ideal class F power amplifier assumes the inclusion of an infinite number of harmonics, which is unrealistic in the designs. The number of harmonics used in the class F power amplifier is a tradeoff between complexity and efficiency. Figure shows the voltage and current waveforms of the class F power amplifier with the third harmonic. The drain current waveform have any conduction angle $2\theta < 2\pi$, which contains higher harmonics. In most applications, the conduction angle is $\theta=\pi$, like in the class B amplifier. In the class F amplifier, the drain current is a half – sine wave given by

$$i_D = i_{DM} \cos \omega_0 \, t \qquad for -\frac{\pi}{2} < \omega_0 t \leq \frac{\pi}{2} \tag{5}$$

$$i_D = 0 \qquad for \frac{\pi}{2} < \omega_0 t \leq \frac{3\pi}{2} \tag{6}$$

Where I_{DM} is the peak value of the drain current, which occurs $\omega t = 0$. The output resonant circuit tuned to the fundamental frequency f_0 acts like a band-pass filter and filters out all the harmonics of the drain current.

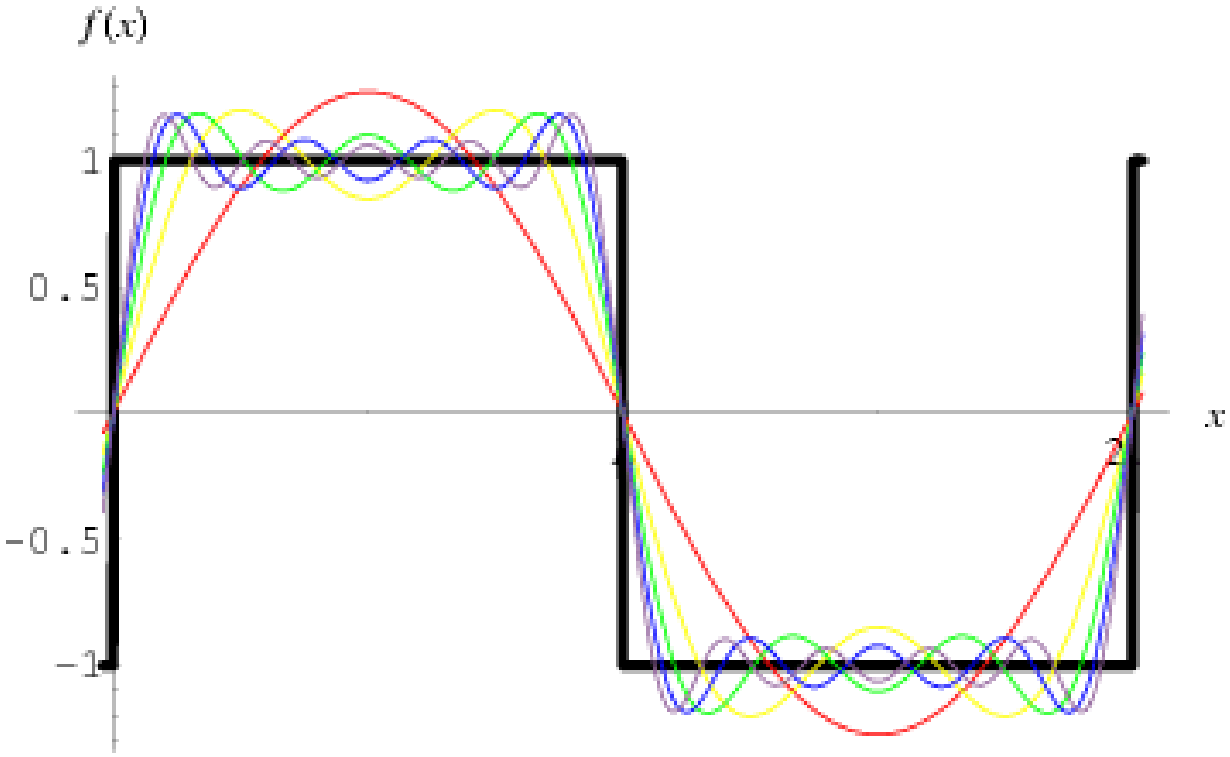

Figure 4: Ideal waveform of class F power amplifier

Therefore the output voltage waveform is sinusoidal

$$V_0 = -V_m \cos \omega_0 \, t \tag{7}$$

The fundamental component of the drain-to-source voltage is

$$V_{ds}1 = V_0 = -V_m \cos \omega_0 \, t \tag{8}$$

The voltage across the parallel-resonant circuit tuned to the third harmonic $3f_0$ is

$$V_{ds}3 = V_m 3 \cos 3 \, \omega_0 \, t \tag{9}$$

The third harmonic voltage waveform is 180^{o} out of phase with respect to the fundamental frequency voltage *vds*1. The voltages at all other harmonic frequencies are zero. The drain-to-source voltage waveform is given by

$$V_{DS} = V_I + V_{ds}1 + V_{ds}3 = V_I - V_m \cos \omega_0 t + V_m 3 \cos 3 \omega_0 t \quad (10)$$

The efficiency of the inverse class F amplifier is better than that of the class F amplifier with due to the higher V peak. The inverse class F has the less dc power dissipation with the same RF power output.

CHAPTER THREE: DESIGN OF CLASS F POWER AMPLIFIER

There are four types of design of the class F power amplifier where explained in this chapter. Which are 1) single stage class F power amplifier, 2) Cascode class F power amplifier, 3) single stage inverse class F power amplifier, 4) Cascode inverse class F power amplifier.

Non-Cascode class F power amplifier

Figure 5 shows the schematic diagram of a single stage conventional class F power amplifier at frequency of 5.8 GHz. TSMC 0.18µm technologies were used in this design. The CMOSFET is biased at V_{DD} is 2V and the V_{GG} is 0.7V

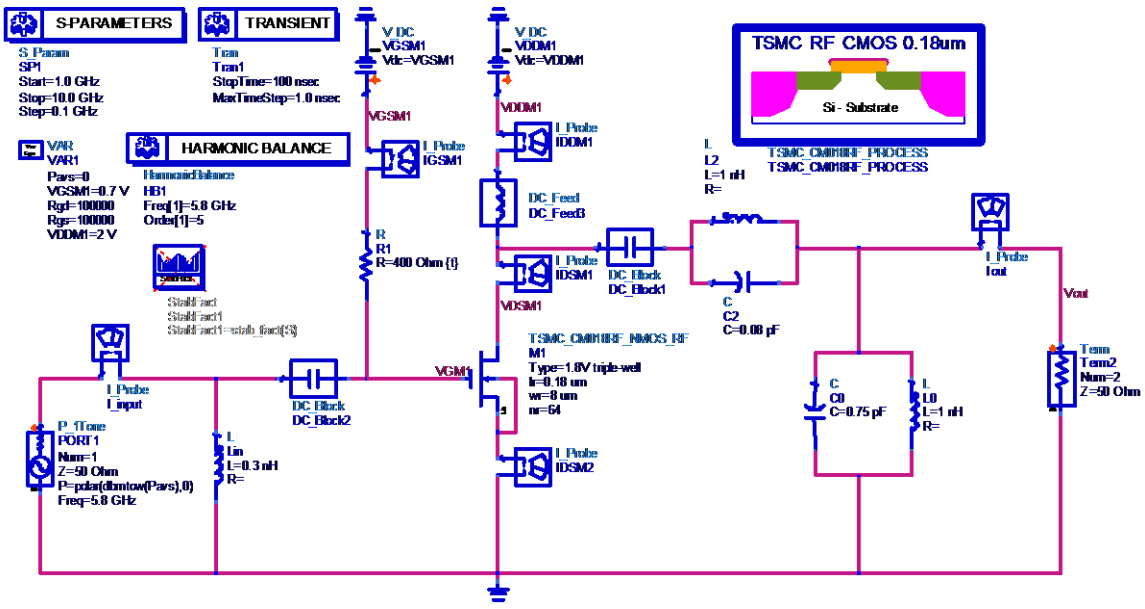

Figure 5: Single stage class F power amplifier circuit

The input of the amplifier contains the input matching, DC block capacitor, RF chock and Gate bias supply. The output of the amplifier contains the Drain bias, RF chock, DC block, 3rd harmonics tuning circuit, fundamental harmonics frequency tuning circuit and output matching circuit. The software used for simulation is Advanced Design System (ADS 2009). The output harmonics tuning circuit designed for $3f_0$ and f_0.

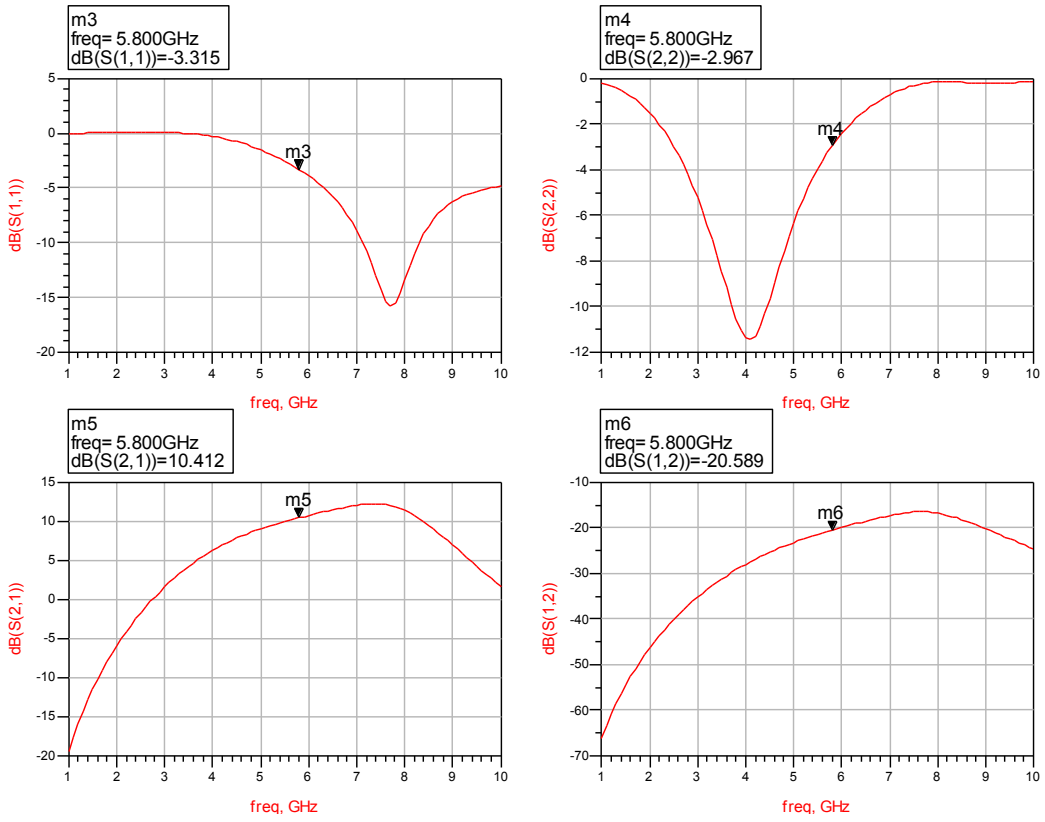

Figure 6: S-parameters for single stage class F PA

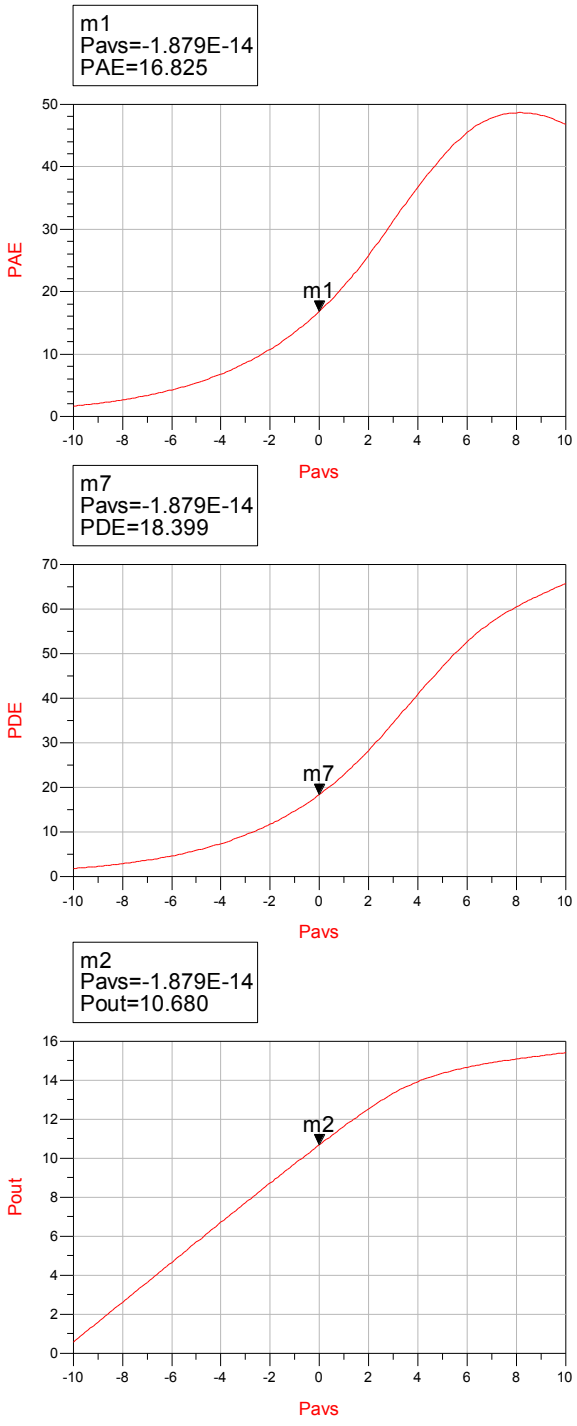

Figure 7: *PAE, DE, P_{out}* of single stage class F PA

The definition of the efficiency can be expressed as follows

$$\eta = \frac{Signal\ power\ delivered\ to\ load}{DC\ power\ supplied\ to\ output\ circuit} \tag{11}$$

or Power Added Efficiency,

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{12}$$

The output tuned resonator will shape the drain voltage and drain current waveforms to reduce the power dissipation by the transistor and thus to increase the efficiency of the power amplifier. In this design, there is one parallel resonant LC circuit at $3f_0$ for odd harmonics blocking and another parallel resonant LC circuit at f_0 which is open for the fundamental and short for other harmonic frequencies. The two resonant circuits are connected in series. The ac power is delivered to the load resistor RL. A 16.8% *PAE* and P_{out} is 10 dB were achieved from the simulation result, which is very low *PAE* and P_{out}. Figure 7 shows the simulation result of the *PAE*, *DE* and P_{out}

Figure 8 shows the transient response of the single stage class F power amplifier.

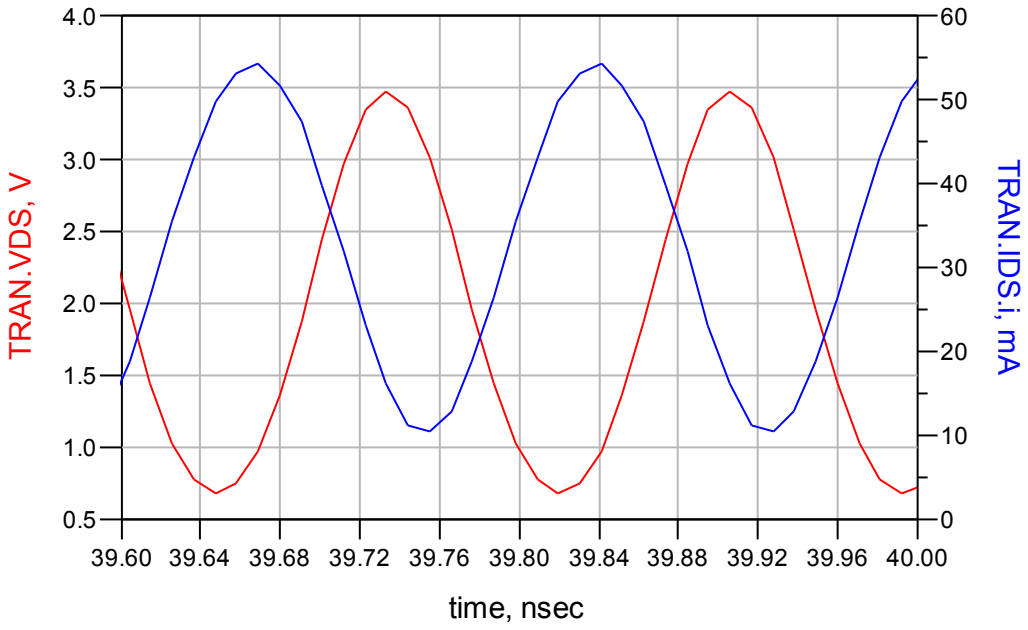

Figure 8: Transient waveform of single stage class F PA

The harmonic tuning tank circuits were designed for f_0 and $3f_0$. The fundamental frequency f_0 is 5.8GHz and the 3rd harmonic of the fundamental is 17.4 GHz. In a class F power amplifier there will not be additional matching circuits, since the harmonic tuning circuit is an important circuit that cannot change. The output harmonic tuning circuit also serves as the output matching. The inductor Lin acts as the input matching circuit. The S-parameters of the single stage class F power amplifier is shown in figure 6.

From the above waveforms, the V_{DS} in red color and the I_{DS} in blue color. The Drain-Source voltage swing is 2.8 V.

High voltage differential across the Drain-Source of the transistor cause gate oxide breakdown in the single stage class F power amplifier. This effect can be affect to the transistor long term performance. One of the methods is to improve the circuit reliability is by reducing the Drain-Source voltage. Cascode topologies were implemented to reduce the Drain-Source voltage across the transistor.

Cascode class F power amplifier

The design of a Cascode class F power amplifier is shown figure 9 below.

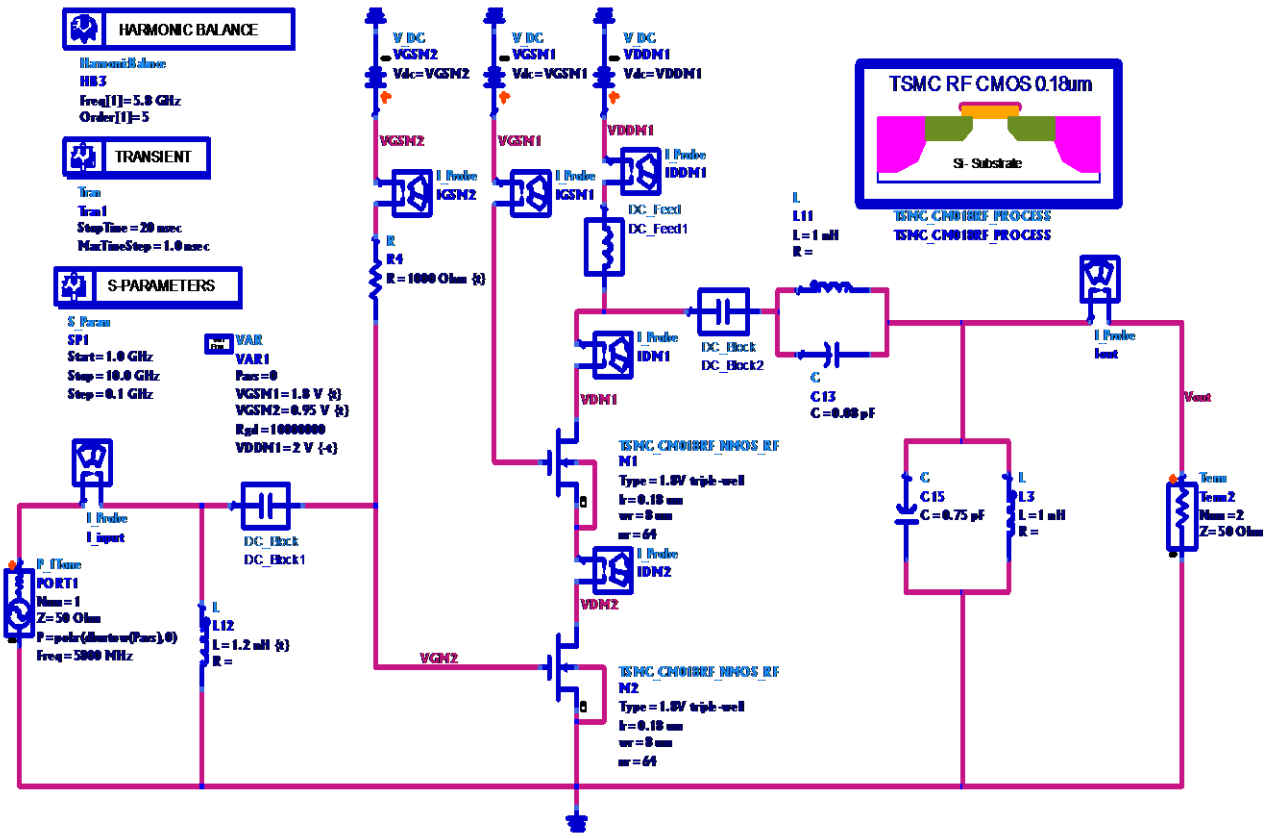

Figure 9: Cascode class F power amplifier circuit

The Cascode topology means the source of the main transistor connected to the drain of a second transistor which gate is the input of the power amplifier. The gate of the main transistor was constant gate supply to reduce the stress of the transistor. The Cascode structure gives the top transistor to have its gate oxide stress reduced by providing its constant gate biasing. The

input matching is achieved by using an inductor Lin which is tuned to have good S11. The main transistor biased with 1.8V constant at the gate of the main transistor. The gate of the second transistor was biased with 0.95V. The Drain supply of the main transistor is 2V. There are two harmonic tuning circuits in the output, which are 3rd harmonic blocking and fundamental open circuits. These two tuned circuits act also as the output matching to achieve a good S22.

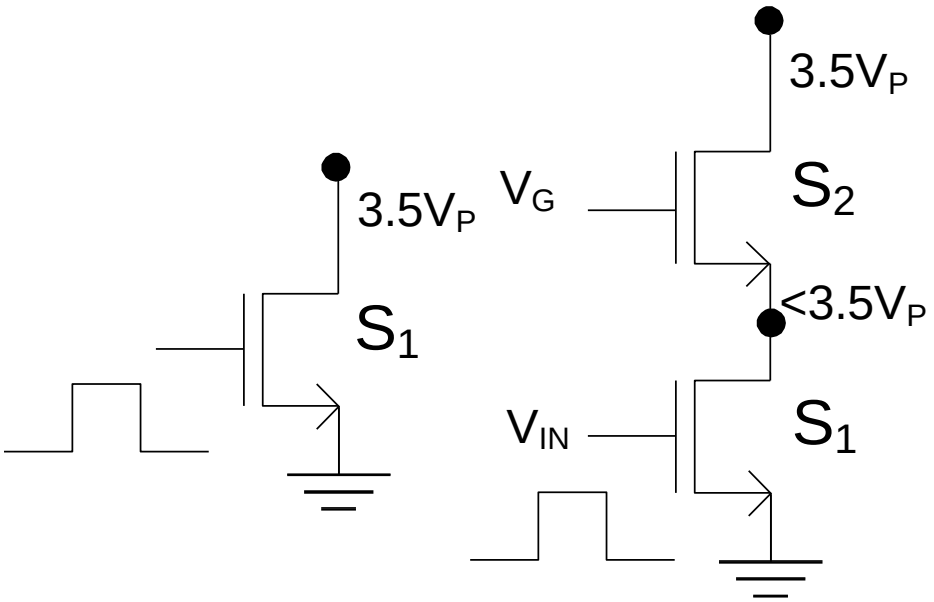

Figure 10: Comparison single stage versus Cascode topology

Figure 10 shows the comparison of the single stage and Cascode topology to reduce the stress. As seen in the figure, with V_G as a constant, 3.5 V_P – V_G < V_{IN}. This method helps to reduce the drain-source voltage in both transistors. Basically, with a single transistor, the voltage across drain-source will more compared to the Cascode topology

The simulation result of the Cascode class F power amplifier is explained below. Figure 11 shows the s-parameters result. The input and output matching were satisfied.

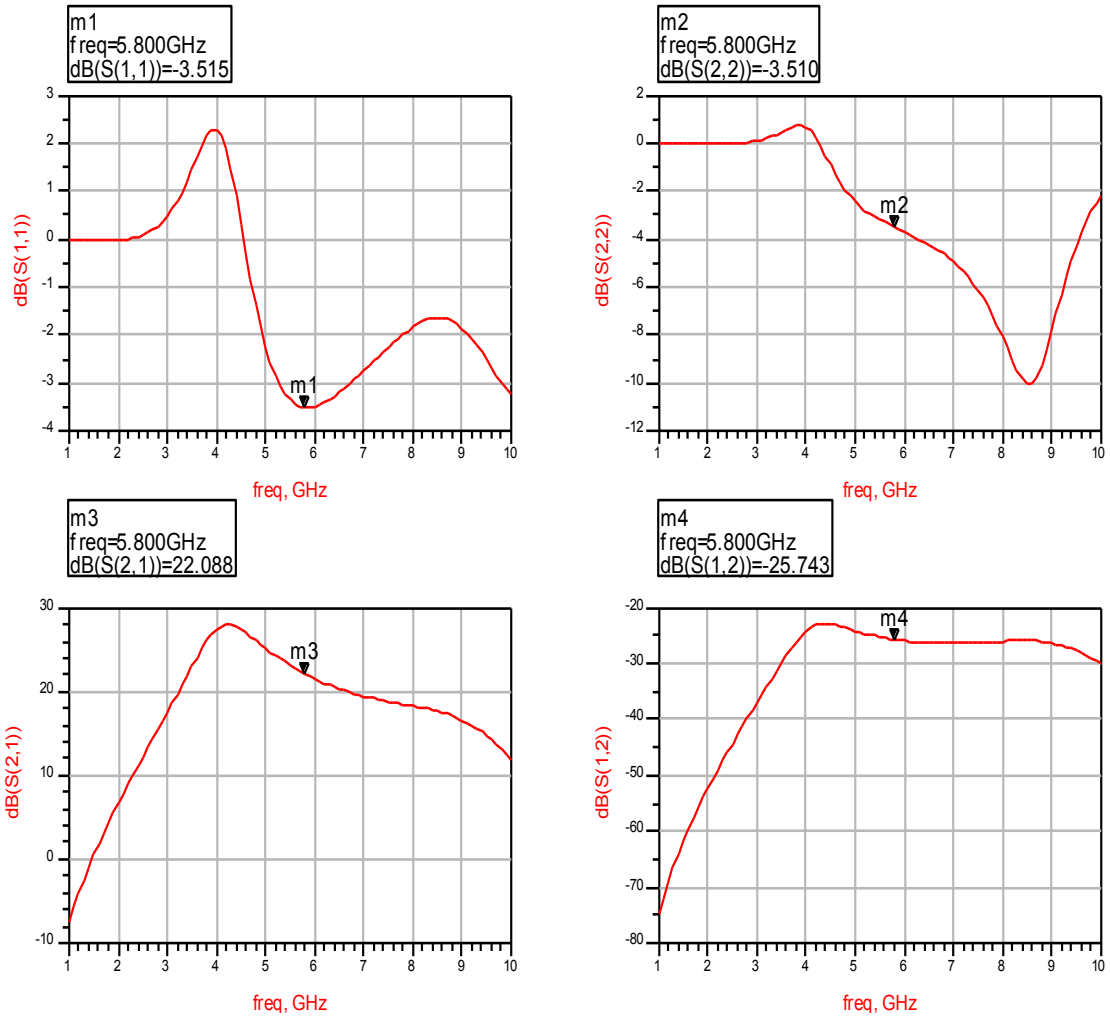

Figure 11: S-parameters of Cascode class F power amplifier

As seen in figure 11, the input and output matching were improved in the Cascode topology. The *PAE*, P_{out} and *DE* were also improved significantly. Figure 12 shows the result of *PAE*, P_{out} and *DE*.

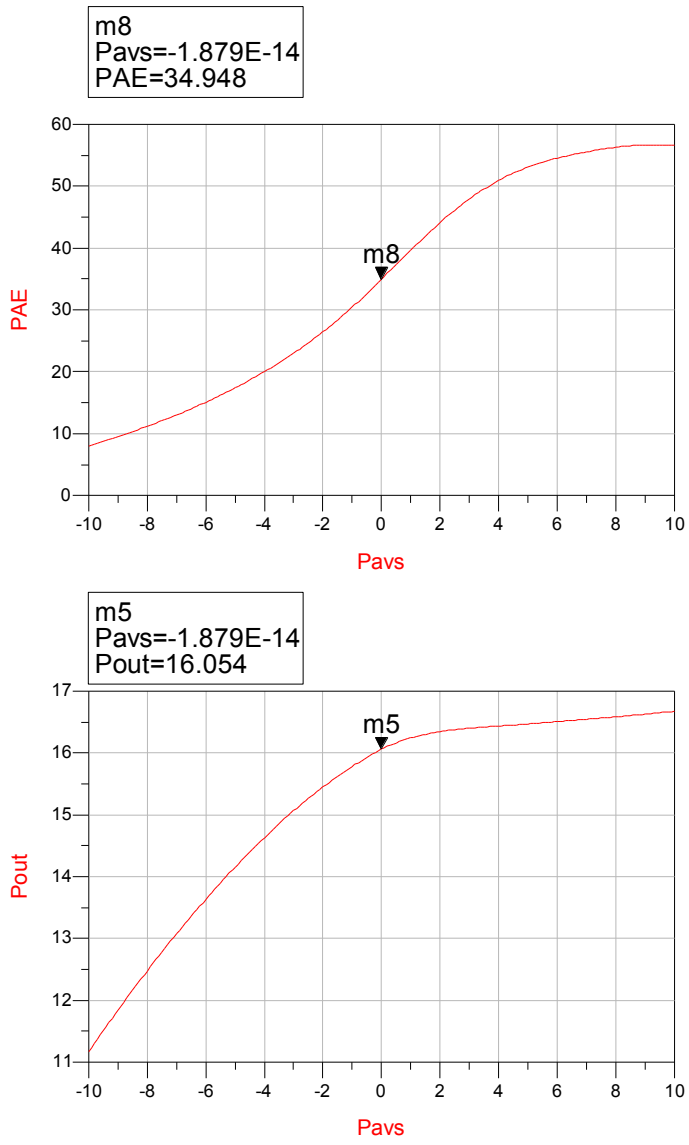

Figure 12: *PAE* & P_{out} of Cascode class F PA

A 35% of *PAE* and 16dB P_{out} were obtained at 0dBm input power. As seen in the previous section, the *PAE* & P_{out} were lower in the single stage class F PA than the Cascode class F power amplifier.

Figure 13 shows the V_{DS} and I_{DS} waveforms of the top transistor of the Cascode class F power amplifier.

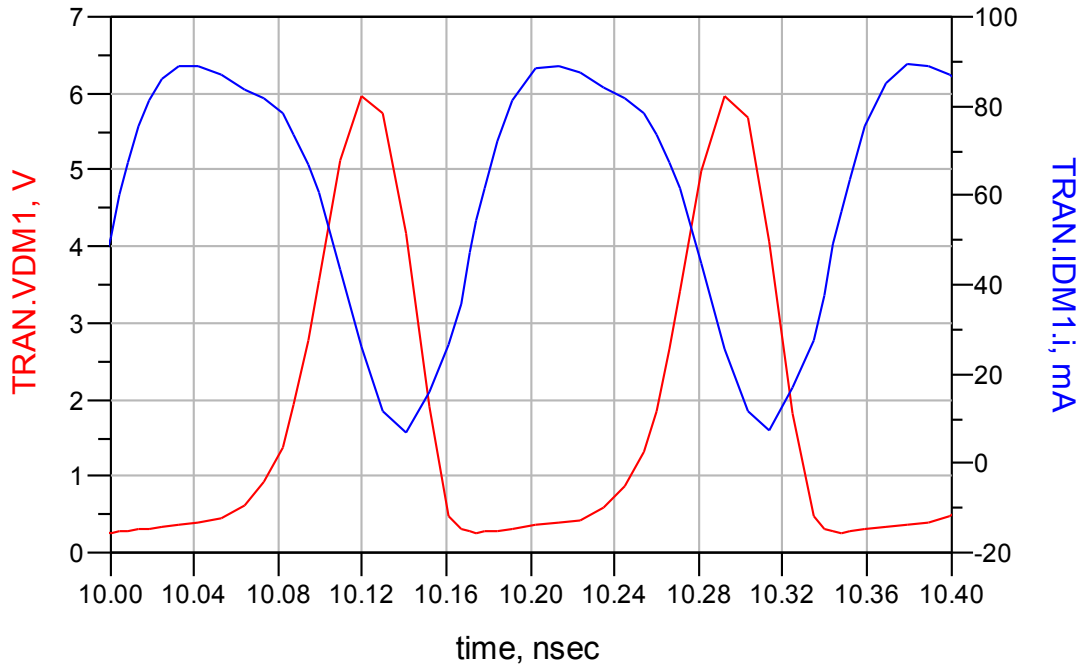

Figure 13: Transient wave form of a Cascode class F PA (top transistor)

V_{DS} (Red) & I_{DS} (Blue)

The V_{DS} and I_{DS} waveforms of the bottom transistor of the cascode class F power amplifier are shown in figure 14. The drain-source voltage of the top transistor is 5.5 V. and the drain-source voltage of the bottom transistor is 1.4 V. the difference between these two voltages is the stress across the transistors.

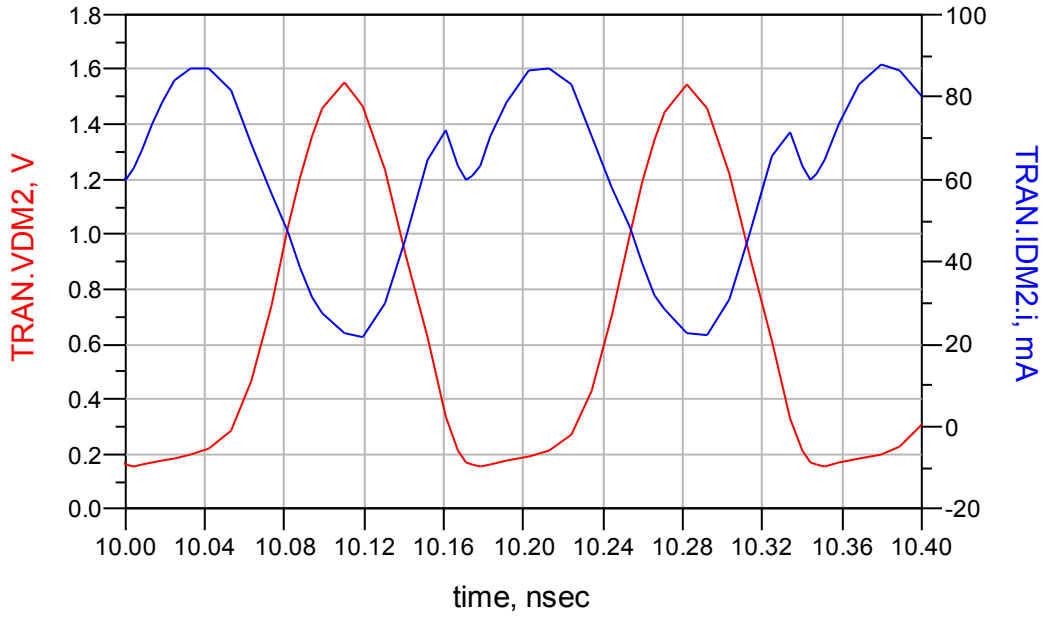

Figure 14: Transient wave form of a Cascode class F PA (bottom transistor)

V_{DS} (Red) & I_{DS} (Blue)

The stress of the Cascode class F power amplifier is shown in figure 15 below.

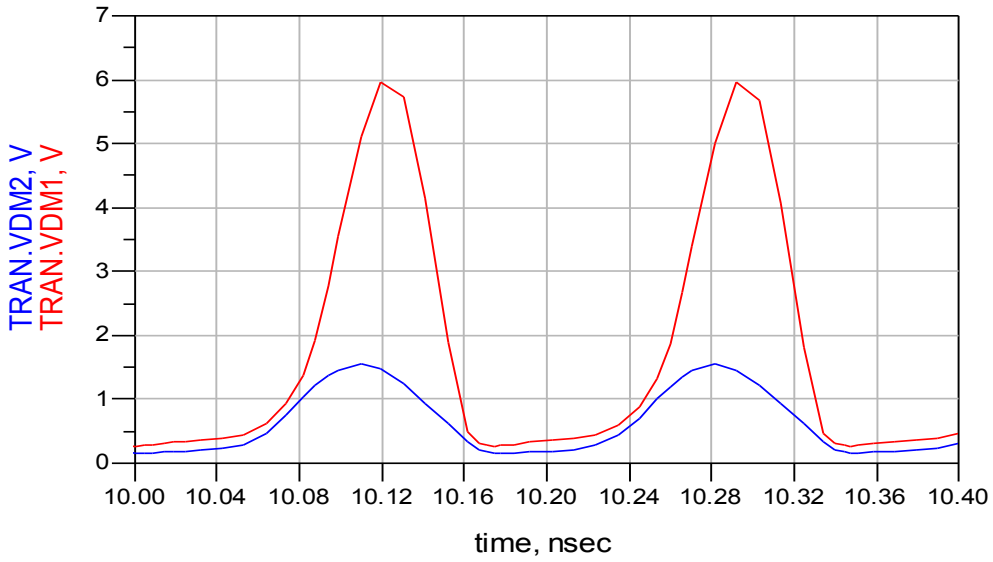

Figure 15: Transient waveforms V_{DS} (top transistor) Red, V_{DS} (Bottom Transistor) Blue.

Non-Cascode Inverse class F power amplifier

The designed circuit for a non-Cascode class F power amplifier is shown in figure 16 below. The circuit is same as the non-Cascode class F power amplifier as seen in figure 5 except the harmonic tuning circuit. This is tuned for 2nd harmonic and fundamental frequency.

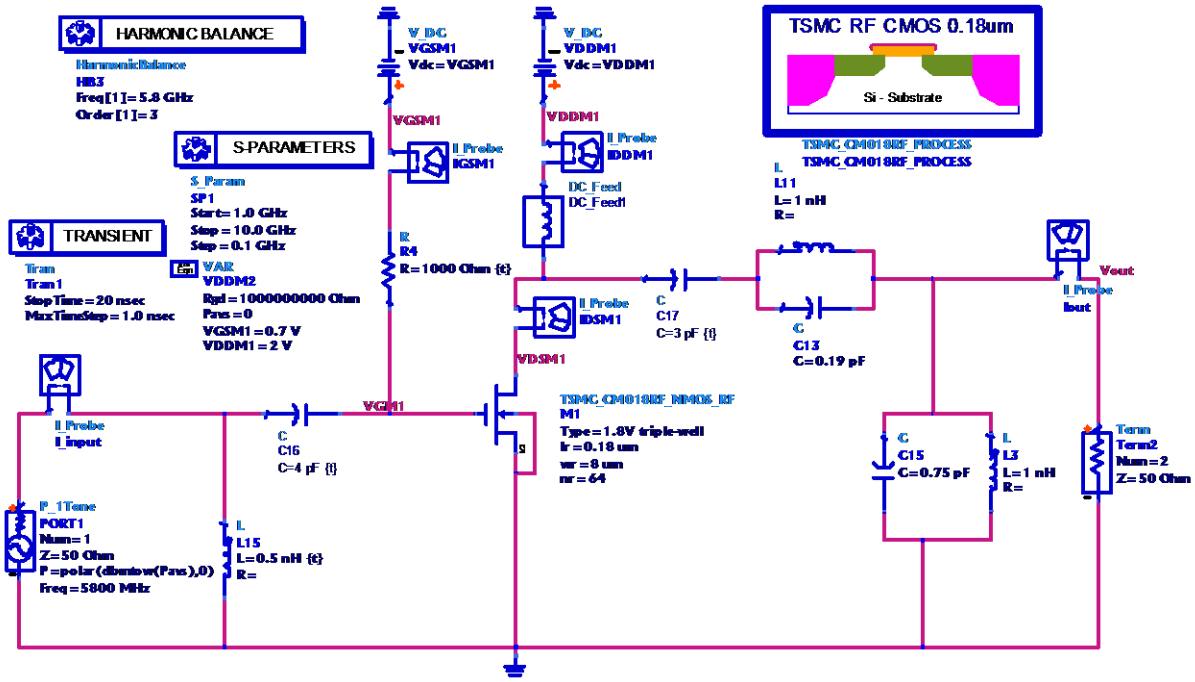

Figure 16: Non-Cascode Inverse class F power amplifier circuit

As seen in the circuit the capacitor value of the 2nd harmonic blocking circuit were changed from the previous based on the 2nd harmonic frequency 11.6GHz. For the inverse class-F power amplifier, the harmonic conditions for both the current and voltage waveform can be obtained from the following conditions. The first one is, the infinite impedance for even order harmonic

frequencies is provided to remove the even harmonics in the current waveform. The second one is the, zero impedance for the odd harmonics frequencies are provided to remove the odd harmonics in the voltage waveform.

The input of the circuit contains one inductor Lin and a capacitor Cin which are used for input matching S11. The S-parameters result is shows in figure 17 below

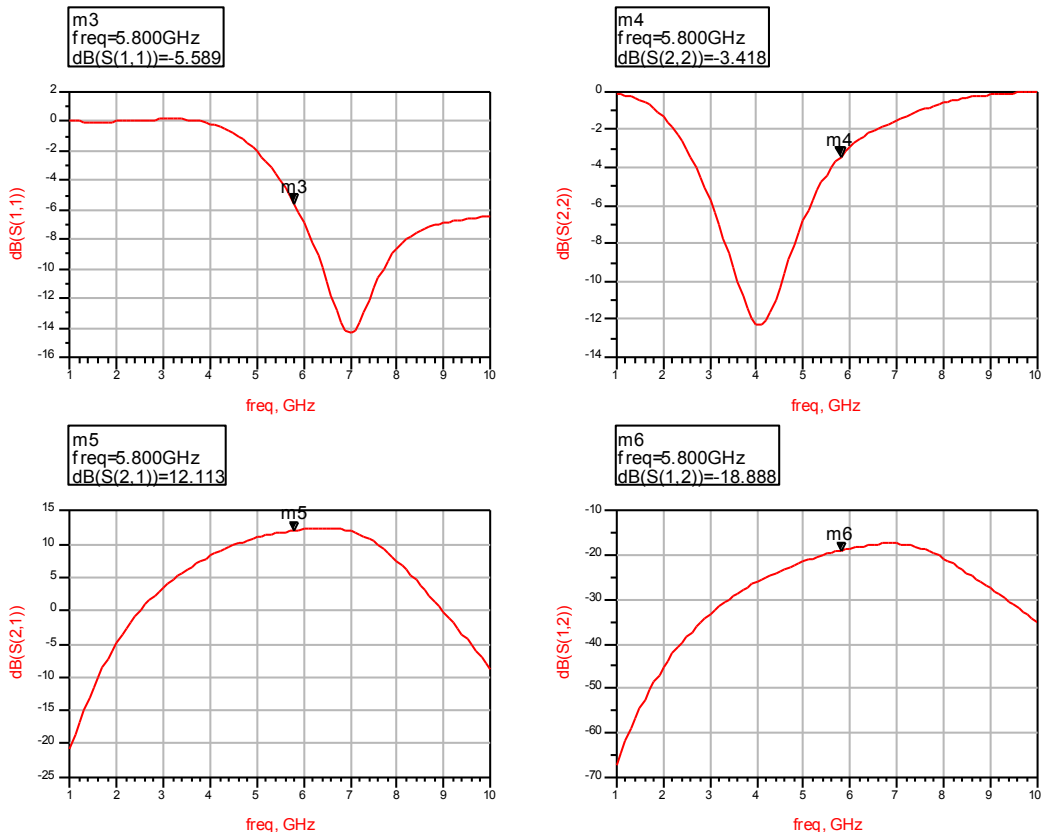

Figure 17: S-parameters of non-Cascode inverse class F power amplifier.

The designed circuit were simulated and a 24% *PAE* and 12dB P_{out} were achieved which is very good achievement than the non-Cascode class F power amplifier. Figure 18 shows the *PAE* and P_{out} results.

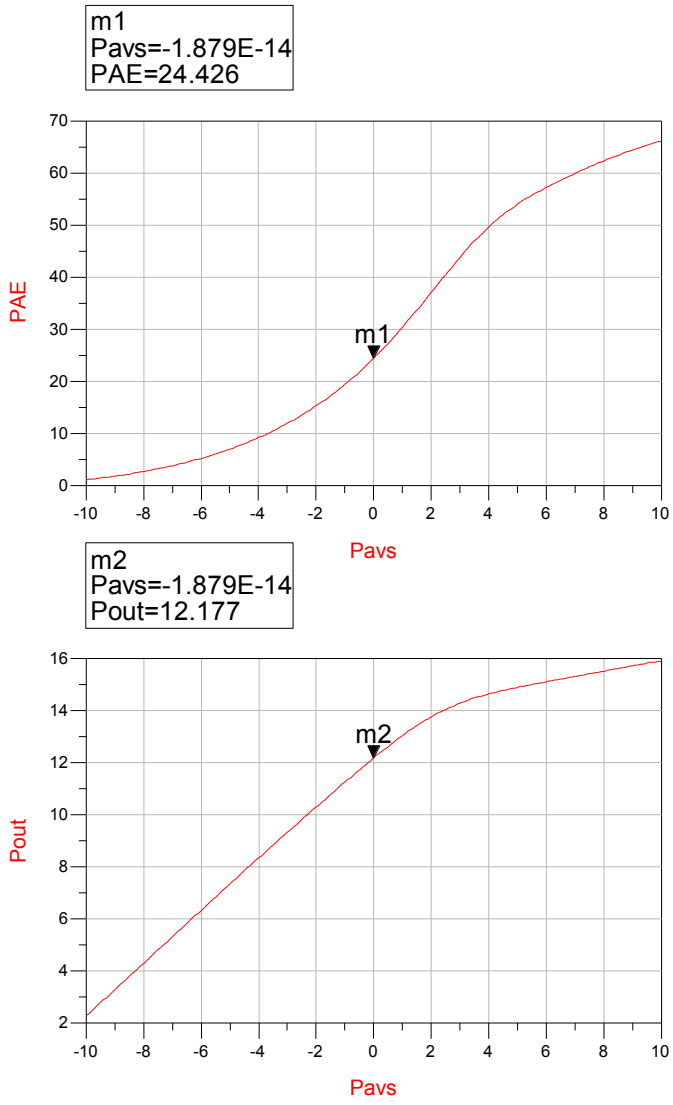

Figure 18: *PAE* & P_{out} of the non-Cascode inverse class F power amplifier

The transient waveform of the non-Cascode inverse class F power amplifier is shown in figure 19 below.

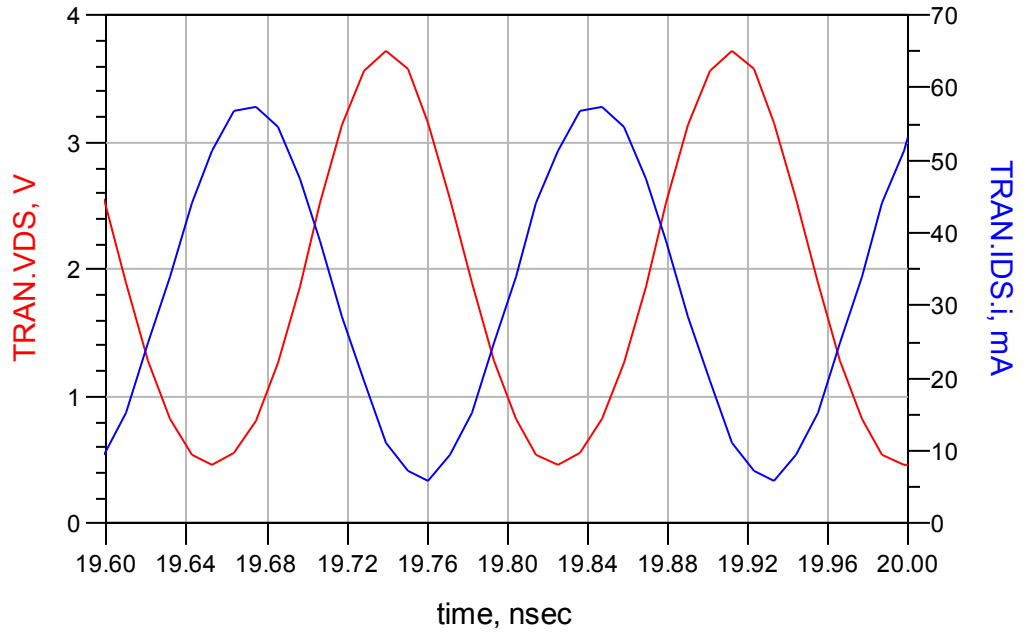

Figure 19: Transient waveform of non-Cascode inverse class F PA V_{DS} (Red), I_{DS} (blue)

The drain-source voltage swing is 3.3V were calculated. This is quite good stress compared to the non-cascode regular class F power amplifier. To reduce the stress a Cascode topology were implemented in the inverse class F power amplifier, which is explained in the below section.

Cascode Inverse class F power amplifier

The designed circuit diagram for a Cascode inverse class F power amplifier is shown in figure 20 below.

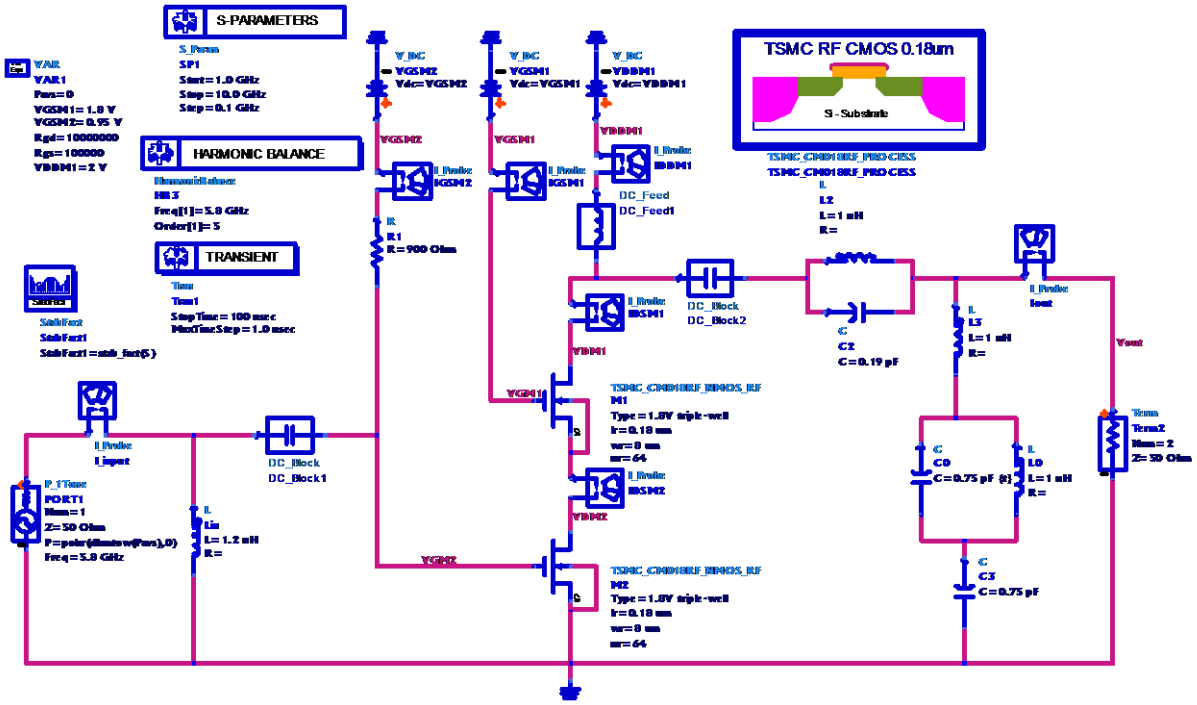

Figure 20: Cascode inverse class F power amplifier circuit.

In the Cascode inverse class F power amplifier circuit, the harmonic tuning circuits were same as the non-Cascode inverse class F power amplifier. The only change is the additional transistor which is connected in Cascode with the main transistor to reduce the electrical stress in between drain-source. The s-parameters result is shown in the figure 21 below.

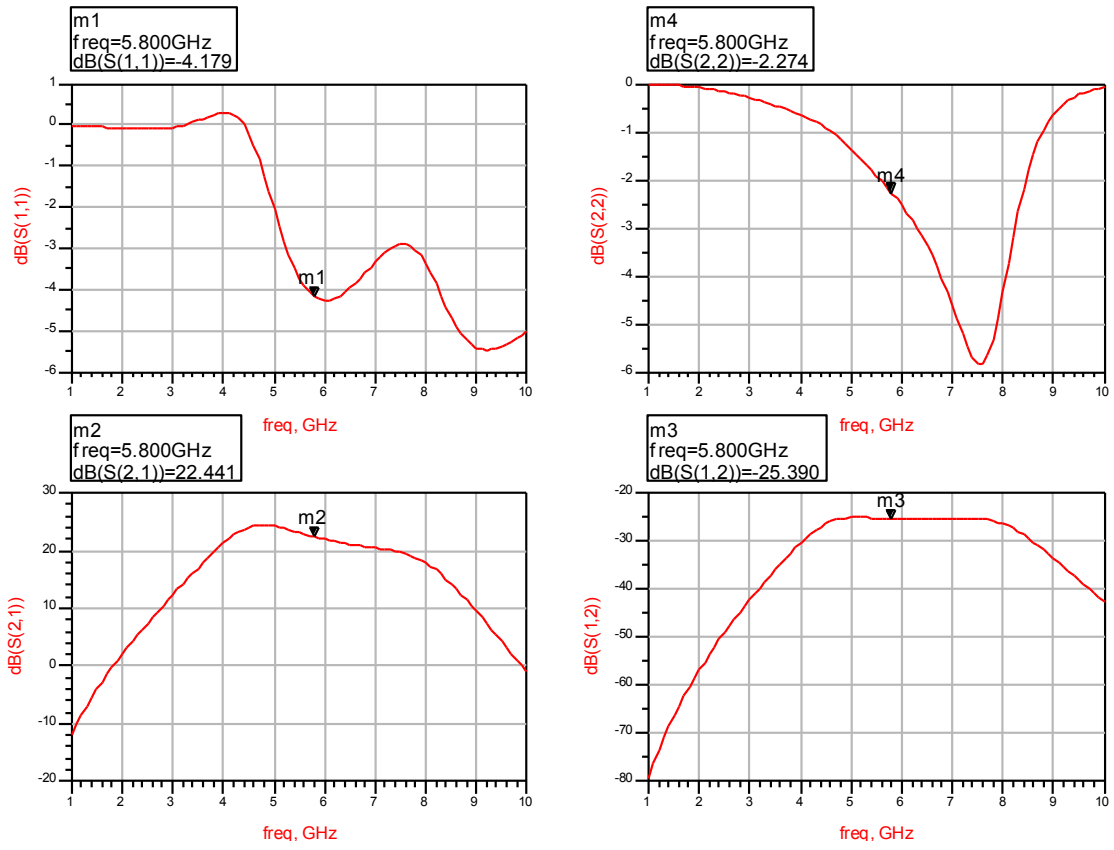

Figure 21: S-parameters of the Cascode inverse class F power amplifier.

As seen in the figure above the S11 and S22 are the input and output matching which is quite good compared to the regular Cascode class F power amplifier. The gain and the insertion loss were satisfied according to the design goal.

Figure 22 shows the simulated result of PAE and Pout of the Cascode inverse class F power amplifier.

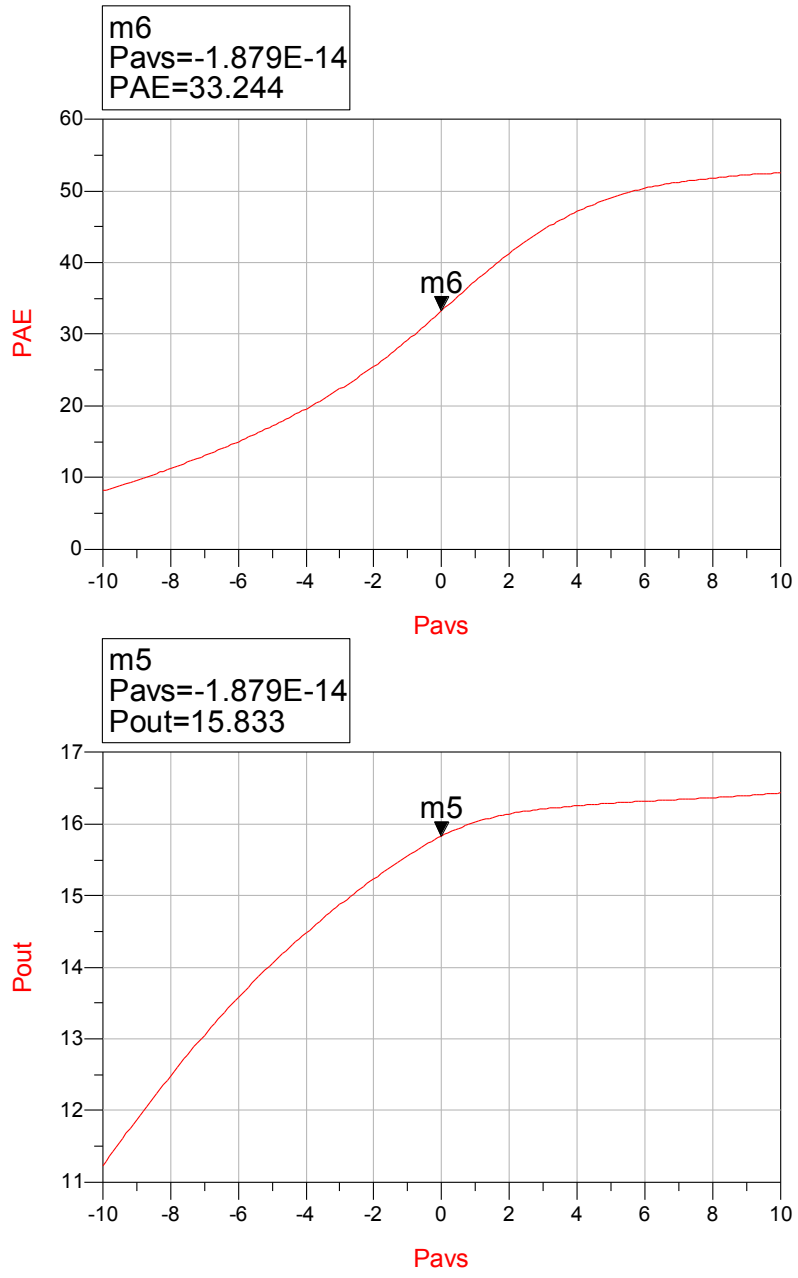

Figure 22: *PAE* & P_{out} of the Cascode class F power amplifier

A 33% *PAE* and 15dB P_{out} were achieved from the Cascode inverse class F power amplifier. This is the highest *PAE* and P_{out} were achieved from all the four circuits. So the Cascode inverse class F power amplifier is the good configuration for a good *PAE* and P_{out} amplifier. Let's take a look the stress effect in the Cascode inverse class F power amplifier. Figure 23 shows the transient waveform of the top transistor.

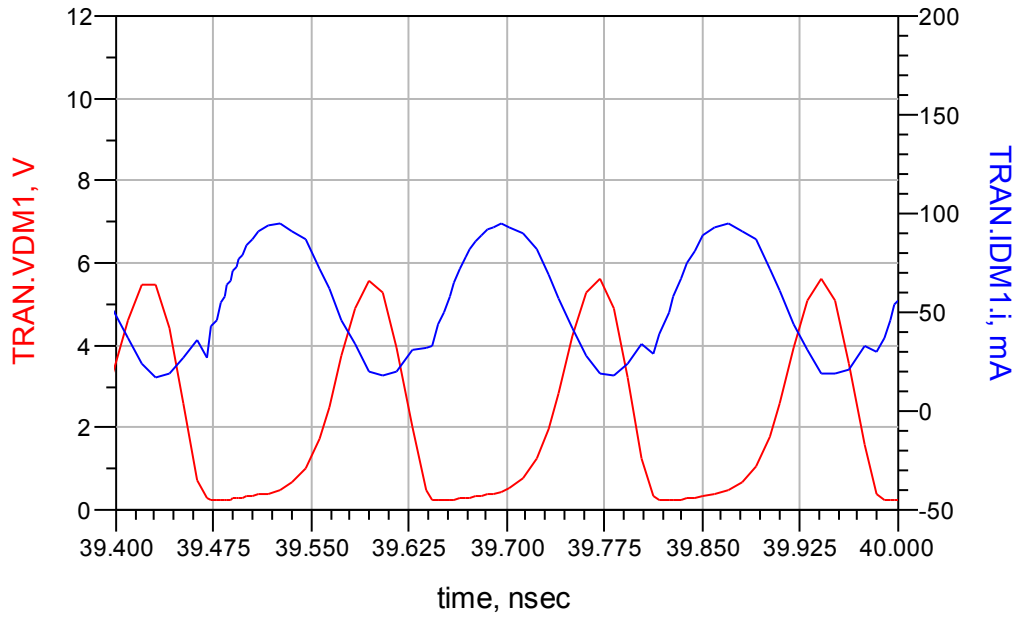

Figure 23: Transient waveform of Cascode inverse class F PA (top Transistor) V_{DS} (red, I_{DS} (blue)

As seen in the figure the drain – source voltage on the top transistor is 5.5 V. Figure 24 shows the transient wave form of the bottom transistor.

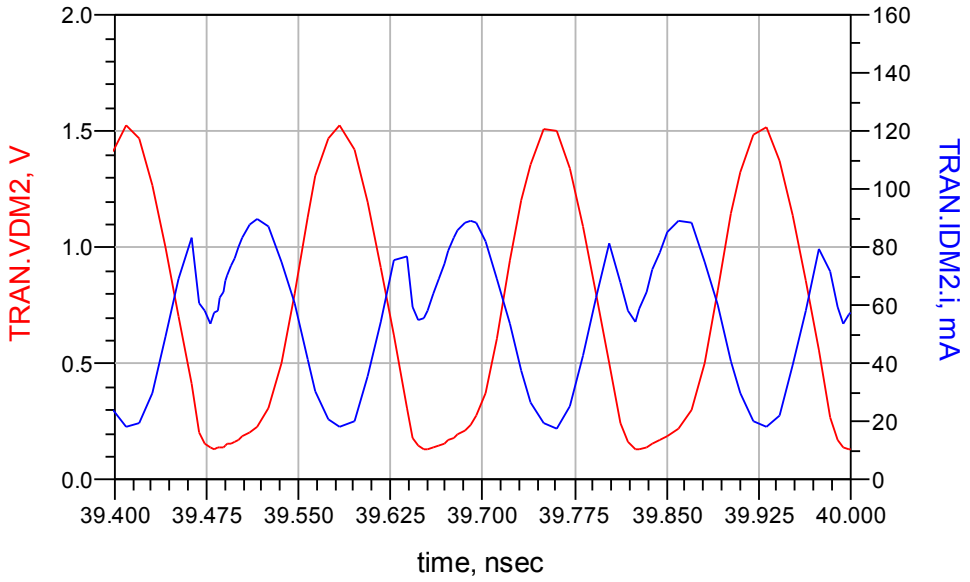

Figure 24: Transient waveform of the Cascode inverse class F PA (bottom transistor)V_{DS} (red), I_{DS} (blue)

The drain-source voltage of the bottom transistor is 1.5V. The voltage difference between the V_{DS} of the top and bottom transistor is 4.6 V, which is less stress than the other power amplifier configuration. Figure 25 shows the transient waveform which represents the stress of the Cascode inverse class F power amplifier shown below.

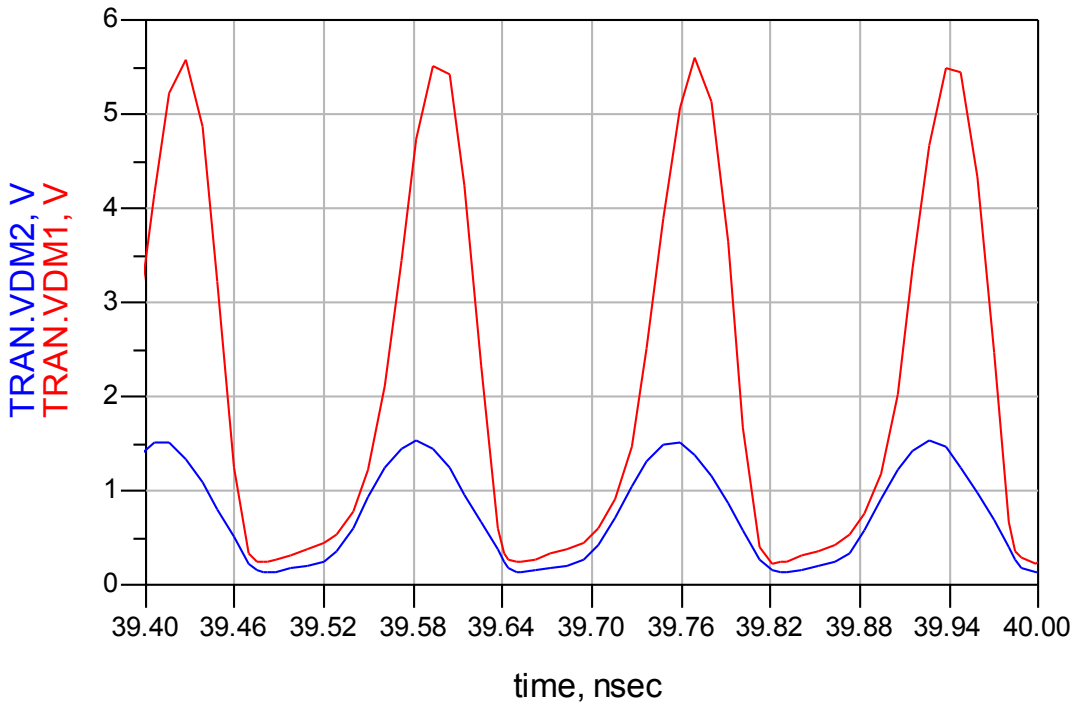

Figure 25: Transient waveform of V_{DS} (red) top transistor, V_{DS} (blue) bottom transistor

Table 2 shows the comparison of all the results.

Parameters	Class F		Inverse class F	
	Non-Cascode	Cascode	Non-Cascode	Cascode
V_{DD} (Top MOSFET)	2 V	2 V	2 V	2 V
V_{GG} (Top MOSFET)	0.7 V	1.8 V	0.7 V	1.8 V
V_{GG} (Bottom MOSFET)	---	0.95 V	---	0.95 V
PAE (%)	16.8 %	35.0 %	24.4 %	33.2 %
DE (%)	18.4 %	37.2 %	26.0 %	35.0 %
P_{out} (dB)	10.6 dB	16.0 dB	12.1 dB	15.8 dB
V_{DS} (V)	2.8 V	5.3 V	3.3 V	4.6 V

Table 2: Comparison of class F and Inverse class F PA both non-Cascode and Cascode structure

CHAPTER FOUR: GATE OXIDE BREAKDOWN

Even though the Cascode topology for the class F power amplifier is a solution for reducing the gate drain electrical stress on the switching transistor, it is not a solution that completely solves the gate oxide breakdown problem. Designers can increase the sully voltage V_{DD} to achieve a higher P_{out}. An increase in V_{DD} will result in a direct increase in the peak voltage V_P. If the gate voltage also increased along with V_P, then the oxide stress is shifted from the drain-gate region to drain-source region

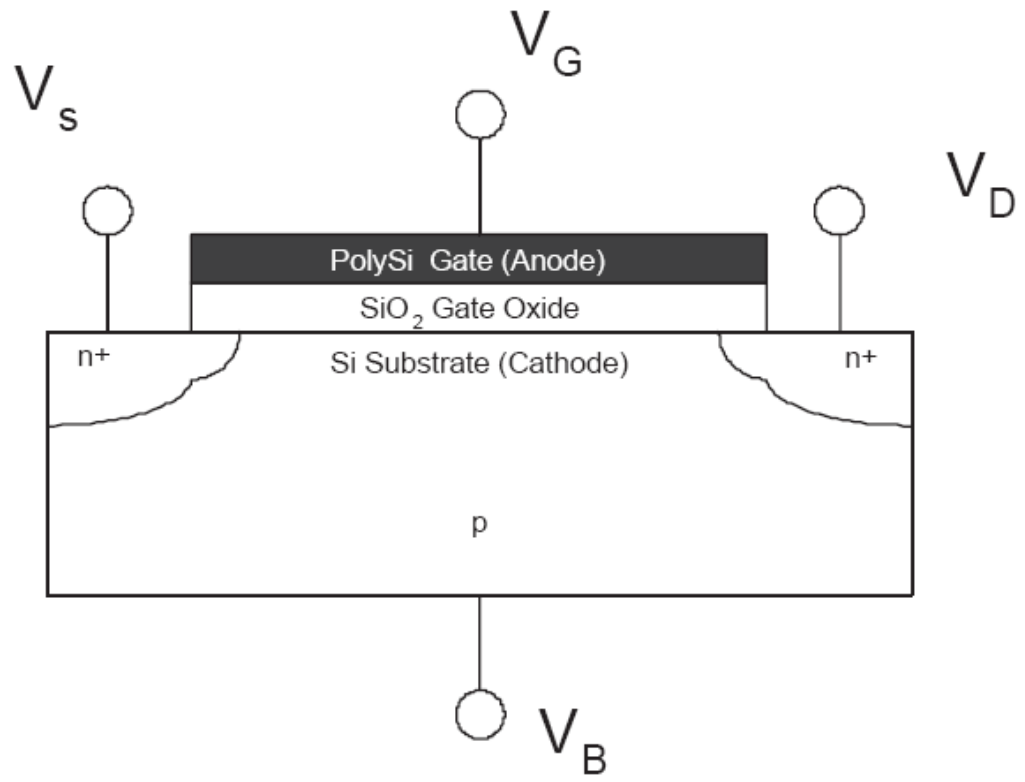

Figure 26: Cross section of an NMOSFET

R_{GD} effect

When the transistor under stress, high electrical fields were build near the gate oxide region. Due to high electrical field, the electrons were trapped inside the gate oxide region. For long term stress, the gate oxide becomes a short circuit path for anode and cathode. Because of this reason the transistor can burn.

To analyze the gate breakdown of the transistor in the circuit, a resistance were connected between gate and drain terminal of the main transistor. Figure 27 shows the gate-drain resistance effect of the non-Cascode class F power amplifier circuit.

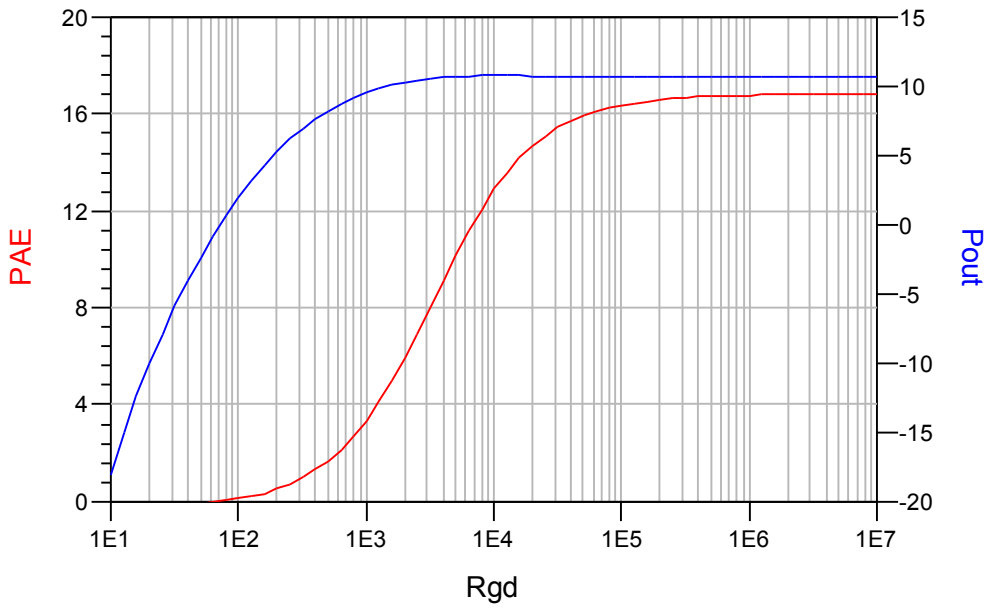

Figure 27: *PAE & P_{out}* in drain-gate resistance domain -single stage (log scale).

R_{GD} effect of the Cascode class F power amplifier is shown in figure 28 below

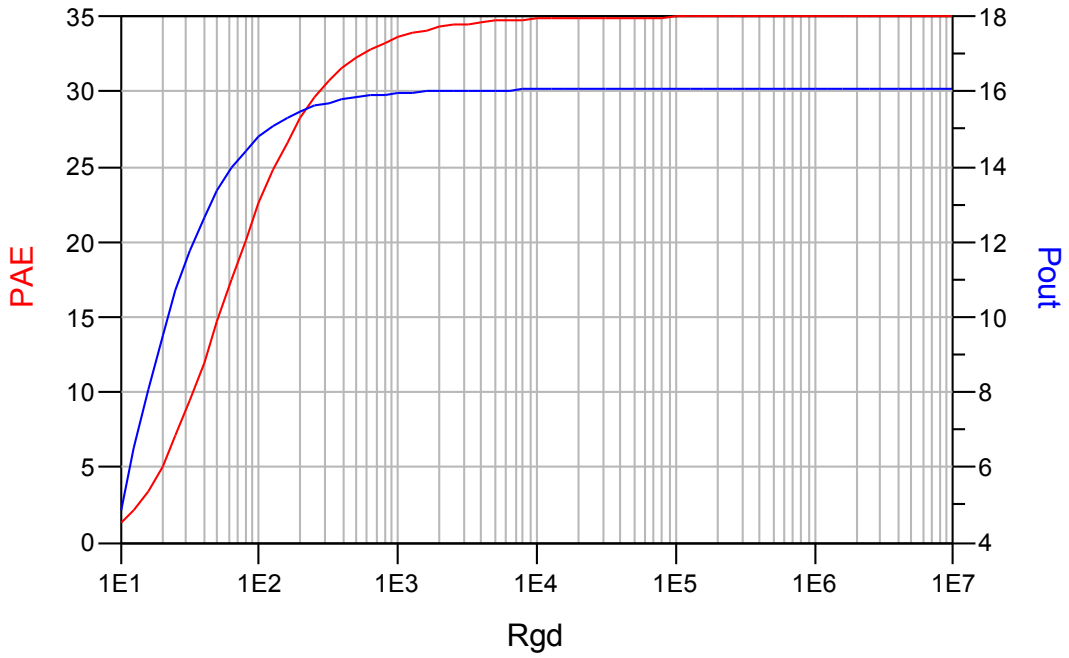

Figure 28: *PAE & P_{out}* in drain-gate resistance domain-Cascode structure (log scale).

As seen in the above figures the oxide breakdown occur in the single stage class F amplifier is much easier than the Cascode class F power amplifier circuit. Because, in the single stage class F power amplifier, the *PAE & P_{out}* achieve after the resistance reach 10K Ω. but in the Cascode structure, the *PAE & P_{out}* were achieved when the resistance reach 100 Ω.

Look the same R_{GD} effect for the Inverse class F power amplifier. This is similar to the class F PA. Figure 29 and 30 shows the *PAE* & P_{out} in gate-drain resistance domain.

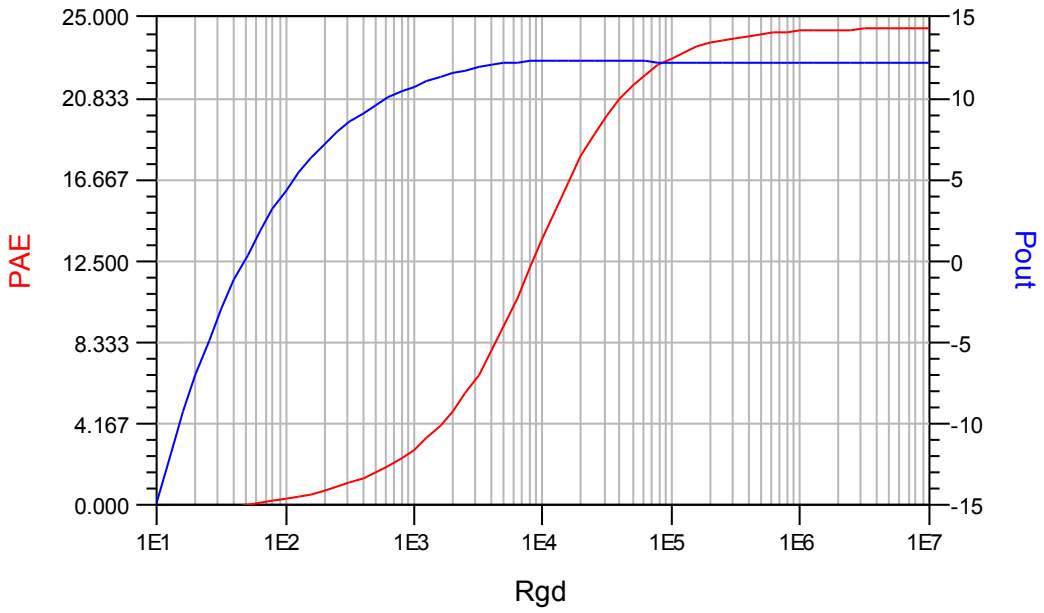

Figure 29: *PAE* & P_{out} in gate-drain resistance domain –single stage - (log scale)

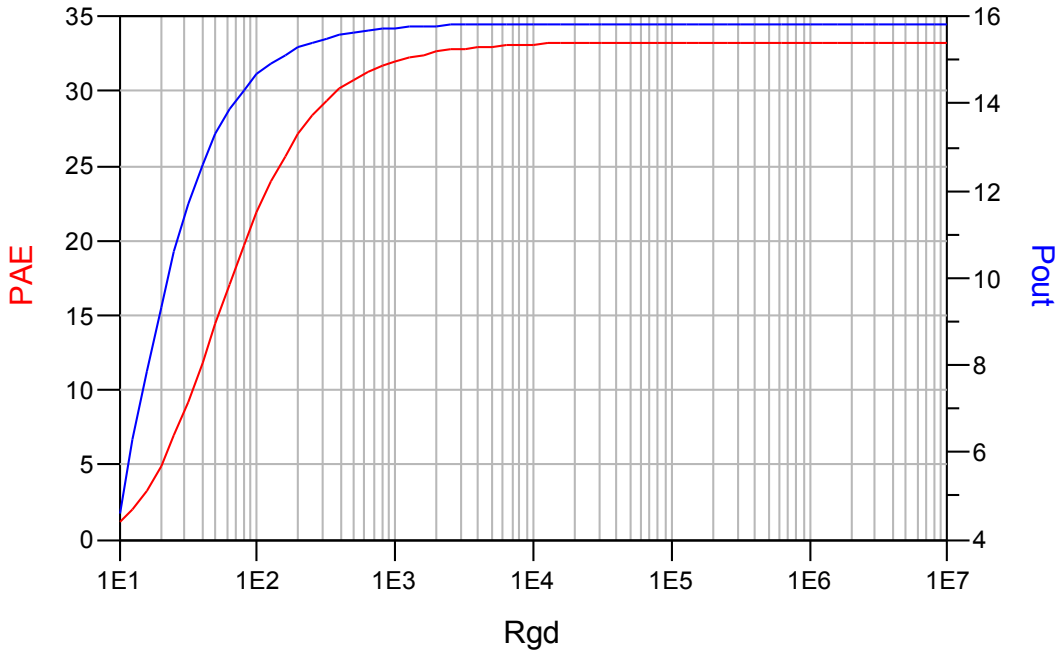

Figure 30: *PAE & P_{out}* in gate-drain resistance domain -Cascode structure (log scale)

V_{DD} variance effect

Figure 31 shows below the *PAE* & P_{out} with respect to V_{DD} sweep of the non-Cascode class F power amplifier.

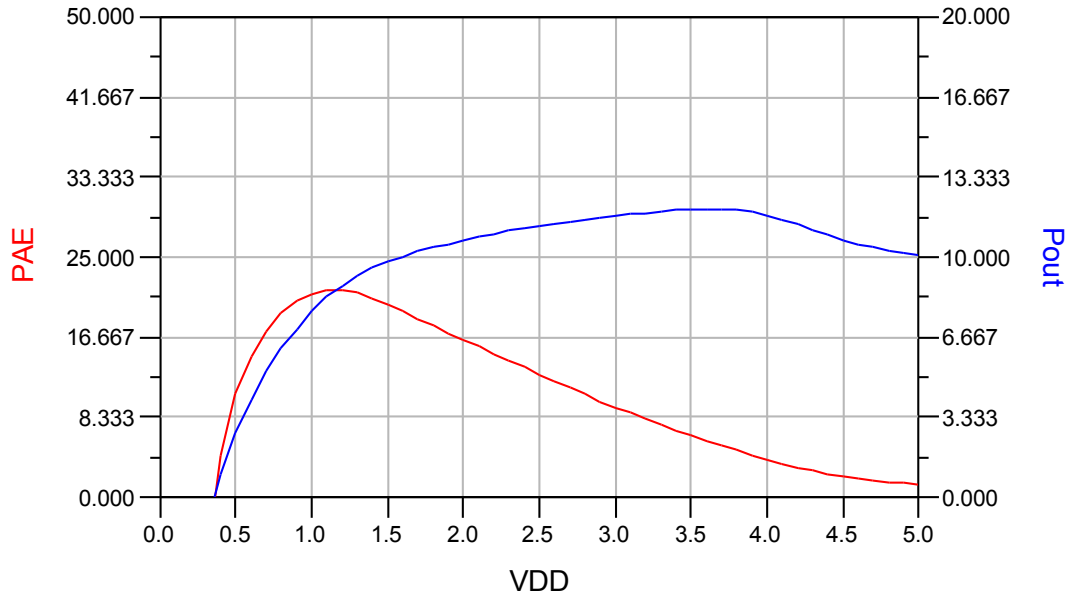

Figure 31: *PAE* & P_{out} versus V_{DD} (Non-Cascode structure-class F)

As seen in the above figure the PAE drop significantly when the V_{DD} goes high, because there is going to be high power dissipation that becomes low *PAE* but the P_{out} is keep increasing if the V_{DD} increase.

However, in the Cascode structure, when the V_{DD} goes high the *PAE* and P_{out} increase significantly. Figure 32 shows the *PAE* & P_{out} versus V_{DD} of the Cascode class F power amplifier.

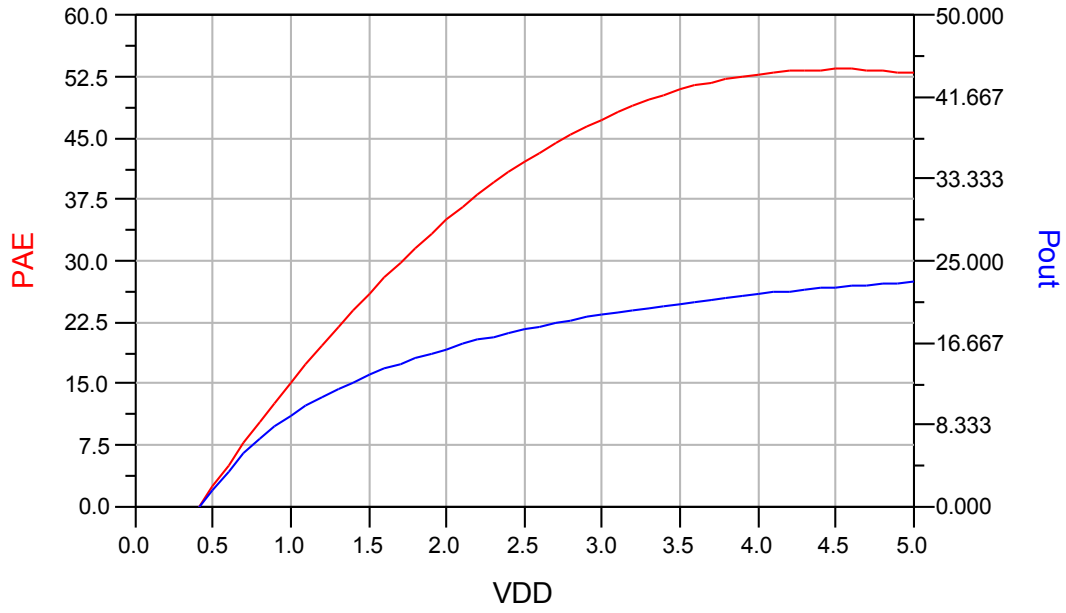

Figure 32: *PAE* & P_{out} versus V_{DD} (Cascode structure-class F)

This simulation is also done in the inverse both non-Cascode and Cascode PA. The results were shown in figure 33 and figure 34 as below.

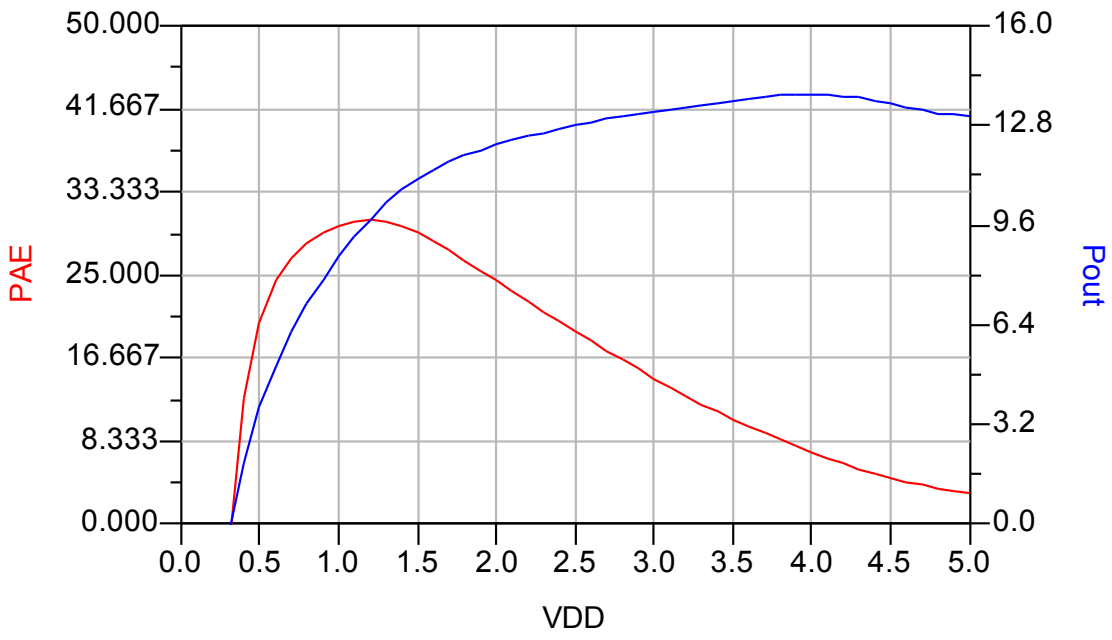

Figure 33: *PAE & P_{out}* versus V_{DD} (non-Cascode Inverse class F PA)

The response of both the non Cascode class F and non- Cascode inverse class F were similar. Because the single stage class F amplifier handle more stress than the Cascode class F power amplifier. Figure 34 shows the Cascode inverse class F power amplifier V_{DD} effect. As seen in the figure the Cascode topology were having the good V_{DD} effect which is quit necessary.

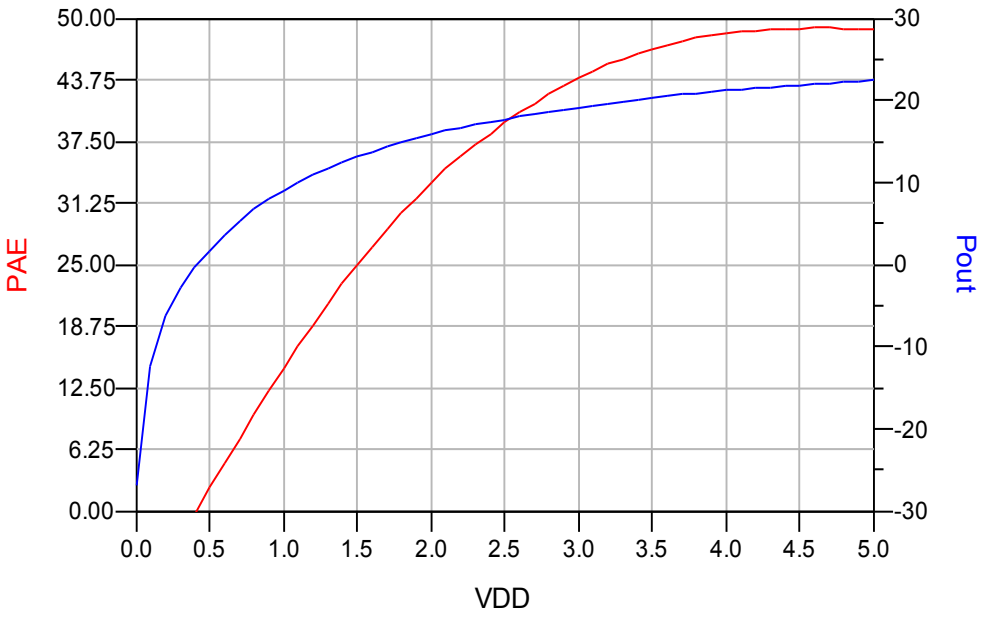

Figure 34: *PAE & P_{out}* versus V_{DD} (Cascode structure-inverse class F)

Temperature variance effect

To analyze the temperature variance effect in the class F power amplifier circuit, a temperature variable has to be setup in the circuit. In the harmonic balance simulation tool, set the temperature sweep from 0°C - 125°C. Perform the harmonic balance simulation and the *PAE* & P_{out} of the selected circuit were plotted in the temperature domain. Figure 35 shows the non Cascode class F power amplifier result.

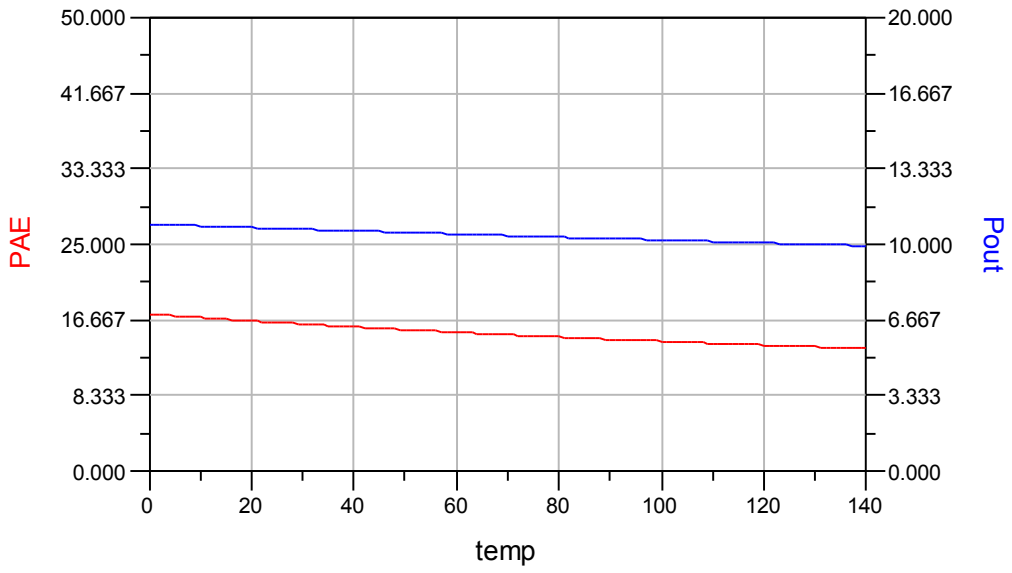

Figure 35: *PAE* & P_{out} versus Temperature (non-Cascode class F PA)

As seen in the above graph, the efficiency and the power output were slightly degraded with respect to the temperature increase. This is quite natural all other circuit performance was simulated and the results were plotted. The figure given below shows the other circuits result.

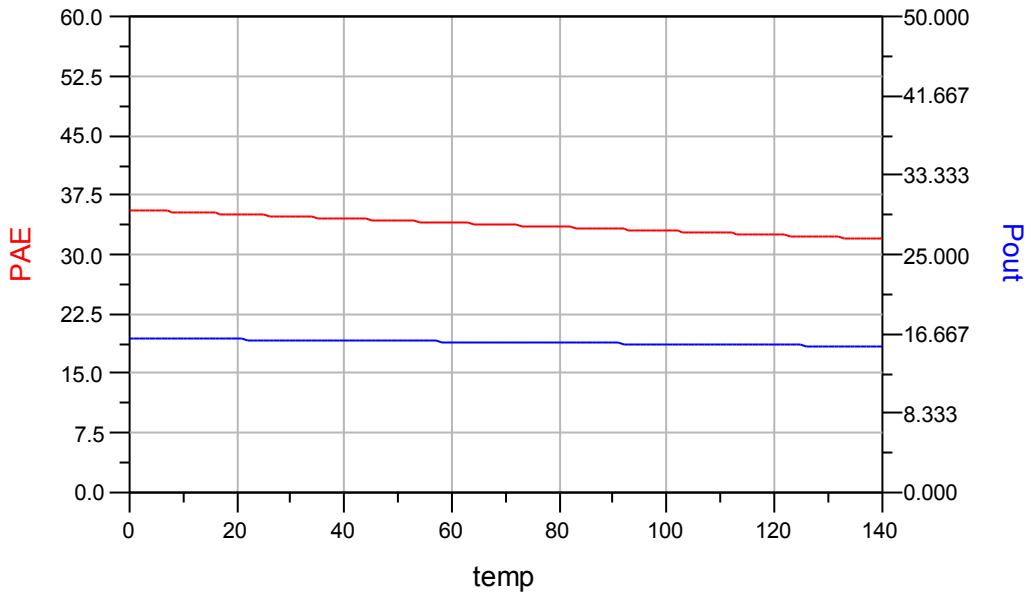

Figure 36: *PAE & P_{out}* versus temperature (Cascode class F PA)

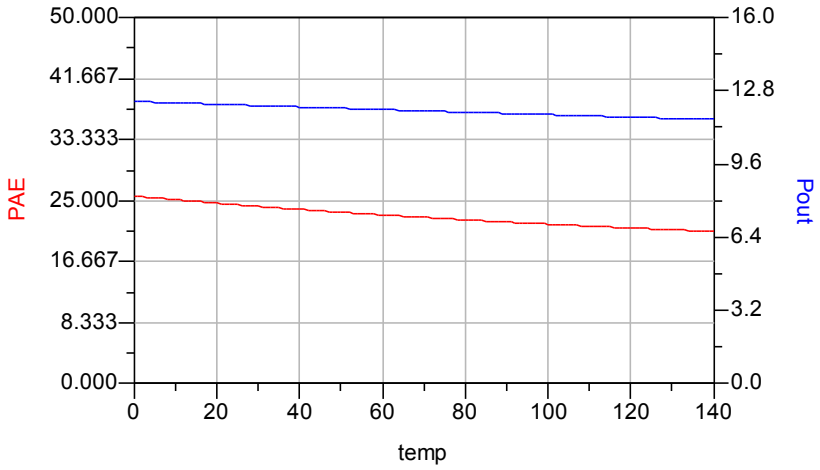

Figure 37: *PAE & P_{out}* versus temperature (non-Cascode inverse class F PA)

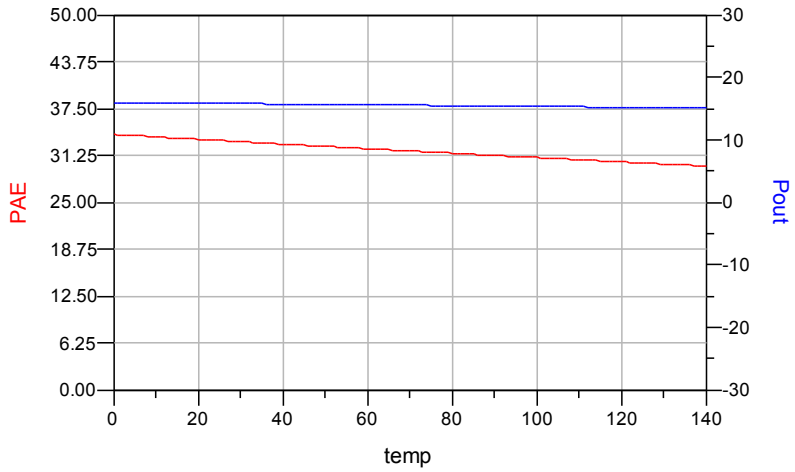

Figure 38: *PAE & P_{out}* versus temperature (Cascode-Inverse class F PA)

CHAPTER FIVE: SENSITIVITY ANALYSIS

Sensitivity analysis is the study of the variation in the output or circuit performance of a statistical model can be attributed to different parameters variation in the model parameters. It is a technique for symmetric variation analysis by using different iteration in a single simulation. For the sensitivity analysis the circuit has to be setup with a simulation tool called Monte Carlo in ADS. The number of iteration per simulation can me change according to how much accuracy demanded. The Monte Carlo simulation was performed in all the circuits.

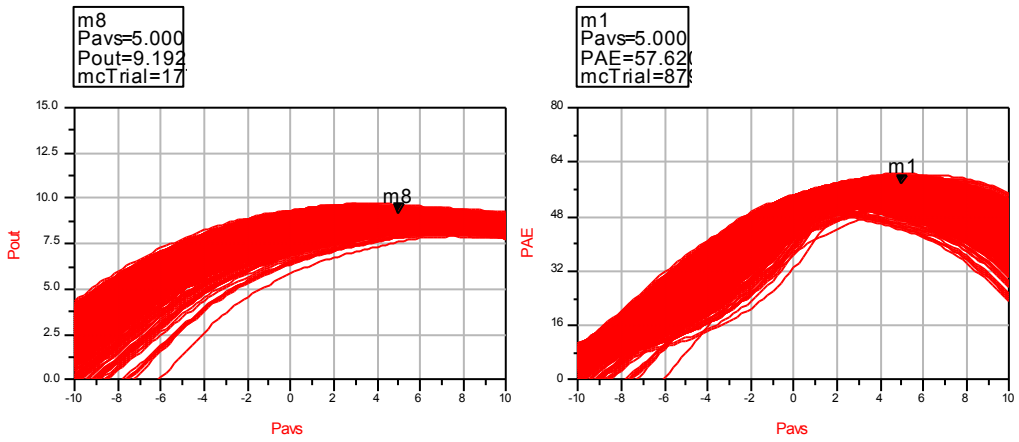

Figure 39: *PAE & P_{out}* result from Monte Carlo simulation (without substrate bias circuit)

The model were used for the sensitivity analysis was 65nm BSIM4. In this model the mobility and threshold voltage parameters can vary while the Monte Carlo simulation performs. Cascode class F and Cascode inverse class F circuits were simulated since the Cascode topology was the most efficient amplifiers.

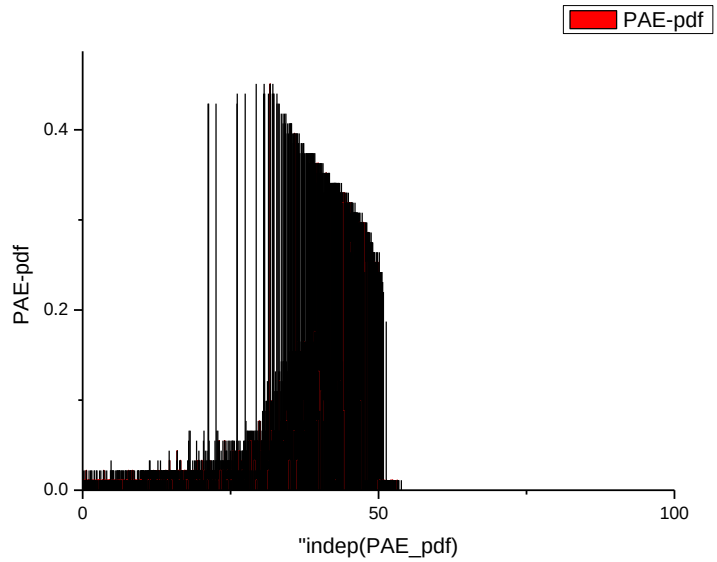

Figure 40: *PAE_* probability distribution factor (without substrate bias circuit)

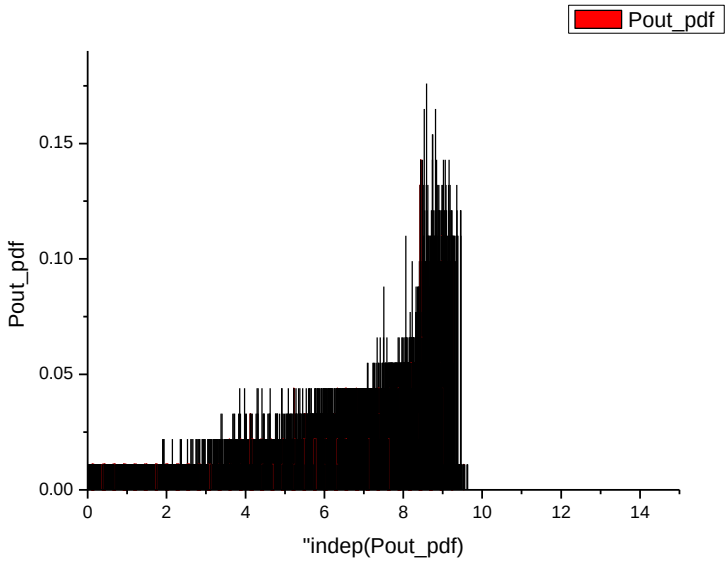

Figure 41: P_{out} _ probability distribution factor (without substrate bias circuit)

As seen in the figure shows, a large variation in the distribution factor were found. To reduce this variation a substrate bias circuit was implemented. Figure shows the circuit diagram with substrate bias circuit connected to the substrate of the main MOSFET.

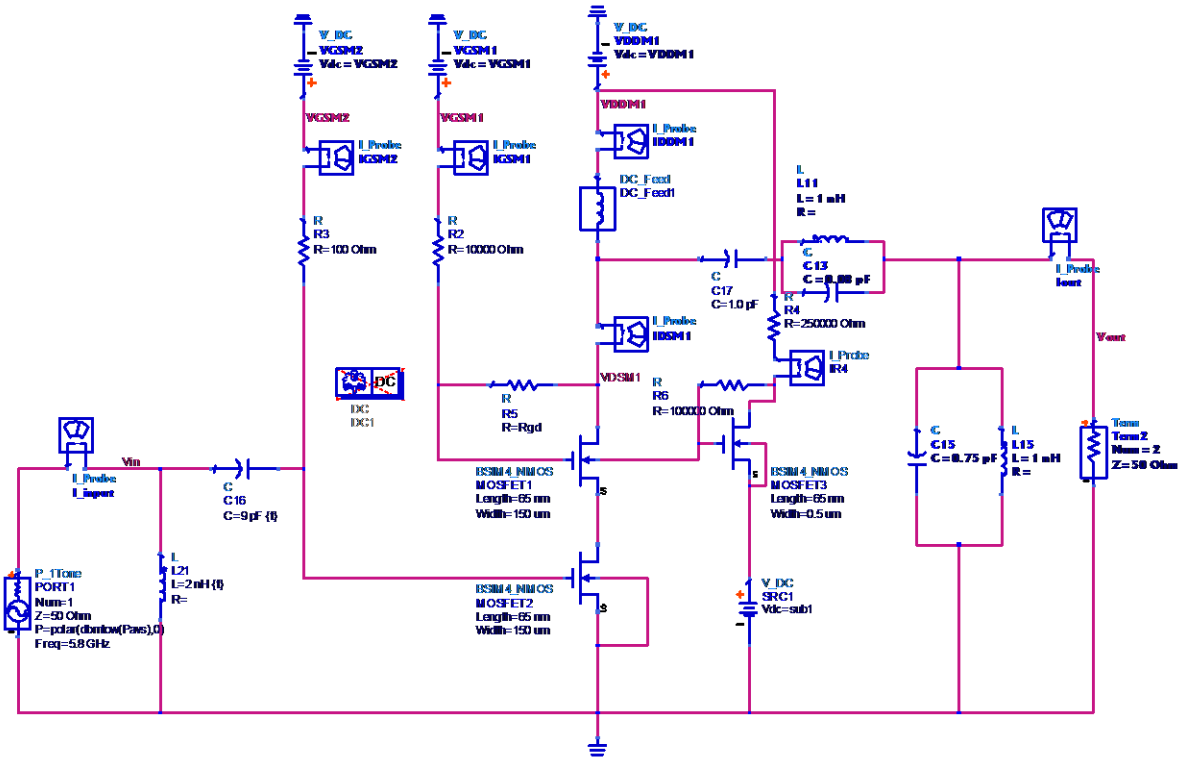

Figure 42: Cascode inverse class F PA with substrate bias circuit.

From the design, -2V were supplied to the substrate of the main transistor, which is connected via a transistor switch biased from the main V_{DD}. The gate of the substrtae bias circuit provides a -2V to reduce the variation in distribution. Figure given shows the simulation result of the Cascode class F power amplifier with substrate bias circuit.

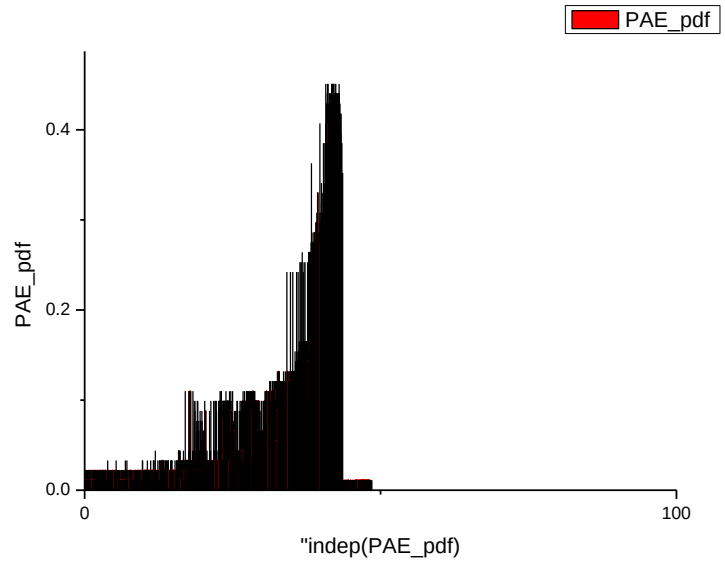

Figure 43: *PAE_* probability distribution factor (with substrate bias circuit)

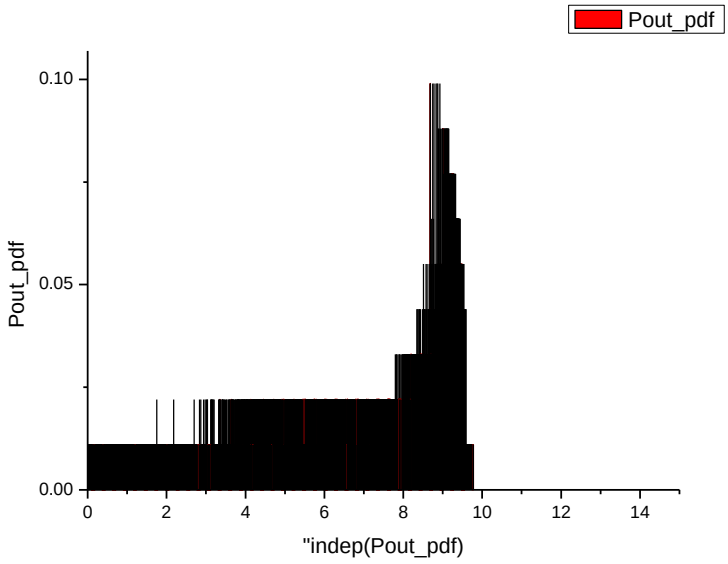

Figure 44: P_{out} _ probability distribution factor (with substrate bias circuit)

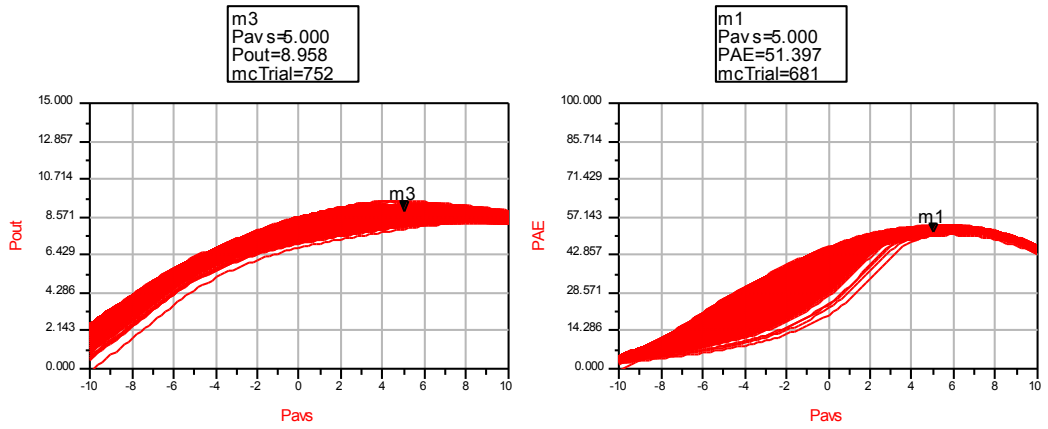

Figure 45: *PAE & P_{out}* - Monte Carlo simulation result (with substrate bias circuit)

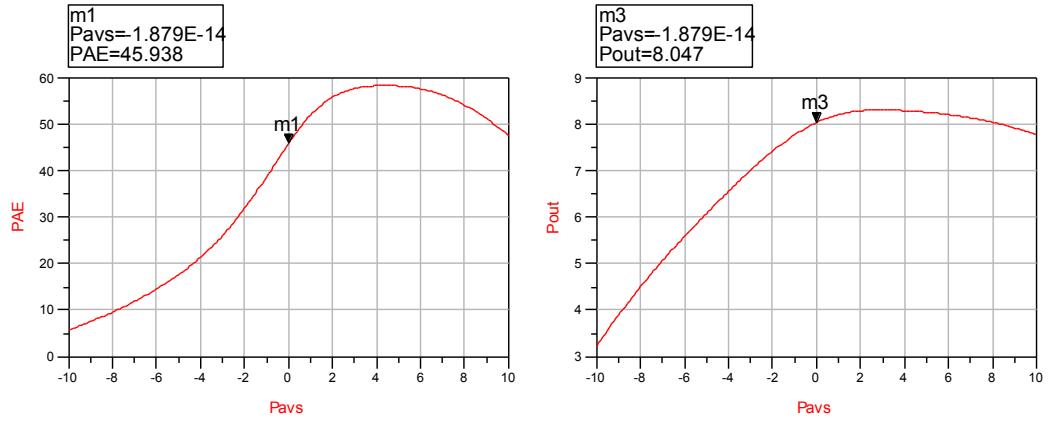

Figure 46: *PAE & P_{out}* (Cascode class F PA with substrate bias circuit)

CONCLUSION

This paper presented the design and analysis of class-F and inverse class F power amplifier both in non-Cascode and Cascode structures for using in the high efficiency wireless applications. TSMC 0.18μm CMOS technology and 65nm BSIM4 models were used for this amplifier design and analysis. The Rgd effects were analyzed both Cascode and Non-Cascode Class-F and Inverse class-F power amplifier for the first time in this paper. Additional harmonics tuning circuit will flatten the V_{DS} voltage, reduce the transistor loss, and improve the efficiency. There is a trade-off between the efficiency and circuit complexity of class F amplifiers. There is a trade-off among *PAE*, P_{out}, matching, and transient response for optimization. Cascode class F power amplifier reduces stress in the transistor to improve reliability. A substrate bias circuit helps reduce the variation of the parameter distribution (sensitivity).

FUTURE WORK

To layout the Cascode class F power amplifier with substrate bias circuit.

To fabricate the PA using *TSMC* process.

To test the fabricated power amplifier and verify circuit performance by experiment

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