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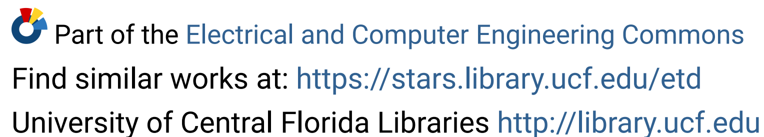

UNCOOLED INFRARED DETECTOR FEATURING SILICON BASED NANOSCALE THERMOCOUPLE

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical Engineering and Computer Science
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ABSTRACT

The main focus of this dissertation is to improve the performance of thermoelectric (TE) infrared (IR) detectors. TE IR detectors are part of uncooled detectors that can operate at room temperature. These detectors have been around for many years, however, their performance has been lower than their contesting technologies. A novel high-responsivity uncooled thermoelectric infrared detector is designed, fabricated, and characterized. This detector features a single stand-alone polysilicon-based thermocouple (without a supporting membrane) covered by an umbrella-like optical-cavity IR absorber. It is proved that the highest responsivity in the developed detectors can be achieved with only one thermocouple. Since the sub-micrometer polysilicon TE wires are the only heat path from the hot junction to the substrate, a superior thermal isolation is achieved. A responsivity of 1800 V/W and a detectivity of $2 * 10^8$ $(\mathrm{cm.Hz^{\frac{1}{2}}W^{-1}})$ are measured from a 20μm x 20μm detector comparable to the performance of detectors used in commercial focal planar arrays. This performance in a compact and manufacturable design elevates the position of thermoelectric IR sensors as a candidate for low-power, high performance, and inexpensive focal planar arrays. The improvement in performance is mostly due to low thermal conductivity of thin polysilicon wires. A feature is designed and fabricated to characterize the thermal conductivity of such a wire and it is shown for the first time that the thermal conductivity of thin polysilicon films can be much lower than that of the bulk. Thermal conductivity of ~110nm LPCVD polysilicon deposited at 620C is measured to be ~3.5W/m.K.

This Thesis is dedicated to my parents who relentlessly helped and guided me to be a better person and taught me that anything can be accomplished if it is done one step at a time. I sincerely thank my advisor, Dr. Reza Abdolvand, for teaching me not only the science and the knowledge that I needed but also life skills and the lifelong guidelines. I am also very thankful to my colleagues for their support and helpful discussions. Last but definitely not the least, I really want to thank my wife, Hedy, and dedicate my work to her. She has been on my side and supportive from the first day I started the graduate school. She always backed me up and helped me during rough times. I thank her for being there and being who she is.

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LIST OF ABBREVIATIONS

D*: Specific detectivity

η: fill factor

G: Thermal conduction

ICP: Inductively coupled plasma

IR: Infrared

K: Thermal conductivity

LPCVD: Low Pressure Chemical Vapor Deposition

NiCr: Nichrome

NIST: National Institute of Standards and Technology

NW: NanoWire

PC: PhotoConductors

Pt:Platinum

PolySi: Polysilicon

PV:PhotoVoltaic

R: Responsivity

RIE: Reactive Ion Etching

R_{IR}: Optical responsivity

R_{El}: Electrical responsivity

S: Seebeck

SEM: Scanning Electron Microscope

Si: Silicon

τ: Thermal time constant

TE: Thermoelectric

um: Micro meter

W: Watt

CHAPTER ONE: INTRODUCTION

Infrared (IR) radiation is utilized in many applications from identifying numerous materials through Fourier transform infrared spectroscopy to night vision cameras. The IR radiations are electromagnetic waves emitted from any object above zero Kelvin. The total radiated power can be estimated by Stefan Boltzmann law:

$$P_{rad} = \epsilon(T) * \sigma * T^4 \quad (1)$$

Where σ is Stefan Boltzmann constant and approximately is $5.6 * 10^{-8} (\frac{W}{m^2 * K^4})$, and Emissivity (or ϵ) is defined as the power radiated by an object to the radiation from a black body. This radiated power at any temperature varies in frequencies (or wavelengths) and follows Planck's radiation law:

$$M_e, \lambda = \frac{2\pi hC^2}{\lambda^5} \frac{1}{\exp\left(\frac{hc}{\lambda KT}\right) - 1} \quad (2)$$

Where h,C, λ, and K are $6.6 * 10^{-34}$ (Joule $*$ Sec), the speed of light, the wavelength in centimeters and Boltzmann's constant $1.3 * 10^{-23}$ ($\frac{Joul}{K}$) respectively.

Some of radiated power is absorbed by the molecules in the atmosphere and the remaining can propagate through. Water molecules for instance would absorb all the radiation between 5 um to 7.4 um [1]. At room temperature, most of the IR radiation is centered around 10um and interestingly, there is an atmospheric window from 8 to 14um that lets the radiation through with little to no absorption.

An IR detector can be used to detect the propagated radiation power at different wavelengths or a range of wavelengths. In any detector in general, the goal is to produce an electrical signal proportional to the incoming radiation. All the detectors can be categorized in two groups: photon

and thermal detectors

Photon detectors are mainly comprised of either photoconductors (PC) or photovoltaic (PV) detectors. In PV detectors, the IR radiation absorbed at the p-n junction can produce a measurable voltage. In contrast in PC based detectors, absorbed radiation would affect the conductance of the PC material that can be measured with a readout circuit. In general, photon detectors offer a good signal to noise ratio and a fast response to a change in the incoming radiation [2]. E.g. Mercury cadmium telluride (HgCdTe) or MCT can operate up to 30 um wavelength and can also be used as a photovoltaic device by stacking CdTe/HgTe on top [1].

For proper operation, however, these detectors must be cooled around or below ~77 Kelvin. At elevated temperatures, unwanted signal can be generated due to thermal excitation of the valence band electrons into the conduction band. The required cooling system adds extra cost and limitation to some applications where mobility is desired. There are also fabrication challenges, specifically for MCTs, such as material uniformity, lattice mismatch, and thermal expansion mismatch which make them unsuitable for 2D arrays [1].

Thermal detectors, on the other hand, do not require cooling and are usually offered at lower cost and smaller size compared to cooled detectors while their image quality is acceptable for many applications such as night vision. Resistive bolometers, pyroelectric, thermoelectric detectors, and Golay cells [2] are the main subcategories of this class.

Bolometers utilize a resistive material with a large temperature coefficient of resistance (TCR) [3]. Vanadium oxide and amorphous silicon are examples of resistive materials that are commonly used in bolometers [2]. Upon absorption of IR radiation, the resistive material heats up and the read-out circuit measures the thermally-induced change in the resistance. One great advantage of

bolometers over their rivals is that their responsivity is not only a function of material properties but also is proportional to the applied bias current/voltage. This means that in order to have a large output response, the bias current could be increased to the limit of destruction [4].

Pyroelectric detectors employ materials like barium strontium titanate (BST) to detect IR radiation [1]. Temperature change in pyroelectric materials alters the internal dipole moments, which induces an instantaneous surface charge that can be measured by a read out circuit. These detectors offer high responsivity and have been used in large format arrays [1]. However, to create a temperature change inside the pyroelectric material, the incoming radiation has to be modulated by a mechanical chopper. Although adding a chopper helps in eliminating multiple sources of noise such as substrate temperature drift, but it is not suitable for applications in which ruggedness, low power consumption, and compact size are of prime importance. In addition, pyroelectric material processing is costly and not CMOS-compatible which adds complexity to the design.

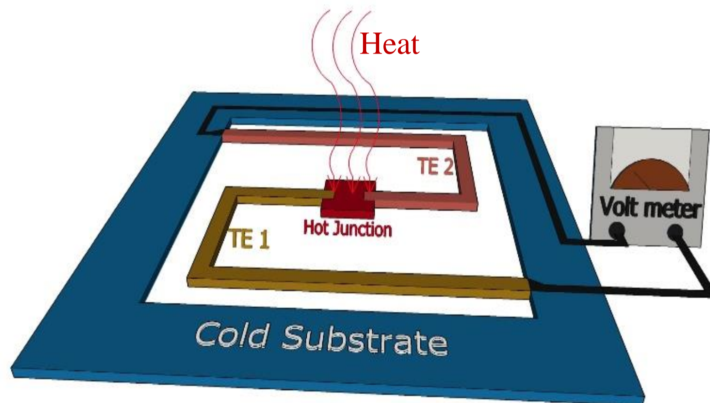


Figure 1. A schematic showing two different TE materials connected between a hot junction and a cold substrate

Golay cells can also be considered as a different type of thermal detectors. The gas contained

in a cell can expand due to absorption of the IR radiation and deforms a membrane. The induced stress in the membrane can be measured with different techniques. These detectors are bulky and not suitable for imaging applications.

Thermoelectric detectors which are the focus of this work operate based on the Seebeck effect [5] which is the ability of some materials to produce a voltage when there is a temperature difference across their ends (Figure 1). TE detectors do not require choppers (the output is a function of temperature difference as opposed to temperature change in pyroelectrics). Moreover, no temperature stabilization (i.e. peltier coolers) is required since the output signal is produced by the difference between the temperature of a thermally-isolated structure and its substrate. In fact, it has been shown that thermopiles are much less sensitive to change in the instrument (housing) temperature than bolometers [6]. One great advantage of TE detectors is that they usually operate under an open circuit condition which means almost no current is flowing in or out of the device. Therefore, negligible shot and 1/f noise are expected [7], leaving Johnson noise as the primary source of noise. Comparing this to bolometers in which the contribution of both Johnson noise and the 1/f noise coming from the large bias current are considerable, it is believed that thermopiles are great candidates for low noise applications. However, the relatively low responsivity of TE detectors has been a barrier for their widespread use in IR imaging applications.

A history of the thermoelectric infrared detectors will be presented in the next chapter followed by the basic operation concept of the detectors. In chapter 3, the design details of a TE detector will be discussed. Finite element analysis of the detectors is brought next followed by the fabrication process. Measurement results are summarized at the end of this chapter. Next chapter is focused on measuring thermal conductivity of polysilicon nanowires and thin films. Design,

fabrication, measurement setup and results are all summarized in the same chapter respectively.

The summary and the conclusion is in the final chapter, chapter 5. Future research and possible improvements are also summarized in this section.

CHAPTER TWO: LITERATURE REVIEW

2.1 History

Since the discovery of Seebeck effect, there has been numerous works on thermoelectric detectors and sensors and especially in the past decades, micro-machined infrared detectors have been the focus of many researchers. In 1986, Choice and Wise reported the fabrication of a thermopile array with the responsivity of 12 V/W and the detectivity of $5 * 10^7 \ \frac{\mathrm{cm} * \sqrt{\mathrm{Hz}}}{\mathrm{W}}$ [8]. In this context, responsivity is defined as the electrical output voltage per input radiation power and detectivity is found using the following:

$$\mathrm{D}^* = \frac{(\mathrm{A_d} * \Delta \mathrm{f})^{0.5}}{\mathrm{Vn}} * R_v \tag{3}$$

Where A_d is the area of the detector, Δf is the electronic bandwidth, and V_n and R_v are the RMS electronic noise and responsivity respectively. The higher the responsivity and detectivity are the better the detectors. Choice [8] used 40 thermocouples of polysilicon and gold. Their detector area was 400 um * 700 um, which is relatively large compared to the today's technology. Volkein et al. reported a fabrication of single pixel detector by using BiSbTe and BiSb thermocouple pairs with the responsivity of 500 V/W in 1991 [9]. A year later, a responsivity of 150 V/W was reported by ETH for a detector with p type and n type thermocouple pair that was fabricated on a chip with Op-Amps [9]. Kanno et al. in 1994, from the Japan Defense Agency in collaboration with NEC Corporation made a 128 * 128 pixel thermoelectric array using p and n type polysilicon. The responsivity of 1550 V/W was measured with the pixel size of 100 um * 100 um [9]. In 1998, Foote et al. reported the construction of 1500 um * 75 um, linear array detector which was made

of BiTe and BiSbTe thermocouple materials. Their device had a responsivity of 1100 V/W while the response time of the device was about 99 ms [10]. In the same year, Nissan research laboratory, (Hirota et al.) reported the fabrication of a 48 * 32 pixel array with a pixel size of 116 um * 116 um. Their pixel was supported with two isolation beams that each one was 14 um wide. The thermopile itself was 0.8 um. Each pixel consisted of a six pair thermocouple and they could reach 2100 V/W responsivity. Three years later, in 2001, they improved their pixel performance and could reach 2770 V/W. To do so, they reduced the isolation beam width from 14 um to 4.4 um. This time the pixel size was also reduced to 100 um * 100 um with a absorber size of 65 um * 65 um. Four years later, 2005, they made an array of 48 * 48 pixels with their best devices with the responsivity of 4300 V/W. This improvement was due to reduction of the beam and the thermopile width to 2.4 um and 0.34 um respectively [11].

David Kryskowski and Justin Renkenc, in 2009, made a large array of 80 * 60 pixels. n and p type silicon was used as the thermoelectric materials to produce the responsivity of 300 V/W for a detector size of 130 um * 130 um [12].

2.2. Principle of thermoelectric detectors

Any thermal detector has a structure like the one shown in Figure 2. The incoming infrared radiation incidents on the sensor and is absorbed by the absorber layer on the surface. This causes the temperature of the sensor to rise and creates a temperature difference between the sensor area and the substrate.

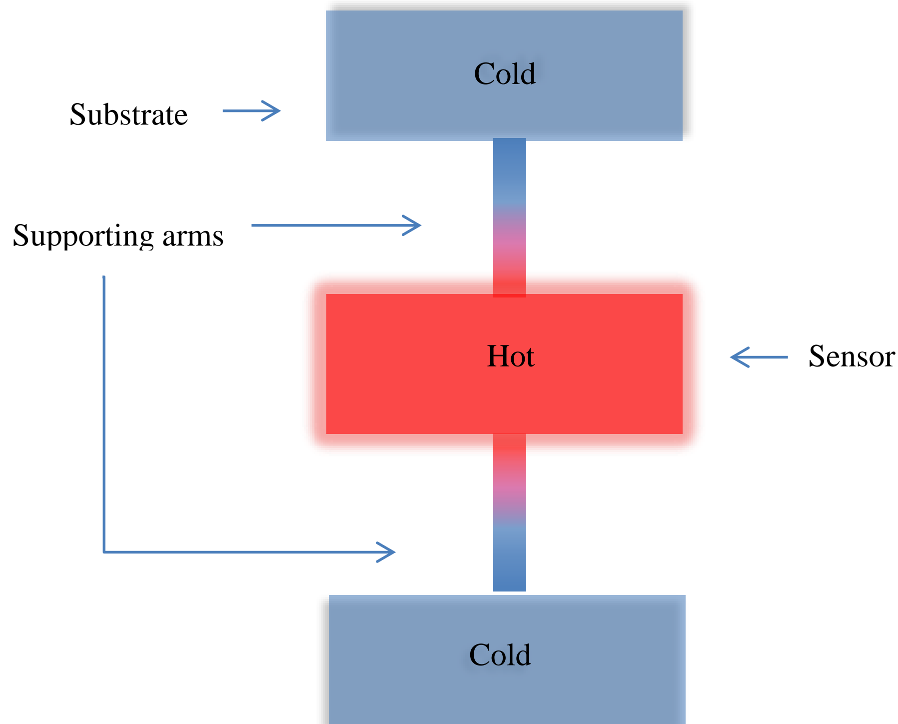


Figure 2. Principle of thermoelectric detector

The temperature difference between the hot element and the substrate can be converted to an electric signal and measured by a precision voltmeter. The output voltage can be expressed in the following mathematical format:

$$\delta V = S * \delta T \tag{4}$$

Where S is called Seebeck coefficient and δT is the temperature difference between the cold and hot junctions. As it can be seen in the above equation, materials with large Seebeck coefficient can produce large output voltages with a same temperature difference. This is the first important point in the thermoelectric detectors that a material with high Seebeck coefficient should be used. Metals usually have Seebeck coefficients less than $50 * 10^{-6}$ V/K and semiconductors have larger

Seebeck coefficient (e.g. Silicon = $400 * 10^{-6}$ V/K and Se = $900 * 10^{-6}$ V/K [13]). Unfortunately, intrinsic semiconductors have very low electrical conductivity, and hence very high electrical resistivity which is not desired for sensor applications. One reason is that the noise voltage generated by the thermal noise (shown in the equation below) will be very large if the electrical resistance is high. The Johnson noise for a resistor can be found using the following equation:

$$V_n = \sqrt{4k_B TR\,\Delta f} \quad [14] \tag{5}$$

Therefore, materials with low resistivity are required. From another point of view, if the output impedance of the detector is high, most of the output voltage drops across the internal resistor and there would be no detectable voltage at the output of the device.
To increase the electrical conductivity, semiconductors have to be doped to some level. When semiconductors are highly doped (if possible), their properties becomes similar to that of metals meaning that the Seebeck coefficient decreases and the electronic part of the thermal conductivity increases. Both of these effects are not desired. The importance of low thermal conductivity of the thermoelectric materials will be discussed later in the next section.
ZT is the thermoelectric figure of merit which is used to express the performance of a thermoelectric device. [15] ZT is defined as

$$ZT = \frac{S^2\sigma}{K}\,T \tag{6}$$

Where T, S, σ and k are temperature in Kelvin, Seebeck coefficient, electrical conductivity and thermal conductivity respectively. It has been shown that high ZT is achievable on highly doped

semiconductor where the doping concentration is somewhere between 10^{19} to $10^{21}\ \frac{\text{carrier}}{\text{cm}^3}$ [16]. Figure 3 shows the variation of ZT versus doping concentration [16].

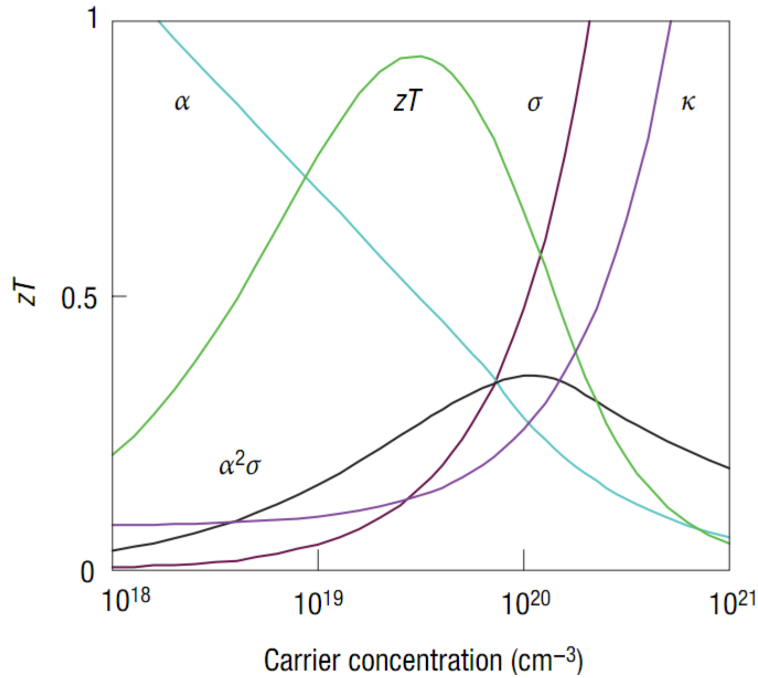


Figure 3. ZT and power factor vs. doping concentration for Bi_2Te_3(Reprinted with permission from Nature Publishing Group)

Power factor which is defined as $S^2\sigma$ is also shown in Figure 3. Power factor is also important in the nanostructured materials where lattice thermal conductivity is dominant portion of the thermal conductivity. In this situation, power factor is tried to become maxmized and once that is achieved, reduction in the thermal conductivity by the means of nanostructuring is also attainable at the same time [17, 18]. The conclusion is that to produce a large electric signal at the output, a material with high ZT at room temperature should be chosen. This material should also be compatible with the fabrication processes like deposition and etching. Polysilicon is a good option since it is compatible

with conventional CMOS processes. It is not the best thermoelectric material at room temperature because of its high thermal conductivity but it has relatively high ZT comparing with other materials especially if nanowires are used instead of a bulk material [19, 20].

Earlier in the previous section, it was noted that the thermal conduction from the hot surface to the surroundings should be minimized. The reason is that to make a larger δT and hence larger δV ($\delta V = S * \delta T$ (4)

$\delta V = S * \delta T$) with the same amount of input radiation. There are three major mechanisms for heat transfer from the hot element to the surroundings: conduction, convection and radiation [9]. Uncooled infrared detectors should operate under vacuum (<10 mTorr) to eliminate convection and conduction through the gas in the package [21]. Heat loss from the hot element due to radiation is usually negligible compared to heat loss through the supporting arms which is the principal heat loss mechanism. Thus, the heat conduction through the supports should be minimized. Supports are composed of the thermoelectric materials and few protective layers which enclose the thermoelectric materials to protect them in different steps of fabrication from solvents and other corrosive gases and also to provide the required mechanical strength.

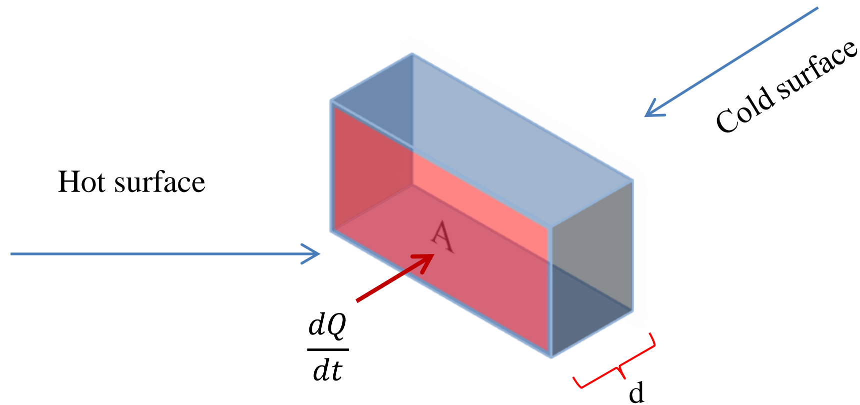


Figure 4 - Fourier law in 1D

In our work, polysilicon used as the thermoelectric material but since it has high thermal conduction, the cross section of the wires is made very small to lessen its undesired effect. As it is seen in the equation below:

$$\frac{dQ}{dt} = -K * A * \frac{dT}{dx} \tag{7}$$

where the parameters are shown on the Figure X, the rate of the heat flow (dQ/dt) can be decreased by reducing the thermoelectric material cross section, A, between hot and cold surfaces. In addition, the longer the length of the support is, the lower would be the rate of the heat flow. In conclusion, a long silicon nanowire would be proper for the TE wire. There is also another important phenomenon that should be stated here. Silicon nanowires have electrical conductivity and Seebeck coefficient that do not vary by much from the bulk values, but their thermal conductivity is almost 100 times less than the bulk value [22].

Unfortunately, Silicon nanowires do not have enough mechanical strength to survive the fabrication process and they might break. Therefore, another material with low thermal conduction should support and protect the nanowires during the fabrication steps. Silicon dioxide and silicon

nitride films have been used for the purpose of protecting different thermoelectric materials [23, 24].

At some part of this, work Parylene has been used to support the silicon nanowires. Parylene is a polymer that has been used in printed circuit board industry and has a very low thermal conductivity ($\sim 0.1\ \frac{W}{m*K}$) [25]. Comparing the thermal conductivity of Parylene to silicon dioxide ($\sim 1.4 \frac{W}{m*K}$ for thickness larger than 250 nm) [26] and silicon nitride ($\sim 32\ \frac{W}{m*K}$) [27] shows that using Parylene as the supporting arms can substantially improve the detector performance (Actual values of thermal conductivity for the stated material may change with different thicknesses and the deposition techniques). In the latest work, it will be shown that even the thin polysilicon layers can solely be used to form the structure. Moreover, it will be shown that even though the thermal conductivity of the parylene layer is very low, it still has a substantial adverse effect.

CHAPTER THREE: THERMOELECTRIC INFRARED DETECTOR

In this chapter, the details of the design for different sections of the infrared detector will be discussed. As a result of this work, it is shown that thermoelectric infrared detectors with only one thermocouple, instead of having a thermopile, can potentially produce the largest temperature difference between the suspended island (and the absorber) and the substrate which can lead to higher performance devices compared to other designs.

A new figure of merit for evaluation of thermoelectric materials is also introduced. The conventional figure of merit, ZT, was defined based on power generation applications. On the other hand, ZT/k, the new figure, is more appropriate for sensing applications and shows the importance of reducing the thermal conductivity to achieve higher performance. The new merit may help the designers to choose the best material among the available options.

The detector performance is predicted using finite element analysis. Vibration modes are also predicted for a structure similar to a fabricated one and it is shown that the generated phononic noise has higher frequency than the operating bandwidth of the device which means that vibration related noise can be filtered out effectively.

The fabrication process of these detectors is also laid out next. The process flow is presented first and it is followed by discussions on different steps of the process. It will be discussed why different sacrificial layers were chosen. Some of the process recipes are included here and the effect of varying some parameters are explained.

At the end of this chapter, the process of measuring the performance of the detectors will be discussed. The measurement results is summarized at last. To the best of author's knowledge, the highest reported responsivity and detectivity is reported for a detector of $20\ \mu m * 20\ \mu m$ size.

3.1 Design

There are a few important parts to a thermoelectric infrared detector and they will be detailed in this section. The first and the most important part of thermoelectric detector is the thermoelectric material. The material with high Seebeck, high electrical conductivity and low thermal conductivity is desired. It will be discussed in details that why polysilicon is chosen for this purpose. The level of doping can be used to adjust the thermoelectric parameters to a desired level.

In any thermal detector, the incident radiation needs to be absorbed at high rate. The thermal absorber design for the detectors will be laid out in the next subsection. Cavity absorbers will be compared to other coatings and absorbers and the design of this work will be detailed later.

There are a few options for a thermal detector structure. This work is based on a umbrella design which provides the maximum fill factor

3.1.1 New figure of merit

The main component of a TE IR detector is the TE material which senses the temperature difference between the absorber and the surroundings. To compare the efficiency of different TE materials, ZT is the most common figure of merit and is defined as $\frac{S^2}{\rho K} * T$ where S is the Seebeck coefficient, ρ, K, T are the electrical resistivity, the thermal conductivity, and the absolute

temperature respectively. ZT represents the efficiency of a TE material in generating electrical power [28].

However, it is more appropriate to use ZT/K as a figure of merit in sensing applications [29]. This definition is directly drawn from the specific detectivity (D*), which is defined as $\frac{\sqrt{A_d * \Delta f}}{V_n} * R_{v,DC}$ where A_d and Δf are detector area and $R_{v,DC}$ and V_n being the DC responsivity and noise voltage. D* is the most common figure for comparing the performance of different detectors.

To derive the dependency of D* on the material properties, closed-form equations for DC responsivity and noise voltage are required. DC responsivity of a TE detector is

$$R_{DC} = \frac{\eta N S}{G} \text{ [1]} \tag{8}$$

where η, N, and G, are detector absorptivity, number of thermocouples, and thermal conduction from the detector respectively. Detector noise voltage, under the assumption that Johnson noise is the only source of noise, for a given bandwidth, Δf, is

$$v_n = \sqrt{4 K_B T R \Delta f} \text{ [14]} \tag{9}$$

where K_B is Boltzmann's constant, T is the detector absolute temperature and R is the detector resistance. By substituting the responsivity and noise voltage in D* and by neglecting spatial and time dependent parameters, it can be shown that D* is proportional to

$$\frac{S}{\sqrt{\rho * K}} \text{ or } \sqrt{\frac{Z}{K}} \tag{10}$$

For ease of comparison and using the results of the previous works in thermoelectric materials,

$$\frac{Z}{K} * T \tag{11}$$

will be used here instead of $\sqrt{\frac{Z}{K}} * T$.

presents ZT, thermal conductivity, and ZT/K for two different bismuth telluride compounds. The first compound, $(Bi_{0.25}Sb_{0.75})_2Te_3$, has a ZT of 1.5 which is more than twice the value of the other compound and is a superior thermoelectric material at room temperature for power generation. However, the newly defined figure of merit (ZT/K) for the Tl_9BiTe_6 compound is calculated to be 1.67 and is higher than that of $(Bi_{0.25}Sb_{0.75})_2Te_3$ showing that the former is potentially a better candidate for IR detection. This example emphasizes the effect of thermal conductivity reduction in sensing applications.

Table 1. Comparison chart for ZT and $\frac{ZT}{K}$ of $(Bi_{0.25}Sb_{0.75})_2Te_3$ and Tl_9BiTe_6 at room temperature.

Material name	ZT	Thermal conductivity (W/m.K)	ZT/K
$(Bi_{0.25}Sb_{0.75})_2Te_3$ [30]	1.5	1.2	1.25
Tl_9BiTe_6 [31]	0.65	0.39	1.67

3.1.2 Thermoelectric material

In general, uncooled infrared detectors are intended to work at room temperature and BiTe compounds have yet the highest performance in this range [32]. However application of BiTe to achieve the highest levels of system integration is challenging. This is mainly because processing BiTe is neither compatible with the fabrication of microelectronic circuits nor cost effective.

Furthermore, in small pixel arrays, the slightest material non-uniformity over the area of the array will deteriorate the detectors' performance and needs further attention [33].

The most natural choice to guarantee large scale manufacturability is silicon-based materials. However, silicon was not perceived as an efficient thermoelectric material until recently that silicon nanowires (SNWs) were shown to exhibit ZT values as high as 0.6 and thermal conductivity of as low as 1.6 W/m.K close to the amorphous Si limit [22,34]. Such low thermal conductivity in SNWs is mainly a result of phonon boundary scattering and this property of nanowires was the motivation to use doped polysilicon as thermoelectric wires in our detector. It is expected to achieve even lower thermal conductivity in polysilicon compared to silicon because of its granular structure resulting in more phonon grain boundary scattering [35] while electron scattering is minimally affected. Moreover, thin film polysilicon deposition/patterning are amongst very mature micro-fabrication processes [36,37] with a high degree of control over grain size, thickness, preferred crystalline orientation, percentage of crystallinity and doping concentration.

It has been known that high ZT is achievable in highly-doped semiconductors [16]. Since the thermal conductivity of semiconductors is mostly affected by the lattice structure and not by the electrons, it is believed that the thermal conductivity could be altered by nano-structuring with slight dependency on the other parameters. Therefore the objective for thermoelectric optimization of polysilicon should be to maximize $S^2\sigma$ (called power factor $\sigma = \frac{1}{\rho}$). Low doping concentration is desired to achieve high Seebeck coefficient while high electrical conductivity is demanded for lower voltage drop inside the detector, and lower Johnson noise. Since Seebeck coefficient and electrical conductivity are not independent from each other, there is an optimal point at which the

power factor is maximized. It has been proved that for any TE material there exists an optimal Seebeck value and that is in the range of 130 to 187 $\frac{\mu V}{K}$ [38] which occurs at high dopant concentration (>10^19) in silicon. Thus, one could control Seebeck and electrical conductivity by doping concentration and manipulate thermal conductivity by changing the grain size, crystalline orientation, dopant type, percentage of crystallinity, and the size of the thermoelectric wires. 115nm thick phosphorous and boron doped polysilicon films deposited at $630°C$ are used to produce the TE wires of this work and a doping concentration close to ~10^20 is targeted.

3.1.3 Number of required thermocouples

To improve the performance of a TE detector, traditionally they are placed in series to each other to enhance the output voltage. In this work, only one thermocouple is used and below, it is shown that using more than one pair will adversely affect the detector's performance.

As described earlier [1], the DC responsivity of a thermopile is given by $R = \frac{\eta * N * S}{G}$. If G is only comprised of $N * g$ where g is thermal conduction of one thermocouple (i.e. the only thermal path is through the thermoelectric wires which is the case in our design), then the responsivity becomes $R = \frac{\eta * S}{g}$, independent of the number of thermocouples. Thus, adding more thermocouples will not increase the responsivity. On the other hand, it increases the detector resistance resulting in higher Johnson noise and ultimately lower detectivity. If there is any thermal pass other than TE wires between the isolated structure and the surroundings like a protective layer or a membrane, then adding more thermocouples may be beneficial depending on the contribution of the residual path in the overall thermal conductivity.

Even if the increase in the Johnson noise is negligible due to other sources of system level noise it is shown here that using one thermocouple is still preferred because of the following. The maximum efficiency of a heat engine is limited by its Carnot efficiency ($\eta_c = \frac{\Delta T}{T_H}$ where T_H, and ΔT are the hot junction and the difference between the hot and cold junction temperature respectively). The total efficiency of an actual system can be written as the product of its Carnot efficiency by a factor calculated for that specific system. For a thermoelectric material assuming that the material properties are not changing with temperature which is the case for IR sensors (since the temperature variation across the device is commonly less than one Kelvin), the total efficiency is found to be

$$\eta = \eta_C * \frac{\sqrt{1+Z\overline{T}}-1}{\sqrt{1+z\overline{T}}+\frac{T_C}{T_H}} = \eta_C * \frac{\sqrt{1+Z\overline{T}}-1}{\sqrt{1+z\overline{T}}+1-\eta_c} \text{ [28]} \qquad (12)$$

where $\overline{T}$, is $\frac{T_H+T_C}{2}$, and T_C is the substrate temperature (assumed constant) and T_H is the isolated membrane temperature which only rises slightly above T_C. As it can be seen for this situation, the higher the η_C the better the overall efficiency and this can be achieved by using the least number of TE pairs.

3.1.4 Thermal absorber

Another important part of any thermal detector is its radiation absorber. High radiation absorption is necessary to produce large output signals. Different materials and structures have been proposed and used for the absorber. Metal-black coatings such as gold-black, silver-black, platinum-black, etc. have been used by researchers and companies for years [24,39,40]. Most of the metal-black coatings are deposited using evaporation technique at high nitrogen pressure.

Among the coatings, gold-black has relatively low density, low reflection, and high thermal conduction. If the Au-black is deposited thick enough, the transmittance would be also zero and hence the incident radiation would be fully absorbed. In addition, it can be used for a wide range from 1 um to 50 um wavelengths range [39]. Unfortunately, the gold-black coatings can be easily scratched, damaged and destroyed with a physical contact, air flow and/or if they become wet [39]. Therefore, it is very hard to pattern the deposited film and it has to be the last step in the fabrication process. Usually proximity masks [41] or laser trimming is used to pattern the film. Overall, consistency is a problem in using gold-black coatings.

Silver-black is also can be deposited in high argon pressure [42] and it also has low reflectance. One advantage of silver-black over gold-black is that it is more mechanically stable and scratch resistant [39].

Other black coatings like graphite-black, catalac-black, etc. can also be used as an absorber material but when the absorber size is so small like 80 um * 80 um, it would be difficult to pattern them and if there is an array of detectors that are closely fabricated, thick coatings can connect the adjacent absorbers to each other and reduce the final image resolution.

Optical cavities are also being used to maximize the absorption of the incident radiations. It has been shown that in a metal – dielectric – metal configuration with two different metals of different thicknesses, high absorption can be achieved [43,44]. The first metal layer on top should have a sheet resistance of 377 $\frac{\Omega}{\blacksquare}$ [44,45]. The dielectric layer can be any material with good thermal conductivity and extinction coefficient (imaginary part of the refractive index or K) of zero at/and around the resonance frequency of the cavity. Silicon nitride due its compatibility with out

fabrication process is chosen as the dielectric material in this work. The thickness of the silicon nitride determines the resonance frequency of the cavity and is found using $\frac{\lambda}{4n}$ where λ is the wavelength of maximum absorption and n is the refractive index of silicon nitride. The bottom metal layer should be a perfect reflector with a sheet resistance of 37 $\frac{\Omega}{\blacksquare}$ or lower [44]. Metals like gold, platinum, and nickel are preferred reflectors in the range of 2 to 15um. Although nichrome is not as good of an IR reflector and slightly degrade the absorber's performance, it is used in this work due to its fabrication compatibility with the rest of the process.

The following sections explains how metals can be a good infrared absorber. Metals usually have high reflection because of their high refractive index. To increase the absorption or lower the refractive index, the metal layer should become thin [44, 45,46]. At normal incidence to the surface, reflectance, R, can be calculated using Fresnel equations.

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right) * \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^* \text{ [47]} \tag{13}$$

As an example, at the interface of air ($n_1 = 1$) and copper ($n_2 = 10.8 + j\ 47$ at9.5 um [48]), 98% of the incident radiation will be reflected.

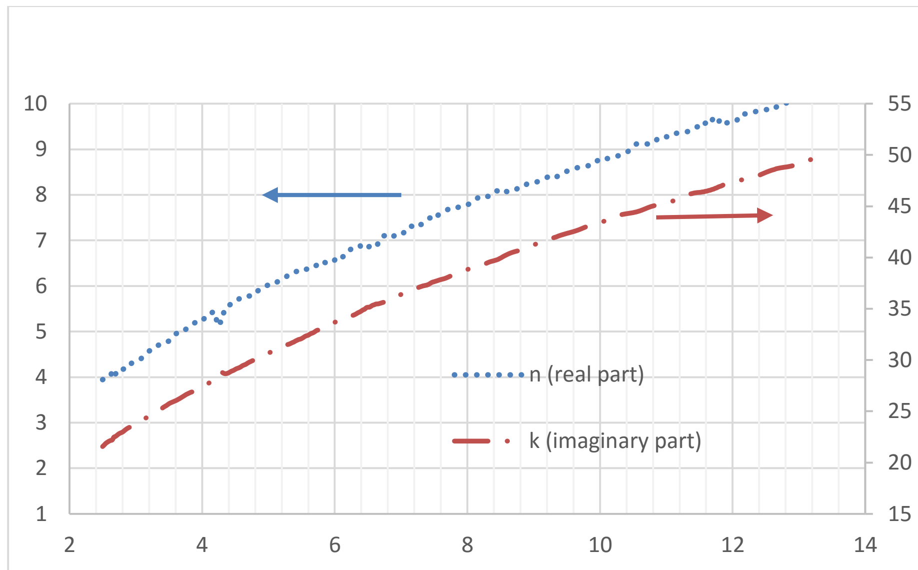
In the infrared region, refractive index can be approximated by [44]

$$n = k = \left(\frac{\sigma}{2 * \omega * \epsilon_0}\right)^{.5} \tag{14}$$

Where k is the extinction coefficient, σ is electrical conductivity, ω is the incoming light frequency in radian, and finally $\epsilon_0 = 8.85 * 10^{-12}$ is the vacuum permittivity. Therefore, based on the above equation, if the metal film thickness is reduced, its sheet resistance ($\frac{1}{\sigma}$) increases and hence the final refractive index will be lowered. As a result, the reflection intensity will be reduced.

If a ray can make into inside of a metal film, it will be absorbed since metals are generally good absorber because of their large extinction coefficient but if they are made very thin, the ray may go through the film without being absorbed, therefore, the optical cavity is required to make multiple passes for any ray to assure its absorption.

To simulate the absorption of a three layer absorber stack over the desired range of frequencies, the complex refractive indexes of nichrome and silicon nitride are required. To find these values, two samples of 2.5nm of nichrome, and 1 um of PECVD silicon nitride was deposited on two 1mm thick germanium substrates. Then the reflection and transmission spectra of each sample were recorded using an FTIR (Fourier transform infrared spectroscopy) system. A contour map of reflection and transmission spectra for a range of n and k (real and imaginary parts of refractive index) was created and overlapped with the experimental results [49,50]. Out of the possible solutions, a meaningful initial estimate was used to choose the correct solution [51]. In the computation of the aforementioned spectra, coherent radiation in the thin film and incoherent reflection in the substrate is assumed. The calculated complex refractive index is shown in Figure 5.



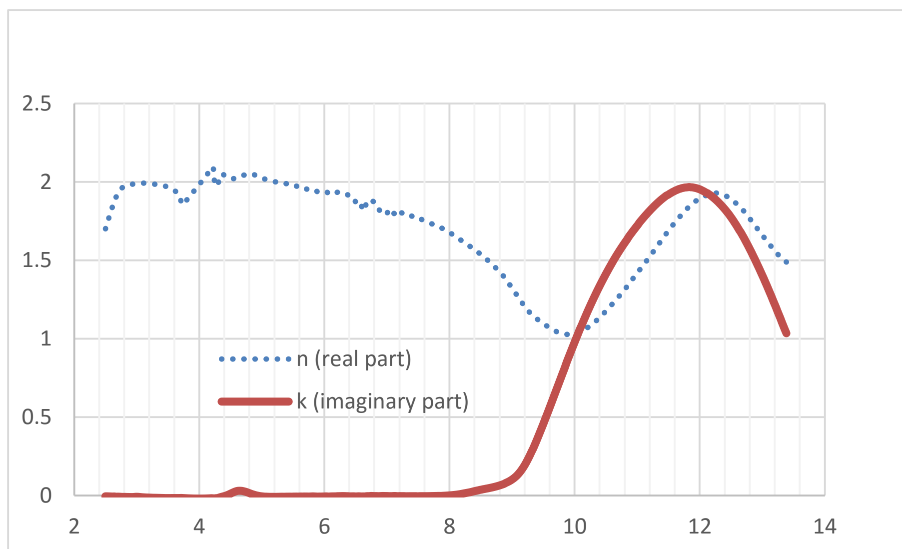


Figure 5. Complex refractive index of 2.5nm sputtered nichrome and 1um PECVD silicon nitride

The absorption spectra of the three layer stack was then calculated based on the above information and formulation presented in [52] with slight modification and presented in Figure 6.

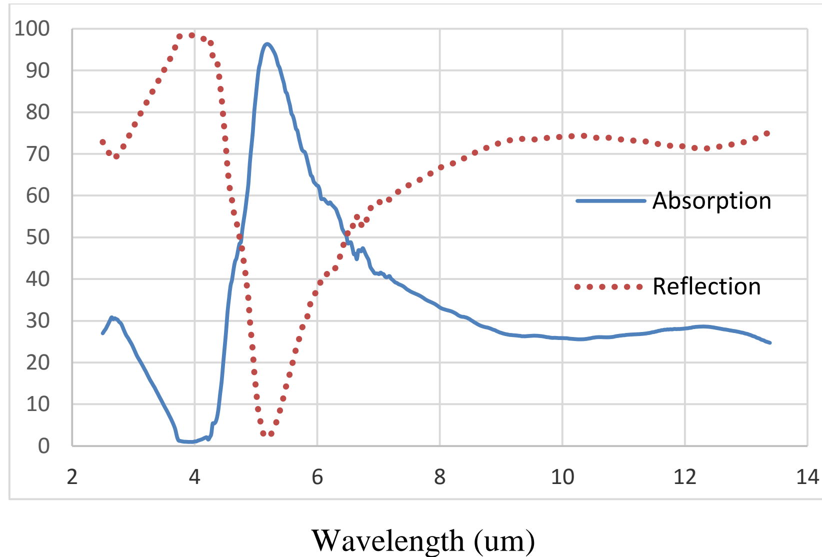


Figure 6. Absorption spectra of a three layer stack

This absorber is designed to have maximum absorption around 5.8um which is the peak of the spectral-exitance of a blackbody at 500K (for lab measurement purposes).

3.1.5 Detector Structure

The detector structure is schematically presented in Figure 7(a) and is comprised of TE wires and an umbrella-like absorber on top anchored to a suspended membrane through a post. This structure requires a more complex fabrication process compared to the single level design developed by others (e.g. Honeywell [53]). However, a higher fill factor and contrast ratio is expected from this design.

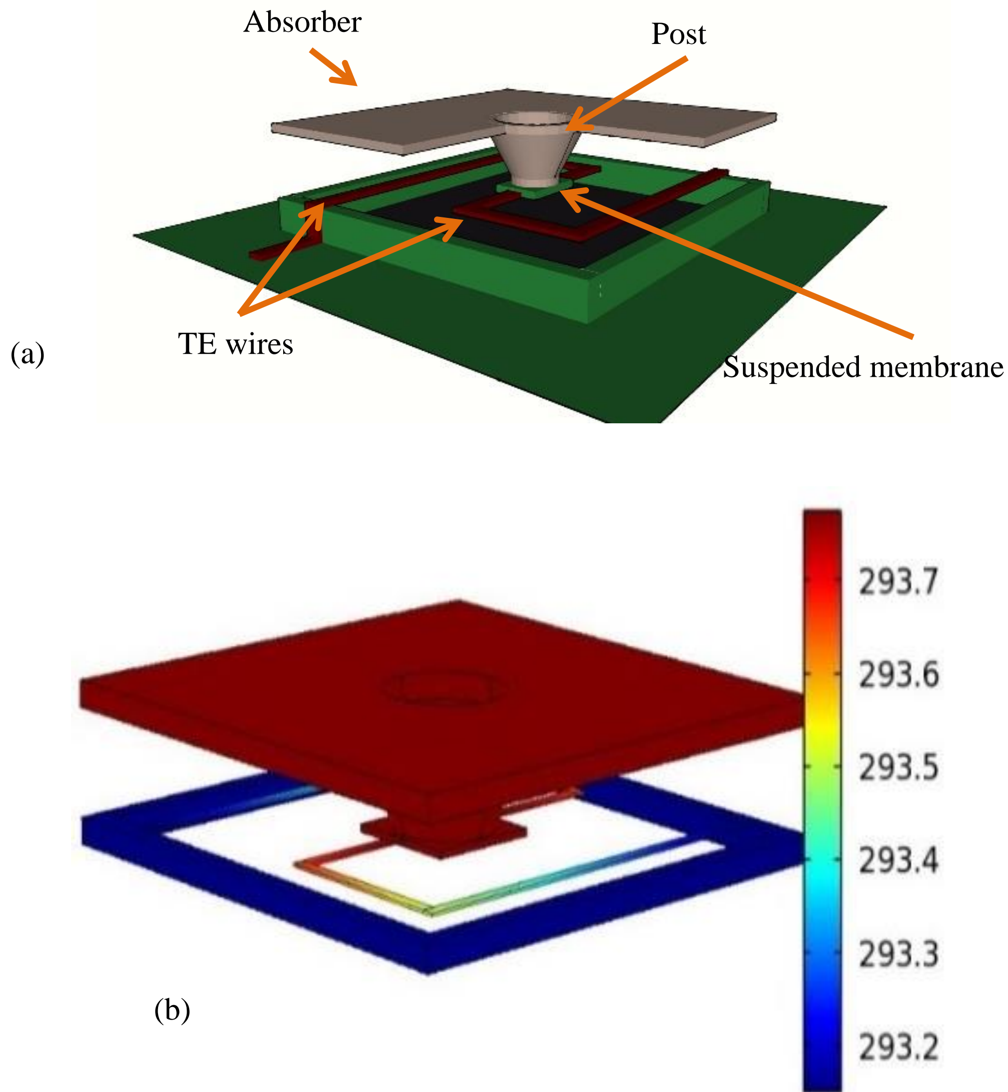


Figure 7. (a) Side view of the detector, (b) Color coded detector structure showing temperature distribution across the detector [29]. The absorber, its post, and the suspended membrane are all at a same temperature and shown in red.

The incident radiation is absorbed by the absorber and raises its temperature. Consequently, the suspended membrane will heat up since the thermal conduction between the absorber and the suspended membrane is much greater than the thermal loss through the TE wires. For the same

reason, it can be assumed that the absorber, the post, and the suspended membrane are all at the same temperature (as shown in the simulated temperature distribution in Figure 7(b)). Thus, the temperature drop is mostly across the TE wires placed between the isolated membrane and the substrate. This temperature difference is sensed by the wires and a proportional differential signal is generated.

3.1.6 Limit of IR detection

Calculating the limit of IR detection for a technology shows how much improvement in the performance of a detector can be achieved and would let scientist to compare the different technologies together and see the potentials in them.

There are many noise sources present in a thermal detector. To name a few: shot noise, generation recombination noise, Johnson noise, 1/f noise, temperature fluctuation noise, background noise, etc. In thermoelectric based detectors mainly Johnson noise and potentially temperature fluctuation noise are present and since the readout circuit is designed to draw minimal amount of current from the device, the other noise sources are not present.

Any noise source generates specific amount of power in a certain frequency. If the received thermal power from an object has power less than the total power of noise sources combined together then that radiation cannot be detected. Thus, the minimum thermal power that can be detected depends on how well the noise sources are limited and controlled. The so called NEP or noise equivalent power is a measure that shows how well the noise sources are controlled. The lower the NEP is the higher is the sensitivity of a thermal camera. Since some of the noise sources depend on the

device area and electronic bandwidth, specific detectivity (D^*) as defined before [54] is used to take those effect out and let scientist to measure different IR detection technologies together.

If a detector is background fluctuation noise limited, then it means that radiation is the only heat loss mechanism and the sensitivity of that detectors is given by [1,55]

$$D_{BF}^* = \sqrt{\frac{\epsilon}{8*k*\sigma(T_d^5+T_{bkg}^5)}} \tag{15}$$

Where $k, \sigma,$ and ϵ are the Boltzmann constant, Stephan Boltzmann constant and the surface emissivity respectively and T_d and T_{bkg} are detector and background temperatures respectively. Assuming that the detector is at room temperature, then D^* is $\sim 1.8 * 10^{10}$ and this is the limit for all thermal detectors. This is equal to NEP of $3 * 10^{-17}$ W/unit area.

In addition to radiation, heat transfer can impose a limit on the maximum performance of a detector. This noise is called temperature fluctuation noise and it comes from the fact that the heat transfer from the detector to the substrate fluctuates. This fluctuation in the heat transfer introduces noise in temperature measurement. The variance in temperature measurement is shown to be [1,56]:

$$\langle \Delta T^2 \rangle = \sqrt{4 k_B T^2 R} \tag{16}$$

Where T and R are detector temperature and heat resistance from the detector to the reservoir respectively.

Finally, the most pronounced source of noise in thermoelectric IR detectors is the Johnson noise as mentioned earlier.

The following equation summarizes how D^* is defined for TE IR detectors:

$$D^* = \frac{\sqrt{A_{detector} * \Delta f}}{\sqrt{8 * k_B * A_{detector} * \sigma\left(T_d^5 + T_{bkg}^5\right)} + \sqrt{4 k_B T^2 G} + \frac{\sqrt{4 k_B T R}}{R_V}} \tag{17}$$

Where G and R are thermal conduction with the unit of watt/K and electrical resistivity of the detector respectively. All other parameters are the same as defined earlier. The first and the second term from the left in the denominator are NEPs due to thermal radiation and temperature fluctuation noise. The last term is NEP due to Johnson noise.

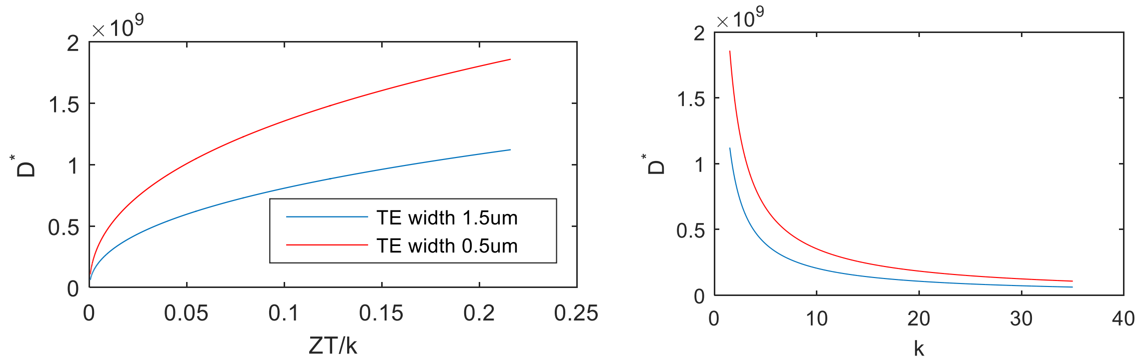


Figure 8. Left shows how specific detectivity changes with ZT/k for a realistic detector. The two lines show how changing the wire width can affect the D^*. Right graph presents the same information but it is plotted vs Thermal conductivity.

For a square detector with a width of 21um and with thermoelectric wires with the dimension of 115nm X 1.5um and Seebeck value and electrical resistivity of 180uv/K and 20 µOhm [57], the limit of D* is shown in Figure 8:

3.2 FEM simulation

Finite element method (FEM) is utilized to predict the detector's performance. The detector is comprised of an absorber on top, an absorber post made of the same material as the absorber and connected to the suspended membrane, and the TE wires. The TE wires serve also as supports to suspend the structure. When the absorber is irradiated, the rise in its temperature (shown in Figure 7) causes the suspended membrane temperature to increase and because of the relatively high thermal conductance between the absorber and the suspended membrane compared to the thermal conductance between TE wires and substrate, it can be assumed that suspended membrane and the absorber are at the same temperature. It is worthwhile to evaluate the detector performance as the design parameters change.

3.2.1 Thermal simulation

A complete list of the physical dimensions and variables are presented in Table 2. According to Wien's displacement law, human body has a maximum radiation at around 10um wavelength. If the area of a human body is assumed to be $1\ \mathrm{m}^2$, by using Planck's radiation equation, the total transmitted power in the range of 8-14 um is about 170 watts. If the body is radiating isotropically and is a meter away from the detector, $13.5\,\frac{\mathrm{watt}}{\mathrm{m}^2}$ is the power density incident on the detector. This value is used for the absorber heat source.

Table 2. Parameters used in the simulation.

Parameter	Value
Pixel size	20 um * 20 um
Suspended membrane size	5 um * 5um
Suspended membrane thickness	300 nm
Absorber post height	4 um
Absorber post bottom radius	2.2 um
Absorber post inclining angle	20 degree

Parameter	Value
Absorber thickness	1 um
TE Width	Variable 100 to 1200 nm
TE thickness	115nm
Absorber absorption	80% - Flat 8-14um
Polysilicon thermal conductivity	Varied from 1 to 30 W/m.K

In this simulation, the effect of thermal radiation off of the absorber is also included. In COMSOL, Stefan-Boltzmann equation is used to take the radiation losses into account. However, in this way, all the radiated power in all wavelengths are combined which results in a number much larger than the actual value since the radiation losses should only be taken into account in the range that absorption is significant. Assuming that the absorber temperature is not deviating from its initial value by more than 2 to 3 degree, a correction coefficient is calculated from Planck's radiation equation and is multiplied to the emissivity of absorber. For an absorber with the initial temperature of 293.15 K, the correction factor is ~0.37 for 8-14 um window.

The steady state responsivity as described above is proportional to the thermal conductivity ($\text{responsivity} \propto \frac{1}{k}$). However when radiation losses are taken into account, the detector performance deviates from this simple proportional equation especially when TE wire thermal conductance is small and ultimately approaching zero.

Since the output voltage of the detector is $S * (T_{suspended\ membrane} - T_{substrate})$ for a constant radiation, the temperature of the suspended membrane is a good indicator of how different parameters are affecting the output signal. For instance, if TE thermal conductivity could be independently reduced by nano-structuring, roughening the surface, and/or introducing nano-holes, the suspended membrane temperature would be higher which translates into a larger output signal or higher responsivity. For a detector with TE width of 200 nm and a constant substrate temperature, the suspended membrane variation with thermal conductivity is shown in Figure 9 (left). Figure 9 (right) shows the error introduced when absorber radiation losses are ignored.

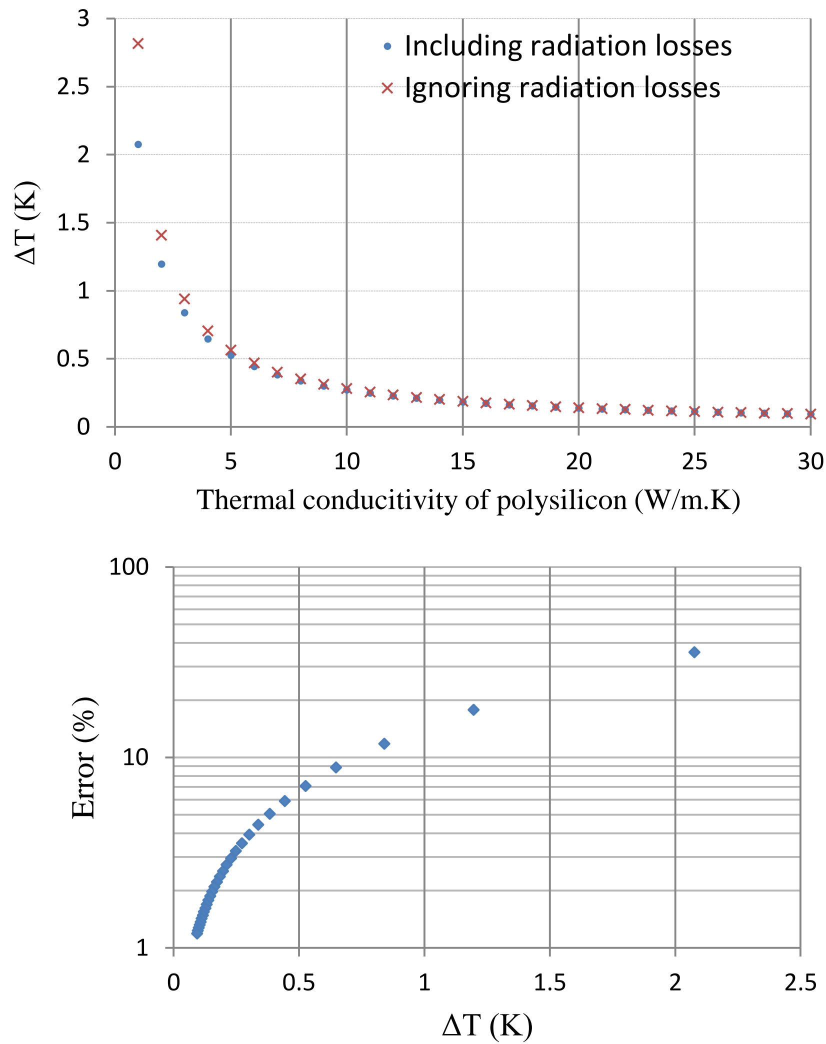


Figure 9. Left plot shows the variation of the suspended membrane temperature with respect to substrate vs. thermal conductivity of TE wires when radiation losses are included and ignored. Right plot shows the percentage of the error introduced when radiation losses are ignored as a function of the temperature difference across the TE wires.

If the material thermal conductivity is presumed to be constant, then it is useful to know the variation of the suspended membrane temperature versus the widths of the TE wires. Thickness of the TE wires is controlled at the time of the deposition and their widths can be adjusted by

lithography. The simulated increase of ΔT across the TE wires presented in Figure 10 is based on an assumption that thermal conductivity of polysilicon is 5 W/m.K.

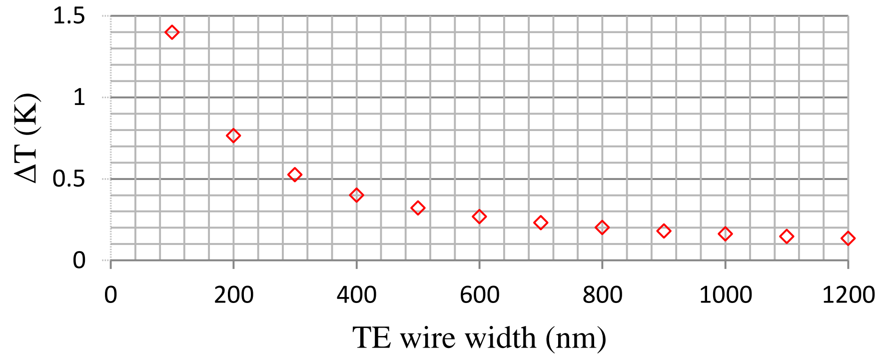


Figure 10. Temperature variation of the suspended membrane with respect to its substrate vs. the widths of the TE wires.

3.2.2 Vibration mode simulation

The longer the wires the better is the thermal isolation and the higher is the output signal. However, the long thin TE wires can compromise the structural integrity of the detector and also the resulted low natural resonance frequencies of the device can lead into the generation of unwanted signals in the output due to the piezo-resistivity effect in polysilicon [58]. Thus, the width and length of the wires should be designed in such a way that natural resonance frequencies are much higher than the detector's maximum operating frequency. Therefore, the associated harmonics can be suppressed by a low-pass filter. Finite element analysis is used to find the resonance modes in our design. The three lowest resonance frequencies for polysilicon wires with width and thickness of 500 and 100nm are 21, 23.5, and 29 kHz (from left to right in Figure 11) assuming Young's modulus of 150GPa, Poisson ratio of 0.22 and density of 2320 $\frac{\mathrm{Kg}}{\mathrm{m}^3}$ for

polysilicon. The next resonance mode has a frequency that is 10 times higher than these three modes therefore, it can be ignored.

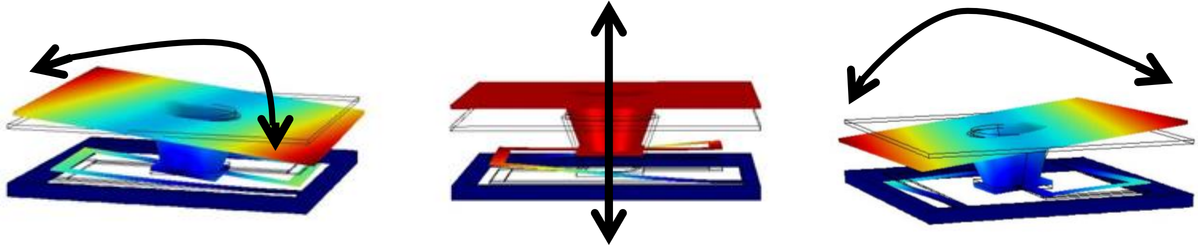


Figure 11. Color coded mode shapes of the three lowest vibrational modes; red color shows the largest displacement as opposed to dark blue areas which are fixed and have zero displacement. Black arrows are showing the direction of movement.

3.3 Fabrication

In the next few subsection, the fabrication steps of an IR detector will be discussed. Fabrication process flow will be shown next followed by describing details of each step. Supporting scanning electron microscope (SEM) images are included for ease of understanding the result of each processing step.

Additional test structures are also designed and fabricated for measuring some film properties especially for the polysilicon layer and the metallic contacts. Discussion on how these structures operate will be discussed later.

3.3.1 Process flow

Prototype devices with various absorber sizes and different number of thermocouple junctions have been fabricated using a 7-step surface-micromachining process which utilizes two sacrificial

layers and is schematically represented in Figure 12. The process outlined here is potentially CMOS-compatible due to the fact that all the material used in the fabrication are accessible in CMOS. This process begins with the deposition of a sacrificial PECVD SiO_2 layer, which is patterned to serve as the platform for the suspended heat-collector. Silicon nitride is then deposited and patterned by dry etching to serve as an insulation layer for the electrical connections on top of both the substrate and the heat absorber post in the middle (Figure 12 (a)).

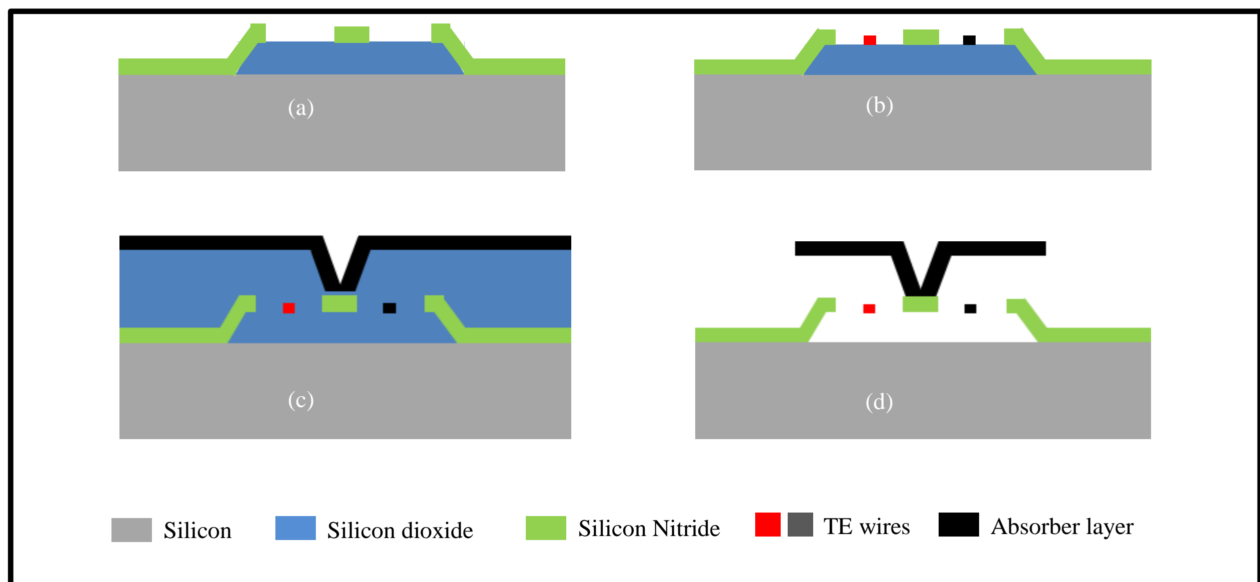


Figure 12. Process flow [59]

Next, the TE junctions are formed from a polysilicon layer deposited using Low pressure chemical vapor deposition, LPCVD, system. The absorber is then formed and patterned to create access to the bottom silicon nitride post (Figure 12 (c)). The heat-collector is then deposited/ patterned and is anchored to the post through the patterned hole in the second sacrificial layer. At last, both sacrificial layers are removed to completely release the structure (Figure 12(d)). The described steps will be detailed in the rest of this chapter.

3.3.2 Sacrificial layer

The fabrication process begins with a single side polished silicon. The wafer is cleaned prior to any deposition to make sure that it is free of any contamination. Any contamination may cause some unknown effects and undesired film formation in the later steps.

There are different choices of sacrificial layers. Polymers such as photoresist can be used as a sacrificial layer but they are not suitable for high temperature processes since may burn or reflow and change the shape or structure. Some polymers can tolerate high temperature, however, polysilicon doping requires annealing at about 950°C and, to the best of author's knowledge, there is no polymer that can survive near that range. Other sacrificial layer like silicon dioxide, silicon nitride, polysilicon, etc. can also be used but except silicon dioxide, other materials either hard to remove or their etchant attacks other material on the wafer. Silicon dioxide can be etched in Hydrofluoric solutions (HF). The HF solution slightly attacks silicon, but it strongly etches oxide which results in high etching selectivity.

After cleaning, sacrificial oxide is deposited. This can be done either in oxidation furnace or PECVD. PECVD oxide is preferable because this film will be removed later on and has higher etch rate in the etchant compared to the thermal oxide. Also the oxide deposition rate in PECVD (2 um per hour) is much higher than the growth rate in furnace (more than 8 hours for 2 um).

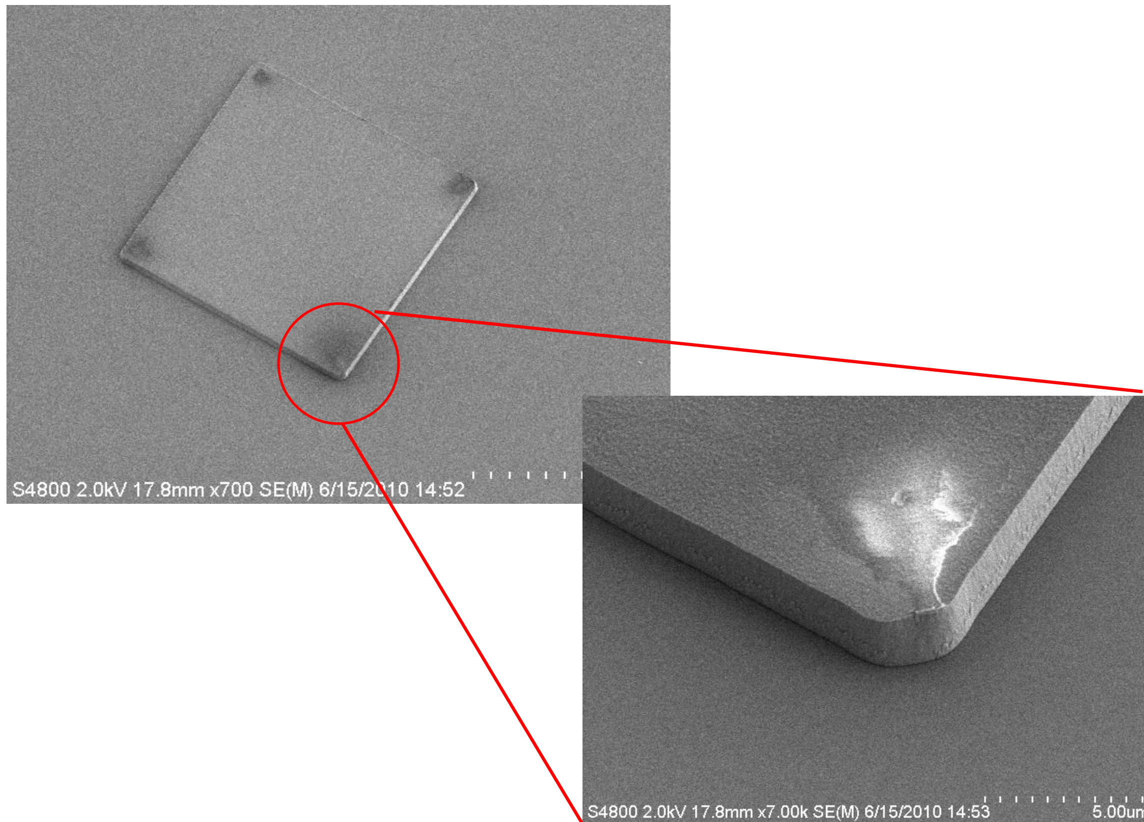


Figure 13**.** SEM showing the etched oxide step

Figure 13 shows the SEM of the oxide sacrificial layer after dry etching in ICP. It should be also noted that in ICP or any dry etching, the sidewalls are very steep. This may cause discontinuity in thermoelectric traces in future steps. To change the sidewall slopes, the mask should have sloped sidewalls. Before etching the oxide, the patterned resist is baked at $150\,°C$, above its glass transition temperature ($T_g \sim 120°C$ [60]), for 15 minutes to reflow and to get sloped sidewalls. The reflowing process works well on positive resists. The polymer in the negative resists is usually cross linked in the process of exposure and post bake and this cured polymer resist to reflow.

The sloped sidewall of the resist will be transferred to the oxide layer during ICP etching of the oxide layer (the actual slope of the sidewall will also depend on the resist to oxide etch rate ratio in the etching process which here is 1 to 2). The etch stop for this step is the silicon substrate since the selectivity of oxide over silicon in CHF_3^+ based plasma is considerably high [61].

3.3.3 Electrical insulator

Undoped silicon wafers can be very expensive and doped ones may short the thermoelectric traces to each other and cause malfunction. To avoid this, a thin layer of an insulator material should be deposited. This layer will not be removed and should not be etched in HF solution. Silicon nitride is the choice of option since it can tolerate high temperature, it is slightly attacked in HF, and it can be deposited with the common IC fabrication tools. Another requirement is that the insulator film should have high thermal conductivity to dissipate the transferred heat from the hot element quickly. Silicon nitride has high thermal conductivity [27] and can rapidly conduct any local heat to the other cold areas. Silicon nitride was chosen because it could be deposited using PECVD and has high deposition rate. Upon different parameters in the process, the deposited films may have different etch rates in HF solution [62]. A recipe was developed to produce films with low stress and low etch rate in BOE and is shown in Table 3.

Table 3. Silicon nitride deposition recipe

Temperature (C)	SiH_4 + He (sccm)	NH_3 (sccm)	He (sccm)	N_2 (sccm)	RF power (watts)	Process pressure (mTorr)
300	1600	5	1200	450	80	750

After nitride deposition, the film should be patterned to form a SiN membrane on the center of the sacrificial oxide which will act as the hot junction as shown in Figure 7.

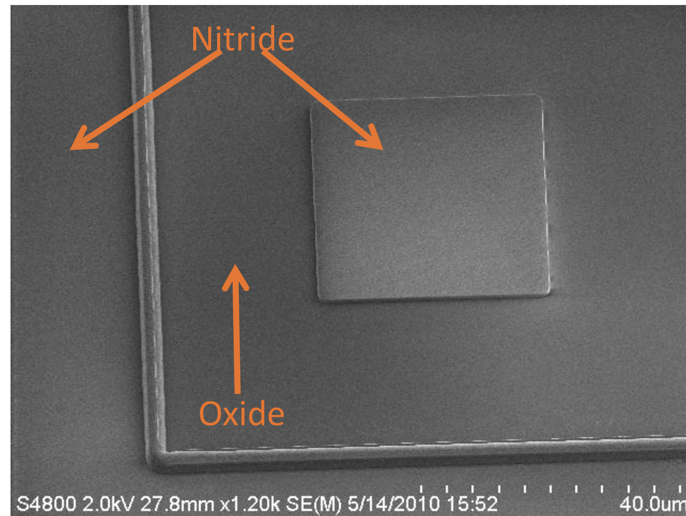


Figure 14. SEM of a device after patterning the nitride layer

For patterning the nitride, phosphoric acid should be used for the wet etching process. However, phosphoric acid attacks the photoresist and hence, photoresist cannot be used as a mask. Dry etching is another option which can be done by using the same recipe as oxide etching and since the selectivity of photoresist over nitride is 1 to 2, the photoresist can be used as the mask. The result after etching is shown in Figure 14. The next step after electrical insulator deposition (or SiN) is polysilicon deposition for the thermoelectric material. Polysilicon deposition is carried out in a furnace which requires 600°C. PECVD nitride cannot withstand that high of a temperature and cracks. Therefore, a substitution is required with thermal and chemical properties close to silicon nitride.

Aluminum nitride (AlN) has high thermal conductivity [63], high melting point, inert to the solvents and etchants and can be deposited by the sputtering method. Aluminum nitride etch-rate in its etchant which is TMAH (Tetramethylammonium hydroxide) and hydrofluoric acid (HF), strongly depends on its quality. TMAH is important because it is the solution which is used to develop (or pattern) the photoresist after the exposure. The etch rate in TMAH should be minimized to prevent undesired undercuts. Many AlN films were deposited using reactive sputtering. However, consistency in the deposition was a serious problem. Most notably was the film rocking curve FWHM (full width at half maximum) that was changing from time to time for the same deposition recipe. FWHM of the rocking curve is a good indication of the alignment between the crystallites in the films. It was observed that the higher the FWHM, the lower the etch rate in HF solution. Lengthy target cleaning process and chamber conditioning resulted in looking for alternatives.

Low stress low pressure chemical vapor deposition (LPCVD) silicon nitride deposited at $850°C$, shows low etch rate in BOE and can easily withstand high temperature processes such as polysilicon deposition. The 400nm film is patterned with positive resist, Shipley 1827, and etched using CHF3 based plasma in an ICP system. This step should be monitored and timed carefully since selectivity of nitride etching over oxide in the etcher is close to 1:1. The schematic of the patterned nitride layer on an oxide island is shown in Figure 12(a).

3.3.4 Thermoelectric wires

Thermoelectric wires are required to generate voltage due to the temperature difference on their ends. As described earlier, polysilicon is chosen due to its unique properties. One of them is the ease in deposition and patterning.

Polysilicon TE wires are deposited at this step as shown in Figure 12(b). The first p-type TE wire is a 115nm LPCVD polysilicon deposited at $630\ °C$ and is in-situ boron doped. The grain size and crystalline structure of the film should be controlled at this step [36,64] and the subsequent annealing steps [65]. Then a 150nm PECVD oxide is deposited on the polysilicon layer as a hard mask for patterning. This hard mask is kept during the second polysilicon layer deposition to prevent counter dopants from entering the p-type wire and also to avoid the out-diffusion of p-dopants from the TE wire. The hard mask is patterned using a positive resist and etched using dry etching techniques. Then, the photoresist is removed in acetone and the remaining of the polysilicon layer is etched in SF6 based plasma. The second in-situ doped polysilicon layer is deposited next and patterned using positive resist and SF6 plasma. At this point, the two TE wires are patterned and the widths of the wires can be adjusted by isotropic over-etching of the wires and achieving the desired undercut.

After removing the resist and cleaning the wafer using an O_2 plasma, dopant activation annealing at $950°C$ is carried out for 30 minutes in a nitrogen environment.

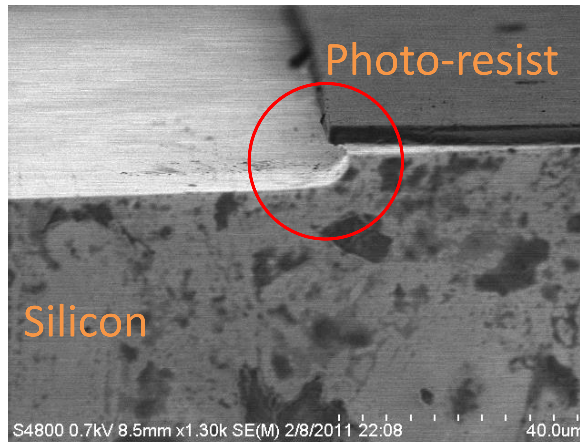
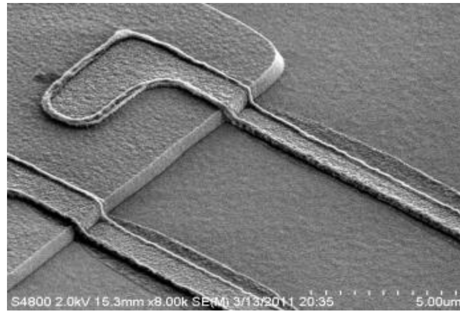
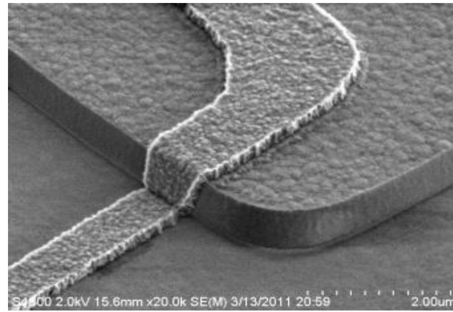


Figure 15. SEM showing etched silicon and the formed undercut underneath the photoresist mask

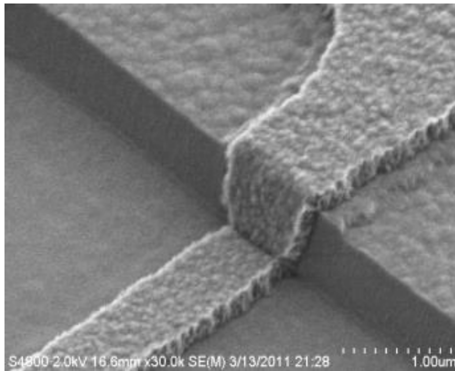
To achieve the desired undercut and not etching the rest of the exposed substrate, a recipe based on SF6 plasma was developed to have high etching selectivity of silicon over silicon dioxide. In the developed recipe the etch-rates of photoresist, silicon dioxide and polysilicon are 85, 43, and >1000 nm/min respectively. The undercut can be clearly seen in Figure 15. This method was used to create wires with different widths and the fabricated wires are shown in Figure 16.



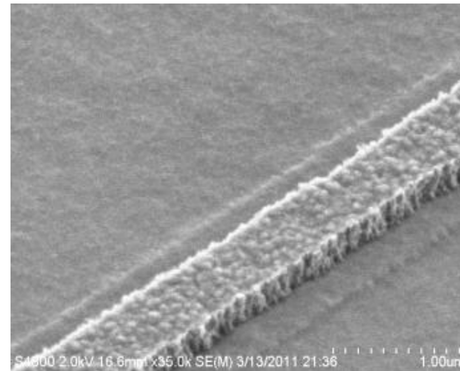
A) Polysilicon wires after etching for 15 seconds



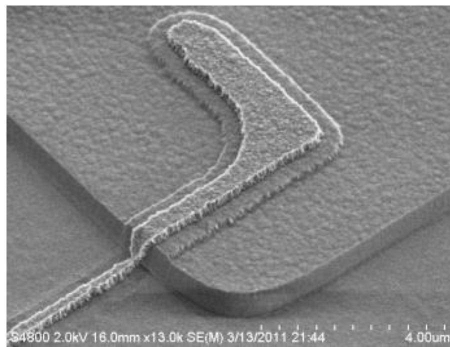
B) Polysilicon wires after etching for 35 seconds



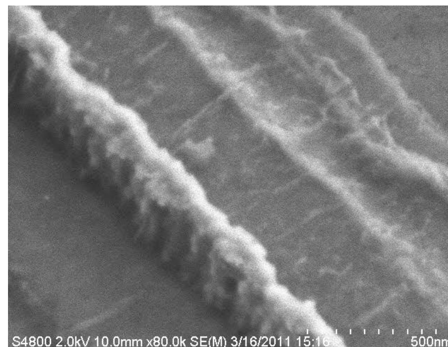
C) Polysilicon wires after etching for 60 seconds



D) Polysilicon wires after etching for 80 seconds



E) Polysilicon wires after etching for 100 seconds



F) Polysilicon wires after etching for 120 seconds

Figure 16 - SEMs of the fabricated wires showing the wire width reduction versus time etching time

The described technique was used to fabricate a complete device and it is shown in Figure 17.

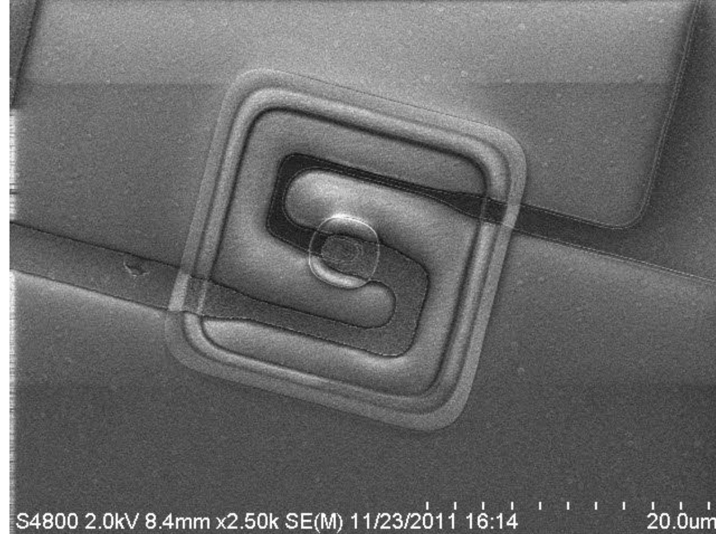


Figure 17. Top view SEM image showing the etched polysilicon wires

The only problem that was observed with this technique was that etch rate of highly doped polysilicon phosphorous is much higher than the boron doped wires. [66] This non-uniform etching can be taken care of by changing the wire patterns. A different approach of patterning undoped wires and then doping them using dopant diffusion sources was also utilized to achieve more uniform wire sizes. For this approach, the deposition order of the layers changed as follows. Electrical insulator, the silicon nitride layer, was deposited first followed by the deposition of PECVD silicon dioxide. Then an undoped polysilicon layer with the desired thickness was deposited next. At this point, the surface of the wafer is completely flat and has low roughness. E-beam lithography was used to create the patterns for the wire as shown in Figure 18.

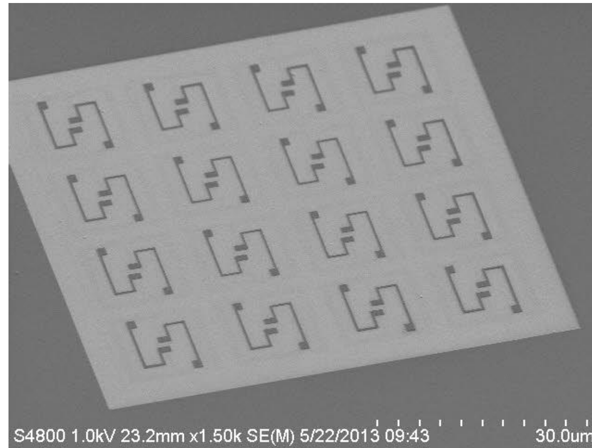


Figure 18. SEM image showing patterned wires using E-beam lithography.

To dope the wires, one of the wires was covered with a layer of PECVD oxide and the other layer was exposed to a diffusion dopant source at high temperature of about 1100°C. Then, the previous silicon dioxide mask was removed and a new mask was used for the other wire to be doped with the counter type of dopant. The sacrificial oxide layer under the wires can be etched to form the islands at this step. The SEM image showing the doped wires on the etched silicon dioxide island is shown in Figure 19.

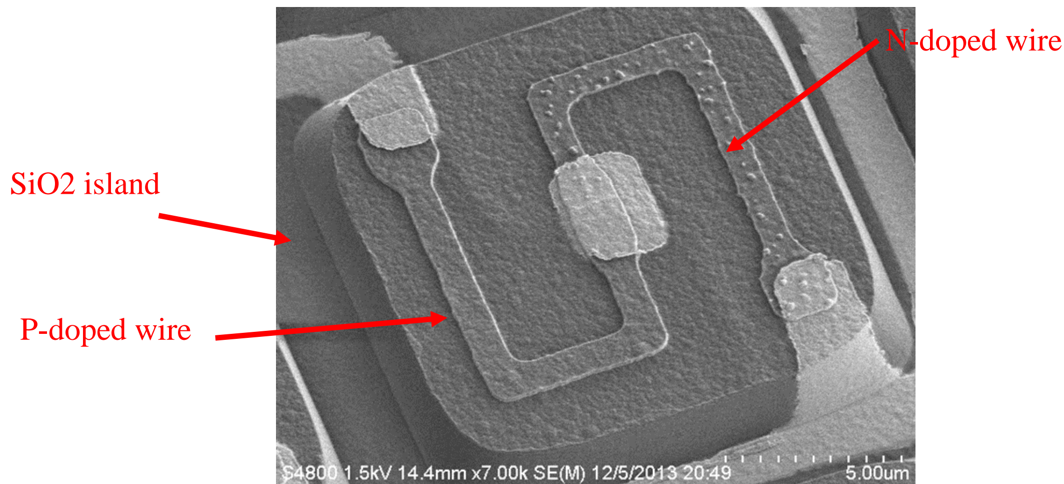


Figure 19. A SEM showing the etched wires on an oxide island

3.3.5 Electrical contact

Interconnections and metallic contacts are an important part of MEMS devices. In thermoelectric infrared detectors, the TE wires are made of n-type and p-type polysilicon and the ability to have low contact resistance to these wires are crucial for high performance detectors. To reduce contact resistance, polysilicon wires need to be highly doped. To further more reduce this undesirable resistance, silicides can be used. Silicides have low resistance, easy to process and have negligible electromigration. Among silicides, nickel silicide requires low thermal budget for preparation. It has very low film resistivity compared to other silicide and is stable up to 600°C [67,69].

TLM (Transfer length method) technique is used to accurately measure the contact resistance. The formation of desirable phase of Nickel silicide (NiSi which has the lowest resistance) occurs at a temperature range of 400 to 600C. The TLM technique can be used to find the effect of different parameters such as annealing temperature, duration of annealing, metal film thickness, etc. on

contact resistance. Figure 20 shows scanning electron microscopy images from the fabricated devices. Nickel silicide changes phases depending on the temperature it is annealed at. At about 250-300°C the Ni_2Si phase is formed [68] which can be used to help make the next phase. The NiSi phase forms at about 400-600°C and is the phase with the lowest resistance [69]. After about 600°C the high resistivity $NiSi_2$ phase begins to form.

To measure contact resistance, resistance of different polysilicon lengths are measured and plotted in a graph. The measured resistances are the sum of two terms:

$$R_{measured} = R_{polysilicon}(l) + 2 * R_{contact\ resistance} \tag{1}$$

The intersection of plotted line with zero length axis will be the second term of the above equation.

A Nickel film of about 86 nm thick was sputtered on 170nm boron-doped polysilicon with a sheet resistance of $580\frac{Ohm}{\square}$ and then annealed at 550 C for 5 minutes.

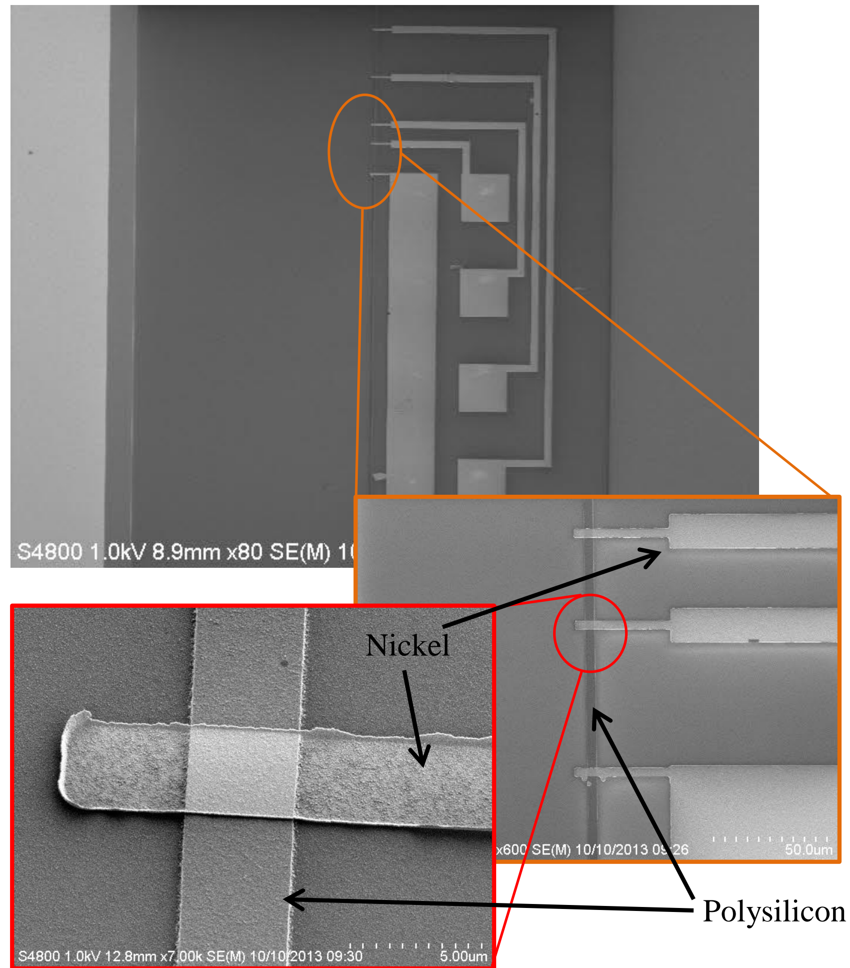


Figure 20. SEM showing the fabricated device based on TLM method for measuring the contact resistance to polysilicon

Figure 21 shows the measured data and the extracted contact resistance for a nickel film on polysilicon without annealing. The contact area is about $4um * 4um$. Figure 22 shows the measured result after annealing for 5mintues at 550C. The contact resistance, on average, is about 242 Ohm which results in 33% reduction in the contact resistance.

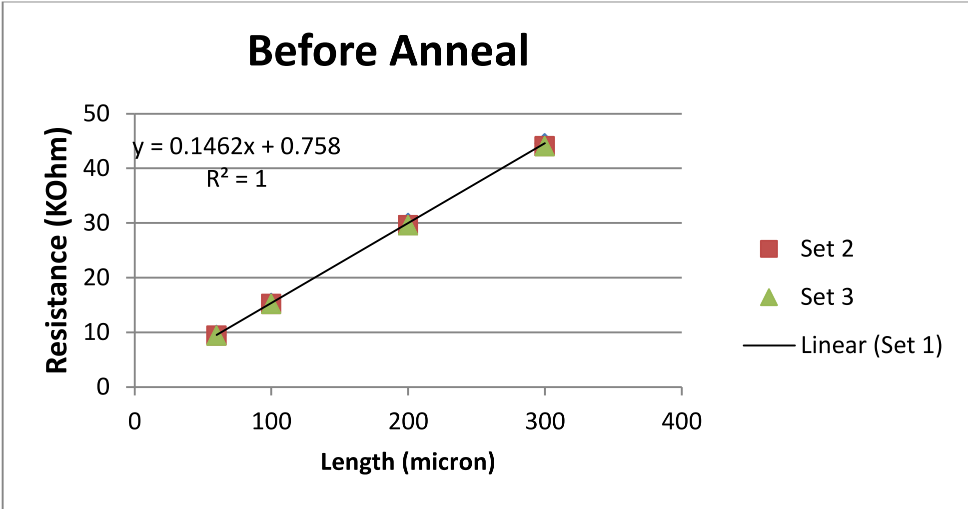


Figure 21. Shows the measured resistances vs length along with the equation that fits data. As shown above, on average the contact resistance before annealing is about 364 Ohm.

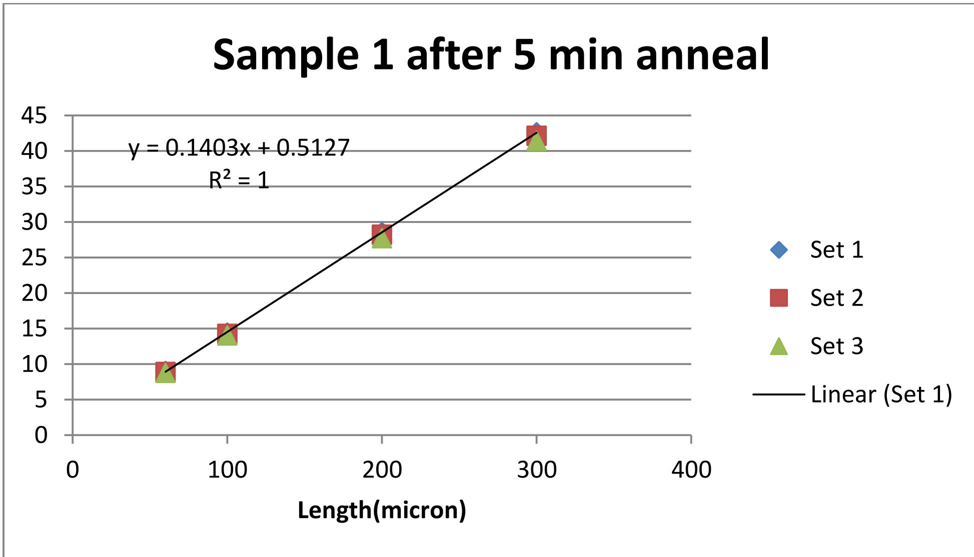


Figure 22. shows the contact resistance of some devices after annealing at 550C for 5mintues. As shown the contact resistance of the silicide is ~242 Ohm.

On some of the detectors where the polysilicon film was highly doped, laying down a metallic film on the polysilicon has low contact resistance as making a silicide. The metal layer has to be resistant to HF acid and it has to be stable on silicon and polysilicon up to $400°C$, while it also has to have electrochemical potential close to that of polysilicon in order to minimize galvanic corrosion [70] during the release step. Galvanic corrosion can also be controlled by adjusting the area of polysilicon to metal ratio. For highly doped samples, 150nm of tungsten was sputtered as the contact material using an AJA sputtering system. To improve the tungsten layer's adhesion to the silicon nitride substrate, 10nm thick film of Cr was pre-sputtered beforehand. Figure 23 shows a 4x4 array of TE detectors after depositing the metallic contacts.

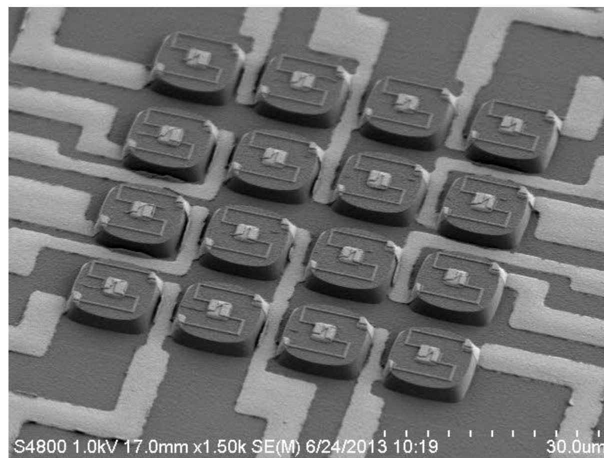


Figure 23. SEM image showing a 4x4 array of TE detectors after contact metal deposition step.

3.3.6 Parylene deposition

Parylene film is used to support the thin polysilicon layer wires during the wet release step. It will be removed at the very final step of cleaning the device in an O_2 based plasma. Parylene is

deposited at room temperatures with Specialty Coating Systems (SCS) tool. The thickness of the result film depends on the amount of the loaded dimer. Parylene-C with different thicknesses were deposited and patterned. Oxygen based plasma is used to etch the Parylene film in ICP. Since photoresist is a polymer as well as Parylene, it cannot be used as a mask. Even if the thickness of the photoresist mask is chosen much thicker than the thickness of the Parylene film, the etched film result will not have sharp and straight sidewalls. A hard mask such as silicon dioxide is required. The fabrication result after patterning the Parylene film is shown in Figure 24.

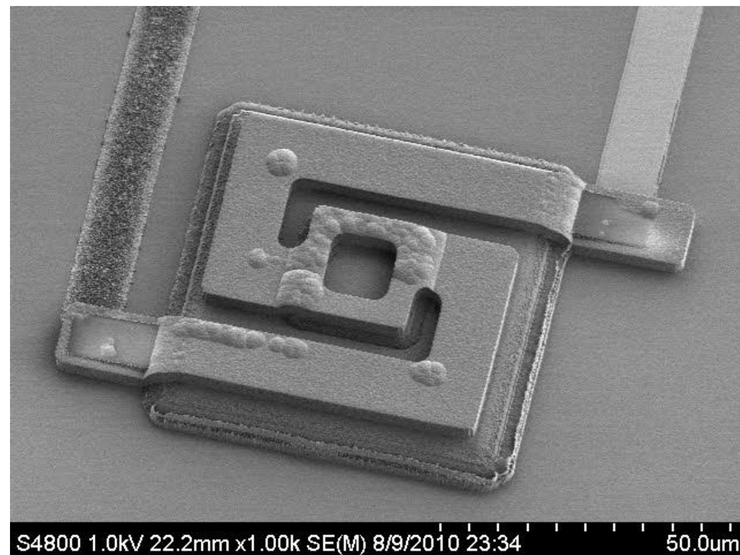


Figure 24. Top-view of a device after etching Parylene

The next step in the fabrication process is absorber deposition. Since the absorber may be deposited at high temperature, higher than 300°C, parylene C is not proper because its melting point is 290°C [71]. Parylene N has almost the same characteristic but it has higher melting point, 490°C [71]. Thus, Parylene N films were deposited by acquiring the necessary dimer and applying required .modifications to the tool.

3.3.7 Thermal absorber

To deposit the absorber, 4um PECVD silicon dioxide used as a sacrificial layer should be deposited first. To form the absorber post, the oxide layer is patterned and etched using a thick positive resist in an ICP system. Prior to etching, the positive resist is baked above its glass transition temperature to reflow and to create sloped sidewalls same as the first sacrificial etching step.

After formation of the absorber post, the patterned resist is removed in acetone followed by cleaning in oxygen plasma for organic residue removal. Then the first layer of the absorber, nichrome, is sputtered followed by the deposition of the dielectric layer, silicon nitride, in PECVD. The top metal layer which is another layer of nichrome is sputtered next. A thin layer of PECVD silicon nitride may be deposited prior to the first metal layer sputtering to improve the adhesion of the absorber post to the underlying membrane on the wafer. The thickness of the different layers in the absorber is summarized in Table 4.

Table 4. Absorber layers with their specs

Layers name	Material	Thickness
Bottom adhesion layer	Silicon nitride	100-200nm
Bottom metal layer	Nichrome	30-50nm
Dielectric layer	Silicon nitride	~1 um
Top metal layer	Nichrome	2.5-5nm

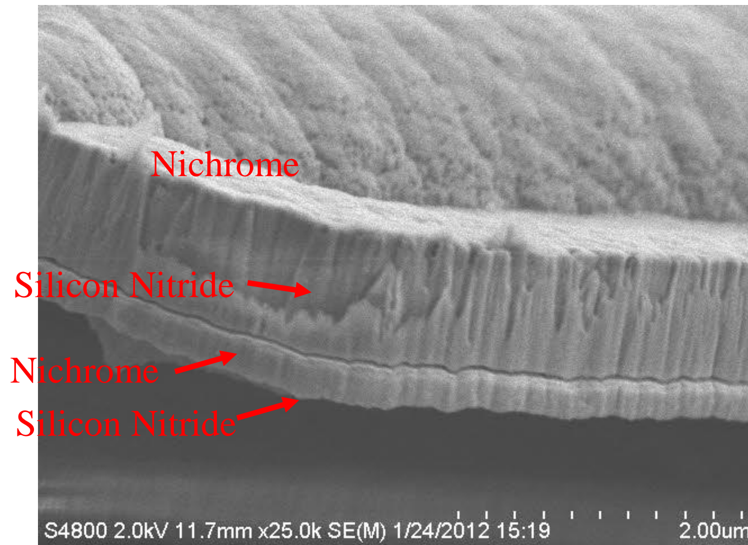


Figure 25. SEM image showing the side of a thermal absorber

Nichrome TFN etchant (Transene, Danvers, MA) along with a PR mask was used to etch the top nichrome layer and pattern the absorber. This solution has minimal effect on the exposed silicon nitride layer and that layer can be used as an etch stop layer. After etching the top nichrome, the PECVD silicon nitride is etched in an ICP etcher using CHF_3^+ based plasma. The etch stop for this layer is the bottom nichrome layer which has close to zero etch rate in the aforementioned plasma. The bottom nichrome layer is etched in the same way as the top metal and the etch stop for this etching is the sacrificial oxide layer.

3.3.8 Releasing the detectors

In this step the final goal is to completely suspend the detectors over the substrate by removing the sacrificial silicon dioxide layers in HF solutions. Based on the detector size and design, different approaches may be used to release them from substrate. The main difficulty in this step comes from the fact that when a polar molecule like water is evaporating or removed from an area

between two surfaces, the liquid surface tension forces the two surfaces to move towards each other and stick together [72]. Figure 26 shows two SEM images of two partially released detectors. On the left, the detector that had 4 arms could survive this step, however, the detector on the right with only two long arms failed to hold its integrity. It can be seen that at least one of the arms is stuck to the substrate.

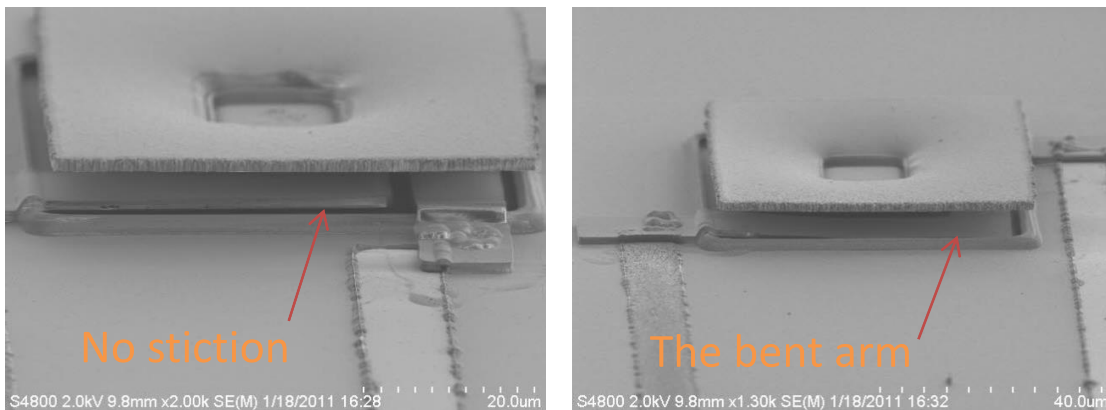


Figure 26. SEM images showing the effect of stiction on the supporting arms

Different releasing approaches were utilized. At first, using only HF in the vapor phase was applied to the sacrificial layer. To produce HF vapor, N_2 is bubbled through liquid HF. The HF vapor along with water vapor with N_2 carrier is passed through a chamber where the wafer is placed. The HF vapor etches the silicon dioxide, and the byproducts and the remaining gases are pushed to another chamber, neutralization chamber, in order to consume the remaining HF vapor before releasing to the pump.

Excessive water vapor in the processing chamber may cause condensation on the wafer surface which results in stiction. To reduce condensation, the wafer should be heated. However, Silicon dioxide etching requires water vapor to initiate. Thus, the etch rate depends on water vapor

concentration on the wafer surface. The higher the temperature the lower is the etch rate. Thus, the substrate temperature should be carefully controlled to have high etch rate while having no condensation [73,74].

The negative side HF vapor etching is that the etched oxide leaves a residue known as Cryptohalite (identified by using x-ray diffraction technique as shown in Figure 27) due to nitrogen impurities in the PECVD deposited film.

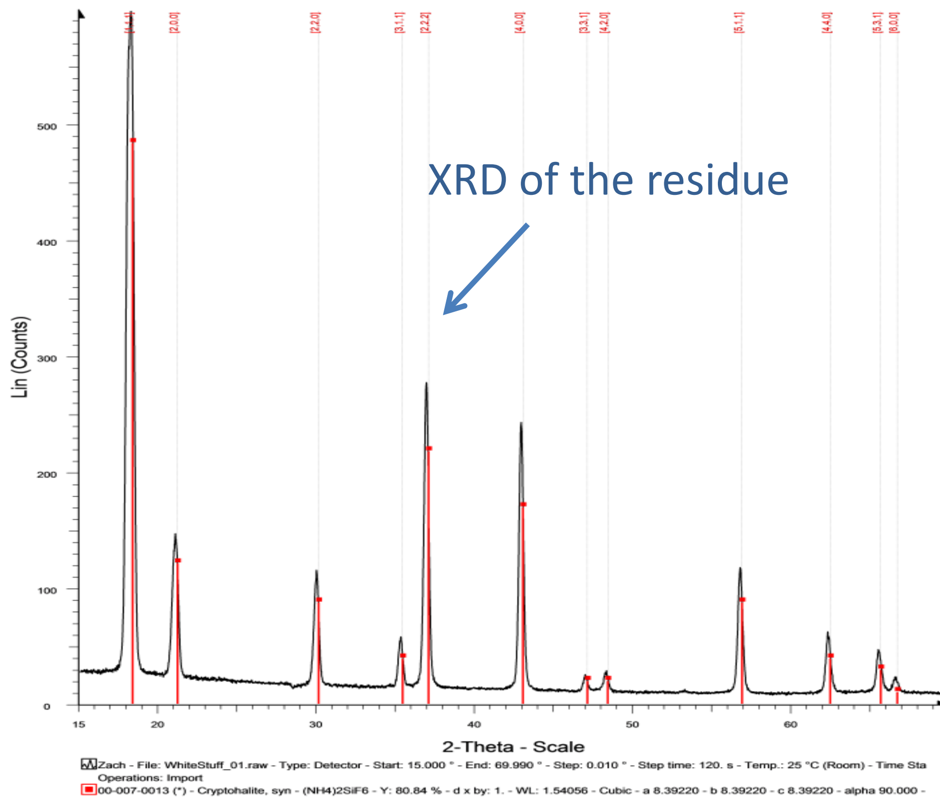


Figure 27. X-Ray diffraction pattern of the residue created during PECVD oxide etching using HF vapor

This residue can be removed by heating the substrate above 100°C [75]. However, all of the solid phases of Cryptohalite have lower density [76] than silicon dioxide and the resulted

expansion during the etching causes the detector to deform and break as shown in Figure 28. This residue is only created for PECVD deposited silicon dioxide and not for thermally grown oxide. However, the etch rate of thermally grown oxide in HF vapor is much slower than PECVD oxide and this prolonged exposure to HF vapor negatively affects the silicon nitride layers on the absorber and the wafer.

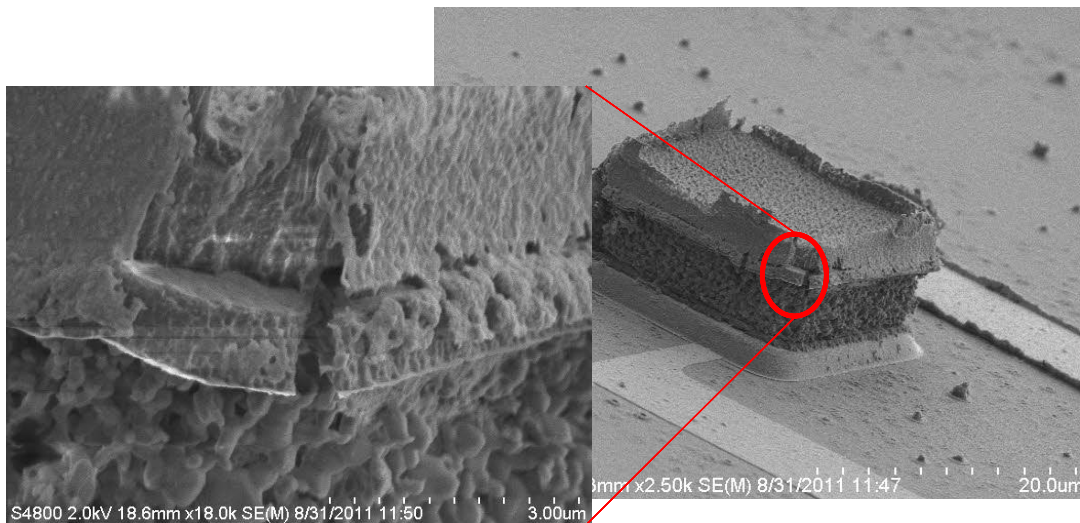


Figure 28. SEMS showing a crack on a protected absorber

Another technique to release a detector without stiction is to etch a wafer from the backside. One way is Bosch process or DRIE (deep reactive ion etching) which results to steep side walls. The other way is anisotropically wet etching with KOH or TMAH. For this process, larger holes on the backside are required. Both of the techniques were pursued to release the devices.

After completing a process on the wafer, the front side was protected with 2 um of PECVD oxide for wet etching the backside. After an hour of etching in TMAH, it was observed that the front side has been attacked and the polysilicon wires were wiped off the front surface. Another

protective layer, Protek, was added to the front side. Figure 29 shows a SEM from a device etched from the back in TMAH. The front side is released later using HF solution for 5minutes.

As it is evident in Figure 29 since the TMAH etching of silicon is anisotropic meaning that the etch rate is not equal in different planes, the right size of the backside hole should be used. TMAH etch rate on the silicon (111) plane is very low [77]. Since the wafer thicknesses might vary from one to another, the whole size should be changed or wafers with constant thickness should be used. Moreover, due to backside misalignment, larger holes are required. As a result a detector on a silicon nitride membrane is created which is prone to crack and is difficult to probe. This approach is not appropriate for fabricating arrays. As described earlier, another way of backside etching is Bosch process (Deep reactive ion etching or DRIE). The result is shown in Figure 30.

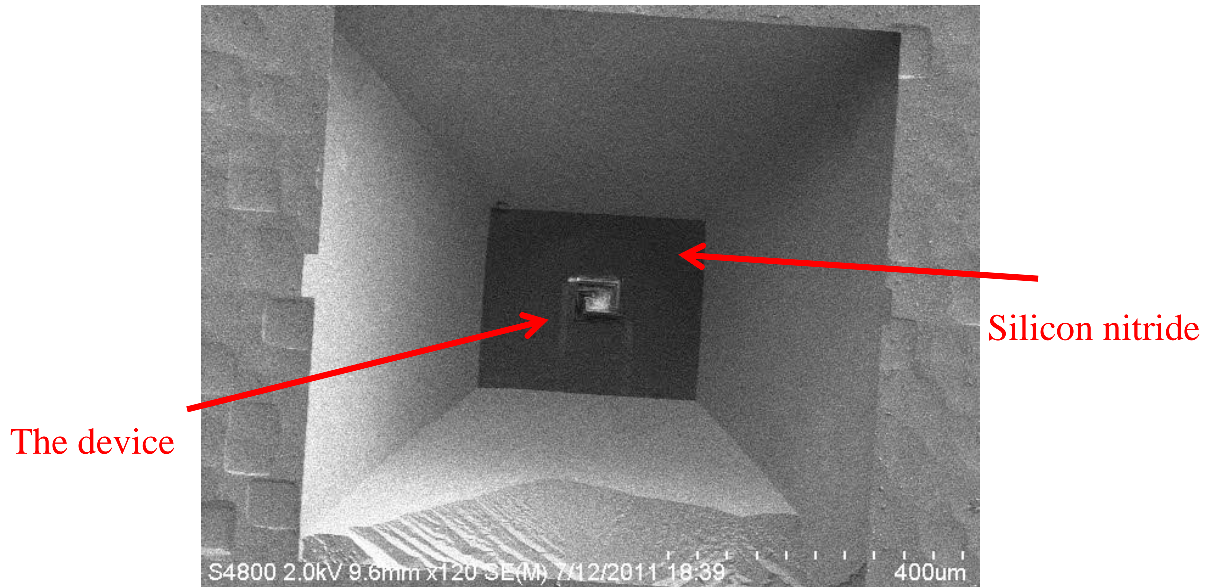


Figure 29. A SEM from a device (backside view)

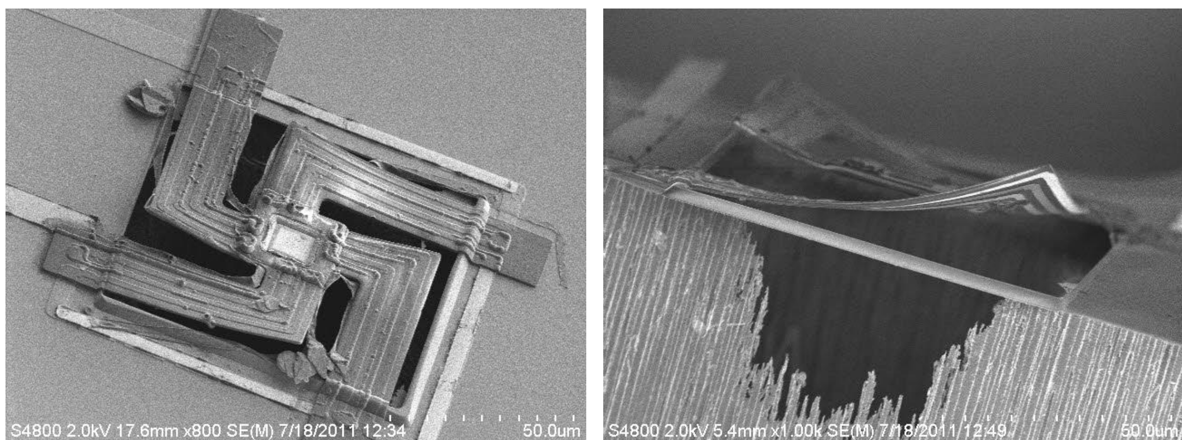


Figure 30. SEM showing the released devices from the back, top view (left) and side view (right)

As it can be seen in the above SEMs, none of the absorber could survive the submerging in HF step due to physical failure of the absorber.

One thing to note is that the parylene arms are also bent upwards. When the Parylene film goes under heat cycles, an internal stress will be induced. The author believes that the film eases the

internal stress at the annealing temperature and the induced stress is the result of thermal coefficient mismatch between the Parylene film and the underneath layer [78]. It has been shown that at first, the deposited Parylene has tensile stress, but after a heat cycle, the stress will become compressive. Specifically, Parylene N goes under phase change at 250°C and 270°C which these phase changes will reduce the internal stress. To further lessen this stress, in any heat cycle, the sample should be slowly cooled down [79]. This induced stress is the result of thermal mismatch between the Parylene film and the underneath layer [80].

To overcome this arm bending problem, the size of the detectors were reduced to 20 um * 20 um. In addition, to understand the effect of the film stress, two devices were prepared with two different conditions. One of the devices was baked and then released in HF vapor and then the other one went through the same steps but in reverse order. The result is shown in Figure 33.

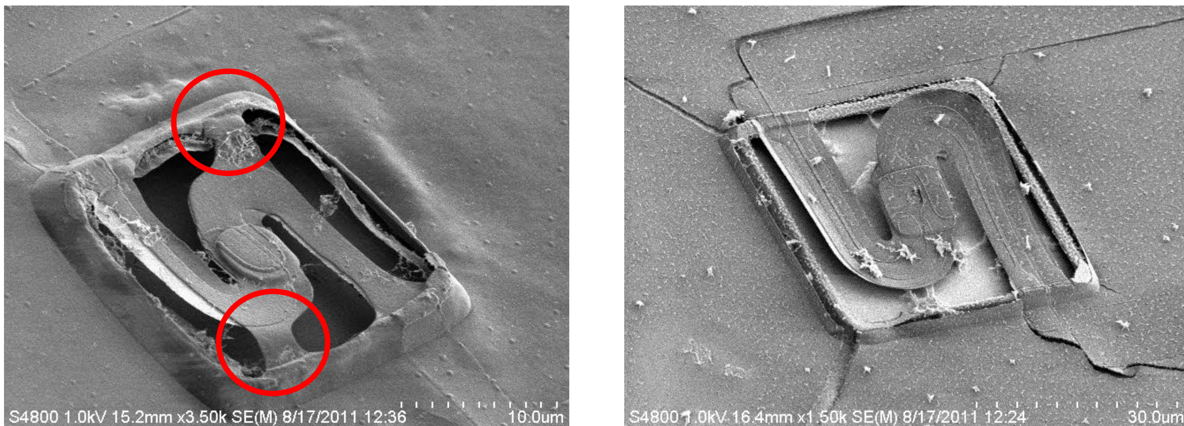


Figure 31. The SEM on the right shows a device baked at 300°C for 5 hours and then released and the SEM on the left shows another device released in HF vapor and then baked under same condition as the previous one

The above result completely supports the described reason regarding the stress generation inside

the film. The one that is baked and then released cracked due to high tensile stress. This stress was generated due to thermal coefficient mismatch between Parylene and silicon dioxide and silicon nitride. Silicon nitride is the bottom layer on the substrate and the silicon dioxide is the layer on top of the Parylene film which was used for patterning the film. Since the generation of stress inside the Parylene film is inevitable, two small supports were added to the Parylene film to hold the arms down. Those supports are shown in Figure 31 and circled in red.

At the end, the best method for releasing these devices was developed to be a combination of wet and dry etching techniques respectively. Wet etching is timed in a way that the entire top and most of the bottom sacrificial oxide layers are etched away. A small remaining oxide in the middle of the device supports the structure against stiction and will be etched away in HF vapor as shown in Figure 32.

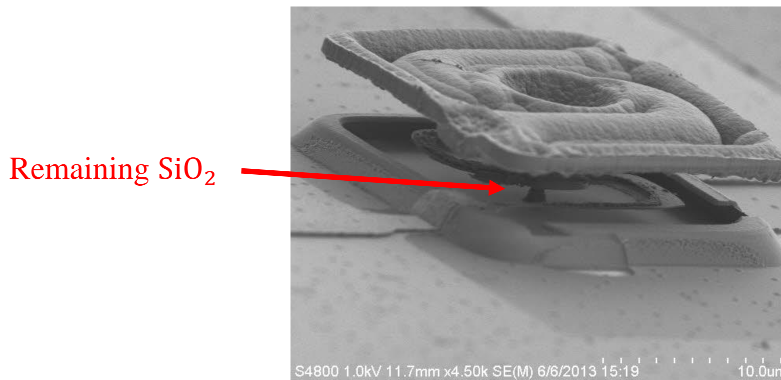


Figure 32. SEM image showing the small remaining silicon dioxide under the silicon nitride membrane

At this point the created residue (Cryptohalite) can expand from the sides without destroying the detector and can be removed upon heating at $120°C$ on a hot plate. As mentioned earlier, the

supporting parylene layer should be removed at this final step in an oxygen based plasma. A SEM of a completely fabricated detector is shown in Figure 33.

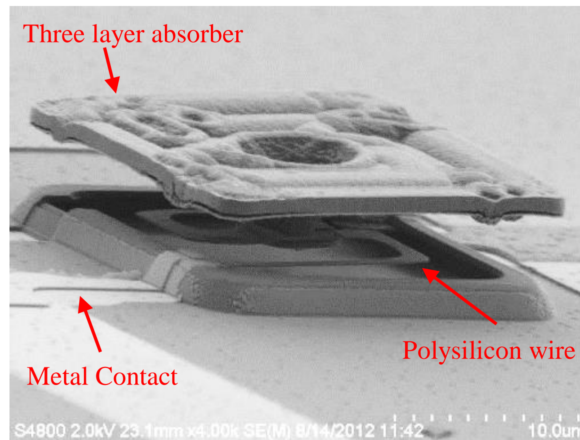


Figure 33. SEM of a completely released device [59]

3.4 Measurement results

To characterize the performance of the fabricated detectors, a number of quantities such as output noise, responsivity, and thermal time constant should be measured. This requires a special measurement setup which will be discussed in the next section. To measure effective Seebeck coefficient and thermal conduction of the detector to the substrate, the technique described by Mc Foote [10] was utilized. Once electrical and optical responsivities are measured, many of the detector parameters can be calculated. The procedure of characterizing a detector performance is described in measurement result section. The summary of the measurement results will be discussed at the end of this section.

As a result of this work, the highest reported responsivity for a 20um by 20 um thermoelectric detector is achieved (to the best of author's knowledge).

3.4.1 Measurement setup

The schematic of the test setup is shown in Figure 34. The detector is placed inside a vacuum chamber to reduce convection and conduction losses through atmosphere. On top of the chamber is a view port that allows infrared rays to enter the chamber. Thus, the view port should be IR transparent but preferably opaque to visible light. This is desired to prevent any photoelectric effect induced output voltages. A germanium window with proper antireflection coating suits for this application the best [81].

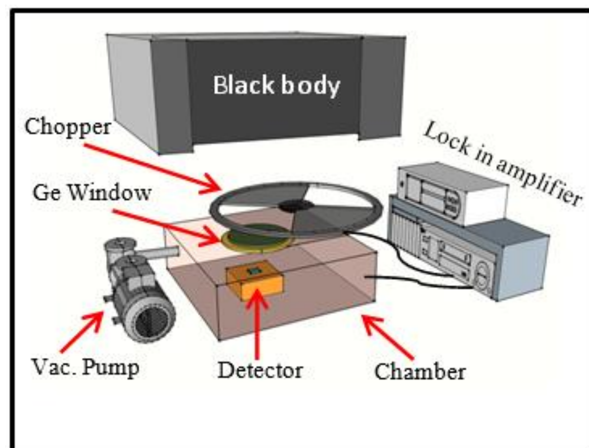


Figure 34. Schematic of the measurement setup. The black body source is on top of the vacuum chamber and is radiating down towards the germanium window. The chopper is placed between the black body and the germanium window and is connected to the lock in amplifier.

To evaluate the performance of a detector to heat, an infrared source is required. A blackbody can be used for this purpose. A blackbody has the emissivity of about 1 and based on its surface temperature can generate different flux of infrared radiation. For the purpose of lab measurement, the blackbody temperature was set to 500 K.

The detector produced voltage can be measured using a DC volt meter. However, the weak signal may be buried inside noise. Lock-in-amplifier technique is utilized for more accurate measurement. Using this technique, the measurement bandwidth is substantially reduced and would result in higher signal to noise ratio. To realize this, an optical chopper is placed right on top of the view port. Thus, IR radiation from the blackbody source has to propagate through the chopper and the electrical signal proportional to the radiation can be measured. The chopper frequency is controlled by the lock in amplifier.

3.4.2 Measurement result

In this section, measurement procedure for an IR detector will be discussed. The result of the measurements are summarized in each section.

3.4.2.1 Optical Responsivity

At first, a detector is placed inside a vacuum chamber (pressure less than 10mtorr [82]) to avoid convection losses. Then the detector output voltage is recorded while a large area black body at 500 K is radiating towards the chamber as depicted in Figure 34. The incoming radiation is chopped at a controllable frequency. A lock in amplifier is then used to extract the signal from the detector output. The advantage of using a lock in amplifier is that only a small bandwidth of noise (less than 0.1 Hz depending on the lock in amplifier) is integrated into the output. Therefore, a very weak signal of even few nano volts can be measured. To get the largest signal to noise ratio, the chamber pressure should be controlled to avoid performance loss due to undesired heat convection. Figure 36 shows how the rise of chamber pressure adversely affects the detector's responsivity. A typical waveform from a detector is shown in Figure 39. Knowing the irradiance,

responsivity can be calculated by simply dividing the detector's output voltage by the input power (The unit of responsivity is volt/watt). Irradiance or the input power can be found by substituting a NIST calibrated sensor for the fabricated detector and recording its output signal. The fabricated detectors have a responsivity of around 1800 v/w.

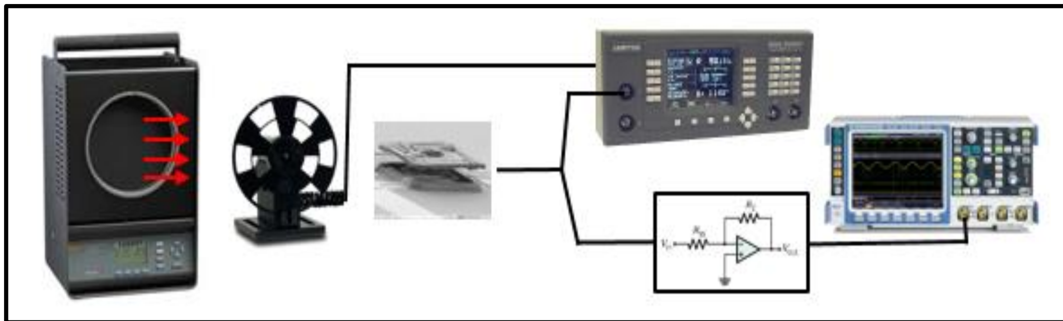


Figure 35. Measurement setup showing the blackbody, optical chopper, TE detector, lock-in-amplifier, amplifier and oscilloscope from left to right.

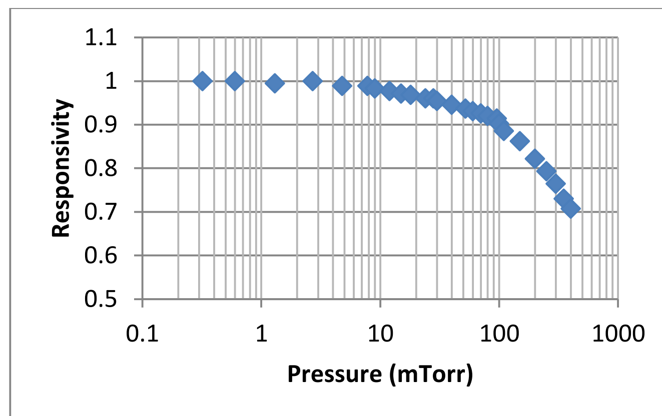


Figure 36. Showing how increase in the chamber pressure (conduction and convection losses) adversely affects the responsivity of a detector

3.4.2.2 Electrical Responsivity, Seebeck, and Thermal Conduction

To measure Seebeck coefficient, the circuit shown in Figure 37 is used. If a DC current is passed throught a detector, two phenomenon happen inside the detector simultaneously, joule heating and peltier cooling/heating. Joule heating happens because the TE wires are resistive and passing current would result in heat generation. Peltier cooling/heating, the 2nd phenomenon, happens right where TE wires are connected to each other on the membrane. (The latter phenomenon also happen on the substrate but that is not of interest.) Depending on the direction of the current, heat can be generated or absorbed at the junction.

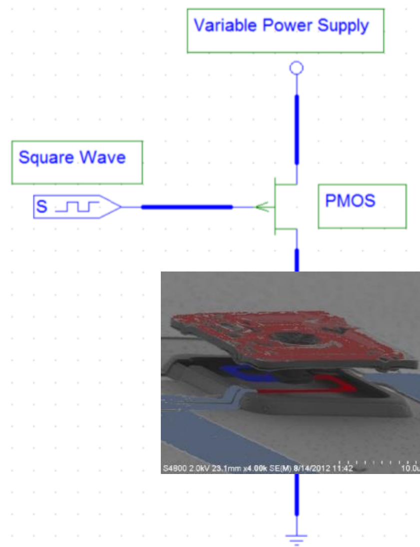


Figure 37. Schematic of the circuit used for extracting electrical paramteters

The heat generation inside the detector is:

$$\text{Heat} = \frac{\text{IV}}{2} - \text{I} * \text{S} * \text{T} \tag{18}$$

Where I, V, S and T are current passed through the detector, voltage across the detector, Seebeck coefficient and temperature respectively. The first term on the right hand side is showing the joule heating part and second term is peltier cooling. At very low current the peltier cooling is dominant effect. However, at higher currents, the joule heating becomes dominant.

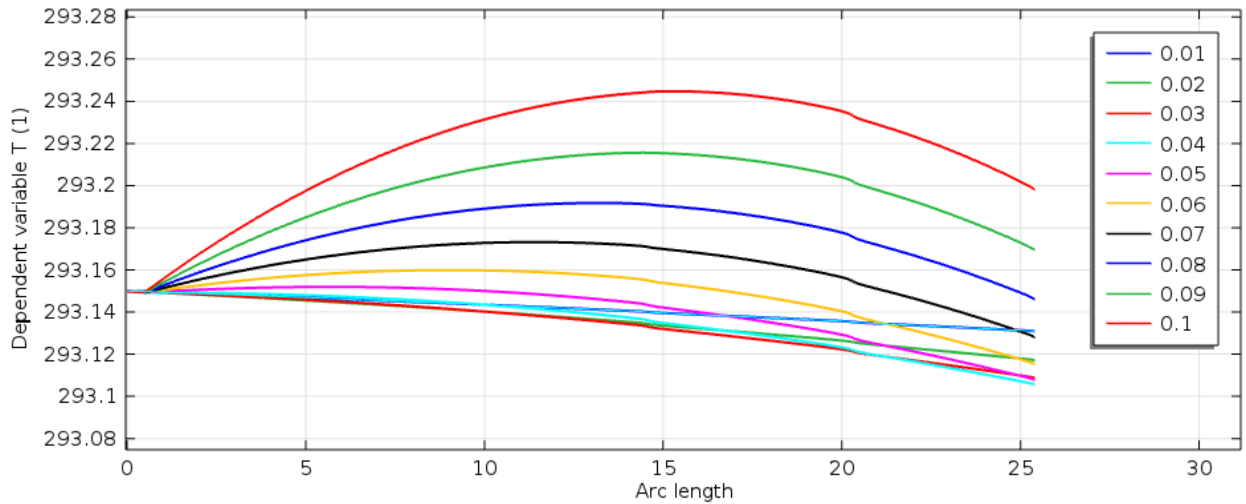


Figure 38. The lines show how temperature varies across the wire from the substrate (one the left) to the membrane. At some applied voltage (or current through the detector), the membrane temperature does not change. The joule heating term and the peltier cooling cancel each other out. Here the value is about 0.08v.

There is a point where two terms are equal and cancel each other and Seebeck can be found from

$$\text{S} = \frac{\text{V}}{2 * \text{T}} \tag{19}$$

When the DC current is cut from the detector, the voltage across the detector drops sharply to a new value. This new voltage is the product of Seebeck coefficient and the temperature difference between the membrane and the substrate. When the joule heating and peltier cooling cancel each

other out, the detector voltage (after cutting the DC current) would be zero. At low current densities, the measured voltage is negative (showing the membrane is cooler than the substrate) and high current densities, the output voltage becomes positive (which means that the membrane is cooler). Thus, the current density is varied to find the zero crossing point and find the Seebeck coefficient. For this detector the effective Seebeck coefficient was 500µv.

The electrical responsivity is:

$$R_{Electrical_DC} = \frac{\eta * S}{G} \tag{20}$$

Where η is the detector fill factor and the rest of the parameters are the same as before. G or thermal conduction is found from the above equation. Combining electrical and optical responsivity equations, the effective absorption coefficient of the absorber can be found. The electrical responsivity is ~2600 which result in the absorption rate of about 70%.

3.4.2.3 Effect of Parylene on the detector performance

As described previously, parylene is a chemically stable and inert polymer that can be deposited at room temperature and because of its low thermal conductivity, it is a great candidate to be used as a supporting layer for thin fragile TE wires. A wafer was fabricated with 400nm parylene following the procedure outlined in the fabrication section. The output response of ten detectors with different designs was measured. Then, the parylene layer was removed using oxygen plasma followed by testing the same detectors under the same condition. The test results are summarized in Table 5.

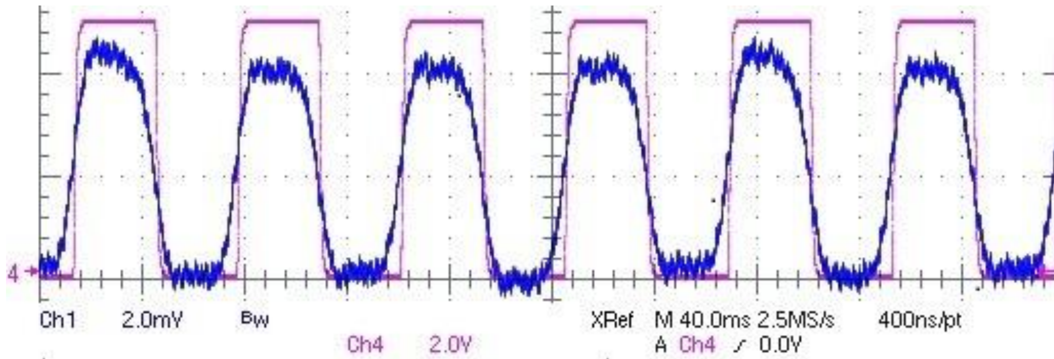


Figure 39. The red plot is the inverted signal coming out of the chopper while the blue plot is the device amplified and processed output signal. The vacuum probe station aperture is few times smaller than the chopper blade opening. The rise time is measured to be less than 8ms.

Table 5. The responsivity of several detectors before and after removing 400nm thin-film parylene off of the TE arms.

Device number	Output voltage before removing the parylene (uV)	Output voltage after removing the parylene (uV)
1	4.15	10.9
2	3.6	14.2
3	10.9	24.1
4	6.65	13.4
5	4	12.6
6	9	16.7
7	5	15.5
8	3.5	15.2
9	15	22.4
10	9.7	22.4

As it can be seen, depending on the detector structures, the improvement in the detectors' performance is different but on average, a 2.5 times improvement is achieved by removing the

parylene layer. This result shows that the heat conduction through the parylene layer is comparable to that of TE wires.

3.4.2.4 Thermal time constant

The detector's thermal time constant can be found from the change in the responsivity with respect to the chopping frequency (f_{ch}). Since the detector output cannot track the modulated optical input as f_{ch} increases, the responsivity slowly decreases. When the detector responsivity is down to 70% of the DC value, the time constant is equal to $\frac{1}{2\pi f_{ch}}$. For our detectors, the equivalent thermal time constant was measured to be 8ms. Figure 40shows how responsivity changes with f_{ch}. The red line is fitted using:

$$R_{normalized} = \frac{R}{R_{DC}} = \frac{1}{\sqrt{1+\omega^2\tau^2}} \quad (21)$$

where $\omega = 2\pi f_{chopper}$.

To find the noise associated with the device, the detector is covered and its amplified output is recorded for 10 seconds using a digital oscilloscope. Then the total RMS noise which is the sum of the oscilloscope, the amplifier and the detector noise is one standard deviation of the amplitude of the recorded signal assuming Gaussian distribution [83]. Next, the detector is replaced by a carbon resistor of equal value and the similar procedure is repeated. Knowing the amplifier bandwidth and assuming that noise sources are independent of each other, detector noise can be back calculated. For our devices, the detector noise is about 30 $\frac{nv}{\sqrt{Hz}}$ which is slightly above the expected Johnson noise. Fourier transform of the output signal reveals that this higher noise is

partially due to mechanical vibrations induced by the vacuum pump and partially due to 60Hz signal caused by ground loops.

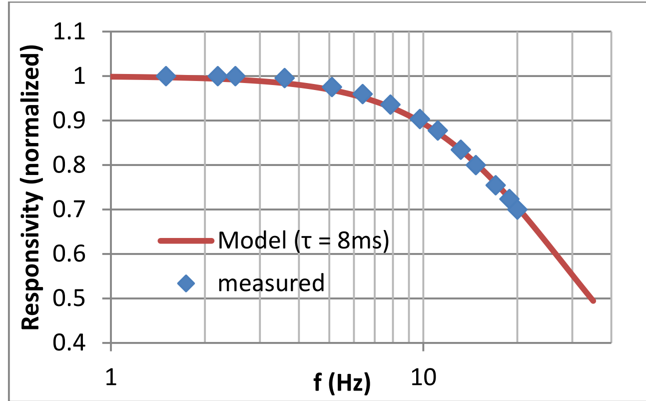


Figure 40. Responsivity vs. chopping frequency – The blue marks are the measured data and the red line is the TE responsivity model for $\tau = 8\text{ms}$

3.4.2.5 Noise

D^* of $2 * 10^8$ $(\text{cm.Hz}^{\frac{1}{2}}\text{W}^{-1})$ is calculated from $[\frac{\sqrt{A_d\,\Delta f}}{V_n} * R_v]$. The limit of D^* for an ideal thermal detector is slightly less than $2 * 10^{10}$ $(\text{cm.Hz}^{\frac{1}{2}}\text{W}^{-1})$ [2].

To further enhance the D*, the thermal isolation between the absorber and the substrate should be improved. This can be achieved by using longer and thinner wires and/or by reduction of thermal conduction through TE wires by changing the material grain size. By reducing the polysilicon deposition temperature and adjusting the deposition rate, more amorphous silicon can be embedded in the film [84] which lowers phonon mean free path and hence thermal conductivity (K). Although this would slightly and negatively affect the electrical conductivity, higher $D^*(\propto \frac{ZT}{K} \propto \frac{\sigma}{K^2})$ can be achieved.

CHAPTER FOUR: THERMAL CONDUCTIVITY CHARACTERIZATION OF POLYSILICON WIRES

A microstructure along with a robust fabrication process is developed for measuring the thermal conductivity (K) of nanowires and thin films. The thermal conductivity of a thin-film material plays a significant role in the thermoelectric efficiency of the film and is usually considered the most difficult thermoelectric property to measure. The lower the K, the higher is the thermoelectric efficiency and hence a higher detectivity can be attained if utilized for infrared detection. Previously it was shown that high responsivity uncooled thermoelectric IR detectors that utilize polysilicon as the thermoelectric material. To further improve the performance of these devices, it is required to understand how the wire dimensions and different deposition parameters affect the thermal conductivity of polysilicon.

It has been shown that silicon nanowires exhibit lower thermal conductivity compared to bulk silicon [22] resulting in a higher thermoelectric efficiency for silicon nanowires. In other words, ZT which is the conventional figure of merit for thermoelectric materials can be improved by reducing thermal conductivity through nano-structuring while other parameters stay relatively unaffected. This reduction in thermal conductivity of nanowires is mainly a result of phonon boundary scattering [22]. We have previously shown high performance uncooled thermoelectric infrared detectors utilizing doped polysilicon as the thermoelectric materials [29]. Polysilicon films are relatively easy to deposit and pattern as opposed to silicon. Additional, polysilicon was expected to exhibit lower thermal conductivity due to phonon grain boundary scattering [35] as well as phonon boundary scattering. To further improve the performance of the IR detectors, the

thermoelectric properties of the polysilicon wires need to be precisely controlled. Seebeck or electrical conductivity can be measured with conventional measurement platforms. To measure these values for a nanowire, four contacts across the wire plus additional heater/thermometer lines on a substrate is adequate to carry out a measurement [85]. However, thermal conductivity measurement has always been challenging since heat flow cannot be directly measured. A special microstructure or a technique is required to find the heat flow and to measure the thermal conductivity of polysilicon wires. The focus of this chapter is to extract the thermal conductivity of polysilicon nanowires.

Previously, thermal conductivity of single crystalline silicon thin film have been measured and reported in [86,87,88]. Thermal conductivity of as low as 22 W/m.K is reported for 20nm thick silicon films [88]. Lower thermal conductivity values of less than 10 W/m.K is reported for 22nm thick silicon nanowires [89]. Thermal conductivity close to amorphous limit (~1.8 W/m.K [34]) is reported for rough silicon nanowires [22]. Compared to silicon as described earlier, thermal conductivity of polysilicon thin films is generally lower due to phonon scattering by grain boundaries [35]. Thermal conductivity of about 15 to 20 W/m.K has been measured for one micron thick polysilicon films at room temperature [90]. Other works has also reported similar values [91,92, 93]. However, to the best of our knowledge, no one has reported thermal conductivity measurement of polysilicon nanowires or ultra-thin films.

In the following, the structure employed for thermal conductivity measurement is explained followed by its fabrication process. Experimental results are summarized in the last section.

4.1 Structure design

The structure used in this work is similar to [89,94]. This free standing structure is comprised of two metal coils on top of two membranes where each membrane is suspended by four supports as depicted in Figure 41. Patterned platinum coils on the membranes are used as heater/thermometer. In the heater mode, upon passing an electric current through a coil, the temperature of the membrane rises due to joule heating. The generated heat will propagate to the other membrane through the nanowires and increases the temperature in the second membrane (sense membrane). In the thermometer mode, the change in the resistance of the coil due to temperature variation is used to find the temperature of the membrane.

Four point probe technique is utilized for accurate resistance measurement. A current is passed through the metal coil from two of the metal connections (shown in Figure 41) and using the other two connections, the voltage drop across the metal coil is measured. Knowing the temperature coefficient of resistance (TCR) of the metal coil, the temperature of the membrane can be found.

To avoid heat generation in the sense membrane when sensing current is applied, an extremely low current should be passed through the coil. As described in [94], an effective method to improve signal to noise ratio and the measurement accuracy is through using an AC current instead of a DC current. Thus, a lock in amplifier is utilized to measure the voltage drop across the coil in this method.

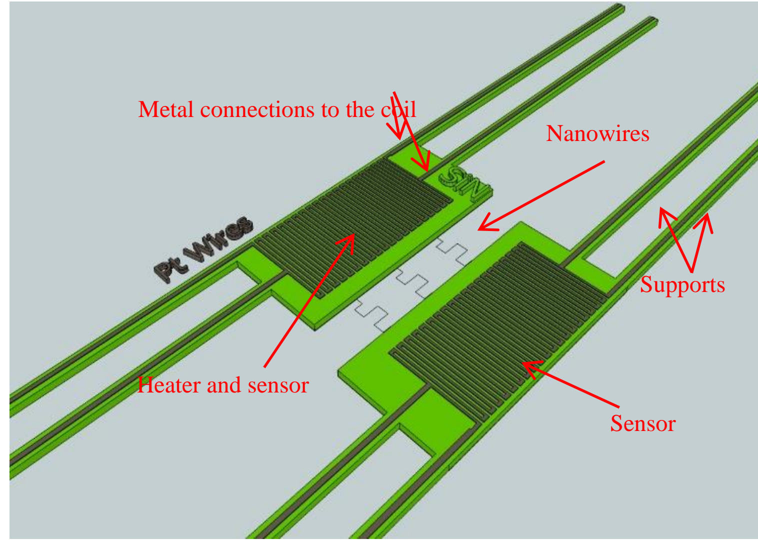


Figure 41. Schematic of the structure used for measuring thermal conductivity of polysilicon nanowires

After measuring the temperature of the membranes, the thermal conduction of the nanowires can be calculated from [94]:

$$G_b = \frac{Q_h + Q_l}{\Delta T_h + \Delta T_s} \tag{22}$$

$$G_s = G_b * \frac{\Delta T_s}{\Delta T_h - \Delta T_s} \tag{23}$$

where G_b is the total heat loss through the supports and G_s is the thermal conduction through the nanowires, Q_h is the heat generated by the metal coil on the hot membrane, Q_l is the heat generated on the beams carrying the hot metal lines, ΔT_h is the hot membrane temperature difference, ΔT_s is the sense membrane temperature change. Given the total heat generated inside the structure from joule heating of the wires and the coil on the hot membrane, heat distribution across the supporting beams, the temperature of the membranes, and the geometry of the wires, the thermal conductivity of the wires (k_sample) can be calculated.

4.2 Fabrication process

This section discusses the process flow and all the details about the fabrication process. The challenges faced during the fabrication steps are discussed. The goal to fabricate this structure is to have two membrane that are well isolated from the substrate and to achieve this goal, the length of the support arms are lengthened which caused many difficulties and they will be explained in this chapter.

4.2.1 Process flow

The fabrication is a 5-mask process as depicted in Figure 42. The process starts with a blank silicon wafer. A layer of silicon dioxide is deposited followed by polysilicon deposition. Then the polysilicon film is patterned to form the desired structure. A thin layer of PECVD silicon dioxide is deposited and patterned over the polysilicon structure to protect them during the next few steps. A dielectric layer is deposited and patterned to from the supports and the membranes. Electrical wires are created next and the final step is to release the structure using bulk silicon etching from topside. More details about each step is provided in the next sections.

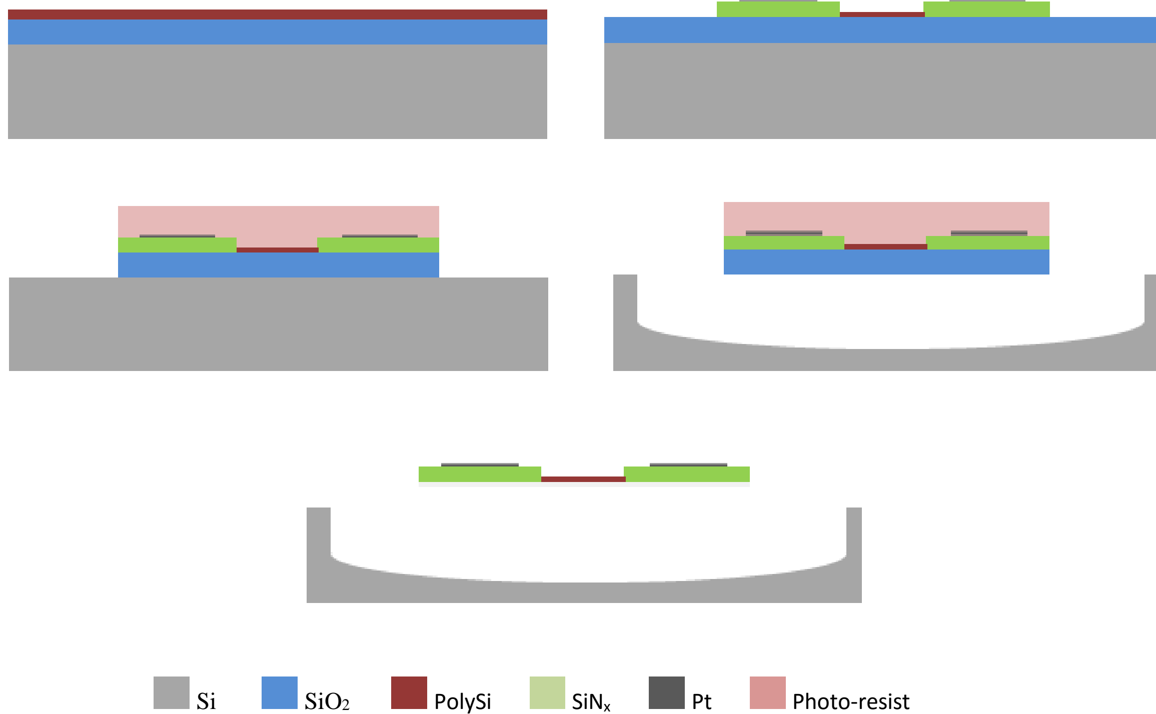


Figure 42. The schematic process flow: (A) all the deposited layers, (B) patterned nanowires, silicon nitride membranes and metallization, (C) after silicon dioxide etch showing the coverage of the resist on the main structure, (D) suspended structure by removal of the silicon substrate (E) completely fabricated and released structure.

4.2.2 Process steps

The process starts with a blank silicon wafer. 100nm silicon dioxide film is grown using wet oxidation technique at high temperatures. The high oxidation temperature is required to achieve low stress in the film [95]. The low stress ensures that the device can be suspended without any deformation. There are also other thin films that can be used as a sacrificial layer like silicon nitride, polysilicon, PECVD oxide, etc. however, the thermally grown silicon dioxide meets the thermal budget, stress, and etching requirement for the rest of the process.

Next is to deposit the polysilicon layer in an LPCVD (low pressure chemical vapor deposition) system (Figure 42 (A)). The process parameters should be well controlled since polysilicon nanowires will be formed out of this film and the thickness of the deposited film is the final thickness of the nanowires. Also, grain size and crystallinity of the nanowires must be adjusted at this step by changing process pressure and temperature.

If thermal conductivity of a doped polysilicon layer is of interest, then the deposited film needs to be doped at this step. The polysilicon film can be implanted or in-situ doped. Dopant diffusion sources were used to achieve the desired doping concentration inside the film. A single note is that any high temperature annealing after initial deposition will result in larger grain size which consequently increases the value of the thermal conductivity [35] and it should be taken into account.

Two separate patterns are created from the polysilicon film, nanowires and thin films. E-beam lithography is used to form the nanowires as shown in Figure 43. The wider wires are created using conventional lithography.

The wires are protected throughout the process with 300nm of PECVD (plasma enhanced CVD) silicon dioxide. This film will be removed in the final releasing steps. This PECVD film needs to be partially patterned and removed before silicon nitride deposition. To pattern this layer, a combination of dry and wet etching techniques should be used. Only dry etching might result in partially etching the under laid polysilicon layer. Thus, to get straight sidewalls and avoid etching the polysilicon film, most of the film is etched in ICP using CHF_3 based plasma and wet etching in BOE 6:1 utilized to etch the remaining. The wet etching has negligible effect on the underneath

layer. The wet process needs to be timed closely to avoid over etching the rest of the substrate (which is silicon dioxide too). The result after etching is shown in Figure 44(a).

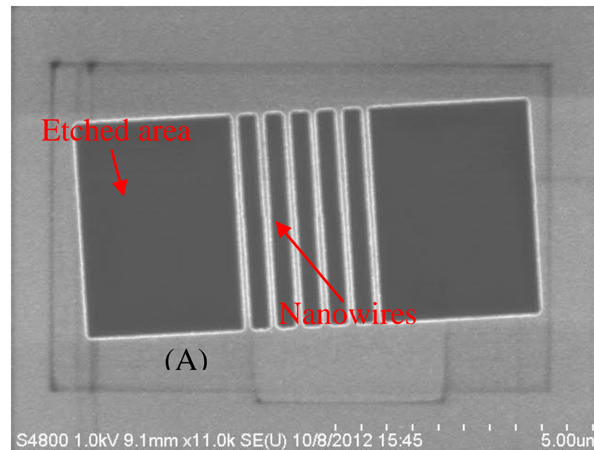


Figure 43. SEM of the patterned nanowires using e-beam lithography technique [96].

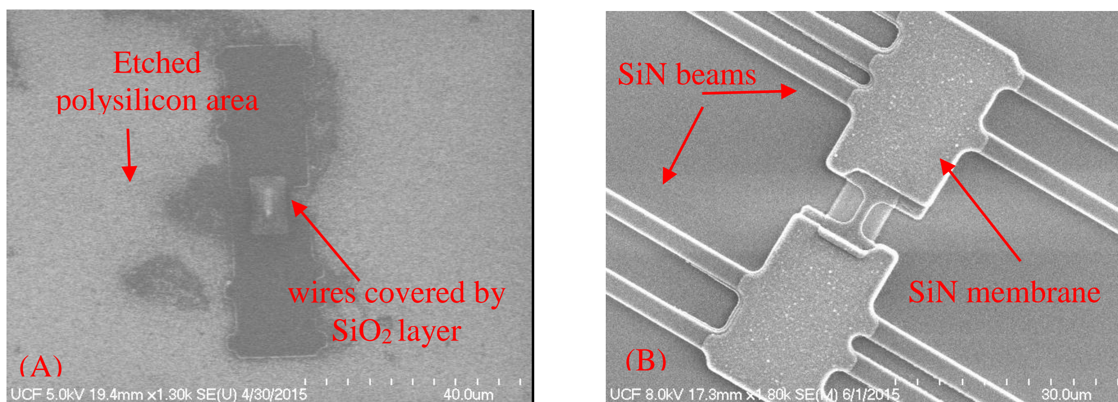


Figure 44. (A) SEM showing the patterned SiO_2 layer on the wires, (B) Top view of a device after patterning the silicon nitride layer and removing the protective oxide from top of the wires.

A silicon nitride film is deposited as an electrical insulator before metallization. This layer will also be used to form the membranes and the support arms for the membranes. The silicon nitride is required to have low etch rate in hydrofluoric (HF) acid and as-deposited tensile stress (in order

to avoid deformation after release). Thus, different layers from different types of silicon nitride are deposited in a stack to achieve the desired goal. The stack is comprised of a 300nm thick stoichiometric silicon nitride layer with tensile stress sandwiched between two 50nm silicon rich films. Having silicon rich films ensures low etch rate in HF based chemicals. The stress in the silicon nitride layer can be varied by changing the ratio of nitrogen to helium of the plasma during the deposition. Figure 49 shows how stress in the silicon nitride film can affect the shape of the support beams. The above approach was used when the Silane used during the PECVD deposition was diluted in Helium. The effect of He inside the plasma is to bombard the surface and increase the surface adatoms and as a result the film becomes compressive. Thus, reducing He or increasing N2/He ratio can lead to tensile stress. If the Silane was diluted in nitrogen, the grown film is intrinsically tensile and by adding a small amount of He, the stress can be adjusted as required. After depositing the proper film, it is etched in $CHF3^{+}$ based plasma. Figure 44 (B) shows the SEM of an etched film. Silicon nitride membranes and the beams are marked on the SEM.

The next step is depositing metallic heater on the silicon nitride membranes using a lift-off process. Platinum is the preferred material for this step due to its linear TCR however, it does not have good adhesion to the substrate. Sputtered Pt with a thin adhesion layer of Cr was sputtered for some of the devices. However, the lack of good adhesion reduced the fabrication yield. Instead, Nickel was deposited using e-beam evaporation technique. Nickel has better adhesion and higher TCR compared to Pt, however, its resistance does not vary linearly with temperature. This problem can be eliminated by plotting the film resistance vs temperature and calculating TCR at each temperature. Figure 45 shows the device after metal film deposition.

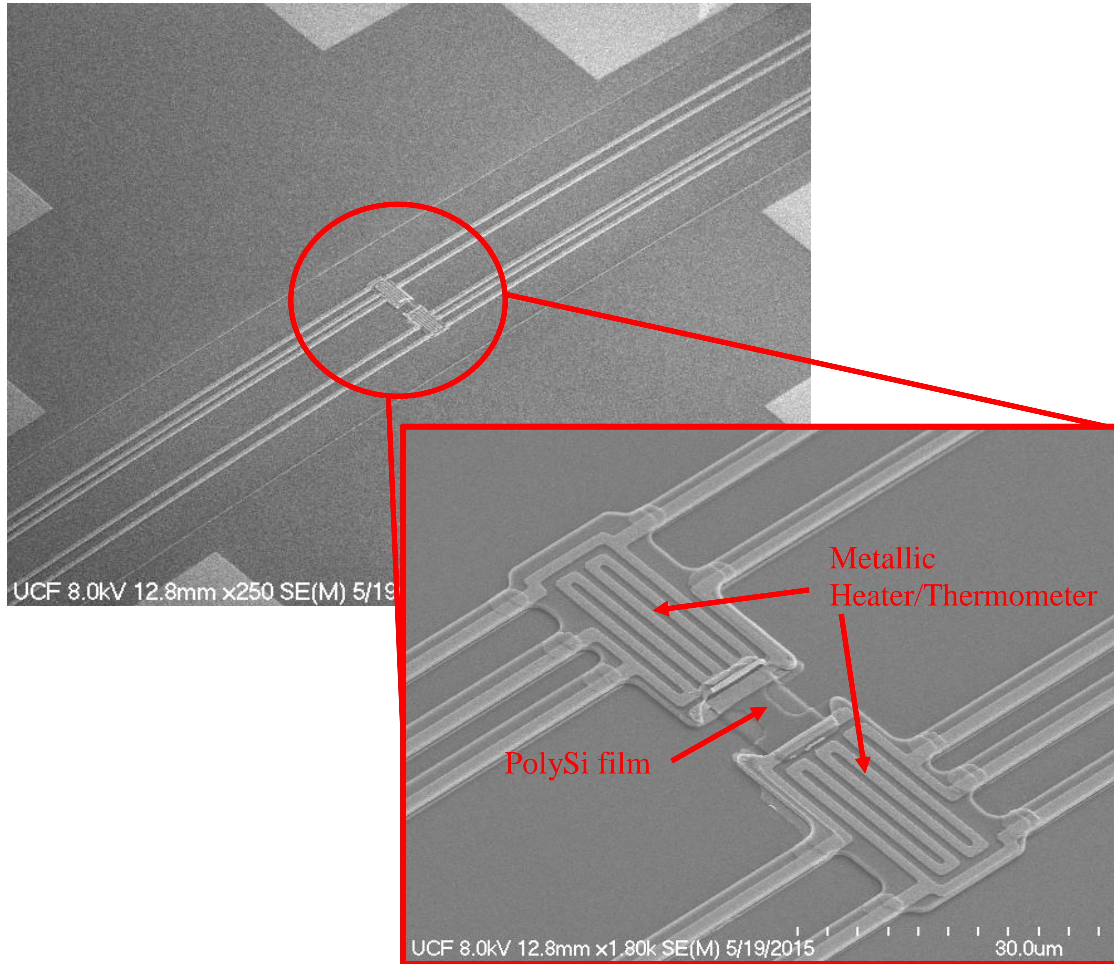


Figure 45. On the top is the top view of a device and at the bottom is a close-up of the two membranes and the metallic heaters on top. Also the polysilicon film fabricated between the membranes can be seen.

Figure 46 shows the discontinuity in one of the metallic films used for measuring electrical resistivity and Seebeck coefficient. The step height on the silicon nitride is about 300nm and the 50nm deposited nickel cannot form a continuous coating on the sidewall. This problem is more severe for the e-beam evaporated than the sputtered film. A new layer is added to address this issue. A thick aluminum layer is deposited over the steps and also over the contact areas to reduce

electrical resistivity. This Aluminum step also prohibits galvanic corrosion of polysilicon in the final release step in BOE. Figure 47 shows the how 500nm aluminum covers this step.

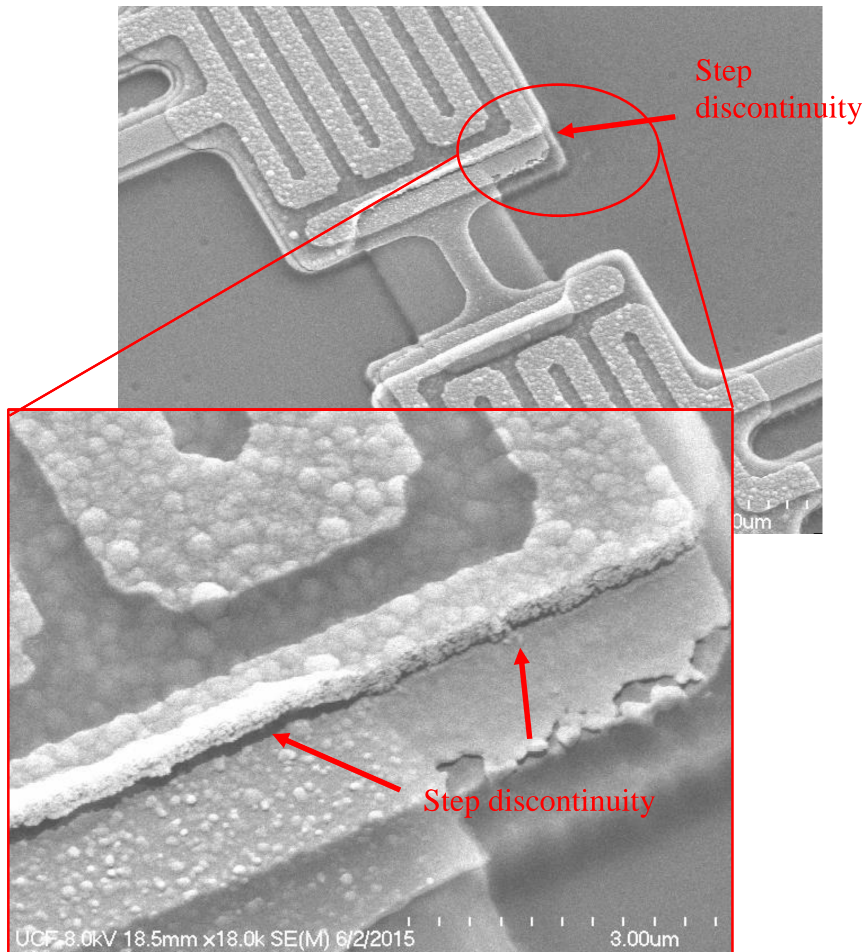


Figure 46. SEMs showing discontinuity in the nickel film over the silicon nitride step.

At this point, devices are ready to be released from the substrate by anisotropic etching of the substrate. To protect the structure during the wet etching step, a layer of photoresist is used to cover the device. Through the etch holes in the resist, the thermally grown oxide layer is etched away in an inductively coupled plasma system until the silicon substrate is exposed (Figure 48). At this stage as depicted in Figure 42(D), silicon substrate is etched isotropically using SF6 based

plasma until desired undercut is achieved and the structure becomes completely suspended. Next, a short dip in HF based solution will remove all the silicon dioxide layers at the same time. At this point the device is completely released and the photoresist layer is left on the device helping the structural integrity. There is no wet processing step from this point and the resist is removed in an O_2 based plasma (Figure 42(E)). Figure 50 shows SEM images from a completely fabricated and suspended structure.

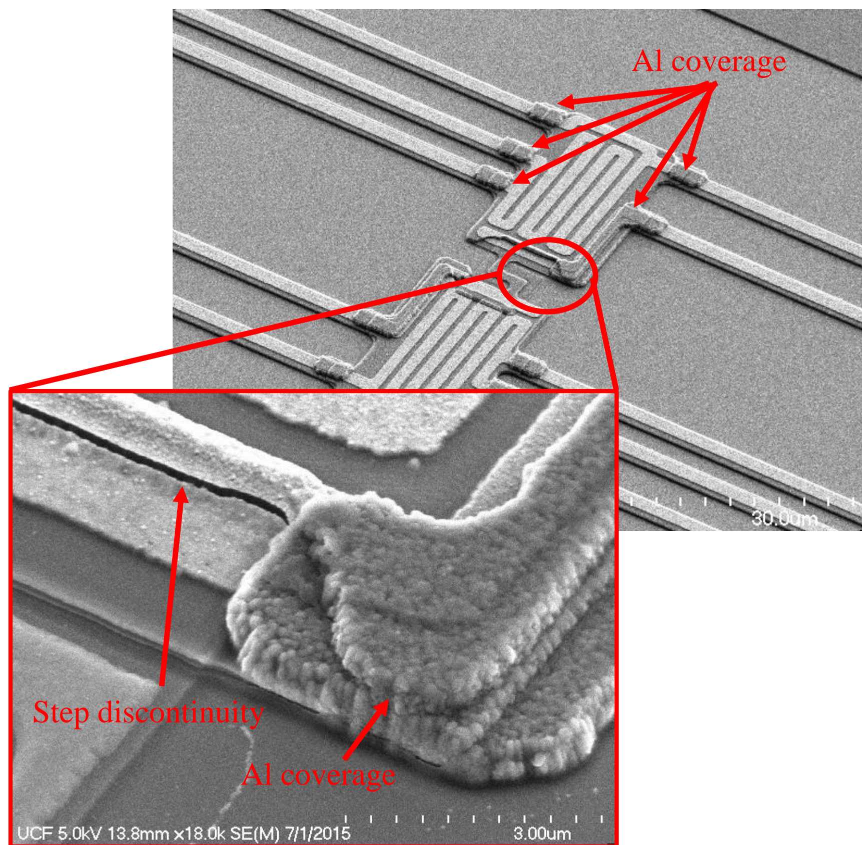


Figure 47. SEMs showing how the silicon nitride step is covered with a thick layer (500nm) of Al.

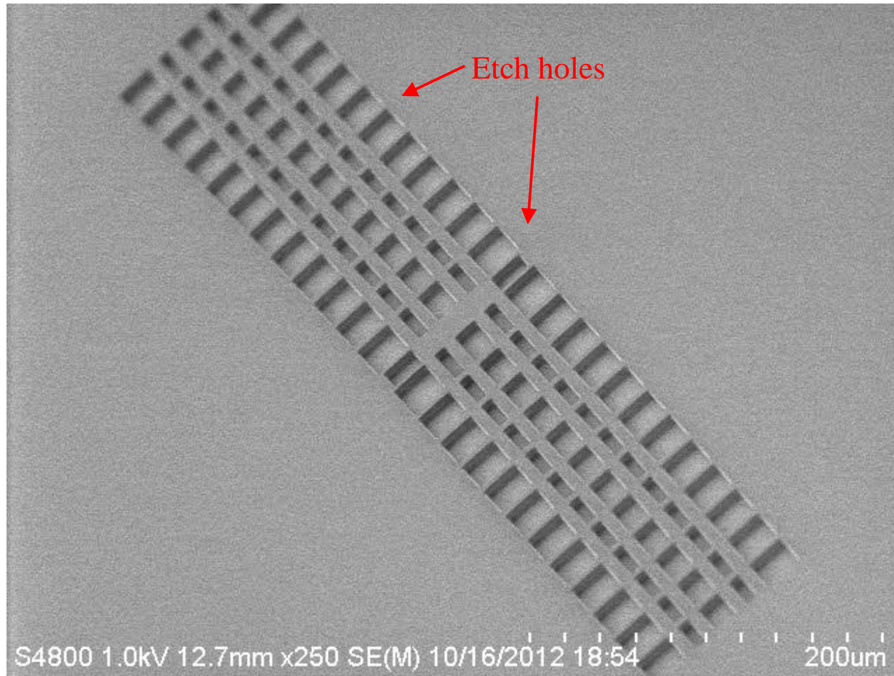


Figure 48. SEM showing the top view of the etch holes [96]

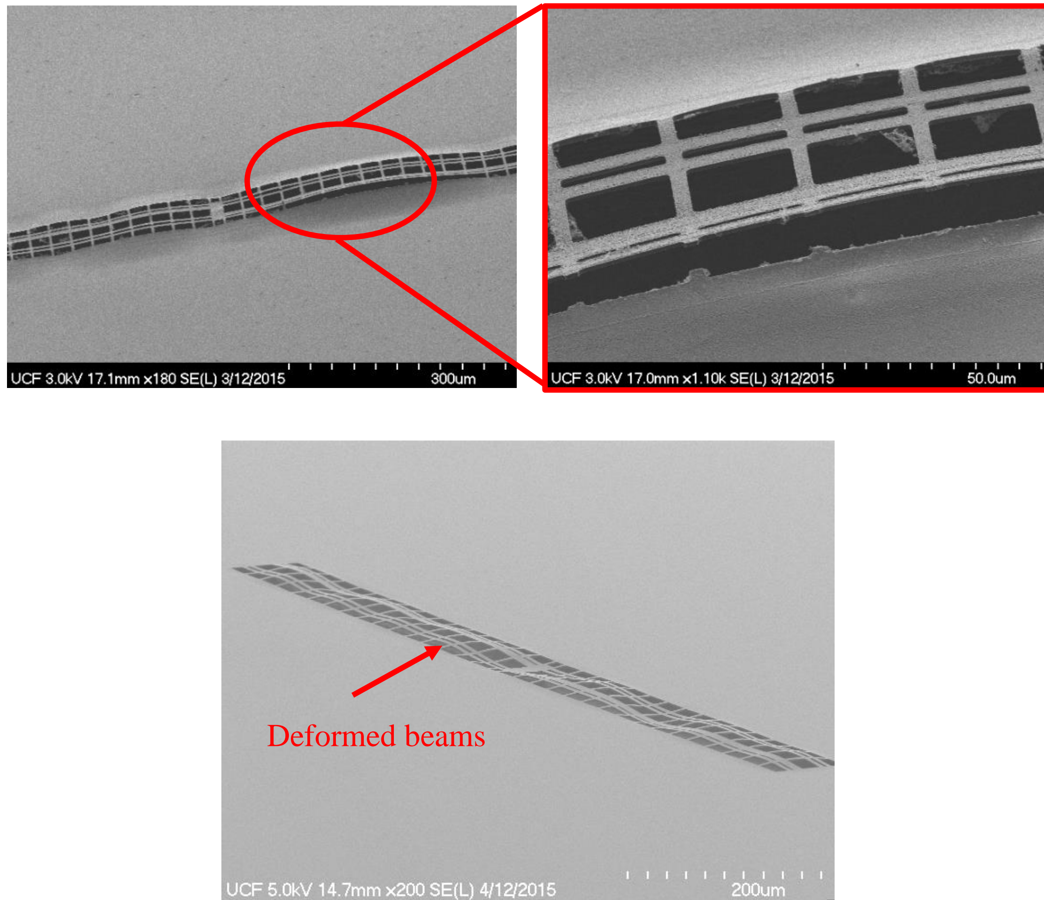


Figure 49. SEMs showing deformed structure due to high compressive stress in the supporting beams

The stress in the silicon dioxide film can deform the structure. To reduce the adverse effect of this high compressive stress, the initial thickness of the thermally grown oxide is reduced from 2um to about 100nm. Additionally, the tensile stress in the silicon nitride film is increased by completely removing He from the process and increasing the ammonia content. Increasing ammonia is carefully carried out since it also increased the etch rate of the film in BOE. The effect of the stress induced deformation is shown in Figure 49. The SEM of a completely fabricated device is shown below. SEMs of the devices made for measuring all the thermoelectric properties of a thin film at once is shown in Figure 51.

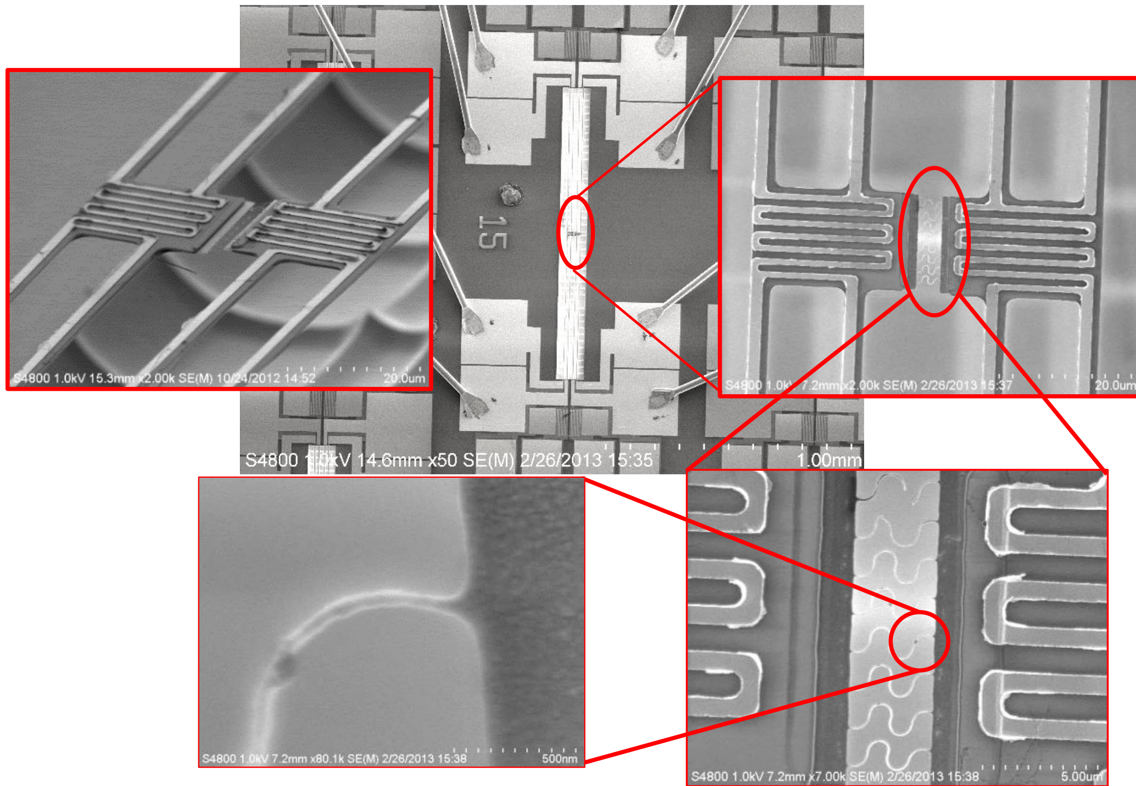


Figure 50. (A) SEM of the top view of a complete device after wire-bonding, (B) SEM of the side view showing suspended structure, (C) SEM of the top close-up view, (D) Close-up form nanowires, (E) SEM of the single wire.

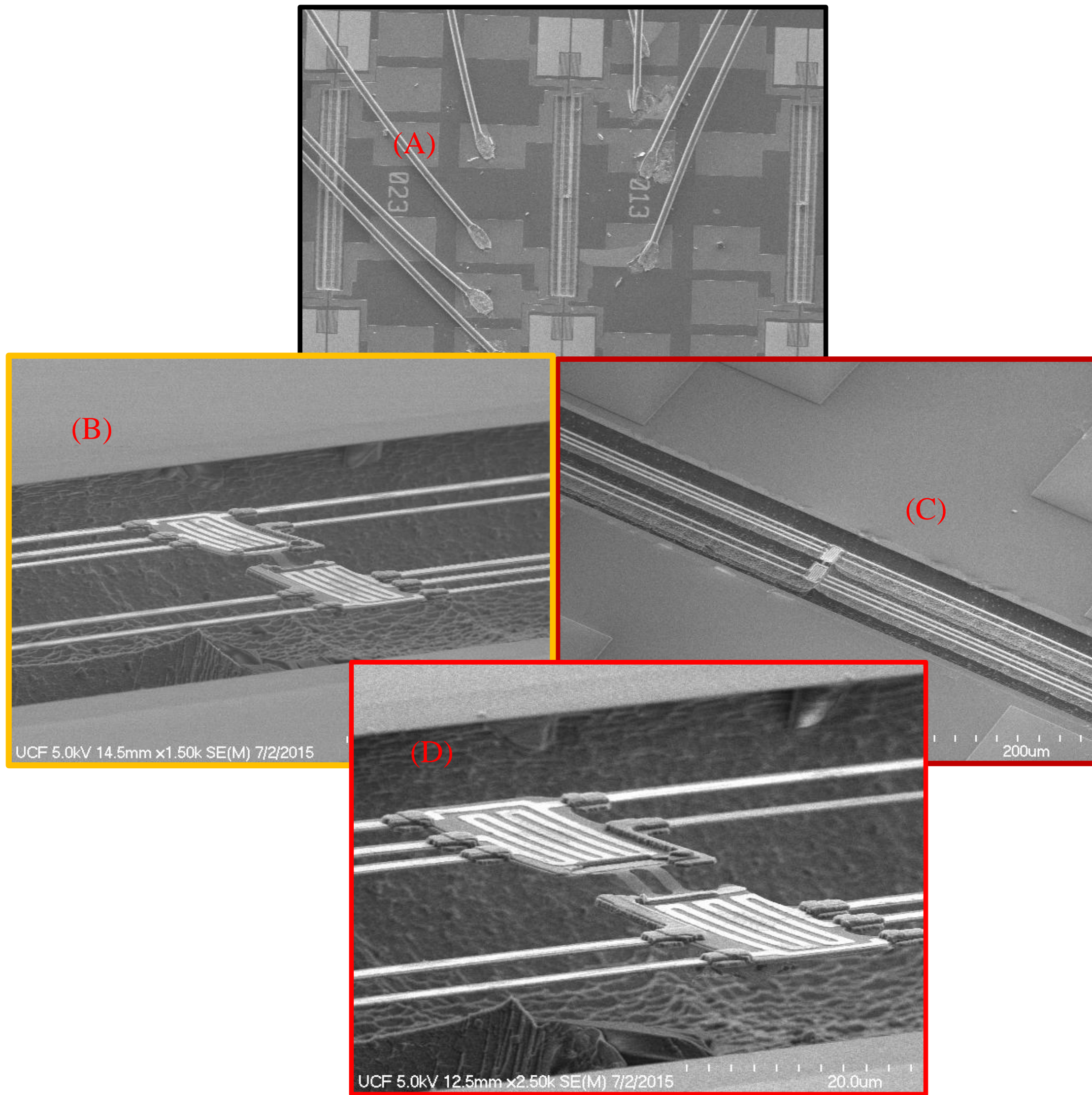


Figure 51. (A) Shows the top view of the wirebonded device, (B) presents the side view of a device with a wire between the membranes, (C) shows the top view of the device, (D)shows the side view of a device with two wires. It can also be observed that the membranes are completely suspended over the substrate.

4.3 Measurement

In the following subsections, the experiment setup is discussed followed by the measurement results. All the measured properties are summarized in a table for convenience. At the end of this section, the limit of the measurement is also discussed.

4.3.1 Measurement setup

As mentioned before, equations (22) and (23) are used to find the thermal conduction through the nanowires. Given the geometry of the wires, the thermal conductivity of the wires can be extracted. To find the temperatures of the suspended membranes, the following equation is used:

$$\Delta T = \frac{\Delta R}{R_0 \alpha} \qquad (24)$$

where α is TCR and R_0 and ΔR are the coil resistance and change in the resistance of the coil due to being heated respectively. A coil-like calibration structure was used to find the value of TCR. The structure temperature was controlled in a vacuum probe station and the resistance of the coils were recorded at different temperatures. The measurement setup is schematically shown in Figure 52. TCR was found to be $0.0015 \ \frac{1}{°C}$ with a linear relation with temperature around room temperature.

In order to measure the temperature change in the membranes due to heat generation, the fabricated microstructure wire-bonded to a readout circuit (Figure 50(A)) was placed inside the vacuum probe station to avoid thermal losses due to convection and conduction to air. The vacuum level was kept at 3 mtorr or lower at all time during the measurement. Then a current of about 20 µA was applied to one of the coils on a membrane. The changes in the resistance for both coils on the membranes

were found by measuring the current going through and the voltage across the coils. Table 6 is the summary of the important parameters and measured values. The size of the wires was measured from the acquired SEM (Figure 50(E)).

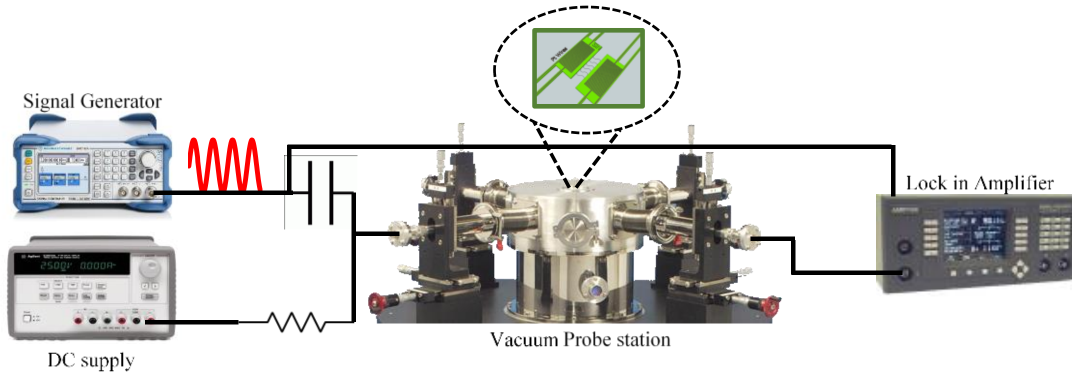


Figure 52. Measurement setup.

Table 6. Summary of the measurement

Support beam length	550um	**ΔR for hot membrane**	**4.3Ω**
NW width	60nm	**ΔT for hot membrane**	5.47°C
Number of NWs	6	**ΔR for sense membrane**	0.96Ω
Length of the NWs	6.07um	**ΔT for sense membrane**	0.9°C
Applied current to the coil	19.72uA	$\mathbf{G_b}$	$9.56 * 10^{-8}$ W/K
$\mathbf{Q_L}$	$3.9 * 10^{-7}$W	$\mathbf{G_s}$	$1.89 * 10^{-8}$ W/K
$\mathbf{Q_h}$	$2.18 * 10^{-7}$W	$\mathbf{K_{sample}}$	3.48 W/m.K

From previous experiments, it was observed that nanowires with the same thickness (not the same width) have very comparable thermal conductivity. This convinced us to try thin films with the same thickness as the nanowires but with a much larger width. In addition, grain sizes on the thin films changed intentionally during fabrication. Three different samples were fabricated. Sample 1 was amorphous silicon (Si:H) deposited using PECVD from Silane. Sample 2 was polysilicon deposited at 620C and sample 3 was again polysilicon film deposited at the same time with sample 2. However, it was annealed later at 1100 for 5 minutes. Everything else was tried to be kept the same for all of the samples. To increase the signal to noise ratio, Nickel micro heaters were used instead of Platinum (Nickel TCR is higher than Pt [97]).

The same procedure was used to measure the thermal conductivity of the samples. The measurement result is summarized in Table 7.

Table 7. Summary of the thermal conductivity measurement

Sample #	Film Thickness	Measured K (W/m.K)	Description
1	90nm	~0.8	a-Si:H
2	108nm	~3.8	Polysilicon deposited at 620C
3	108nm	~6	Polysilicon deposited at 620C and the annealed at 1100C for 5minutes

In all of the calculation, it is assumed that the substrate temperature does not change and the only heat path from the hot side to the cold side is through the sample. To make sure this assumption is right and also to check for the accuracy of the measurement, some devices were fabricated without the thin film between the membranes. Same measurement procedure was repeated to see if the temperature rise in the hot membrane would lead to any temperature rise on the cold side. Over 10 measurements were carried out. Some of the measurements were showing temperature rise and

some other showing the other membrane cooling down. On average, there was 0.1C increase in the temperature of the second membrane which is about 2.5% of the temperature rise in the cold membrane (The typical temperature rise in the cold membrane is about 4 degrees).

The thermal conductivity measured for the as deposited polysilicon film is very close to the value measured for nanowires and both values are considerably lower than the bulk value (30W/m.K). This suggests that the drop in the thermal conductivity is mostly due to reduction of the thickness and the lateral dimension is not a major factor. In another word, the out of the plane contribution to thermal conductivity is more important than the in plane contribution in this case. This very well aligns with the granular structure of polysilicon [35]. The LPCVD grown polysilicon film has thickness limited crystal size in the out of plane direction. In the in plane directions, there are many grain boundaries and the grain boundary scattering limits thermal conductivity. The difference between the thermal conductivity of polysilicon and single crystalline silicon is basically due to these grain boundaries.

Annealing at 1100C does not change the thickness or the grain size in the out of the plane direction. However, the in plane grain size grow and this explains why thermal conductivity increases for sample 3 compared to sample 2 and this supports the previous explanation.

Thus to effectively control and limit thermal conductivity, both the film thickness and grain sizes should be controlled. The temperature used for polysilicon deposition is of great importance. At lower temperatures (590C [98]), the film is mostly amorphous and as the deposition temperature increases, the film contains more crystalline domains and structure changes from amorphous to granular.

Other factors like the film stress and sheet resistance in some applications, can limit the process window and other factors like doping can be used to further limit the thermal conduction.

Thermal time constant of a device is a measure of how well thermal conduction is limited from substrate to substrate.

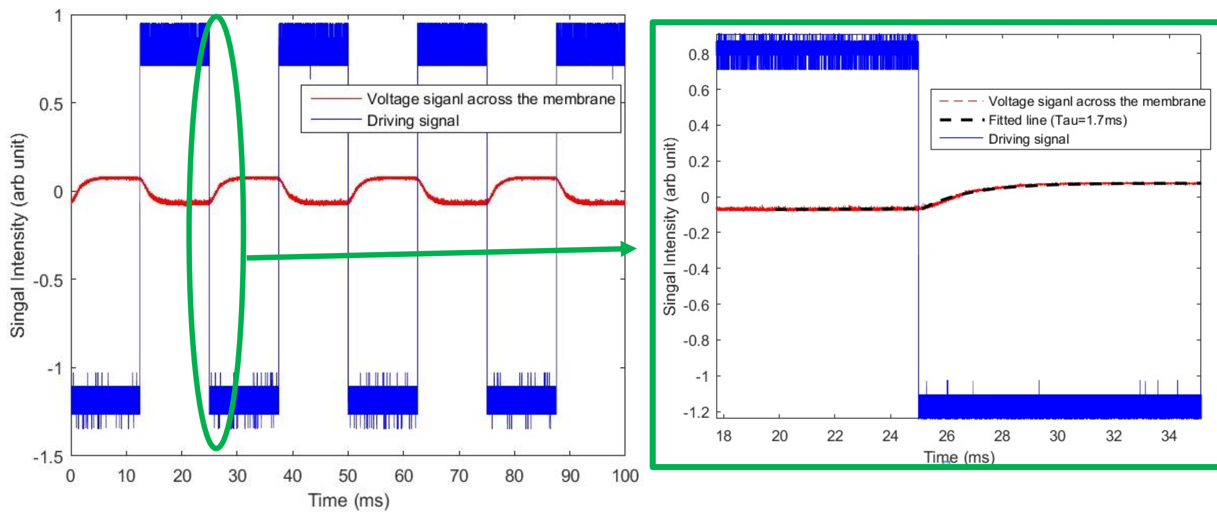


Figure 53. On the left, blue line is the driving signal and the red color shows how the voltage on the membrane is changing. On the right, the dashed black line is the fitted line with time constant of 1.7 ms.

To get an idea on what the thermal time constant of structure is, a pulsed DC current was fed to a membrane. The RF signal used for resistance measurement in the previous section was monitored during the pulsing sequence. Since the membrane has a relatively large thermal time constant, it takes some measureable time, correlated to thermal time constant, for the voltage to drop or rise due to turning off or on the current respectively. Figure 53 shows the measurement results. Blue line is the driving signal and the red line shows how the voltage on the membrane is changing. On the right, an enlarged part of the signal is shown. The dashed black line is the fitted line with the time constant of 1.7 ms.

4.3.2 Limit of thermal conductivity detection

To estimate the limits of thermal conductivity measurement, the noise equivalent G_s (NEG_s) should be lower or comparable to G_s. From equation (17), it can be seen that NEG_S depends on the values of G_B and the minimum resolvable temperature of the sensing element (or NET_S). NET_s was measured independently and found to be less than 50mK. Based on the measured value of G_b ($1 * 10^{-7} \frac{W}{K}$), and $\Delta T_h - \Delta T_s = 5°C$, the NEG_s is calculated to be $1 * 10^{-9} \frac{W}{K}$ at room temperature which is much lower than the measured G_s.

Heat loss due to radiation can be approximated by $Q = A_1 \, F \, \sigma \, (T_{device}^4 - T_{room}^4)$ where A_1 is the area of the device, F is view factor, σ is Stefan Boltzmann constant. Assuming worst case emissivity of 1 and device temperature 5 degree above room temperature and ignoring the fact that the membranes are covered by Pt lines, the total heat loss due to radiation would be $\sim 4 * 10^{-9}$ W which again is small compared to the thermal conduction through the supporting beams and can be ignored.

CHAPTER FIVE: CONCLUSION

This last chapter is a brief conclusion of the work presented in this dissertation and also a short summary of the accomplishments. The last section is a short discussion about the future research.

5.1. Accomplishments

This work is mainly focused on two projects that are closely related. The first one is creation of high performance thermoelectric infrared detectors and the second project is characterizing the properties of the polysilicon wires that are utilized in the detectors and the final goal is to optimize the property of the wires.

As a result of this work, ZT/K as a new figure of merit for sensing application has been introduced and it was illustrated that the reduction of the thermal conductivity of the thermoelectric material is of great importance.

Highly doped n and p type polysilicon were chosen as the thermoelectric material pair. Polysilicon is cost effective, easy to deposit/pattern, and widely available in CMOS industry. In addition, it offers lower thermal conductivity than silicon due to grain boundary phonon scattering. Discussions on the doping concentration, the optimum Seebeck coefficient which is in the range of 130 to 190 μV, and the required number of thermocouples were also provided. It was shown that for the proposed structure, minimum number of thermocouple (i.e. one) is the optimum design.

A detector based on stand-alone polysilicon wires and a high fill-factor umbrella-like optical-cavity absorber has been fabricated. Superior thermal isolation was achieved since sub-micrometer polysilicon wires were the only heat path from the absorber to the substrate. A high responsivity of 1800V/W and a detectivity of $2 * 10^8$ $(\mathrm{cm.Hz^{\frac{1}{2}}W^{-1}})$ has been measured from a 20um x 20um device which is due to the unique features stated above. This high detectivity makes thermoelectric detectors feasible for low cost fabrication of IR arrays for low-power and high performance application.

As a result of the second part of the project, a microstructure is created to measure the thermoelectric properties of polysilicon wires and thin films.

For the first time, thermal conductivity of polysilicon nanowires have been measured. To improve measurement accuracy compared to previous works, several nanowires are placed in parallel which results in higher heat transfer between the isolated membranes. Also, to avoid measurement errors due to thermal contact resistance, the nanowires are formed from a thin film.

As a result, thermal conductivity value of 3.5 W/m.K has been measured for an un-annealed/undoped polysilicon nanowires deposited at 620 °C and the cross section of 60nm by100nm which is much smaller than that of the bulk. This low thermal conductivity of polysilicon nanowires suggests that high performance thermoelectric infrared detectors can be constructed using this wires.

Comparable thermal conductivity to nanowires is measured for thin films with the same thickness suggesting that thermal conductivity of polysilicon films is a strong function of the film thickness.

In the in plane direction, the thermal conductivity is limited by the phonon grain boundary scattering and in the out of the plane direction, it is limited by phonon film boundary scattering.

5.2. Future Research

To further improve the performance of the thermoelectric infrared detectors, the thermoelectric properties of polysilicon wires should be improved. To further reduce the thermal conductivity of the polysilicon film, the grain size of the film should be controlled. Different dopants affect the grain growth during the dopant activation process. Thus, careful consideration for the annealing process and the film thickness should be in place.

To reduce the detector resistance, a good ohmic contact to the thermoelectric wires should be formed. This would increase the signal to noise ratio. All the results reported in this work regarding IR detectors suffer from high contact resistance and do not have the silicide contact. Adding a silicide contact as described earlier can greatly reduce the device resistance.

Another performance enhancement is to improve the absorber absorption. There are many absorber designs that can be used to optimize this. Any design needs to have low heat capacitance to decrease the thermal time constant (which this is ultimately results in higher frame rate).

This can be accomplished by introducing holes into the absorber. However, holes' sizes should be exactly designed to avoid absorption loss.

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