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Chemical And Biological Treatment Of Mature Landfill Leachate

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A NON-ISOLATED HALF-BRIDGE BUCK-BASED CONVERTER FOR VRM APPLICATION AND SMALL SIGNAL MODELING OF A NON-CONVENTIONAL TWO PHASE BUCK

by

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ABSTRACT

The challenges imposed on Voltage Regulator Modules (VRM) become difficult to be achieved with the conventional multiphase buck converter commonly used on PC motherboards.

For faster data transfer, a decrease in the output voltage is needed. This decrease causes small duty cycle that is accompanied by critical problems which impairs the efficiency. Therefore, these problems need to be addressed.

Transformer-based non-isolated topologies are not new approaches to extend the duty cycle and avoid the associated drawbacks. High leakage, several added components and complicated driving and control schemes are some of the trade-offs to expand the duty cycle.

The objective of this work is to present a new dc-dc buck-based topology, which extends the duty cycle with minimum drawbacks by adding two transformers that can be integrated to decrease the size and two switches with zero voltage switching (ZVS).

Another issue addressed in this thesis is deriving a small signal model for a two-input two-phase buck converter as an introduction to a new evolving field of multi-input converters.

To all beautiful minds out there…

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"Thanks be to God, who always leads us in triumphal procession..."

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CHAPTER 1

INTRODUCTION

1.1 Overview

Power supplies are the core element in most of the electrical equipment needed today. Loads can be very critical in the sense that they need to be fed with a constant, highly regulated input power. Computer processors are one such example of critical loads, which is why the silver box power supply in the computer case cannot be directly connected to the microprocessor. Instead, it is connected to a dc-dc converter, the output of which feeds the processor.

Point of Load (POL) regulation has replaced the old centralized power box due to its vicinity to the microprocessor, which results in a closed dc-dc converter being dedicated to deliver the power needed by the microprocessor. This has alleviated the undesired effect of the parasitic elements that existed in the old system. These POLs are called Voltage Regulator Modules (VRM).

The trend to have low voltage VRMs as a microprocessor's power supply is increasing due to the benefit of lower power loss and faster data transfer. Hence, the initially used power delivery structure, which adopted a centralized silver box to supply the load, became unsuitable for meeting the challenge of low output voltage due to the resistive and inductive parasitics.

The equivalent inductance of the regulator is the barrier of output current slew rate; for lower ripple current and consequently lower rms current resulting in lower power loss, the output inductor should be large. On the other hand, large inductors mean

slower transient response. It is a design challenge faced by switching converter engineers to compensate both cases. Fast transient response under fast load change is a crucial issue in dc-dc converters with modern microprocessors [1-5].

Dynamic response of the converter has been a research focus to enhance the transient response of the control loop during significant step-up and step-down load conditions, which may reach 120A/us [11-17, 19, 20- 24, 27-28].

The main VRM cannot handle the required fast transient effectively due to its large filter inductance, which is needed to decrease the output current ripple. The delay times of the controller, LC filter and the compensation network also add some restrictions on how fast the VRM can respond to any load change. Therefore, many efforts have been put into increasing the transient response of the VRM [11-17, 19, 20- 24, 27-28].

A conventional step-down buck converter is the building block of any VRM, but due to the high output ripple, an interleaved multiphase buck replaced the buck with the same 12 Volt input [23]. Another possible solution is to parallel several converters, each with a large inductor, which results in a small overall inductance value; however, the steady-state performance will still not be satisfactory due to higher losses.

A stepping inductor introduces a method to achieve a fast transient response during load variation, and at the same time guarantees lower current ripple during normal steady-state mode. This is done by having two different inductor values in series. The smaller value dominates during transient period and the larger during steady-state [14, 30].

The output suffers from two voltage spikes that occur during step-up and step-down conditions [25]. The methods and suppression techniques developed so far focused

mainly on decreasing the second voltage spike as there is no control over the first spike due to its very short time period and its dependency on the capacitor parasitic.

The current compensation technique to enhance the output voltage during transient is based on two injection methods: linear and switching [11-16].

Active Transient Voltage Compensator (ATVC) approaches the problem in a similar yet opposite way. It relies on injecting a voltage source instead of current [25]. ATVC simply acts as another buck converter but with smaller inductance and at a much higher frequency. The small inductor helps by increasing the slew rate of the current, and thereby minimizing the current supplied by the output capacitors and decreasing the voltage spike at the load side. The introduction of the transformer in the ATVC circuit helps in reducing the current in the switches, which will decrease the power loss. On the other hand, the lower turns ratio at the secondary side will increase the current supplied to the load.

The techniques mentioned so far focus on increasing the transient response during load change. Nevertheless, they suffer from a small duty cycle resulting from stepping the 12 Volts input down to the required one Volt at the load side. Efforts have been directed into non-isolated, transformer-based buck topologies to enlarge the duty cycle, including tapped inductor buck, active-clamp couple buck and forward and push pull converters to name a few [27- 31].

1.2 Thesis Outline

A concise overview of this work is presented in Chapter One, in which the problem is briefly addressed and the two major techniques to solve the problem are stated. Investigation of an Intel roadmap shows the trend of lowering the output voltage and increasing the current and power densities of future VRM. Efforts took two research directions in redesigning the current VRM to meet the new requirements of the next generation processors.

Chapter Two introduces the background of the work, discussing in detail all aspects of the VRM challenges and limitations. Two main output voltage spikes occur at the load side, and passive and active methods were deeply examined to alleviate such spikes. The passive method of adding more capacitors is limited by space and cost. Active compensation methods, which vary from current to voltage injection, are studied in Chapter Two. In Section 2.1, the complete scenario of VRM requirements is presented and the accompanied challenges are discussed. Section 2.2 reviews prior arts, which were dedicated to solving the problem by passive and active means. Transformer-based topologies are discussed in Section 2.3.

The new proposed topology, which is based on a half-bridge buck, is given in Chapter Three. The half-bridge buck offers an extended duty cycle and avoids the problems associated with small duty ratios. Detailed discussion and analysis are given in this chapter.

Chapter Four gives an insight on the magnetic part of the half-bridge buck presented earlier and provides a design approach and experimental results. The half-bridge buck has a flyback transformer as the core of its operation. Simulation results

show the severe impact of leakage on converter efficiency and the need for a solid and tight magnetic design.

Multi-input converters are introduced in Chapter Five with a complete small-signal modeling of a two-input converter. Small-signal modeling is inevitable in control design. A two-phase buck with different inputs is analyzed in detail. Circuit averaging and Middlebrook's state space averaging are applied, and consequently, a small-signal model is derived.

The conclusion and future work are summarized in Chapter Six.

CHAPTER 2

LITERATURE REVIEW

2.1 Background

Roadmaps of semiconductor and microprocessor companies continue to call for the lowering of the output voltage of the VRM to values less than one Volt and are expected to even decrease more [1]. Meanwhile, VRM switching frequency is pushed higher for the purposes of decreasing the component size and enhancing the transient response.

The computer processor is connected to the motherboard through a socket, which serves as an interface between the motherboard and the processor, and it allows for electrical connectivity and easy removal to replace the processor when needed [2]. Socketing technology has moved from the micro Pin Grid Array (mPGA) to the Land Grid Array (LGA) because of some limitations that are beyond the scope of this thesis [2]. Intensive efforts at Intel have produced the LGA 775 socket [2].

Tables 2.1.1 and 2.1.2 show Intel Motherboard versions on LGA 775 and mPGA 478 sockets [3].

Table 2.1.1 Intel Desktop Motherboards on LGA 775

Chipset	Intel Desktop Motherboard
Intel 915GV Express Chipset	Intel Desktop board D915GLVG
Intel 915 G Express Chipset	Intel Desktop board D915GUX

Table 2.1.2 Intel Desktop Motherboards on mPGA 478

Chipset	Intel Desktop Motherboard
Intel 865PE Chipset	Intel Desktop board D865 PESO
Intel 865P Chipset	Intel Desktop board D865 PCK
	Intel Desktop board D865 PCD

The difference between sockets PGA and LGA is that LGA has smaller fewer number of pins and a reduced cost. Figures 2.1.1 and 2.1.2 show the two different sockets [2]. Figure 2.1.3, shows both mPGA and LGA packages [2].

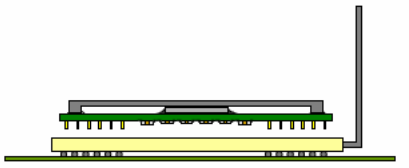

Figure 2.1.1 PGA Package and Socket

Figure 2.1.2 LGA Package and Socket

Figure 2.1.3 LGA 775 and mPGA 478 Packages

The package consists of a socket housing with stitched contacts, a stiffener plate, a load plate and a load lever as shown in Figure 2.1.4.

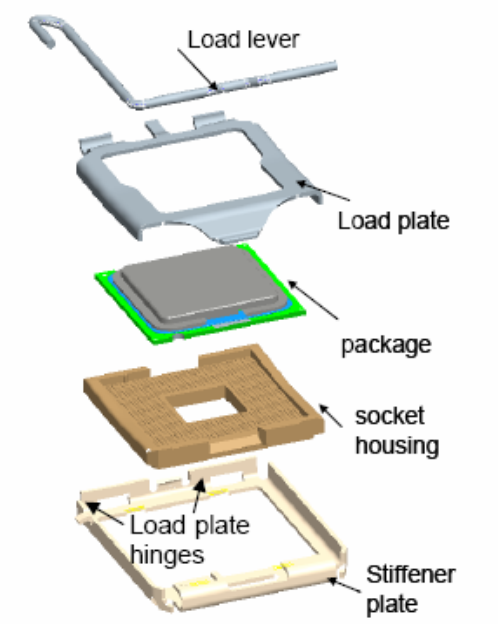

Figure 2.1.4 LGA Socket Assembly View

Figure 2.1.5 shows a picture of a complete assembly of an Intel motherboard D915GUX version 10.1 with VRM components and LGA package [4-5].

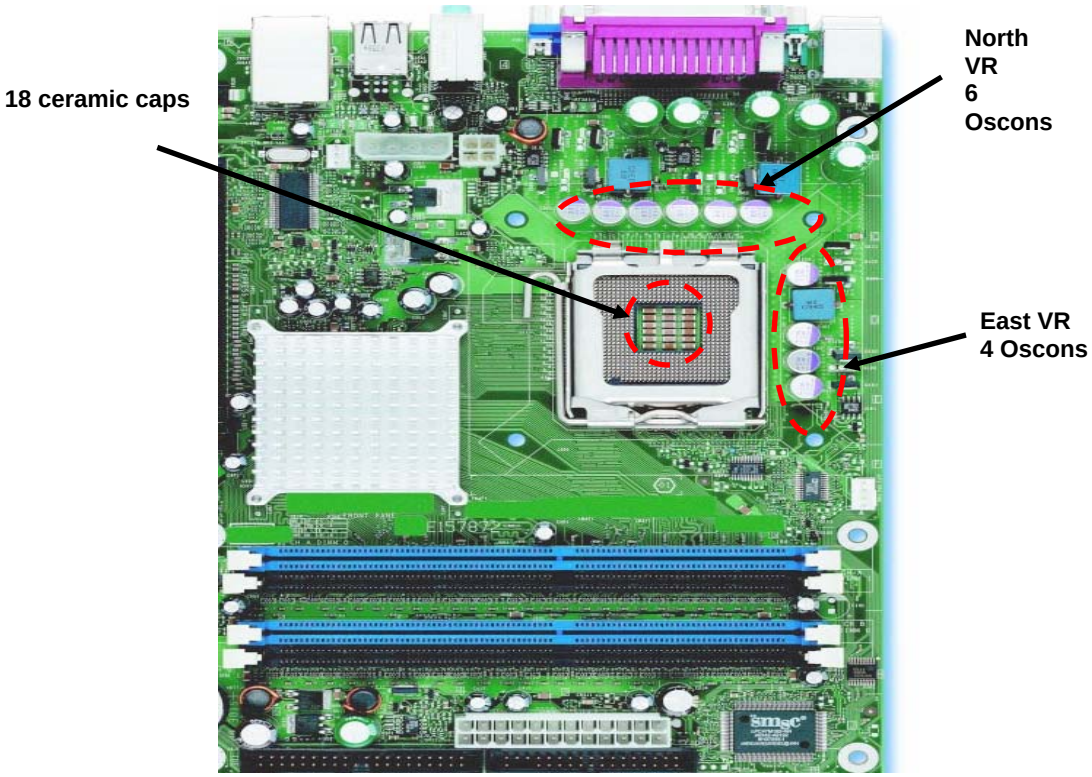

Figure 2.1.5 Intel Desktop Motherboard

The overall circuit can be depicted in the block diagram shown in Figure 2.1.6.

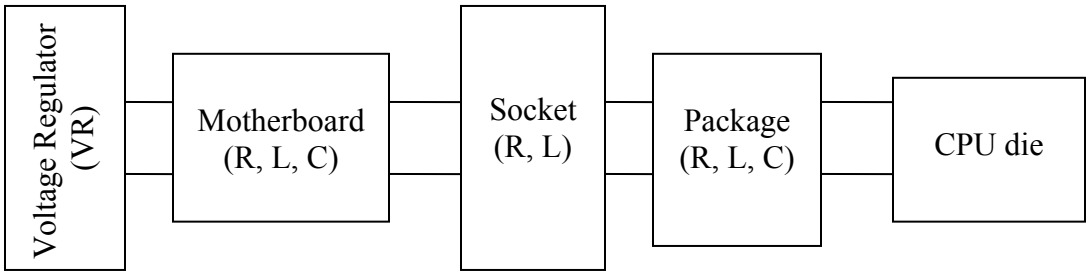

Figure 2.1.6 A Block Diagram of a Motherboard

According to the International Technology Roadmap for Semiconductors (ITRS), Semiconductor Industry Association (SIA) and Intel's roadmap, the operating voltage is

decreasing continuously to values less than One Volt along with increasing the processor current exceeding 100A.

Some example specifications for Intel microprocessor are shown in Table 2.1.3 [6-9].

Table 2.1.3 Example Specifications for Intel Microprocessors

Parameter/Processor	Pentium® II	Pentium® III	Pentium® 4
Clock Speed (Hz)	233M 266M 300M	600M 550M 450M	1.4G 1.5G 1.7G
Core Voltage (V) min. /max.	2.8	2.05 2.00	1.56/1.7 1.555/1.7 1.53/1.7
Converter Voltage (V) min. /max.	-	-	1.627/1.7 1.625/1.7 1.61/1.7
Core Current (A)	11.8 12.7 14.2	17.8 17.0 14.5	-
Converter Current (A)	-	-	40.6 43.0 52.7
Core Current Slew Rate ($A/\mu s$)	30	20	-
Converter Current Slew Rate ($A/\mu s$)	-	-	50

Inspecting the numbers in Table 2.1.3, it can be noted that there is a huge current increase from 14A in Pentium II to above 50A in Pentium 4 versus the drop in voltage from 2.8V to 1.6V in the same processors versions mentioned above.

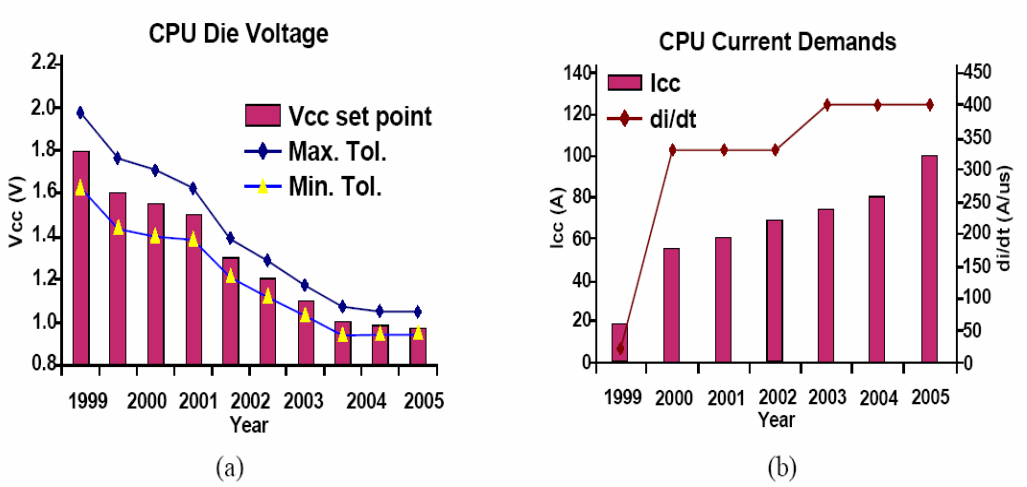

Figure 2.1.7 Intel Roadmap of a 32-bit CPU showing (a) CPU Die Voltage and (b) Current Demand and Slew Rate

Figure 2.1.7 confirms the preceding discussion; the CPU will be expected to run with a voltage below the one Volt level and currents hitting the 120A as fast as 400A/us [10].

The main power source available on the motherboard provides three power levels: + 12V, +5V and +3.3 V output as depicted in Fig. 2.1.8.

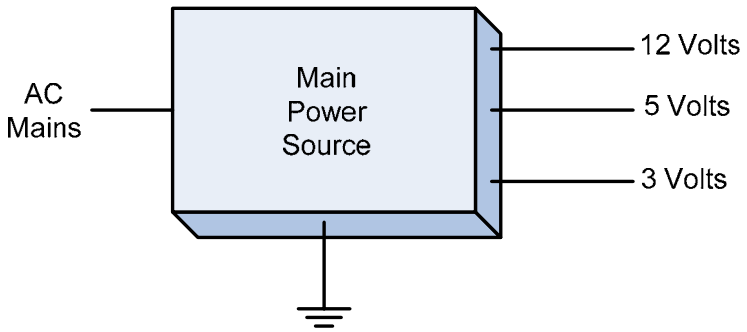

Figure 2.1.8 A Conceptual Block of the Motherboard Main Power Source

As seen in the Intel roadmap shown in Fig. 2.1.7, in the late 1990s, the CPU needed 2 Volts, which were initially supplied from the 5 Volts port [9]. However, the resistive and inductive parasitic elements between the power source, known as the silver box, and the CPU dramatically affect the quantity, as well as the quality at the CPU input, -i.e. the load. With the increasing trend of lowering the output voltage, this power flow scheme could not be accepted or used any longer. Hence, the point of load (POL) converter, which was placed close enough to the load, replaced the previous power flow.

Again, the centralized silver box was no longer used due to the parasitic effect it added, which placed a restriction on further lowering of the output voltage. Consequently, dedicated dc-dc converters came to play an important role in the CPU industry. VRMs became the center of the motherboard. With the continuous decrease in the CPU voltage, and an analogous increase in the current, the input voltage shifted to the 12 Volts port [9]

The most simple and logical method to achieve the low output voltage from the 12 Volts input is to have a voltage source stepped down to the required CPU voltage level. The buck converter is therefore the cornerstone in any VRM. A buck converter is merely a level stepping-down circuit consisting of a switching network, which is mainly N-channel MOSFET and a low pass filter, as shown in Figure 2.1.9, where the input voltage is stepped down in accordance with the switching mechanism to produce an output voltage that is less than the input by a factor equal to the duty cycle of the main switch. The switching part of the circuit is followed by a filtering network to smooth out the spikes and supply the load with a clean output voltage of the desired value. The

control variable in this case is the duty cycle; in other words, the output voltage is ideally proportional to the duty cycle.

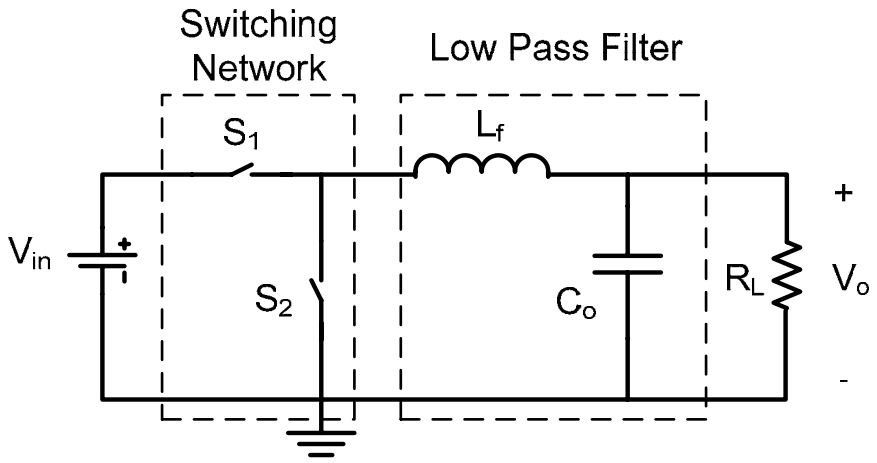

Figure 2.1.9 A Simple Basic Buck Converter

Central Processing Units (CPUs) in computers are treated as critical loads in VRM literature. The challenges VRM designers face are compacted in two aspects:

1) The clean, constant and low-output voltage the CPU needs, together with high current and power densities, add thermal issues to the design complexity.

2) The fast transient response is equally important as in the CPU realm.

With the above design considerations in mind, it is obvious that a single-phase buck converter will not meet the CPU requirements due to the large inductor ripples that the single buck presents. The shift to interleaved multiphase buck was inevitable [23].

An interleaved multiphase buck converter efficiently replaced its single phase counterpart improving the transient response and increasing the efficiency. Figure 2.1.10, shows an N phase buck consisting of identical N phases shifted by 360^{o} / N. This control scheme obviously decreases the output current ripples. The lower the current ripple, the

lower the rms current, which means the lower the losses. This can also mean better efficiency and better thermal management.

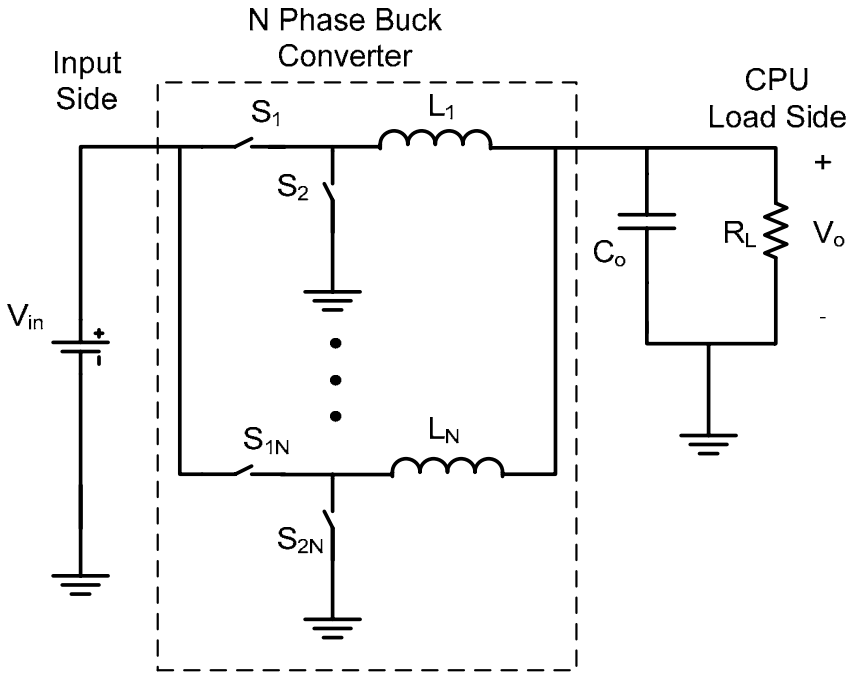

Figure 2.1.10 An Interleaved N phase Buck Converter

As discussed earlier, the input to the VRM has been switched from the 5 Volt to the 12 Volt port. Thus, there is a 12 DC Voltage source at the input of a multiphase buck converter that supplies the processor of the motherboard with the low voltage it needs. The lower the output voltage, the less the power consumption and the faster the data transfer becomes. Therefore, the future trend is to further decrease the voltage and consequently increase the current. The amount of data handled by the processor varies with the number of programs being run that comprise the processor load. The load may not only change from no load to full load, but it can do so with a very high slew rate up to 120A/us [10].

When the load change occurs, whether step-up or down, the difference of the current should be handled. In the case of step-up load, the extreme scenario is when the load changes from no load to full load. When this happens, the output voltage tends to decrease, but in order to maintain a constant output voltage, current injection will be needed from the source which leads to increase the duty cycle to be able to supply the load with the current it needs. Before the VRM supplies the output load completely, the output capacitor will help in supplying the current needed, and thus a voltage spike will occur at the output voltage. In an analogous way, when step-down load happens, energy stored in the filter inductor needs be recovered and thus the off time — no source period — increases until all the energy that was stored in the filter inductor is consumed.

In the above cases, the controller, the LC filter, and the compensation network delay times will deteriorate the voltage spike at the output. In short, there are two voltage spikes that appear at the output, and their presence is a problem and their remedy depends on the understanding of their original source. The first voltage spike is determined by the capacitor parasitic ESR and ESL and also by the output current slew rate SR_o. The second spike is determined by the energy stored in the inductor.

Only passive methods can reduce the first voltage spike by adding more output capacitors to reduce their equivalent series resistance and inductance, which is cost and space limited. As seen in Figure 2.1.5, many OSCON and ceramic capacitors are dwelled close to the CPU and occupy a lot of space on the motherboard [4, 5].

The first voltage spike is almost constant for a certain output filter inductance value, and it is hardly dependant on the inductor value and mainly relies on the parasitic values of the capacitor. The only way of eliminating the spike is to add more output

capacitors in parallel, thus decreasing the ESR and ESL. This passive method is limited by the available free space on the motherboard and by the cost.

The second spike is controllable, and is highly dependent on the filter inductance. The smaller the inductor the faster the transient response, and thus, the less the charge and the smaller the voltage spike becomes. In other words, the first voltage spike dominates when a small filter inductor is used at which the second spike is eliminated due to the high transient response. Similarly, the larger the inductor value, the slower the transient response and the larger the voltage spike. Thus, the second spike dominates with a large filter inductance.

Consequently, there are two design methods: the first method is an ESR- and ESL-based transient design with a small filter inductance [19]. The second design method is an energy-based design procedure with a large output filter inductance. As mentioned earlier, those spikes are deteriorated with non-ideal controllers. All practical controllers suffer from delay times, which when added to the delays resulting from IC propagation time and LC network will have even more impact on increasing the spikes.

2.2 Prior Arts in High Slew Rate VRM

This section presents previous approaches to designing VRMs to meet the stringent requirements of the VRM design. There are two main fields in VRM: non-isolated topologies which focus on enhancing the transient response [11-19, 20-24, 27-28], and isolated topologies in which a transformer is applied to extend the duty cycle [25-29]. These two VRM topologies are discussed in this section.

2.2.1 Non Isolated Technologies

2.2.1-I Current Compensators

As stated before, the problem of the inability of the main voltage regulator in supplying the load with the needed current under-load changes is of great concern. Therefore, current compensators are based on the idea of injecting the current needed during transients instead of relying on the output capacitors to provide the load current. Current compensation injects current in two modes: linear mode current compensators, [11-13] and switching mode current compensators, [15-16] as shown in Figures 2.2.1 and 2.2.2, respectively.

In both topologies, the unbalanced current is supplied by the extra converter and results in high-current stresses.

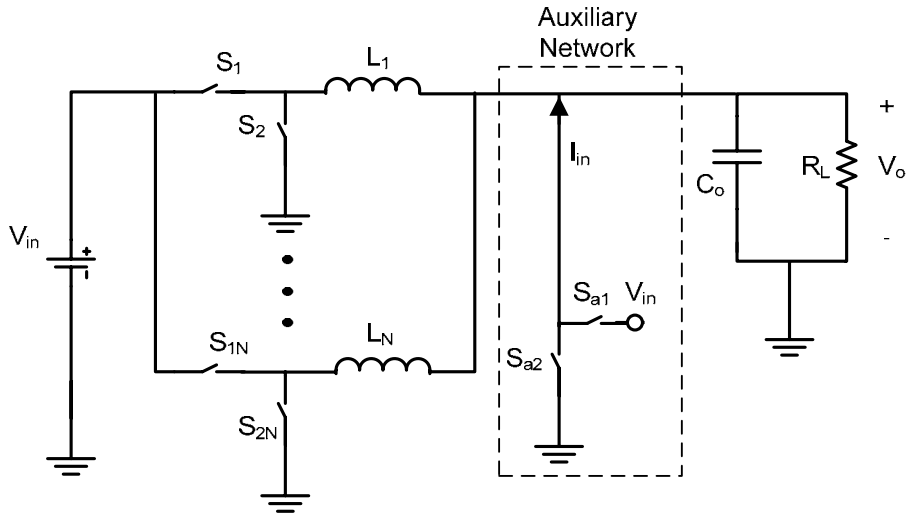

Figure 2.2.1 Linear Mode Current Compensator Topology

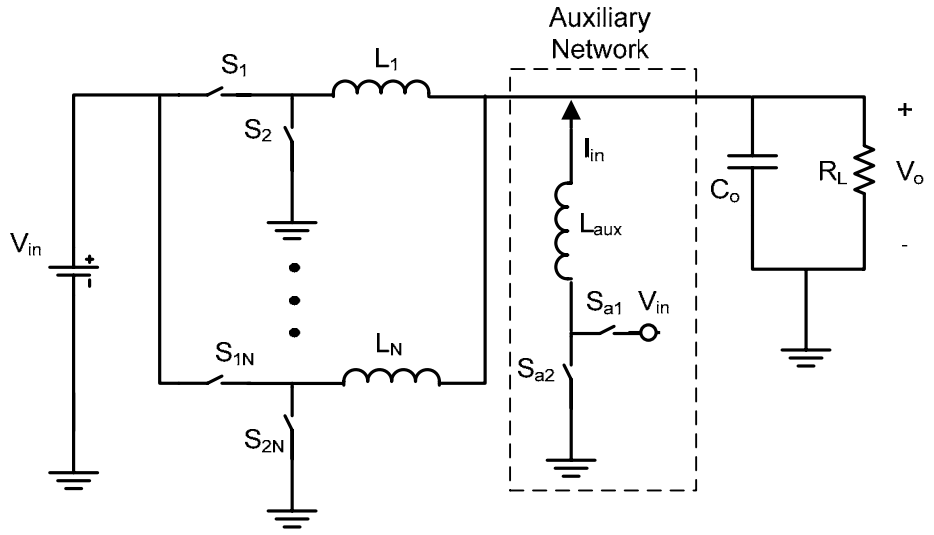

Figure 2.2.2 Switching Mode Current Compensator Topology

The auxiliary circuit provides the unbalanced current in either a linear or a switching mode. The main disadvantage in the linear compensator is the conduction losses, and in the switching compensator, the disadvantage is the switching losses that result in a major decrease in efficiency of the overall converter, making current compensators very difficult in low-voltage and high-current applications.

2.2.1-II Stepping Inductance VRM

Figure 2.2.3 shows the basic configuration of the stepping inductance where, inductor L_r is smaller than L_o [14].

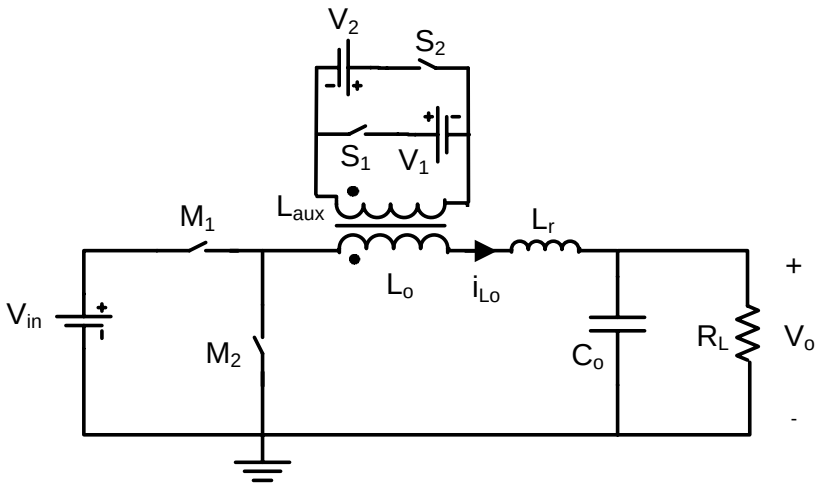

Figure 2.2.3 The Basic Configuration of the Stepping Inductance Circuit

S_1 is programmed to turn on during increased-load transients and S_2 turns on during decreased-load transients to short circuit the larger inductor L_o in both cases [14]. When S_1 turns on, the net inductance decreases, leaving the smaller one to be used, and this will increase the output inductor slew rate during that period, resulting in a reduced voltage deviation [14].

At step-up load, the output voltage decreases, and as a result, S_1 turns on, which also decreases the output inductance. This will increase its slew rate until the current in the leakage inductance reaches the output current, and then V_o stops decreasing and starts to increase. When it reaches a certain value, S_1 turns off, and once again, L_o takes over the output inductance and its current i_{Lo} dominates. However, since it is still less than the output-load current, the output voltage will decrease again, and consequently, S_1 will turn on once the output voltage reaches a value less than a certain threshold. This oscillatory on and off switching of S_1 stops once the i_{Lo} equals the output load current I_o [14].

Having a voltage source, V_1 serves in keeping the large inductor current increasing during the time period when M_1 and S_1 are on. This further decreases the transient period and results in a faster transient response to maintain a constant output voltage to the load. The same operation takes place in a reverse order at load step-down switching S2 on and off [14].

2.2.1-III Active Transient Voltage Compensators (ATVC)

Active transient voltage compensator (ATVC) approaches the problem in a similar yet opposite way. It relies on injecting voltage source instead of current. Figure 2.2.4 shows the ATVC circuit [25].

ATVC simply acts as another buck converter, with smaller inductance and at much higher frequency. The small inductor helps to increase the slew rate of the current and thus minimizing the difference between the output current and the current from the main VRM. Once this difference decreases, the output capacitor charge decreases and leads to lower voltage spike at the output.

As shown in Figure 2.2.4, ATVC consists of a transformer with N turn ratio, two auxiliary switches S_{a1} and S_{a2} and a voltage source V_1 that can be of any value.

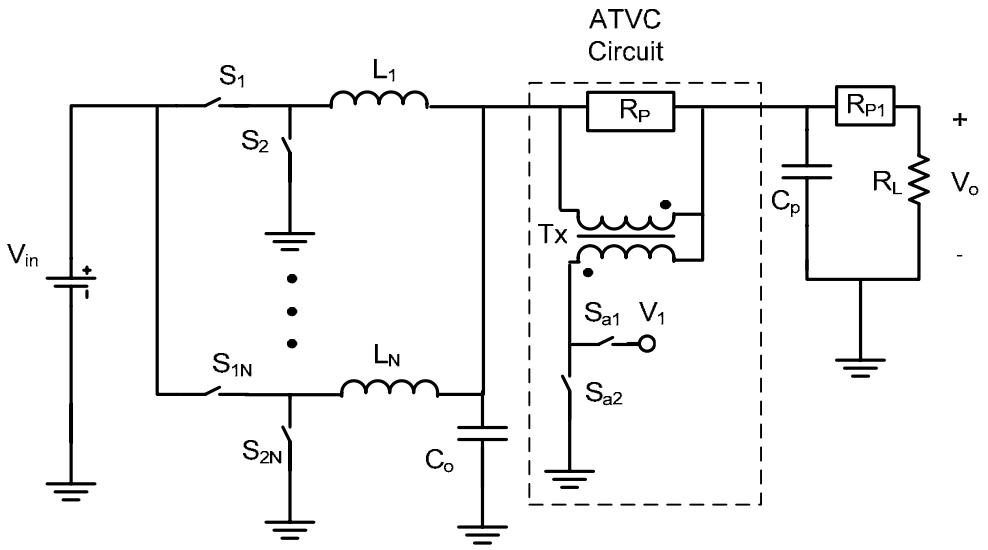

Figure 2.2.4 ATVC Circuit

The introduction of the transformer helps in decreasing the current in the switches. This will decrease the power loss, from which the current compensation methods suffer. On the other hand, the lower turn ratio at the secondary will increase the current supplied to the load. The main VRM operates at relatively low frequencies maintaining good efficiency values.

ATVC comes in two configurations: series and parallel, which are shown in Figures 2.2.5 and 2.2.6, respectively.

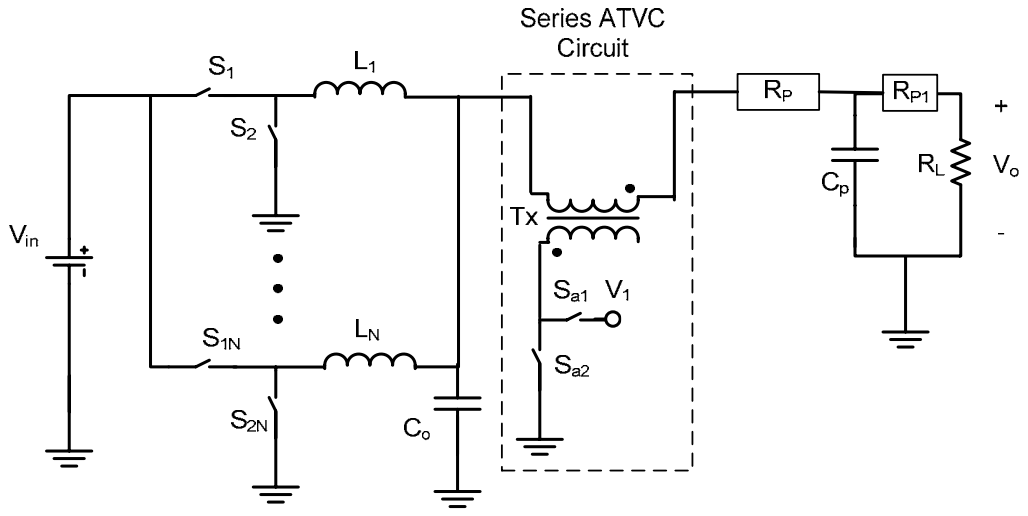

Figure 2.2.5 Series ATVC Implementation Circuit

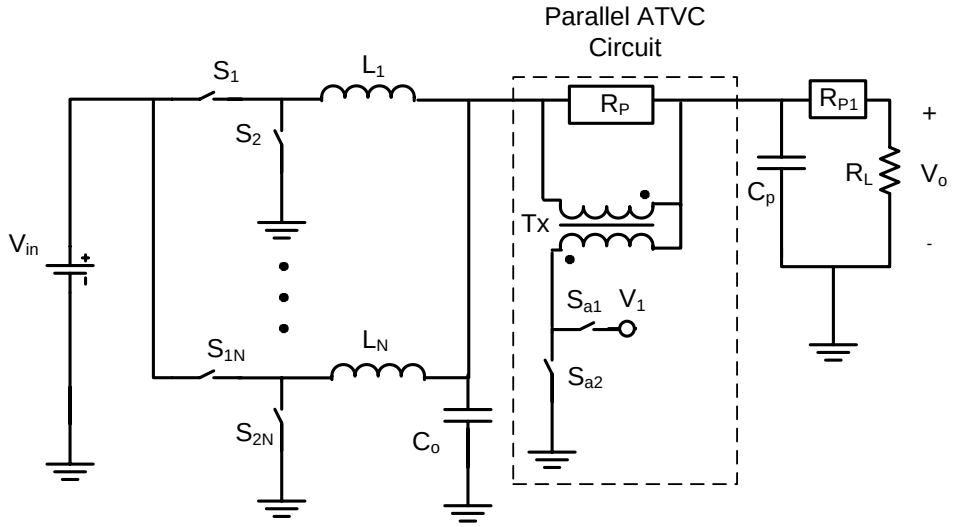

Figure 2.2.6 Parallel ATVC Implementation Circuit

The only difference between series and parallel ATVC is that series ATVC handles all the unbalanced current between the main VRM and the load, whereas parallel ATVC carries only a portion of that current according to the voltage divider (K) of R_p and R_{LM}, following the equation;

$$K = \frac{R_P}{\left(R_P + R_{LM}\right)}$$

Where:

R_p is the equivalent resistance of the traces and the parasitic,

and,

R_{LM} is the magnetizing inductance resistance as shown in Figure 2.2.7.

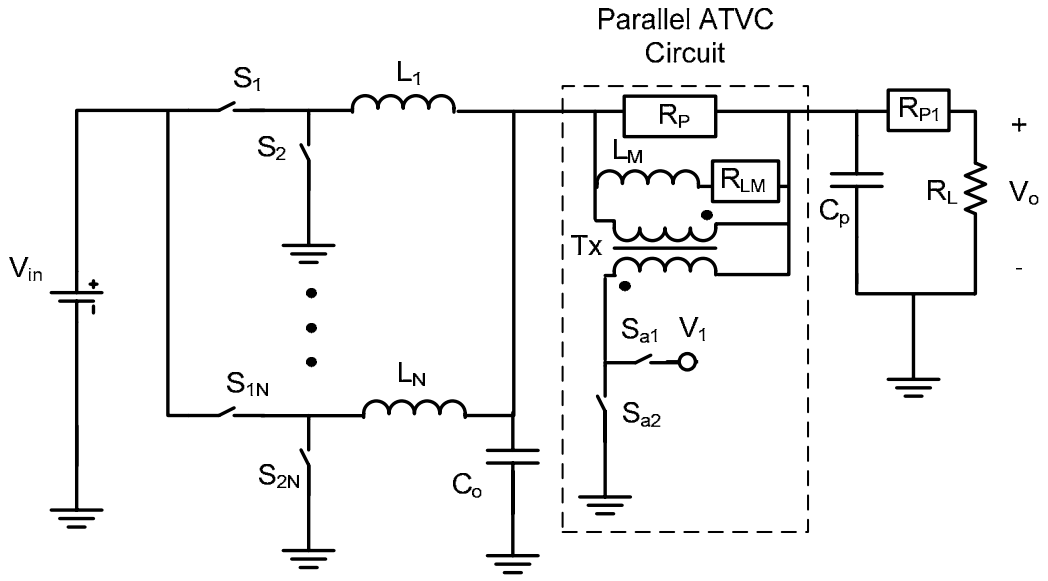

Figure 2.2.7 Conceptual Parallel ATVC Implementation Circuit

Hence, parallel ATVC current stress is less than that in series ATVC. Also, series ATVC increases the static load line, and yet, the transient load line improvements of both ATVC types are the same.

The complete cycle of ATVC can be divided into three modes of operation: current injection mode, steady-state and energy recovery mode.

1) Current Injection Mode

This is the period of time during which the load current increases abruptly. Consequently, the output voltage decreases according to the power conservation during

this mode when ATVC kicks in to help the main VRM in supplying the current needed at the load side.

The small leakage inductance is what is needed to increase the slew rate of the current injected by the ATVC, so that the current is quickly supplied to the load without the help of the output capacitors, decreasing the charge difference and consequently decreasing the voltage spikes at the output. When the load current increases, the output voltage will consequently decrease to a certain limit when S_{a1} turns on. At this instance, ATVC is activated, and the current supplying the load is the addition of the current from the main VRM plus the current from ATVC. Due to the small leakage inductance, the current rises very quickly with a high slew rate.

The transition between the on and off states of S_{a1} and off and on states of S_{a2} will continue until the magnetizing current (main VRM) reaches the output needed current and the output voltage reaches V_o. This period of time is what is known as current injection period.

2) Steady-State Mode

Once the current supplied to the load from the main VRM, along with the added current from the ATVC side, reaches the current needed at the output, then the ATVC can go into standby mode.

It should be noted here that with the introduction of the transformer with N turns ratio, ATVC handles a current (1+N) times less than that handled by the current compensators thus reducing the conduction and the switching losses. In addition, it provides a current (1+N) higher than that of the previous arts with same filter inductance.

During the steady-state mode of operation both auxiliary switches S_{a1} and S_{a2} turn off. The body diode of S_{a2} should not turn on during this mode and this can be guaranteed by satisfying the following condition: $N \cdot V_S < Vo + V_D$

Where: Vs is the secondary voltage of the transformer and V_D is the on-state voltage drop of the body diode of S_{a2}. Since the voltage drop across R_p is small, the above condition can be met easily.

3) Energy Recovery Mode

The last mode of operation is the energy recovery mode. During this period, the load current steps down with a very large negative slope, thus the output voltage increases. The excess energy should be recovered, and this is done by making the ATVC act as a boost converter by controlling S_{a2}.

This mode is the mirror opposite of the current injection mode in that the same logic is applied, but instead of increasing the current, the direction is taken into recovering the energy (discharging the current in the inductors feeding it back to the supply voltages).

This mode will continue until the output voltage decreases to the required value.

In summary, ATVC injects high slew rate current in step-up load and recycles extra energy stored in the VRM filter inductor into its input voltage V_I during step-down load.

2.2.2 Transformer Based Non-Isolated DC-DC Converters

As mentioned earlier, a conventional step-down Buck converter is the building block of any VRM, but due to the high output ripple, interleaved-multiphase buck replaced the simple single-phase buck with the same 12 Volts input.

The stepping down from the 12 Volts input to the required one Volt at the load side entails a very small duty cycle, and added to that is the high switching frequency that results in some associated problems and low efficiency.

Efforts have been directed into non-isolated transformer-based buck topologies to solve the above mentioned problems, including tapped inductor buck, active-clamp couple buck and forward and push pull converters to name a few [26-29].

2.2.2-I A Deeper Insight into a Small Duty Cycle

The major problem associated with low output voltage and high switching frequency is having a small duty cycle as mentioned above. This is considered the source of all other accompanied limitations as listed below [29-32]:

1- A fast comparator is needed to create the small driving signal, which will increase the cost.

2- The top switch conduction period decreases with the increasing of the switching frequency, which may cause a malfunction of the converter, known as gate drive problems, and that cause an increase in the switching losses of the top switch and consequently increase the conduction loss of the lower switch.

3- Asymmetric transient response causes a clear difference in the step-up and step-down speeds.

4- Efficiency will drop due to the high peak current that is associated with the small duty cycle and the long conduction period of the bottom body diode switch.

The problems associated with a small duty cycle are of great importance especially with the accompanied increase of switching frequencies to improve the transient response and to decrease the size. To address the small duty cycle issue, designers used coupled magnetic configuration including tapped inductor, coupled buck converters [26, 27] and the non-isolated Push Pull Converter [28, 32].

The straight forward solution to the above problem is to add another control parameter besides the duty cycle, which allows us to decrease the output voltage and maintain an optimum duty cycle and consequently avoids the problems related to small-duty ratios.

Transformer-based non isolated-dc-dc converters were foreseeable and an expected solution. It helps achieve the desired low-output voltage and, at the same time, sustain a relatively high duty cycle with better ripple cancellation and lower switching currents [32].

It is essential here to stress the fact that for many 12 V microprocessor power supplies, which are the subject of this study, there is no isolation required [32]. This explains why VRM designers are inclined towards transformer-based yet non-isolated dc-dc converters.

Two of the VRM requirements come back to back. The output voltage is in continuous decrease and the need for smaller passive components and faster transient response dictate the shift to higher switching frequencies. But, this doesn't come easily or empty handed, as the lower the output voltage, the lower the duty cycle. With the necessity of higher switching frequency, the efficiency will go down as well. Hence, there is justification to add a transformer to create a new VRM family designated for the

transformer-based non-isolated dc-dc converter, which includes: the tapped inductor buck converter [26] (with its twin circuit with lossless clamp circuit [29]) the active clamp couple buck converter [27], push pull buck [28] and the non-isolated half-bridge [29].

Each of these converters adds an advantage and a contribution for solving the above mentioned problems. But a well-known trade off issue is that it also fails in one aspect. The following is a brief listing of the pros and cons of the above converters.

2.2.2-II Tapped Inductor (TI) Buck

As with the case of the stepping inductance, the idea is to have a smaller inductance value to enhance the transient response. The two windings w_1 and w_2 shown in Figure 2.2.8 constitute the overall inductance in the charging period, whereas the small winding, w_2, takes over during the discharging period [26, 29].

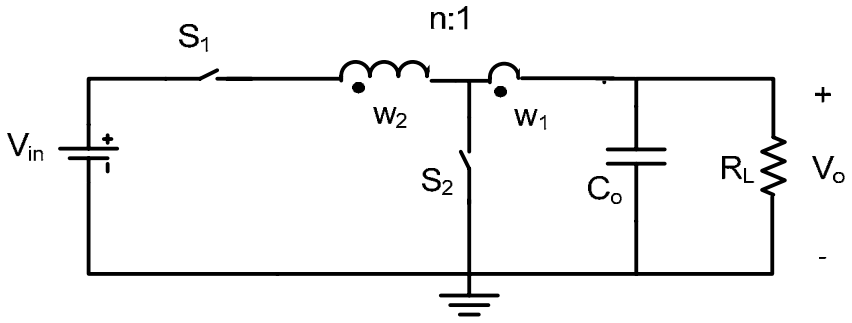

Figure 2.2.8 The TI-Buck Circuit

The advantages of the tapped inductance are summarized as follows:

1- The availability of another parameter to control the output voltage besides the duty cycle allows for a better (wider) duty cycle according to the equation below [26, 29]:

$$D = \frac{nV_o}{V_{in} + (n-1)V_o}$$

This allows for solving the problem by extending the duty cycle.

2- The mismatch between the transient response speeds can be solved by precisely designing for w_1 and w_2 [26, 29].

3- Efficiency is also claimed to be better due to the n factor that decreases the current that passes through the top switch, and the enlarged duty cycle achieved will decrease the conduction period of the bottom switch body diode. These two consequences will increase the efficiency.

On the other hand, the TI-Buck suffers from limitations that counteract its above list of advantages.

The top switch driving scheme becomes a challenge, since it will not be as easy as the conventional buck. The second severe limitation is due to leakage energy. The leakage energy of winding w_2 will be lost in the resonant circuit of w_2, and the top switch capacitor creates a high voltage spike across the switch, which decreases the efficiency and generates the possibility of destroying the top switch. Thus, the twin circuit of the TI-buck with the added clamp circuit offered a solution for the leakage energy.

2.2.2-III TI-Buck with Lossless Clamp Circuit

The TI-buck shown in Figure 2.2.8 was rearranged to form the converter shown in Figure 2.2.9. This new arrangement will solve the gate driving problem simply by using the boot strap circuit for the top switch S_1 [29].

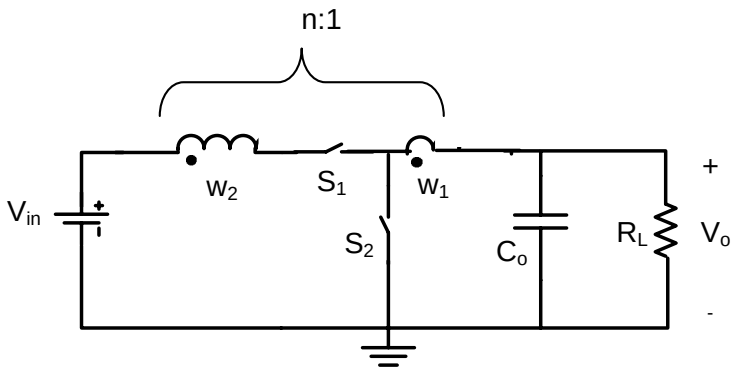

Figure 2.2.9 Rearranged TI-Buck

Adding a lossless circuit to trap the leakage energy resulted in the circuit shown in Figure 2.2.10.

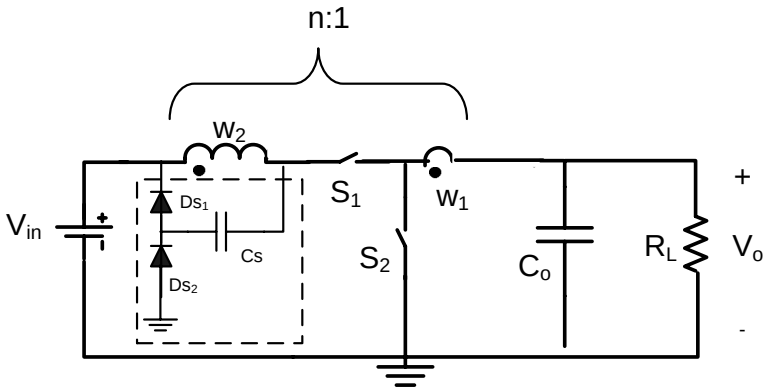

Figure 2.2.10 The TI-Buck with Lossless Clamp Circuit

The modified TI-Buck solves the problem of the basic TI-Buck but with the added complexity of the magnetic design plus the losses of the two added diodes in the clamp circuit.

Therefore, the solution offered by the modified TI-Buck with the lossless clamp circuit was equally leveled by the disadvantages of the magnetic design difficulty and the clamp diodes losses.

2.2.2-IV The Active Clamp Couple Buck Converter

As discussed before, the synchronous multiphase buck became the building block of the VRM for the benefits of transient response improvement and output current ripple cancellation, which help to decrease the output capacitance.

Nevertheless, the small duty cycle limits the ripple cancellation gained unless more phases are added with increased complexity.

The other problem addressed is the asymmetric transient response. Reducing the inductance value and decreasing the bandwidth are two approaches adapted to achieve symmetric transient response on one side. But on the other pane of the balance, these approaches decrease the efficiency and increase the output capacitance [27].

The TI-Buck offers a new parameter that helps in getting the transient responses closer to being symmetric. This parameter is the turn ratio of the two windings of the inductance.

The parameter n controls the slopes of the charging and discharging periods. Therefore, the design challenge is to get the precise value of the turn ratio n of the two

windings w_1 and w_2, which makes the slopes during the two intervals of the switching period equal, resulting in symmetric transients [26- 27, 29].

Increasing the duty cycle will go side-by-side with decreasing the current in the top switch i_{s1}. Figure 2.2.11 shows a comparison between the top switch current i_{s1} with small duty cycle D_1 and higher duty cycle D_2. This can be translated also into lower losses and higher efficiency.

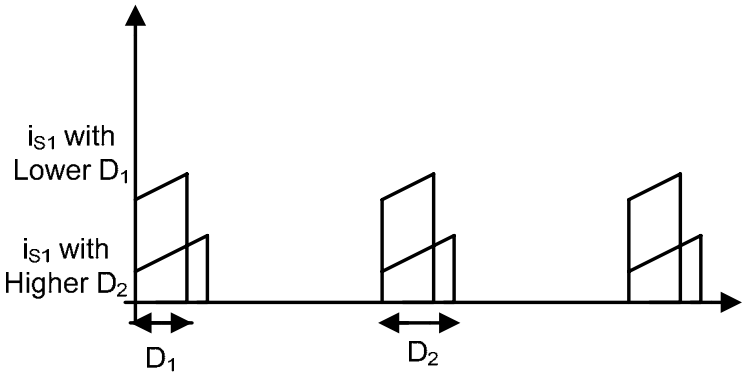

Figure 2.2.11 Top Switch Current and Duty Cycle Relation

Again, the other shortcoming suffered by the TI-buck is the leakage energy, which is dissipated into the top switch capacitor and creates a voltage spike across the switch and could possibly impair the switch. To overcome this problem, the 30V MOSFET is no longer suitable for use and should be replaced with a higher voltage switch, which can be stated as higher R_{dson} which results in higher conduction losses [27].

Many designers faced the challenge of coming up with a lossless snubber circuit to alleviate the spike without negatively affecting either the cost of adding more components or the efficiency.

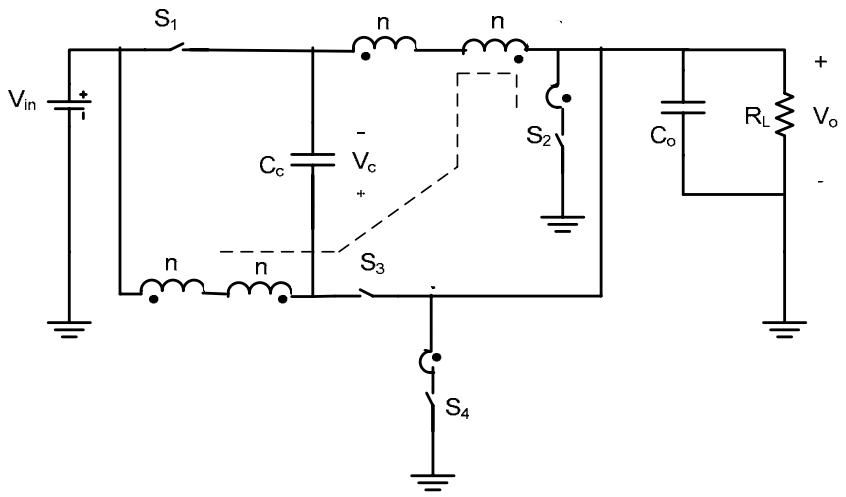

Figure 2.2.12 The Active Clamp Couple Buck Converter

One of the proposed snubbers is the active clamp couple buck shown in Figure 2.2.12. The complexity of the control and the magnetic design is expected including the added cost and decreased efficiency.

2.2.2-V A Non-Isolated Half-bridge DC-DC Converter

The non-isolated half-bridge converter offers the following advantages: lower losses accompanied with the lower peak current and higher duty cycle through the integration of the transformer with its turn ratio and the faster turn off of S_2 [30]. The circuit configuration is shown in Figure 2.2.13.

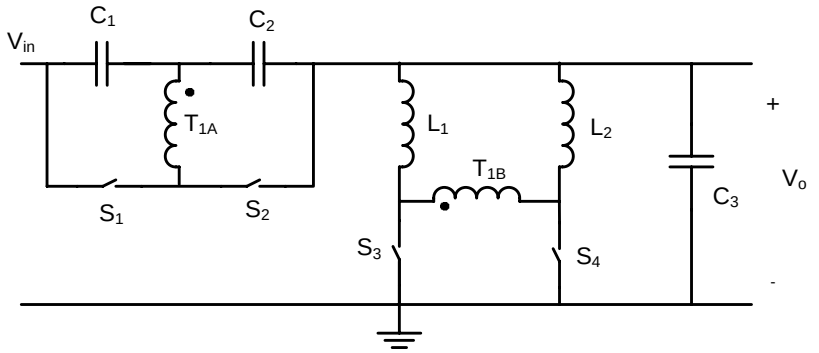

Figure 2.2.13 Non-Isolated Half-bridge Converter

As with the case in the previously discussed topologies, the non-isolated half-bridge doesn't offer the above listed advantages for free. The lower current in the primary branch dictates a higher current in the secondary and is translated into higher conduction losses. A transformer and an inductor are added, which increase the cost as well as the associated losses in the core and cupper besides adding to the design complexity [30].

2.3 Chapter Recap

Future VRMs are heading into lower voltage, higher current and power densities in addition to shifting the switching frequency to ranges as high as mega Hertz in the aim of decreasing the size and enhancing the transient response. Today's converters suffer from two spikes at the output. The first voltage spike is almost uncontrollable but can be suppressed by paralleling different kinds of capacitors. However, this passive method is limited by cost and space.

The second voltage spike is determined by the energy stored in the inductor and there are different approaches to lowering it. But along with lowering it, there is a big tradeoff and design challenge. The smaller the inductor, the faster the response, but the ripple becomes an issue. The higher bandwidth and the smaller spike shift the switching frequency to higher band values, which lead to higher switching losses and therefore lower efficiencies.

Efforts have been made to alleviate the second voltage spike. The conventional current compensation was an attractive method of injecting high slew rate current in step-up load and absorbing the voltage overshoot in step-down load whether by linear or switching modes. The drawback is the large current stress that results in high conduction loss in linear mode and high switching loss in the switching mode.

Active Transient Voltage Compensator (ATVC) is a voltage injection method. The power loss is reduced due to the transformer that is being introduced as a vital element in the circuit of the ATVC. It relies on injecting high slew rate current during step-up load and energy recovery in step-down load.

ATVC activates only during transients with several MHz operating frequencies, whereas the main VRM remains at relatively lower frequency range to maintain better efficiency.

Large delay times inherited in the controller, compensation network and the LC filter deteriorate the voltage spikes even more. Now, all attention has been directed to enhance the controller design.

Finally, ATVC has improved AC load line mainly for the suppression of the second voltage spike with small power loss. It is a very attractive way in high slew rate applications.

The lower the output voltage, the smaller the duty cycle and the lower the efficiency will be. Many design approaches were taken into consideration including adding another output voltage control parameter. The most logical solution was to add a transformer while maintaining the non-isolation requirement of the VRM.

Tapped Inductor Buck was the original solution on which many other topologies were based, and clamp circuits were designed to solve the leakage energy problem. Other topologies were derived from the half-bridge or push pull converters.

Advantages were addressed together with its tail-to-tail limitations.

CHAPTER 3

HALF-BRIDGE BUCK VOLTAGE REGULATOR

3.1 Introduction

Intel roadmap predicts that future VRM will operate at low output voltage hitting the one Volt limit with an increase in current and power densities. Smaller output voltage translates into smaller duty cycle, and this impairs the efficiency of the converter due to the problems discussed in Chapter Two. In non-isolated topologies, D is used to decrease the output voltage. However, for very small output voltage requirements, D becomes very small, and this will result in high current and voltage stresses and therefore high switching losses. A transformer is embedded in non-isolated topologies to add another output voltage level control with an optimized D and therefore provide lower switching losses and higher efficiencies.

The Half-bridge Buck Converter (HBBC) presented in this chapter offers an added control parameter allowing an extended duty cycle for optimum operation and better efficiency. Figure 3.1.1 shows the circuit configuration for the HBBC.

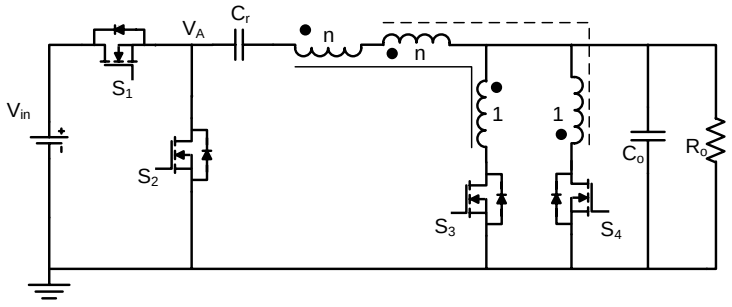

Figure 3.1.1 Half-bridge Buck Converter Circuit Configuration

The HBBC incorporates two coupled inductors, and the turn ratio not only helps to reduce the output voltage by a factor equal to the reciprocal of the turn ratio, but it also increases the current supplied to the load by the secondary side of the transformer enhancing the transient response.

If compared to a conventional two-phase buck converter, the voltage across the lower switches S_3 and S_4, shown in Figure 3.1.1, is lower by a factor of 1/n. This allows for the use of lower voltage MOSFETs with the advantage of lower R_{dson}, which decreases the conduction losses compared to a two-phase buck converter

The current at the primary side is decreased by 1/n, which also decreases the conduction losses of the upper switches S_1 and S_2.

The blocking capacitor, C_r, holds the average voltage, V_{Cr}, according to the equation: $V_{Cr} = V_A - V_o$

Where: V_A is the average voltage of v_A at the phase node as shown in Figure 3.1.1, and it depends on the control type adopted, symmetric or asymmetric, which are analyzed in the following section.

3.2 Half-bridge Buck Control Schemes

3.2.1 Symmetric Half-bridge Buck Converter:

The switching waveforms of the symmetric HBBC are shown in Figure 3.2.1.

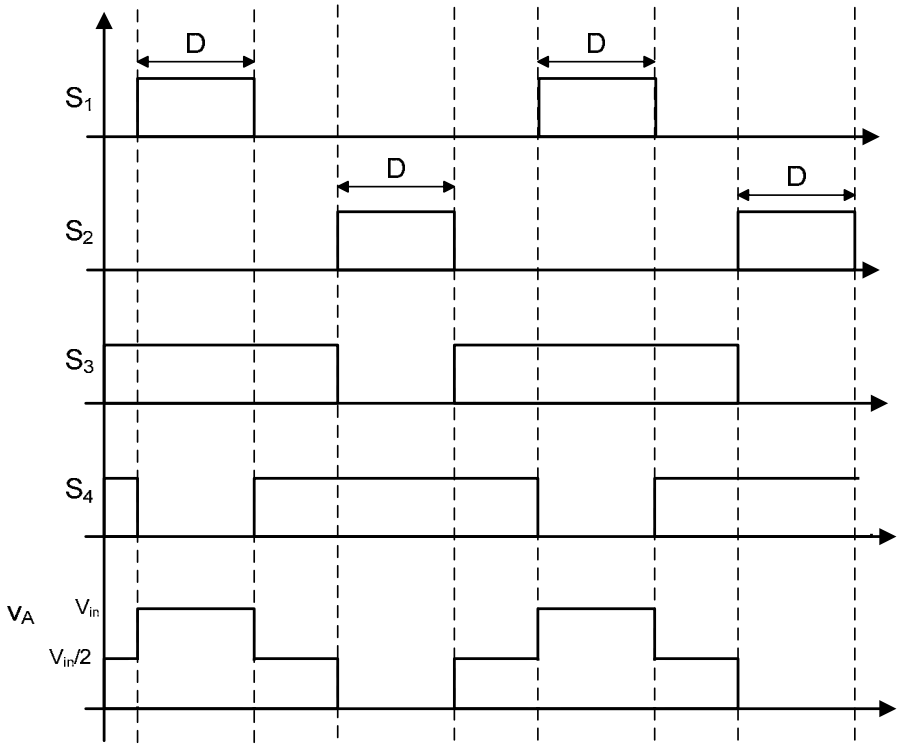

Figure 3.2.1 Switching Waveforms of the Symmetric Half-bridge Buck Converter

It can be shown that the average value of v_A is given by:

$$V_A = V_{in} \cdot D + \frac{V_{in}}{2}(1 - 2 \cdot D)$$

$$= V_{in} D + \frac{V_{in}}{2} - V_{in} D$$

$$= \frac{V_{in}}{2}$$

Therefore, $V_{Cr} = \frac{V_{in}}{2} - V_o$

And this can be considered a voltage source of a value equal to $\frac{V_{in}}{2} - V_o$.

To derive the gain equation, we apply the voltage second balance across the inductors, and from the above waveforms, we can see that there are three different modes of operation: The first mode is when S_1 is ON and S_2 is OFF for the duration of DT. The second mode is when S_2 is ON and S_1 is OFF, and this mode lasts for the same duration of time as the first mode (DT), since the driving signals of the switches are symmetric. And the last mode is when both S_1 and S_2 are OFF. Also, the third mode repeats twice within one switching period, and therefore, the duration of the third mode is (1-2D) T.

Mode I (DT):

During this mode, S_1 and S_3 are ON as shown in Figure 3.2.2

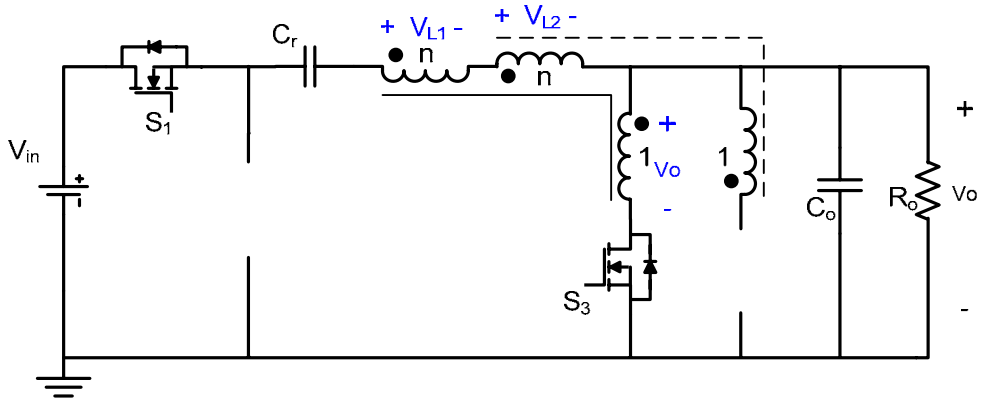

Figure 3.2.2 Mode I of the Symmetric Half-bridge Buck Converter

The inductor voltages are given by the following relations

$$v_{L1} = nV_o$$
$$v_{L2} = V_{in} - V_{Cr} - nV_o - V_o$$

Where V_{Cr} can be substituted by $V_{Cr} = \frac{V_{in}}{2} - V_o$ to yield,

$$v_{L2} = \frac{V_{in}}{2} - nV_o$$

Mode II (DT):

During this mode, S_2 and S_4 are ON as shown in Figure 3.2.3

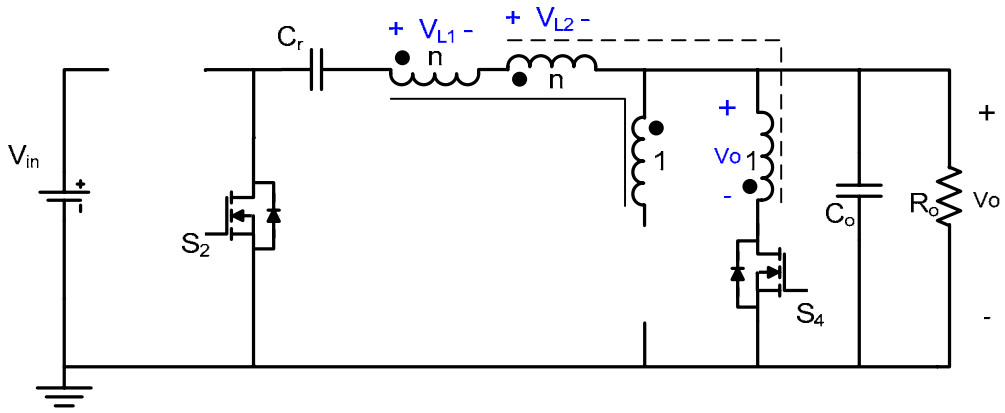

Figure 3.2.3 Mode II of the Symmetric Half-bridge Buck Converter

In this mode, the inductor voltages can be written as;

$$v_{L2} = -nV_o$$
$$v_{L1} = -V_{Cr} + nV_o - V_o$$

Where: $V_{Cr} = \frac{V_{in}}{2} - V_o$

Therefore, $v_{L2} = \frac{-V_{in}}{2} + nV_o$

Mode III (1-2D)T:

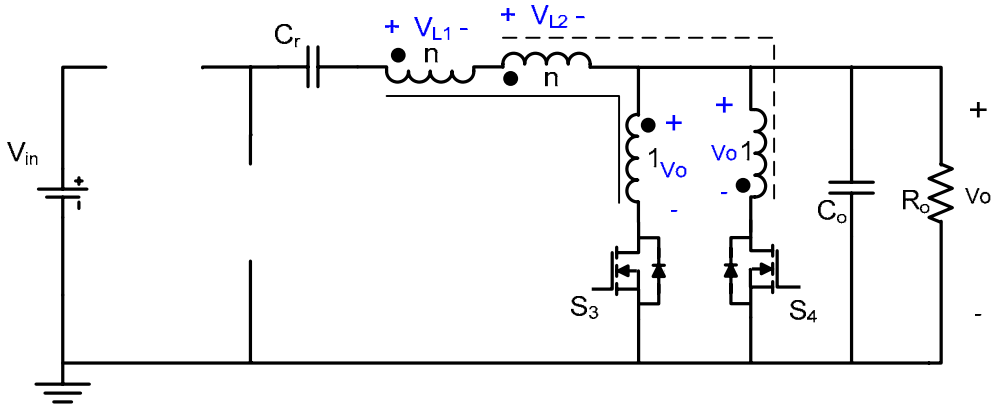

Figure 3.2.4 Mode III of the Symmetric Half-bridge Buck Converter

In this mode, S_3 and S_4 are ON as shown in Figure 3.2.4 and the inductor voltages are expressed as;

$$v_{L1} = nV_o$$

$$v_{L2} = -nV_o$$

Applying the volt second balance on $L1$ or $L2$, we obtain:

$$nV_oD + (nV_o - \frac{V_{in}}{2})D + nV_o(1-2D) = 0$$

Hence, the voltage gain becomes;

$$\frac{V_o}{V_{in}} = \frac{D}{2n}$$

3.2.2 Asymmetric Half-bridge Buck Converter:

As opposed to the symmetric HBBC, the switching waveforms of the asymmetric HBBC are shown in Figure 3.2.5.

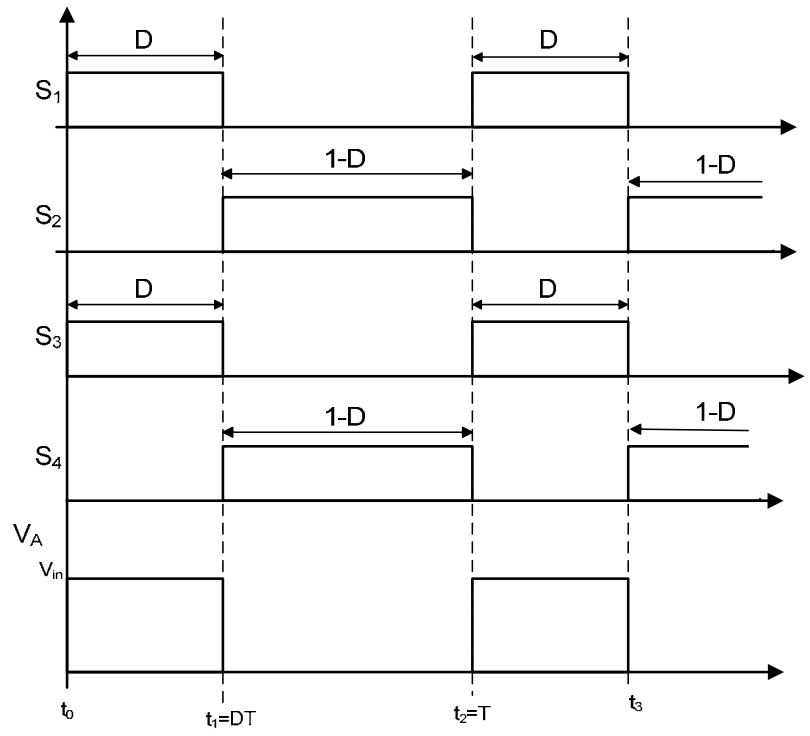

Figure 3.2.5 Switching Waveforms of the Asymmetric Half-bridge Buck Converter

Where the average voltage at the phase node in the Asymmetric HBBC is guven by:

$V_{A\_asym} = V_{in} D$

Therefore, for the asymmetric case: $V_{Cr} = V_{in} D - V_o$

As noted in the asymmetric case, the blocking capacitor voltage depends on the duty cycle D, whereas on the symmetric case it is a constant value equal to $\frac{V_{in}}{2} - V_o$.

To derive the gain equation, we apply the volt second balance across the inductors. Also, we have two modes of operation as shown in Figure 2.3.5.

The first mode is when S_1 is ON, and this mode continues for a period of time equal to DT. The second mode is when S_1 is OFF and S_2 is ON for duration of time equal to (1-D) T.

Applying the volt second balance for the inductors, we get the gain of the converter as shown below.

Mode I: (DT)

In this mode, S_1 and S_3 are ON while S_2 and S_4 both are OFF. The equivalent circuit is shown in Figure 3.2.6:

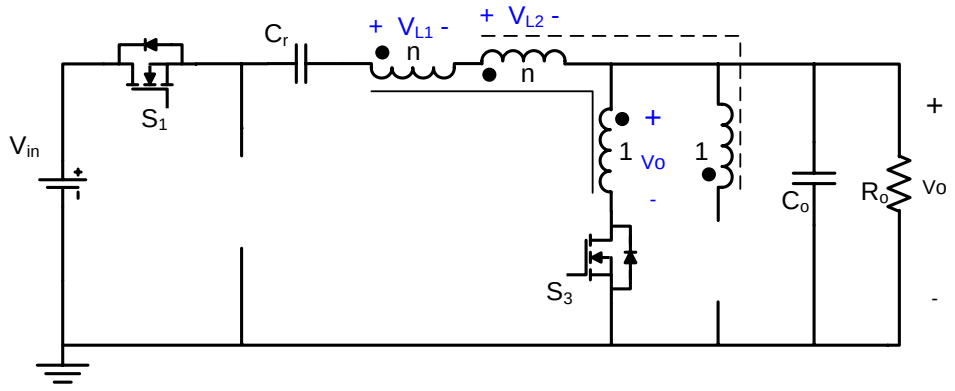

Figure 3.2.6 Mode I of the Asymmetric Half-bridge Buck Converter

The inductor voltages are given by:

$$v_{L1} = n \cdot V_o$$
$$v_{L2} = V_{in} - V_{Cr} - nV_o - V_o$$

Mode II (1-D)T:

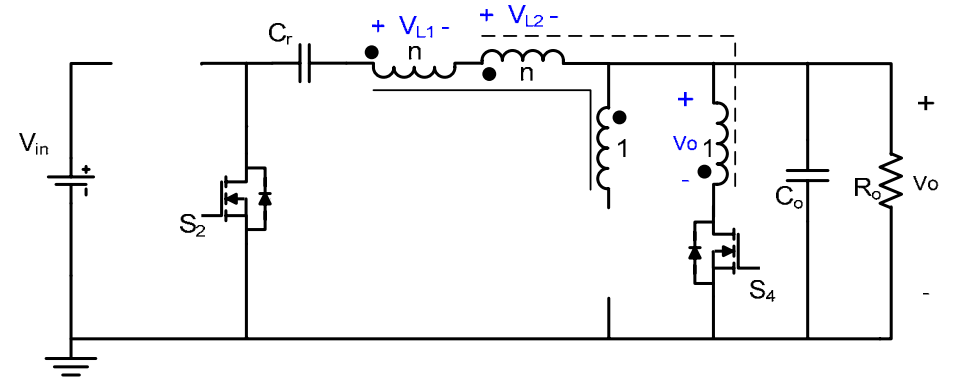

Figure 3.2.7 Mode II of the Asymmetric Half-bridge Buck Converter

$$v_{L2} = -nV_o$$
$$v_{L1} = -V_{Cr} + nV_o - V_o$$

Where: $V_{Cr} = V_{in}D - V_o$

Subsututing V_{Cr} we get, $v_{L1} = -V_{in}D + nV_o$

Applying the volt second balance on V_{L1} or V_{L2}, we get:

$$nV_oD + (nV_o - V_{in}D) \cdot (1 - D) = 0$$

The voltage gain in the Asymmetric HBBC can be written as:

$$\frac{V_o}{V_{in}} = \frac{D(1-D)}{n}$$

3.3 HBBC Modes of Operation

3.3.1 Symmetric Half-bridge

The Half-bridge Buck Converter will be analyzed in more depth in this section, and the symmetric HBBC will be examined prior to the asymmetric. Modes of operation and stress analysis are inspected for both control methods. Figure 3.3.1 shows key waveforms of the converter.

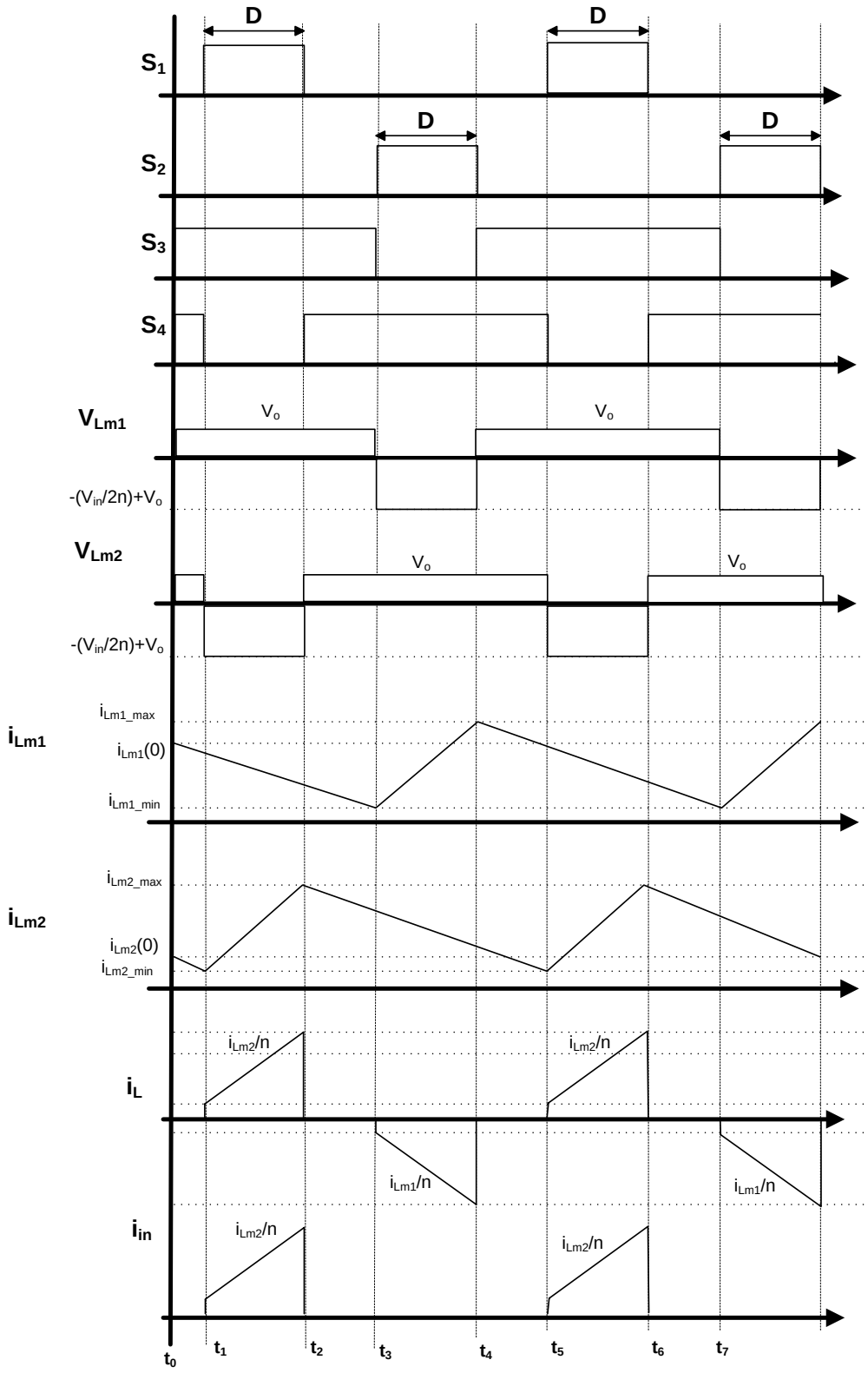

Figure 3.3.1 Key Waveforms of Symmetric Half-bridge Buck Converter

The modes of operation of the converter are as follows;

Mode I: ($t_0 - t_1$)

S_1	S_2	S_3	S_4
OFF	OFF	ON	ON

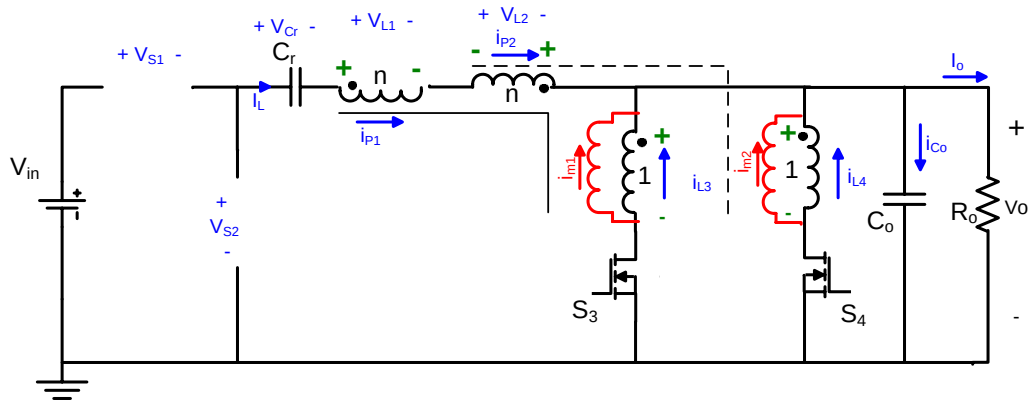

Figure 3.3.2 Mode I In the Analysis of Symmetric Half-bridge Buck Converter

In this mode, the main switches are off and the energy in the magnetizing inductance will be trapped in the transformer. Whereas, the secondary currents i_{L3} and i_{L4} will supply the load current as shown in the following equations:

$$i_L = 0$$

$$v_{L3} = v_{Lm1} = V_o$$
$$v_{L4} = v_{Lm2} = V_o$$

The equations take into consideration the dot notation as shown in Figure 3.3.2.

Therefore:
$$v_{L1} = nV_o$$
$$v_{L2} = -nV_o$$

Where the primary winding of the first transformer can be written as;

$$v_{p1} = v_{L1} = nV_{Lm1}$$

Similarly,

$$v_{p2} = v_{L2} = -nV_{Lm2}$$

The currents through the magnetizing inductance can be expressed as;

$$i_{m1} = -\frac{V_o}{L_{m1}} \cdot t + I_{m1}$$

$$i_{m2} = \frac{-V_o}{L_{m2}} \cdot t + I_{m2}$$

Where: I_{m1} and I_{m2} are the initial conditions for the first and second magnetizing currents respectively.

The output capacitor current and the voltage across S_1 and S_2 are given by;

$$i_{Co} = i_{Lm1} + i_{Lm2} - I_o$$

and $v_{s1} = v_{s2} = \frac{V_{in}}{2}$

Mode II: ($t_1 - t_2$)

S_1	S_2	S_3	S_4
ON	OFF	ON	OFF

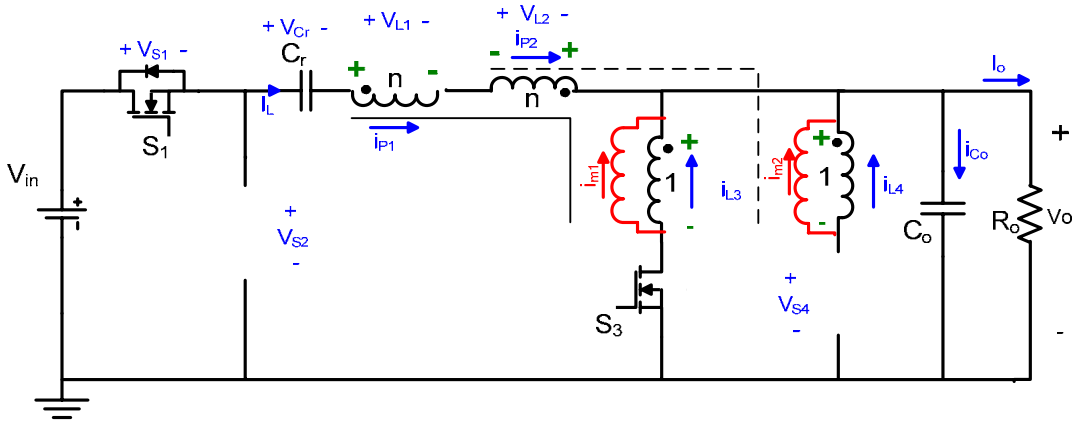

Figure 3.3.3 Mode II In the Analysis of Symmetric Half-bridge Buck Converter

The second inductor acts as an inductance making $i_{p2} = 0$ and with S_4 open, $i_{L4} = 0$.

$$i_{p2} = i_{L4} = 0$$

Examining Figure 3.3.3, the voltages across the inductors can be written as;

$$v_{L3} = V_o$$
$$v_{L1} = nV_o$$
$$v_{L2} = V_{in} - V_{Cr} - v_{L1} - V_o$$

$$= V_{in} - (\frac{V_{in}}{2} - V_o) - nV_o - V_o$$
$$= \frac{V_{in}}{2} - nV_o$$

The currents through the magnetizing inductances are given by;

$$i_{m1} = -\frac{V_o}{L_{m1}} \cdot (t - t_1) + i_{m1}(t_1)$$
$$i_{m2} = \frac{V_{in} - 2n \cdot V_o}{2nL_{m2}} \cdot (t - t_1) + i_{m2}(t_1)$$

The current i_L through the blocking capacitor C_r, and the output capacitor current i_{Co} are given as;

$$i_L = i_{m2} \big/ n$$
$$i_{Co} = i_{m1} + i_{m2} + i_L - I_o$$

Mode III': (t_2- $t_{2'}$)

S_1	S_2	S_3	S_4
OFF	OFF	ON	OFF – D_{S4} ON

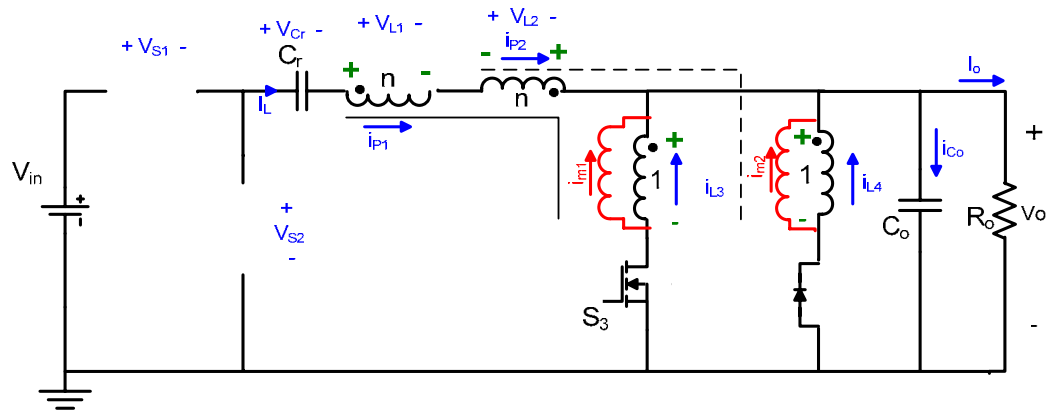

Figure 3.3.4 Mode III' In the Analysis of Symmetric Half-bridge Buck Converter

In this mode, S_1 is turned off and, before turning on S_4, the body diode of S_4 starts conducting for a short period. It is not even shown in waveforms, which allows it to achieve ZVS for S_4. Then, when S_4 is turned on with ZVS, we enter mode IV.

Mode III: ($t_{2'} - t_3$):

S_1	S_2	S_3	S_4
OFF	OFF	ON	ON

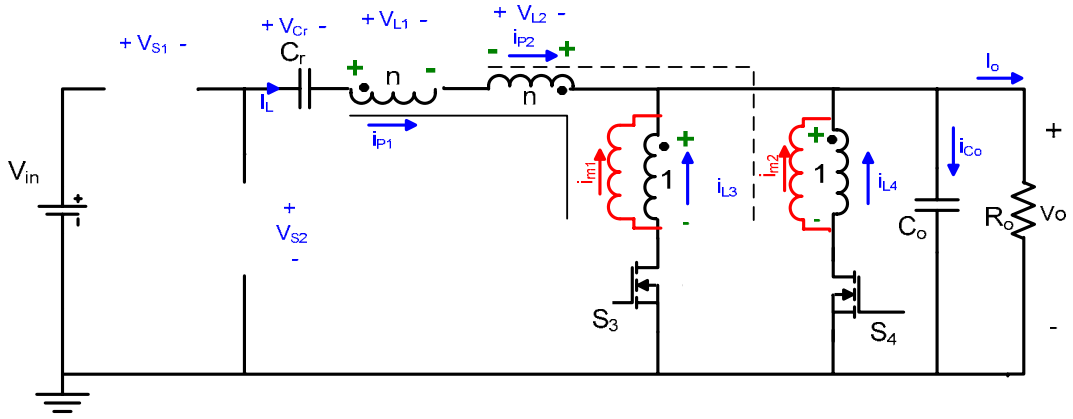

Figure 3.3.5 Mode III In the Analysis of Symmetric Half-bridge Buck Converter

Again, we enter a freewheeling mode in which the load current is supplied by the secondary sides, and the primary side traps the magnetizing currents. The first magnetizing current is negative, and the second one is positive. This mode is no more than the exact duplicate of Mode I, with the appropriate time shift of $\left(t - t_2^{'}\right)$.

Mode IV: ($t_3 - t_4$):

S_1	S_2	S_3	S_4
OFF	ON	OFF	ON

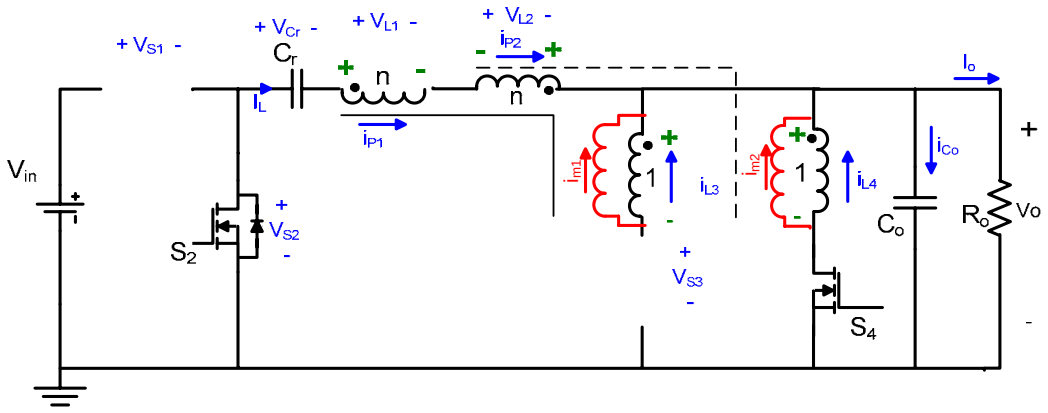

Figure 3.3.6 Mode IV In the Analysis of Symmetric Half-bridge Buck Converter

The first inductor acts as an inductance making $i_{p1} = 0$ and with S_3 open, $i_{L3} = 0$.

$$i_{L3} = i_{P1} = 0$$

Examining Figure 3.3.6, the voltages across the inductors can be written as;

$$v_{L4} = V_o = V_{Lm2}$$
$$v_{L2} = -nV_o$$
$$v_{L1} = -V_{Cr} - v_{L2} - V_o$$

$$= -(\frac{V_{in}}{2} - V_o) + nV_o - V_o$$
$$= -(\frac{V_{in}}{2}) + nV_o$$

The currents through the magnetizing inductances are given by;

$$i_{Lm2} = -\frac{V_o}{L_{m2}} \cdot (t - t_3) + i_{m2}(t_3)$$

$$i_{m1} = \frac{+V_{in} - 2n \cdot V_o}{L_{m1}} \cdot (t - t_3) + i_{m1}(t_3)$$

We can notice that both magnetizing currents reverse their slope direction, where i_{m1} was negative, and now it is ramping up with a positive slope. The same applies on i_{m2} but in the opposite direction.

The current i_L through the blocking capacitor C_r, and the output capacitor current i_{Co} are given as;

$$i_L = i_{m2} / n$$

$$i_{Co} = i_{m1} + i_{m2} + i_L - I_o$$

Mode V': ($t_4 - t_4'$):

S_1	S_2	S_3	S_4
OFF	OFF	OFF- D_{S3} ON	ON

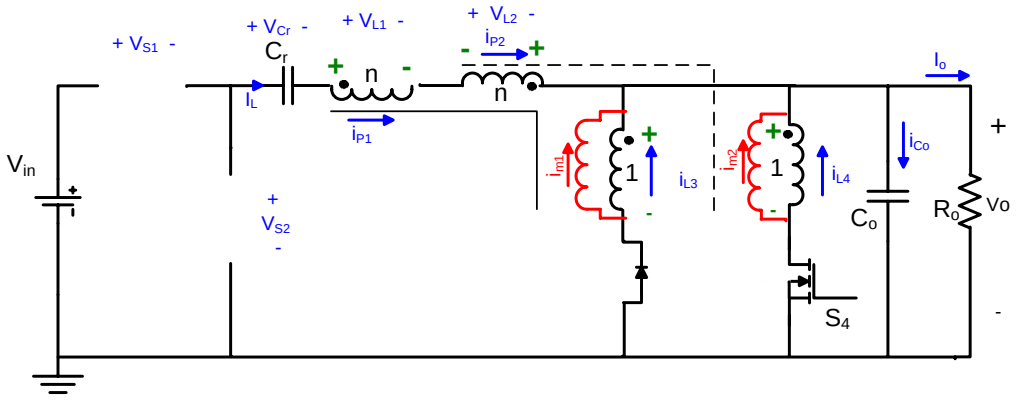

Figure 3.3.7 Mode V' In the Analysis of Symmetric Half-bridge Buck Converter

In this mode, S_2 is turned off, and before turning on S_3, the body diode of S_3 conducts in this mode which is a short period of time and is not shown in the waveforms.

This allows achieving ZVS for S3 and minimizing the body diode conduction losses, Then, when S_3 is turned on with ZVS, we enter mode V and repeat the cycle.

Mode V: (t_4' – t_5)

S_1	S_2	S_3	S_4
OFF	OFF	ON	ON

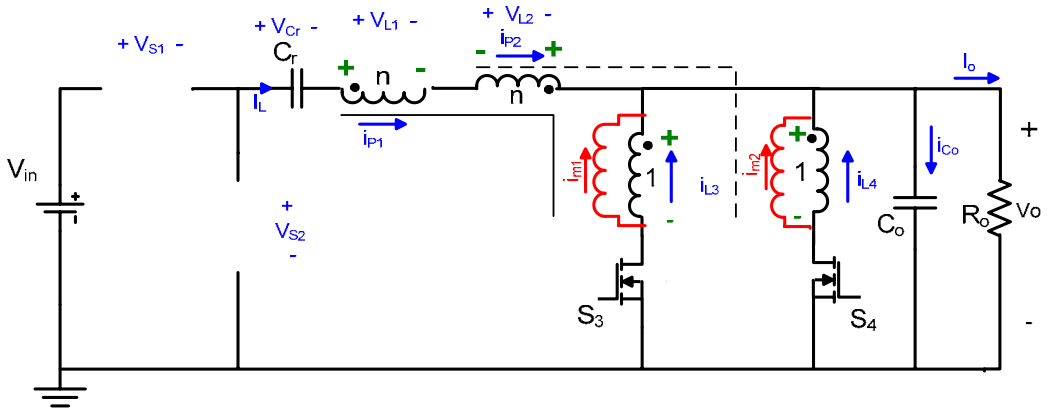

Figure 3.3.8 Mode V In the Analysis of Symmetric Half-bridge Buck Converter

Again, this mode is an exact duplicate of mode I, with the exception of the appropriate time shift that is now $\left(t - t_4^{'}\right)$.

As a summary of the voltage and current stresses across and through the switches, the Table 3.3.1 shows the voltages across the switches during turn off and the current through the switches while conducting.

Table 3.3.1 Voltage and Current Stress Analysis for the Symmetric HBBC

	Mode II		Mode I, III, V		Mode IV	
	V.S.	I.S.	V.S.	I.S.	V.S.	I.S.
S_1	0	i_{m2}	$V_{in}/2$	0	V_{in}	0
S_2	V_{in}	0	$V_{in}/2$	0	0	$-i_{m1}$
S_3	0	i_{L3}	0	i_{L3}	$V_{in}/(2n)$	0
S_4	$V_{in}/(2n)$	0	0	i_{L4}	0	i_{L4}

3.3.2 Asymmetric Half-bridge

Modes of Operation:

Mode I: ($t_0 - t_1$): ($t_0 - DT$)

S_1	S_2	S_3	S_4
ON	OFF	ON	OFF

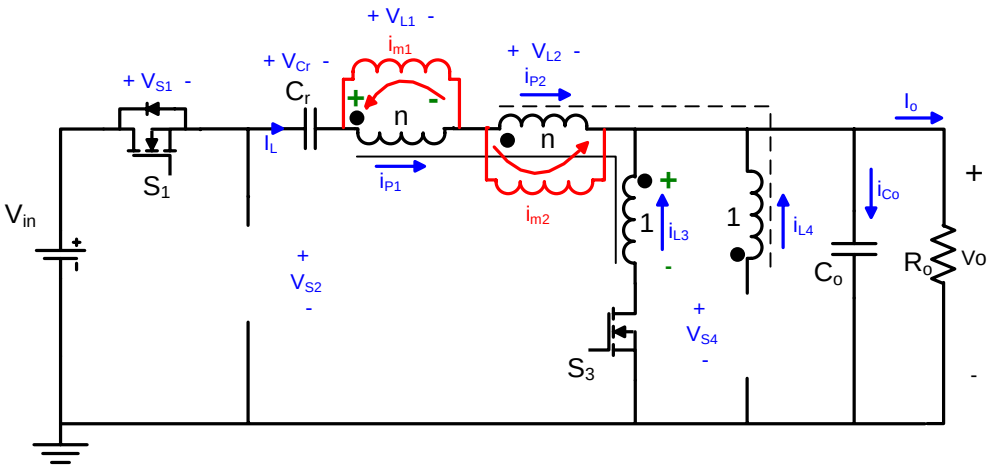

Figure 3.3.9 Mode I In the Analysis of Asymmetric Half-bridge Buck Converter

The second inductor acts as an inductance making $i_{p2} = 0$ and with S_4 open, $i_{L4} = 0$.

$$i_{p2} = i_{L4} = 0$$

Examining Figure 3.3.9, the voltages across the inductors can be written as;

$$v_{L3} = V_o$$
$$v_{L1} = nV_o$$
$$v_{L2} = V_{in} - V_{Cr} - v_{L1} - V_o$$

$$= V_{in} - (V_{in}D - V_o) - n \cdot V_o - V_o$$
$$= V_{in}(1 - D) - n \cdot V_o$$

The currents through the magnetizing inductances are given by;

$$i_{m1} = -\frac{n \cdot V_o}{L_{m1}} \cdot t + I_{m1}$$

$$i_{m2} = \frac{(V_{in}(1-D) - n \cdot V_o)}{L_{m2}} \cdot t + I_{m2}$$

$$i_{P1} = i_{m1} + i_{m2}$$

Where: I_{m1} and I_{m2} are the initial conditions of the first and second magnetizing inductances respectively.

The current through S_3 is $i_{L3} = n \cdot i_{P1}$

The current i_L through the blocking capacitor C_r, and the output capacitor current i_{Co} are given as;

$$i_L = i_{m2}$$

$$i_{Co} = i_{m2} + i_{L3} - I_o$$

Mode II': (t_1- t_1')

S_1	S_2	S_3	S_4
OFF	OFF	ON	OFF – D_{S4} ON

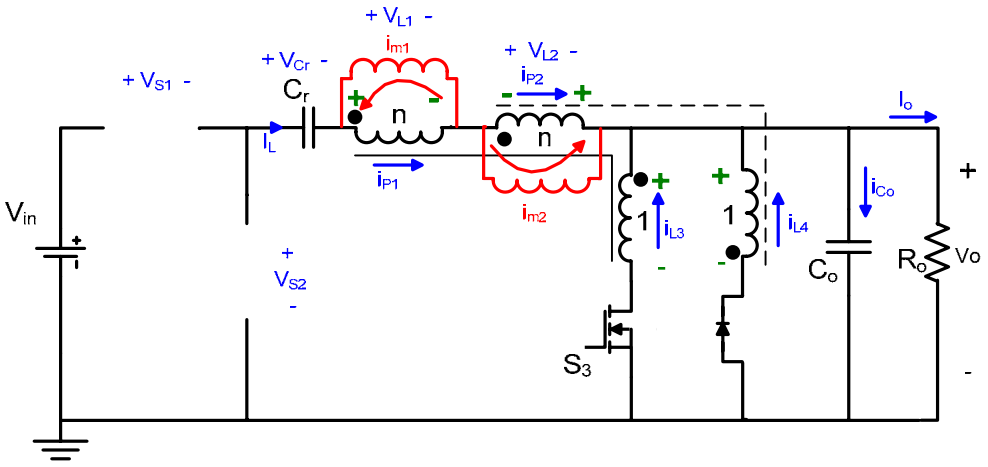

Figure 3.3.10 Mode II' In the Analysis of Asymmetric Half-bridge Buck Converter

In this mode, S_1 and S_3 are turned off and before turning on S_4; the body diode of S_4 conducts in this mode for a short period of time and is not shown in waveforms, allowing it to achieve ZVS for S_4. Then, when S_2 and S_4 are turned on with ZVS for S_4, we enter mode II.

Mode II: (t_1' – t_2): (t_1' – (1-D) T):

S_1	S_2	S_3	S_4
OFF	ON	OFF	ON

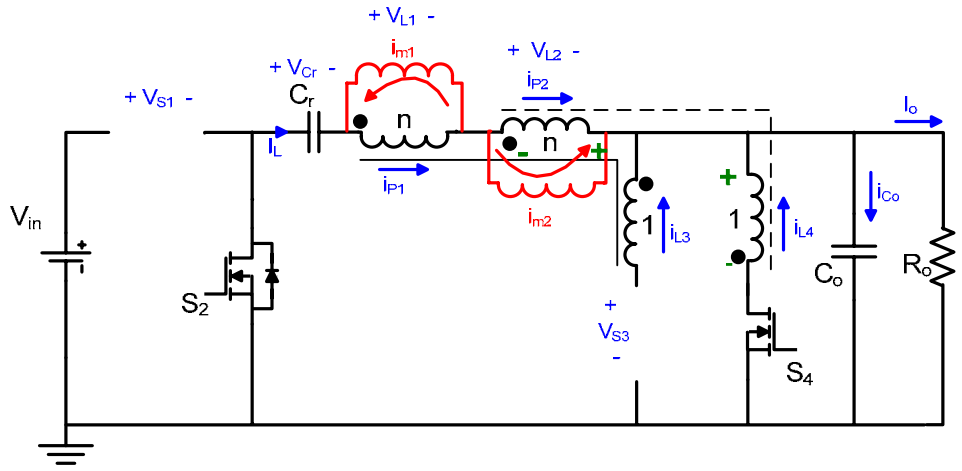

Figure 3.3.11 Mode II In the Analysis of Asymmetric Half-bridge Buck Converter

The first inductor acts as an inductance making $i_{p1} = 0$ and with S_3 open, $i_{L3} = 0$.

$$i_{L3} = i_{P1} = 0$$

Examining Figure 3.3.11, the voltages across the inductors can be written as;

$$v_{L4} = V_o$$
$$v_{L2} = -n \cdot V_o$$
$$v_{L1} = -V_{Cr} - v_{L2} - V_o$$
$$= -(V_{in}D - V_o) + nV_o - V_o$$
$$= -V_{in}D + nV_o$$

The currents through the magnetizing inductances are given by;

$$i_{m2} = -\frac{n \cdot V_o}{L_{m2}} \cdot t + i_{m2}(t_2)$$
$$i_{m1} = \frac{-V_{in} D + n \cdot V_o}{L_{m1}} \cdot t + i_{m1}(t_2)$$
$$i_{P2} = -(i_{m1} + i_{m2})$$

We can note that both magnetizing currents reversed their slope direction, where i_{m1} was negative and now it is ramped up with a positive slope. The same applies on i_{m2} but in the opposite direction.

$$i_{L4} = -n \cdot i_{P2}$$

The current i_L through the blocking capacitor C_r, and the output capacitor current i_{Co} are given as;

$$i_L = -i_{m1}$$
$$i_{Co} = -i_{m1} + i_{L4} - I_o$$

The cycle repeats, and to illustrate the ZVS for S_3 switch, another half cycle is discussed below.

Mode I': ($t_2 - t_{3'}$):

S_1	S_2	S_3	S_4
OFF	OFF	OFF – D_{S3} ON	ON

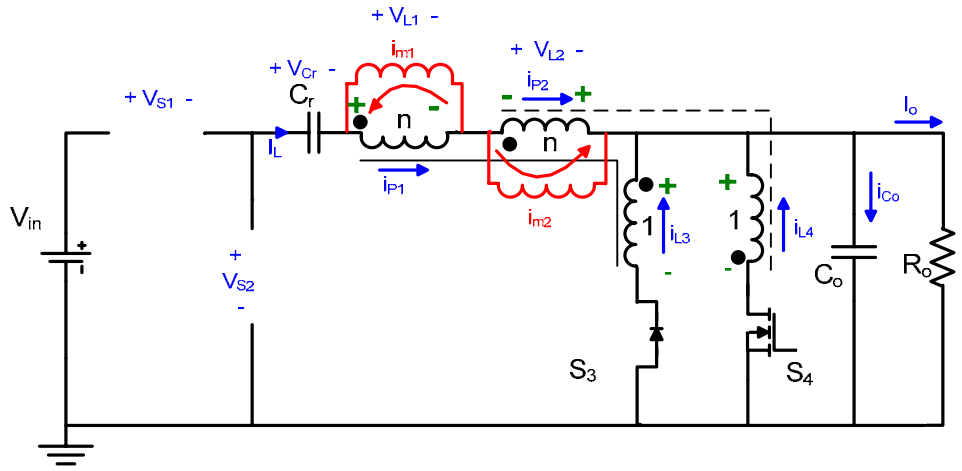

Figure 3.3.12 Mode I' In the Analysis of Asymmetric Half-bridge Buck Converter

In this mode, S_2 is turned off, and before turning on S_3, the body diode of S_3 conducts. This mode should be short and is not shown in the waveforms, as the body diode conduction losses are high allowing it to achieve ZVS for S_3. Then when S_1 and S_3 are turned on with ZVS for S_3, the cycle is repeated, and we enter mode I again.

As a summary of the voltage and current stresses across and through the switches, Table 3.3.2 shows the voltages across the switches during turn off and the current through the switches while conducting.

Table 3.3.2 Voltage and Current Stress Analysis for the Asymmetric HBBC

	Mode I		**Mode II**	
	V.S.	**I.S.**	**V.S.**	**I.S.**
S_1	**0**	**i_{m2}**	**V_{in}**	**0**
S_2	**V_{in}**	**0**	**0**	**$-i_{m1}$**
S_3	**0**	**i_{L3}**	**$V_{in}D/n$**	**0**
S_4	**$V_{in}(1-D)/n$**	**0**	**0**	**i_{L4}**

The focus of this work in centered on symmetric control for the benefit it offers of identical transformer design, which facilitates the magnetic design.

It is clear from the above discussion that the asymmetric half-bridge will need different magnetizing inductances to compensate for the difference in the period during which they store energy. This will complicate the analysis and is subject to future investigation.

Duty Cycle Shift (DCS) is another attractive control scheme in which Zero Voltage Switching can be achieved on S_1 and S_2, which further reduces the switching losses and increases efficiency. Again, this control scheme is not covered in this work and falls in the scope of future analysis.

3.4 Simulation Results

The HBBC circuit is simulated and some waveforms are shown in Figures 3.4.1 and 3.4.2:

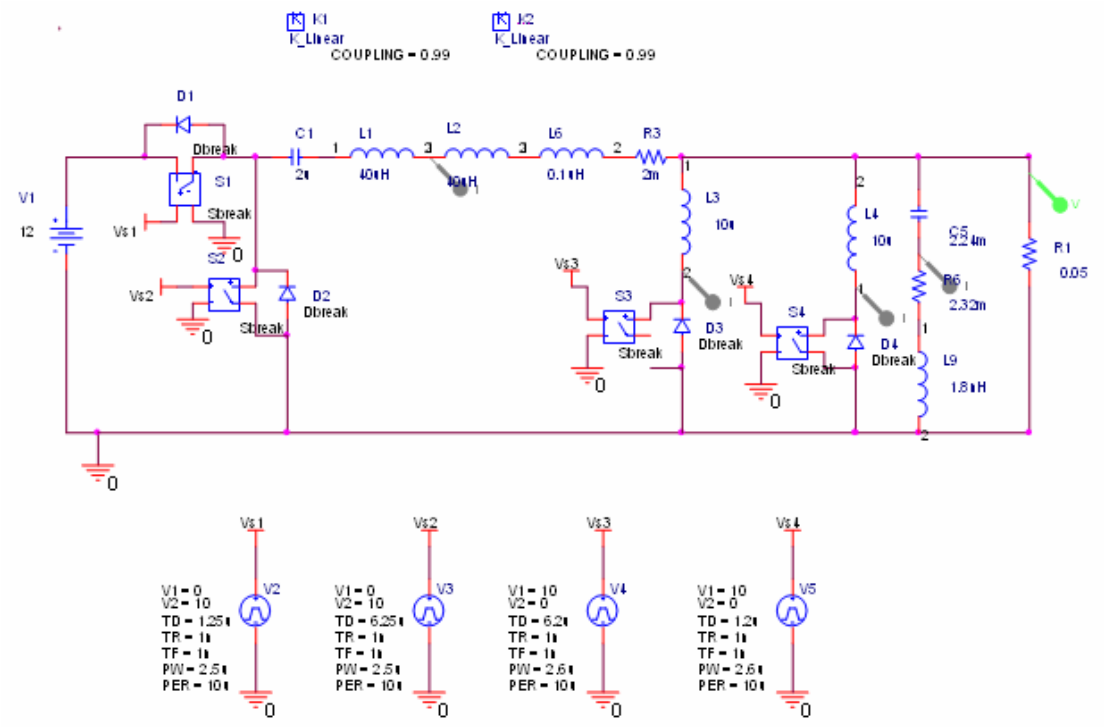

Figure 3.4.1 Simulation Circuit for a Symmetric HBBC

The switching signals v_{S1}, v_{S2}, v_{S3} and v_{S4} are shown in Figure 3.4.2 with a small dead time to allow ZVS for S_3 and S_4 as explained in the modes of operation.

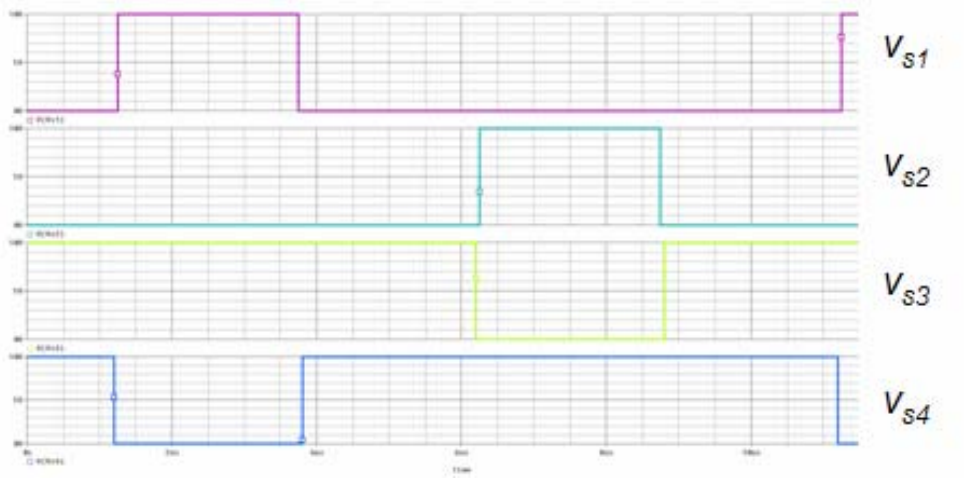

Figure 3.4.2 Switching Waveforms Simulation Result for a Symmetric HBBC

Some other waveforms of interest are as shown in Figure 3.4.3.

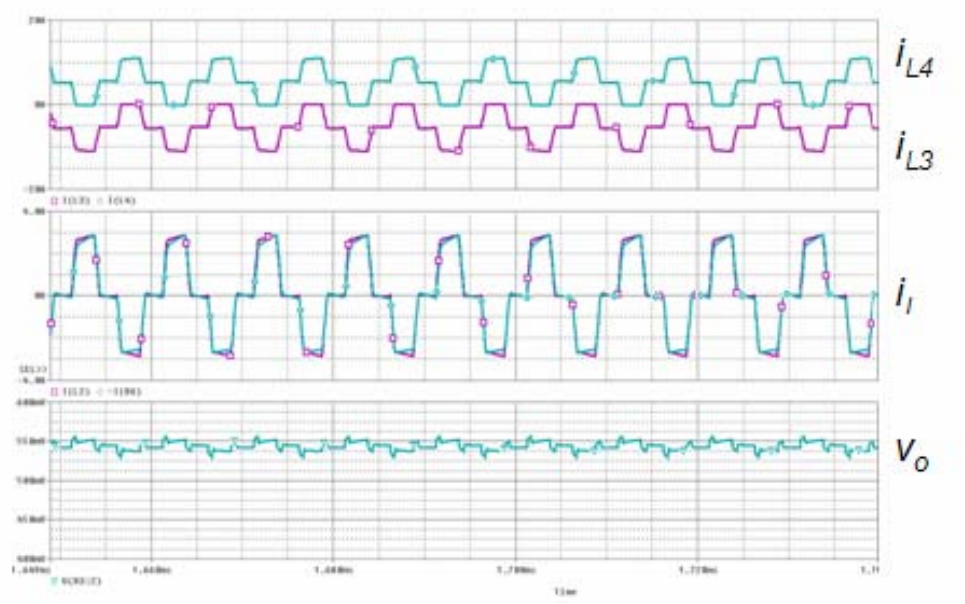

Figure 3.4.3 Simulation Results for a Symmetric HBBC

3.5 Turns Ratio vs. Efficiency

The microprocessor industry is moving towards lowering the output voltage for faster data transfer and lower power consumption together with increasing the current and the power density. The target of the industry now is to feed the processor with as little as one Volt.

Buck-based converters have been the main building block stepping the 12 Volts input to the one Volt needed at the processor side. Multiphase buck was used to further decrease the output ripple. The main drawback is the small duty cycle needed.

For a buck converter: $D = \frac{V_o}{V_{in}}$

In our case: $V_{in} = 12V$ and $V_o = 1V$ resulting in $D = 1/12 = 0.0833$

This small duty cycle produces many problems. The smaller the duty cycle, the higher the current peak is, and consequently, the higher the RMS values, which result in higher conduction loss. Added to the above comes the urge for achieving faster response while decreasing the converter size. This will push into increasing the bandwidth and the switching frequency, which is always accompanied by higher switching losses.

These requirements — low output voltage, small size and fast response — result in lower efficiency.

Efforts are now dedicated and directed towards increasing the duty cycle. Hence, transformer-based buck converters have been a research topic for solving the above-mentioned problems.

In the half-bridge buck presented here, the output voltage is a function of not only the duty cycle and input voltage, as in the case of the buck converter, but also it is a function of the turn ratio n.

$$V_o = \frac{D \cdot V_{in}}{2 \cdot n}$$

A study on how the turn ratio affects the efficiency is shown below. Rearranging the above equation to solve for *D*, we get:

$$D = \frac{V_o . 2 . n}{V_{in}}$$

For the same 12V at the input side and One Volt at the output side, the optimal value of *D* is chosen as follows.

As shown in Table 3.5.1, for the same 12V input and One Volt output, varying n we get:

Table 3.5.1 Turns Ratio versus Efficiency

N	D
1	0.126
2	0.33
3	0.5

Therefore, the HBBC improves the duty cycle even with 1 turn and in light of the fact that the output voltage is multiplied by two; the duty cycle is increased by a factor of two. Examining Table 3.5.1, it is obvious that the optimum turn ratio (n) is *n*= 2 for the following reasons:

1) The voltage stress across S_3 and S_4 will be twice less than that of a two-phase buck; this will allow the use of a lower voltage MOSFET with lower R_{dson} and lower losses. This benefit will not be achieved if *n*= 1 was used.

2) ZVS for S_3 and S_4 was achieved by applying a small dead time which was doable because D was less than 0.5. This advantage will not be possible if n= 3 were used and higher values for n will not allow for synchronous driving, therefore, n= 3 was the maximum turn ratio in Table 3.5.1.

3.6 Small Signal Modeling

Circuit averaging has been applied to the circuit to obtain the small signal model and design the control loop. After perturbation and linearization, the AC small signal model was derived as shown in the following equations:

$$\hat{\dot{x}} = \underbrace{\left(A_{avg}\,\hat{x} + B_{avg}\,\hat{u} \right)}_{Line\ variation} + \underbrace{\left(\left(A_1 + A_3 - 2A_2\right)X + \left(B_1 + B_3 - 2B_2\right)U \right)\hat{d}}_{duty\ variation}$$

$$\hat{y} = \underbrace{\left(C_{avg}\,\hat{x} \right)}_{Line\ variation} + \underbrace{\left(\left(C_1 + C_3 - 2C_2\right)X \right)\hat{d}}_{duty\ variation}$$

Where; A_1, A_2, A_3 and A_4 are the state matrices of each mode of operation. Similarly for B_1, B_2, B_3 and B_4 since B_2= B_4 and the output matrices C_1, C_2, C_3 and C_4.and A_{avg}, B_{avg} and C_{avg} are the average matrices.

The canonical form was also derived as shown in Figure 3.6.1.

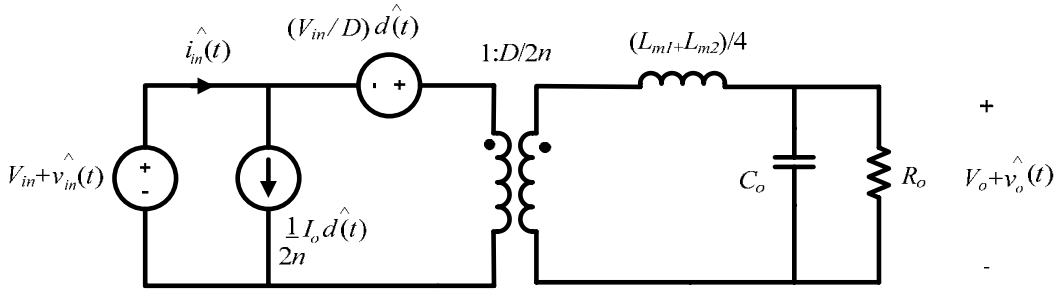

Figure 3.6.1 The Canonical Equivalent Circuit

The transfer functions of interest are:

$$G_{vd}(s) = G_{do} \frac{1}{1 + {}^{s}\!/_{\omega_o Q} + \left({}^{s}\!/_{\omega_o}\right)^2}$$

where:

G_{vd} is the output to duty cycle transfer function.

$$G_{do} = \frac{V_{in}}{2n}$$

$$\omega_o = \frac{2}{\sqrt{C_o(L_{m1} + L_{m2})}}$$

and:

$$Q = 2R_o \sqrt{\frac{C_o}{(L_{m1} + L_{m2})}}$$

Output impedance can be expressed as:

$$Z_{out}(s) = Z_1 // Z_2$$

where:

$$Z_1 = \omega\left(\frac{L_{m1} + L_{m2}}{4}\right)$$

and:

$$Z_2 = \frac{R_o}{1 + \omega R_o C_o}$$

The compensator was designed and the results are shown in Figure 3.6.2.

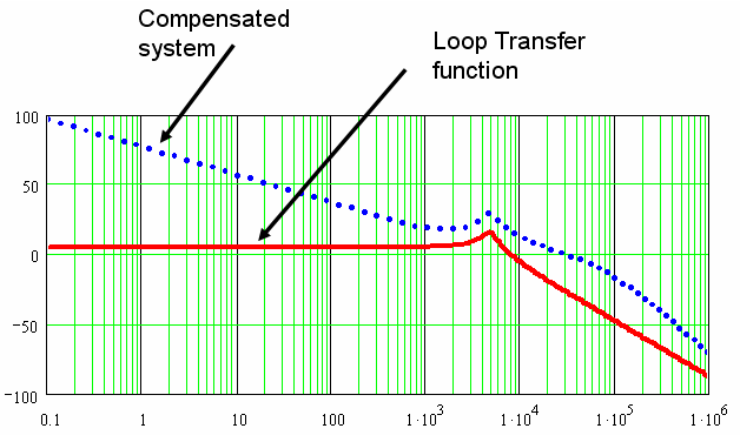

Figure 3.6.2 Loop and Compensated System Frequency Response

Figure 3.6.2 shows the loop transfer function and the compensated on which the control loop was designed.

3.7 Chapter Recap

In this chapter, the Half-bridge Buck transformer-based non-isolated topology was examined in detail, and the symmetric and asymmetric control schemes were compared.

This topology offers many advantages to the VRM research field, and the transformer introduced helped as a current doubler, increasing the current supplied to the load and thereby decreasing the voltage spikes at the output to enhance the transient response.

The step-down turns ratio helped not only to increase the duty cycle and consequently avoid all associated problems. And it also decreased the voltage across the switches; which enabled the use of a lower voltage MOSFET and in turn decreased losses. In an analogous direction, the current is increased, which helped decrease the output capacitance and saved space and cost.

The two switches added - S_3 and S_4- are zero voltage switched which decreased switching losses and consequently increased the efficiency.

CHAPTER 4

MAGNETICS DESIGN AND EXPERMINTAL RESULTS

4.1 Introduction

Magnetic components are present in almost all switch mode power supplies (SMPS). Their purpose may vary depending on the application. All filters contain magnetic components that must be designed, and those "magnetic-based" filters are inevitable among SMPS. Sometimes energy is needed to be stored and recovered during a certain interval of the switching period to achieve resonant conditions for zero switching. These energy storage devices have to be inductors or flyback transformers. Some SMPS need isolation or level conversion, hence the need for a transformer that is a purely magnetic element.

In summary, SMPS designers need to know a great deal about the magnetic realm to be able to efficiently design these magnetic elements. Nevertheless, their design is a big challenge, especially at high switching frequencies in the sense that their natural innate parasitic elements are the cause of so many problems: high losses, high spikes, noise, etc., which will dramatically affect efficiency [33, 39].

Farady, Lenz and Ampere are the three corners on which the constitution of the magnetic theory is based, and each contributed by stating a law that is available in almost all magnetic books.

According to Faraday's, the total flux change, $\frac{d\Phi}{dt}$ in a winding or a conductor loop induces voltage in the wire [39].

$$v(t) = \frac{d\Phi(t)}{dt}$$

Whereas, Lenz declares that the above mentioned voltage is induced with a certain polarity that, when divided by the impedance of the loop, will in turn drive a current to oppose the original flux [39].

Ampere states that the total current passing through the interior of a path is equal to the net magnetomtoive force, MMF, around the closed path [39].

These three laws govern the magnetic world. An understanding of the magnetic field and components will help to optimally design any inductor or transformer. Since all inductors and transformers are merely copper windings on magnetic cores, an insight on the core characteristics and properties, together with detailed comprehension of the methods of winding, will assist in a more robust design and higher efficiency.

4.2 Properties and Characteristics of Magnetic Cores

Physics tells us that any current-carrying conductor will produce magnetic field or equipotnetials perpendicular to the conductor. If this conductor is placed in a magnetic core, then this field will be contained in this core. Cores are the medium in which the magnetic flux is transferred from one part to another whether magnetic or electric [34].

Ideal transformers do not store energy. Rather, they transfer power from one primary magnetic side to the other or to multiple secondary magnetic sides. Primary and secondary windings are linked via a magnetic core, and cores are not energy storage media by any means. Energy is stored in what is called and intentionally created

magnetizing inductance. Ideal transformers have "ideally" infinite magnetizing inductance and zero magnetizing current, which is why they do not store energy. Magnetizing inductance is created by adding a non-magnetic material in the core. Air gaps are the non-magnetic storage media, which are added to create the magnetizing inductances in which energy is stored. The equivalent circuit of the transformer shows that the magnetizing inductance is in parallel with the ideal transformer, and therefore adds air gaps that decrease the inductance value of the transformer [34].

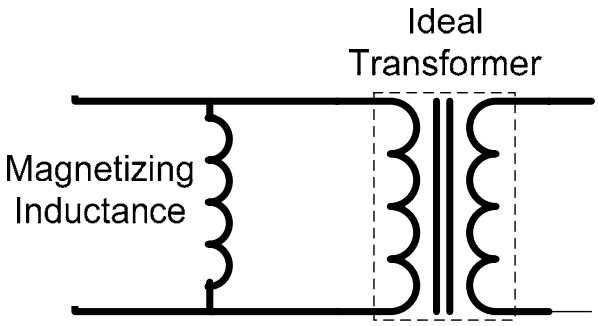

Figure 4.2.1 Transformer Equivalent Circuit

Cores have a specific measure of how magnetic their magnetic material is, and this quantity is reflected by their permeability. The higher the magnetic permeability, the tighter the coupling is, and this means the total flux produced at one side is fully transferred through the core to the other side. Higher permeability means less leakage [39].

Magnetic permeability of cores is given the Greek symbol μ. Air gaps are another channel for flux, and their permeability is of free space and is given the symbol μ_o.

Where: $\mu_o = 4\pi \cdot 10^{-7}$ and $\mu >> \mu_o$

μ is highly dependent on temperature [39].

The inductance L, in an ideal transformer, is directly proportional to μ;

$$L = \frac{n^2 \cdot A_c \cdot \mu}{l_m}$$ [39].

Where: n is the number of turns of the winding.

A_c and l_m are the core geometrical area and length respectively. In the case when air gap is added, the inductance value becomes:

$$L = \frac{n^2}{R_c + R_g}$$ [39].

Where: R is the reluctance.

$$R_c = \frac{l_c}{A_c \cdot \mu} \quad \text{and} \quad R_g = \frac{l_g}{A_c \cdot \mu_o}$$ [39].

It is obvious that when air gap is added, the inductance value will be less affected on the temperature-dependent μ. Consequently, this means there is a need for more solidly designed inductance that is independent of any variation on temperature. Air gaps also allow for more current before reaching saturation [39].

Inductors and flyback transformers store energy in their magnetizing inductances. Flyback transformers are considered inductors with more than one winding or gapped transformers [37].

To maintain a certain inductance value with the presence of air gaps, one can either increase the number of turns with the tradeoff of increasing cupper loss and leakage inductance or use bigger cores with core utilization in mind.

As a conclusion, cores play an important role in the design in addition to providing flux channel. Understanding the characteristics of cores is vital for better design.

Magnetic core materials include:

1- Metal Alloy Tape-wound Cores [34, 39]:

- Application: best used for ideal transformers
- Examples: permalloy and amorphous metal alloy cores
- Frequency range: low, 50 60 and 400 Hz applications
- Properties: high permeability and high saturation flux density
- Drawback: low core resistivity
- Notes:
    a. Low resistivity allows more eddy currents to flow in the core, which increases losses. This can be alleviated by using thin tape-wound laminations
    b. Amorphous metal alloys are the newer tape wound cores that can be used in high frequency applications.

2- Powdered Metal Cores [34]:

- Application: best for inductors and flyback transformers
- Examples: powdered iron, koolM μ and permalloy powder cores
- Frequency range: up to 100 kHz
- Properties: Low permeability and thus higher magnetizing current for energy storage
- Drawback: Lossy cores, powdered iron are the worst among them, koolM μ is better and permalloy is the best

- Notes: for application of 100 kHz frequency or less, powdered metal cores with their spread air gap among the core particles are better than ferrite cores with the series added air gap due to their higher saturation limit.

3- Ferrite Cores [34, 39]:

- Application: Ferrites are ceramic materials and are the most popular among magnetic cores for different applications
- Examples: MnZn (manganese and zinc ferrite cores) and NiZn (Nickel and zinc ferrite cores)
- Frequency range: up to MHz
- Properties: Lower permeability and higher resistivity thus less losses
  Less expensive with a wide variety of shapes
- Drawback: Less robust since it is ceramic with less saturation limit
- Notes: Saturation is not considered an issue in high-frequency applications, which is the range in which ferrite cores are used.

In summary, the core materials compared are shown in Table 4.2.1.

Table 4.2.1 Core Material Comparison

Material	**Lousiness**	**Bsat**	**Required gap**
Ferrite	Not lousy	Low	Discrete
Powdered Iron	Lousy	High	Distributed among the particles
Kool-mu	Lousy	high	
Laminated metal	Lousy	high	Discrete

Cores have many limitations and losses such as: core losses, window utilization and saturation. Depending on the application and frequency range, cores are chosen to

best design and operate the circuit. Core losses are the main concern in high frequency applications, whereas saturation is not a problem. Core saturation is an issue in low frequency application.

Tape wound cores are best used in low frequency ranges for transformer purposes, but they are replaced by their less robust counterparts such as ferrites for higher frequency applications. Powdered iron is not an option due to its high core losses and low permeability [34].

For inductors and flyback transformers, gapped tape wound cores or lossy powdered iron cores are used in low frequency ranges, which give credit to their high saturation limits and neglect AC core losses at this low range. Again, ferrites outperform them in high frequency ranges, where high core losses come to play and saturation setback diminishes [34].

4.3 Losses

4.3.1 Core and Hysteresis Losses

Core loss is mainly hysteresis loss at low frequencies, and at higher frequencies eddy current loss overtakes hysteresis loss.

4.3.2 Eddy Current Losses

As pointed out above, magnetic cores are made of iron alloys, which unfortunately have some resistance. The induced voltage across the winding is also applied across the core, and dividing this voltage by the core impedance will result in eddy current flowing in the core, which is translated to losses. Thus, eddy current losses

are function of the volts/turn ($d\phi/dt$) applied to the windings and the duty cycle and it is indirectly independent of the frequency [34, 39].

Eddy current losses are negligible in the high resistance ferrite cores and avoided in the low-resistance tape-wound cores when the lamination method is applied. Laminating the windings decreases the cross section area, which decreases the voltage induced within the core and thus further reduces the eddy current losses [34, 39].

4.3.3 Skin Effect

Conductors are represented by inductors and resistors as shown in Figure 4.3.1.

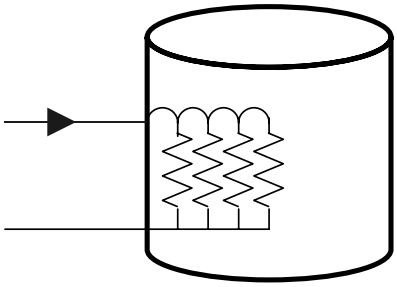

Figure 4.3.1 Effect of Skin Depth

The difference between two currents, one passing at the surface of the conductor and the other one passing in the center of the conductor, is the resistance. In our case, the conductor under study is the core, and a higher resistance cores means less eddy currents and therefore less losses. At low frequency, the inductor impedance is low, allowing the current to be equally divided as it passes through the center of the core. With higher frequency, the impedance of the inductor increases, shifting the current flow to the surface where skin depth becomes an issue [34, 35].

Solid cores may cause the flux to be on the surface of the core, which increases eddy current losses, hence the importance of calculating the core penetration (skin effect) [34, 35]:

$$D_{PEN} = \sqrt{\frac{\rho}{\pi \mu_o \mu_r f}}$$

It is directly proportional to the square root of the resistivity ρ, divided by frequency.

At the same frequency, skin effect is not a problem in high resistivity ferrite cores. But it is an issue at higher frequencies [34, 35].

4.4 Windings

An efficient magnetic design should take into consideration many of the problems and roots of all losses, such as the dc resistance of the copper, the core characteristics and the leakage inductance, to name a few. Copper loss of the winding can be, in straight forward method, expressed as [39]:

$$p_{cu\_loss} = I_{rms}^2 \cdot R_{cu}$$

Where: R_{cu} is the cupper dc resistance and is equal to:

$$R_{cu} = \rho \frac{l_w}{A_w}$$

Where: l_w and A_w are the length and cross-sectional area of the wire.

ρ is the resistivity of copper and is equal to 1.724×10^{-6} Ω-cm.

As illustrated in the previous section, core materials and properties have a strong impact on the magnetic design. Winding is another vital topic to be regarded and will be discussed in this section.

A few main rules come in handy in the area of magnetic design. The first rule is that the wire diameter should be 1.5 – 2 times the skin depth. The second rule is copper windings should be operated at current densities of around 4 – 4.5A/ mm^2. If the frequency is shifted to higher values, current densities may increase as well.

Window shape and size affect utilization and losses and both a wider window as well as interleaved winding in turn will decrease eddy currents and leakage inductances. But the price paid is higher capacitance between windings. In other words, methods adopted to decrease eddy currents and leakage inductance, which include using a wider window, interleaving windings and small spacing between the primary and the secondary sides, will lead into higher capacitance [35].

4.5 Experimental Results

The topology discussed in the previous chapter is highly sensitive to any leakage inductance, thus the magnetic design should be robust and tightly coupled to decrease the leakage. A Maxwell simulation was used to compare two transformers. The first transformer was winded using PC44EE16-Z cores and twisted wires of 0.2mm thickness to avoid skin depth. 1 mm wire in diameter with six turns made up the primary side and is twice the thickness, and three turns wire made up the secondary. Figure 4.5.1 shows the transformer.

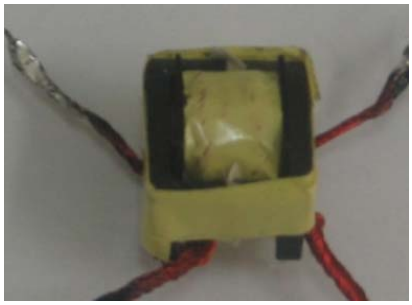

Figure 4.5.1 PC44EE16-Z Transformer

The transformer was modeled and simulated using a Maxwell magnetostactic simulation, and the model and simulation results are shown in Figures 4.5.2 and 4.5.3.

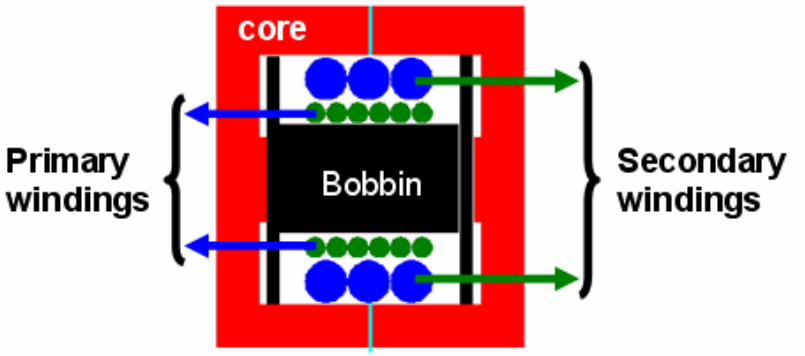

Figure 4.5.2 PC44EE16-Z Transformer Model

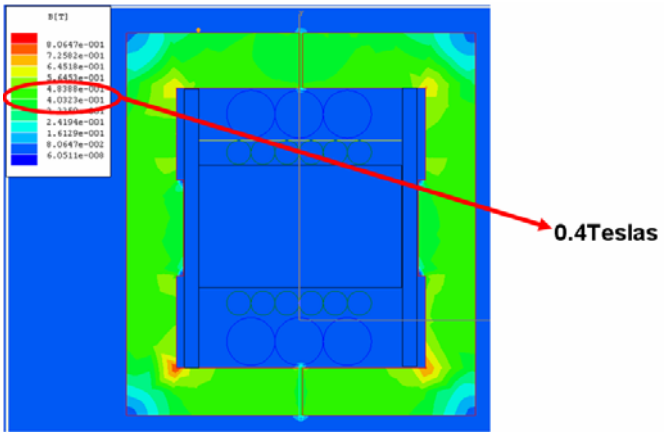

Figure 4.5.3 PC44EE16-Z Transformer Simulation

As shown from Figure 4.5.3, the core was saturated, and therefore this transformer could not be used. Added to the above, the transformer offered 0.7 coupling at maximum, making it a high leakage and saturated core. The circuit was built and tested, and Figure 4.5.4 shows the prototype.

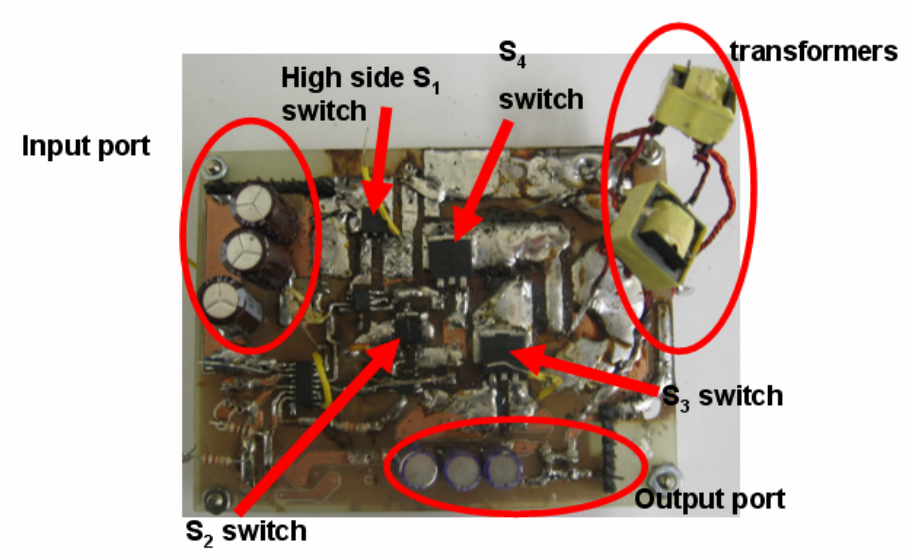

Figure 4.5.4 Prototype #1 with PC44EE16-Z Transformer

The waveforms obtained from the prototype in Figure 4.5.4 are shown in Figure 4.5.5.

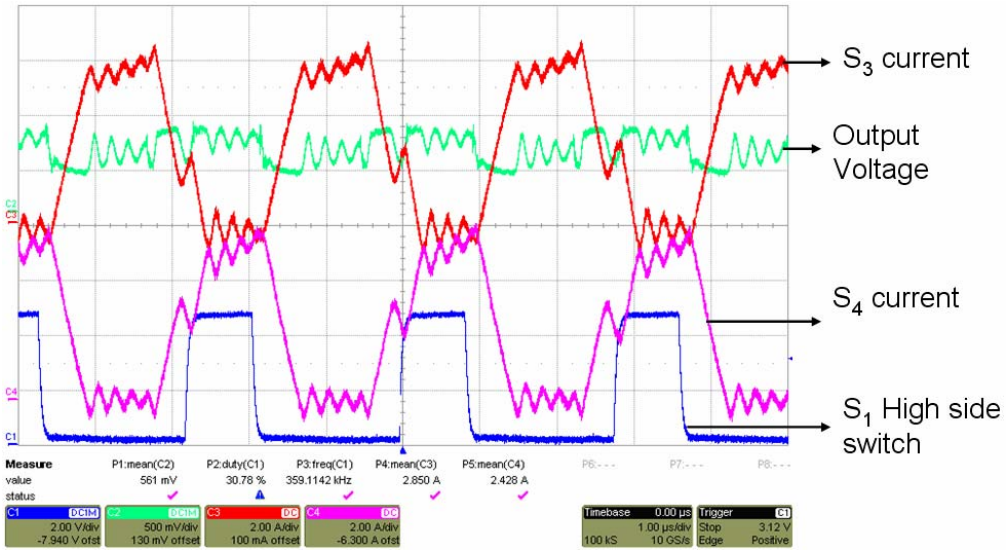

Figure 4.5.5 Experimental Results Using PC44EE16-Z

The magnetizing current and output voltage ripples are not accepted, and another transformer was built and tested.

The second transformer was a planar transformer to reduce the leakage. A PC95ELT18/07.3Z core was used with two windings at the primary side and one at the secondary side as shown in Figure 4.5.6.

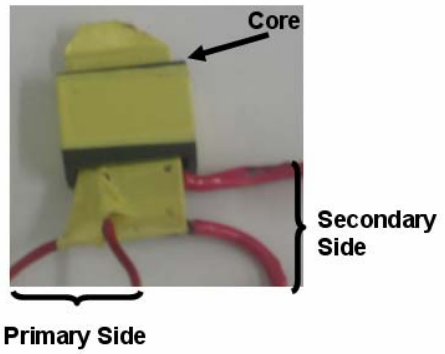

Figure 4.5.6 PC95ELT18/07.3Z Transformer

The transformer model and simulation results are shown in Figures 4.5.7 and 4.5.8.

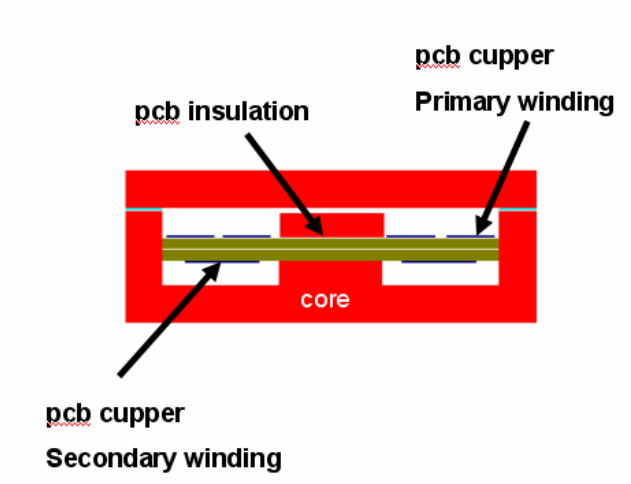

Figure 4.5.7 PC95ELT18/07.3Z Transformer Model

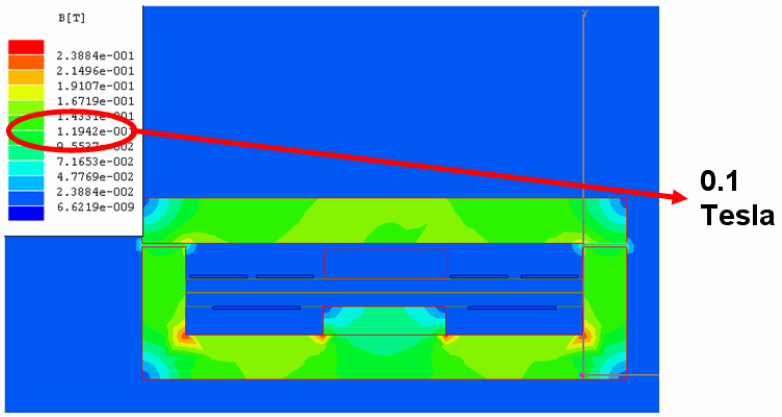

Figure 4.5.8 PC95ELT18/07.3Z Transformer Simulation

The measured leakage was 0.9, which is better than the previous transformer, but the topology was still sensitive. Circuit simulation showed that 0.96 coupling was needed as a minimum, and thus a small snubber was added with the planar transformer mounted on a new board as shown in Figure 4.5.9. The experimental waveforms in Figure 4.5.10 were as follows.

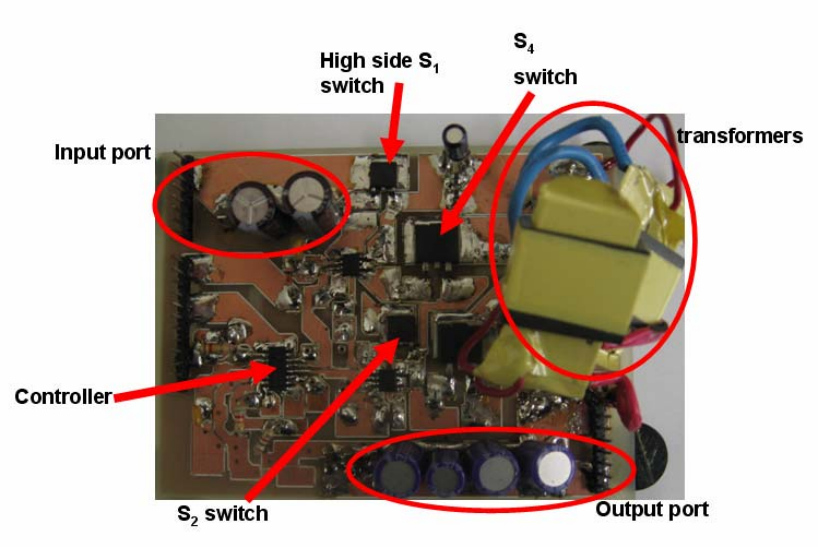

Figure 4.5.9 Prototype #2 with PC95ELT18/07.3Z Transformer

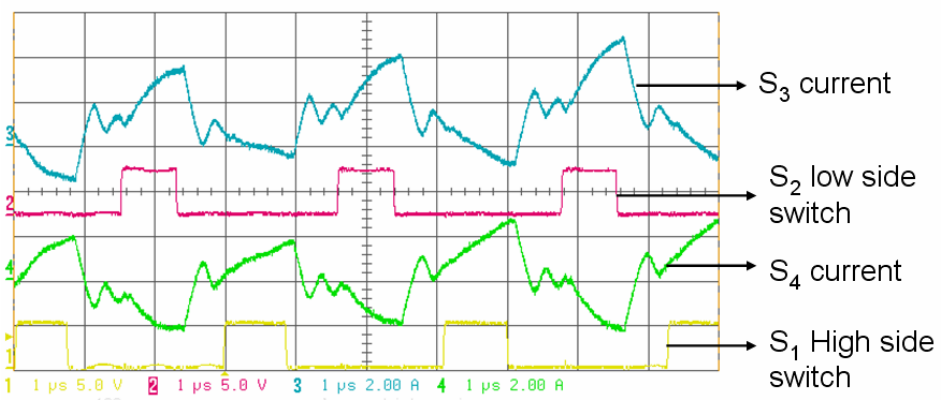

Figure 4.5.10 Experimental Results Using PC95ELT18/07.3Z

As shown from the waveforms above, the current ripple was less than before, but the output voltage still experienced a lower value due to the losses added by the snubber.

4.6 Chapter Recap

This chapter focused on the technical issues of the prototype, and the first part discussed some important magnetic issues and design. The second part was the experimental aspect. Two transformers were built, simulated and mounted on prototype boards, and waveforms were examined. The first winded transformer had low coupling, high leakage, and simulation showed that the core was saturated. A planar transformer was investigated, built, simulated and tested.

In both cases, a prototype was built for each transformer, and the following components were also used:

ISL 6558 controller

ISL 6612 drivers

IRL3716, 20 Volts MOSFETS for the low side switches: S_3 and S_4.

IRLR 7843, 30 Volts MOSFETS for the high side switches: S_1 and S_2.

The topology showed clear dependency on leakage, and a solid and tightly designed transformer is needed, where interleaving multilayered integrated magnetics offer a solution for this leakage dependency.

CHAPTER 5

MULTIPHASE BUCK

5.1 Introduction

Voltage Regulator Modules were based on stepping the input voltage down to a desired output level. Hence, single conventional Buck converters, shown in Figure 5.1.1, are the building block of any VRM [23].

Conventional synchronous Buck-based VRMs suffer the trade off between transient response and efficiency. For faster transient response, smaller inductance is needed, which increases the current ripple and consequently decreases efficiency. Higher filter inductances will decrease current ripple. Nevertheless, it will limit the dynamic response of the converter [43].

Numerous output capacitors were needed to smooth out the output voltage spikes, which took a lot of the available space on the motherboard and increased the cost.

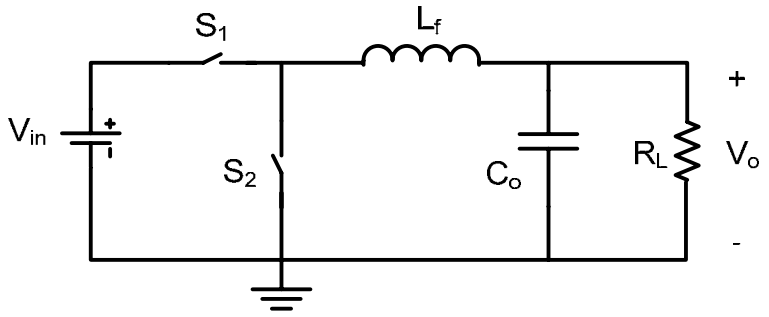

Figure 5.1.1 Single Phase Buck Converter

Many efforts were dedicated to lower the output capacitors and push the switching frequency into higher ranges.

The load varies with high slew rates, which need the capacitors to supply the load in all cases with the appropriate necessary current as fast as possible to reduce any unwanted high spikes. Many have addressed the issue of quantitively specifying the output spikes in order to study the effect of the output capacitors on the overall system [43].

The space on the motherboard was almost fully occupied, with the filtering capacitors increasing the price and restricting the transient response. The effect of adding more capacitors will be limited by the inductance of the trace [25]. Methods for decreasing those capacitor filters and increasing the transient response while maintaining low current ripple and high efficiency were investigated continuously.

Multiphase buck was one big step in the goal of decreasing the current ripple with interleaving phases and switching peaks to smooth out the total output current ripple [16, 24, and 40]. Interleaving efficiently decreased the current ripple, which allowed for smaller inductances to be used to enhance the transient response. The smaller the current ripples are then the smaller the output voltage spikes will be. And the less the filter capacitors are needed, the less the price will be. Therefore, interleaving became almost inevitable in VRM systems.

Figure 5.1.2 shows a conventional multiphase buck converter.

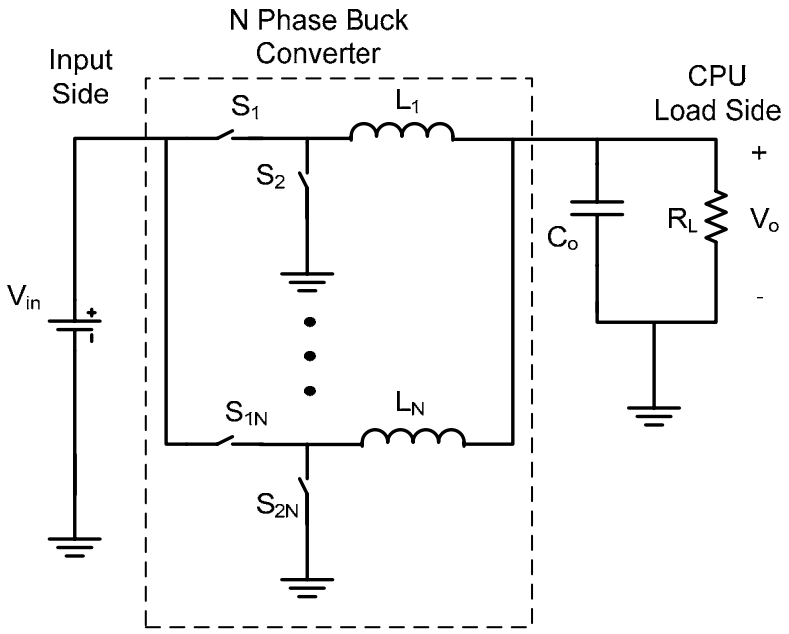

Figure 5.1.2 Conventional Multiphase Buck Converter

With the current ripple reduction, which interleaving offered, the use of smaller inductance became very beneficial for high slew rate currents and faster dynamics, allowing for less output capacitors to meet the transient requirements.

In summary, multiphase converters not only helped the current ripple improve, but consequently led to output capacitor reduction. Also, it paved the way for higher switching frequencies to come into play with all their accompanying advantages including lowering the inductance and boosting the transient response [23, 44].

The benefits of using multiphase buck are not offered for free. For current ripples to be cancelled, narrow duty cycles are needed, which harms the efficiency greatly as shown in Figure 5.1.3. It can be noted that stepping the voltage from 12Volts down to one Volt imposes a very small duty cycle.

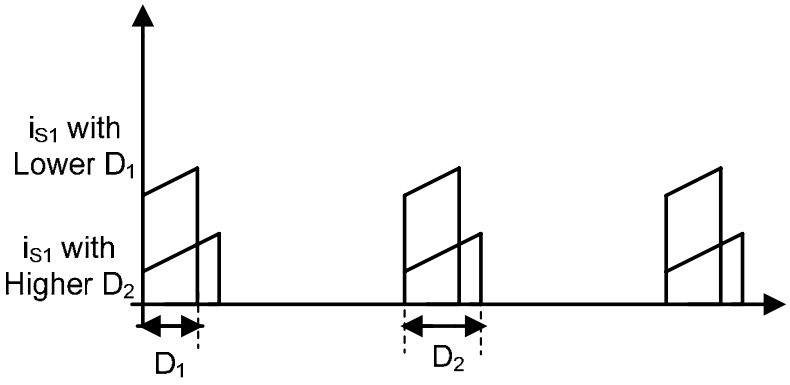

Figure 5.1.3 The Top Switch Current and Duty Cycle Relation

This problem not only initiated optimization need in converter operation but also released another important research field in device optimization. As clearly determined from Figure 5.1.3, the switching losses in the upper switch are more severe than the conduction losses, whereas the opposite scenario applies on the lower switch. This dictates the need for a low R_{dson} switch at the bottom switch and a small gate capacitance device at the top switch. Efforts are put into that filed of device optimization [44].

Thorough analysis and studies highlight the impact of higher bandwidth to achieve faster transient response, and other studies show the importance of output impedance as another aspect.

In a similar analogy, increasing the output capacitor will be limited by the inductance of the trace and will no further help to decrease the voltage spikes. In a parallel and equivalent logic, increasing the inductance value will face a threshold beyond which smaller inductance will have no further effect on either the slew rate or the transient response as long as the control loop bandwidth is constant [25].

5.2 Conventional Multiphase Buck

A buck converter is the main building block of any VRM. It is the simplest dc-dc converter found on all motherboards, and it steps the voltage down from 12 Volts to nearly one Volt for microprocessor applications.

To start with, let us investigate the well known single phase buck, which is shown in Figure 5.2.1 with its driving and key waveforms.

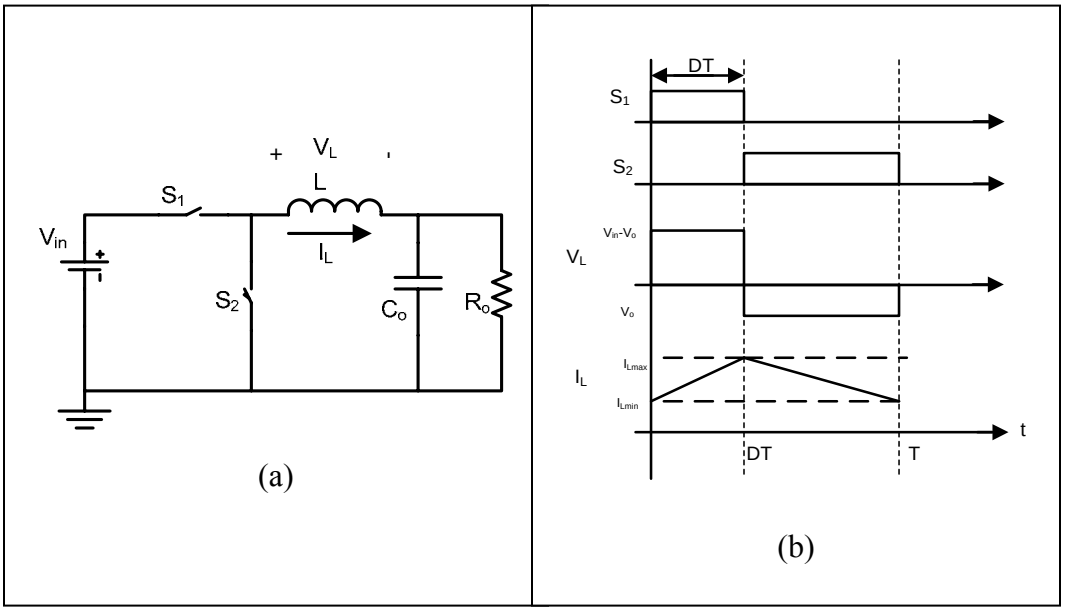

Figure 5.2.1 Single Phase Buck (a) Circuit and (b) Switching and Inductor Waveforms

As already available in literature, this converter operates in two modes.

Mode I:

$$I_{L\_1} = \frac{(V_{in} - V_o)}{L}(DT) + I_{L\min}$$

Mode II:

$$I_{L\_2} = \frac{-V_o}{L} \cdot (1-D)T + I_{L\max}$$

With its minimum and maximum values as:

$$I_{L\min} = V_{in} D(\frac{1}{R_o} - \frac{T(1-D)}{L})$$

$$I_{L\max} = V_{in} D(\frac{1}{R_o} + \frac{T(1-D)}{L})$$

And average current:

$$I_{L\_avg} = \frac{(I_{L\max} + I_{L\min})}{2} = I_o = \frac{V_o}{R_o} = \frac{V_{in} D}{R_o}$$

A multiphase buck converter overrides its counterpart single phase for the benefits of reducing the output current ripple to values that allow the use of smaller inductance values and hence increase the transient response.

Conventional multiphase has the following characteristics:

- Same V_{in}
- Same inductance
- Therefore, the same slopes for I_L
- For ripple cancellation: V_o=D*V_{in}
- Where D=$1/n$
- And n is the number of phases

Shown in Figure 5.2.2 is the conventional multiphase circuit with its driving and important waveforms.

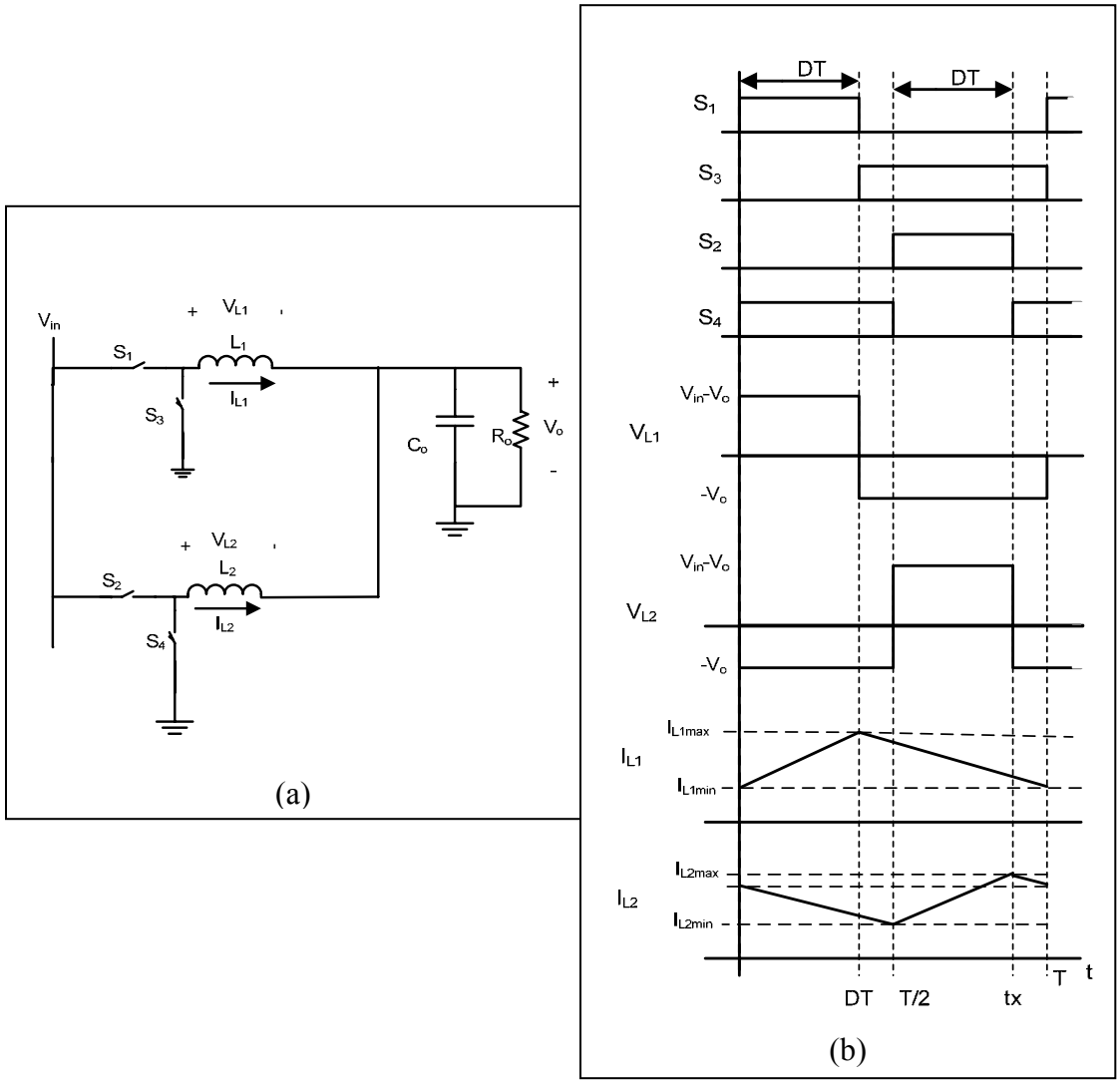

Figure 5.2.2 Conventional Multiphase Phase Buck (a) Circuit and (b) Key Waveforms

Conventional multiphase buck is explained in literature, and in concept, multiphase buck is merely a repetition of a single-phase buck with $360^{o}/n$ phase shift, where n in the

number of phases. Therefore, for the above two-phase buck, the following equations can be easily derived:

$$I_{L1\max} = \frac{I_o}{2} + \frac{(V_{in1} - V_o)DT}{2L_1}$$

And

$$I_{L1\min} = \frac{I_o}{2} - \frac{(V_{in1} - V_o)DT}{2L_1}$$

Similarly, for the second phase we have:

$$I_{L2\max} = \frac{I_o}{2} + \frac{(V_{in2} - V_o)DT}{2L_2}$$

And

$$I_{L2\min} = \frac{I_o}{2} - \frac{(V_{in2} - V_o)DT}{2L_2}$$

Each phase carries half the output voltage, hence the symmetry.

Intel has proposed a new, modified multiphase-buck, where the input voltages are not the same, and the duty cycle of each phase is different accordingly. Due to the resulting asymmetry, each phase will carry a different portion of the output current [45].

In the conventional multiphase buck converter, each phase will carry an average current equal to I_o/n.

where:

I_o is the average output current and n is the number of phases.

In the following non-conventional multiphase buck, each phase will carry an average current equal to I_{Ln_avg}/I_o.

where:

I_{Ln_avg} is the inductor average current of each phase, and I_o is the average output current.

In other words, for a two-phase non-conventional multiphase buck, the first phase carries an average current of I_{L1_avg}/I_o, and the second phase carries the rest which is equal to I_{L2_avg}/I_o.

We can define k_n to be the ratio of each phase average current to the total output current, i.e. $k_1 = I_{L1\_avg}/I_o$ and $k_2 = I_{L2\_avg}/I_o$ or $I_{L1\_avg} = k_1 I_o$ and $I_{L2\_avg} = k_2 I_o$

where: $k_1 + k_2 = 1$

In Figures 5.2.3 and 5.2.4, the circuit and driving signals are shown.

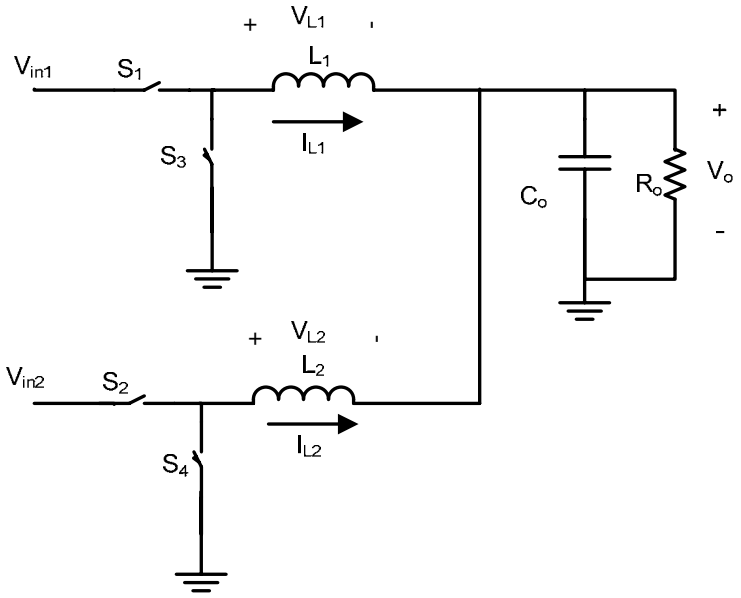

Figure 5.2.3 Multi-Input Multiphase Phase Buck Circuit Configuration

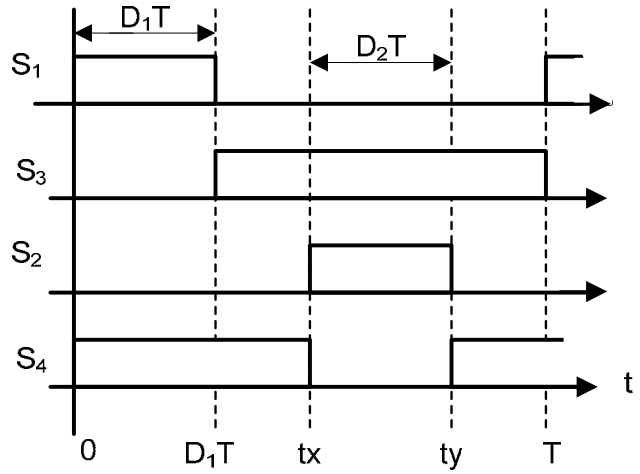

Figure 5.2.4 Multi-Input Multiphase Phase Buck Driving Waveforms

Where: $t_x = \frac{(1 + D_1 - D_2)T}{2}$ and $t_y = \frac{(1 + D_1 + D_2)T}{2}$

The general waveforms are shown in Figure 5.2.5.

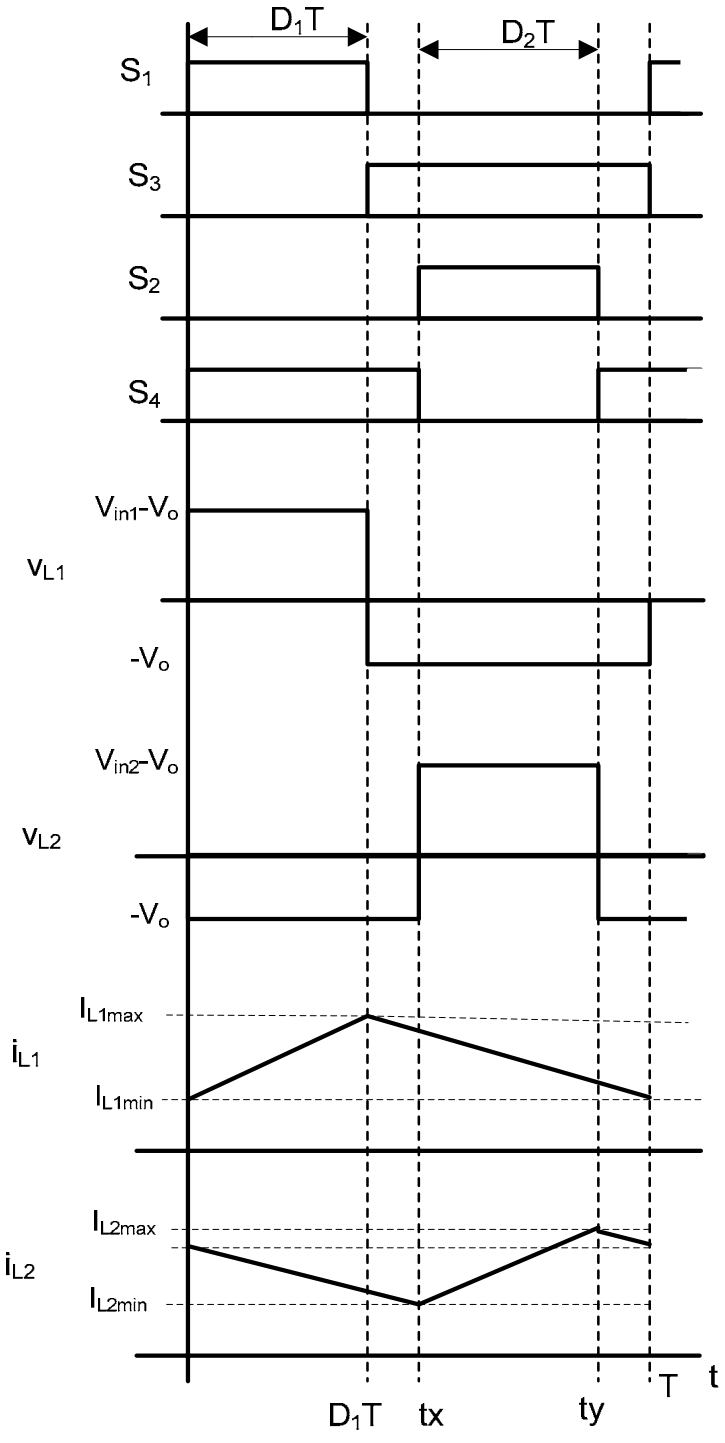

Figure 5.2.5 Multi-Input Multiphase Phase Buck Key Waveforms

The following expressions were derived and will be used in the subsequent analysis.

$$I_{L1\max} = k_1 I_o + \frac{(V_{in1} - V_o)D_1 T}{2L_1}$$

Where: $k_1 = I_{L1}/I_o$.

and $$I_{L1\min} = k_1 I_o - \frac{(V_{in1} - V_o)D_1 T}{2L_1}$$

Similarly, for the second phase we have;

$$I_{L2\max} = k_2 I_o + \frac{(V_{in2} - V_o)D_2 T}{2L_2}$$

$k_2 = I_{L2}/I_o = 1-k_1$

$$I_{L2\min} = k_2 I_o - \frac{(V_{in2} - V_o)D_2 T}{2L_2}$$

and

$$I_{L2}(0) = \frac{I_{L2\min} \cdot (1 - D_1 - D_2) + I_{L2\max}(1 + D_1 - D_2)}{2(1 - D_2)}$$

The average inductor current in each phase is:

$$I_{L1\_avg} = \frac{(I_{L1\max} + I_{L1\min})}{2} = k_1 I_o$$

and

$$I_{L2\_avg} = \frac{(I_{L2\max} + I_{L2\min})}{2} = k_2 I_o$$

It is also known that:

$$I_{L1\_avg} + I_{L2\_avg} = \frac{(I_{L1\_\max} + I_{L1\_\min})}{2} + \frac{(I_{L2\_\max} + I_{L2\_\min})}{2} = I_o = \frac{V_o}{R_o}$$

From which we can state that:

$$k_1 = \frac{1}{1 + \frac{I_{L2\_avg}}{I_{L1\_avg}}} , \qquad k_2 = \frac{1}{1 + \frac{I_{L1\_avg}}{I_{L2\_avg}}}$$

5.3 Steady-State Analysis

5.3.1 Gain Equation

i) 1st Phase:

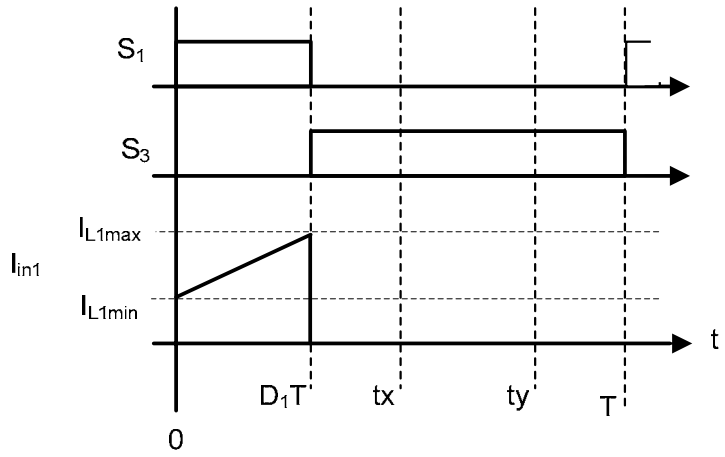

Figure 5.3.1 Phase One Driving and Inductor Waveforms

The average input energy is given by;

$$E_{in1} = \int_0^{D_1 T} \left(i_{in1}(t) \cdot V_{in1} \right) \cdot dt$$

Substituting the input current of the 1st phase we get;

$$= V_{in1} \cdot \int_0^{D_1 T} \left[\left(\frac{V_{in1} - V_o}{L_1} \right) \cdot t + I_{L1\min} \right] \cdot dt$$

$$E_{in1} = V_{in1} \cdot (D_1 T) \cdot k_1 \cdot I_o$$

ii) 2nd Phase:

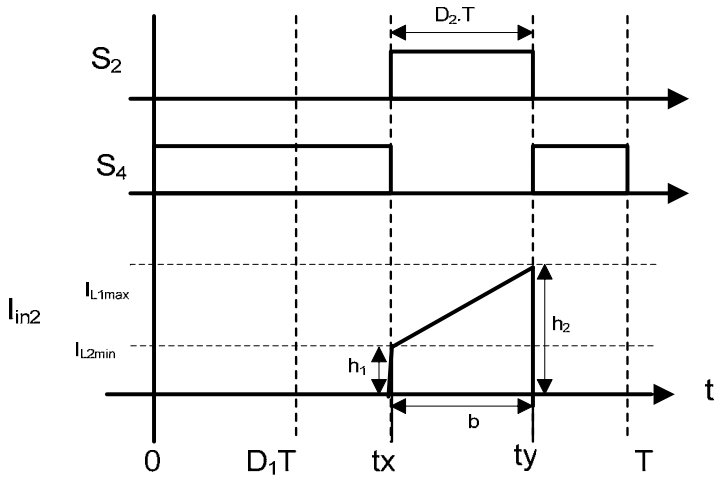

Figure 5.3.2 Phase Two Driving and Inductor Waveforms

The average input energy of the 2nd phase is given by;

$$E_{in2} = \int_{t_x}^{t_y} (i_{in2}(t) \cdot V_{in2}) \cdot dt$$

Examining Figure 5.3.2, the average of the waveform can be written as;

$= V_{in2}$ * area of the trapezoid

Substituting the area of the trapezoid from Figure 5.3.2 we get;

$= V_{in2}$ * b $(h_1+h_2)/2$

$$= V_{in2} \cdot \left[\frac{(D_2 T) \cdot (I_{L2\min} + I_{L2\max})}{2} \right]$$

The average input energy of the 2nd phase can be written by;

$$E_{in2} = V_{in2} \cdot (D_2 T) \cdot (k_2 \cdot I_o)$$

The total average input energy is: $E_{in} = E_{in1} + E_{in2}$

Substituting for E_{in1} and E_{in2} we get;

$$E_{in} = V_{in1} \cdot D_1 T \cdot k_1 I_o + V_{in2} \cdot D_2 T \cdot k_2 I_o$$
$$E_{in} = T \cdot I_o \cdot \left(V_{in1} \cdot D_1 \cdot k_1 + V_{in2} \cdot D_2 \cdot k_2\right)$$

And the average output energy is: $E_o = V_o \cdot I_o \cdot T$

Equating the terminal energy satisfying energy balance we get:

$$E_o = E_{in}$$
$$V_o \cdot I_o \cdot T = T \cdot I_o \cdot \left(V_{in1} \cdot D_1 \cdot k_1 + V_{in2} \cdot D_2 \cdot k_2\right)$$

The voltage gain can be written as;

$$V_o = \left(V_{in1} \cdot D_1 \cdot k_1 + V_{in2} \cdot D_2 \cdot k_2\right)$$

5.3.2 Ripple Calculation

To study the benefit of this new converter the ripple is calculated. From Figure 5.3.3 the ripple equation can be derived in a straightforward manner:

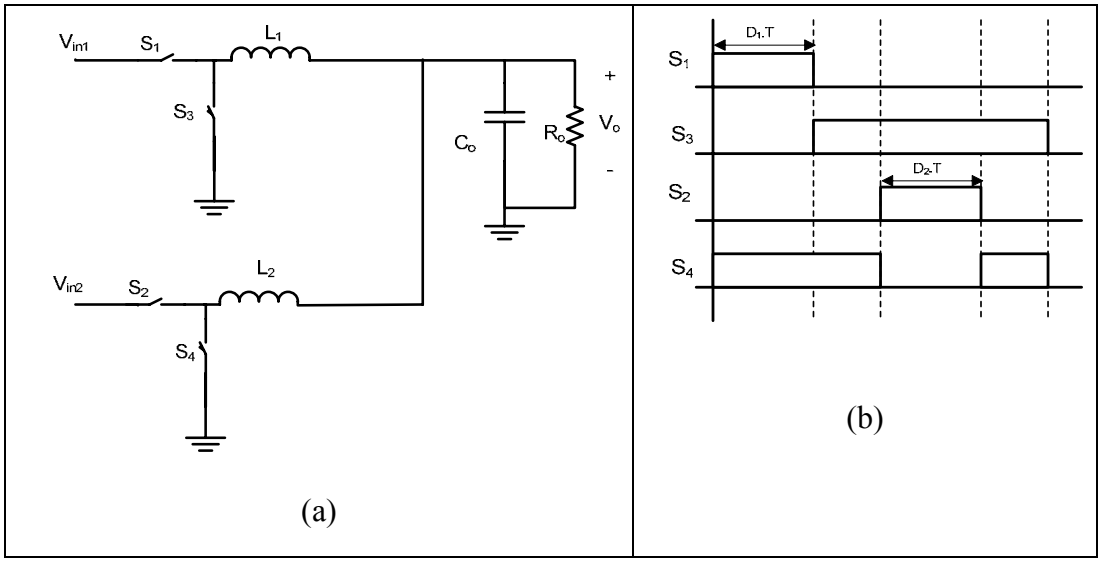

Figure 5.3.3 Multi-Input Multiphase Converter (a) Circuit and (b) Driving Signals

From the waveforms shown in Figure 5.3.3, the inductors currents can be written as:

The inductor current in the 1st phase can be written as;

$$i_{L1}(t)=\begin{cases}\left(\frac{V_{in1}-V_o}{L_1}\right)\cdot t+I_{L1\min}\rightarrow 0\le t<D_1T\\ \left(\frac{-V_o}{L_1}\right)\cdot\left(t-D_1T\right)+i_{L1}\left(D_1T\right)\rightarrow D_1T\le t<\frac{(1+D_1-D_2)T}{2}\\ \left(\frac{-V_o}{L_1}\right)\cdot\left(t-\frac{(1+D_1-D_2)T}{2}\right)+i_{L1}\left(\frac{(1+D_1-D_2)T}{2}\right)\rightarrow \frac{(1+D_1-D_2)T}{2}\le t<\frac{(1+D_1+D_2)T}{2}\\ \left(\frac{-V_o}{L_1}\right)\cdot\left(t-\frac{(1+D_1+D_2)T}{2}\right)+i_{L1}\left(\frac{(1+D_1+D_2)T}{2}\right)\rightarrow \frac{(1+D_1+D_2)T}{2}\le t<T\end{cases}$$

Where: $i_{L1}(D_1\cdot T)=I_{L1\max}$ and $i_{L1}(0)=i_{L1}(T)=I_{L1\min}$

And $I_{L1\max}=k_1I_o+\frac{\left(V_{in1}-V_o\right)\cdot D_1T}{2\cdot L_1}$, $\qquad I_{L1\min}=k_1I_o-\frac{\left(V_{in1}-V_o\right)\cdot D_1T}{2\cdot L_1}$

The inductor current in the 2nd phase is:

$$i_{L2}(t)=\begin{cases}\left(\frac{-V_o}{L_2}\right)\cdot t+I_{L2}(0)\rightarrow 0\le t<D_1T\\ \left(\frac{-V_o}{L_2}\right)\cdot\left(t-D_1T\right)+i_{L2}\left(D_1T\right)\rightarrow D_1T\le t<\frac{(1+D_1-D_2)T}{2}\\ \left(\frac{V_{in2}-V_o}{L_2}\right)\cdot\left(t-\frac{(1+D_1-D_2)T}{2}\right)+i_{L2}\left(\frac{(1+D_1-D_2)T}{2}\right)\rightarrow \frac{(1+D_1-D_2)T}{2}\le t<\frac{(1+D_1+D_2)T}{2}\\ \left(\frac{-V_o}{L_2}\right)\cdot\left(t-\frac{(1+D_1+D_2)T}{2}\right)+i_{L2}\left(\frac{(1+D_1+D_2)T}{2}\right)\rightarrow \frac{(1+D_1+D_2)T}{2}\le t<T\end{cases}$$

Where: $i_{L2}\left[\frac{(1+D_1-D_2)T}{2}\right]=I_{L2\min}$ and $i_{L2}\left[\frac{(1+D_1+D_2)T}{2}\right]=I_{L2\max}$

$$I_{L2}(0)=\frac{I_{L2\min}\cdot\left(1-D_1-D_2\right)+I_{L2\max}\cdot\left(1+D_1-D_2\right)}{2\cdot\left(1-D_2\right)}$$

And $I_{L2\max} = k_2 I_o + \dfrac{(V_{in2} - V_o)\cdot D_2 T}{2\cdot L_2}$, $\qquad I_{L2\min} = k_2 I_o - \dfrac{(V_{in2} - V_o)\cdot D_2 T}{2\cdot L_2}$

The total inductor current is expressed as $i_L(t)$

$$i_L(t) = i_{L1}(t) + i_{L2}(t)$$

Substituting fir $i_{L1}(t)$ and $i_{L2}(t)$ we get;

$$i_L(t) = \begin{cases} \left(\frac{V_{in1} - V_o}{L_1} - \frac{V_o}{L_2}\right)\cdot t + I_{L1\min} + I_{L2}(0) \rightarrow 0 \le t < D_1 T \\ -V_o\left(\frac{1}{L_1} + \frac{1}{L_2}\right)\cdot (t - D_1 T) + i_{L1}(D_1 T) + i_{L2}(D_1 T) \rightarrow D_1 T \le t < \frac{(1 + D_1 - D_2)T}{2} \\ \left(\frac{V_{in2} - V_o}{L_2} - \frac{V_o}{L_1}\right)\cdot \left(t - \frac{(1 + D_1 - D_2)T}{2}\right) + i_{L1}\left(\frac{(1 + D_1 - D_2)T}{2}\right) + i_{L2}\left(\frac{(1 + D_1 - D_2)T}{2}\right) \rightarrow \frac{(1 + D_1 - D_2)T}{2} \le t < \frac{(1 + D_1 + D_2)T}{2} \\ -V_o\left(\frac{1}{L_1} + \frac{1}{L_2}\right)\cdot \left(t - \frac{(1 + D_1 + D_2)T}{2}\right) + i_{L1}\left(\frac{(1 + D_1 + D_2)T}{2}\right) + i_{L2}\left(\frac{(1 + D_1 + D_2)T}{2}\right) \rightarrow \frac{(1 + D_1 + D_2)T}{2} \le t < T \end{cases}$$

The total current ripple in the inductor current is defined by;

$$\Delta I_L = i_L\left[\frac{(1 + D_1 + D_2)T}{2}\right] - i_L\left[\frac{(1 + D_1 - D_2)T}{2}\right]$$

Substituting the above values, the ripple equation can be written, after mathematical manipulation, as:

$$\Delta I_L = \left[\frac{(V_{in2} - V_o)}{L_2} - \frac{V_o}{L_1}\right]\cdot (D_2 T)$$

Equating the end of the total current, and maintaining volt-balance, we get:

$$i_L(0) = i_L(T)$$

where: $i_L(0) = I_{L1\_\min} + I_{L2}(0)$

and $\qquad i_L(T) = \dfrac{-V_o}{L_1}\cdot (1 - D_1)T + \Delta I_{L1} + \Delta I_{L2} + \dfrac{-V_o}{L_2}\cdot (1 - D_2)T + I_{L1\_\min} + I_{L2}(0)$

We get:

$$\Delta I_{L1} + \Delta I_{L2} = \frac{V_o}{L_1}\cdot (1 - D_1)T + \frac{V_o}{L_2}\cdot (1 - D_2)T$$

We know that: $\Delta I_{L1} = \left(\frac{V_{in1} - V_o}{L_1} \right) D_1 T$ and $\Delta I_{L2} = \left(\frac{V_{in2} - V_o}{L_2} \right) D_2 T$

We end up with:

$$\frac{(V_{in1} D_1 - V_o)}{L_1} = \frac{(V_o - V_{in2} D_2)}{L_2}$$

From the gain equation, we get: $V_o = (V_{in1} \cdot D_1 \cdot k_1 + V_{in2} \cdot D_2 \cdot k_2)$ and the fact that $k_1+k_2=1$, we get after equation manipulation.

$V_{in1} D_1 = V_{in2} D_2$

Engaging the above results in a MathCAD sheet we get the analysis in the next section.

5.3.3 Analysis

Considering an example with the following design specifications:

$V_{in1} = 12V$	$k_1 = 0.3$	$L_1 = 1uH$
$V_{in2} = 8V$	$V_o = 1.5V$	$L_2 = 0.45uH$
$D_1 = 0.187$	$f_{sw} = 300kHz$	$I_o = 20$
$D_2 = 0.125$		

We get the following waveforms shown in Figures 5.3.4, 5.3.5 and 5.3.6.

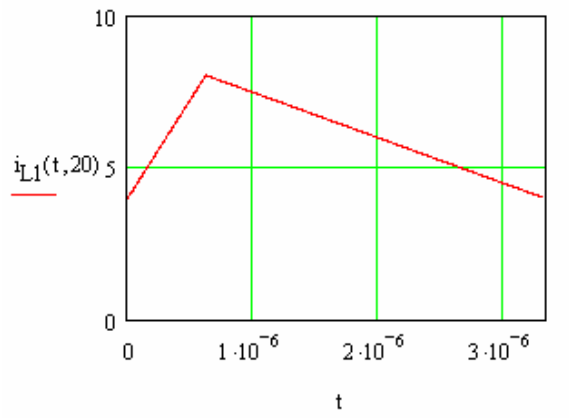

Figure 5.3.4 Inductor Current in Phase 1 of a Two-Input Two-Phase Converter

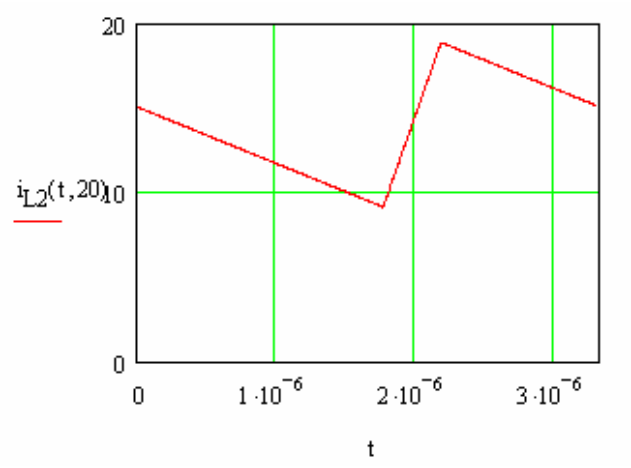

Figure 5.3.5 Inductor Current in Phase 2 of a Two-Input Two-Phase Converter

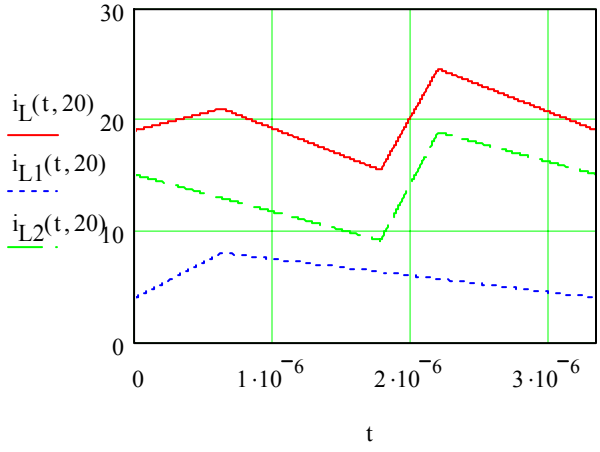

Figure 5.3.6 Total Inductors Current in a Two-Input Two-Phase Converter

5.4 Small Signal Modeling

Critical loads such as microprocessors need to have a well-regulated, tightly maintained constant voltage regardless of the input or output variations in input voltage or output load. These variations are a physical behavior that needs to be mathematically quantified in order to study their effect on the output voltage and to try and regulate them. Modeling is a mathematical description of physical activities based upon which a solid control design can be achieved through a deep understanding of the relation between those variations and the desired constant output voltage by focusing on prevailing actions and ignoring small non dominant behavior, i.e., neglecting high frequency components and switching harmonics in turn will simplify the design but, on the other hand, will give missing data.

Averaging is the mathematical tool that smoothes out ripple and harmonic switching, thus averaging will be the adopted approach. This averaging technique creates a set of non-linear differential equations which need to be linearized before applying control theory by the means of small signal modeling.

To derive the small signal modeling, we care about the energy storage elements in the circuit, which are two inductors and a filtering capacitor;

For the two inductors, we have the voltage across them according to the waveforms shown in Figure 5.4.1.

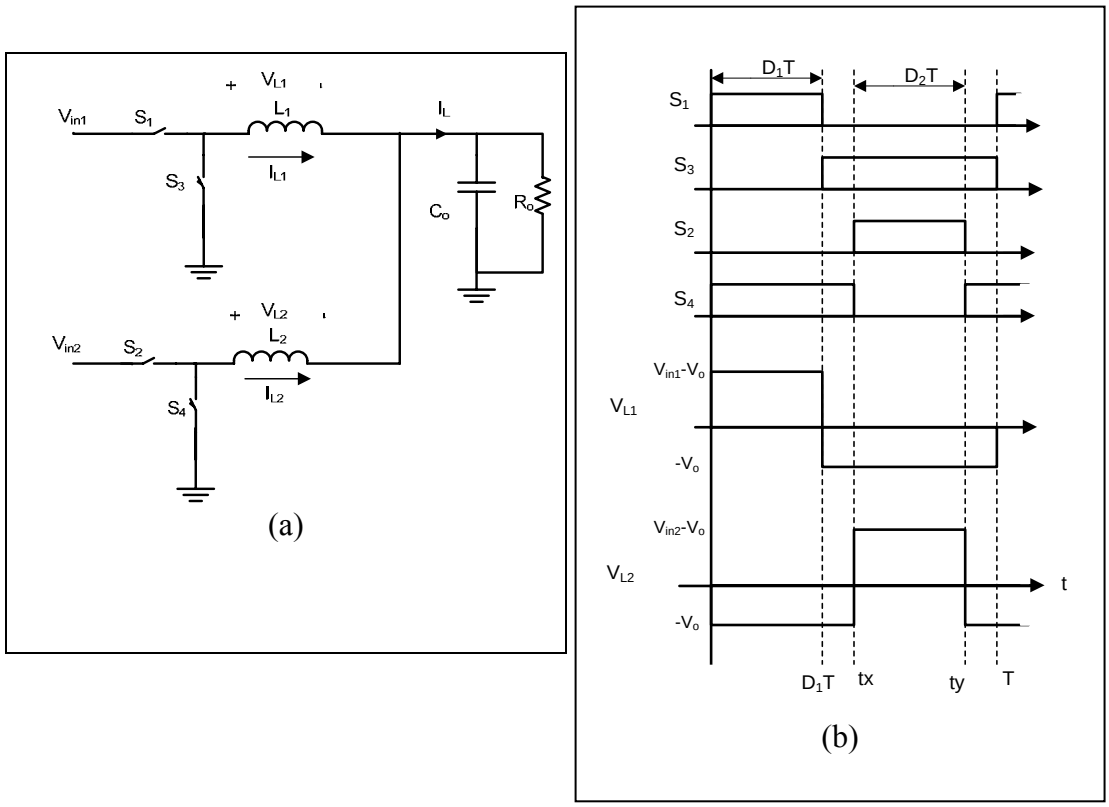

Figure 5.4.1 Multi-Input Two-Phase Buck (a) Circuit and (b) Inductor Voltages

Where: $t_x = (1 + D_1 - D_2)T/2$ and $t_y = (1 + D_1 + D_2)T/2$

The voltages across the inductors and the current through the capacitor can be written as follows:

$$L_1 \frac{di_{L1}(t)}{dt} = \begin{cases} v_{in1}(t) - v_o(t) \rightarrow 0 \le t \le D_1 T \\ -v_o(t) \rightarrow D_1 T \le t \le (1 + D_1 - D_2)T/2 \\ -v_o(t) \rightarrow (1 + D_1 - D_2)T/2 \le t \le (1 + D_1 + D_2)T/2 \\ -v_o(t) \rightarrow (1 + D_1 - D_2)T/2 \le t \le T \end{cases}$$

$$L_2 \frac{di_{L2}(t)}{dt} = \begin{cases} -v_o(t) \rightarrow 0 \le t \le D_1 T \\ -v_o(t) \rightarrow D_1 T \le t \le (1 + D_1 - D_2)T/2 \\ v_{in2}(t) - v_o(t) \rightarrow (1 + D_1 - D_2)T/2 \le t \le (1 + D_1 + D_2)T/2 \\ -v_o(t) \rightarrow (1 + D_1 - D_2)T/2 \le t \le T \end{cases}$$

$$C_o \frac{dv_{Co}(t)}{dt} = \begin{cases} i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R_o} \rightarrow 0 \le t \le D_1 T \\ i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R_o} \rightarrow D_1 T \le t \le (1 + D_1 - D_2)T/2 \\ i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R_o} \rightarrow (1 + D_1 - D_2)T/2 \le t \le (1 + D_1 + D_2)T/2 \\ i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R_o} \rightarrow (1 + D_1 - D_2)T/2 \le t \le T \end{cases}$$

The above results can be restated in each mode of operation as state space representation in the following forms.

During the first mode of operation:

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_o \end{bmatrix} \begin{bmatrix} \dfrac{di_{L1}(t)}{dt} \\ \dfrac{di_{L2}(t)}{dt} \\ \dfrac{dv_{Co}(t)}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & \dfrac{-1}{R_o} \end{bmatrix}}_{A_1} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B_1} \begin{bmatrix} v_{in1}(t) \\ v_{in2}(t) \end{bmatrix} \Rightarrow D_1 T$$

During the second mode of operation:

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_o \end{bmatrix} \begin{bmatrix} \dfrac{di_{L1}(t)}{dt} \\ \dfrac{di_{L2}(t)}{dt} \\ \dfrac{dv_{Co}(t)}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & \dfrac{-1}{R_o} \end{bmatrix}}_{A_2} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B_2} \begin{bmatrix} v_{in1}(t) \\ v_{in2}(t) \end{bmatrix} \Rightarrow (1 - D_1 - D_2)T/2$$

During the third mode of operation:

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_o \end{bmatrix} \begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{Co}(t)}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & \frac{-1}{R_o} \end{bmatrix}}_{A_3} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix}}_{B_3} \begin{bmatrix} v_{in1}(t) \\ v_{in2}(t) \end{bmatrix} \Rightarrow D_2 T$$

During the forth mode of operation:

$$\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_o \end{bmatrix} \begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{Co}(t)}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & \frac{-1}{R_o} \end{bmatrix}}_{A_4} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{B_4} \begin{bmatrix} v_{in1}(t) \\ v_{in2}(t) \end{bmatrix} \Rightarrow (1 - D_1 - D_2)T/2$$

The output vectors are the two input currents, which are shown in Figure 5.4.2:

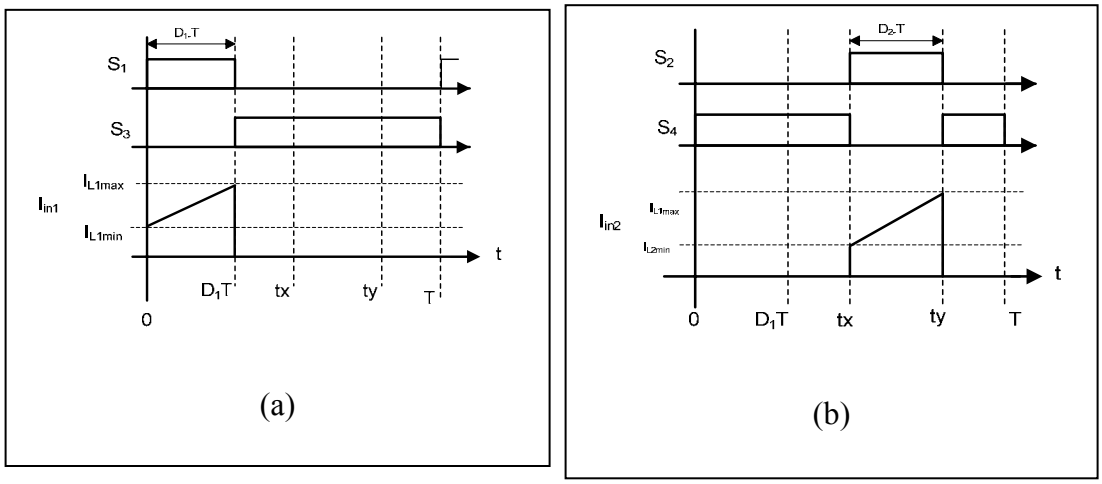

Figure 5.4.2 Input Current in (a) Phase One (b) Phase Two

The output state space vectors are the two input currents and can be easily shown to be the two following state space forms.

During the first mode of operation:

$$\begin{bmatrix} i_{in1}(t) \\ i_{in2}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{C_1} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} \Rightarrow D_1 T$$

During the second mode of operation:

$$\begin{bmatrix} i_{in1}(t) \\ i_{in2}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{C_2} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} \Rightarrow (1 - D_1 - D_2)T/2$$

During the third mode of operation:

$$\begin{bmatrix} i_{in1}(t) \\ i_{in2}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}}_{C_3} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} \Rightarrow D_2 T$$

During the forth mode of operation:

$$\begin{bmatrix} i_{in1}(t) \\ i_{in2}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{C_4} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{Co}(t) \end{bmatrix} \Rightarrow (1 - D_1 - D_2)T/2$$

The average state spaces matrices can be calculated from the above as follows;

$$A_{avg} = A_1 \cdot D_1 + A_2 \cdot (1 - D_1 - D_2)/2 + A_3 \cdot D_2 + A_4 \cdot (1 - D_1 - D_2)/2$$

$$B_{avg} = B_1 \cdot D_1 + B_2 \cdot (1 - D_1 - D_2)/2 + B_3 \cdot D_2 + B_4 \cdot (1 - D_1 - D_2)/2$$

$$C_{avg} = C_1 \cdot D_1 + C_2 \cdot (1 - D_1 - D_2)/2 + C_3 \cdot D_2 + C_4 \cdot (1 - D_1 - D_2)/2$$

The results are summarized as:

$$A_{avg} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & \dfrac{-1}{R_o} \end{bmatrix} \qquad B_{avg} = \begin{bmatrix} D_1 & 0 \\ 0 & D_2 \\ 0 & 0 \end{bmatrix} \qquad C_{avg} = \begin{bmatrix} D_1 & 0 & 0 \\ 0 & D_2 & 0 \end{bmatrix}$$

The result of perturbation and linearization is:

$$\hat{\dot{x}} = \underbrace{\left(A_{avg}\,\hat{x} + B_{avg}\,\hat{u} \right)}_{Line\ \mathrm{var}iation} + \underbrace{\left((A_1 - A_2)X + (B_1 - B_2)U \right)\hat{d}_1}_{duty\,1\ \mathrm{var}iation} + \underbrace{\left((A_3 - A_2)X + (B_3 - B_2)U \right)\hat{d}_2}_{duty\,2\ \mathrm{var}iation}$$

$$\hat{y} = \underbrace{\left(C_{avg}\,\hat{x} \right)}_{Line\ \mathrm{var}iation} + \underbrace{\left((C_1 - C_2)X \right)\hat{d}_1}_{duty\,1\ \mathrm{var}iation} + \underbrace{\left((C_3 - C_2)X \right)\hat{d}_2}_{duty\,2\ \mathrm{var}iation}$$

therefore, the small signal modeling equations of the energy storage, devices can be written as follows.

$$L_1 \frac{d\,\hat{i}_{L1}(t)}{dt} = -\hat{v}_o(t) + D_1\,\hat{v}_{in1}(t) + V_{in1}\,\hat{d}_1(t)$$

$$L_2 \frac{d\,\hat{i}_{L2}(t)}{dt} = -\hat{v}_o(t) + D_2\,\hat{v}_{in2}(t) + V_{in2}\,\hat{d}_2(t)$$

$$C_o \frac{d\,\hat{v}_{Co}(t)}{dt} = \hat{i}_{L1}(t) + \hat{i}_{L2}(t)_{in1} - \frac{\hat{v}_o(t)}{R_o}$$

The output equations are:

$$\hat{i}_{in1}(t) = D_1\,\hat{i}_{L1}(t) + k_1 I_o\,\hat{d}_1(t)$$

$$\hat{i}_{in2}(t) = D_2\,\hat{i}_{L2}(t) + k_2 I_o\,\hat{d}_2(t)$$

Transforming the equations into small signal modeling equivalent circuits will result in the circuits shown in Figures 5.4.3, 5.4.4, 5.4.5, 5.4.6 and 5.4.7

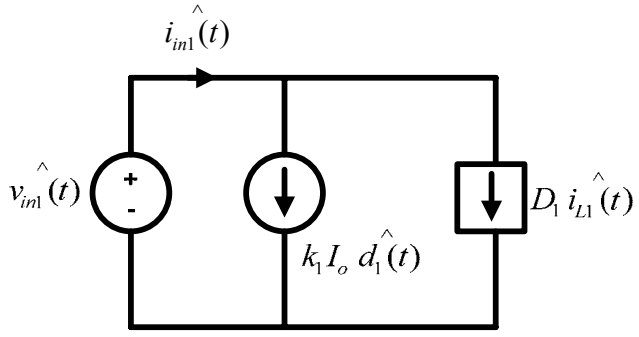

Figure 5.4.3 Input Current of the First Phase

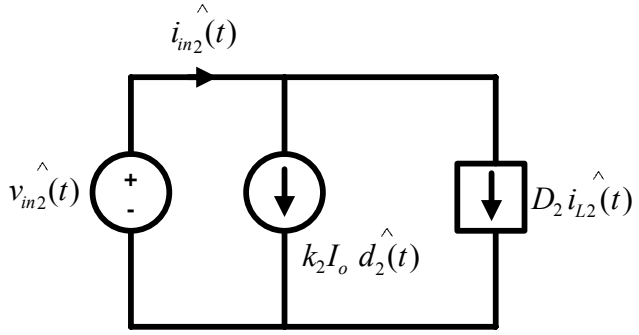

Figure 5.4.4 Input Current of the Second Phase

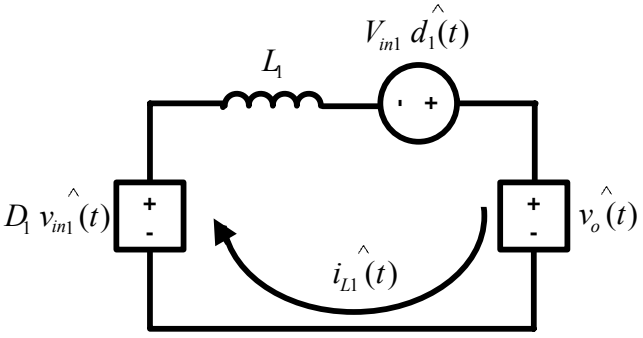

Figure 5.4.5 Energy Storage Element Number 1 (inductor in the first phase)

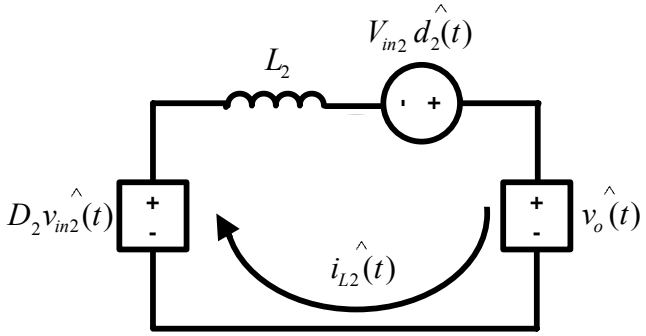

Figure 5.4.6 Energy Storage Element Number 2 (inductor in the second phase)

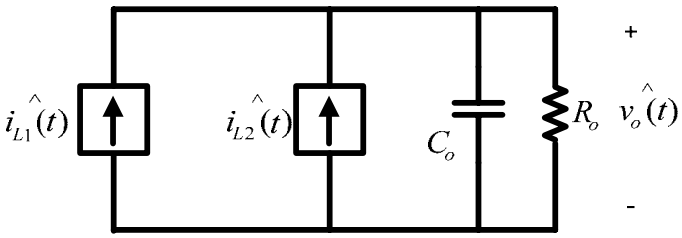

Figure 5.4.7 Energy Storage Element Number 3 (output filter capacitor)

From the perturbed equations, we get the transfer functions.

Output voltage to input voltage 1:

$$\frac{\hat{v}_o}{\hat{v}_{in1}} = \frac{R_o L_2 D_1}{s[\left(\left(s^2 C_o R_o + s\right)L_1 + R_o\right)L_2 + L_1 R_o]}$$

Output voltage to input voltage 2:

$$\frac{\hat{v}_o}{\hat{v}_{in2}} = \frac{R_o L_1 D_2}{s[\left(\left(s^2 C_o R_o + s\right)L_2 + R_o\right)L_1 + L_2 R_o]}$$

Output voltage to duty cycle 1:

$$\frac{\hat{v}_o}{\hat{d}_1} = \frac{V_{in1} R_o L_2}{\left(\left(s^2 C_o R_o + s\right)L_1 + R_o\right)L_2 + L_1 R_o}$$

Output voltage to duty cycle 2:

$$\frac{\hat{v}_o}{\hat{d}_2} = \frac{L_1 R_o V_{in2}}{\left(\left(s^2 C_o R_o + s\right)L_2 + R_o\right)L_1 + L_2 R_o}$$

Drawing the duty cycle transfer function;

Renaming: $\frac{\hat{v}_o}{\hat{d}_1} = G_{d1}$

And

$$\frac{\hat{v}_o}{\hat{d}_2} = G_{d2}$$

For the following specifications:

V_{in1} = 12V,
V_{in2} = 5V,
D_1 = 0.083,
D_2= 0.2

V_o = 1V,
I_o = 60A,

f_{sw} = 300kHz,
L_1 = 0.27uH,
L_2 = 0.57uH,

We get the following Bode plot shown in Figure 5.4.8:

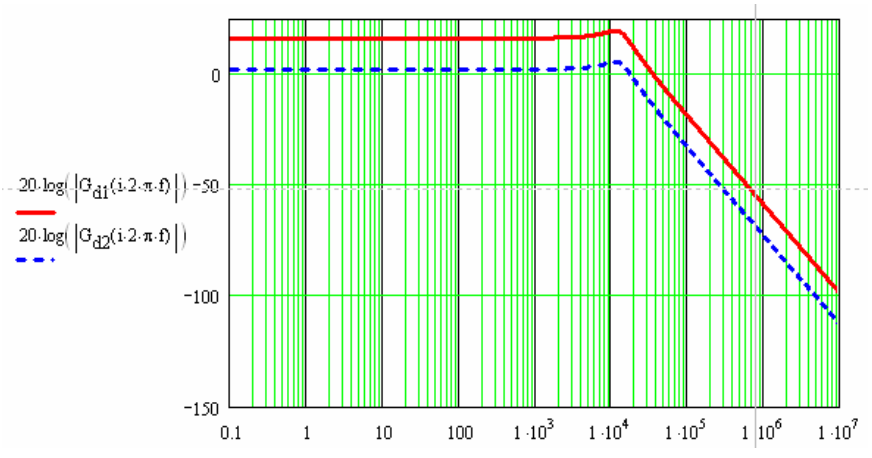

Figure 5.4.8 Bode Plot of a Two-Input Two-Phase Buck Converter

5.5 Chapter Recap

Multi-input port topologies are invading the research fields for their use in hand held devices. The VRM roadmap also predicts that the continuous output voltage will decrease with side-by-side increase in the current.

This chapter introduced a new Intel launch topology, with different input ports, and a detailed analysis with derived small signal modeling was presented.

Transfer functions obtained and bode plots are shown as paving the way for a control design that is inevitable and is accompanied with intriguing challenges to be addressed in other contexts.

CHAPTER 6

SUMMARY

6.1 Conclusion

Voltage Regulator Modules are faced by increasing challenges imposed on designers to propose a solution that takes care of all critical issues. The low core voltage needed to supplement high current and power densities are hard to meet due to the requirements of fast transient response and high switching frequency.

The motherboard space at the processor area is occupied with many different kinds of capacitors to alleviate the spikes at the load. This passive method is not as efficient and is space and cost limited. The aim of freeing the motherboard from these capacitors and maintaining a well-regulated, constant and spike-less voltage is the goal to be achieved for future VRM.

Step-down dc-dc Buck converters are the nucleus on which almost all topologies are based. Single-phase buck is not used per se; nevertheless, conventional multiphase presents balanced pros and cons. Some of the advantages it offers are lower inductance faster transient, enhanced thermal distribution and less ripples. In a way, it increases the efficiency, but on the other side of the comparison, conventional multiphase suffers some drawbacks, of which are; the inability of the current to quickly catch up with the fast slew rated load change. This results in voltage spikes, and the small duty cycle is inherited by the fact that the 12V input voltage is to be stepped down to the 1 V needed at that output. These downsides prevent the use of multiphase without injection means.

Current injection helped supply the load linearly with the current it needed during step-up and recovered it in switching means during step-down. The concept presents a logical solution, but the conduction and switching losses in the two modes it operates in reduces efficiency.

Voltage injection offered by ATVC, reduces conduction and switching losses through the use of a transformer that has a turns ratio that effectively reduces the current passing in the extra ATVC circuitry, which reduces both conduction and switching losses.

Small duty cycle, which is inevitable in the process of stepping the input voltage to the level required at the load side, is associated with efficiency impairing problems. The top MOSFET switching losses, the bottom MOSFET conduction losses, the asymmetric transient response and the failing operation at high frequency are a summary of the shortcomings of small duty ratio.

Transformer-based non-isolated topologies proposed a solution to such setbacks including tapped inductor, coupled buck converters and non-isolated Push Pull Converters to name a few. The leakage and control complication are issues of concern in the above converters.

This thesis presents a new topology — the Half-bridge Buck Converter — to extend the duty cycle and avoid the problems mentioned above, through the addition of two coupled inductors and two switches. The HBBC improves the transient response and increases efficiency.

The transformers can be integrated together to reduce size and cost. The two added MOSFETS are zero voltage switched, which cancels out switching losses. The

magnetizing inductances continuously supply the load and perform as a current doubler, which enhances the transient. The overall operation resembles that of a conventional two-phase buck, but the HBBC allows the use of a lower voltage rating MOSFETS for the extra switches with low R_{dson}, which surpasses the conventional two-phase buck.

High efficiency is the target of all designers. Light load compels another research interest, and multi-input converters are coming to the VRM field to straighten the efficiency curve especially at light load.

The work in this thesis also covers the derivation of a small-signal model of a new two-phase buck introduced by Intel.

6.2 Future Work

Optimizing the HBBC converter will be the scope of the future work as the Half-bridge Buck highly depends on the leakage of the transformer. For guaranteed better efficiency, the transformer should be designed with a minimum of 96% coupling. This leads to the use of multilayered interleaved planar transformers. Integrating the inductors also will help reduce the size of the overall converter.

Symmetric and asymmetric control schemes were examined in this thesis, although symmetric control was adopted. The duty-cycle shift is an attractive control to be applied on the HBBC to further reduce the losses and increase efficiency.

A design method to optimally choose the turns ratio of the transformer when control methods other than the symmetric is also another future scope work.

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