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Integrated Topologies And Digital Control For Satellite Power Management And Distribution Systems

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INTEGRATED TOPOLOGIES AND DIGITAL CONTROL FOR SATELLITE POWER MANAGEMENT AND DISTRIBUTION SYSTEMS

by

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ABSTRACT

This work is focused on exploring advanced solutions for space power management and distribution (PMAD) systems. As spacecraft power requirements continue to increase, paralleled by the pressures for reducing cost and overall system weight, power electronics engineers will continue to face major redesigns of the space power systems in order to meet such challenges. Front-end PMAD systems, used to interface the solar sources and battery backup to the distribution bus, need to be designed with increased efficiency, reliability, and power density.

A new family of integrated single-stage power converter structures is introduced here. This family allows the interface and control of multiple power sources and storage devices in order to optimize utilization of available resources. Employing single-stage power topologies, these converters control power flow efficiently and cost-effectively. This is achieved by modifying the operation and control strategies of isolated soft-switched half-bridge and full-bridge converters—two of the most popular two-port converter topologies. These topologies are reconfigured and utilized to realize three power processing paths. These paths simultaneously utilize the power devices, allowing increased functionality while promising reduced losses and enhanced power densities.

Each of the proposed topologies is capable of performing simultaneous control of two of its three ports. Control objectives include battery or ultra-capacitor charge regulation, solar array maximum power point tracking (MPPT), and/or bus voltage regulation. Another advantage of the proposed power structure is that current engineering design concepts can be used to optimize the

new topologies in a fashion similar to the mother topologies. This includes component selection and magnetic design procedures, as well as achieving soft-switching for increased efficiency at higher switching frequencies. Galvanic isolation of the load port through high-frequency transformers provides design flexibility for high step-up/step-down conversion ratios. It further allows the converters to be used as power electronics building blocks (PEBB) with outputs connected in different series/parallel combinations to meet different load requirements. Utilizing such converters promises significant savings in size, weight, and costs of the power management system as well as the devices it manages.

Chapter 1 of this dissertation provides an introduction to the requirements, challenges, and trends of space PMAD. A review of existing multi-port converter technologies and digital control techniques is given in Chapter 2. Chapter 3 discusses different PMAD system architectures. It outlines the basic concepts used for PMAD integration and discusses the potential for improvement. Chapters 4 and 5 present and discuss the operation and characteristics of three different integrated multi-port converters. Chapter 6 presents improved methods for practical digital control of switching converters, which are especially useful in complex multi-objective controllers used for PMAD. This is followed by conclusions and suggested future work.

To those who fear
but dare to stand,
and those who grieve
but dare to smile.

To the land of sad oranges…

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Hussam Al-Atrash

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LIST OF ACRONYMS

A-BI-PS-FB	Asymmetric boost-integrated phase-shift full-bridge
Ac	Alternating current
ADC	Analog-to-digital converter
APECOR	Advanced Power Electronics Corporation
ASIC	Application-specific integrated circuit
CCM	Continuous conduction mode
DAC	Digital-to-analog converter
Dc	Direct current
DCM	Discontinuous conduction mode
DCS-HB	Duty-cycle shifted half-bridge
DSP	Digital signal processor
EMI	Electromagnetic interference
FET	Field effect transistor
FloridaPEC	Florida Power Electronics Center
FPGA	Field-programmable gate array
HEV	Hybrid-electric vehicle
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
IncCond	Incremental conductance

IVR	Input voltage regulation
LHS	Left-hand side
LPF	Low-pass filter
LSB	Least significant bit
MPP	Maximum power point
MPPT	Maximum power point tracking
MSB	Most significant bit
NASA-GRC	National Aeronautics and Space Administration - Glenn Research Center
OVR	Output voltage regulation
PEBB	Power electronics building block
PFC	Power factor correction
PMAD	Power management and distribution
PnO	Perturb and observe
POL	Point-of-load
PS-FB	Phase-shift full-bridge
PWM	Pulse-width modulation
RHS	Right-hand side
Rms	Root-mean square
S-BI-PS-FB	Symmetric boost-integrated phase-shift full-bridge
SBIR	Small Business Innovation Research
SCBR	Series-Connected Boost Regulator
TM-HB	Tri-modal half-bridge
UCF	University of Central Florida

ZCS	Zero-current switching
ZOH	Zero-order hold
ZVS	Zero voltage switching

CHAPTER 1: INTRODUCTION

The Sun provides the energy necessary to support life on Earth. Thousands of miles above, it remains the primary source of energy. Solar radiation is the most abundant, convenient, and reliable source of energy for satellite systems. Battery energy storage is utilized in order to accommodate the mismatch between solar power availability and loading profiles.

The ever-increasing cost of launching a spacecraft into space, approximately $100,000/kg, is a major driving force behind the efforts to minimize the volume and weight of the different systems it comprises [1]. It is generally accepted that the platform power system constitutes around 25% of the total dry spacecraft mass, while the battery and the solar arrays account for 90% of the power system mass [2]. In this light, highly optimized utilization of the solar source and batteries is an important design concern. This calls for the use of flexible PMAD systems with advanced control.

1.1. Trends and Challenges of Satellite Power Management and Distribution

The state-of-the-art, trends, and challenges relating to the different components of satellite PMAD systems are discussed in this section.

1.1.1. Photovoltaics and Maximum Power Point Tracking

Photovoltaic (solar) cells are semiconductor devices capable of producing voltage and associated current when exposed to light. Solar cell technology has made significant progress over the last few decades. Crystalline silicon, both mono- and multi-crystalline, dominates the solar cell industry. This material is a poor absorber of light and requires a large thickness, but yields stable solar cells with good efficiencies (11-16%) and uses process technology developed from the vast knowledge base of the microelectronics industry [3]. Thin film technologies were developed to reduce cost by utilizing materials with better light absorption. Thin film materials include amorphous silicon and the polycrystalline materials: cadmium telluride and copper indium (gallium) diselenide. This technology still faces challenges in manufacturability, durability, and efficiency (5-8%). The potential for lower cost remains the main drive for thin film solar cells.

For space solar cells, constraints on size, weight, and reliability are far more critical than manufacturing cost. This has escalated the interest in complex high-efficiency cells for space applications. Multi-junction solar cell technologies target a wider portion of the incident spectrum and promise efficiencies in excess of 30% [4, 5]. The development of nano-materials also holds potential for the future.

The voltage-current relationship of a typical solar array is given by Equation (1.1): [6]

$$I = I_{photo} - I_o \cdot \left(\exp\left[\frac{q}{AKT} \cdot \left(V + I \cdot R_{series} \right) \right] - 1 \right) - \frac{V}{R_{shunt}} \tag{1.1}$$

where I_{photo} is the photo current generated due to insolation, I_o is the reverse saturation current of semiconductor material, R_{series} represents series ohmic resistance of the cell, R_{shunt} accounts for leakage current, K is Boltzman's constant, T is the absolute operating temperature, q

is the charge of a single electron, and A is an ideality factor of the p-n junction. Typical terminal characteristics of a solar array at different operating conditions are shown in Figure 1. The incremental resistance of the array is negative; that is, the current output of the array strictly decreases with increased terminal voltage. Each curve has a point at which it delivers maximum power, dubbed the maximum power point (MPP). This point is the optimal operating point, since it maximizes the utilization efficiency of the solar arrays. It separates the left-hand side (LHS) of the curve from its right-hand side (RHS). On the LHS, the array resembles a current source, supplying increased power with increased voltage. On the RHS, the array resembles a voltage source, supplying decreased power with increased voltage. The terminal characteristics continuously change following variations in irradiance, temperature, and other operating conditions. The location of the MPP moves accordingly.

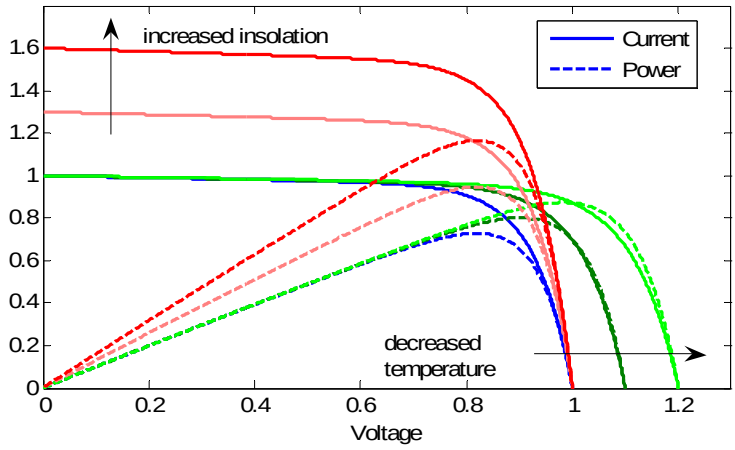


Figure 1 Typical -normalized- terminal characteristics of solar arrays

MPPT is a control scheme under which the MPP of the solar source is located in real-time. Active control—often by dc-dc converters—forces the system to operate at that point. Such

an approach significantly increases the average power yield of a given array [2] and allows the system to avoid large-signal instability conditions [7-9].

Different approaches to MPPT have been developed over the years. One class of algorithms requires prior examination of the source characteristics and uses a model of these characteristics to relate the location of the MPP to ambient condition measurements [10]. Another class, called hill-climbing algorithms, locates the MPP by relating changes in power to changes in the control variable used to control the array. This class includes the perturb and observe algorithm (PnO) [11-13], the incremental conductance algorithm (IncCond) [11-12, 14], as well as other more elaborate algorithms derived from them. This group of algorithms is particularly popular because it does not require prior study or modeling of the source characteristics and can account for characteristics drift resulting from ageing, shadowing, or other operating irregularities.

1.1.2. Batteries and Battery Management

Solar cells are limited power sources. An attempt to draw more power from a solar array than what is available results in large-signal instability and the collapse of the power system [9]. It is impractical and often impossible to size the solar source to suffice the load under all operating conditions and load levels. The utilization of a properly-sized battery bank allows the solar arrays to be sized slightly larger than the average load. During light loading, excess energy is stored in the battery bank. The load is supported by the battery bank when its demand exceeds the power available from the solar source.

High energy density, low or no maintenance, together with a long lifetime are all critical requirements for batteries used in space. One of the first space batteries was the Silver-Zinc

battery, which dominated the industry in the 1960s. This is a premium system with very high specific power and energy, but it is quite expensive due to the use of Silver. These batteries have a relatively short life cycle. Nickel-Cadmium has been the most common space battery since the 1970s. They were used in all commercial communications satellites, in most earth orbiters, and in some space probes. They are compact, can last ten to twenty years in space, and are tolerant to severe radiation environments. The Nickel-Hydrogen battery is currently the most popular space battery. It is significantly lighter than Nickel-Cadmium, but it is more difficult to package. It is the longest-lasting space battery yet built, commonly with ten to twenty-year lifetimes. The latest technology for space is the Lithium-Ion battery. High voltage Lithium-Ion cells are moving into space for short to moderate length missions. They are easy to package and very light [15].

It is very convenient to think of a battery as an ideal voltage source/sink or as a huge capacitor, and to use it accordingly. Such an approach, however, degrades battery performance, lifetime, and reliability. Most batteries require a specific charging scheme for optimized performance. A high-end battery charger is able to apply controlled charging currents, and/or controlled charging voltages. Some schemes also require pulse-charging at some stage of the charging process. Lithium-based batteries, a space industry trend, are especially sensitive to the charging method and require a three-stage charging process that includes both constant-voltage and constant-current stages. In order to allow the application of customized charging schemes to a particular battery, the power system is required to provide a control degree of freedom to be used for charge regulation. This is often the duty-cycle of some converter stage interfaced to that battery bank.

1.1.3. Power Management and Distribution

The design of a spacecraft PMAD system is heavily dominated by the compromise between system architectures. A limited number of conversion stages yields a simple non-flexible system, often with over-sized sources and storage components. Adding more conversion stages allows enhanced power management with tighter bus regulation at the cost of increased conversion loss and control complexity.

Batteries are conventionally interfaced to a solar power system in several fashions as discussed next:

1. Unregulated bus topology: connecting the solar array directly to the battery, as shown in Figure 2, offers a very simple, reliable, and cost-saving solution. A shunt regulator is connected for battery protection from over-charge. Unfortunately, this topology does not allow control over the solar array voltage, nor bus voltage regulation.

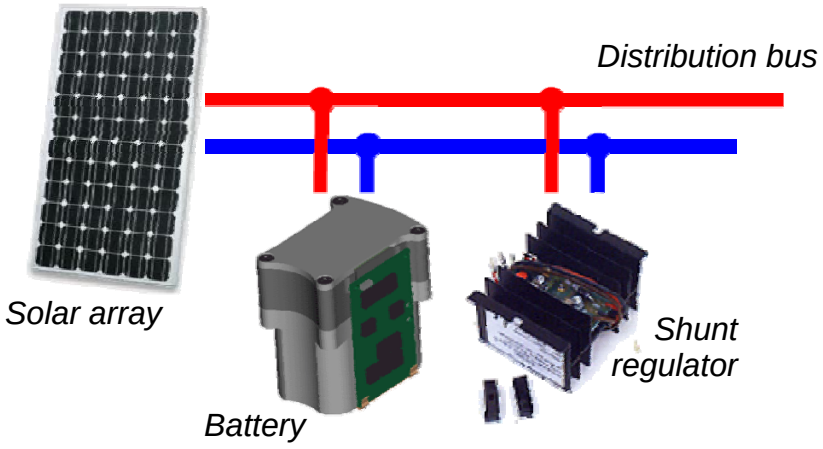


Figure 2 Unregulated bus topology

2. Regulated bus topology: interfacing the battery to the system through a charge/discharge regulator, as shown in Figure 3, allows voltage regulation of the system bus. The solar array voltage is clamped to that bus voltage and cannot be independently controlled.

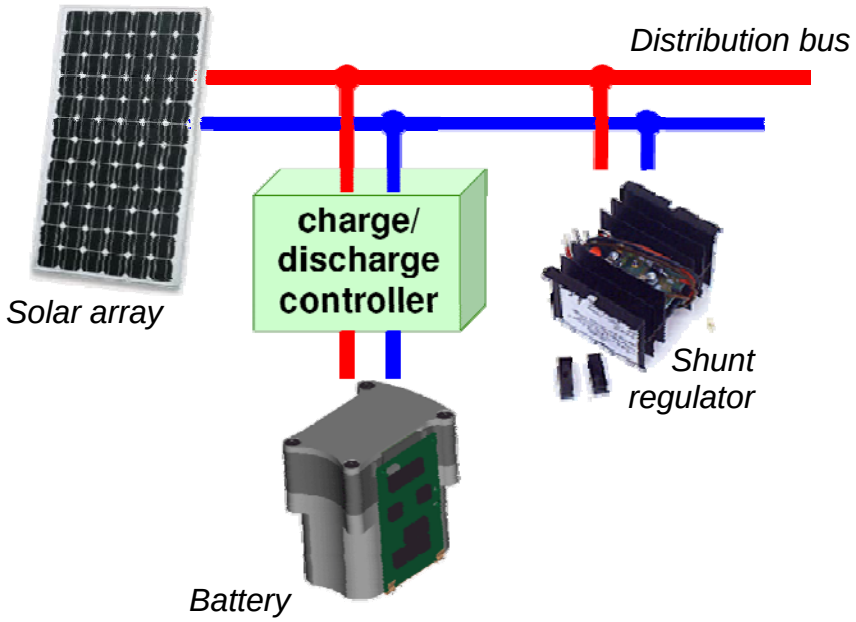


Figure 3 Regulated bus topology

3. MPPT battery bus topology: a dc-dc converter interfacing the array to the battery, as shown in Figure 4, allows control over the operating voltage of the array, and opens the door for the advantageous MPPT operation. The bus voltage, however, is not regulated and is a function of the battery state of charge.

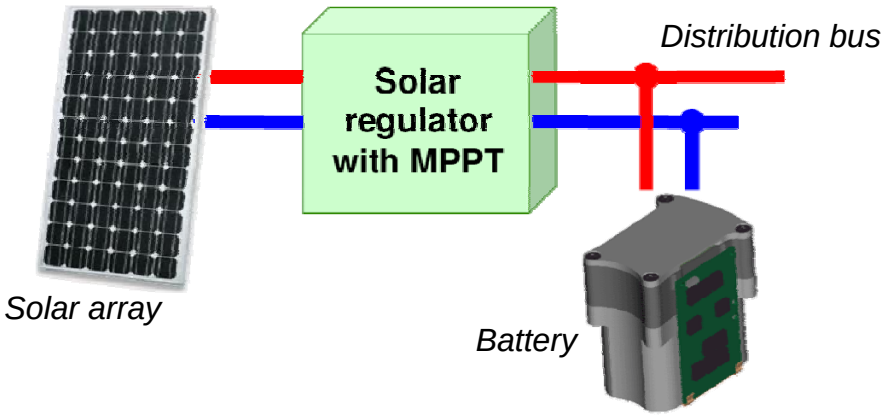


Figure 4 Battery-dominated MPPT bus topology

Many missions require voltage regulation of the distribution bus. It is desirable to achieve this while maintaining either MPPT or battery charge regulation. The risk of large signal instability due to source-load mismatch is eliminated by charging the battery during periods of high insolation, and covering the load power deficit from the battery during periods of low insolation. The solar arrays can then be sized to suffice the average load, allowing significant reduction of their size. These goals require the addition of one more power control variable, or power conversion path.

The interfaced system components are a power source, a power sink, and a bidirectional power storage device: the array, the distribution bus, and battery respectively. The power path configurations that can achieve this are:

1. Two stage interface: the solar array is interfaced through an MPPT converter to an intermediate battery-dominated dc-link. Another converter stage then interfaces that link to the distribution bus, as shown in Figure 5. The main disadvantage of this scheme is that solar power goes through two lossy conversion stages before reaching the output.

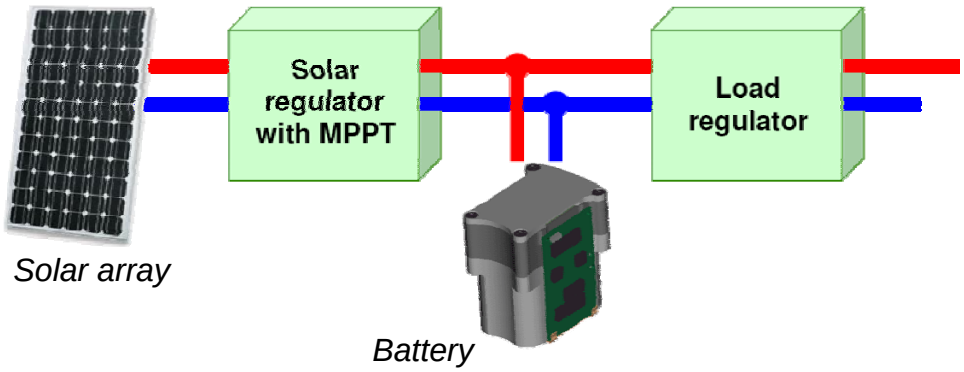


Figure 5 Two-stage fully-regulated PMAD topology

2. Bidirectional chargers: the solar array is interfaced to the distribution bus through a single-stage converter, thus allowing higher input to output efficiency. A bidirectional converter interfaces the battery either to the input or to the output, as shown in Figure 6. If interfaced to the input, the battery charge needs to go through two conversion stages to reach the bus. If interfaced directly to the bus, the battery is charged from the solar array through two conversion stages. This scheme is efficient if the loading pattern closely matches the source, and very low energy is stored and later drawn from the battery.

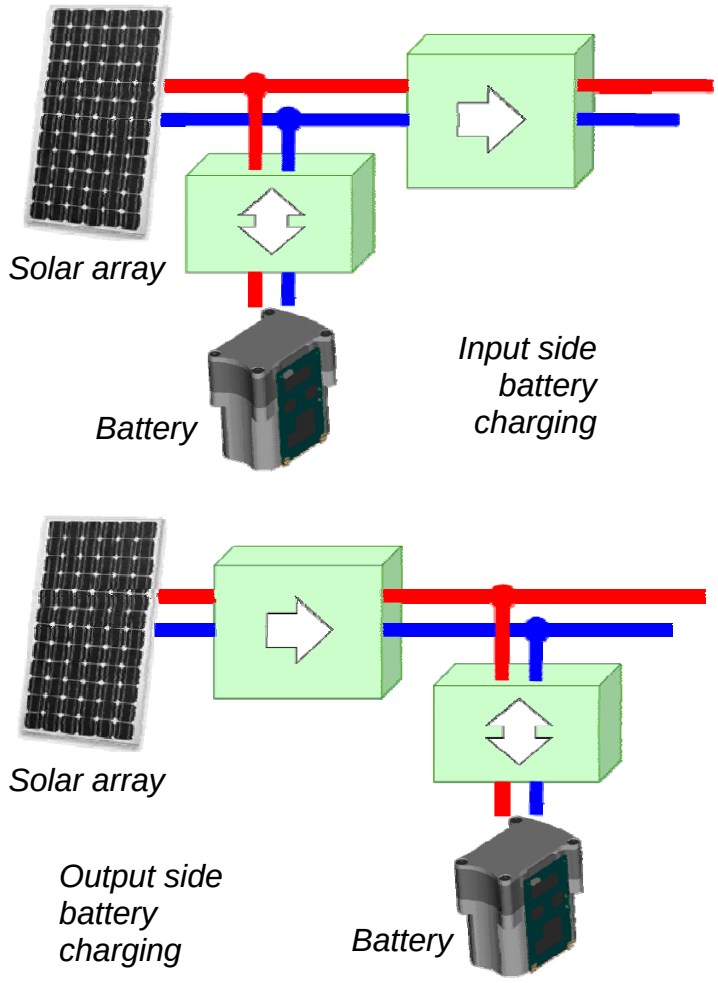


Figure 6 Fully-regulated PMAD topologies with bidirectional battery chargers

3. Independent charge and discharge: the bidirectional battery converter can be split into two unidirectional converters: a charger interfaced to the input, and a discharge converter interfaced to the distribution bus. This configuration, shown in Figure 7, assures that power goes through one conversion stage when traveling between any two ports, allowing for higher efficiency. The price paid is an additional converter, increased size, weight, cost, and increased component count of the system.

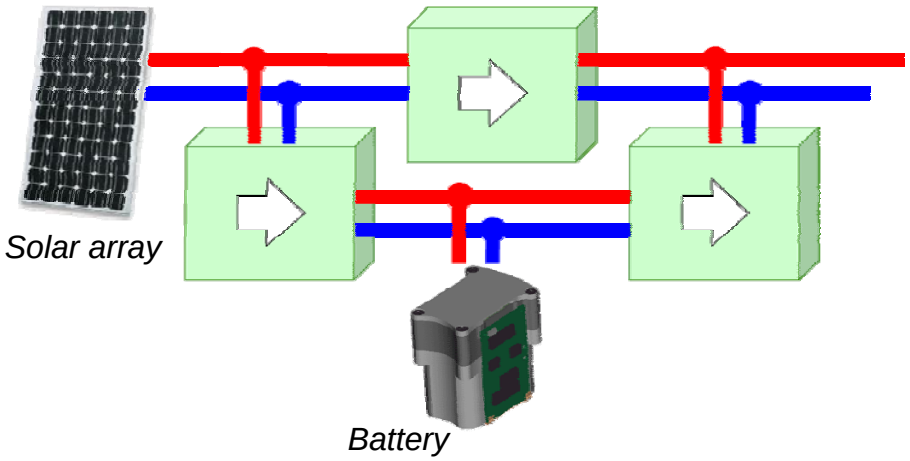


Figure 7 Fully-regulated PMAD with independent battery charging/discharging

The added complexity, together with increased losses, size, weight, and cost, as well as decreased reliability, has impeded wide-spread adoption of such architectures for space. The potentially profitable MPPT technology has often been difficult to justify given the cost and control complexity overhead.

Proposed here is the use of a single converter stage to efficiently achieve the functionality of the three-converter configuration. This greatly simplifies the power architecture and control schemes needed for realizing MPPT and battery charge control. The multi-function utilization of power processing components and integration of control tasks reduces the size, cost, and complexity, making these control objectives more relevant and the design alternatives more feasible.

CHAPTER 2: REVIEW OF MULTI-PORT CONVERTERS AND DIGITAL CONTROL TECHNIQUES

An increased demand for versatile energy harvesting and management systems has been witnessed in recent years. Systems capable of collecting energy from solar cells, fuel cells, regenerative braking, and mechanical oscillations are particularly useful for powering remote communication repeaters, traffic lights, sensor networks, small satellites, hybrid electric vehicles (HEVs), laptops, and other electronic products. This chapter reviews the existing and emerging technologies for multi-port systems. It also reviews the recent trends for digital control of power electronics—an enabler technology for effective multi-variable multi-objective control of complex systems.

2.1. Multi-Port Converter Technologies

The simplest approach to building multi-port converters is the interface of several converter stages to a common dc bus with centralized control. A multi-input bidirectional converter system, shown in Figure 8, was designed for use in HEVs and interfaces a fuel cell, a battery, and a super-capacitor bank [16].

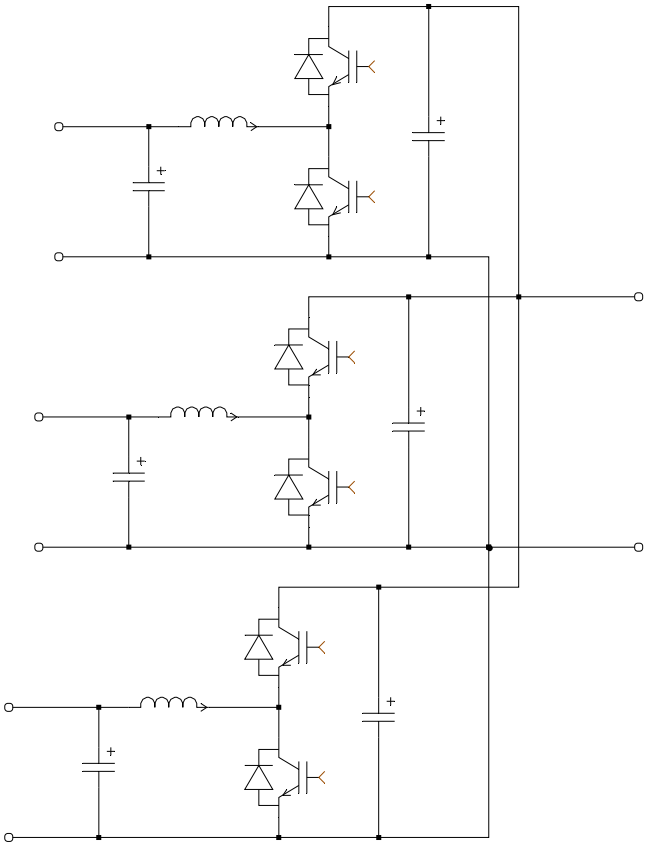


Figure 8 Bidirectional multi-input converter system for HEVs [16]

The investigation of new converter topologies designed to handle multiple power ports has recently become a recurring theme. Many believe that topologies specifically tailored for multi-port applications can reduce cost and losses while retaining the functionality of more traditional multi-converter designs.

2.1.1. Integrated Multi-Input Converters

A two-input tri-state dc-dc converter, shown in Figure 9, based on the buck topology was an early attempt to integrate spacecraft front-end PMAD systems [17]. Dynamic modeling and control of this converter were further discussed in [18]. This converter provides two degrees of

freedom, and thus can be used to achieve two control objectives. When sourced by a solar array and the system battery, it is possible to simultaneously perform MPPT and output voltage regulation. Unfortunately, the input ports are unidirectional and the converter cannot be used to charge the battery from the solar array. This converter also requires bidirectional-blocking devices to properly operate, uncommon in the industry for the voltage and power levels intended.

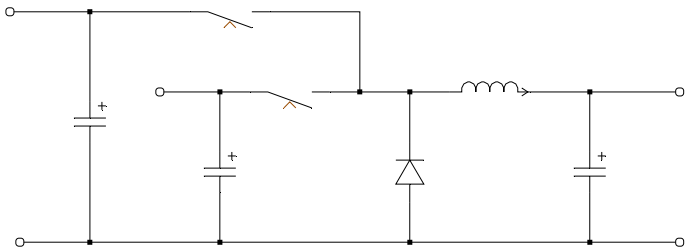


Figure 9 Topology of the two-input tri-state dc-dc converter [18]

Another multi-input converter was proposed in [19] based on the flyback topology. This converter, shown in Figure 10, can achieve galvanic isolation between all ports by coupling them to a common flyback transformer.

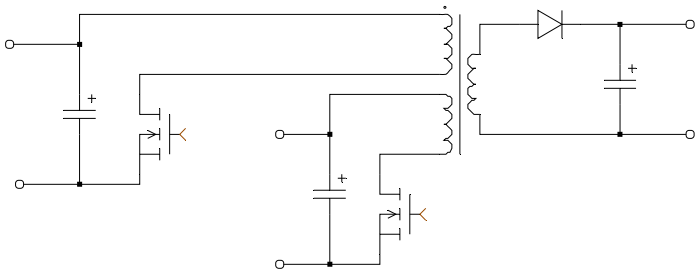


Figure 10 A multi-input flyback converter [19]

A simplified version of this circuit was later proposed as shown in Figure 11 [20]. This multi-input circuit, based on the buck-boost (non-isolated flyback) topology, was later modified

to isolate the loading port only and generalized to supply multiple loads as shown in Figure 12 [21]. The power budgeting capabilities of these configurations were also discussed in [21]. Each of these topologies possesses a number of control variables equal to the number of sources. They can perform independent regulation over a maximum of one output given that regulation over one of the inputs is dropped. It was again shown that a two-input converter can regulate its load voltage while governing the operating point of a solar array connected as one of its inputs.

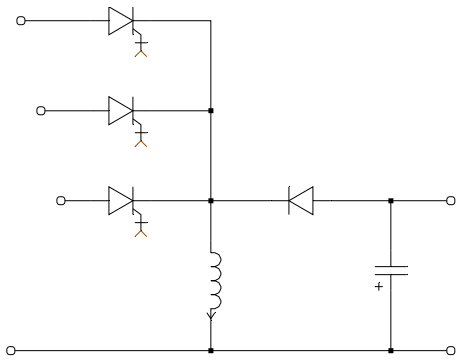


Figure 11 A multi-input buck-boost converter [20].

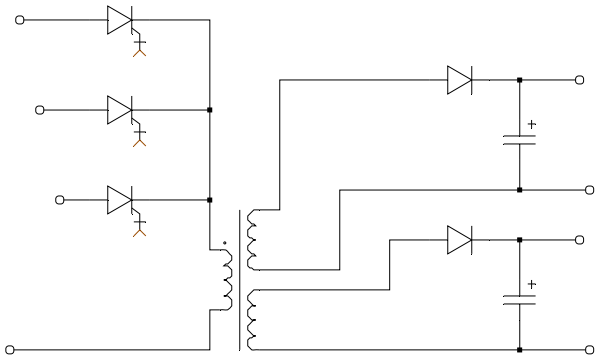


Figure 12 A multi-input multi-output flyback converter [21]

The main limitations of these configurations are the lack of a bidirectional port for energy storage, the utilization of bidirectional-blocking switches, the limitation of individual duty-cycles

when a large number of sources is used, and/or operation based on the flyback principle with magnified inductor currents.

Figure 13 shows a two-input boost-derived isolated converter proposed in [22]. This converter is able to simultaneously achieve MPPT of a solar input, power factor correction (PFC) of a sinusoidal source, and load regulation. This converter, being boost-derived, draws low ripple input currents from its sources. Due to instantaneous energy balance constraints, the speed by which the load is regulated is limited. The main disadvantage, however, is its requirement of a large number of bidirectional-blocking switches, and the absence of a bidirectional port.

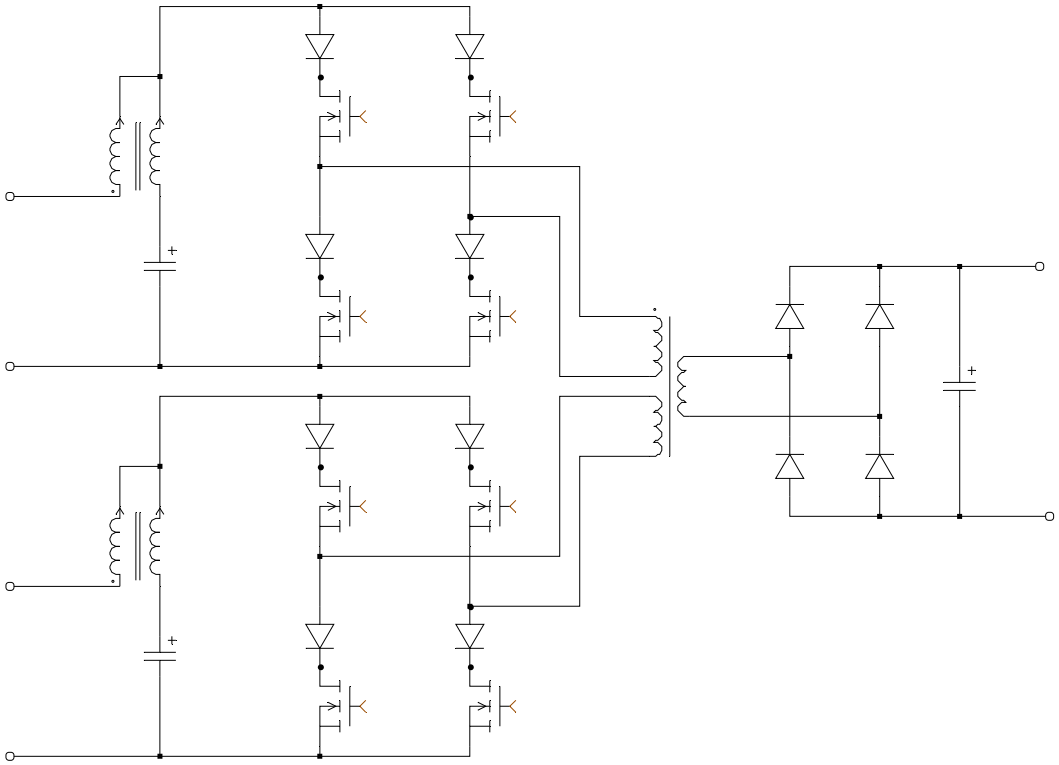


Figure 13 A two-input isolated boost converter [22]

2.1.2. Isolated Bidirectional Multi-Port Converters

Recent publications focused on load-side control through the utilization of a half-bridge structure magnetically coupled to the source chopper [23, 24]. The converter shown in Figure 14 is suitable for HEVs or fuel cell powered electric vehicles [23]. Energy exchange between the 14V and 42V busses is governed by the duty-cycle of the primary-side phase-leg, while energy exchange with the high voltage bus on the secondary side is governed by the relative phase-shift between the switching waveforms on either side of the transformer.

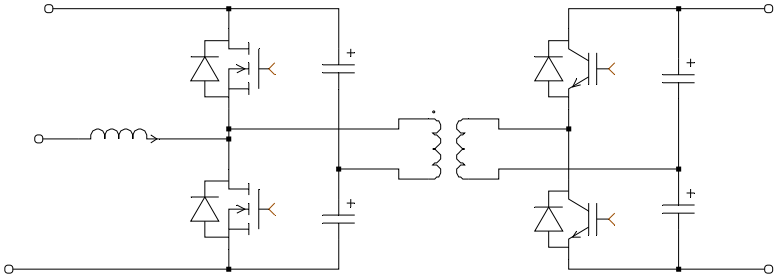


Figure 14 Triple-voltage bus dc-dc converter [23]

This concept can be further extended to a larger number of isolated and non-isolated ports [24]. A number of half-bridge circuits can be coupled as shown in Figure 15. These are essentially independent converters that share a common ac distribution transformer. Control over the power flow can be achieved by changing the relative phase-shift between the switching sequences of those bridges. It is also possible to interface additional non-isolated ports to the system by adding buck/boost stages.

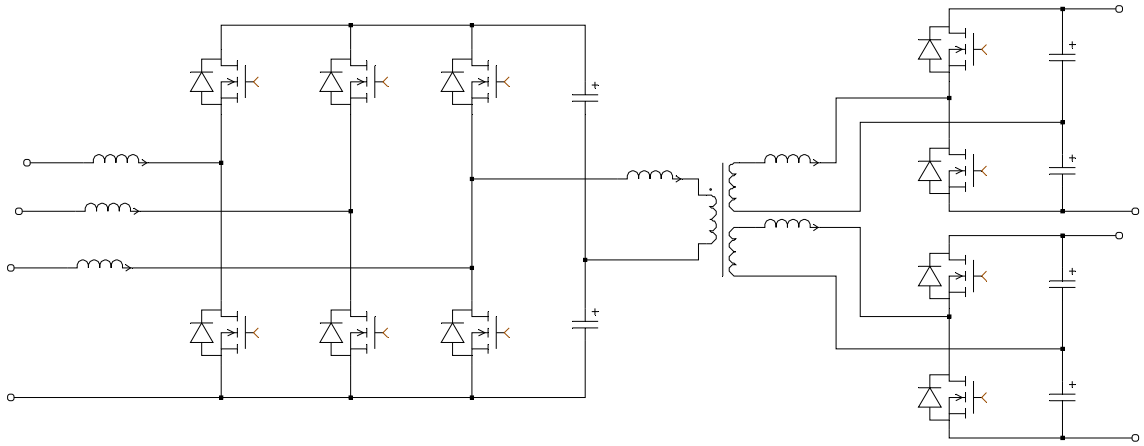


Figure 15 Bidirectional magnetically coupled multi-port converter [24]

Following the same principle, isolated bidirectional multi-port converters can be constructed out of full-bridge structures as shown in Figure 16 [25]. Full-bridge structures are more popular for lower voltage higher current applications since they apply the full bias voltage to the transformer and thus circulate lower currents.

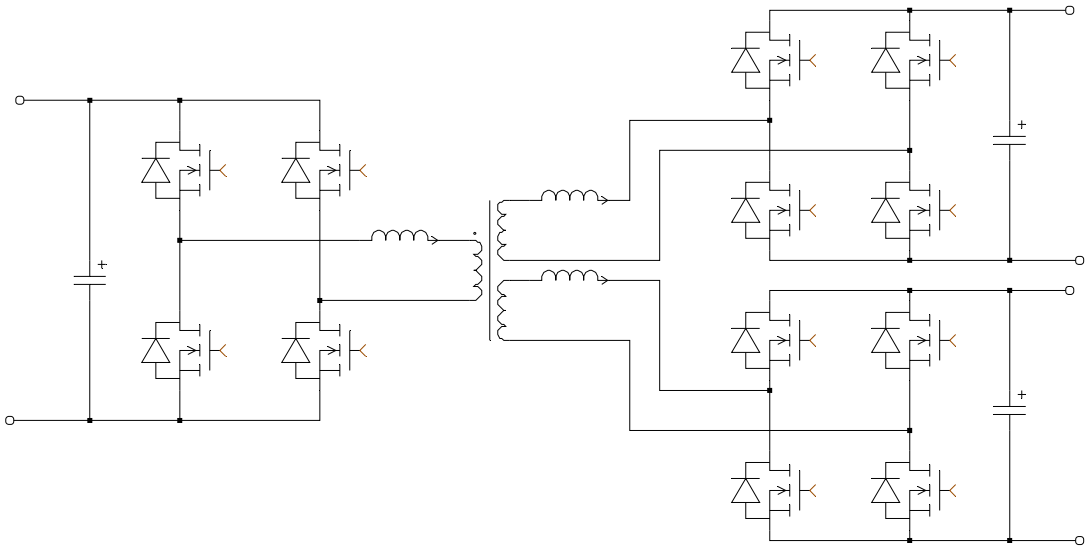


Figure 16 The construction of isolated bidirectional multi-port converters using full-bridge structures [25]

The main advantage of these systems is that all ports are bidirectional and can be chosen to be isolated. They utilize the very popular phase-leg structure with popular unidirectional-blocking switches that make them especially attractive and expandable. They utilize, however, a large number of active switches, and require fairly complex modulators and controllers.

2.1.3. Integrated Power Factor Correction Converters

Power factor correction (PFC) converters are two-port converters. They, however, require the storage of energy in an intermediate capacitor that would absorb the instantaneous difference between the pulsating power from the source and the power delivered to the load. This bulk capacitor represents a long-term energy storage element, and its capacity can be better utilized if it is not directly interfaced to the source or the load. In this case, a PFC converter essentially becomes a three-port converter with a bidirectional port interfacing that bulk capacitor. Several publications have proposed the integration of a bi-phase boost into a phase-shift full-bridge (PS-FB) converter in order to achieve single-stage PFC, see Figure 17 [26-29].

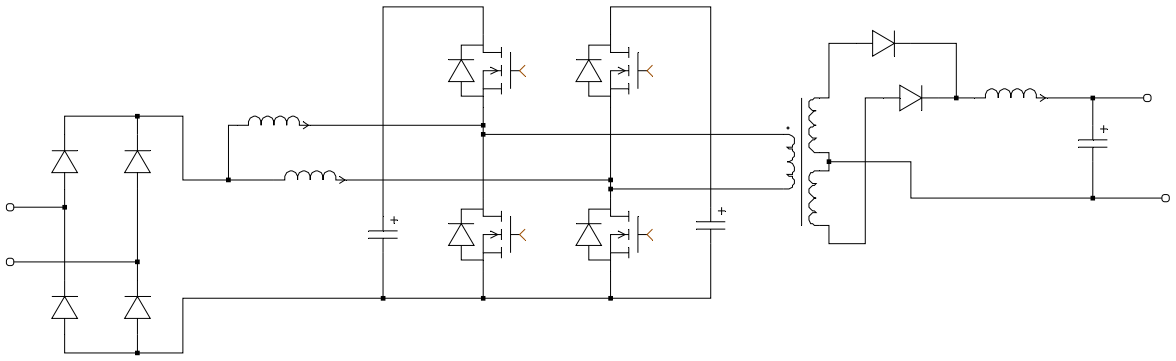


Figure 17 PFC converters integrating a boost and a PS-FB stage [26-29]

Interestingly, simultaneous variation of duty-cycle and phase-shift was proposed in [29] to allow output voltage regulation, while constraining the amount of energy storage in the bulk capacitor. In this converter, shown in Figure 18, the boost inductors are designed to operate in discontinuous conduction mode (DCM) in order to enhance the power factor. The phase-shift between the switching of the two legs is used to control power flow to the load. The duty-cycle of each leg is used to achieve some control over the voltage of the bulk capacitor, reducing the voltage stress over the switching bridge and rectifier diodes. The application of this scheme to PFC introduced a number of challenges that overshadowed a lot of it merits.

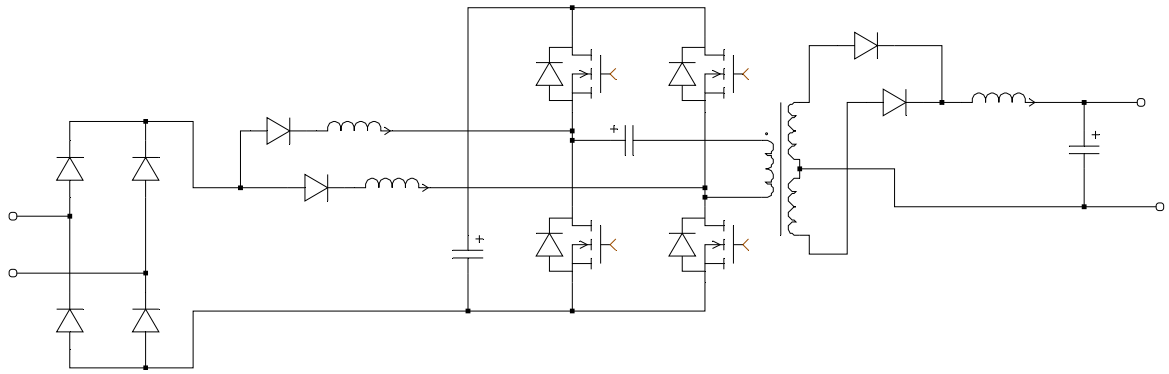


Figure 18 Constraining the voltage of the bulk capacitor using combined duty-cycle and phase-shift control

2.2. Digital Control of Switching Power Converters

A strong trend toward digital control of power converters, or "digital power," has recently surfaced. Digital power is gaining momentum due to: the need for supervisory digital controllers in many systems, rapid increase in digital integrated circuit (IC) resources paralleled by a rapid decrease in their cost, reduced board space and system cost due to integration of

multiple control functions into a single digital chip, increased flexibility with feed-forward and non-linear control techniques, and improved protection and health monitoring [30-36]. Still missing, however, is a simple step-by-step design method approachable by a practicing engineer. Bridging the gap between digital control and practicing engineers requires improvements in two key challenging areas: compensator design, and controller mapping into software code.

In recent years, digital controller design for power converters has been an active area of research. Two main approaches were proposed: analog redesign, and direct-digital design. Analog redesign proceeds by using a chosen transformation to approximate the continuous-time s-domain controller transfer function by one in the discrete-time z-domain [32-35]. This approach is popular because it relies on traditional design techniques in the analog frequency domain. However, it suffers an inherent behavioral mismatch between the original analog, and the resultant digital designs. Figure 19 shows several digital approximations of an analog zero, while Figure 20 shows the response of the resultant digital closed loops compared to an analog-controlled original. The trapezoidal rule has the closest correspondence to the original analog function, but yields the most complicated expression in the z-domain. Moreover, the analog redesign method fails to account for a zero-order holds (ZOH) and computational time delays inherent in a digitally closed loop.

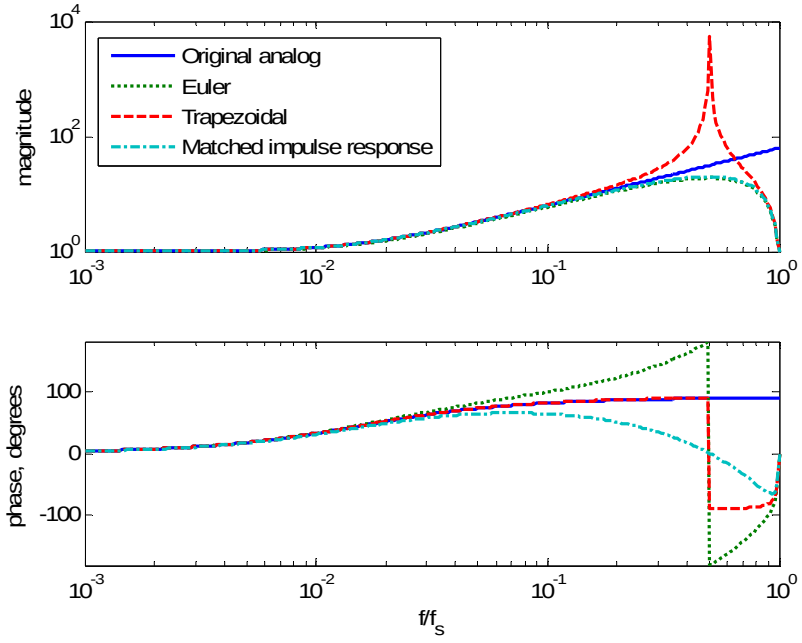


Figure 19 The frequency response of an analog zero and several digital approximations

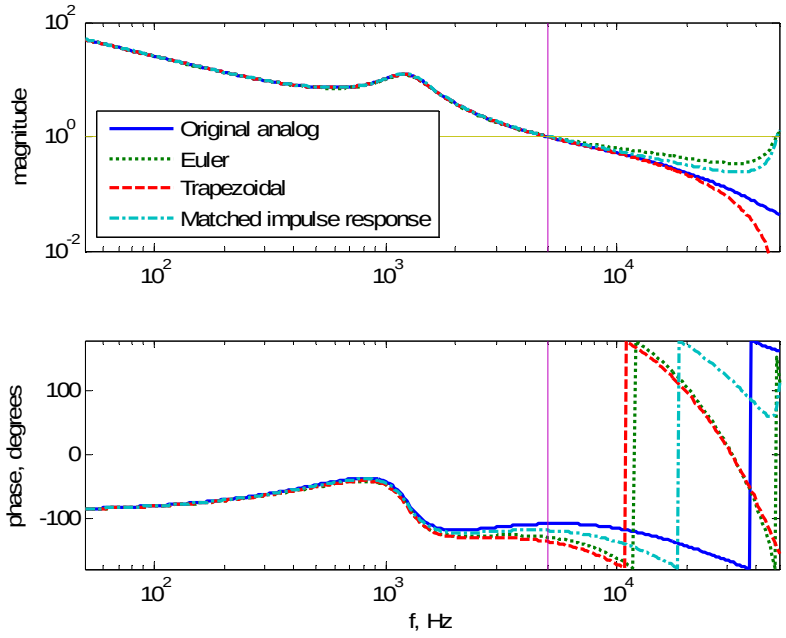


Figure 20 Typical loop frequency response with an analog controller and its digital redesigns

A number of powerful direct-digital controller design techniques have been introduced and demonstrated in literature [36-40]. Controller design is performed in the z-domain using an approximated discrete-time model of the controlled plant. Nonetheless, these were not widely used by practicing engineers because they are mathematically involved and lack a strong link to traditional analog controller design methods.

Mapping the digital controller function into software code requires full understanding and accurate modeling of the components of the digital controller. Several publications presented good models of the analog-to-digital converter (ADC) and pulse-width modulator (PWM) modules, and discussed their quantization effects [30, 40]. Quantization effects within the internal registers of a fixed-point controller IC—dominating the digital power market—have not been fully addressed. A simple system for efficient number storage and manipulation is still needed.

CHAPTER 3: THREE-PORT CONVERTER SYSTEM INTEGRATION

This chapter explores the basic principles of converter integration into multi-port systems.

3.1. Integration Objectives

The main objective of converter integration is the construction of flexible, efficient, reliable, and light-weight PMAD systems. These objectives translate to a more specific set governing the power converters, their controllers, and the general architecture.

3.1.1. Objectives for the Power Stage

This work targets the integration of the power train into a single converter stage that interfaces three power ports: an input, an output, and a bidirectional port. This promises reduced losses thus allowing enhanced utilization of available power, reduced thermal stress, and enhanced power density.

Galvanic isolation of the output port through a transformer is required. This ensures:

1. Design flexibility for choosing the output voltage level: high bus voltages reduce distribution losses in large systems, while lower voltages simplify the design of point-of-load (POL) converters.
2. Ability to achieve high voltage step-up/down ratios.

3. Fault isolation and enhanced operator safety.
4. Flexible series/parallel converter connection in modular designs, and compatibility with NASA's Series Connected Boost Regulator (SCBR) concept, shown in Figure 21 [41].

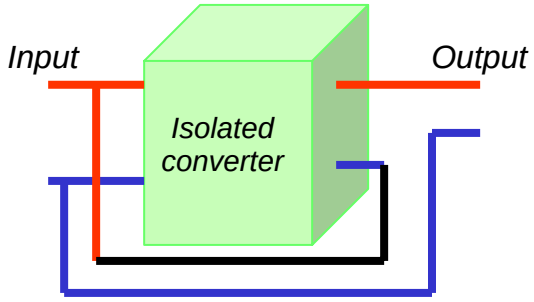


Figure 21 NASA's SCBR configuration [41]

It is preferable to base integrated converter topologies on popular existing two-port converters. Engineering concepts and experiences available with practicing engineers can then be used to optimize the new topologies in a fashion similar to their mother topologies. This includes component selection and magnetic design procedures, as well as achieving soft-switching for increased efficiency at higher switching frequencies.

3.1.2. Control Objectives

Following energy conservation principle, a maximum of two ports can be independently controlled in a three-port power converter. The third port operating point is governed by the need for it to accept or supply the power balance and compensate for conversion power losses.

Control decisions and transients on one power port in a multi-port system are expected to affect the remainder. Controller coordination and feed-forward architectures can simplify controller design and enhance performance.

An integrated controller performing simultaneous control over two power ports is targeted in this work. The goal controller also should be able to switch between different control objectives in real time. Choices in a battery-backed solar power system are: MPPT, battery charge control, and bus voltage regulation.

3.1.3. Modularity Objectives

The utilization of PEBBs is becoming increasingly popular in space PMAD systems [42]. The standardization of power modules allows repetitive utilization of optimized designs, thus reducing the design time and cost, and simplifying testing and qualification cycles. Paralleled converter structures provide hot-swap capabilities and enhanced fault-tolerance, thus improving system reliability and availability.

The standardized converters must be able to be independently sourced or parallel connected at their input, as well as at their storage ports. With electrically isolated output ports, these can be the building blocks for a wide choice of voltage and current ratings at the bus. Converter outputs can be connected in series or parallel, as shown in Figure 22, independent from the input connection topology. Techniques for uniform voltage, current, and power stress distribution must be implemented.

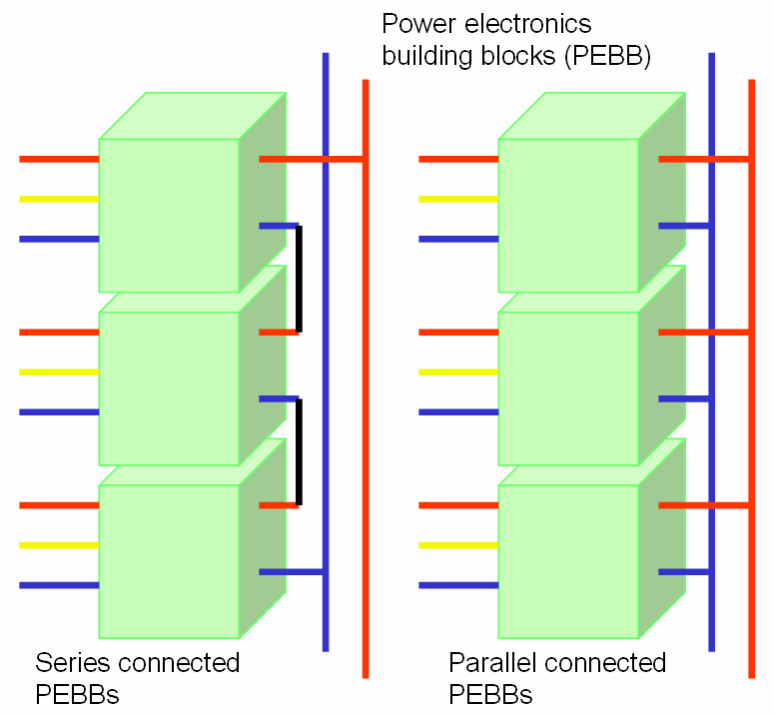


Figure 22 PEBB approach applied to three-port converters

3.2. Topology Integration Approach

The fundamental scientific concepts upon which this work is based are described in this section. This is followed by a description of some members of a novel topological family.

3.2.1. Unity of Power Topologies

The operation of a large majority of power electronic circuits relies on different variations of one basic structure. This structure, often dubbed a phase-leg, consists of two series connected switching devices biased by a dc voltage bus, as shown in Figure 23. The switching action causes the middle point (phase-node) to be connected alternatively to either rail of the biasing dc voltage. This is then utilized in one of two ways:

1. As an ideally lossless “time-division voltage divider”: a power filter is used to smooth the voltage at the phase-leg into a controlled voltage value. In this case, one of the switches can be replaced by a diode to create the basic topologies: buck, boost, and buck-boost. It is, however, common practice to keep it an active switch, allowing the topology to achieve bidirectional power flow, as well as decreased conduction losses in low voltage applications.
2. As a driver for a high-frequency transformer: the ac component of the phase-leg voltage waveform is applied to the primary winding of a transformer. A rectifier circuit, together with a filter, is used to reconstruct a dc voltage level at the secondary. This is the operating principle of the half-bridge, forward/active-clamp forward, and the full-bridge topologies.

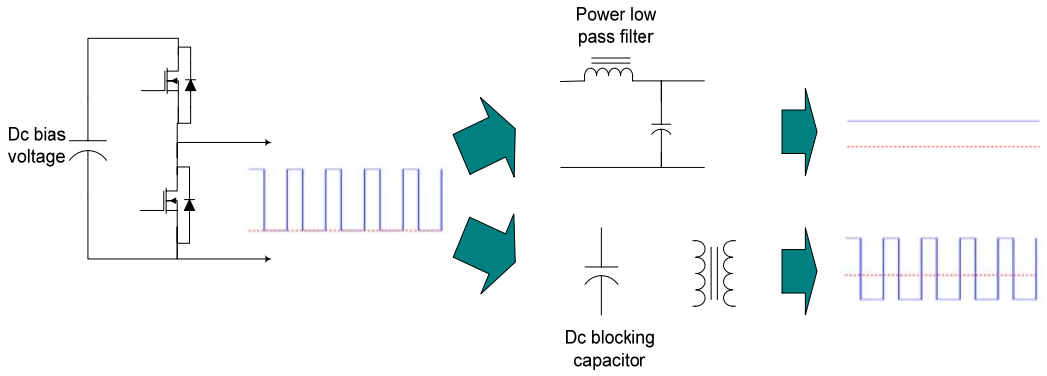


Figure 23 Typical functions of a phase-leg

There is a striking similarity between the half-bridge converter and the active-clamp forward converter. The half-bridge circuit places the source at the dc bias voltage of the phase-leg, while a dc voltage is accumulated on a filter capacitor that removes the dc component from the transformer voltage waveforms. The active-clamp forward circuit connects the source in

place of this dc-blocking capacitor, and results in creating a higher dc-bias voltage across the phase-leg. With both sources connected, the relationship between the dc-bias and the dc-blocking voltages are governed by the characteristics of the "parasitic" synchronous buck converter interfacing them.

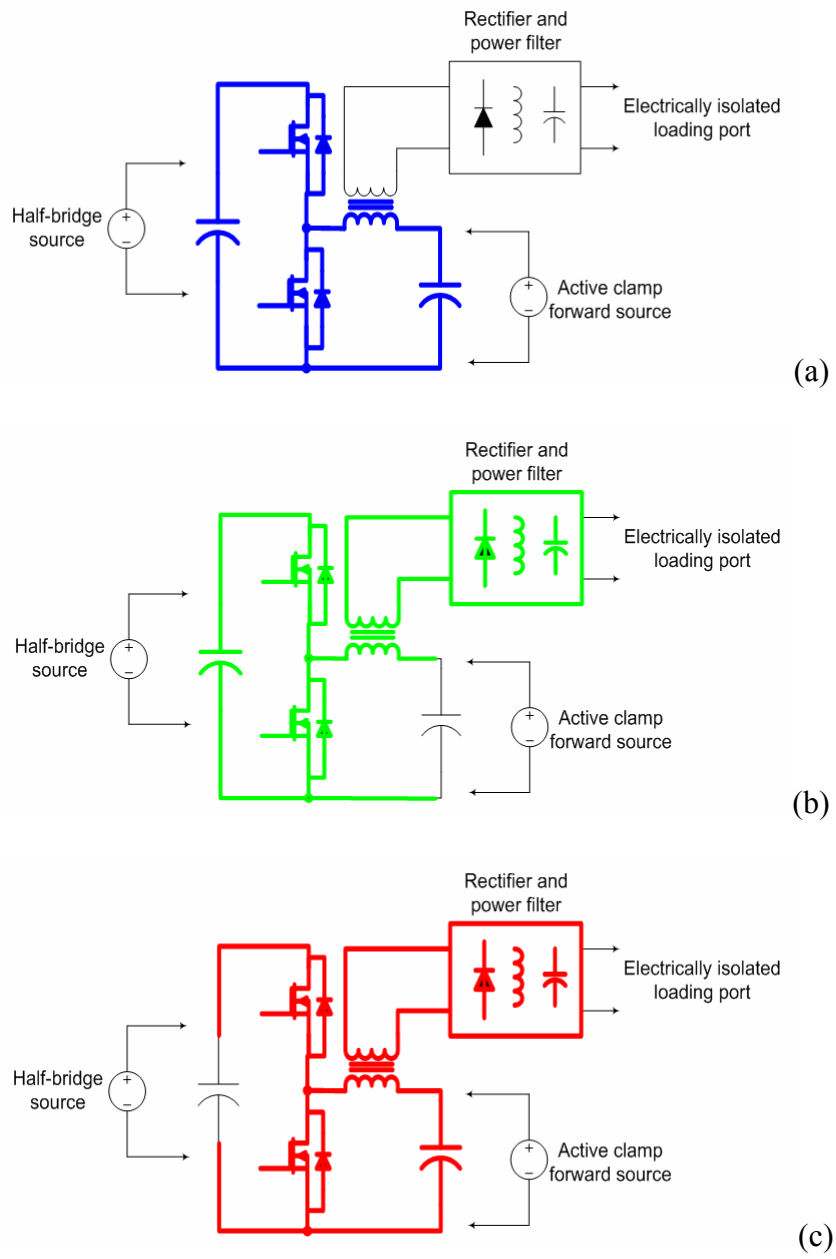


Figure 24 Unity of (a) buck, (b) active clamp forward, and (c) half-bridge converter topologies

The dual utilization of a phase-leg as a time-division voltage divider and a transformer driver is a powerful tool for three-port interface. The ac and dc components of the phase node waveform can be independently controlled to realize tight regulation of two power ports.

3.2.2. Savings Potential

This integration concept has great potential to deliver savings in both conduction and switching losses—see Figure 25. In a non-isolated topology, the phase-leg would drive low-ripple dc current. Using two FETs with equal on-state resistance, the conduction loss incurred by these FETs can be estimated as:

$$P_{loss}^{cond} = r_{ds}^{on} \cdot \overline{i_{dc}^{\,2}} = r_{ds}^{on} \cdot I_{dc}^{\,2} \tag{3.1}$$

where r_{ds}^{on} is the on-state resistance of the FETs used, and I_{dc} is the value of dc current driven by that phase-leg.

When driving ac current through the transformer of an isolated topology, the conduction loss would be estimated as:

$$P_{loss}^{cond} = r_{ds}^{on} \cdot \overline{i_{ac}^{\,2}} = r_{ds}^{on} \cdot I_{ac}^{\,2} \tag{3.2}$$

When the same phase-leg is used to drive both currents, conduction loss is estimated as:

$$P_{loss}^{cond} = r_{ds}^{on} \cdot \overline{\left(i_{dc} + i_{ac}\right)^2} = r_{ds}^{on} \cdot \left(I_{dc}^{\,2} + I_{ac}^{\,2}\right) \tag{3.3}$$

where I_{ac} is the rms value of ac current driven by that phase-leg.

Note that the result is simply the sum of the individual loss to be incurred by the dc and ac components separately. This means, ideally, that a single phase-leg can be used to do the job of two without increasing the conduction power loss. The designer can also choose to invest the same silicon area—perhaps by paralleling the devices of the two phase-legs. In such a case, the

on-resistance would significantly drop, allowing the integrated structure to incur lower conduction loss using the same investment in silicon.

The integrated structure is also capable of reducing FET turn-on losses through zero-voltage switching (ZVS). When a phase-leg drives a dc current in a non-isolated topology, ZVS is naturally achieved for one FET only while the other remains hard-switched. The upper FET is hard-switched in a buck converter, while a boost converter hard-switches its lower FET. In many isolated topologies, the transformer current direction is suitable to force ZVS turn-on of all primary FETs. An integrated topology is likely to have a wide range of operating conditions where all FETs are switched with ZVS. In other words, the ac current of the isolated section aids in avoiding the hard-switched transition of the non-isolated section.

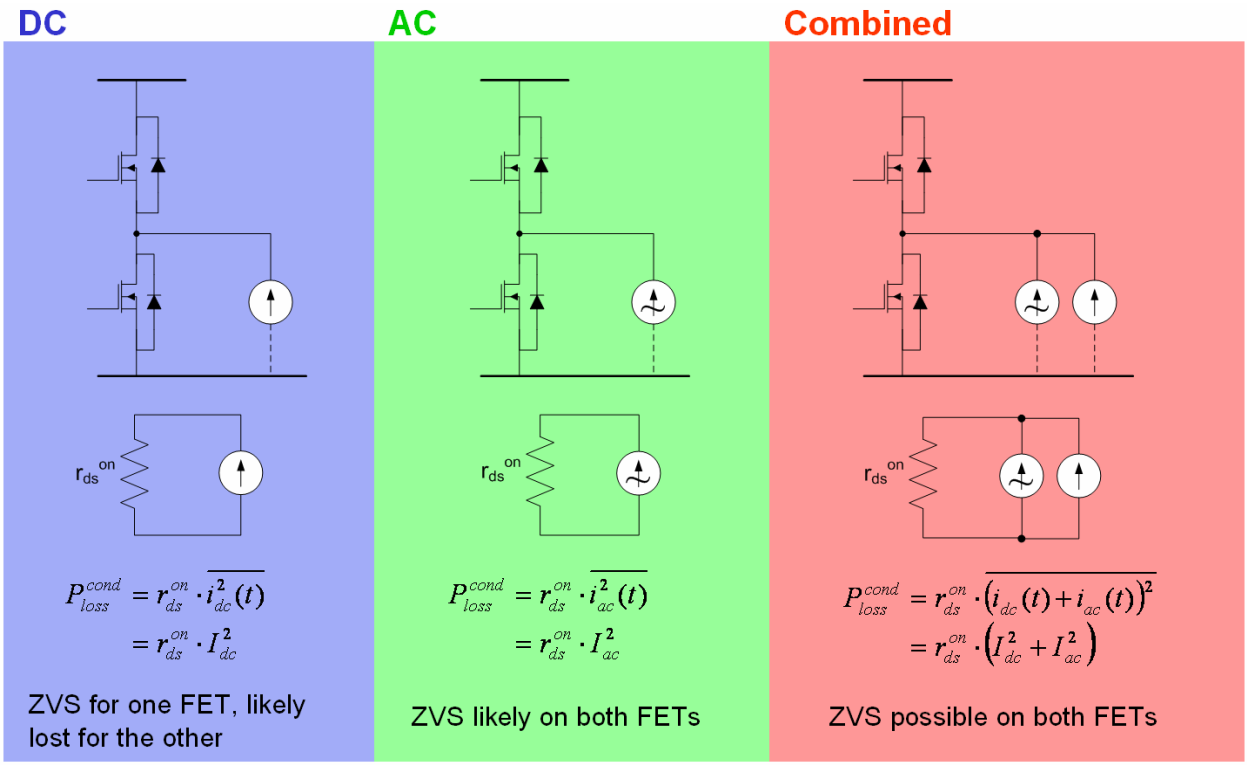


Figure 25 Savings potential of the proposed topology integration approach

3.2.3. Attractive Conventional Topologies

A number of popular conventional isolated topologies exist that can be modified to interface three ports. Rather than searching for completely new configurations, this evolutionary approach recaptures the technical merits of popular existing two-port topologies. It allows circuit designers to use their design experience and knowledge base to better optimize the new topologies.

3.2.3.1 The Duty-Cycle Shifted Half-Bridge Converter

The half-bridge topology uses a single phase-leg to create the driving waveforms for the transformer. A dc-blocking capacitor is used to remove the dc component from the driving waveforms. This is particularly attractive because of its reduced switch count and simplified control.

Symmetric control of the half bridge circuit balances voltage stresses across the circuit components and achieves regulation of the load. Unfortunately, this driving scheme does not allow ZVS of the switches, creating voltage stress and electromagnetic interference (EMI) problems in the converter. Asymmetric control of this topology has been introduced as a technique for achieving ZVS operation, but at the expense of unbalanced stresses across converter components [43].

The Florida Power Electronics Center has introduced the concept of the duty-cycle shifted half-bridge (DCS-HB) converter [44]. This converter, shown in Figure 26, is able to achieve ZVS on one of the switches while retaining the symmetry of component stresses. Moreover, the addition of an auxiliary switch path allows soft-switching on all switches of the

circuit. This lowers component stresses and switching losses, and solves EMI problems in the circuit. This approach has thus been adopted in commercial production.

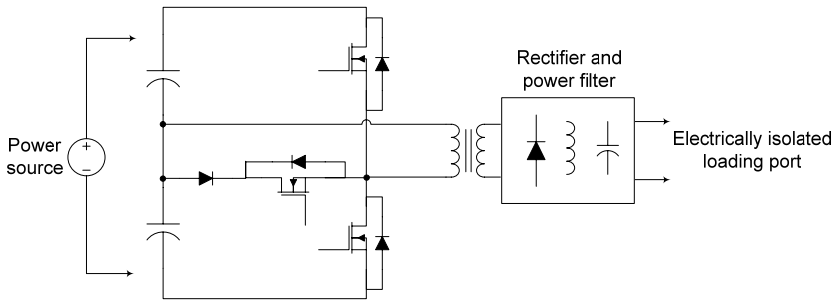


Figure 26 Soft-switched DCS-HB converter with auxiliary branch

3.2.3.2 The Phase-Shift Full-Bridge Converter

Full-bridge isolated converters, as that shown in Figure 27, utilize two phase-legs to drive the transformer. The increased switch count is justified by the configuration ability to instantaneously apply the full input voltage to the transformer winding. ZVS for all four switches can be achieved by driving the topology in a phase-shift controlled manner. This has made this topology specifically popular at moderate-to-high power conversion applications.

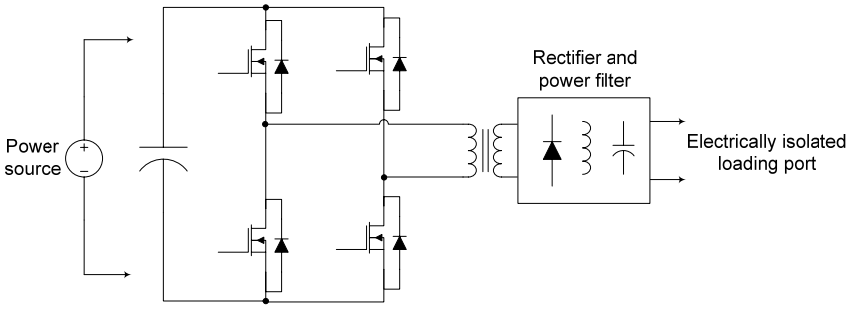


Figure 27 The PS-FB converter

The development of different three-port converter topologies based on such practical optimized conventional techniques provides feasible alternatives for a wide variety of applications at different power levels.

3.3. Three-Port Topology Options

Introduced here are some possible members of the novel three-port family that were based upon the topologies described above.

3.3.1. The Tri-Modal Half-Bridge Converter

The DCS-HB with the auxiliary switch branch is topologically suitable for use as a three-port converter, as shown in Figure 28. A bidirectional port is readily available at the lower dc-blocking capacitor on the primary side. This capacitor voltage is conventionally set to half of the input voltage by equating the duty-cycles of the two phase-leg switches. Dynamic control of this duty-cycle ratio allows independent control of this bidirectional port. The resultant converter has three modes of operation within a constant-frequency switching cycle, and was thus dubbed the tri-modal half-bridge (TM-HB) [45, 46].

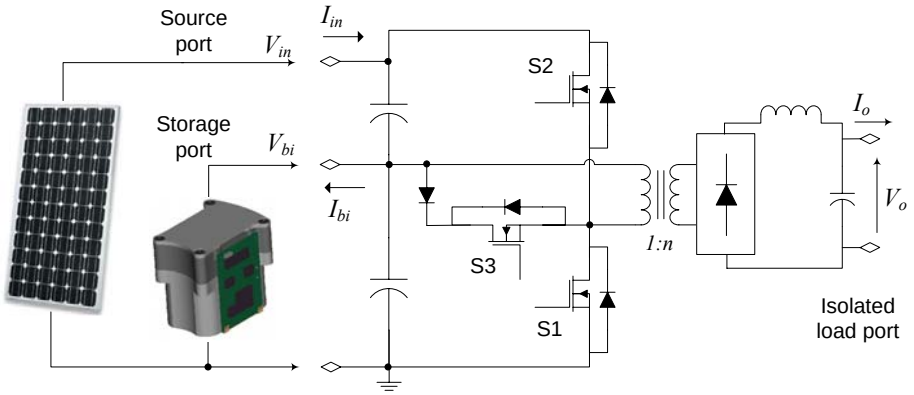


Figure 28 The TM-HB converter

3.3.2. Boost-Integrated Phase-Shift Full-Bridge Converters

Phase-Shift Full-Bridge (PS-FB) converters are more suitable for higher power applications, [47], typically above 1kW. Applying the same concept of dual use of the phase-legs, two three-port topologies can be derived from the full-bridge circuit. The asymmetric boost-integrated phase-shift full-bridge (A-BI-PS-FB) converter results from adding an inductor to the structure as shown in Figure 29. This creates a "parasitic" synchronous boost stage that interfaces a new bidirectional port. The voltage of this bidirectional port is controlled by duty-cycle of the phase-leg used. Power flow to the output is controlled by modulating the phase-shift between the two phase-legs in a similar fashion to the conventional PS-FB converter [48-50].

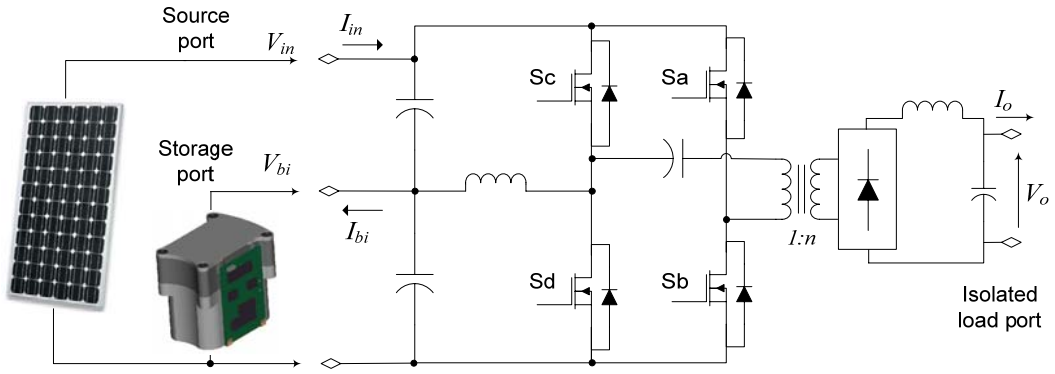


Figure 29 The A-BI-PS-FB converter

It is also possible to interface this added bidirectional port using two boost inductors each connected to a different phase-leg as shown in Figure 30. This allows better distribution of the current stress among the bridge FETs. The resultant topology, the symmetric boost-integrated phase-shift full-bridge (S-BI-PS-FB), is more suitable when a large amount of current flows in the boost section. Power flow is controlled in a similar fashion as in the A-BI-PS-FB.

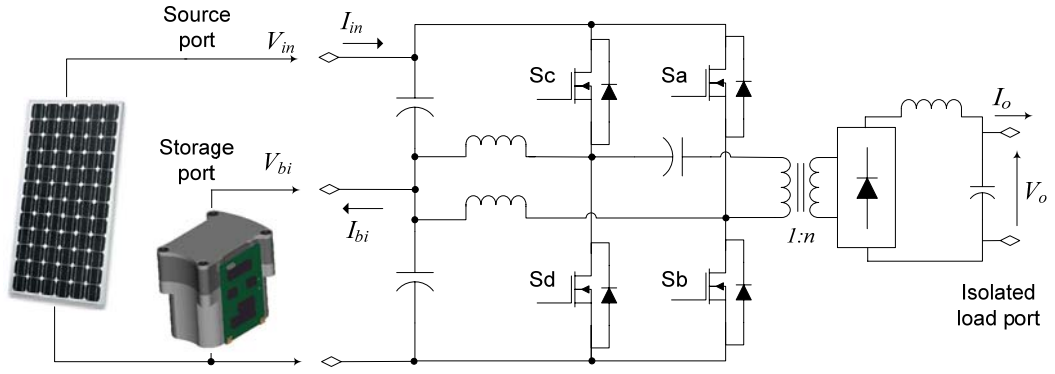


Figure 30 The S-BI-PS-FB converter

3.4. Control Aspects of Multi-Port Systems

3.4.1. Control Objectives, and Degrees of Freedom

In the general sense, the switching waveforms of a power converter can provide any number of degrees of freedom, translating to control variables. The number required, however, depends on the control functionality it is expected to perform. Bus converters do not require a control variable and often implement a fixed voltage transfer ratio. Conventional two-port converter topologies generally provide a single control variable, which is utilized to perform a single control function. Output voltage regulation is a classic example of such a control objective.

In some cases, a single control variable is utilized to achieve multiple mutually-dependent control objectives. The most common example is input current shaping and average output voltage regulation in a PFC ac-dc stage. It is notable here, however, that the shape of the input current is tightly regulated, while its amplitude is variable and is adjusted to regulate the average output voltage.

According to the principle of conservation of energy, a generalized *n*-port converter operating in steady-state, and containing no independently controlled loss mechanisms (dissipative regulators), can perform independent regulation of the operating parameters of up to *(n-1)* ports. This follows from the need for at least a single flexible unregulated port that maintains the power balance in the circuit.

While the number of independently regulated ports is limited in such a system, the number of degrees of freedom provided in the converter is not. The existence of degrees of freedom that exceed the number of independently controlled ports is generally associated with the existence of intermediate converter states not directly coupled to any of the outputs.

Intermediate bus capacitor voltages are a common example of such states. In such cases, it is preferable that the control structure used for the conversion system monitors such intermediate states and ensures their convergence to a suitable steady-state value.

Each of the topologies proposed above exhibits two degrees of freedom, or control variables. For the TM-HB, these are the duty-cycles of the two main switches. For the BI-PS-FB topologies, these are the duty-cycle of the phase-legs, and the relative phase-shift between their switching waveforms.

The two control variables of each topology are sufficient to perform tight independent regulation of two of the converter's ports. The choice of regulated ports is dependent on the application. This choice strongly affects the control structure adopted. It is further possible to dynamically alter the choice of regulated ports and control objectives, as well as the associated control structure, depending on the operating conditions of the devices and systems interfaced through the converter.

3.4.2. Operating Modes of a Battery-Backed Photovoltaic Power System

Consider a sample photovoltaic power system where a solar array and a battery bank are connected to the two ports on the input side of a three-port converter, while the output bus is interfaced through the isolated port on the secondary side. Such a system is likely to operate in one of three modes:

1. Battery-balanced operation: the output voltage is tightly regulated, and the solar array is run under MPPT control. In this case, the battery preserves the power balance in the system by storing unconsumed solar power, or providing the deficit during peak load intervals.

2. Excess insolation operation: the output voltage is regulated and sinks less power than is available, while the battery charge rate is limited. In this case, the battery current or voltage is regulated, while the solar array is left to operate in its voltage-source region where it provides less power than it has available.
3. Flexible load operation: the battery charge is regulated, and MPPT controls the solar arrays. This mode is active when the load is able to sink a variable amount of power, while the battery charge rate is limited. This is useful for a grid-tie inverter system.

3.4.2.1 Sample Control Structure

For the purpose of demonstration, a possible control structure is presented for the mode of battery-balanced operation. The control objectives can be achieved by closing two feedback loops: input voltage regulation (IVR), and output voltage regulation (OVR), as shown in Figure 31.

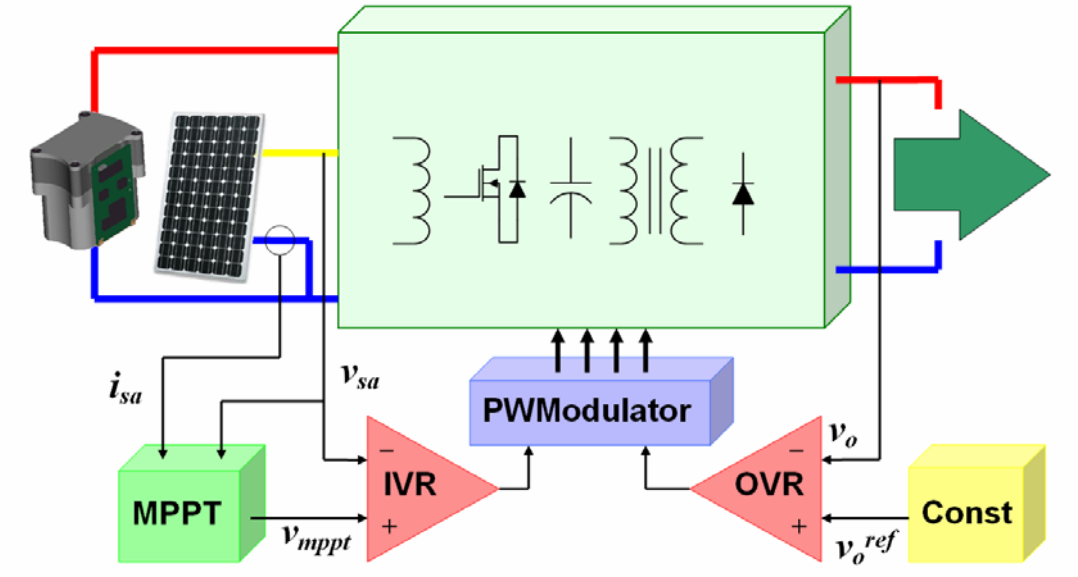


Figure 31 Sample controller structure for a battery-backed solar power system

The IVR loop is used to regulate the solar array voltage to its reference value. This reference is to be provided by an MPPT controller, and represents an estimate of the optimal operating voltage. This intermediate IVR loop allows improved performance and enhanced stability of the MPPT controller whose design is beyond the scope of this work. The OVR loop uses the remaining control variable to tightly regulate the voltage at the output port. Operation of each of the proposed converters under this scheme is discussed in later chapters.

CHAPTER 4: TRI-MODAL HALF-BRIDGE CONVERTER

In this chapter, the operation and characteristics of the TM-HB converter are discussed. This three-port converter, shown in Figure 32, is a modified version of the DCS-HB converter reported in [44]. The fundamental difference is that the DCS-HB topology is a two-port topology with its two main switches, S1 and S2, operated at equal duty-cycles. The proposed tri-modal topology independently controls the duty-cycles of these switches in order to introduce an additional control variable necessary for interfacing the added bidirectional port. This modification results in asymmetric operation of the topology, and changes the design constraints on the converter components, while preserving the topological ability for ZVS. Figure 33 shows the expected steady-state operating waveforms of the proposed topology.

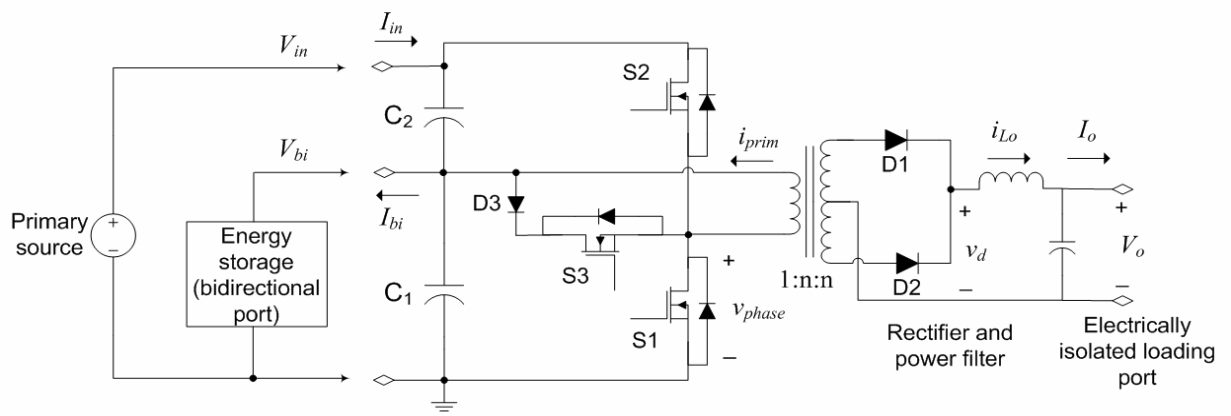


Figure 32 The TM-HB converter

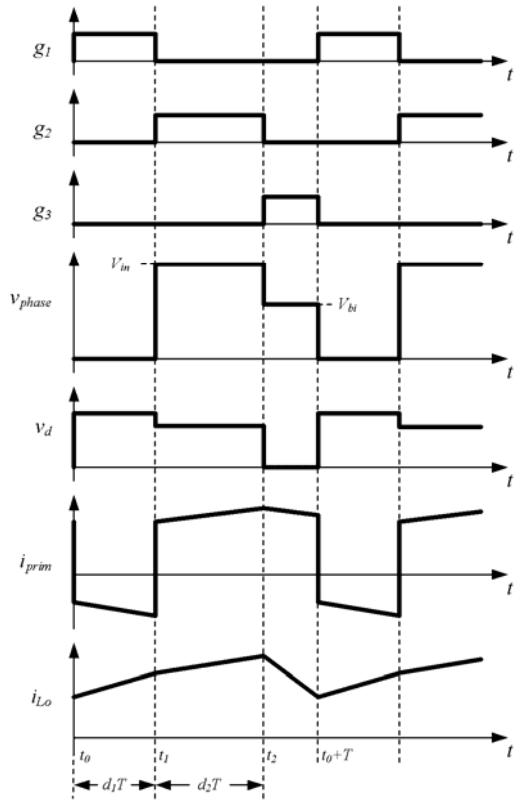


Figure 33 Basic switching waveforms of the TM-HB converter

4.1. Modes of Operation and Steady-State Analysis

In a constant frequency PWM control scheme, the tri-modal topology has three basic modes of operation within a switching cycle. In Mode I, S1 is gated on, applying a positive voltage to the transformer primary winding, until S2 is turned on and S1 turned off to start Mode II. In Mode II, a negative voltage is applied to the transformer primary winding until S3 is gated on to start Mode III, during which zero voltage is applied to the transformer primary. This allows both the magnetizing and load-filter inductor currents to free-wheel.

4.1.1. Regular Operating Modes

Assuming an ideal lossless converter, the steady-state relations between different port voltages can be determined by equating the voltage-second product across the converter's two main inductors to zero. First, using volt-second balance across the primary transformer magnetizing inductance when operating in continuous conduction mode (CCM), there is:

$$-D_1 \cdot T \cdot V_{C1} + D_2 \cdot T \cdot V_{C2} = 0$$

With $V_{in} = V_{C1} + V_{C2}$, and $V_{bi}=V_{C1}$, the voltage at the bidirectional port, V_{bi}, may be given by:

$$V_{bi} = \frac{D_2}{D_1 + D_2} \cdot V_{in} \tag{4.1}$$

where V_{in} is the voltage of the input port, D_1 and D_2 are the duty-cycles of S1 and S2, respectively, and T is the duration of the switching cycle. Assuming CCM operation, the volt-second balance across the load filter inductor yields:

$$D_1 \cdot T \cdot \left(n \cdot V_{C1} - V_o\right) + D_2 \cdot T \cdot \left(n \cdot V_{C2} - V_o\right) - \left(1 - D_1 - D_2\right) \cdot T \cdot V_o = 0$$

$$V_o = D_1 \cdot n \cdot V_{C1} + D_2 \cdot n \cdot V_{C2} = 2 \cdot \frac{D_1 \cdot D_2}{D_1 + D_2} \cdot n \cdot V_{in} \tag{4.2}$$

where n is the turns' ratio of the transformer, and V_o is the load-port voltage. Using Equation (4.1), this can also be re-written as:

$$V_o = 2 \cdot D_1 \cdot n \cdot V_{bi} \tag{4.3}$$

Assuming a lossless converter, steady-state port currents can be related by applying the power conservation principle as follows:

$$V_{in} \cdot I_{in} = V_{bi} \cdot I_{bi} + V_o \cdot I_o \tag{4.4}$$

where I_{in}, I_{bi}, I_o are the average input, bidirectional, and load currents, respectively.

4.1.2. Irregular Operating Modes

While S3 is gated on, if the load filter inductor current is not sufficient to free-wheel the magnetizing inductor current, and if this magnetizing current is negative, the current of D1 drops to zero and turns it off. D2 still conducts the load current, the D3-S3 branch is turned off, and the magnetizing current is either locked to the reflected load current, or exceeds it and forces the body diode of S2 on.

Under such modes, the converter voltages do not follow the relations in Equations (4.1) to (4.3). It is important to note that while these modes are irregular, they are not dangerous. In fact, these modes of operation allow the converter to continue supplying the load from the bidirectional port if the main source is absent. Experimental waveforms of the converter operating under these modes are shown in Section 4.4.

4.2. Component Stress and Design Considerations

4.2.1. Magnetizing Current

The magnetizing inductance of the transformer is used to store energy to interface the input and bidirectional ports. The transformer design needs to allow for this dc current flow and becomes similar to an inductor or a flyback transformer design. The average magnetizing current, I_M, reflected to the primary side satisfies:

$$I_{bi} = D_1 \cdot \left(I_M - n \cdot I_o\right) + D_2 \cdot \left(I_M + n \cdot I_o\right)$$

Rearranging:

$$I_M = \frac{I_{bi} + \left(D_1 - D_2\right) \cdot n \cdot I_o}{D_1 + D_2} \tag{4.5}$$

Another expression for I_M can be obtained by using the average input current relation given by:

$$I_{in} = D_2 \cdot (I_M + n \cdot I_o)$$

Rearranging, we have:

$$I_M = \frac{I_{in}}{D_2} - n \cdot I_o \tag{4.6}$$

Notice that I_M can be reduced during design by increasing the nominal value of D_1 and D_2.

4.2.2. Semiconductor Stress

The ideal reverse voltages seen by the switches on the primary side are:

$$V_{S1} = V_{S2} = V_{in} \tag{4.7.a}$$

$$V_{S3} = V_{bi} \tag{4.7.b}$$

While that seen by the diode, D3, is:

$$V_{D3} = V_{in} - V_{bi} \tag{4.8}$$

Assuming CCM operation, and neglecting inductor ripple currents, the rms current in the primary switches are given by:

$$I_{S1}^{rms} = \sqrt{D_1} \cdot \left| n \cdot I_o - I_M \right| \tag{4.9.a}$$

$$I_{S2}^{rms} = \sqrt{D_2} \cdot \left| n \cdot I_o + I_M \right| \tag{4.9.b}$$

$$I_{S3}^{rms} = \sqrt{1 - D_1 - D_2} \cdot \left| n \cdot I_o + I_M \right| \tag{4.9.c}$$

The average current of carried by D3 is:

$$I_{D3}^{avg} = \left(1 - D_1 - D_2\right) \cdot \left(n \cdot I_o + I_M\right) \tag{4.10}$$

Note that it is assumed that the primary leakage inductance carries the reflected load current through the primary winding for the duration of Mode III.

The average currents through the rectifier diodes are:

$$I_{D1}^{avg} = D_1 \cdot I_o \tag{4.11.a}$$

$$I_{D2}^{avg} = (1 - D_1) \cdot I_o \tag{4.11.b}$$

Assuming perfect snubbing (no ringing), the ideal voltage stress seen by the rectifier diodes of a center-tapped rectifier are:

$$V_{D1} = 2 \cdot n \cdot (V_{in} - V_{bi}) \tag{4.12.a}$$

$$V_{D2} = 2 \cdot n \cdot V_{bi} \tag{4.12.b}$$

4.2.3. Selecting the Transformer Turns' Ratio

Stress analysis clearly shows that the turns' ratio of the transformer has a major effect on circuit component stresses. A higher turns' ratio increases the circulating currents on the primary side, translating to higher switch currents and a higher dc magnetizing current. It also increases the voltage at the secondary side, applying higher reverse voltages to the rectifier devices. A minimum turns' ratio, however, is necessary to maintain the ability to achieve the targeted output voltage level with an acceptable head-room for regulation. The proper choice of turns' ratio is strongly dependent on the voltage specifications at the different ports.

For a given bidirectional port voltage, V_{bi}, Equation (4.3) indicates that V_o can be achieved using a suitable combination of n and D_1. The turns' ratio, n, can be reduced by maximizing D_1. This, however, is constrained by the need to allow enough space for D_2, needed in turn for low values of the input voltage, V_{in}.

Given values for V_o and n, the duty-cycle of Mode I is given by:

$$D_1 = \frac{V_o}{2 \cdot n \cdot V_{bi}}$$

The minimum value for the input voltage, corresponding to $D_2^{\max} = 1 - D_1$, can then be given by:

$$V_{in}^{\min} = \left(1 + \frac{D_1}{D_2^{\max}}\right) \cdot V_{bi} = \frac{{V_{bi}}^2}{V_{bi} - \frac{V_o}{2 \cdot n}}$$

Normalizing to the target output voltage:

$$\frac{V_{in}^{\min}}{V_o} = \frac{\left(\frac{V_{bi}}{V_o}\right)^2}{\frac{V_{bi}}{V_o} - \frac{1}{2 \cdot n}} \tag{4.13}$$

This equation can then be used to draw the turns' ratio design curves, over which the design specifications can be overlaid as shown in Figure 34. Theoretically, the input voltage can be raised infinitely high by lowering D_2. This means that a particular converter design can properly operate and regulate the average voltage if the port voltage combination at the primary side lies at or above the curve corresponding to the turns' ratio.

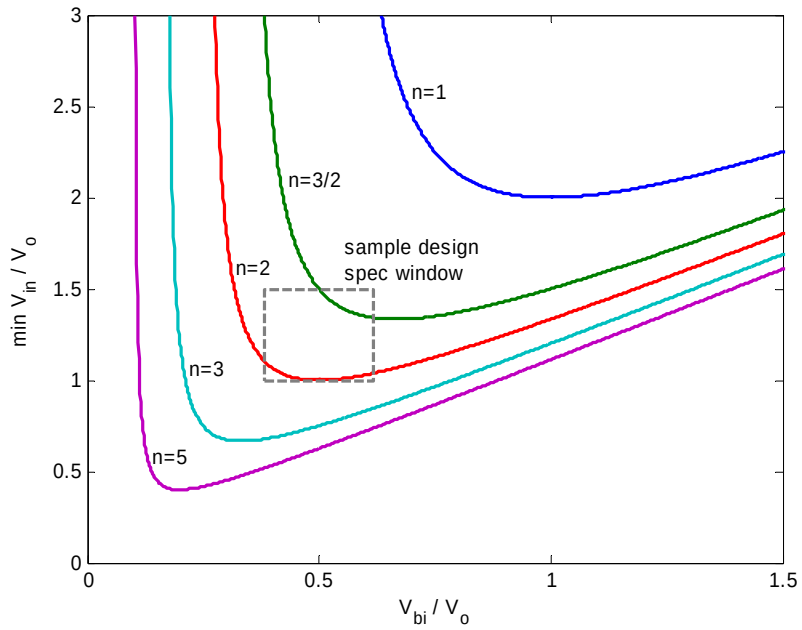


Figure 34 Turns' ratio design curves

The smallest turns' ratio whose curve lies completely below the design specifications window is theoretically sufficient to achieve the target output voltage, V_o. It is recommended that a turns' ratio 20-30% higher be chosen to account for non-idealities, and allow head-room for proper dynamic regulation performance.

4.2.4. Driving Considerations

To avoid shoot-through in S1/S2 or S1/S3, it is important to allow dead-time intervals between Modes I and II, and Modes III and I, respectively. The duration of such dead-time intervals is dependent on the specific converter design and affects ZVS behavior. On the other hand, S2 and S3 need to have some gating overlap time. The duration of this overlap time is not critical, since S3 is forced to have zero current until S2 is turned off. A typical bootstrap mechanism can be used to drive switches S2 and S3 if N-channel devices are used.

4.3. Control Strategy

The proposed converter topology is suitable for a number of power harvesting and energy management applications. The control objectives and strategy should be chosen according to the specific application.

Consider a system powered by a solar array connected to the input port and backed by a battery bank connected to the bidirectional port. Stable system operation requires the maintenance of power balance in the system. That is, in steady-state, the sum of average input power to the converter is required to equal the sum of average output power plus any power losses. This implies that, for a three-port system, the operating point of up to two ports can be tightly regulated, while the third port should be kept "flexible" and would operate at any point that satisfies the power balance constraints.

The choice of the flexible power port dictates the feedback control layout. This choice can be fixed, or may dynamically vary with the operating conditions. Figure 35 shows a suggested control structure for this system when it operates in its battery-balanced mode. Two feedback controllers utilize the two control inputs of the modulator: an OVR controller utilizes signal s, while an IVR controller utilizes signal r. This strategy allows the load voltage to be tightly regulated and prevents load transients from affecting the operation of the solar source. The operating voltage of the solar source is independently controlled by the IVR loop to match its reference value, v_{mppt}, provided by the MPPT controller. In this system, battery storage plays a critical role of balancing the system energy by injecting power at heavy loads and absorbing excess power when available solar power exceeds the load demand.

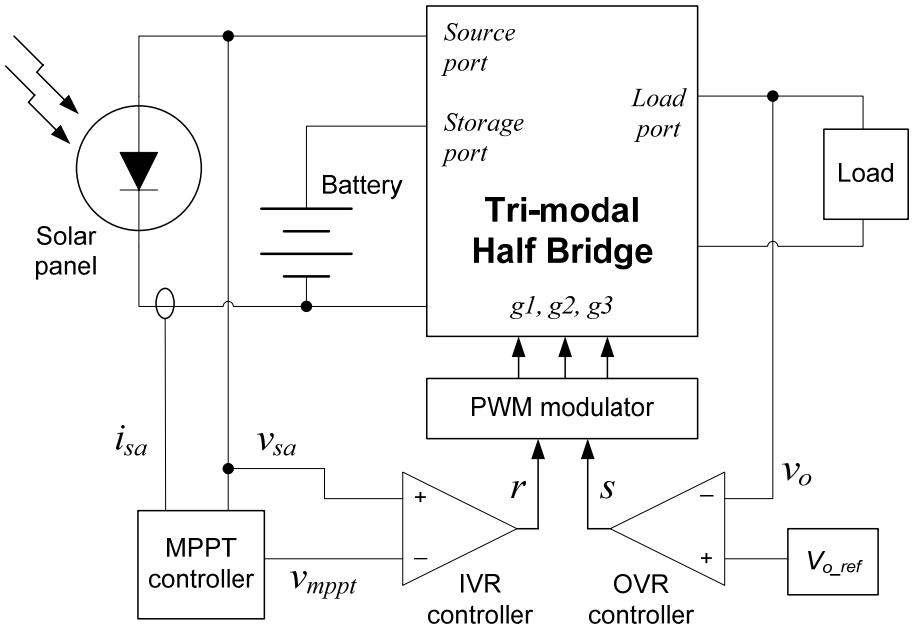


Figure 35 Suggested control structure for battery-balanced operation of a solar power system

Equation (4.3) suggests that the output voltage is determined primarily by the battery voltage and the value of D_1. D_2 affects the input voltage and ideally has no effect upon the steady-state voltage at the load. This allows for the use of a simplified modulator where the control variables r and s are equal to d_2 and d_1, respectively. Such an arrangement lends itself to a digitally-controlled implementation of the controller.

Figure 36 shows a small-signal model of the closed-loop system. The plant is described by four transfer functions that describe the response of the two controlled variables to the duty-cycle values. The symbolic derivation of these linearized transfer functions is fairly tedious. Alternatively, the dynamics of the plant can be described in matrix form. A computer can then be used evaluate and plot the necessary transfer functions for the frequency range of interest.

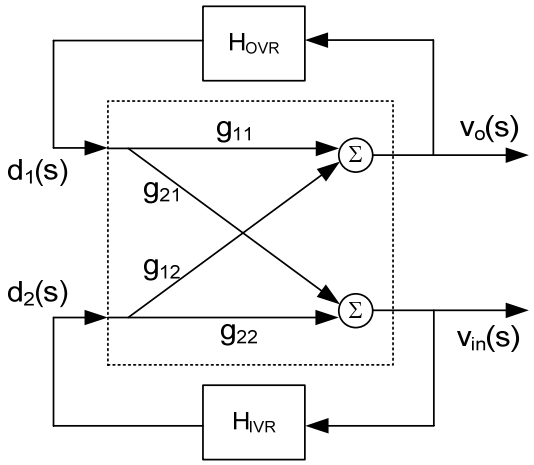


Figure 36 Small signal dynamic model structure of the closed-loop system

The plant small-signal dynamics can be described as:

$$A(s)\cdot X(s) = B(s)\cdot U(s) \tag{4.14}$$

with:

$$A(s) = \begin{bmatrix} Y_{in}(s) & D_2 & nD_2 & 0 \\ -D_2 & Z_M(s) & 0 & 0 \\ -nD_2 & 0 & Z_{Lo}(s) & 1 \\ 0 & 0 & -1 & Y_o(s) \end{bmatrix},\ X(s) = \begin{bmatrix} v_{in}(s) \\ i_M(s) \\ i_{Lo}(s) \\ v_o(s) \end{bmatrix},$$

$$B(s) = \begin{bmatrix} 0 & -(I_M + nI_o) \\ -V_{bi} & V_{in} - V_{bi} \\ nV_{bi} & n\cdot(V_{in} - V_{bi}) \\ 0 & 0 \end{bmatrix},\ U(s) = \begin{bmatrix} d_1(s) \\ d_2(s) \end{bmatrix}$$

where:

$Y_{in}(s) = sC_{in} + 1/r_s$, $Z_M(s) = sL_M$, $Z_{Lo}(s) = sL_o$, and $Y_o(s) = sC_o + 1/r_o$. C_{in} and C_o are the input and output port capacitor values, L_M is the magnetizing inductance referred to the primary side, L_o is the load filter inductance, r_s is the incremental output resistance of the source, and r_o is the incremental load resistance.

Open-loop characteristics of the plant can then be described as:

$$X(s) = C(s) \cdot U(s) = A(s)^{-1} \cdot B(s) \cdot U(s) \tag{4.15}$$

$$g_{11} = C(s)(4,1)\,,\ g_{21} = C(s)(1,1)\,,$$

$$g_{12} = C(s)(4,2)\,,\ g_{22} = C(s)(1,2)\,. \tag{4.16}$$

The design of the OVR controller is dictated by the frequency response of the output voltage to perturbations in d_1, $v_o(s) \big/ d_1(s)$. A perturbation of d_1 induces a perturbation of the input voltage. If the IVR loop is closed, that induces a perturbation in d_2 and has a secondary effect upon the response of the output voltage. This is described mathematically as:

$$\frac{v_o(s)}{d_1(s)} = \frac{g_{11}}{1 + g_{21} \cdot g_{22} \cdot g_{12} \cdot H_{IVR}} \tag{4.17}$$

A similar scenario is encountered when designing the IVR loop. The IVR controller design is dictated by the response of the input voltage to perturbations in d_2, which is given by:

$$\frac{v_{in}(s)}{d_2(s)} = \frac{g_{22}}{1 + g_{12} \cdot g_{11} \cdot g_{21} \cdot H_{OVR}} \tag{4.18}$$

This interdependence of the loops through the power stage complicates the optimization of the controllers. Certain modified modulator structures can be utilized to decouple the control variables and allow each control input to affect a single controlled variable while minimizing its effect on the other. The investigation of such modulator structures, however, is left for future work.

The IVR loop typically has less stringent transient response requirements than the OVR loop. If the IVR loop is designed to have a significantly lower bandwidth, its loop gain can be neglected and it can be considered open around the cross-over frequency of the OVR loop. The OVR controller can then be designed with the approximation:

$$\frac{v_o(s)}{d_1(s)} \approx g_{11}$$

Once the OVR controller, described by H_{OVR}, is designed, the IVR loop design becomes straightforward utilizing Equation (4.18).

4.4. Experimental Verification

A 200W prototype of the proposed converter was constructed and is shown in Figure 37. The converter was designed to handle a 60-90V source, a 25-33V battery, and regulate the load to 60V. Based on the analysis above, the transformer was chosen with a 1:3:3 turns' ratio and designed to handle the rated dc magnetizing current. The magnetizing inductance value referred to the primary side was 165μH. N-channel FETs, IRFB4410, were used for all three switches and were driven by bootstrap-compatible drivers, IR2110. A Schottky barrier diode, B20100, was used in the auxiliary switching branch. Soft recovery diodes, MSR860, were used for the secondary rectifier. No snubber was placed in this experimental phase. The value of the output filter inductor was 147μH. The input, bidirectional, and output port capacitors were 220μF, 390μF, and 33μF. The converter was switched at 100 kHz. A digital board based on the TMS320f2812 DSP chip was utilized to supply the customized switching waveforms required and to perform closed-loop control.

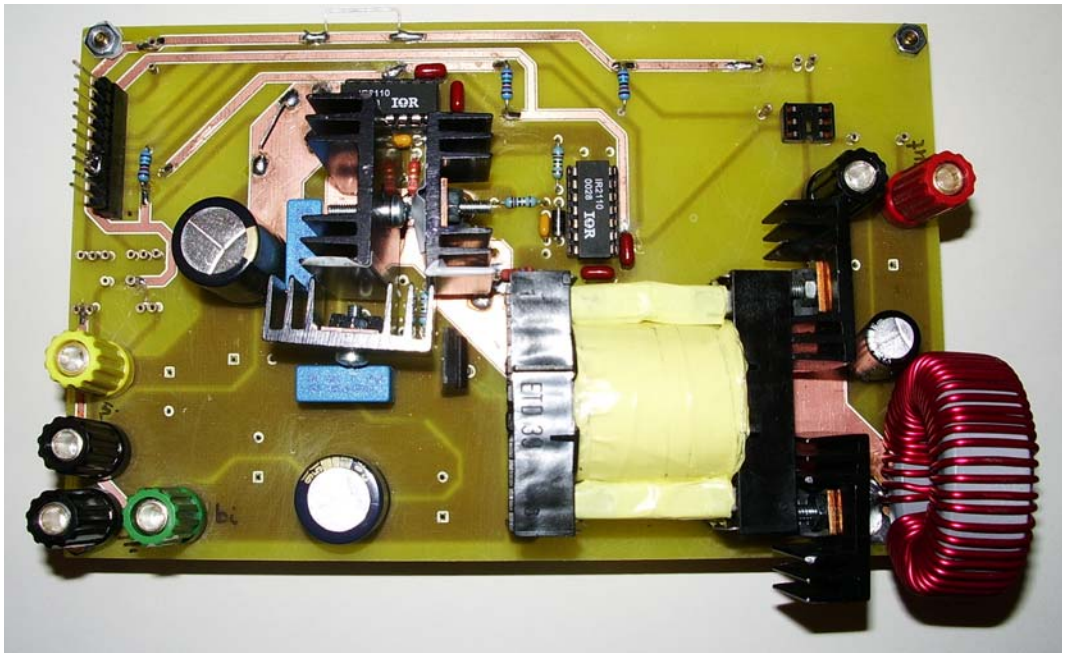
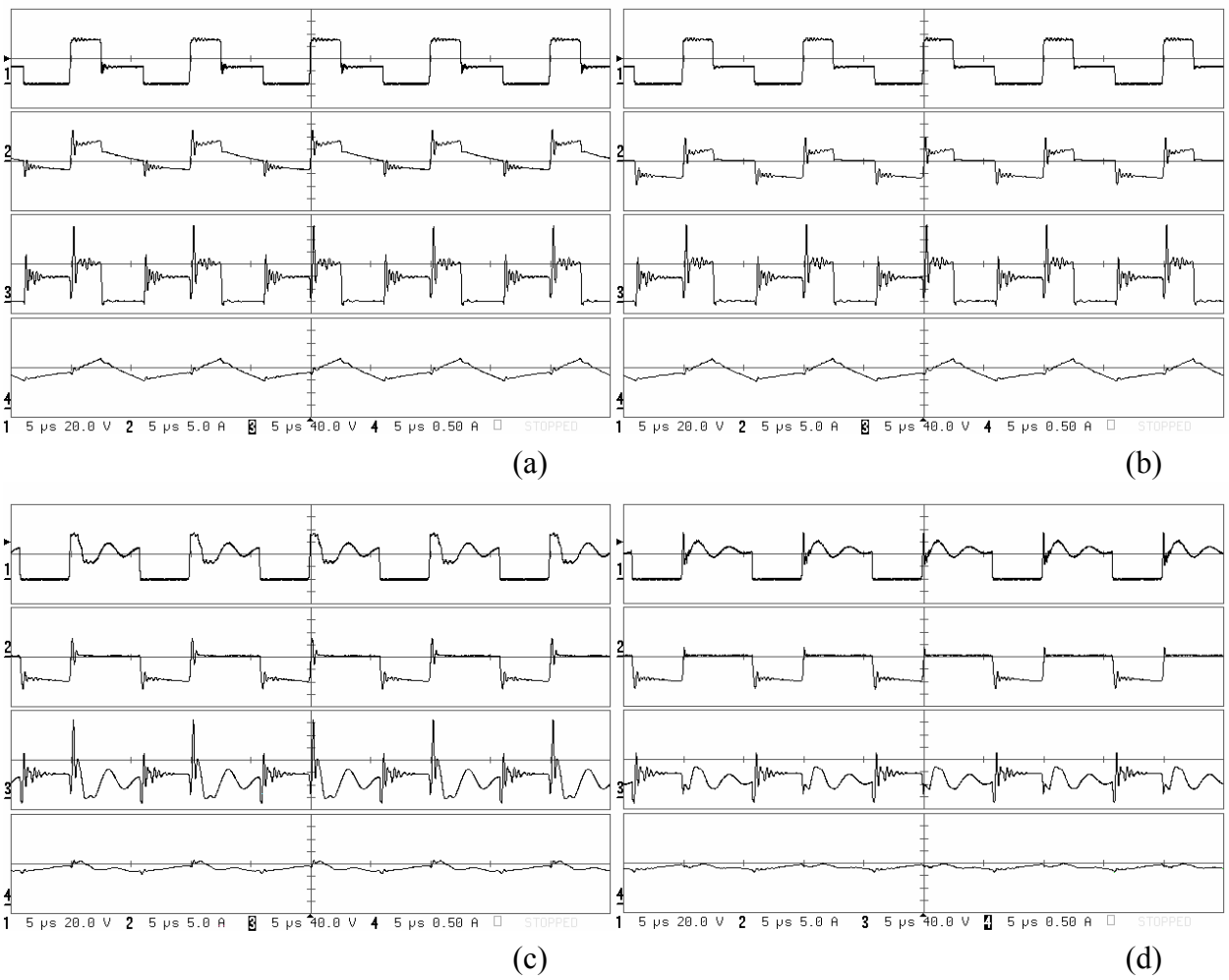


Figure 37 Experimental TM-HB prototype

Figure 38(a-d) shows experimental switching waveforms of the converter. During the four captures, the bidirectional port was held near 28V by a source/load combination simulating a battery. A solar array simulator was used as the primary source, programmed to different power levels. Its voltage was regulated by the converter to 70V. The converter was loaded by a 40Ω resistor, and its voltage was regulated to 60V. Figure 38(a) corresponds to a strong source, supplying 1.78A, with the bidirectional port sinking 0.63A to balance the system power. The source was weaker in Figure 38(b) and supplied 0.89A, and the bidirectional port sourced 1.60A to make up for the power difference. The source was further weakened in Figure 38(c) to source 92mA, and the bidirectional port supplied 3.75A. The source was completely turned off in Figure 38(d) and the bidirectional port supplied 3.92A. In Figure 38(c) and (d), the converter operation deviates from the normal operating modes and operates similar to a forward converter.

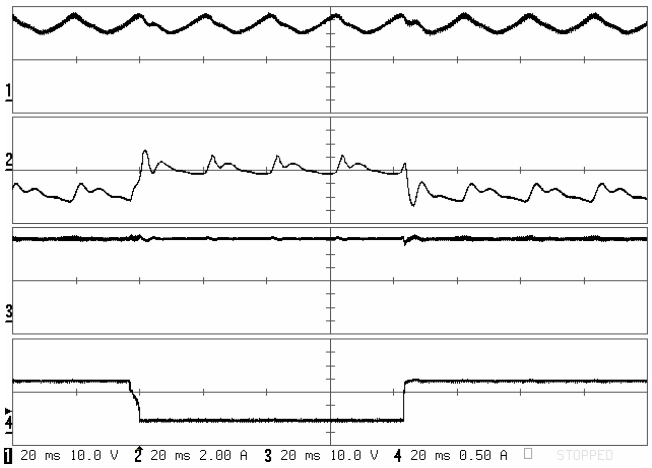


(1) v_{in}, 20V/div (2) i_{bi}, 5A/div (3) v_o, 40V/div (4) i_{lo}, 0.5A/di

Figure 38 Experimental switching waveforms of the TM-HB converter

The control structure described above for battery-balanced system operation was implemented and tested. The output voltage was regulated to 60V using d_1. The input voltage was controlled using d_2 to follow a triangular pattern between 50 and 60V at 50Hz, simulating the output of an MPPT block. The source/load combination at 28V was used to simulate the battery. The source had an open-circuit voltage of 80V, a short-circuit current of 1A, and supplied 0.7A at 60V.

Figure 39 shows the response of this system to a load transient. The load was switched from 30Ω to 130Ω and back. Both the input and load voltages are slightly disturbed due to the load transient, but are recovered very quickly. The bidirectional port seamlessly changes polarity from negative (sourcing) to positive (sinking) and back. Throughout operation, this current exhibits fluctuations at 50Hz—effectively compensating for the power fluctuations in the source power due to dithering.



(1) v_{in}, 10V/div (2) i_{bi}, 2A/div (3) v_o, 10V/div (4) i_{lo}, 0.5A/di

Figure 39 Load transient under closed-loop operation

CHAPTER 5: BOOST-INTEGRATED PHASE-SHIFT FULL-BRIDGE CONVERTERS

This chapter revisits the concept of integrating a boost stage into a PS-FB converter in search for multi-port dc-dc converter topologies. The conventional PS-FB converter utilizes two phase-legs to provide a high-frequency ac voltage waveform suitable for driving the isolation transformer. A "parasitic" synchronous boost converter can be introduced to the structure by introducing one or two boost inductors. Two three-port topologies can be derived in that fashion, where the duty-cycles of the phase-legs are utilized to control power flow in the boost section, while power flow to the load is regulated through changing the phase-shift between the phase-legs.

5.1. Symmetric Boost-Integrated Phase-Shift Full-Bridge

The S-BI-PS-FB converter is constructed by adding two inductors, each to a switch node of the phase-legs of a PS-FB converter, as shown in Figure 40. The free terminals of these two inductors are joined, effectively forming a bi-phase boost converter. This creates a new port capable of sourcing or sinking continuous average power.

This proposed topology is an attractive design alternative when a large amount of power is to be transmitted across an isolation barrier. It promises reduced converter cost through the reduction of component count and converter logistics such as drivers, sensors, and heat-sinks. It

further promises high efficiency due to its ability to achieve ZVS of the bridge switches for a considerable range of operating conditions.

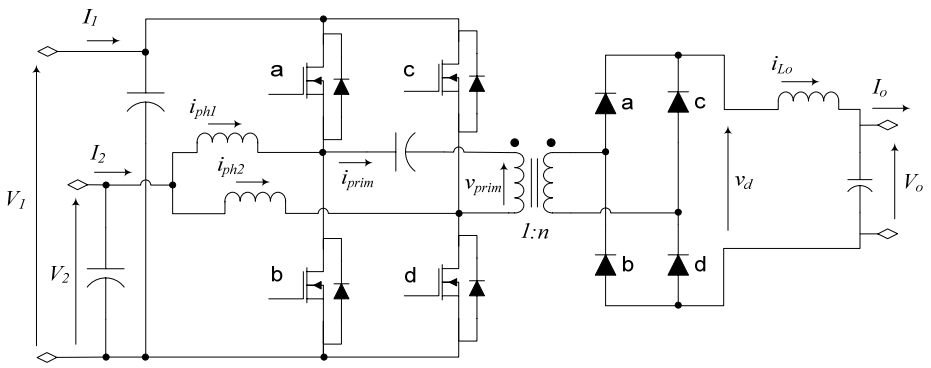


Figure 40 The S-BI-PS-FB converter

The two ports of the topology on the primary side of the transformer are inherently bidirectional. That is, each can source or sink average power depending on the state of the converter and connected devices. The third port, the Load Port, is strictly a power sink if diode rectifiers are used and becomes bidirectional if synchronous rectification is utilized.

5.1.1. Operation and Steady-State Analysis

The characteristics and operation of the S-BI-PS-FB converter are largely inherited from the original topologies it comprises. Typical switching waveforms of the S-BI-PS-FB are shown in Figure 41. As seen in a synchronous boost converter, the two switches of each phase-leg are driven complementarily—with the exception of a very short dead-time to avoid shoot-through. The duty-cycles of both phase-legs are kept equal. Following the approach of a PS-FB topology, the relative phase-shift between the pulse trains of the two legs is used to control power delivery

to the load. The phase-leg duty-cycle values, however, are not kept at 50%. They are rather varied and used to control power flow through the boost section.

The choice of the rectifier topology at the load side is dependent upon application. Full-wave, center-tapped, or current-doubler rectifiers can be used, either with diodes or synchronous devices. A full-wave diode rectifier is assumed in this work. The extension of analysis results to other rectifiers requires only slight modifications.

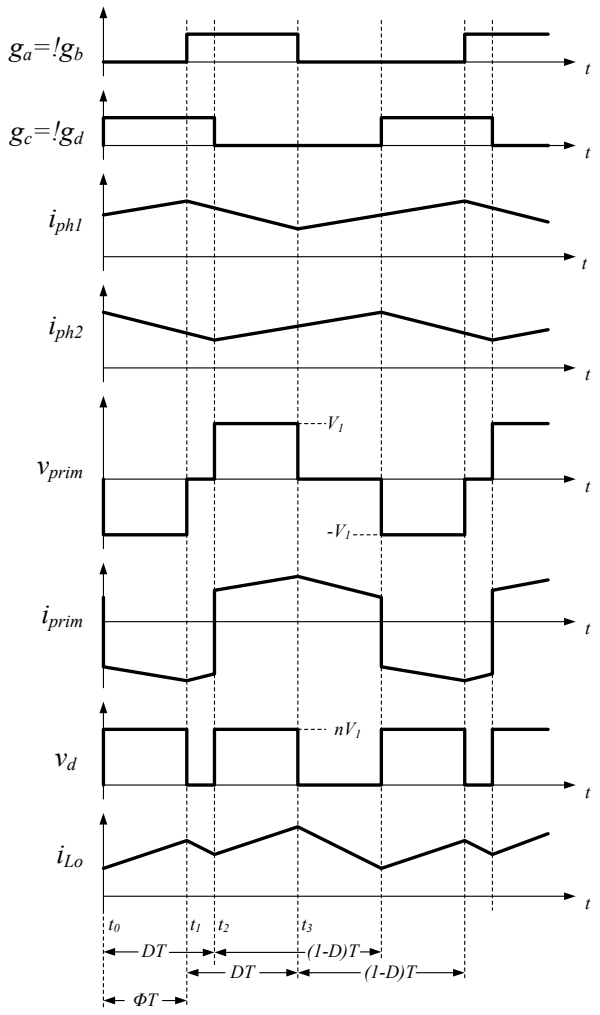


Figure 41 Steady-state switching waveforms of the S-BI-PS-FB topology

Steady-state analysis results are presented here for an ideal loss-less converter operating in CCM. Moreover, duty-cycle loss due to transformer leakage inductance is neglected.

Considering volt-second balance across the boost inductors:

$$D \cdot T_s \cdot (V_1 - V_2) - (1 - D) \cdot T_s \cdot V_2 = 0$$

$$\therefore D \cdot V_1 = V_2 \tag{5.1}$$

where V_1, V_2 are the voltages at Port 1 and Port 2, respectively, D is the duty-cycle of each phase-leg, and T_s is the duration of a switching cycle.

It is notable that this applies to both boost inductors, indicating that the duty-cycle of the two phase-legs is required to be equal to ensure proper operation of the converter. In a practical circuit, small mismatches between the two duty-cycles will produce an imbalance between the currents in the boost inductors. This imbalance is only limited by the parasitic resistances in the current paths. If these resistances are not enough to limit the imbalance to a tolerable value, current-sharing control can be used to enhance the current balance.

Considering volt-second balance across the output filter inductor:

$$2 \cdot \Phi_{eff} \cdot T_s \cdot (n \cdot V_1 - V_o) - (1 - 2 \cdot \Phi_{eff}) \cdot T_s \cdot V_o = 0$$

$$\therefore V_o = 2 \cdot \Phi_{eff} \cdot n \cdot V_1 \tag{5.2}$$

where n is the transformer turns' ratio, V_o is the load voltage. Φ_{eff} is the effective value of the phase-shift between the two switching phase-legs. It is related to the phase-leg duty-cycles and the relative phase-shift, Φ, by:

$$\Phi_{eff} = \min(\Phi, D, 1 - D) \tag{5.3}$$

Note that Φ and Φ_{eff} are expressed as dimensionless values in the range [0, 0.5], corresponding to radian phase-shift values [0, π], or absolute time-shift values of [0, $T_s/2$].

The load current is reflected to the primary side during power delivery periods and is held during free-wheeling periods by the transformer leakage inductance. Due to the presence of a dc-blocking capacitor, a limited dc magnetizing current is born that opposes any dc component resulting from the reflected load current. This can be quantified by considering ampere-second balance through the dc-blocking capacitor:

$$D \cdot T_s \cdot \left(I_M - n \cdot I_o\right) + \left(1 - D\right) \cdot T_s \cdot \left(I_M + n \cdot I_o\right) = 0$$

$$I_M = \left(2 \cdot D - 1\right) \cdot n \cdot I_o \tag{5.4}$$

where I_o is the load current, and I_M is the dc magnetizing transformer current, as seen on the primary winding. This dc magnetizing current is small, and is naturally eliminated at 50% duty. It is important to note that it is not accompanied by any dc voltage imbalance, as guaranteed by the dc-blocking capacitor.

5.1.2. Semiconductor Stress Analysis

The ideal maximum voltage stresses seen across the switching devices are simply given by:

$$V_{switches} = V_1 \tag{5.5}$$

Assuming CCM operation and neglecting inductor current ripple, the rms currents in the switching devices are given by:

$$I_{Sa}^{rms} = \sqrt{D \cdot \left(\left(I_M - I_{ph1}\right)^2 + n^2 \cdot {I_o}^2\right) + 2 \cdot \left(2 \cdot \Phi - D\right) \cdot \left(I_M - I_{ph1}\right) \cdot n \cdot I_o} \tag{5.6.a}$$

$$I_{Sb}^{rms} = \sqrt{\left(1 - D\right) \cdot \left(\left(I_M - I_{ph1}\right) + n^2 \cdot {I_o}^2\right) + 2 \cdot \left(1 - D - 2 \cdot \Phi\right) \cdot \left(I_M - I_{ph1}\right) \cdot n \cdot I_o} \tag{5.6.b}$$

$$I_{Sc}^{rms} = \left|I_{ph2} + I_M - n \cdot I_o\right| \cdot \sqrt{D} \tag{5.6.c}$$

$$I_{Sd}^{rms} = \left| I_{ph2} + I_M + n \cdot I_o \right| \cdot \sqrt{1-D} \tag{5.6.d}$$

where I_{ph1}, I_{ph2} are the boost inductor currents.

The actual voltage stress seen across the secondary rectifier diodes can largely vary depending on many details of a particular design and its associated parasitics. The ideal minimum stress, assuming perfect snubbing, is given by:

$$V_{diodes} = n \cdot V_1 \tag{5.7}$$

The dc currents in the secondary rectifier diodes can be approximated by:

$$I_{Da}^{dc} = I_{Dd}^{dc} = (1-D) \cdot I_o \tag{5.8.a}$$

$$I_{Db}^{dc} = I_{Dc}^{dc} = D \cdot I_o \tag{5.8.b}$$

5.1.3. Zero-Voltage Switching

The S-BI-PS-FB topology merges the ZVS characteristics of the boost and PS-FB converter topologies. The achievement of ZVS is dependent on the amount of current processed by each of the converter sections. ZVS is achieved if the combination of the transformer primary current and the boost inductor current discharges the parasitic capacitance of the switch to zero voltage during the switching dead-time. This forces its anti-parallel diode to conduct until the switch is turned-on. ZVS conditions are discussed next.

5.1.3.1 Switches (a) and (b): Leading Leg Switches

In a PS-FB converter, ZVS of switches (a) and (b) is achieved using the reflected load inductor current. Therefore, the amount of energy stored in the leakage inductance is of no significance.

Considering the boost inductor current, ZVS of switch (a) can be achieved only if:

$$i_{ph1}(t_1) - i_{prim}(t_1) > 0 \tag{5.9.a}$$

This condition is likely to be met at normal operating conditions. It is generally breached when the load is light and a significant amount of current flow through the boost inductor towards Port 2. The operation of the bridge is then dominated by its boost section.

ZVS of switch (b) can be achieved only if:

$$-i_{ph1}(t_3) + i_{prim}(t_3) > 0 \tag{5.9.b}$$

This condition is likely to be breached when the load is light and a significant amount of current flows through the boost inductor towards Port 1. Again, the operation of the bridge would be dominated by its boost section in this instance.

5.1.3.2 Switch (c) and (d): Lagging Leg Switches

The transformer leakage inductance plays the most important role in achieving ZVS of these two switches in the conventional PS-FB topology. Considering the effect of the boost inductor current of that phase, ZVS of switch (c) can be achieved only if:

$$\left(i_{prim}(t_0) + i_{ph2}(t_0)\right) \cdot \sqrt{L_k} > V_1 \cdot \sqrt{2 \cdot C_{ds}^{eff}} \tag{5.9.c}$$

where L_k is the leakage inductance of the transformer as seen on the primary winding and C_{ds}^{eff} is the effective drain-to-source capacitance of each switch.

ZVS of switch (d) is possible if:

$$\left(i_{prim}(t_2) + i_{ph2}(t_2)\right) \cdot \sqrt{L_k} < -V_1 \cdot \sqrt{2 \cdot C_{ds}^{eff}} \tag{5.9.d}$$

In addition to the quantitative constraints presented here, a suitable duration of switching dead-time is required to secure proper ZVS operation.

5.1.4. Power Loss Estimation

5.1.4.1 Conduction loss

Using four identical FETs and assuming equal currents in the boost inductors, the primary switch conduction power loss can be estimated using equations (6.a)-(6.d) to be:

$$P_{chopper}^{CondLoss} = r_{ds}^{on} \cdot \left[\left({I_{ph1}}^2 + {I_{ph2}}^2 \right) + 2 \cdot \left(n^2 \cdot {I_o}^2 - {I_M}^2 \right) \right] \tag{5.10}$$

where r_{ds}^{on} is the on-resistance of the devices used.

Assuming proper boost current sharing, that is, equal dc currents in both phases, the conduction loss expression can further be simplified to:

$$P_{chopper}^{CondLoss} = r_{ds}^{on} \cdot \left[{I_2}^2 \Big/ 2 + 2 \cdot \left(n^2 \cdot {I_o}^2 - {I_M}^2 \right) \right] \tag{5.11}$$

where I_2 is the total boost input current

Rectifier diode conduction power loss can be estimated as:

$$P_{rectifier}^{CondLoss} = 2 \cdot V_D^{on} \cdot I_o \tag{5.12}$$

where V_D^{on} is the on-voltage drop of the rectifier diodes used.

5.1.4.2 Switching Loss

The switching loss of a converter realized using FETs is dominated by turn-on losses, while turn-off losses are negligible. The proposed topology is conditionally able to achieve ZVS of all four switches, resulting in minimized turn-on losses as well. The switching frequency of the converter can then be increased without significantly degrading efficiency.

According to the ZVS constraints derived above, it is possible to design the converter such that it loses ZVS operation for a maximum of two switches. This is the case when low power flows in the PS-FB section, and operation is dominated by the characteristics of the boost section. Worst case switching loss can then be estimated by:

$$P_{chopper}^{SwitLoss} = 2 \cdot C_{ds}^{eff} \cdot V_1^2 \cdot f_s \tag{5.13}$$

Note that this is analogous to the switching loss in a conventional bi-phase boost converter.

5.2. Asymmetric Boost-Integrated Phase-Shift Full-Bridge

The A-BI-PS-FB converter is formed by integrating a uni-phase boost into the PS-FB converter, as shown in Figure 42. This allows the two phase-legs to operate at different duty-cycles, thus increasing the voltage gain of the PS-FB section. Under certain design constraints, this option can lower conduction loss compared with the S-BI-PS-FB, as will be discussed later in this chapter. The boost inductor is introduced to the lagging phase-leg in order to maintain less stringent constraints for ZVS. Similar to the S-BI-PS-FB converter, both primary-side ports are bidirectional, while the functionality of the Load Port is governed by the rectifier used.

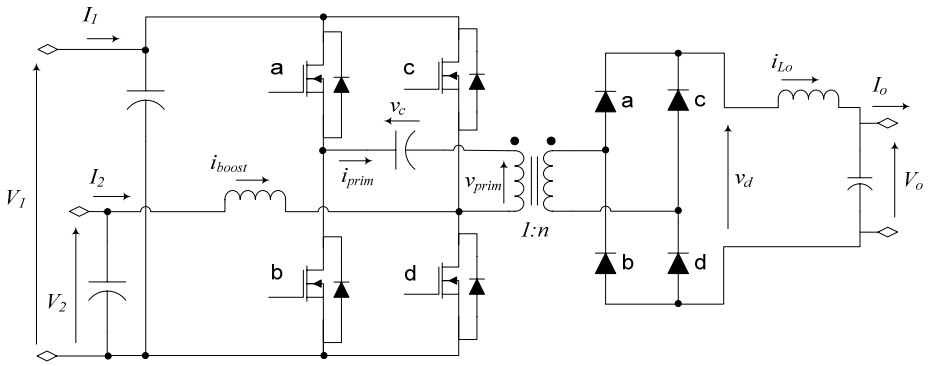


Figure 42 The A-BI-PS-FB converter

5.2.1. Operation and Steady-State Analysis

Typical switching waveforms of the A-BI-PS-FB converter are shown in Figure 43. The boost section of the converter is controlled by varying the duty-cycle of the phase-leg it utilizes, namely the lagging leg. The duty-cycle of the leading leg is chosen to be complementary to that of the lagging leg, while the relative phase-shift of the switching waveforms controls power flow to the load. The dc-blocking capacitor now becomes an indispensable part of the circuit and serves to account for the difference in average voltage between the phase-nodes of the phase-legs. The strength of this switching scheme is its ability to deliver a higher voltage gain of the PS-FB section when the boost duty-cycle is far from 50%.

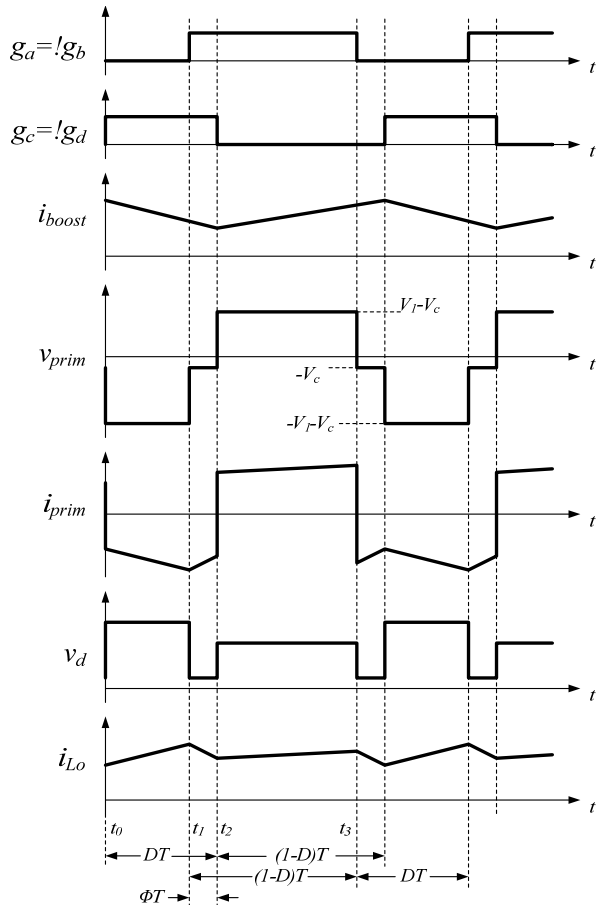


Figure 43 Steady-state switching waveforms of the A-BI-PS-FB topology

Steady-state analysis results are again presented for an ideal loss-less converter operating in CCM. Duty-cycle loss due to transformer leakage inductance is neglected.

Considering volt-second balance across the boost inductor:

$$D \cdot T_s \cdot (V_1 - V_2) - (1 - D) \cdot T_s \cdot V_2 = 0$$

$$\therefore D \cdot V_1 = V_2 \tag{5.14}$$

where D is the duty-cycle of the lagging phase-leg, to which the boost is integrated.

Adopting the asymmetrical switching scheme, the leading leg is switched at a duty-cycle complementary to that of the lagging leg. As a result, the average dc-blocking capacitor voltage, V_c is generally not equal to zero. Its dc value is instead predicted to be the average voltage at the leading leg switch node less that at the lagging leg switch node:

$$V_c = (1 - D) \cdot V_1 - D \cdot V_1 = (1 - 2 \cdot D) \cdot V_1 \tag{5.15}$$

The output voltage is determined by considering the volt-second balance across the output filter inductor:

$$\begin{aligned}(D - \Phi_{eff}) \cdot T_s \cdot [n \cdot (V_1 + V_c) - V_o] + (1 - D - \Phi_{eff}) \cdot T_s \cdot [n \cdot (V_1 - V_c) - V_o] \\ + 2 \cdot \Phi_{eff} \cdot T_s \cdot (n \cdot |V_c| - V_o) = 0\end{aligned}$$

$$\therefore V_o = 4 \cdot \left[D \cdot (1 - D) - \Phi_{eff} \cdot \min(D, 1 - D)\right] \cdot n \cdot V_1 \tag{5.16}$$

It is important to note the fashion by which the phase-shift, Φ, is defined for the A-BI-PS-FB. Using this definition, the output voltage decreases with increased effective phase-shift, Φ_{eff}, as predicted by Equation (5.16). Nevertheless, the relation between the actual and effective phase-shift continues to conform to Equation (5.3).

Due to the presence of a dc-voltage across the dc-blocking capacitor, the load current is reflected to primary side during all main modes of operation. A dc-magnetizing current is formed

in order to oppose any dc-current in the primary winding, and can be estimated by considering the ampere-second balance through the dc-blocking capacitor:

$$\begin{aligned}&(D-\Phi)\cdot T_s\cdot(I_M-n\cdot I_o)+(1-D-\Phi)\cdot T_s\cdot(I_M+n\cdot I_o)\\&+2\cdot\Phi\cdot(I_M-n\cdot I_o\cdot sign(1-2\cdot D))=0\end{aligned}$$

$$I_M=n\cdot I_o\cdot[2\cdot D-1+2\cdot\Phi\cdot sign(1-2\cdot D)] \tag{5.17}$$

5.2.2. Semiconductor Stress Analysis

The ideal maximum voltage stresses seen across the switching devices are simply given by:

$$V_{switches}=V_1 \tag{5.18}$$

Assuming CCM operation and neglecting inductor current ripple, the rms currents in the switching devices are given by:

$$I_{Sa}^{rms}=\sqrt{\begin{aligned}&\left(I_M{}^2+n^2\cdot I_o{}^2\right)\cdot(1-D)\\&+2\cdot I_M\cdot n\cdot I_o\cdot[1-D+\Phi\cdot(sign(2\cdot D-1)-1)]\end{aligned}} \tag{5.19.a}$$

$$I_{Sb}^{rms}=\sqrt{\begin{aligned}&\left(I_M{}^2+n^2\cdot I_o{}^2\right)\cdot D\\&+2\cdot I_M\cdot n\cdot I_o\cdot[-D+\Phi\cdot(sign(2\cdot D-1)+1)]\end{aligned}} \tag{5.19.b}$$

$$I_{Sc}^{rms}=\sqrt{\begin{aligned}&\left((I_M+I_2)^2+n^2\cdot I_o{}^2\right)\cdot D\\&+2\cdot(I_M+I_2)\cdot n\cdot I_o\cdot[-D+\Phi\cdot(sign(2\cdot D-1)+1)]\end{aligned}} \tag{5.19.c}$$

$$I_{Sd}^{rms}=\sqrt{\begin{aligned}&\left((I_M+I_2)^2+n^2\cdot I_o{}^2\right)\cdot(1-D)\\&+2\cdot(I_M+I_2)\cdot n\cdot I_o\cdot[1-D+\Phi\cdot(sign(2\cdot D-1)-1)]\end{aligned}} \tag{5.19.d}$$

The ideal minimum voltage stress across the secondary rectifier diodes, assuming perfect snubbing, is given by:

$$V_{Da}=V_{Dd}=n\cdot(V_1+V_c)=2\cdot D\cdot n\cdot V_1 \tag{5.20.a}$$

$$V_{Db} = V_{Dc} = n \cdot (V_1 - V_c) = 2 \cdot (1 - D) \cdot n \cdot V_1 \tag{5.20.b}$$

The dc currents in the secondary rectifier diodes can be approximated by:

$$I_{Da}^{dc} = I_{Dd}^{dc} = (1 - D + \Phi \cdot sign(2 \cdot D - 1)) \cdot I_o \tag{5.21.a}$$

$$I_{Db}^{dc} = I_{Dc}^{dc} = (D - \Phi \cdot sign(2 \cdot D - 1)) \cdot I_o \tag{5.21.b}$$

5.2.3. Zero-Voltage Switching

Similar to the S-BI-PS-FB, the A-BI-PS-FB converter is conditionally capable of achieving ZVS of all primary bridge switches. The conditions for achieving ZVS are dependent on the operating conditions of either converter section: boost and PS-FB stages. Quantitative conditions for ZVS are derived here, assuming that the boost inductor is interfaced to the lagging leg, as described earlier. This choice is believed to yield better performing converters for most common applications.

5.2.3.1 Switches (a) and (b): Leading Leg Switches

The presence of a dc voltage across the dc-blocking capacitor slightly affects the ZVS behavior of the bridge.

ZVS of switch (a) can be achieved only if:

$$-\sqrt{L_k} \cdot i_{prim}(t_1) > -\sqrt{2 \cdot C_{ds}^{eff}} \cdot V_c \tag{5.22.a}$$

while ZVS of switch (b) can be achieved only if:

$$\sqrt{L_k} \cdot i_{prim}(t_3) > \sqrt{2 \cdot C_{ds}^{eff}} \cdot V_c \tag{5.22.b}$$

As observed from equations (22.a) and (22.b), complete ZVS is dependent on leakage inductance. Given the directions of transformer primary currents, one of these expressions, at most, can be breached at a certain operating condition. These expressions are far less stringent than those of the lagging leg. ZVS of both leading leg switches is practically guaranteed if the leakage inductance is sized to achieve ZVS at the lagging leg.

5.2.3.2 Switch (c) and (d): Lagging Leg Switches

The transformer leakage inductance plays the most important role in achieving ZVS of these two switches in the conventional PS-FB topology. The reflection of load current due to the presence of voltage across the dc-blocking capacitor during "free-wheeling" periods changes the ZVS constraints as follows:

$$i_{prim}(t_0) + i_{ph2}(t_0) > 0 \text{ for } D < 0.5 \tag{5.22.c-1}$$

$$\left(i_{prim}(t_0) + i_{ph2}(t_0)\right) \cdot \sqrt{L_k} > 2 \cdot (1 - D) \cdot V_1 \cdot \sqrt{2 \cdot C_{ds}^{eff}} \text{ for } D \geq 0.5 \tag{5.22.c-2}$$

ZVS of switch (d) is possible if:

$$\left(i_{prim}(t_2) + i_{ph2}(t_2)\right) \cdot \sqrt{L_k} < -2 \cdot D \cdot V_1 \cdot \sqrt{2 \cdot C_{ds}^{eff}} \text{ for } D \leq 0.5 \tag{5.22.d-1}$$

$$i_{prim}(t_2) + i_{ph2}(t_2) < 0 \text{ for } D < 0.5 \text{ for } D > 0.5 \tag{5.22.d-2}$$

Again, a suitable duration of switching dead-time is required to secure proper ZVS operation once the constraints above are met.

5.2.4. Power Loss Estimation

5.2.4.1 Conduction Loss

The primary switch conduction power loss can be estimated using equations (5.19.a)-(5.19.d) to be:

$$P_{chopper}^{CondLoss} = \left(r_{ds}^{lead} + r_{ds}^{lag}\right)\cdot\left(n^2 \cdot {I_o}^2 - {I_M}^2\right) + r_{ds}^{lag} \cdot {I_2}^2 \tag{5.23}$$

where r_{ds}^{lead} and r_{ds}^{lag} are the on-resistances of the leading and lagging leg devices, respectively.

Rectifier diode conduction power loss can be estimated as:

$$P_{rectifier}^{CondLoss} = 2 \cdot V_D^{on} \cdot I_o \tag{5.24}$$

where V_D^{on} is the on-state forward voltage drop of the rectifier diodes used.

5.2.4.2 Switching Loss

Similar to the S-BI-PS-FB, the A-BI-PS-FB can lose ZVS of up to two bridge switches at a given operating condition. Worst case switching loss can then be estimated by:

$$P_{chopper}^{SwitLoss} = 2 \cdot C_{ds}^{eff} \cdot V_1^2 \cdot f_s \tag{5.25}$$

5.3. Port Voltage Considerations

The assignment of voltages and voltage windows to different converter ports is dependent on the characteristics of the systems interfaced to it. The port interfacing the main power source is typically required to accept a wide voltage range. A narrower range is typically required for

storage, while the load port voltage is often held regulated. The effect of this on converter design is discussed in this section.

The main consideration governing port voltages is the need to guarantee proper load regulation at the minimum value of voltage at the full-bridge input, Port 1. While the designer can always opt to increase the transformer turns' ratio in order to suffice the load, that choice increases the circulating current in the primary side and the voltage stress at the rectifier diodes. It is thus preferable to maintain the lowest turns' ratio that meets the load requirements. While the voltage at the boost input, Port 2, is not explicitly involved in determining the output voltage, its accepted variation window inherently plays an important factor as discussed next.

5.3.1. The Symmetric Case

Consider Equation (5.2) that governs the voltage gain of the PS-FB section of the S-BI-PS-FB. Maximum load voltage is achieved at the maximum effective phase-shift, which is itself confined by the duty-cycle of the boost section. In the light of Equation (5.3), the highest effective phase-shift is achieved when the duty-cycle, D, is strictly restricted to 0.5. This corresponds to a boost input voltage, V_2, equal to half of that at the input to the full-bridge, V_1. In the general case, the minimum and maximum duty-cycles, $D_{\min}$ and $D_{\max} = 1 - D_{\min}$, confine the maximum invariably attainable phase-shift, $\Phi_{eff}^{\max}$, to $D_{\min}$. The voltage swing ratio at Port 2 can thus be expressed as:

$$r = \frac{V_2^{\max}}{V_2^{\min}} = \frac{D_{\max}}{D_{\min}} = \frac{1 - \Phi_{eff}^{\max}}{\Phi_{eff}^{\max}} \tag{5.26}$$

The maximum attainable voltage gain of the PS-FB section becomes:

$$\left(\frac{V_o}{V_1}\right)_{\max} = 2 \cdot n \cdot \Phi_{eff}^{\max} = \frac{2}{r+1} \cdot n \tag{5.27}$$

Accordingly, in order to match the load regulation performance, the S-BI-PS-FB needs to be designed with a transformer turns' ratio, n_S, related to that of the conventional cascade system, n_{conv}, by:

$$n_S = \frac{r+1}{2} \cdot n_{conv} \tag{5.28}$$

Increasing the voltage at Port 1 lowers the duty-cycle values required to properly interface Port 2. While this further limits the maximum gain attainable by the PS-FB section, the maximum attainable voltage at the load would not change due to the increase in the sourcing voltage. This means that the turns' ratio is primarily governed by the voltage window of Port 2 and the minimum voltage at Port 1.

5.3.2. The Asymmetric Case

A similar relationship governs the A-BI-PS-FB turns' ratio. According to Equation (5.16), the converter achieves maximum gain at zero phase-shift. That gain is most limited at minimum duty-cycle, $D_{\min}$. Considering the voltage swing ratio at Port 2:

$$r = \frac{V_2^{\max}}{V_2^{\min}} = \frac{D_{\max}}{D_{\min}} = \frac{1 - D_{\min}}{D_{\min}} \tag{5.29}$$

The maximum guaranteed gain of the PS-FB section becomes:

$$\left(\frac{V_o}{V_1}\right)_{\max} = 4 \cdot n \cdot D_{\min} \cdot \left(1 - D_{\min}\right) = \frac{4 \cdot r}{\left(r+1\right)^2} \cdot n \tag{5.30}$$

The load regulation performance can be matched by selecting the turns' ratio to be:

$$n_A = \frac{(r+1)^2}{4 \cdot r} \cdot n_{conv} \tag{5.31}$$

5.3.3. Recommended Port Voltages

The recommended port voltages can now be determined in the light of the discussion above. The minimum and maximum voltages at Port 2 should correspond to the minimum and maximum duty-cycles at minimum Port 1 voltage:

$$V_2^{\min} = D_{\min} \cdot V_1^{\min} \tag{5.32.a}$$

$$V_2^{\max} = D_{\max} \cdot V_1^{\min} \tag{5.32.b}$$

Since $D_{\max} = 1 - D_{\min}$, the center of the voltage window at Port 2 is left at half the minimum Port 1 voltage:

$$V_2^{nom} = 0.5 \cdot V_1^{\min} \tag{5.32.c}$$

It is preferable to limit the input voltage range of a conventional PS-FB converter in order to allow a design that better utilizes the circuit components. This same consideration is inherited by the integrated topologies, and is the main limiting factor of the maximum voltage allowed at Port 1. In fact, for a given design, increasing this voltage widens the permissible voltage window at Port 2.

The load voltage is finally used to determine the turns' ratio of the transformer in coordination with Equations (5.28) and (5.31) for the S-BI-PS-FB and A-BI-PS-FB, respectively. Port voltage considerations are summarized in Figure 44.

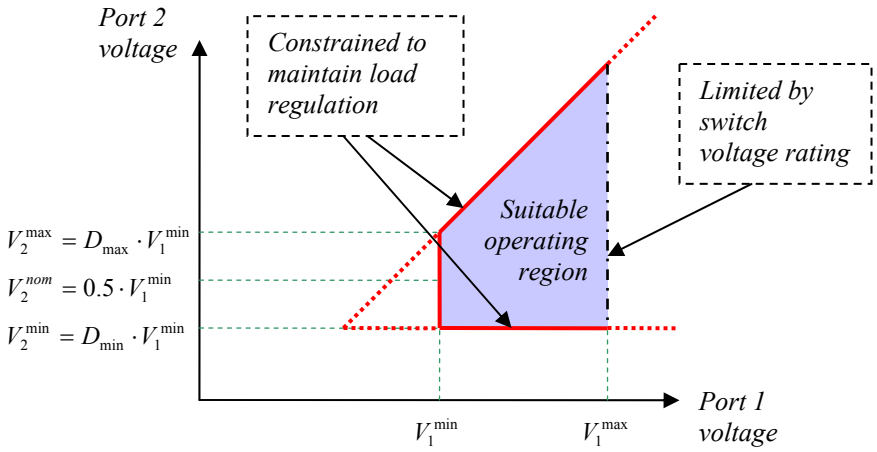


Figure 44 Relation of suitable operating voltages

5.4. Topology Comparison and Selection Guidelines

The two BI-PS-FB topologies introduced in this chapter are each functionally equivalent to a conventional system cascading a synchronous boost and a PS-FB stage as shown in Figure 45. Each of these structures is a valid design alternative and can interface two bidirectional ports and a galvanically isolated loading port. The designer's decision to select one of them should depend on cost, loss, and complexity. This section evaluates the two proposed topologies in reference to the conventional cascade solution, identifies design constraints under which the proposed topologies are preferable, and attempts to quantify the savings they yield. This evaluation focuses on three main aspects most affected by the integration: conduction loss of chopper switches, their ZVS operation, and voltage stress of rectifier diodes.

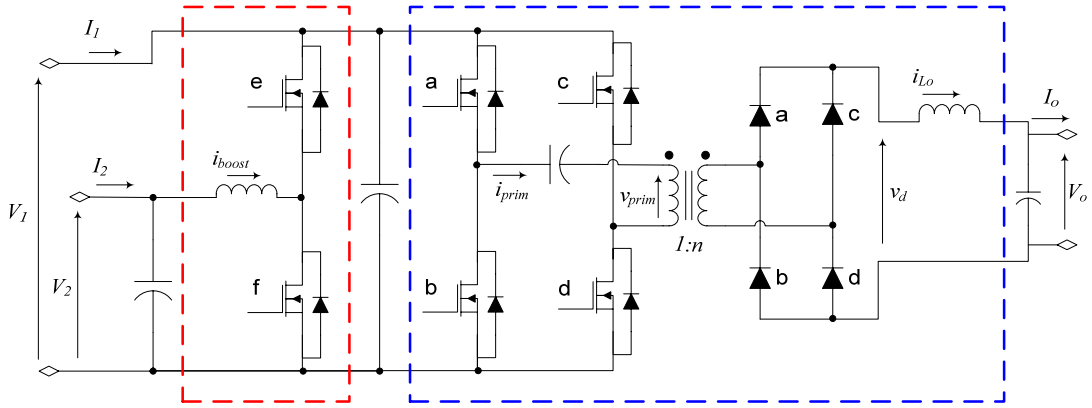


Figure 45 Equivalent conventional cascaded system

5.4.1. Chopper Switch Conduction Loss

In a conventional cascaded system, the switch conduction loss of the boost stage can be estimated as:

$$P_{Bst,Conv}^{CondLoss} = r_{ds}^{B} \cdot I_2^{\,2} \tag{5.33}$$

while that of the switching bridge of the PS-FB stage is estimated by:

$$P_{FB,Conv}^{CondLoss} = r_{ds}^{FB} \cdot n^2 \cdot I_o^{\,2} \tag{5.34}$$

where r_{ds}^{B} and r_{ds}^{FB} are the on-state resistances of the boost and PS-FB stages, respectively.

Estimated switching bridge conduction losses in the S-BI-PS-FB and A-BI-PS-FB are given by Equations (5.11) and (5.23), respectively. Notably, each can be separated into two terms: one related to the boost, and another to the PS-FB section.

The ratio of boost section conduction loss in the two BI-PS-FB topologies to that of a conventional boost converter is primarily affected by the on-state resistance of the devices used.

For the S-BI-PS-FB, realized with four identical FETs, with r_{ds}^{S} on-state resistance, that ratio is estimated as:

$$\frac{P_{bst,S}^{CondLoss}}{P_{bst,Conv}^{CondLoss}} = \frac{r_{ds}^{S}/2 \cdot {I_2}^2}{r_{ds}^{B} \cdot {I_2}^2} = \frac{r_{ds}^{S}}{2 \cdot r_{ds}^{B}} \tag{5.35}$$

Similarly, for the A-BI-PS-FB, the estimate is:

$$\frac{P_{bst,A}^{CondLoss}}{P_{bst,Conv}^{CondLoss}} = \frac{r_{ds}^{lag} \cdot {I_2}^2}{r_{ds}^{B} \cdot {I_2}^2} = \frac{r_{ds}^{lag}}{r_{ds}^{B}} \tag{5.36}$$

The ratio of PS-FB section conduction loss in the BI-PS-FB topologies to that in the conventional system is affected by one more parameter: transformer turns' ratio. As discussed earlier, widening the voltage window required at Port 2 dictates an increase in the suitable turns' ratio, reflecting in turn on the conduction loss. The conduction loss ratio in the PS-FB section of the S-BI-PS-FB to that of a conventional PS-FB converter is:

$$\frac{P_{FB,S}^{CondLoss}}{P_{FB,Conv}^{CondLoss}} = \frac{2 \cdot r_{ds}^{S} \cdot \left({n_S}^2 \cdot {I_o}^2 - {I_M}^2 \right)}{2 \cdot r_{ds}^{FB} \cdot {n_{conv}}^2 \cdot {I_o}^2} = \frac{r_{ds}^{S}}{r_{ds}^{FB}} \cdot \frac{{n_S}^2}{{n_{conv}}^2} \cdot \left(1 - \frac{{I_M}^2}{{n_S}^2 \cdot {I_o}^2} \right) \tag{5.37}$$

This ratio is maximized (worst case) when $I_M = 0$, which corresponds to $D = 0.5$. At that point, this ratio can be related to Port 2 voltage swing ratio, r, using Equation (5.28) as follows:

$$\frac{P_{FB,S}^{CondLoss}}{P_{FB,Conv}^{CondLoss}} = \frac{r_{ds}^{S}}{r_{ds}^{FB}} \cdot \frac{(r+1)^2}{4} \tag{5.38}$$

For the A-BI-PS-FB, that ratio is given by:

$$\frac{P_{FB,S}^{CondLoss}}{P_{FB,Conv}^{CondLoss}} = \frac{\left(r_{ds}^{lead} + r_{ds}^{lag} \right) \cdot \left({n_A}^2 \cdot {I_o}^2 - {I_M}^2 \right)}{2 \cdot r_{ds}^{FB} \cdot {n_{conv}}^2 \cdot {I_o}^2} = \frac{r_{ds}^{lead} + r_{ds}^{lag}}{2 \cdot r_{ds}^{FB}} \cdot \frac{{n_A}^2}{{n_{conv}}^2} \cdot \left(1 - \frac{{I_M}^2}{{n_A}^2 \cdot {I_o}^2} \right) \tag{5.39}$$

At $I_M = 0$, this can be related to the swing ratio, r, using Equation (5.31) as follows:

$$\frac{P_{FB,A}^{CondLoss}}{P_{FB,Conv}^{CondLoss}} = \frac{r_{ds}^{lead} + r_{ds}^{lag}}{2 \cdot r_{ds}^{FB}} \cdot \frac{(r+1)^4}{16 \cdot r^2} \tag{5.40}$$

5.4.1.1 Typical Design Scenario

It is clear from Equations (5.35), (5.36), (5.38), and (5.40) that conduction loss comparisons need to be considered in the light of particular design constraints, governing the available investment in silicon and the flexibility required in the converter operation. Here, we consider a typical situation likely to be encountered in a practical design:

Consider a reference conventional system consisting of two cascaded stages: a uni-phase boost stage, and a PS-FB stage. Assume that the boost converter uses FETs each twice the size of those used in the PS-FB section, thus incurring a comparable amount of conduction loss. The on-state resistances relationship is:

$$2 \cdot r_{ds}^{B} = r_{ds}^{FB}$$

This is compared with an S-BI-PS-FB converter with four identical FETs with on-state resistance:

$$r_{ds}^{S} = r_{ds}^{B} = r_{ds}^{FB} \Big/ 2$$

It is also compared with an A-BI-PS-FB converter with leading and lagging leg FETs of on-state resistances related by:

$$\frac{4}{3} \cdot r_{ds}^{lead} = \frac{8}{3} \cdot r_{ds}^{lag} = r_{ds}^{FB}$$

These resistance relationships were assumed based on an equal investment in FET silicon area in the three systems compared. FET conduction loss ratios can now be evaluated using

Equations (5.35), (5.36), (5.38), and (5.40). They are now plotted against Port 2 voltage swing ratio, r, in Figure 46.

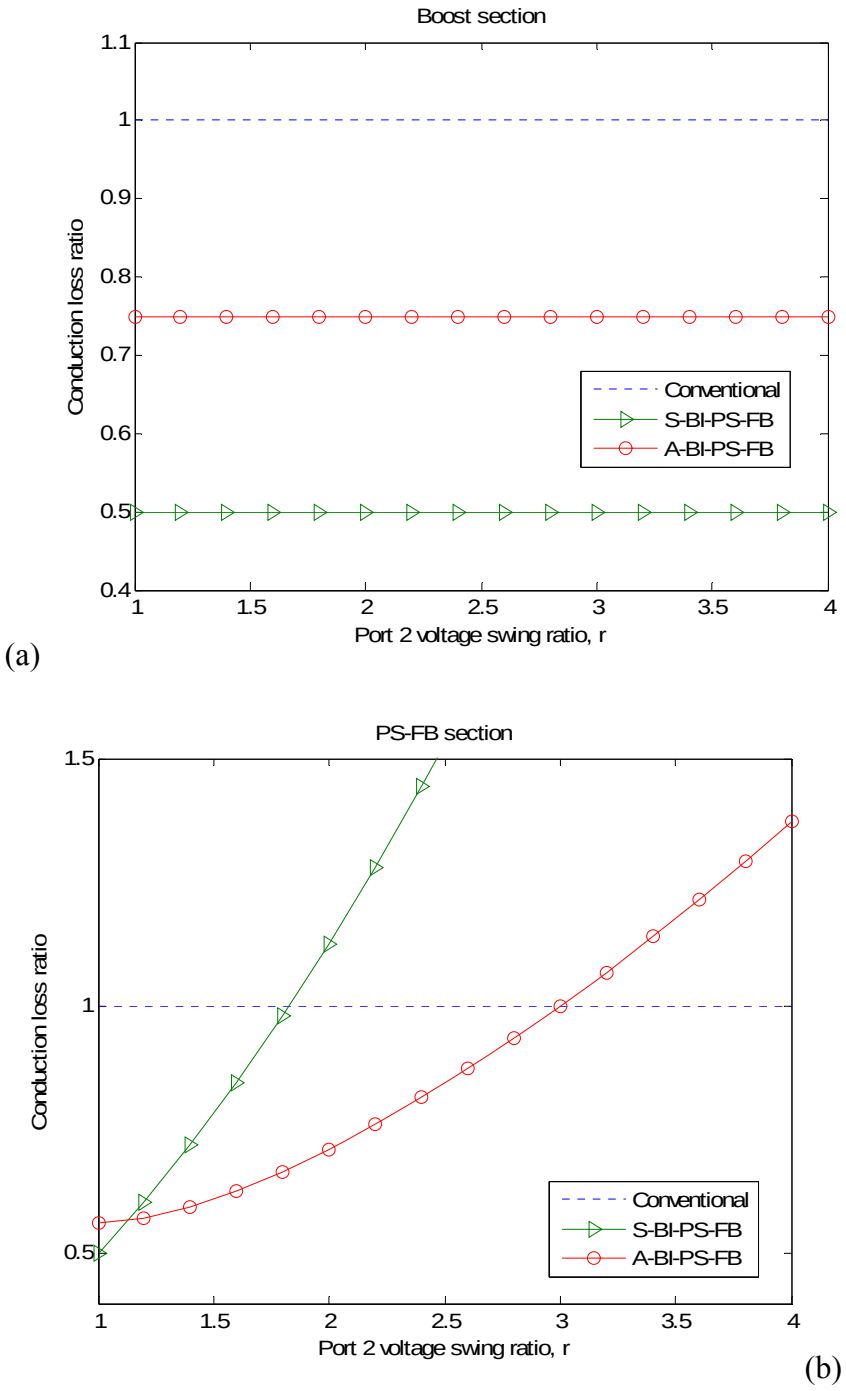


Figure 46 Conduction loss ratio comparison (a) boost section (b) PS-FB section

For the example considered here, the S-BI-PS-FB incurs significantly less conduction loss in the boost section. The A-BI-PS-FB, however, incurs less in the PS-FB for most values of r. Overall conduction loss comparison thus needs to consider the utilization ratio of each section. The conduction loss ratio is plotted in Figure 47 assuming equal utilization of the boost and PS-FB sections. In general, the S-BI-PS-FB is preferred for lower values of r, while the A-BI-PS-FB is preferred for higher values. That is, the A-BI-PS-FB is more suitable for systems that are designed to handle a wider voltage swing at the boost input, Port 2.

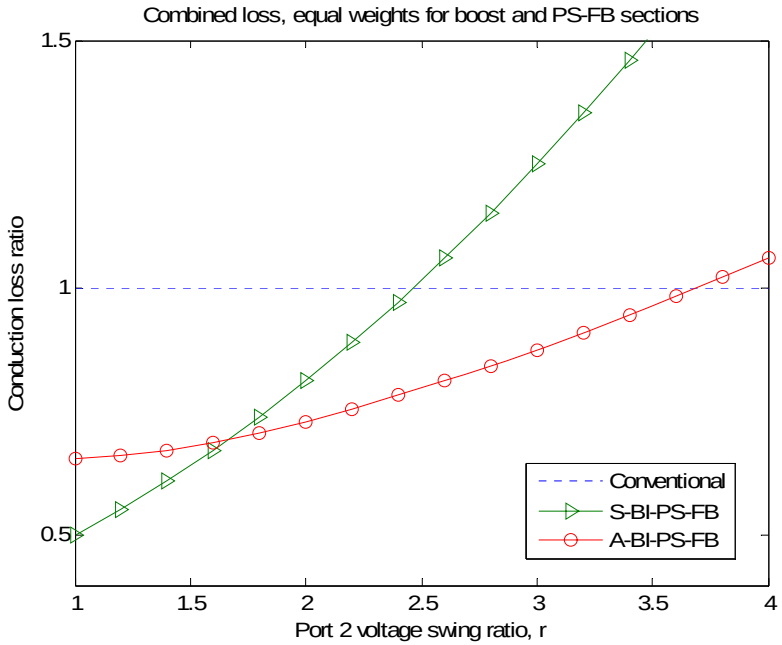


Figure 47 Conduction loss ratio comparison assuming equal utilization of boost and PS-FB sections

5.4.2. Rectifier Diode Voltage Stress

The maximum reverse voltage stress across the rectifier diodes is dependent upon the magnitude of the ac voltage transmitted through the transformer and the amount of ringing

present in the circuit. To provide a fair comparison, the ideal voltage stress is considered here assuming that "perfect" snubber circuits are used, i.e., there is no voltage overshoot.

In the S-BI-PS-FB, the ideal voltage stress is simply given by Equation (5.7). Comparing to a conventional PS-FB stage, Equation (5.7) is combined with (5.28) to yield:

$$V_{diodes}^{S} = \frac{r+1}{2} \cdot n_{conv} \cdot V_1$$

It then follows that:

$$\frac{V_{diodes}^{S}}{V_{diodes}^{Conv}} = \frac{r+1}{2} \tag{5.41}$$

For the A-BI-PS-FB, the ideal voltage stress is further affected by the value of the duty-cycle as suggested by Equations (5.20.a) and (5.20.b). Combining to Equation (5.31), worst-case ideal voltage stress becomes:

$$V_{diodes}^{A} = \frac{2 \cdot r}{r+1} \cdot \frac{(r+1)^2}{4 \cdot r} n_{conv} \cdot V_1 = \frac{r+1}{2} n_{conv} \cdot V_1$$

This yields:

$$\frac{V_{diodes}^{A}}{V_{diodes}^{Conv}} = \frac{r+1}{2} \tag{5.42}$$

At the higher end of the voltage range at Port 1, the duty-cycle of the leading leg can be varied to ensure that the rectifier voltage stress does not increase beyond the designed value due the variation of the dc-blocking capacitor voltage. Equations (5.41) and (5.42) suggest that both proposed integrated topologies, if properly operated, have a similar profile of the voltage stress across rectifier diodes for the same design constraints.

5.4.3. ZVS Operation of Chopper FETs

ZVS operation in the integrated topologies is dependent upon the satisfaction of the constraints developed in earlier sections, as well as the proper choice of switching dead-time. The satisfaction of the constraints is primarily a function of the magnitude and direction of currents flowing in the two sections of the converter. Regions where these topologies are likely to achieve or lose ZVS are investigated here, and discussed in reference to ZVS operation of the reference conventional cascaded system.

The ZVS characteristics of a conventional cascaded system are summarized in Figure 48. The PS-FB stage naturally achieves ZVS of both leading leg FETs at all times. The transformer leakage inductance is sized in order to maintain ZVS for a wide load range at the lagging leg. However, ZVS is lost at low load currents due to the lack of energy to discharge their output capacitances.

The synchronous boost stage, when operated at very low currents, achieves ZVS of both of its FETs by means of current circulating through the filter inductor. As the dc value of the inductor current increases (with increased power flow), ZVS is lost on one of the two switches depending on the direction of power flow. For positive boost dc current, ZVS is achieved at the upper FET and lost at the lower one. Conversely, ZVS is lost on the upper FET for negative boost dc currents and is achieved at the lower FET.

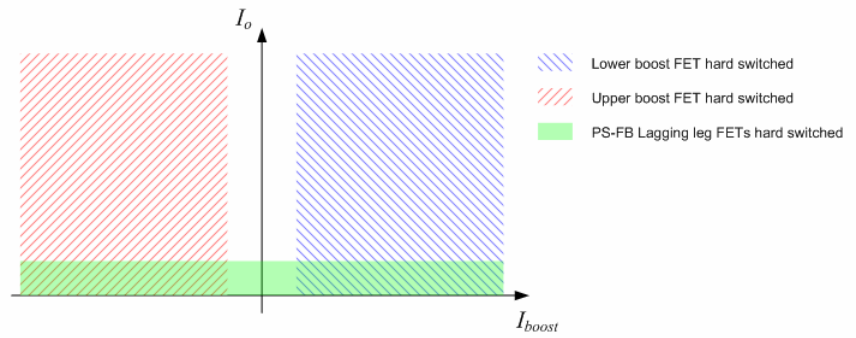


Figure 48 ZVS profile of the conventional cascaded system

A strong merit of the proposed S-BI-PS-FB converter topology is its ability to achieve ZVS of all FETs for a majority of operating conditions. ZVS, however, is partially lost whenever the boost section processes a large amount of power compared to that in the PS-FB section. In this case, the converter is dominated by the characteristics of the boost, and loses ZVS of the lower FETs for large positive boost currents and that of the upper FETs for large negative boost currents. This is summarized in Figure 49.

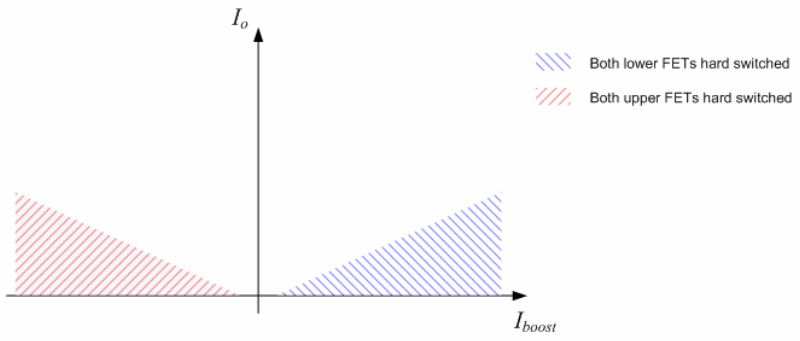


Figure 49 ZVS profile of the S-BI-PS-FB converter

As for the A-BI-PS-FB converter, leading leg FET ZVS is only a function of the currents flowing in the PS-FB section. ZVS operation can be generally maintained for both switches for all practical operating conditions. At very low PS-FB currents, however, the constraints derived

in Section 5.2 suggest that ZVS on the lower leading FET can be lost if the duty-cycle is lower than 0.5, while ZVS on the upper FET can be lost if the duty-cycle is higher than 0.5. This can be attributed to the presence of a dc voltage across the dc-blocking capacitor. The region where leading leg ZVS is partially lost is generally very narrow since it requires considerably less leakage energy than that required by the lagging leg.

Examining Equations (5.22.c) and (5.22.d) indicates that ZVS on the lagging leg FETs is largely dependent on the relation of the boost inductor and transformer primary currents. The ZVS profile is dependent on the phase-leg duty-cycle because of the accumulation of dc-voltages of different polarities across the dc-blocking capacitor. This profile is summarized in Figure 50.

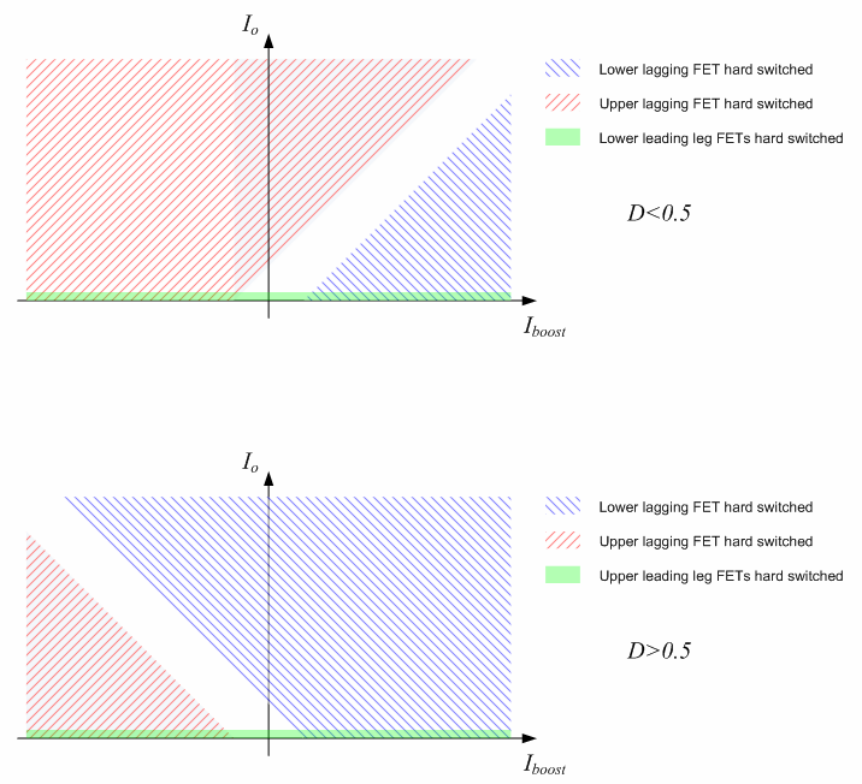


Figure 50 ZVS profile of the A-BI-PS-FB converter with (a) D<0.5 (b) D>0.5

From the graphs shown above, it can be noted that the S-BI-PS-FB converter has the widest operating regions where all FETs are operated at ZVS. It is thus preferable in applications with dominant switching losses.

5.4.4. Comparison Summary

In summary, the comparison of the three design alternatives shows that the best choice of topology is dictated by the application requirements. Port 2 voltage swing ratio, r, required for a given application, directs the selection of the topology. For low values or r, a design based on the S-BI-PS-FB topology is likely to incur least conduction and switching losses. This topology is particularly suitable when most power flow occurs between Port 1 and Port 2, and when switching frequency is required to be high. As the value of r increases beyond 2.0, the conduction loss of the PS-FB of the S-BI-PS-FB increases quickly and becomes a limiting factor. The A-BI-PS-FB topology becomes most favorable, offering the best savings in conduction loss. For extreme value of r, beyond 3.5, integrated topologies become unsuitable due to exaggerated transformer turns' ratio and high voltage stress at the rectifier diodes. In that case, the conventional cascaded system remains the preferred design alternative.

5.5. Control Strategy and Controller Design

5.5.1. Sample Control Structure

For the purpose of demonstration, a possible control structure is presented for the S-BI-PS-FB converter under battery-balanced operating mode. The control objectives can be achieved by closing two feedback loops: IVR and OVR, as shown in Figure 31.

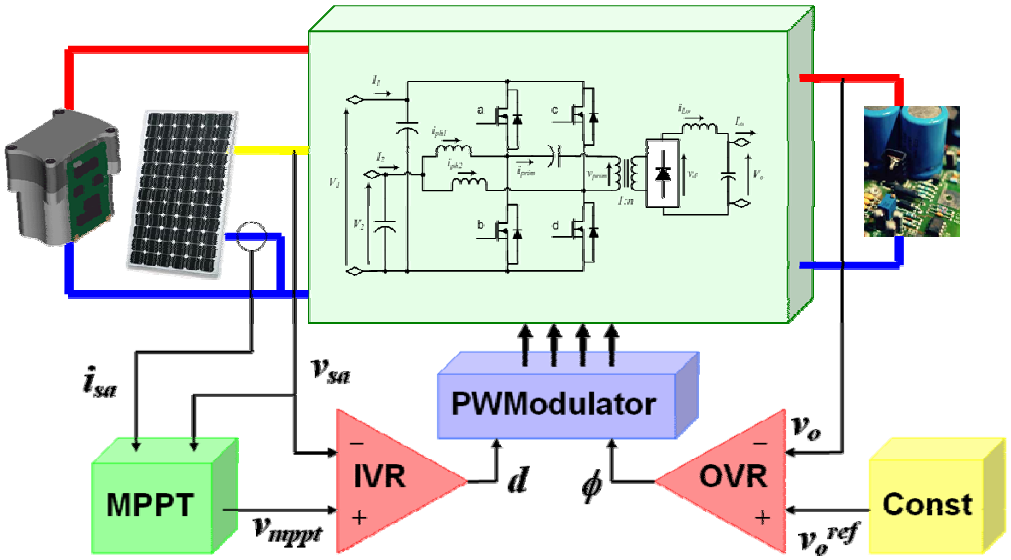


Figure 51 Sample controller structure for a battery-backed solar power system

The IVR loop is used to regulate the solar array voltage to its reference value. This reference is to be provided by an MPPT controller, and represents an estimate of the optimal operating voltage. This intermediate IVR loop allows improved performance and enhanced stability of the MPPT controller, whose design is beyond the scope of this work. Equation (5.1) suggests that the steady-state voltage at Port 2 is dictated by the phase-legs duty-cycle whenever a constant voltage is present at Port 1. The duty-cycle is thus used as the control variable when realizing the IVR loop.

The OVR loop is simply a voltage-mode control loop, closed around the load voltage. Equation (5.2) suggests that the steady-state voltage at the load is dictated by the phase-shift if a constant voltage is present at Port 1. The phase-shift is thus used as the control variable for the OVR loop.

5.5.2. Controller Design

The dynamic response of the system is dependent on a large number of factors. At low frequencies, this response is dominated by the characteristics of the devices connected to its different ports. At higher frequencies, the effect of the connected devices fades, and is shadowed by the dynamic response of the converter itself and its components.

Optimized feedback controller design is normally dictated by the system behavior within the higher frequency range. The gain cross-over frequency is typically chosen in this range, yielding small-signal stability characteristics that are largely independent of the devices external to the converter.

The IVR controller design is dependent on the dynamic response of the input voltage to variation of the duty-cycle of the phase-legs. For the S-BI-PS-FB with a constant battery voltage at Port 1, this is given by the transfer function:

$$\frac{v_2(s)}{d(s)} = \frac{V_1}{1 + s \cdot L_{bst} / r_2 + s^2 \cdot L_{bst} \cdot C_2} \tag{5.43}$$

where L_{bst} is the parallel combination of the boost inductor values, C_2 is the value of the capacitor at Port 2, and r_2 is the incremental resistance of the device connected at that port.

It is interesting that this transfer function is typical of a buck converter operating in CCM. In fact, this buck converter is simply the bi-phase boost converter at the input, observed in the reverse direction. The controller design thus follows the typical design procedures of a voltage-mode buck.

Similarly, the OVR controller design is dependent on the dynamic response of the output voltage to variation of the phase-shift. For the S-BI-PS-FB with a constant battery voltage at Port 1, and assuming CCM operation, this can be described by:

$$\frac{v_o(s)}{\phi(s)} = \frac{n \cdot V_1}{1 + s \cdot L_o / r_o + s^2 \cdot L_o \cdot C_o} \tag{5.44}$$

where L_o is the value of the output filter inductor, C_o is the value of the output filter capacitance, and r_o is the incremental load resistance.

This transfer function is, again, typical of a buck-derived topology. The OVR controller can be designed accordingly.

5.6. Experimental Verification

In order to demonstrate the operation of the proposed topologies and verify the results of the comparative analysis, an experimental test-bed was built and is shown in Figure 52. This test-bed was specifically designed to be easily reconfigured in order to test different converter configurations. It is comprised of removable/replaceable chopper FETs, rectifier diodes, inductors, and a transformer. These converter components were sized to handle 1kW of power, with 90V, 45V, and 175V nominal at Port 1, Port 2, and the Load Port, respectively. According to the converter topology under test, components were selected from those in Table 1.

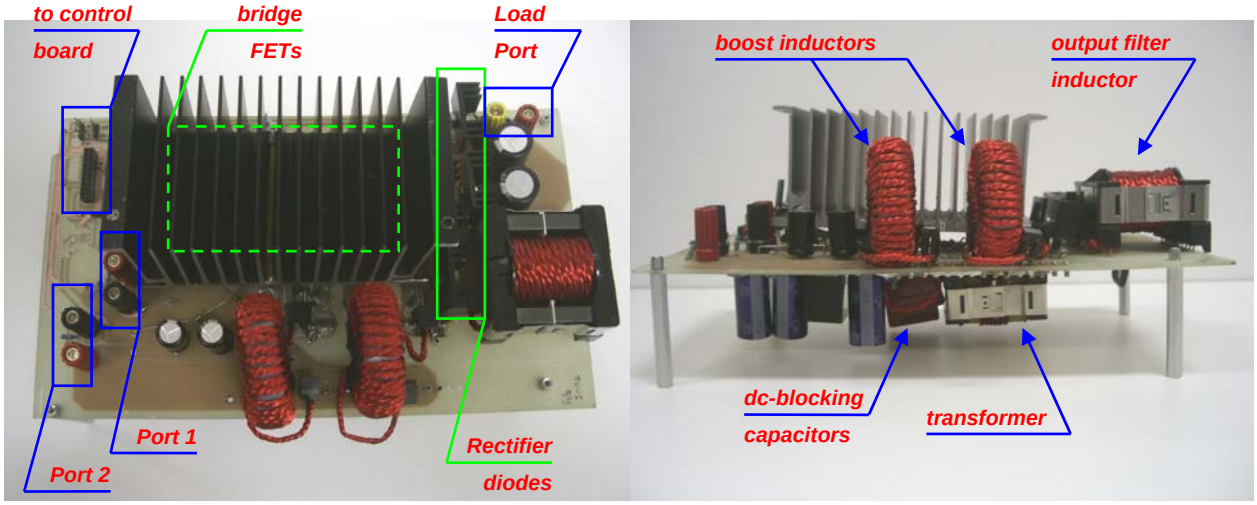


Figure 52 Experimental test-bed

Table 1 Components used in the converters tested

Component/Description	Model no./Construction
Chopper FETs	IRFP90N20D, r_{ds}^{on} = 23mΩ
Rectifier diodes	MSR860
Boost inductors	117μH each
Transformer 1 (T1)	17:44 wound on ETD49 core, not gapped
Transformer 2 (T2)	15:44 wound on ETD49 core, air-gapped
Dc-blocking capacitor	Ceramic 30μF capacitors
Output filter inductor	370μH

The proposed converter topologies require customized switching schemes. The switching patterns were thus generated using a digital board based on Texas Instrument's TMS320F2812 controller chip. Employing a carefully designed timing scheme, the event-manager modules within this chip were programmed to generate two pairs of complementary PWM signals. The duty-cycle of each pair, and the relative phase-shift between them, were subject to software

control. The switching frequency used was 50kHz, and dead-time intervals of 200ns were built into the PWM sequences.

5.6.1. Switching and ZVS Waveforms

5.6.1.1 The Symmetric Case

Figure 53 shows the switching waveforms of the S-BI-PS-FB converter. The test was performed using two of the boost inductors for the boost section and a transformer (T2) for the PS-FB section. The waveforms were captured while a 90V constant voltage source was connected to Port 1; Port2 was operated at 40V and supplied 6A, and the Load Port voltage was regulated to 175V with a 480W resistive load applied.

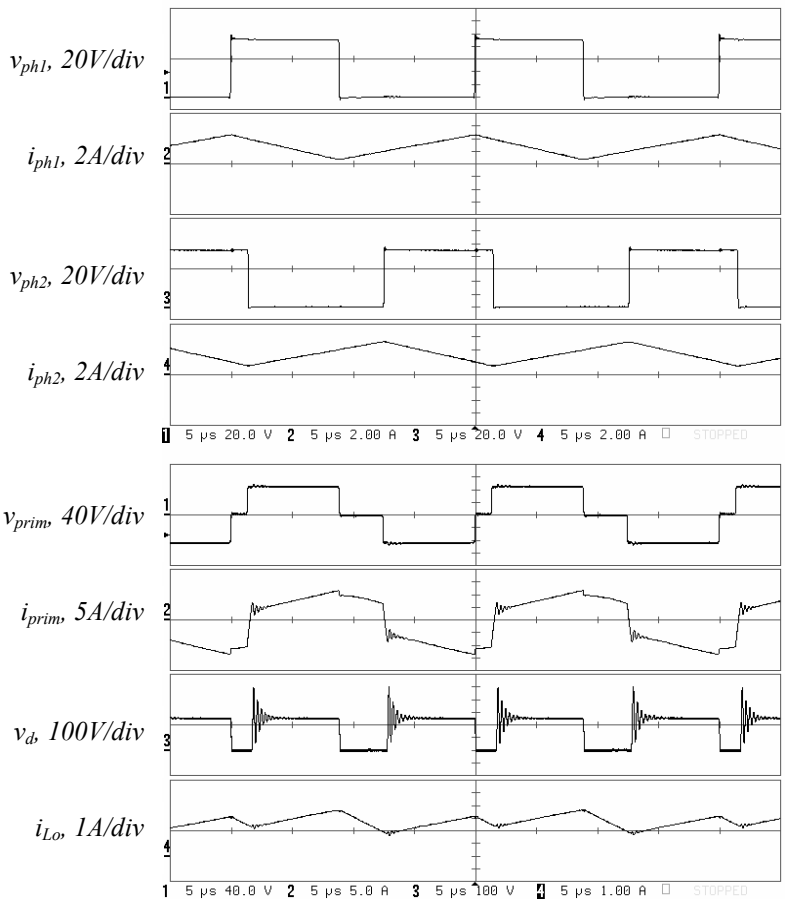


Figure 53 Switching waveforms of the S-BI-PS-FB converter

The boost inductor waveforms and the phase-node voltage waveforms match those of a bi-phase boost converter. The transformer voltage and current, rectified voltage at the secondary, and the filter inductor current, are all similar to those of a PS-FB converter. The main difference is that the two power delivery intervals within a switching cycle are not evenly-spaced, while the two free-wheeling intervals have different durations.

Note that the currents of the boost inductors and transformer primary winding are suitable to cause ZVS of all four chopper FETs. Figure 54 shows the close-ups at the switching instants. Note how the phase-node voltage completes its transition before each of the switches is gated on.

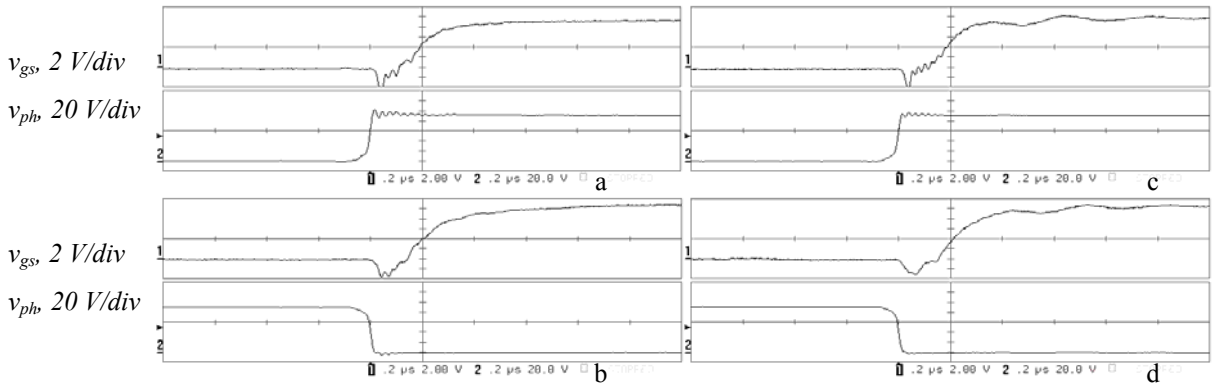


Figure 54 ZVS waveforms of the S-BI-PS-FB converter

5.6.1.2 The Asymmetric Case

In order to test the A-BI-PS-FB converter, both boost inductors were paralleled to form one inductor capable of handling the full boost current. This was connected to the phase-node of the lagging leg. The waveforms were again captured with transformer (T2) with the same operating conditions used to test the S-BI-PS-FB. These are shown in Figure 55.

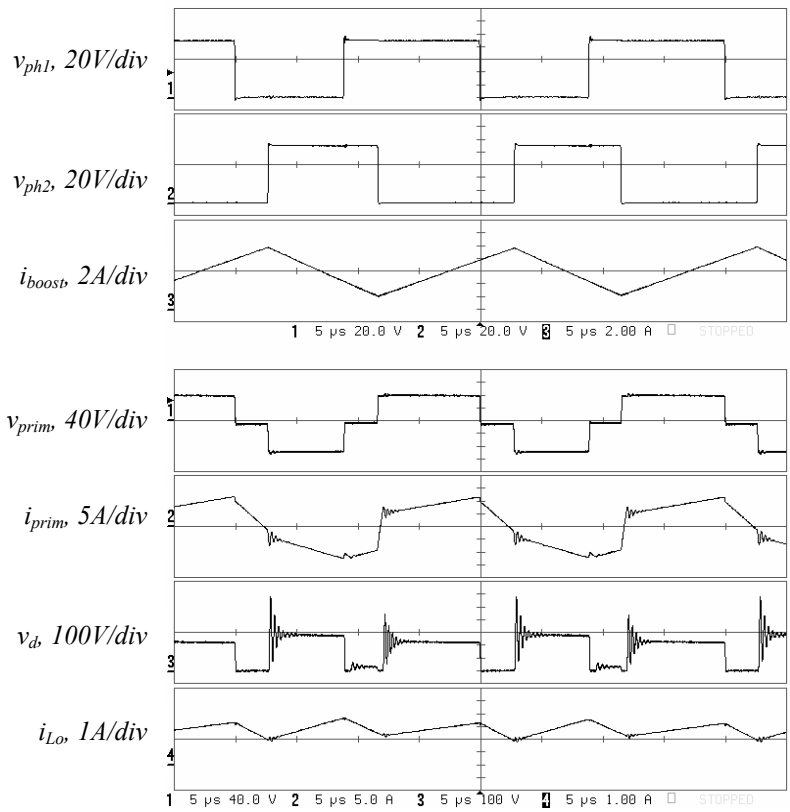


Figure 55 Switching waveforms of the A-BI-PS-FB converter

The boost inductor and lagging phase-node voltage waveforms resemble those of a traditional synchronous boost converter. The leading phase-node voltage has a duty-cycle complementary to that of the boost. The transformer voltage and current, rectified voltage at the secondary, and the filter inductor current, are all similar to those of a PS-FB converter. The main difference is that the two power delivery intervals within a switching cycle have different durations, and the two "free-wheeling" periods are not evenly spaced.

The currents of the boost inductor and transformer primary winding are again suitable to cause ZVS of all four chopper FETs. Figure 56 shows the close-ups at the switching instants. The phase-node voltage completes its transition before the corresponding FET is gated on.

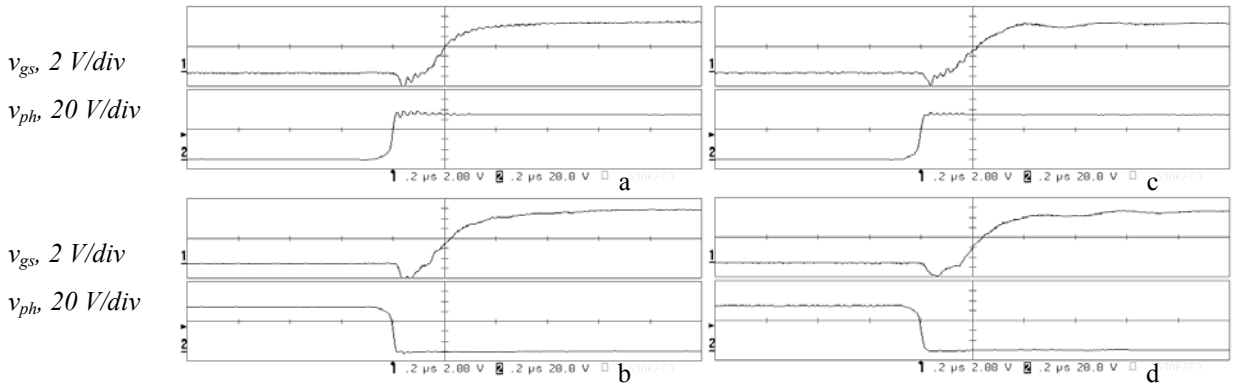


Figure 56 ZVS waveforms of the A-BI-PS-FB converter

5.6.2. Experimental Efficiency Comparison

Experimental efficiency measurements were obtained in order to demonstrate the savings that the proposed topologies promise. Each of the three design alternatives, the two proposed BI-PS-FBs and the cascaded system, comprises two sections: the boost and PS-FB sections. The first step was to investigate the efficiency profiles of these two basic topologies.

The efficiency profiles of two different boost configurations are shown in Figure 57. These correspond to operation from a 45V source at Port 2 (boost input) and 90V nominal at Port 1. The first curve represents a uni-phase boost constructed by connecting both boost inductors in parallel to a single phase-leg, while the second is a bi-phase boost in which each of the two boost inductors is connected to a separate phase-leg. The second has an efficiency edge over the first mainly due to the utilization of four FETs, reducing the conduction loss it incurs.

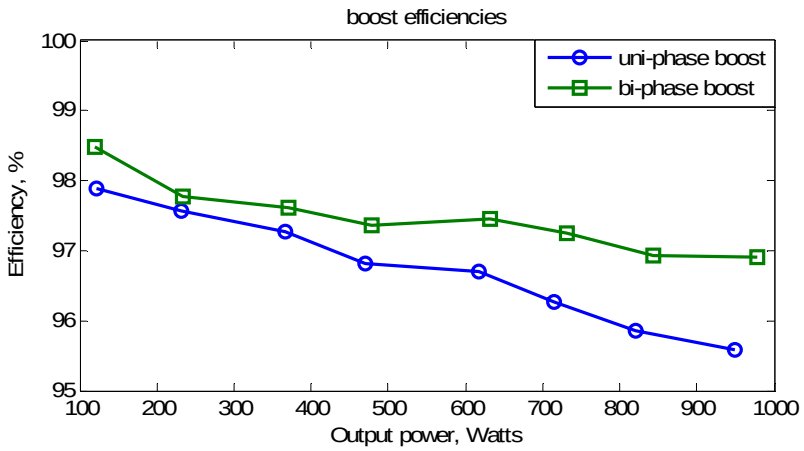


Figure 57 Efficiency comparison of uni- and bi-phase boost converters

Figure 58 shows the efficiency plots of a PS-FB converter using the two transformers in Table 1. The measurements were taken with a 90V source connected at Port 1 (PS-FB input) while the load was regulated to a nominal 175V. The utilization of transformer T1 corresponds to a conventional design where the phase-leg duty-cycle is strictly equal to 50%, with its turns' ratio sized to provide enough margin for proper load regulation. Transformer T2 has a higher turns' ratio, and is adopted for use with the integrated topologies with a boost voltage swing ratio greater than unity. T2 utilizes the same core as T1, but that core is air-gapped in order to allow it to handle the magnetizing current associated with these topologies. As expected, the utilization of T2 slightly decreases the efficiency of the PS-FB section due to increased turns' ratio and the gapping of the core.

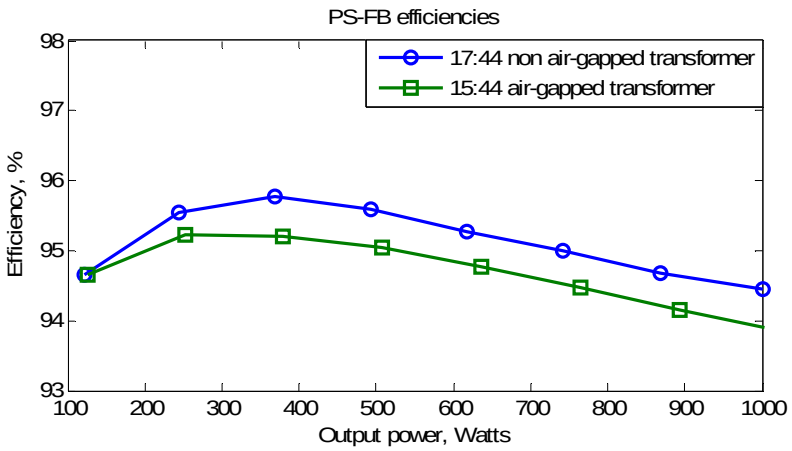


Figure 58 Efficiency comparison of PS-FB converters using transformers T1 and T2

Next, consider an efficiency comparison of the proposed BI-PS-FB topologies to the conventional cascaded approach. As a benchmark, the efficiency is tested when a 45V (nominal) source is connected at Port 2, while leaving Port 1 open, at 90V, and regulating the load voltage to 175V. This test combines the effects of both sections of the converter: the boost and PS-FB sections.

Figure 59 compares the efficiency of the S-BI-PS-FB to the conventional system. The first and second curves represent the efficiency of the cascaded system utilizing uni-phase and bi-phase synchronous boost converters, respectively. The second curve utilizes a larger total silicon area (eight FETs as opposed to six FETs), and thus cuts down on the conduction losses.

The third curve represents the S-BI-PS-FB utilizing transformer T1, where the boost and PS-FB sections are integrated into the same bridge, utilizing only four FETs of the same original ratings. In spite of the reduction of available silicon area, the efficiency is increased, as predicted by the analysis. This efficiency edge is largely attributed to the elimination of turn-on losses of the boost converter. Due to the utilization of transformer T1, the same used in the conventional system, this comparison is valid for the case when Port 2 voltage swing ratio, r, is confined to

unity. Replacing the transformer T1 with T2 increases the value of r to 1.26. A slight drop in efficiency results, but the efficiency of the integrated converter is maintained higher than the best-case cascaded approach. This demonstrates the ability of the S-BI-PS-FB to deliver combined savings in power loss and power FETs for low values of the voltage swing ratio, r.

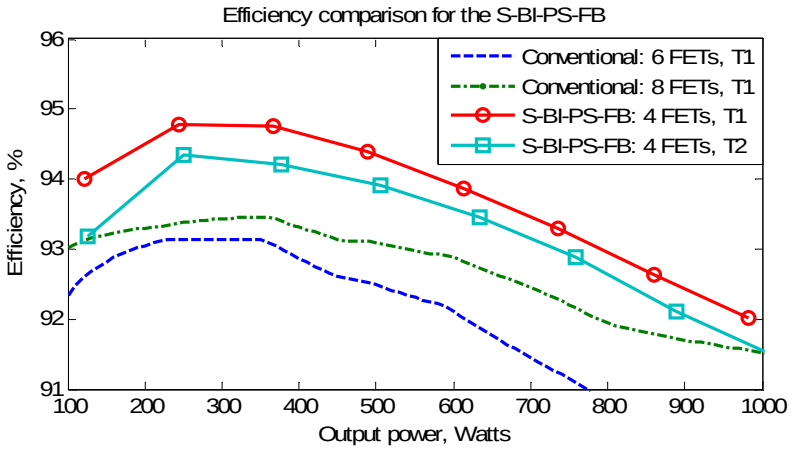


Figure 59 Efficiency comparison of the S-BI-PS-FB converter to the conventional cascaded system

As indicated by the theoretical discussion of Section 5.4, the A-BI-PS-FB becomes a more effective solution for larger values of r. With transformer T2, the A-BI-PS-FB can achieve a voltage swing ratio, r, of 2.044. The corresponding efficiency curve is shown along with those of the conventional system in Figure 60. Utilizing four FETs, the A-BI-PS-FB is slightly more efficient than a conventional cascaded system with a uni-phase boost (six FETs). A conventional system, however, utilizing a bi-phase boost is slightly more efficient, at the cost of doubling the number of FETs used with the same ratings used in the integrated topology.

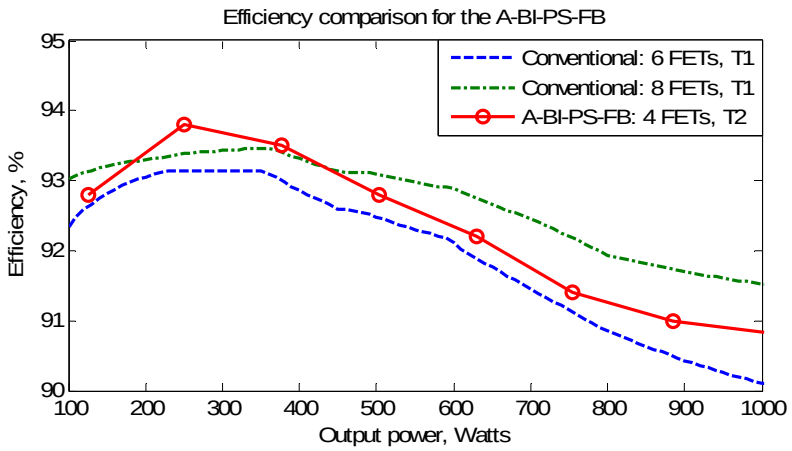


Figure 60 Efficiency comparison of the A-BI-PS-FB converter to the conventional cascaded system

5.6.3. Controller Response

The feedback control structure described earlier was constructed around an S-BI-PS-FB converter prototype with an 11:44 transformer. The on-chip ADC of the DSP was set up to sample the input and output voltage measurements. The two feedback controllers, IVR and OVR, were implemented in software, and provided duty-cycle and phase-shift values to the event-manager module, producing the PWM signals.

Port 1 was connected to a constant 90V source/load combination. Port 2 was connected to a solar array simulator programmed for 60V at open circuit, 12A at short circuit, and 9A at 50V. Resistors were used as the converter load.

A dc value with a superimposed 50Hz triangular wave was provided as the reference to the IVR controller, simulating the output of an MPPT block. The OVR controller was setup to regulate the load voltage to 175V. Figure 61 shows the system response to a load transient from

194Ω to 65Ω and back. Upon a load transient, the OVR controller quickly recovers regulation, while the IVR loop is virtually unaffected.

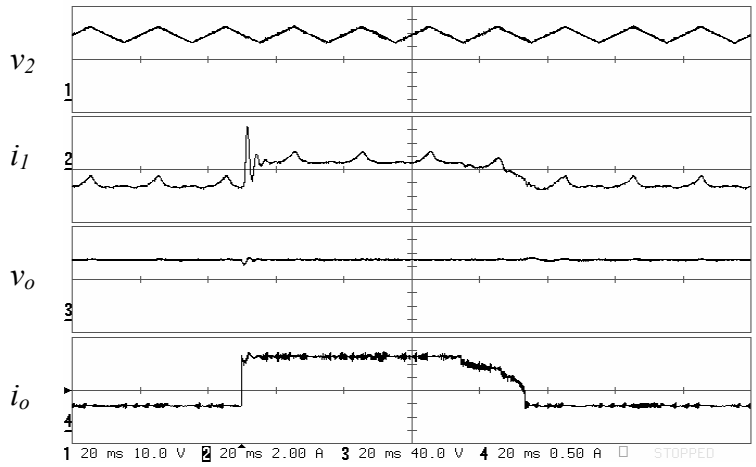


Figure 61 Experimental response of the close-loop system to a load transient

The waveforms demonstrate the ability of the converter to independently regulate the voltages at Port 2 and the Load Port. The current of Port 1 changes in response to variations in the operating conditions at the other two ports. Its current seamlessly changes polarity while it preserves the power balance in the system.

CHAPTER 6: IMPROVED DIGITAL CONTROLLER DESIGN

This work is an effort to develop a systematic digital controller design method that appeals to practicing engineers [51]. A direct-digital compensator design method is proposed where digital compensation tools are analyzed in the familiar analog frequency domain. The implementation aspect is addressed by introducing a numbering system that allows better modeling of a fixed-point digital environment. Models and realizations of common feedback loop components are then discussed, and the application of the proposed concepts to a typical design example is outlined. Experimental results for that design example are then presented.

6.1. Direct-Digital Controller Design in the Analog Frequency Domain

A digitally-controlled power converter is a mixed signal system that contains both continuous-time and discrete-time signals. Dynamic models of the power train, associated sensors, and filters, are traditionally available in the continuous-time domain. These are often linearized and expressed as transfer functions in the s-domain. Digital controllers naturally host discrete-time processes typically expressed as difference equations in the time domain, or as transfer functions in the z-domain. Models of components that interface the controller to the plant often include mixed transfer functions, such as that of a ZOH.

The effect of discrete-time and mixed blocks can be monitored in the analog frequency domain by utilizing the relation of a unit time delay, z^{-1}, to the complex analog frequency, s, given by:

$$z^{-1} = e^{-sT} = e^{-j2\pi \cdot f \cdot T} \tag{6.1}$$

where T is the duration of the sampling period, f is the signal frequency.

In contrast to Euler, trapezoidal, and matched impulse response rules, the relation in Equation (6.1) is exact and is valid throughout the frequency domain. It can be used to accurately monitor the effects of ZOHs, computational time delays, and discrete-time transfer functions on the frequency response of the closed-loop. Figure 62 shows the frequency response plots for common loop components.

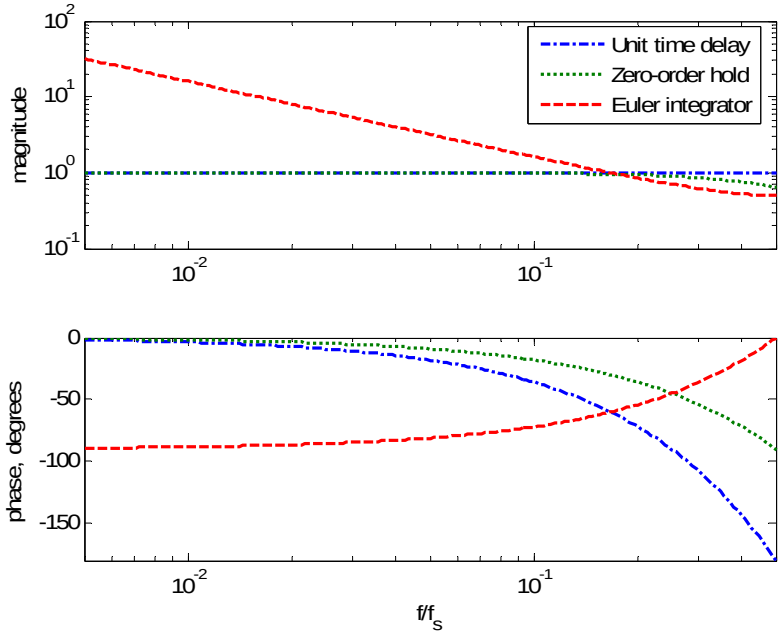


Figure 62 Frequency response of common feedback loop components

Digital control design can proceed by evaluating the frequency responses of all loop components in the analog frequency domain, and combining them either graphically or numerically into familiar Bode plot format. Indigenous digital tools of zeros and poles can then be selected and added to loop in order to tailor its response to the desired form. This aims at achieving the desired dc-gain and gain/phase margins in a routine that closely resembles that of a traditional analog controller design.

6.1.1. Digital Zero/Pole Families

A large variety of digital zero and pole transfer function formats can be utilized to customize the frequency response of the closed loop. Analogous to first-order analog zeros, first-order digital zeros can be utilized to produce a phase-boost of up to 90 degrees. These zeros are formatted as:

$$H_{Zero}(z) = 1 - \left(1 - 1/a\right) \cdot z^{-1} \tag{6.2}$$

where a is a constant larger than unity. Higher values of a correspond to zeros at lower analog frequencies. Figure 63 shows the frequency responses of a set of zeros of this family.

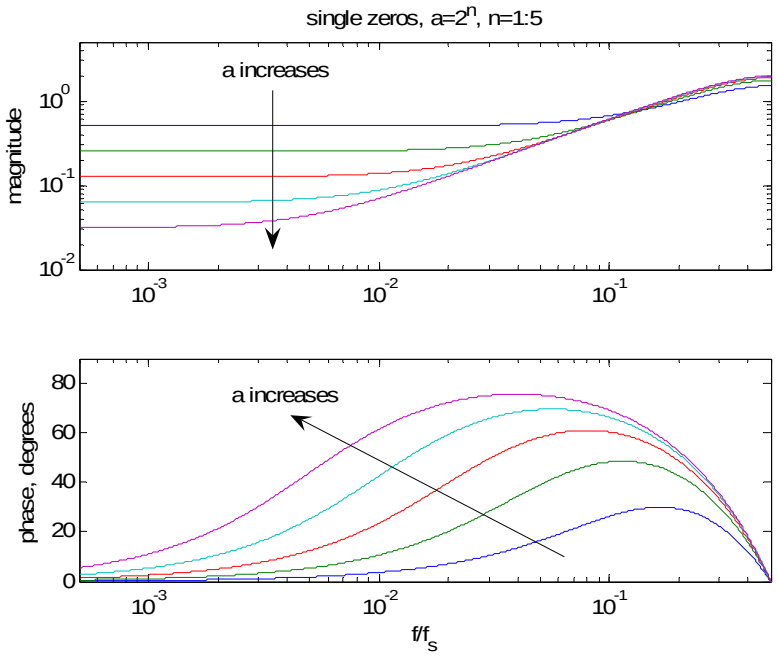


Figure 63 Frequency response of first order digital zeros

Digital control also offers complex conjugate zero pairs as a tool for inducing a sharp phase boost in the loop response. These families of zero pairs are capable of producing a sharp phase boost of 180 degrees. This has been found to be particularly powerful for compensating voltage-mode buck converters with high-Q output filters. While such zeros are theoretically achievable with analog compensators, they are generally avoided due to implementation complexity. In the digital domain, they can be simply added by choosing the proper difference equations. "Hard" complex conjugate zero pairs can be introduced in the format:

$$H_{ZeroPair}^{Hard}(z) = 1 - \left(2 - 1/b\right) \cdot z^{-1} + z^{-2} \tag{6.3}$$

where b is a constant larger than unity. These zero pairs result in a step of 180 degrees in the closed loop phase at a corner frequency dependent on b. Higher values of b result in lower corner frequencies, as shown in Figure 64.

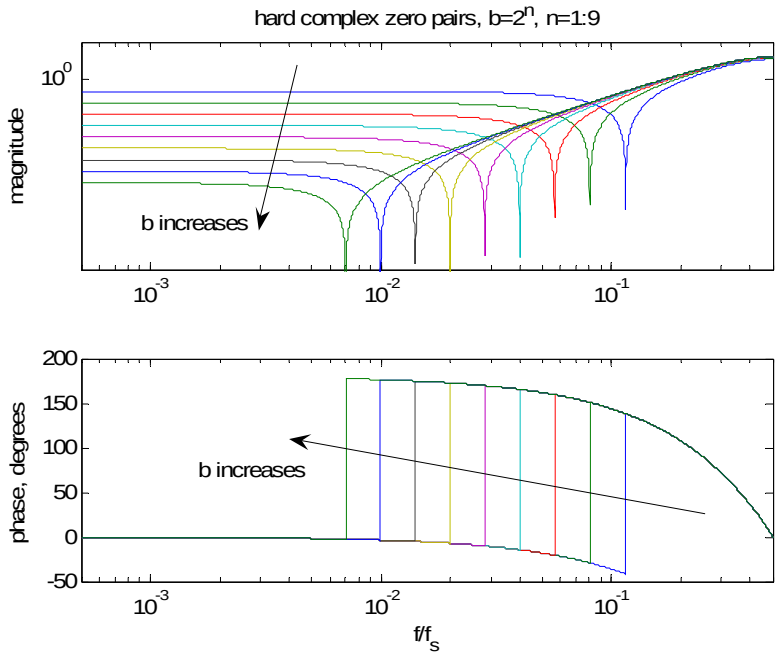


Figure 64 Frequency response of "hard" complex conjugate zero pairs

Hard zero pairs are a special case of a more general family that can induce a softer phase transition. “Soft” complex conjugate zero pairs have the form:

$$H_{ZeroPair}^{Soft}(z) = 1 - \left(2 - 1/b\right) \cdot z^{-1} + \left(1 - 1/c\right) \cdot z^{-2} \tag{6.4}$$

where $c > b > 1$. Figure 65 shows the frequency response of set of these pairs for a single value of b, and different values of c. As can be observed, a soft zero pair approaches a hard zero pair for large values of c.

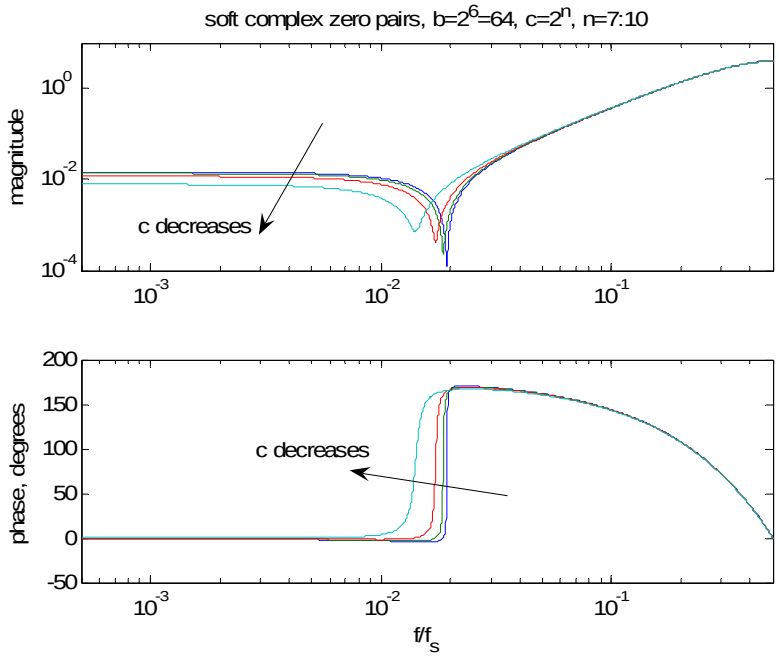


Figure 65 Frequency response of a family of "soft" complex conjugate zero pairs

It is important to note that the member functions of all three digital zero families fail to produce a significant phase boost at frequencies approaching one half of the sampling frequency. In fact, phase crosses zero at that point. This is an inherent limitation to linear digital controller design, irrespective of the design methodology, resulting from the operation in the discrete time domain. Practically, the gain cross-over frequency is often placed below the affected frequency range due to the well-known limitations in average modeling, even for analog-controlled designs.

Families of digital poles can also be used to manipulate the closed-loop frequency response. The transfer functions of such poles are the reciprocals of corresponding zeros, and they have an opposite effect on the frequency response.

When choosing the poles and zeros, it is advantageous to make the constants a, b, and c powers of 2. This allows the implementation of the block with no multiplications, as will be discussed in a later section.

6.1.2. Integrators

Integrators are typically used to ensure infinite dc loop-gain, in order to achieve zero steady-state error. Different integrators can be used, the simplest being an Euler integrator described by the transfer function:

$$H_{Integrator}^{Euler}(z) = \frac{1}{1 - z^{-1}} \tag{6.5}$$

The digital controller design process is clarified using a design example in Section 6.4.

6.2. Number Representation and Arithmetic in a Fixed-Point Environment

Components integrated to the digital controller chip produce or consume digitally stored values. Modeling them accurately thus requires a concise formulation of the numbering and referencing system used to store and process discrete values.

Values are normally stored as digital integer values in a fixed-point digital processor environment. Standard register sizes are 8, 16, or 32 bits. Standard variable definitions are:

- `int`, for integer: 16 bits, signed by default. Range: $[-2^{15}, 2^{15}-1]$
- `unsigned int`, for unsigned integer: 16 bits, always assumed positive. Range: $[0, 2^{16}-1]$
- `long`, for long integer: 32 bits, signed by default. Range: $[-2^{31}, 2^{31}-1]$

The direct interpretation of these numbers to their integer values does not provide an intuitive sense of the values they represent or the limitations imposed on them. This complicates the models of the different components and the implementation of difference equations that realize filters, integrators, and compensators.

6.2.1. Referenced Interpretation of Binary Values

Normalizing digitally stored numbers provides a powerful tool for interpreting them. It simplifies controller design, optimization, and documentation. Proposed here is the assignment of a virtual "binary" point at a pre-defined location within the bit string. This point splits the number into two sections: the most significant bits (MSBs) are separately interpreted as an integer, whether signed or unsigned, while the least significant bits (LSBs) are interpreted as a fractional number less than unity. This allows the treatment of non-integers without using any costly floating-point operations. The number of LSBs that represent the fractional portion is called the reference of the variable. The value is said to be stored in "rM" format, whether signed or unsigned. This is illustrated in Figure 66.

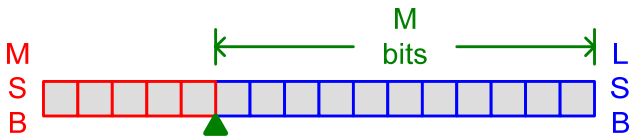


Figure 66 Number representation in rM format

The effective logical value, x, of a number interpreted according to rM format is related to the physical binary integer value, k, by:

$$x = \frac{k}{2^M} \tag{6.6}$$

whether k is signed or unsigned.

Accordingly, the value storage range of a register of length N bits storing a number in rM format is $\left[0, 2^{N-M} - 2^{-M}\right]$, or simply $[0, 2^{N-M})$, for unsigned numbers. For signed numbers, that range becomes $\left[-2^{N-M-1}, 2^{N-M-1} - 2^{-M}\right]$ or simply $[-2^{N-M-1}, 2^{N-M-1})$.

For example, a variable defined as an “integer” and used with r15 format accepts values within [-1.0, 1.0). When used with r14 format, it accepts values within [-2.0, 2.0). A variable defined as an “unsigned integer” and used with r15 format accepts values within [0, 2.0). It accepts values with [0, 4.0) if used within r14 format.

6.2.2. Referencing Rules and Guidelines

The reference assigned to the value can be any integer, whether negative, zero, or positive. It can be lower, equal, or higher than the physical length of the register. That simply affects the range and resolution of the value stored.

The assignment of a reference to the number strictly serves as a design tool. This is not reported to the code compiler or processor. The programmer is responsible for maintaining compatible assignments throughout the code and enforcing the rules it imposes on arithmetic operations. Basic rules associated with this system are:

1. Reference translation: binary shift operations can be used to translate a value from one reference to the other. This is governed by the following relations:
    a. Left shift, `<<m`: reference is increased by m bits,
    b. Right shift, `>>m`: reference is decreased by m bits.
2. Gain/attenuation of a power of 2: binary shift operations can be used to produce a gain or attenuation according to the following relations:
    a. Left shift, `<<m`: gain of 2^m,
    b. Right shift, `>>m`: attenuation by 2^m.
3. Gain/attenuation combined with reference translation: a gain of a power of 2 can be integrated with a reference translation in a single instruction. This is governed by:

a. Left shift, `<<m`, with rI for the input and rO for the output signals produces an effective gain of 2^{I-O+m},

b. Right shift, `>>m`: with rI for the input and rO for the output signals produces an effective gain of 2^{I-O-m},

   In fact, if a value formatted to rI is simply used as an rO value, an inherent gain of 2^{I-O} would result.

4. Addition/subtraction: operands need to be formatted according to a common reference. The resulting value is of that same reference.
5. Multiplication/division: the reference of the product of two values is equal to the sum of their references. The reference of a quotient is equal to the reference of the dividend less that of the divider.
6. Constants: when using constants for direct assignment or comparison, the raw integer value is used. For example, the statements:

```
unsigned int x=0x4000;   // r15
unsigned int x=16384;    // r15
```

   are both equivalent. They declare the unsigned variable, `x`, and assign it the value of 0.5, if assumed to be in r15 format.

It is the responsibility of the programmer to ensure that all variables are assigned a register length and a reference value that provide a sufficient value range and an adequate resolution. It is notable that the reference assignment solution is not unique per design. Depending on the problem at hand, several reference assignments might deliver close or equivalent results. This assignment process is clarified later using the design example.

6.3. Modeling and Implementation of Digital Controller Functions

In the light of the discussion above, the components common in a digital controller environment are analyzed.

6.3.1. Analog-to-Digital Converter Model

A linear ADC can simply be modeled as an ideal sampler with associated gain. The result of the ADC conversion is typically stored in a constant-length register. A simple approach is to interpret the maximum output of the ADC as unity (or approaching it). The result register is assumed to be of the corresponding reference. The gain of the ADC then becomes:

$$K_{adc} = \frac{LogicalValueRange}{PhysicalValueRange} \tag{6.7}$$

For example, consider a 12-bit ADC that measures physical analog voltages of [0.0, 3.0V), whose results are stored in an unsigned 16-bit registers in left-justified format. The analog value range of [0.0, 3.0V) thus corresponds to [0.0, 1.0) stored in an r16-formatted 16-bit register. Its gain is then given by:

$$K_{adc} = \frac{(1.0 - 0.0)(unitless)}{(3.0 - 0.0)(Volts)} = 0.333V^{-1}$$

6.3.2. Pulse-Width Modulator Model

Consider a digital pulse width modulator (DPWM) employing a constant frequency timer, compared with a variable value, representing the commanded duty-cycle. The timer period is determined by the number of clock cycles within a switching period, and is given by:

$$TimerPeriod = \frac{f_{PWMclock}}{f_s} \tag{6.8}$$

where $f_{PWMclock}$ is the clock frequency of the PWM timer, and f_s is the switching frequency of the converter.

The duty-cycle corresponding to the compare value in the compare register is given by:

$$d = \frac{CompareValue}{TimerPeriod} \tag{6.9}$$

It is convenient to regard the value in the compare register as being formatted relative to a reference that maps the full duty-cycle range to logical compare register values lower than unity. The suggested format is rM, where $M = ceil\left(\log_2 TimerPeriod\right)$. The PWM block gain then becomes:

$$K_{pwm} = \frac{2^M}{TimerPeriod} \tag{6.10}$$

The minimum increment in the duty-cycle achievable with such a modulator is given by:

$$\Delta D_{\min} = \frac{1}{TimerPeriod} \tag{6.11}$$

6.3.3. Digital-to-Analog Converter Models

Digital-to-analog converters (DACs) are commonly used when the digital controller acts as a supervisor to external analog controllers, providing analog references and/or limit levels. DACs are also useful for monitoring internal controller states in the digital controller for debugging purposes. Two types of DACs can be used:

6.3.3.1 Dedicated DAC

Dedicated DAC hardware can be used. A referenced format can be assumed for the DAC input that translates the maximum input to the DAC as unity. For example, a 12-bit DAC receiving a 16-bit word with the value bit right-justified is regarded as using the format r12. If this same DAC received left-justified values, it would be regarded as using the format r16. In both cases the gain of the DAC would be:

$$K_{dac} = \frac{PhysicalValueRange}{LogicalValueRange} \tag{6.12}$$

For example, a DAC referenced in that way, with the range [0.0, 3.3) exhibits the gain:

$$K_{dac} = \frac{(3.3 - 0.0)(Volts)}{(1.0 - 0.0)(unitless)} = 3.3V$$

6.3.3.2 PWM DAC

A useful technique to get a simple, but relatively slow, DAC is simply the filtering of a PWM output through a simple RC low-pass filter (LPF). This comes in very handy for monitoring and debugging real-time control systems.

The output of such a DAC is equal to the duty-cycle of the PWM, scaled by the rail voltage, times the gain of the LPF. Receiving rM formatted values and utilizing a simple RC filter with time constant, τ_{RC}, such a DAC can thus be modeled as:

$$H_{PWM\_DAC}(s) = \frac{2^M}{TimerPeriod} \cdot \frac{V_{rail}}{\tau_{RC} \cdot s + 1} \tag{6.13}$$

where V_{rail} is the upper rail voltage of the PWM signal, while the lower rail is assumed ground.

6.3.4. Delay and Zero-Order Hold Models

Some processing time is needed for each sampling cycle. Once the results are ready, they are held and released for use at the next sampling period. This results in an effective delay of one or more time delay units, each equal to the duration of a sampling period, T. The frequency transfer function of the delay is given by:

$$H_{delay}(s) = e^{-s \cdot m \cdot T_s} = z^{-m} \tag{6.14}$$

where s is the complex frequency in the analog domain, and m is the number of sampling period delays.

It is important to note that, in the general sense, the switching period is not necessarily equal to the controller sampling period. However, a common scenario is when they are equal, and the control variable is utilized by the actuator one period after its corresponding ADC sample is obtained. The delay then reduces to:

$$H_{delay}^{typical}(s) = e^{-s \cdot T} = z^{-1}$$

The discrete-time output of the controller is held and applied to controlled plant for a full sampling period. To account for that, a ZOH transfer function typically accompanies the models of PWMs, DACs, or similar blocks used. The ZOH transfer function is given by:

$$ZOH = \frac{1 - z^{-1}}{s \cdot T} \tag{6.15}$$

6.3.5. Implementation of Compensator Zeros, Poles, and Integrators

Zeros of the forms given in Equations (6.2) and (6.4) are described in the time domain by difference equations of the forms:

$$y(n) = x(n) - \left(1 - 1/a\right) \cdot x(n-1) \tag{6.16}$$

$$y(n) = x(n) - \left(2 - 1/b\right) \cdot x(n-1) + \left(1 - 1/c\right) \cdot x(n-2) \tag{6.17}$$

where $x(n)$ and $y(n)$ are the discrete-time input and output signals of the zero block, respectively. These can be implemented as shown in Figure 67 below.

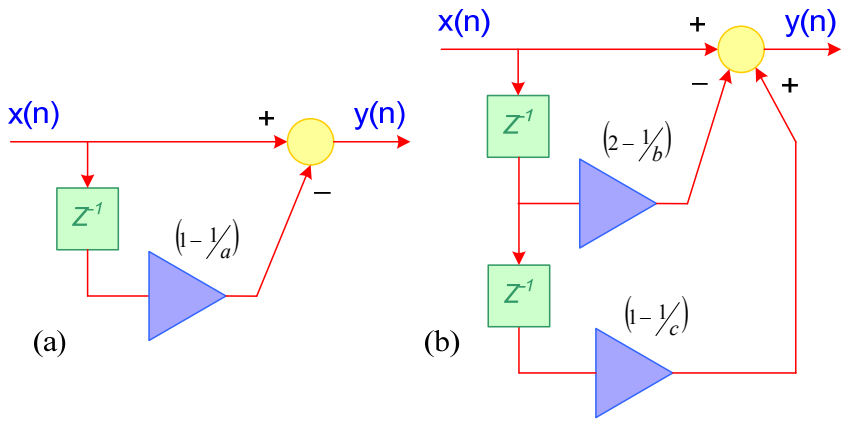


Figure 67 Implementation of digital zeros (a) first order (b) soft complex pairs

Figure 68 shows the implementation of poles reciprocal to such zeros, which are described by the inverse difference equations:

$$y(n) = x(n) + \left(1 - 1/a\right) \cdot y(n-1) \tag{6.18}$$

$$y(n) = x(n) + \left(2 - 1/b\right) \cdot y(n-1) - \left(1 - 1/c\right) \cdot y(n-2) \tag{6.19}$$

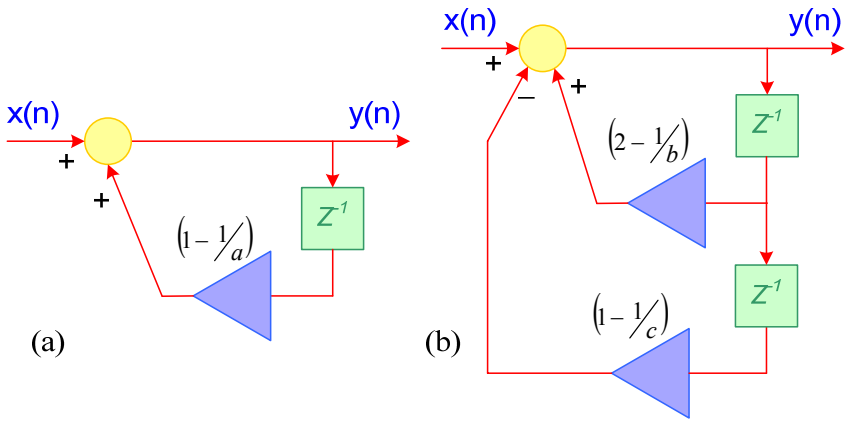


Figure 68 Implementation of digital poles (a) first order (b) soft complex pairs

It is the responsibility of the designer to ensure that all intermediate and output signals are formatted properly to avoid saturation and/or severe loss of signal resolution, as will be clarified using the design example in Section 6.4.

Multiplication can be used to implement the gain blocks, $(1-1/a)$, $(2-1/b)$, and $(1-1/c)$. However, if a, b, and/or c are powers of 2, these gains can be split into two gains, each of which can be implemented using binary bit shifting. The result is multiplier-free controllers that offer great savings in hardware and/or processing time within the digital controller. Moreover, it reduces the risk of zero/pole mis-location due to inaccurate representation of the fractional part of these gains.

An Euler integrator is described in time domain by:

$$y(n) = y(n-1) + x(n) \tag{6.20}$$

It is important to include a limiter function within the integrator structure in order to avoid register overflow. This limiter should not affect the loop operation in steady-state, and it is not considered when studying the small-signal stability characteristics of the loop. Figure 69 shows the implementation of an Euler integrator with a built-in limiter.

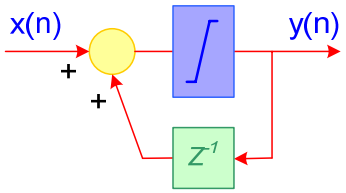


Figure 69 Implementation of a limited Euler integrator

6.4. Design Example: Synchronous Buck Voltage Regulator

In an attempt to clarify the design procedure, an OVR controller is designed for a 200W synchronous buck converter. This system is supplied by a 50V with 0.7Ω output resistance, while the output voltage target is 20V. The load filter inductor is 18µH, the output capacitor is 540µF, the input capacitance is 330 µF, while the switching frequency is 100kHz. The combined parasitic resistance of the inductor and FETs and the equivalent series resistance of the output capacitor were estimated at 50mΩ each. The controller is to be implemented using a control chip with a 12-bit ADC module and timer-based PWM channels clocked at 150MHz.

An overview of the control loop is shown in Figure 70. At the heart of the loop is the controlled plant, the buck power stage. A sensor is attached to the power stage to provide the feedback measurement signal. An ADC is used to read that measurement into the digital controller chip. It is then compared with a pre-defined reference, and the difference is processed through the controller difference equation. The result is held until used by the PWM modulator to create the gating waveforms for the converter switches.

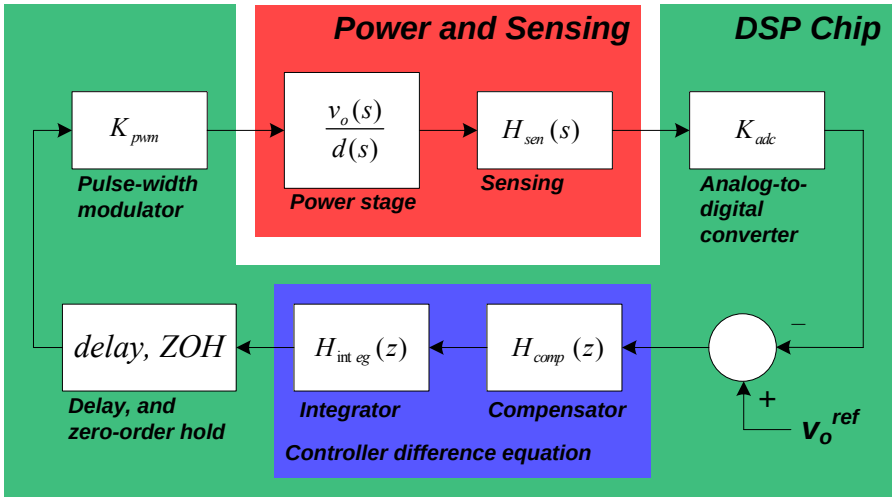


Figure 70 Layout of the closed-loop system

6.4.1. Loop Modeling and Compensator Design

In order to design the compensator, the frequency responses of all other blocks are characterized. The output of the compensator passes through a discrete-time integrator. A simple Euler integrator is chosen, whose transfer function is described by Equation (6.5). The integrator output is delayed to the beginning of the next cycle, passed to the PWM and used to generate the switching waveform. A delay of one cycle and a ZOH are thus added to the loop model. According to Equation (6.8) the PWM timer period is:

$$TimerPeriod = \frac{150MHz}{100kHz} = 1500$$

Assuming an r11 format for the PWM input, its effective gain becomes:

$$K_{pwm} = \frac{2^{11}}{1500} = \frac{2048}{1500} = 1.3653$$

The converter is described by the transfer function relating the controlled variable, the output voltage, to the control variable, the duty-cycle. Conventional average modeling techniques can be used to obtain it. For an idealized buck converter, that yields:

$$\frac{v_o(s)}{d(s)} = \frac{V_{in}}{1 + s \cdot L_o / r_o + s^2 \cdot L_o \cdot C_o}$$

where L_o, C_o, and r_o are the load filter inductor, output capacitor, and incremental resistance of the load. This model was further modified to account for circuit parasitics: inductor ohmic resistance, output capacitor equivalent series resistance, and source output impedance. The resultant transfer function becomes:

$$\frac{v_o(s)}{d(s)} = \frac{\left(V_{in} - D \cdot I_L \cdot Z_{in}\right) \cdot Z_o}{D^2 \cdot Z_{in} + Z_L + Z_o}$$

with:

$$Z_{in} = \frac{r_g}{1 + s \cdot r_g \cdot C_{in}},\ Z_L = s \cdot L_o + r_L, \text{ and } Z_o = \frac{r_o \cdot \left(1 + s \cdot r_{esr} \cdot C_o\right)}{1 + s \cdot \left(r_o + r_{esr}\right) \cdot C_o}$$

where r_g is the output resistance of the source, C_{in} is its capacitance, r_L is the inductor resistance, r_{esr} is the equivalent series resistance of the output capacitor, and r_o is the incremental load resistance.

The output voltage sensor comprises the sensing gain and a first-order RC filter, and is described by:

$$H_{sen}(s) = \frac{K_{sensing}}{1 + \tau_{RC} \cdot s} = \frac{1/20}{1 + (0.6\mu\text{sec}) \cdot s}$$

where τ_{RC} is the time constant of the sensing filter.

Within the digital controller chip, the signal is processed using the ADC. While the ADC used is of 12-bit resolution, it stores its results in left-justified 16-bit result registers. Assuming an r16 format of these registers, and considering the physical range of [0, 3.0V), the ADC gain becomes:

$$K_{adc} = \frac{(1.0 - 0.0)(unitless)}{(3.0 - 0.0)(Volts)} = 0.333V^{-1}$$

The next step is computing and combining the frequency response of all of these blocks: the integrator, computational delay, ZOH, PWM gain, converter power stage, sensing, and ADC gain. In preparation for compensator design, Matlab was used for evaluating and plotting the cascaded frequency response relative to the analog frequency, f, using Equation (6.1) wherever necessary. This "uncompensated" closed-loop frequency response, shown in Figure 71, indicates that the system would be unstable since phase crosses zero degrees while the gain is above zero dB. Adding a "hard" complex zero pair of $b = 256$ produces a phase boost at around 1kHz, just below the natural resonant frequency of the output LC filter. This moves the phase crossover up to 20kHz, and a gain of 32 can then be added to place the gain crossover at 5kHz. The compensator transfer function is thus given by:

$$H_{comp}(z) = 32 \cdot \left[1 - \left(2 - \frac{1}{256} \right) \cdot z^{-1} + z^{-2} \right]$$

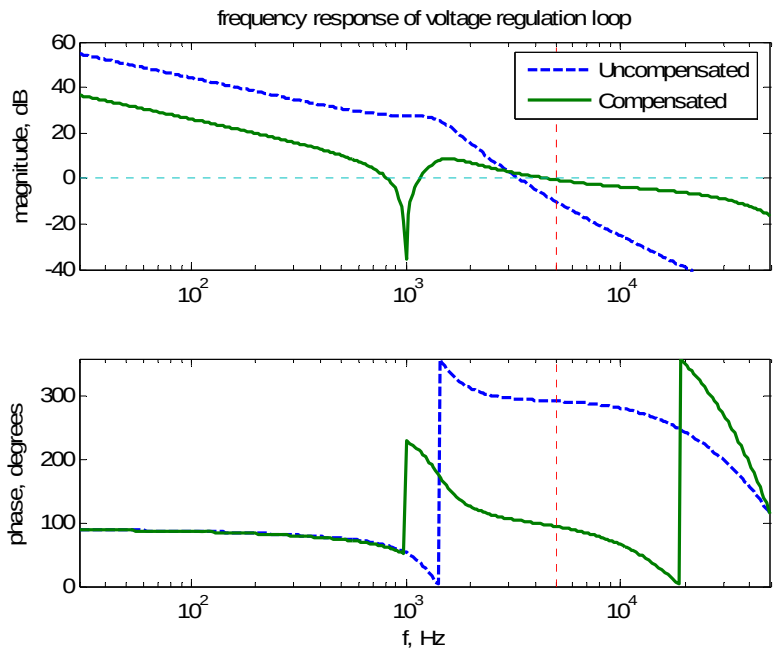


Figure 71 Theoretical closed-loop frequency response for a 2.5Ω load

Time domain simulation of the closed-loop system was conducted in Simulink. The response of the converter to a 2-6A (20-60%) load transient is shown in Figure 72.

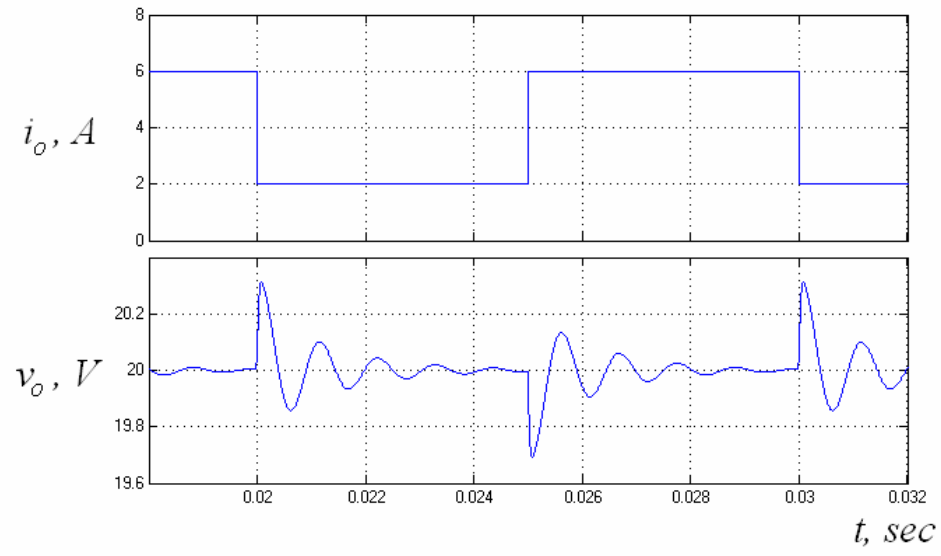


Figure 72 Simulated closed-loop response to a 2-6A load transient

6.4.2. Controller Coding

One suitable layout for controller implementation is shown in Figure 73. The integrator block usually is the only block in the system that exhibits unlimited gain and requires limitation of its internal states. Its decoupling from other system blocks and placement at the end of the chain simplifies the limit calculations and allows better optimization of other blocks. Format translations are done throughout the structure as needed.

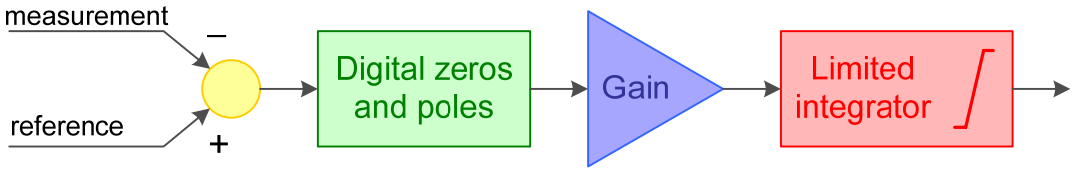


Figure 73 Controller implementation layout

The controller designed for the buck can be implemented as shown in Figure 74. At the front-end, the measurement is subtracted from the reference signal, and the difference is passed to the compensator zero block. A cascade implementation is preferred for the compensator zeros/poles, where each stage realizes one zero/pole, or a pair of complex conjugate zeros/poles. The compensator considered here has one pair of complex conjugate zeros, and requires one stage with two memory blocks (states), u_1 and u_2. The output is then amplified and passed to the integrator. The integrator, per design, is an Euler integrator. A limit function is added within its structure to avoid saturation/overflow of its internal state, u_{int}, and to limit its output to the range acceptable by the PWM module.

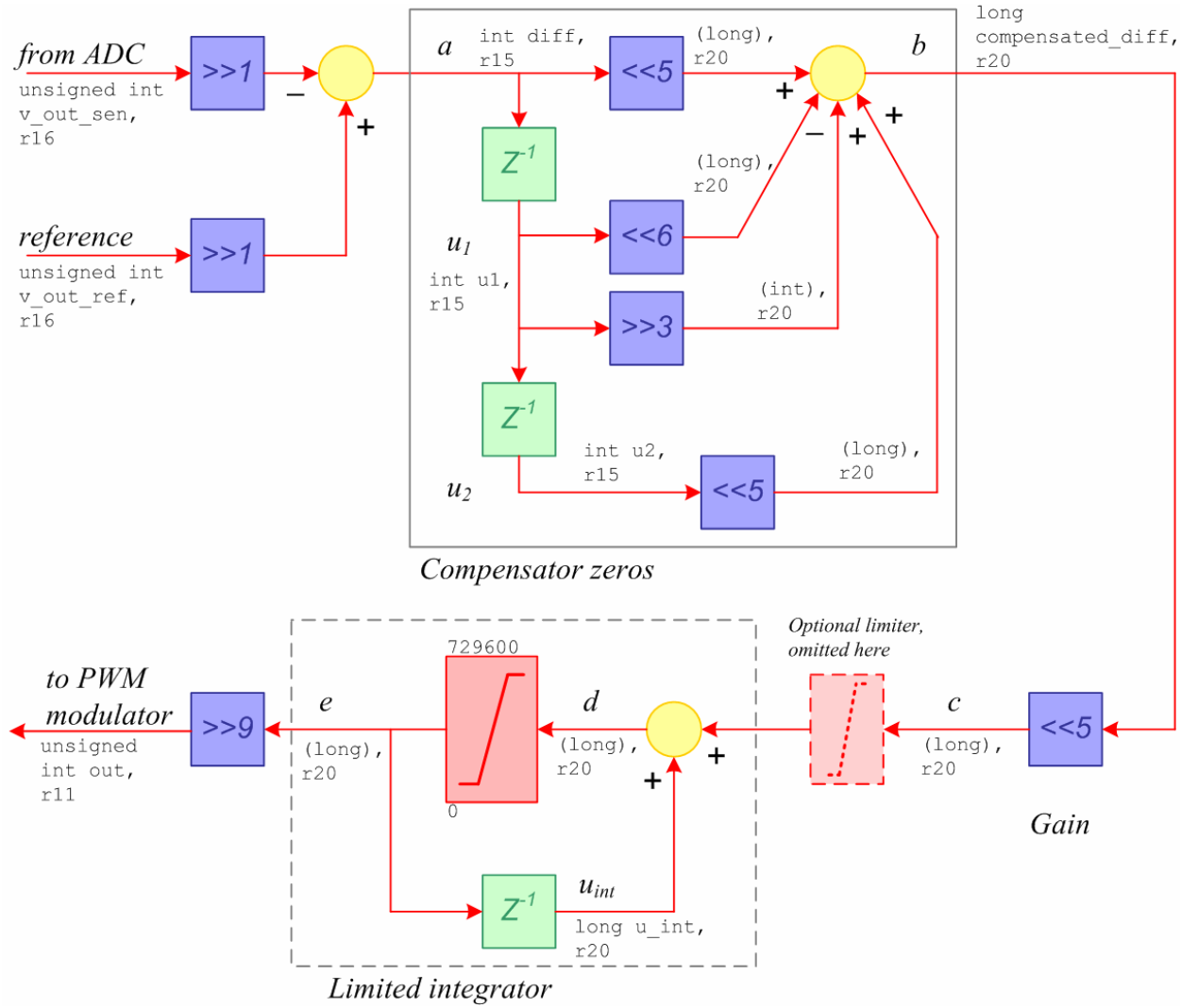


Figure 74 Controller software "blueprint"

According to the worst-case signal amplitude expected at each point and the resolution required, the assignment of formats proceeded as described below.

The output voltage measurement and reference signals are both available in unsigned 16-bit registers, formatted as r16, and each ranging within [0.0, 1.0).

Signal *a* is the difference signal, and ranges within [-1.0, 1.0). If r16 format is adopted, signal *a* would not fit within a 16-bit register. An r15 format was thus chosen for signal *a*. Since the resolution of the measurement signal coming from the ADC is 12 bits, formatting signal *a* in

r15 does not entail any compromise of signal resolution. Reference translations, using bit shifting, can be added before the summer block in order to get the correct format. The shifts were added before the summation in order to avoid saturation in the summer output, which inherits the format of its inputs.

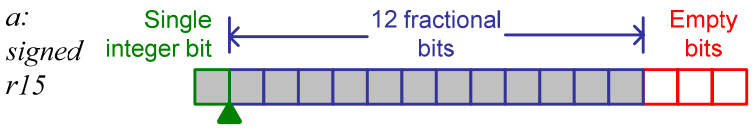


Figure 75 Difference signal in signed r15 format within a 16-bit register

States u_1 and u_2 inherit the format of signal a. They thus require signed integer memory registers. The gain of $\left(2 - 1/256\right)$ is applied to u_1 before feeding it to the summer. In this example, the two parts of the gain, 2 and 2^{-8}, are each implemented independently using bit shifts.

In order to avoid severe loss of accuracy, the gain of 2^{-8} is not implemented using an 8-bit right shift. Instead, a 3-bit shift combined with a reference change from r15 to r20 is adopted. The result register can remain 16 bits long and still accommodate all relevant bits as shown below:

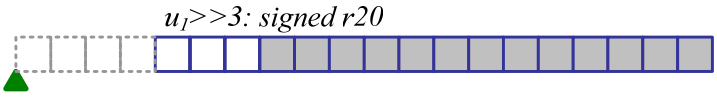


Figure 76 A controller state in signed r20 format within a 16-bit register

To implement the integer gain, 2, and make the reference shift, a 6-bit shift left is required. In order for the result, ranging within [-2.0, 2.0), to fit, a register of at least 22 bits is required. A "long" 32-bit register is used since 22 bits is not a standard length.

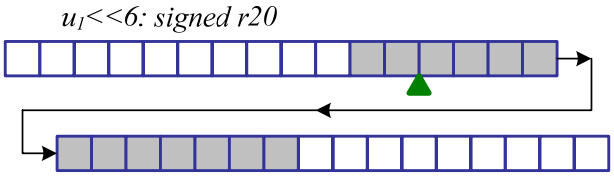


Figure 77 A compensator state in signed r20 format within a 32-bit register

Even though the two gain results are of different register lengths, they can be immediately added because they share a common reference. The result should be stored in a register large enough. It ranges within [-2.0 to 2.0) and will again be stored in a 32-bit register, as "long".

To get signal *b*, this result is added to *a* and *u2*. Signals *a* and u_2 have to be converted to the proper reference, r20. In the worst case, signal *b* ranges within [-4.0, 4.0) and occupies up to 23 bits within a register formatted at r20.

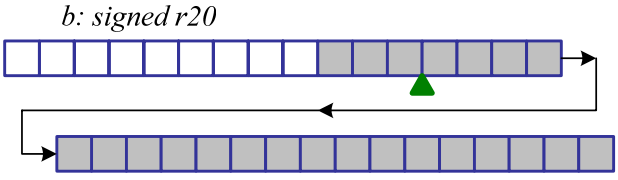


Figure 78 Compensator output in signed r20 format within a 32-bit register

Signal *c* is an amplified version of signal *b*. The gain, 32, can be implemented as 5-bit left shift, keeping the same reference.

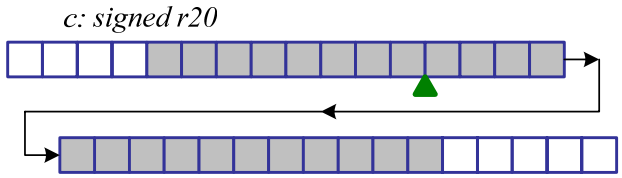


Figure 79 Integrator input in signed r20 format within a 32-bit register

It is notable that in the most general case, signal *c* ranges within [-128.0, 128.0). This vast range represents the worst case scenario. In a typical operating scenario, this signal is expected to be within the range of the integrator state, to which it is directly added. It is thus acceptable to apply an extra limitation function at this stage, effectively limiting the maximum rate of change of the integrator output. This, however, is not done here since all signals happen to fit in their registers without complications.

Signal *c* is then added to the integrator state, u_{int}, to get signal *d*. State u_{int} is confined by the limiter function to the acceptable range at the integrator output. In this example, the range is $\frac{[0.0,1.0)}{K_{pwm}}$, corresponding to output duty-cycles of [0.0 1.0). Signal *d* is thus somewhere within (-129.0, 129.0) and can fit within a 32-bit register formatted in r20.

Signal *e* is the very output of the controller difference equation. As discussed above, it needs to correspond to the allowable range of the control variable. The allowable range of the duty-cycle is [0.0, 1.0), and the corresponding range for signal *e* is:

$$\frac{[0.0,1.0)}{K_{pwm}} = [0.0, {}^{1500}\!/_{2048})$$

The buck converter under consideration uses a boot-strap mechanism to drive the upper N-channel FET. The duty-cycle range is thus further reduced to [0.0, 0.95), with a corresponding $[0.0, {}^{1425}\!/_{2048})$ range for signal *e*. This limitation range needs to be expressed in absolute

integer values for the actual coding in the program. Given r20 formatting of the registers, the range $[0.0, {}^{1425}\!/_{2048})$ translates to:

$$[0.0, {}^{1425}\!/_{2048}) \cdot 2^{20} = [0, 729600)$$

When returning signal *e* to the modulator, its reference needs to be translated to the modulator reference, r11. This is simply done using a 9-bit shift right. Loss in resolution in this stage is not avoidable through software restructuring. Such loss is directly related to the actual control resolution of the modulator. If the loss in resolution is not acceptable, a different—perhaps external—modulator needs to be used.

One important feature of the controller implementation mapped out in Figure 74 is its complete dependence on simple and fast operations: summation/subtraction, bit-shifting, and comparison for limitation. No costly operations such as multiplications or divisions are needed anywhere within the controller. This multiplier-free controller is a great saver for implementations utilizing application-specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs), and can also allow microcontroller-based solutions with no dedicated high throughput multipliers.

6.5. Experimental Results

A buck converter prototype with parameters matching the design example was constructed. The controller was implemented using a board based on Texas Instrument's TMS320F2812 DSP chip. This chip has far more capabilities than actually needed for this example, but was nevertheless used for demonstration purposes. The blueprint in Figure 74 was translated into C code, the core of which is shown in Figure 80.

```
// Output voltage regulation (OVR) controller
unsigned int v_out_ctl(unsigned int v_out_ref)
{

  static int diff=0;                // difference
  static int u1=0,u2=0;             // compensator states
  static long compensated_diff;     // output of compensator
  static long u_int=0;              // integrator state

  // Comparator
  diff=(v_out_ref>>1)-(Vo_AdcVal>>1);       // signed r15, [-1.0, 1.0)

  // Compensator zeros
  compensated_diff= ( (long) diff<<5 )
                   -( (long) u1<<6   )
                   +(        u1>>3   )
                   +( (long) u2<<5   );     // signed r20, [-4.0, 4.0)

  // Update compensator states. This should be done after its difference equation
  u2=u1;
  u1=diff;

  // Gain and integrator
  u_int+=(compensated_diff<<5);             // signed long, (-129.0, 129.0)

  // Limit integrator output
  if(u_int<DUTY_LOWER_LIMIT)
    u_int=DUTY_LOWER_LIMIT;
  if(u_int>DUTY_UPPER_LIMIT)
    u_int=DUTY_UPPER_LIMIT;

  return u_int>>9;                          // return as unsigned int r11, [0.0, 1425/2048]
}
```

Figure 80 The digital controller blueprint translated into C-language code

A frequency analyzer was used to experimentally measure the closed-loop frequency response. Figure 81 shows that response with a resistive load of 2.5Ω. As predicted by the Matlab plots, a sharp 180-degree phase boost accompanied by a sharp dip in the loop gain is seen at 1kHz. The loop gain crosses zero dB at 5kHz with just above 90 degrees of phase margin.

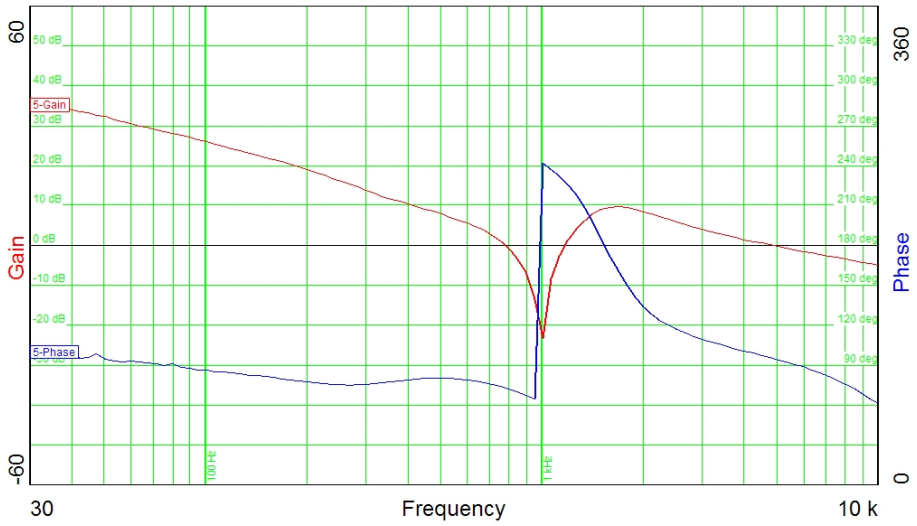


Figure 81 Experimental closed-loop frequency response for a 2.5Ω load

The experimental response of the converter to a load transient is shown in Figure 82. This load transient induces a 300mV over/under-shoot in the output voltage of the converter that dies out within 2 ms. It closely resembles that seen in the simulation results.

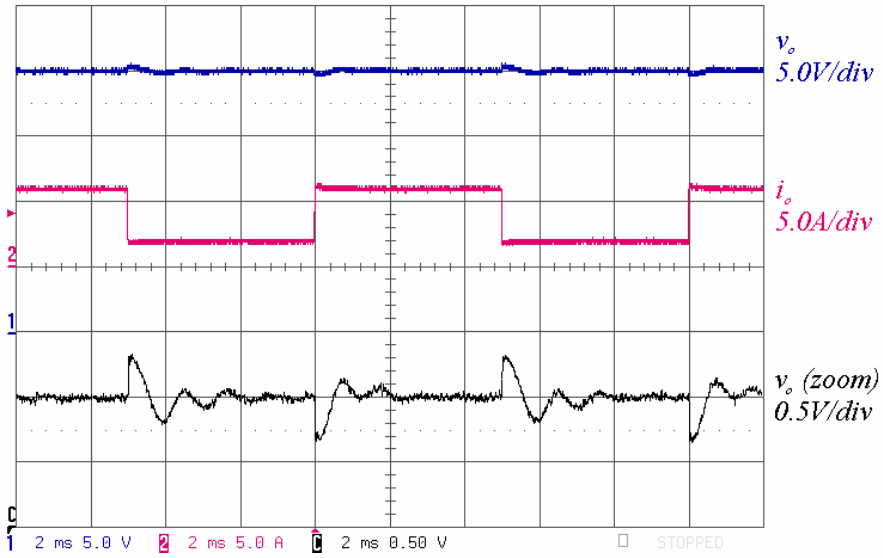


Figure 82 Experimental closed-loop response to a 2-6A load transient

CHAPTER 7: SUMMARY AND FUTURE WORK

7.1. Summary

The proper and optimal design of space PMAD systems plays a key role in the success and economic feasibility of a spacecraft's mission. For solar-powered spacecrafts, the limitation of power instantaneously available from the solar source is particularly challenging. Energy storage is an essential component of their energy harvesting systems. By handling the mismatch between the source availability and loading patterns, storage alleviates the need for exaggerated over-sizing of the source for a given load. Storage absorbs extra available energy when the load is light and covers the deficit when the source is week, preventing load dismissal in response to large-signal instability conditions.

While the power electronics technology available today is capable of performing the management objectives for such systems, there is still plenty of room for enhancement. The design choices of such power management systems are heavily dominated by the compromise between different system architectures. Using a limited number of converters yields a simple non-flexible system, often with over-sized sources and storage devices. Adding more converters allows enhanced power management with tighter bus voltage regulation at the price of increased cost, conversion loss, and control complexity. Independent control of available resources facilitates the realization of crucial control functions such as MPPT and battery charge control. Integrated multi-port converters promise numerous advantages for use in space PMAD systems.

A switching phase-leg is a common structure in switching power converters. This basic structure can be used to achieve both isolated and non-isolated power conversion. A number of multi-port converter topologies can be constructed based on the utilization of this structure to simultaneously realize both. Such an approach has the potential for savings in component count and power loss. Three novel three-port topologies were introduced and discussed in this dissertation based on this approach.

Chapter 4 introduced the TM-HB converter, a topology based on the half-bridge converter and suitable for low power levels. This converter has an input, bidirectional energy storage, and an output port. It is capable of achieving soft-switching of its active switching devices. Using a fixed-frequency PWM switching scheme, it possesses two control degrees of freedom. This allows it to simultaneously achieve two independent control objectives. Experimental captures from a 200W prototype demonstrate the basic operation of the converter and its performance under closed-loop control.

Chapter 5 investigated the integration of a synchronous boost into the structure of a PS-FB stage to form three-port converters. The resultant converters have two bidirectional ports and a galvanically isolated load port. The two proposed topologies, the S-BI-PS-FB and A-BI-PS-FB, are analyzed in detail in terms of operation and design guidelines. A detailed comparison shows that the S-BI-PS-FB converter is an ideal option when interfacing a source with a narrow voltage range at the boost input. It has the potential to minimize both the cost and conversion losses in the system. For a wide input voltage range, however, it imposes constraints on the transformer design that limit the savings it delivers. In such cases, the A-BI-PS-FB converter becomes a more favorable choice. For an extremely wide input voltage range, a conventional cascaded system composed of non-integrated boost and PS-FB stages becomes the most

effective. The results of the theoretical evaluation and comparison were verified using experimental data collected from a 1kW test-bed. The integrated converters are also capable of achieving two independent control objectives as demonstrated by a closed-loop experiment.

Digital control is especially useful for the proposed topologies due to the need for customized switching patterns not found on existing dedicated controller ICs. Moreover, systems based on such topologies require dynamic selection of the relevant control objectives, and the realization of high level controls such as MPPT and battery charge regulation.

Chapter 6 presented an effort to develop a systematic digital controller design method that appeals to practicing engineers. It is shown that the advantageous direct-digital design can be performed without obtaining a discrete-time model of the controlled plant. The behavior of digital blocks can rather be analyzed in the analog frequency domain. Moreover, an enhanced numbering system is developed that simplifies modeling and implementation of the software code realizing the control algorithm. The proposed design and implementation methodology offer simple, robust, and multiplier-free regulation loop design. This methodology was experimentally verified by closing an output voltage regulation loop around a synchronous buck converter prototype.

The proposed topologies are suitable for many applications. They are particularly advantageous for alternative energy systems powered by solar/fuel cells and requiring energy storage in the form of batteries or super-capacitors. The utilization of integrated topologies promises increased efficiency and reduced cost. Applications such as communication repeater stations, traffic lights in remote areas, mobile chargers for laptops, cellular phones, future solar powered electric vehicles, and space PMAD systems can all potentially benefit. Moreover, these

converters can be used as pre-regulator stages of grid-interactive solar inverter systems that offer battery-backed stand-alone operation when the grid is absent or unstable.

7.2. Future Work

The promising results of the work presented here warrant further investigation and extension of the presented concepts. Suggested future areas of investigation are:

1. Derivation of more topologies using the same and similar integration concepts as that presented in Chapter 3: different topologies will prove most useful in different applications with different voltage levels, power levels, and switching frequencies.
2. Enforcing zero-current switching (ZCS) transitions: this will allow the utilization of the integrated topologies in high voltage applications with IGBTs, giving an even higher potential for power loss savings.
3. Investigation of alternative PWM modulator structures that support better decoupling of multiple control loops, as well as current-mode control.
4. Generalized multi-variable multi-port control theory: the development of a more general and concise approach to relating the number of available degrees of freedom to the control objectives and their effective frequency ranges.
5. Optimized controller design for multi-port converters: theoretical work still needs to be done concerning the design of multiple high-bandwidth regulation loops closely coupled through the converter power stage.
6. Evaluation of modular architectures based on multi-port converters, and development of related dynamic models and control strategies necessary for maintaining proper system-wide operation and stability.

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