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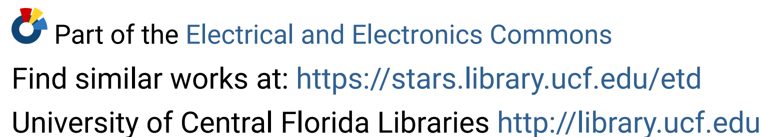

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CMOS RF CITUITS VARIABILITY AND RELIABILITY RESILIENT DESIGN, MODELING, AND SIMULATION

by

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B.S. Shanghai Jiaotong University, 2003
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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical Engineering and Computer Science
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at the University of Central Florida
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2011

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ABSTRACT

The work presents a novel voltage biasing design that helps the CMOS RF circuits resilient to variability and reliability. The biasing scheme provides resilience through the threshold voltage (V_T) adjustment, and at the mean time it does not degrade the PA performance. Analytical equations are established for sensitivity of the resilient biasing under various scenarios. Power Amplifier (PA) and Low Noise Amplifier (LNA) are investigated case by case through modeling and experiment. PTM 65nm technology is adopted in modeling the transistors within these RF blocks. A traditional class-AB PA with resilient design is compared the same PA without such design in PTM 65nm technology. Analytical equations are established for sensitivity of the resilient biasing under various scenarios. A traditional class-AB PA with resilient design is compared the same PA without such design in PTM 65nm technology. The results show that the biasing design helps improve the robustness of the PA in terms of linear gain, P1dB, Psat, and power added efficiency (PAE). Except for post-fabrication calibration capability, the design reduces the majority performance sensitivity of PA by 50% when subjected to threshold voltage (V_T) shift and 25% to electron mobility (μ_n) degradation. The impact of degradation mismatches is also investigated. It is observed that the accelerated aging of MOS transistor in the biasing circuit will further reduce the sensitivity of PA.

In the study of LNA, a 24 GHz narrow band cascade LNA with adaptive biasing scheme under various aging rate is compared to LNA without such biasing scheme. The modeling and simulation results show that the adaptive substrate biasing reduces the sensitivity of noise figure and minimum noise figure subject to process variation and

device aging such as threshold voltage shift and electron mobility degradation. Simulation of different aging rate also shows that the sensitivity of LNA is further reduced with the accelerated aging of the biasing circuit.

Thus, for majority RF transceiver circuits, the adaptive body biasing scheme provides overall performance resilience to the device reliability induced degradation. Also the tuning ability designed in RF PA and LNA provides the circuit post-process calibration capability.

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To my wife T.Y. Ma, my children H.C. Liu and H.Y. Liu

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LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADS	Advanced Design System
ASIC	Application Specific Integrated Circuits
BD	Breakdown
BSIM	Berkeley Short-Channel IGFET Model
BTI	Bias Temperature Instability
BV	Breakdown Voltage
CDMA	Code Division Multiple Access
CHE	Channel Hot Electron
CMOS	Complementary Metal Oxide Semiconductor
C-V	Capacitance versus Voltage
DC	Direct Current
DFR	Design for Reliability
DSB	Double-Side Band
DUT	Device-Under-Test
EOS	Electrical Over Stress
EOT	Effective Oxide Thickness
ESD	Electrostatic Discharge
ESOA	Electrical Safe Operating Area
FET	Field Effect Transistor
FOM	Figure of Merit
HC	Hot Carrier

HCI	Hot Carrier Injection
HF	High Frequency
IC	Integrated Circuit
IGFET	Insulated Gate FET
IIP3	Input Third Harmonic Intercept Point
IP3	Third Harmonic Intercept Point
I-V	Current versus Voltage
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LC	Inductor-Capacitor
LDD	Lightly Doped Drain
LNA	Low Noise Amplifier
MC	Monte Carlo
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NF	Noise Figure or Noise Factor
NFmin	Noise Figure Minimum
NMOSFET	N-type MOS Field Effect Transistor
OPAMP	Operation Amplifier
PA	Power Amplifier
PAE	Power Added Efficiency
PBTI	Positive Bias Temperature Instability

PLL	Phase-Locked Loop
PMOSFET	P-type MOS Field Effect Transistor
PTM	Predictive Technology Model
QPSK	Quaternary Phase Shift Keying
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SBD	Soft Breakdown
SH	Self-Heating
SNR	Signal-to-Noise Ratio
SOC	System on Chip
SOI	Silicon-on- Insulator
STD	Standard Deviation
TDDB	Time Dependent Dielectric Breakdown
VIP3	Third Harmonic Intercept Voltage
VLSI	Very-Large-Scale Integration
V_T	Threshold Voltage

CHAPTER ONE: INTRODUCTION

1.1 Motivation

The continuous scaling down of semiconductor device length to the nanometer regime results in yield and reliability challenges [1-3]. Smaller feature size makes the metal–oxide–semiconductor field-effect transistor (MOSFET) more sensitive to the process variations and stress-induced degradation, which also leads to the fluctuation and degradation of relevant circuits especially for those operating in the radio frequency (RF) range [4-8].

The circuit designer needs larger design margin to insure circuit robustness against issues such as yield and reliability. This leads to many efforts in developing design for reliability techniques [9-11]. The fabrication process variability and long-term reliability resilience design may reduce over-design while increasing yield and circuit robustness. The resilient biasing technique aims to design reliable circuits that are capable of post-process adjustment and insensitive to the transistor parameter degradation over long-term stress effect.

Class-AB Power Amplifier (PA) and Low Noise Amplifier (LNA) are the major RF blocks in RF transceivers. Under the high operation frequency, the performance such as power gain, PAE and noise figure (NF) are subjected to degradation due to the device fabrication fluctuation and long term stress induced transistor parameter degradation. Thus how much improvement does the upgraded biasing schematic provide to these RF

blocks is a major focus in this research work. Comparison is made between these RFICs with and without such design scheme. Analytic modeling is provided as the theoretic basis in case by case study. Analysis from small signal point of view is also proposed, such as performance parameters of LNA. Combined all the modeling analysis, clear observations are made for the resilient body biasing and its impact on the major RF circuits.

1.2 Research Goals

The research work focus on solving the following issues:

1. Variability and reliability characteristics of MOSFET transistors
2. Novel adaptive body resilient biasing design schematic
3. The resilient biasing design analytical modeling
4. Small signal modeling and analysis of RF circuits
5. The performance improvement of the resilient biasing on RF class-AB PA and narrow band LNA
6. The impact of device degradation mismatches on the performance sensitivity of the circuits
7. RFIC performance comparison under Predictive Technology Model (PTM) 65-nm technology [12]

1.3 Outlines

In brief, chapter 2 presents the device fluctuation modeling and reliability issues under submicron technology. A novel adaptive body biasing design schematic is proposed in chapter 3. The tunable body biasing scheme aims to provide RFICs performance resilient to device reliability degradation and capable of post fabrication calibration. Chapter 4 analysis such design on PA and compare the performance advancement in PTM 65 nm technology. The narrow-band LNA resilient structure is analyzed in chapter 5. Chapter 6 arrives the conclusion.

CHAPTER TWO: DEVICE FLUCTUATION MODELING AND RELIABILITY ISSUES

2.1 nMOSFET Fluctuation

With the continuous scaling down of feature length, the semiconductor device tends to be more sensitive to process parameters such as random doping effects.

2.1.1 nMOSFET Structure

A basic n-channel MOSFET (nMOSFET) transistor cross-section view is shown in figure 2.1. For CMOS RF applications, nMOSFET are the major device used as reported by several recent researches [13-17]. Also for the research in this work, CMOS nMOSFET is utilized for the construction of different RF circuit blocks.

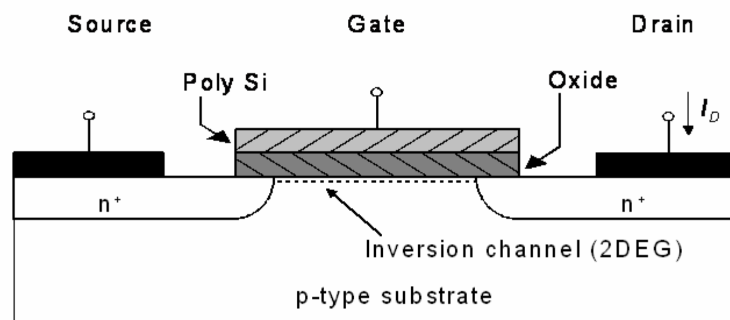


Figure 2. 1. Si nMOSFET cross section view

As predicted by Moore's Law, more and more number of transistors is integrated in one processor. The transistor size will keep shrinking as the smaller device fabricated in lab shown in figure 2.2. The continuous shrinking of device size to the nanometer regime results in fluctuation and reliability challenges. Smaller feature size makes the nMOSFET more sensitive to the process variations. When the process variations are mentioned in this work, it mainly refers to the doping profile fluctuation within a semiconductor device during the fabrication process. Beyond the scope of this work, it may also refer to the fluctuation of gate insulation dielectric thickness and other important process variations.

To clarify the device fluctuation, a 22 nm gate length NMOS transistor is built as an example compared to a standard 65 nm NMOS device. The doping profile of the 22 nm NMOS transistor cross section is selected to be state-of-art as presented in figure 2.3. The bulk Si doped with acceptor concentration of 8×10^{18} cm^{-3} and the drain/source region is doped with donor concentration of 2×10^{20} cm^{-3}. To be comparable with state-of-art CMOS technology, typical LDD structure is also included in the device. For 22 nm device, the oxide thickness is selected to be 1.2 nm, while 1.85 nm oxide thickness is picked for 65 nm device.

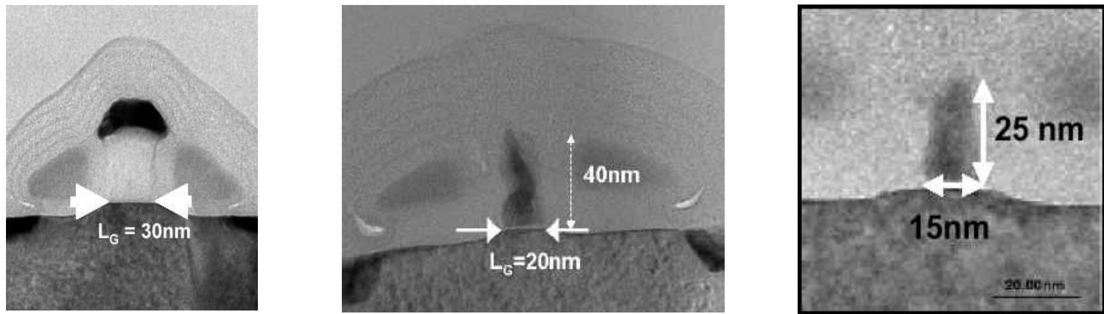


Figure 2. 2. Smaller nMOSFET fabricated in labs

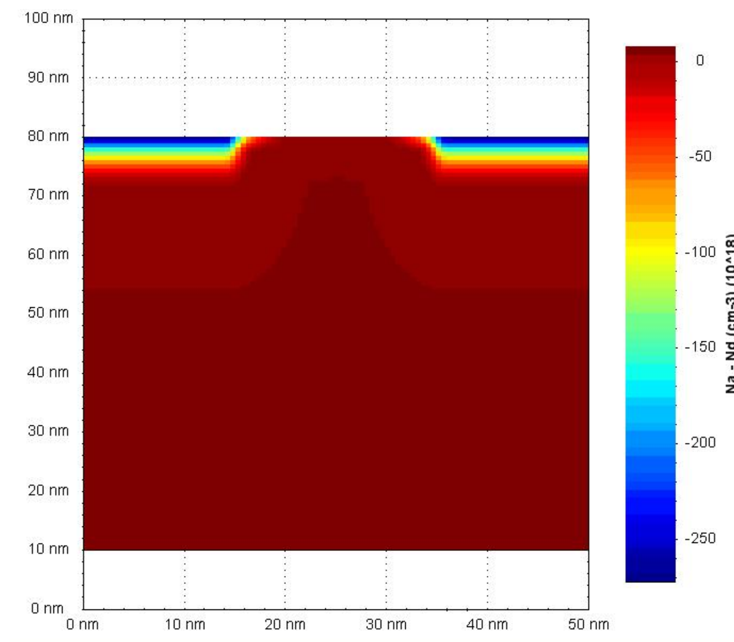


Figure 2. 3. Doping profile of a 22 nm nMOSFET cross section

2.1.3 Random Doping Fluctutation

The threshold voltage (V_T) mismatch is the major RF circuit performance indicator of CMOS technology. Random doping fluctuation [18] is one of the important process fluctuation sources. As a rough approximation, the contribution of V_T fluctuation due to random doping profile is modeled [19] as:

$$\sigma^2_{Vt,doping} = \frac{2q^2 t_{ox}^2}{WL\varepsilon_{ox}^2} \int_0^{W_D} N_A(x)(1 - \frac{x}{W_D})^2 dx \tag{2.1}$$

Note that the dimension dependence of the device deviation to the doping fluctuation. With shrinking trend of gate length L, the deviation of V_T is expected to be larger. The design could be endangered.

A computational effective device simulator [20] is adopted in the study of random doping induced fluctuation in the model parameters of MOSFETs. It is assumed that the fluctuation of some parameters of the device can be calculated from the sensitivity function of the parameter. To study a single MOSFET device, the most important parameters are terminal currents and threshold voltages.

From mixed mode simulation, figure 2.4 shows the drain current fluctuation due to random doping effect. The error bar along the current curve represents the standard deviation of the drain current under that bias point. With a 10 μm width LDD nMOSFET, the fluctuation of drain current increases from increased drain-source voltage swing. Gate bias is selected to be 0.7 V, while the drain voltage is swept from 0 V to 0.5 V.

Figure 2.5 and 2.6 shows the 2-D distribution of sensitivity function of the MOSFET due to donor and acceptor, respectively. For donor dopant fluctuation, one donor at the peak sensitive position can cause V_T to change -0.005 V. For acceptor at the peak sensitive region, it will cause Vth to rise about 0.0045 V. Different dopant type and location can cause different effects on the V_T of the device.

Due to the random doping fluctuation, the standard deviation of V_T of the 22 nm device is computed to be 0.031 V. While compared to the 0.022 V deviation of the 65 nm device, the trend of more sensitivity for shrinking device is observed. So it can be foreseen that the device intrinsic fluctuation becomes more important factor affecting the circuit performance as long as the channel length keeps scaling down.

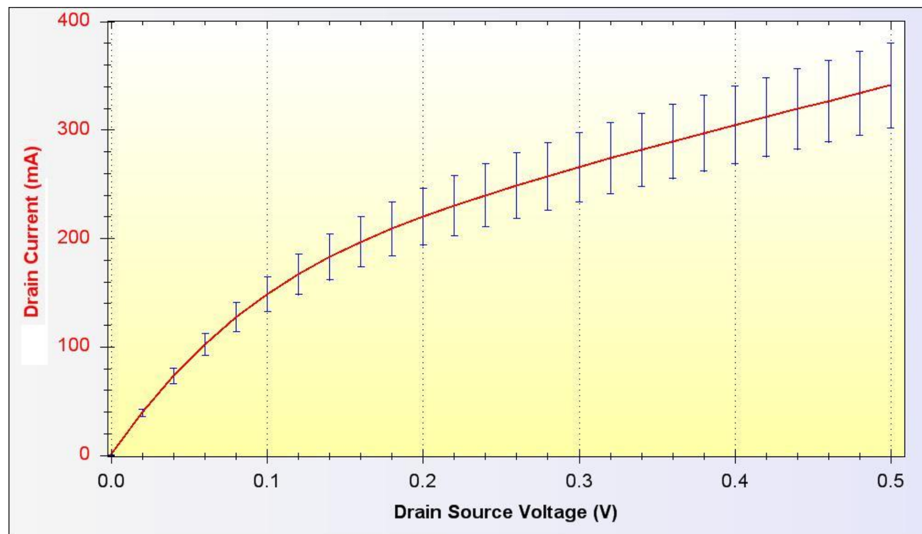


Figure 2. 4. nMOSFET drain current fluctuation

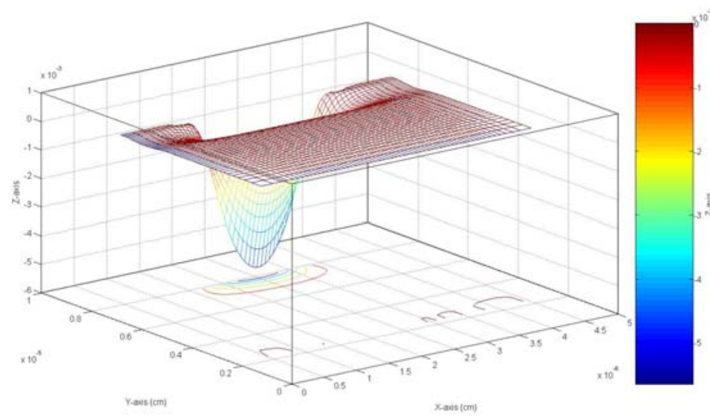


Figure 2. 5. Sensitivity function distribution of V_T Vs Nd

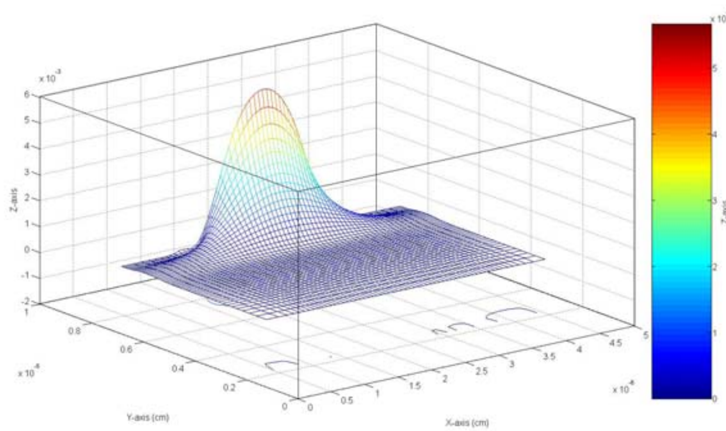


Figure 2. 6. Sensitivity function distribution of V_T Vs Na

2.2 nMOSFET Reliability

The in field degradation of the MOS transistor can be caused by many reliability mechanisms, which includes channel hot electrons (CHE), time-dependent dielectric breakdown (TDDB), and biased temperature instability (BTI). These problems cause the

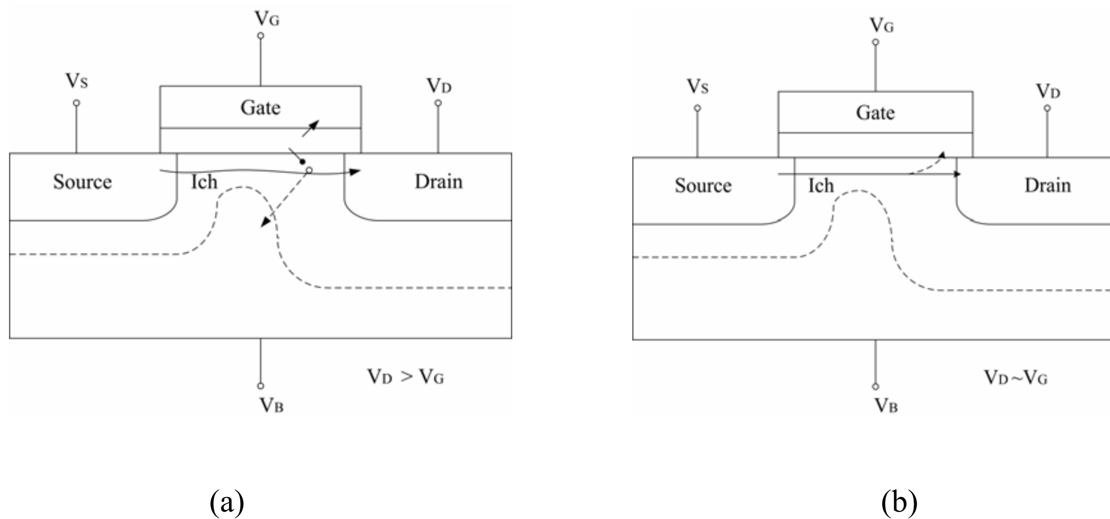
device model parameters shifting such as V_T and mobility degradation. A brief background discussion is described in the follows.

2.2.1 Channel Hot Carriers Injection

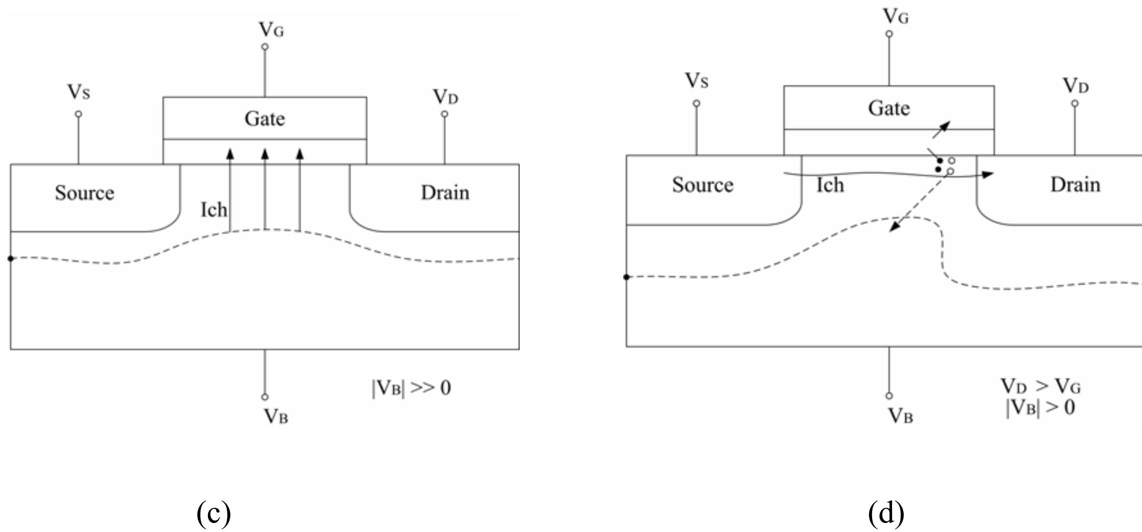
Hot carriers refer to both carriers and electrons in the high electric field region in a semiconductor device. Hot electrons injection is the phenomenon in MOSFET devices where an electron gains sufficient kinetic energy to overcome a potential barrier necessary to break an interface state [21]. The so called hot electron effect occurs when unwanted electrons are trapped in the dielectric interface, which will cause unexpected device degradation and instability.

There are several common bias situations that the hot carriers are triggered: 1. drain avalanched hot electron; 2. channel hot electron; 3. substrate-gate hot electron; 4. substrate hot electron. As shown in figure 2.7 (a), the drain avalanched hot electron happens when the drain bias is much higher than gate bias. Thus a much intense electric field exists within the near gate-drain region. The accelerated channel carriers will have the chance of colliding with Si atom, which will lead to free electron-hoe pair. This is the familiar impact ionization process. The electron near the drain end will get enough kinetic energy from high electric field to surpass the gate dielectric barrier. Some electron will be trapped in the dielectric during the trespass process. The accumulation of such trapped ion will lead to degradation of device performance. These defects then lead to V_T shifts and transconductance degradation of MOS devices. The maximum CHE for deep submicrometer device occurs when the gate-source voltage equal to the drain source voltage [22]. It is also found that CHE generation rate is reduced at AC condition [23].

For the figure 2.7 (b), both the drain and gate voltage is high enough. The impact ionization is triggered in the high electric field drain region for short channel MOS transistor, where channel hot electrons (CHE) are injected into gate oxide [24]. These electrons can be injected into normally forbidden regions of the device, as the gate dielectric. Substrate carriers may be driven to the gate dielectric channel interface when the magnitude of substrate bias is substantially large, as shown in figure 2.7(c). They are so called substrate hot electrons. Combined with gate-drain bias shown in figure 2.7(d), secondary generated hot electrons occurs in the drain side. They are generated by the hot carriers generated by previous impact ionization process. These secondary hot electrons may get enough kinetic energy to cross the oxide barrier, during which they may be trapped and form oxide defects. All these defects will lead to the degradation of the device. There are several device design aspects preventing or reduce the hot electron effects: 1) lightly doped drain to reduce the E-field near the drain; 2) insertion of buried P layer; 3) increased channel length, etc.



(a) (b)



(c) (d)

Figure 2. 7. Hot electron injection into dielectric causing a gate current, interface and gate oxide degradation: (a) drain avalanched hot carrier; (b) CHE effect; (c) substrate hot electron injection; (d) substrate-gate hot electron.

2.2.2 Dielectric Breakdown

Dielectric breakdown refers to the malfunction of dielectric due to certain electric or other damage. There are commonly three types of oxide breakdown for a MOSFET: a) electrical over stress (EOS) and electro-static discharge (ESD) induced dielectric breakdown; b) early life-time breakdown; c) time-dependent dielectric breakdown (TDDB).

The first class of breakdown involves large voltage/current or charge accumulated that is way over the limitation of the device. The proper operation of MOS transistors relies on the insulating properties of the dielectric layer. Each dielectric material has a

maximum electric field it can intrinsically sustain (dielectric strength). Applying a higher field leads to breakdown which destroys the insulating properties and allows current to flow. So the breakdown will happen in very short time due to these over stressed voltage, current, and charge.

The later two types of oxide breakdown have similarity. They happen with the normal operation of the device when ‘wear out’ of oxide take effect. At lower electric fields the insulator can wear-out after some time and finally break down completely. This time-dependent dielectric breakdown (TDDB) is a very important reliability aspect for MOS structures. The ultrathin gate oxide will experience the soft breakdown (SBD) [25]. The SBD will lead to the increased gate leakage current and noise, the resulted circuit including ring oscillator may deviate from its specification [26, 27]. The SBD will also degrade the V_T and mobility as observed by the current-voltage characteristics reported by C. Yu [28].

Several models have been proposed to characterize TDDB in order to explain the mechanisms involved in dielectric degradation, which are Anode Hole Injection Model [29, 30], Electron Trap Generation Model [31-34], and Percolation Model [35, 36]. Figure 2.8 illustrates the Percolation Model for TDDB, where the red shows the conduction path during breakdown. Mainly there is weak pot within the dielectric which comes from the uneven or poor dielectric growth process. These defects or weak pots may be caused by: a) sodium ions; b) contaminations; c) crystalline Si defects. TDDB may be disaggregated by extreme conditions such as high E-field and temperature [37].

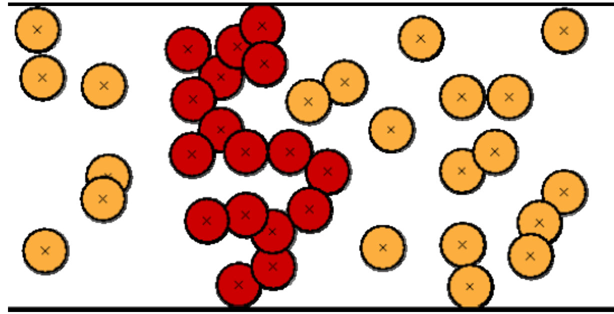


Figure 2. 8. Illustration of Percolation Model

Research [38, 39] shows that TDDB is composed of several stages especially for ultra-thin dielectric: build-up stage, run away stage, partial breakdown and complete breakdown stage. The latter two stages are proposed for ultra-thin dielectric, where the conventional TDDB model ignores the time from partial breakdown to complete breakdown. During the build-up stage, the charges are accumulated in the oxide as trapped charge. With the accumulation of trapped charges, higher E-field are formed until the run away stage comes. When the charge defects form the field exceed the dielectric breakdown limit in some weak pots, the device reaches the run away stage. Large current flows through certain paths, which will be heated up. The heat will also lead to larger current, thus a positive feed back loop is formed. Finally both electric and thermal run away will happen simultaneously, damage the device in a very short time.

2.2.3 Bias Temperature Instability

Bias temperature instability (BTI) is a degradation phenomenon affecting mainly MOS field effect transistors. The highest impact is observed in p-channel MOSFETs

which are stressed with negative gate voltages at elevated temperatures. Electrochemical reactions at the oxide interface take place [40]:

$$\text{Si-H+O}_3\text{-Si-O-Si+h}^+ \leftrightarrow \text{Si+O}_3\text{-Si-OH}^+\text{-Si} \tag{2.1}$$

The released hydrogen from Si-H bond by holes will have the chance of being trapped at the oxide interface. The positive oxide charges will then be formed. Research shows that the interface OH group bonded to Si dioxide bond will leave one trivalent Si at oxide side and one at Si side, which corresponds to the fixed positive charge (Nf) and the interface trap (Nit). NBTI stress will let Nf and Nit shift, which lead to the device performance degradation.

The stress conditions for this negative bias temperature instability (NBTI) typically lie below 6MV/cm for the gate oxide electric field and temperatures ranging between 100-300°C. Higher electric fields can cause additional degradation due to hot carriers and should be avoided for the evaluation of NBTI. Both the mechanisms of NBTI and PBTI are studied in [41, 46-50]. [42] reported V_T shift by NBTI with the reaction-diffusion model and the mobility reduction described in [43]. KT. Lee [44] compared PBTI and CHE effects on nMOSFET high-k/metal-gate dielectrics and shows PBTI associated CHE will worsen the performance further. Huard et al [45] presents the effect of BTI on pMOSFET and nMOSFET under positive and negative voltage stress as shown in figure 2.9.

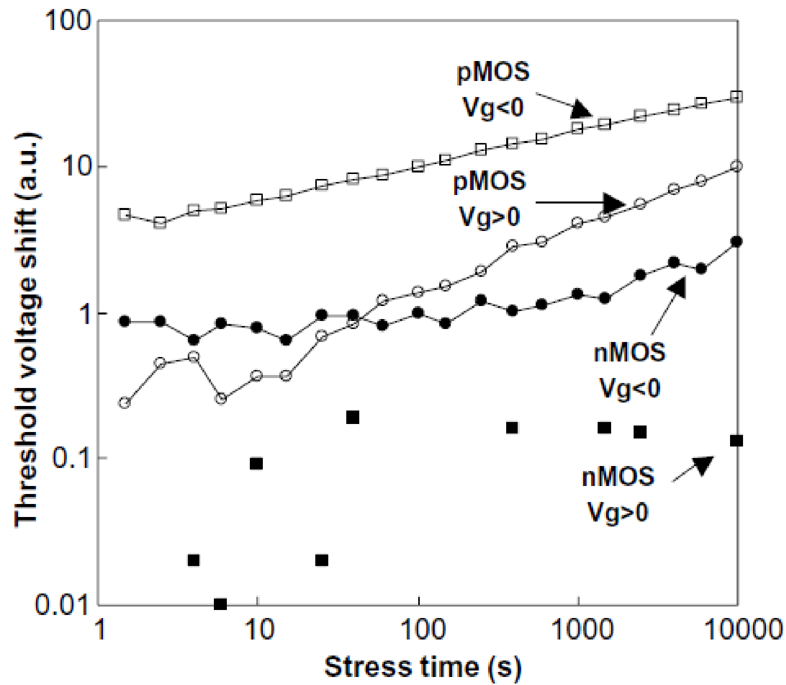


Figure 2. 9. The effect of BTI for p- and n-channel MOSFET with negative and positive voltage stress [45]

2.3 Stress Induced Degradation

2.3.1 nMOSFET BSIM Model

In this thesis, nMOSFET will be expressed in BSIM model card format. BSIM is CMOS technology industry standard model adopted by world semiconductor foundry. The BSIM family is a physical based, accurate, scalable, and predictive MOSFET SPICE model for circuit simulation. It is developed by Research Group in the Department of

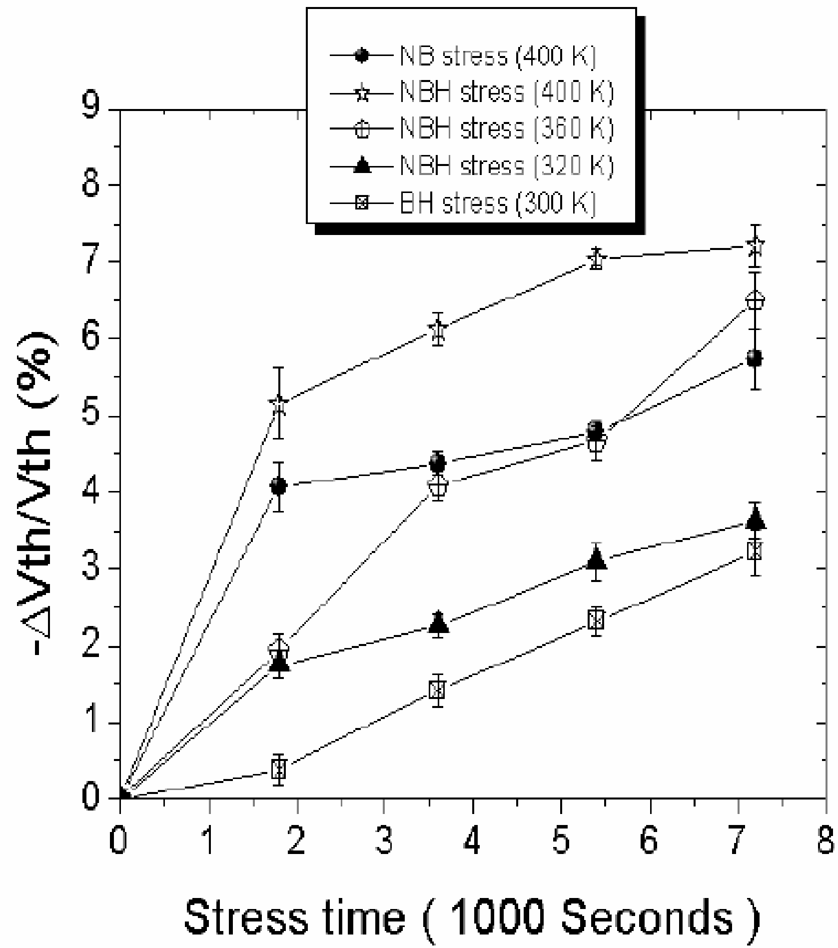
Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley.

BSIM4 is most updated version of its model family. The PTM model extracted parameters are also expressed in BSIM4 format, which will predict the most accurate performance of today's sub-nanometer device especially in radio frequency operation.

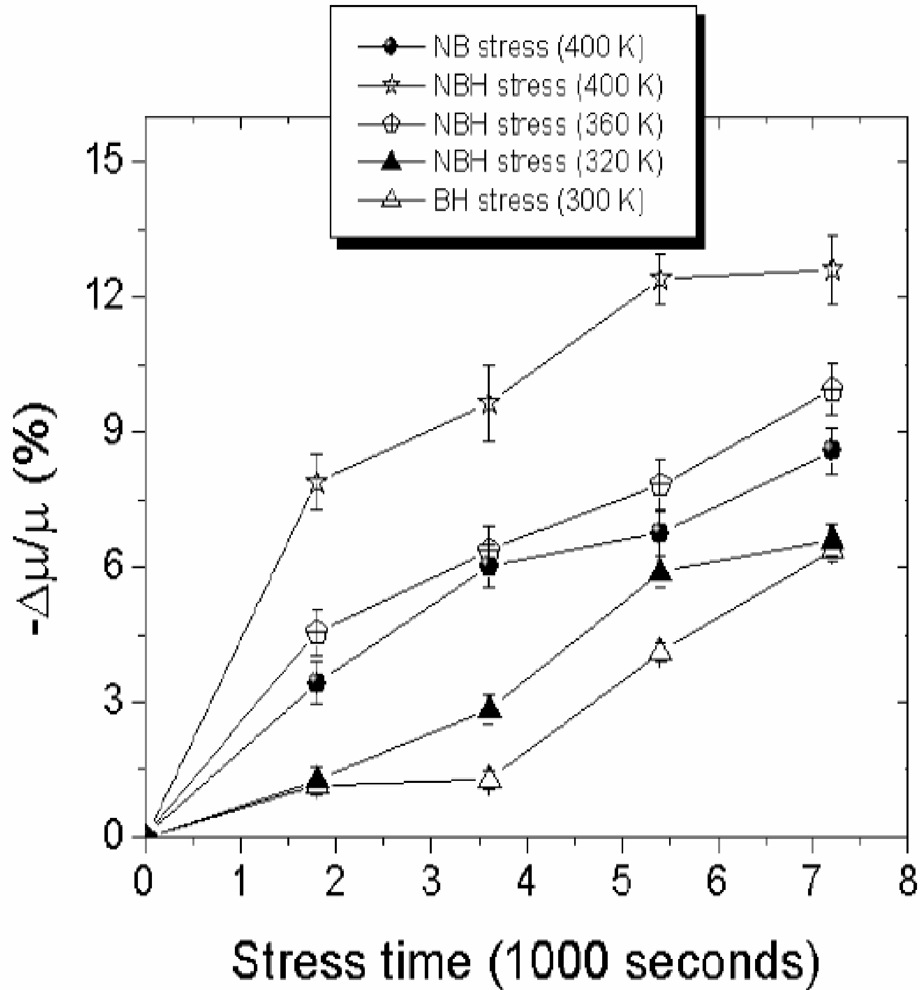
2.3.2 Stress Impacts on Device and Circuits

Major reliability degradation mechanisms are introduced in previous contents. Considered different stress conditions, the impact of reliability induced degradations on the MOSFET transistor and relevant RF circuits have been studied in recent works [51-57]. The square wave voltage stress on the MOSFET gate and drain may degrade the device more than the static DC stress [51, 52]. Increased stress frequency will speed up the wear out progress and shorten the device life time [53-55]. But at extremely high frequency range, the device does not suffer too much from the stress induced degradation as it did in low frequency [56, 57].

The device model such as BSIM4 model parameter shifts due to the stress induced reliability degradation has been studied [58-60]. A comparison for threshold voltage and mobility shift of fresh and NBTI stressed device is illustrated in figure 2.10. The major factors affecting the device degradations are known to be: insulator trapped charge and interface states generation [61, 62].



(a)



(b)

Figure 2. 10 . (a) Threshold voltage degradation versus time; (b) Mobility degradation versus time; with the stresses performed at 400 K.

The circuit level performance degradation after stress is examined for digital, analog, and RF [63-73]. An observation for digital circuits is the gate stress induced increased gate leakage current which reduces the noise margin of 6-T cell SRAM [63]. For power amplifier, the power efficiency will decrease after the stress [64]. RF transceiver circuits performance parameters such as power added efficiency, noise factor

or noise figure, small signal gain, power gain, input third order inter-modulation point, oscillation frequency and phase noise are degraded after various stress including hot electron and NBTI [65-68]. For example, [69] reports increased phase noise of a voltage controlled oscillator after the stress.

In recent years, some design modifications are introduced into the design of digital and analog circuits to get certain margin for reliability [70-72]. A processor taking into account NBTI effect is proposed [73] and an NBTI aware synthesis method is designed for digital circuits' gate delays [74]. But there are still little efforts working towards the circuits in RF domain for such design margins. The influence of hot electron stress on the digital circuits will not affect a lot of its key function. The affected delays may still locate in acceptable range and will not affect the normal operation of the module. Compared to digital and analog circuits, RF circuits are more sensitive to such hot electron stress and NBTI induced device degradation. Especially when the operation frequency is very high, the performances of RF transceivers are very likely to be degraded in certain amount. The impact of reliability is considered as major threaten to the functional robustness of such circuits.

2.4 Chapter Outline

After a brief discussion about main strain silicon transistor and industry trend as predicted by Moore's Law, the random doping fluctuation is introduced as one factor of process fluctuation in state-of-art technology. Then MOSFET reliability degradation due to the long time electric and thermal stress is described by three main categories. All these phenomenons bring the degradation of today's transistor, which will be applied in

the main-strain analog and RF integrated circuits. Thus the circuit performance will deviate from the expectation under the design specification. The content in this section provides the insight of the need to build the novel design targeted for the degradation resilient purpose in this work.

CHAPTER THREE: RF DESIGN FOR VARIABILITY AND RELIABILITY

3.1 RF Design for Reliability

Recently, many papers on reliability and variability for analog, digital, and mixed circuits have been published [75-81]. Chen and Gielen [75] used postfabrication calibration to static errors in the design of a 14-bit current steering digital-to-analog converter. The postfabrication calibration technique dynamically rearranges the switching sequence of most-significant bit current sources to cancel random errors. The runtime monitoring and countermeasures to compensate for reliability errors is presented by Dierickx et al. [76] and Pananikolaou [77] as shown in figure 3.1. The idea is to continuously monitor the operation of a system or circuit and take runtime countermeasures to compensate for variability and reliability errors. Several groups proposed NBTI-aware techniques [78-80] for various chip design applications, which make PMOS transistors sustaining sever stress condition.

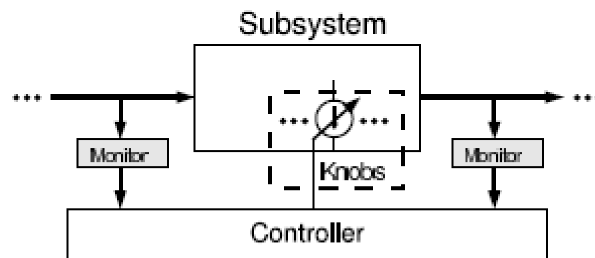


Figure 3. 1. General architecture of a knobs and monitor based system.

A recent novel DFR specific for RF circuits is suggested in 2008 by using adaptive gate biasing scheme [81]. The gate biasing schematic is presented in figure. As a brief explanation quote in [81] by examining the circuit in Fig. 3.2, one could keep the relative V_{GS}–V_T stable to maintain a constant drain current for the MOS transistor M1. The reason why the variation of the threshold voltage does not affect the drain current of M1 is explained as follows. The gate bias of the transistor M1 is set by the input biasing circuit M0 and R_0. When the long-term voltage stress simultaneously increases the threshold voltages of the transistors M1 and M0 due to their identical biasing (stress) conditions, the drain current of M0 decreases. Consequently, the ohmic loss from the resistor R_0 reduces, and the gate bias of M1increases. The design is applied to a class-AB RF PA with source impedance as shown in figure 3.3. The result shows that PAE of the modified PA is robust against V_T and mobility degradation as verified in figure 3.4.

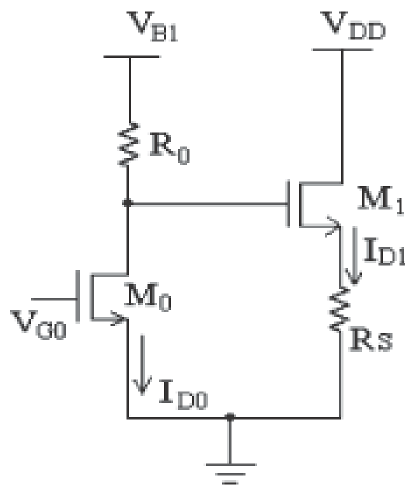


Figure 3. 2. Schematic of adaptive gate-source biasing.

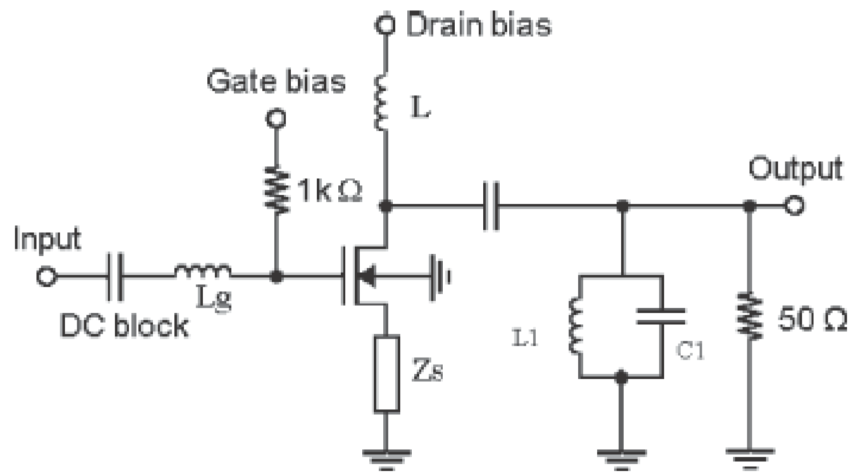
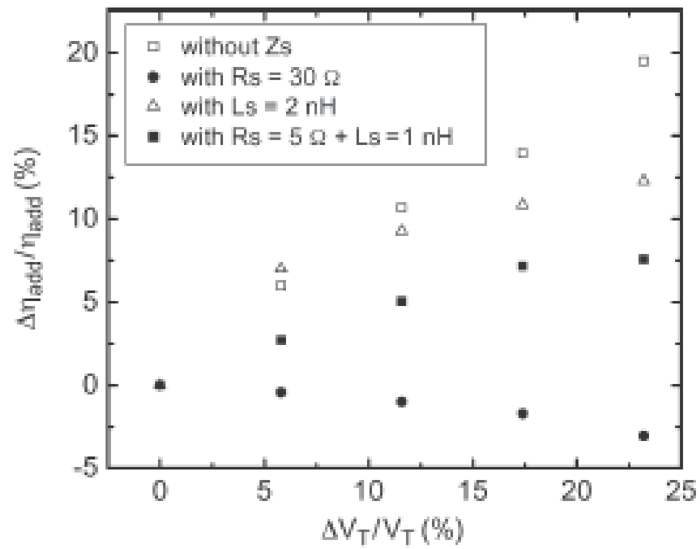
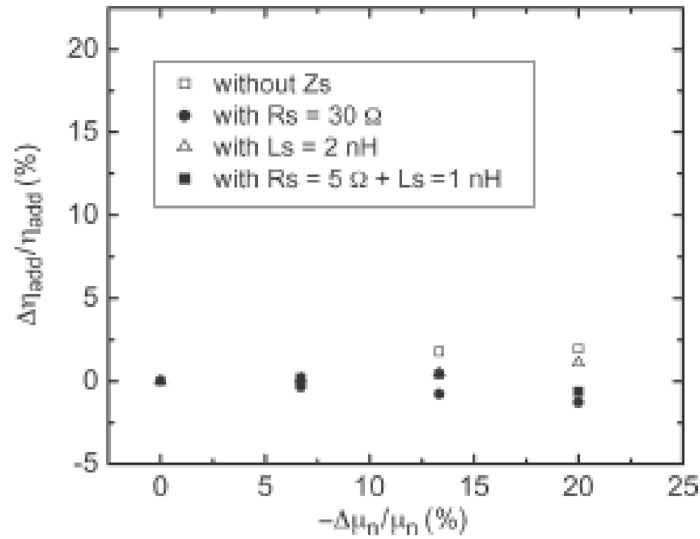


Figure 3. 3. Modified class-AB RF power amplifier with source impedance.



(a)



(b)

Figure 3. 4. Normalized power efficiency versus normalized (a) threshold voltage shift and (b) mobility variation.

There is improvement in the modified RF PA structure as reported in [81], but such method involves the redesign of the original RF circuits. The redesign effort is one major drawback, which may deviate the original RF circuit from its expected specification. Also the gate-source biasing may not be applied to other RF circuits besides PA. Such biasing changes the S11 of the original circuits. Even it is revised by introducing extra matching network, some unpredictable cons may follow such as increased power consumption and risky unstable feedback path.

3.2 Novel Variability and Reliability Resilient Design Analysis

Compared with method in [81], the biasing scheme proposed in this work has the benefit of immediate fit into the RF circuits without redesign of the original schematic and component value. The adaptive body biasing design reduces the sensitivity of low noise amplifier (LNA) to the MOS transistor parameters degradation.

Figure 3.5 shows a simplified variability and reliability resilient biasing design, which introduces tunable adaptive body biasing.

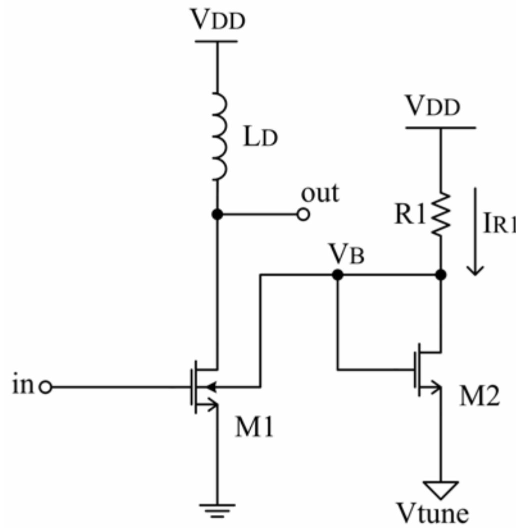


Figure 3. 5. Tunable adaptive body biasing

The right branch of the circuit in Fig. 3.5 controls the body potential of the MOSFET M1. Thus, the threshold voltage of M1 can be adjusted by the body bias. The voltage source Vtune is used for post fabrication calibration. During the long term usage, both M1 and M2 are subject to similar reliability induced threshold voltage and electron mobility shifts. When the V_T of M2 increases, the branch current I_{R1} will decrease. The

reduction in the branch current leads to an increase in the node voltage V_B. Therefore, the V_T of M1 will decrease due to combined reliability degradation and body effect. Similar mechanism applies to electron mobility degradation on both transistors. The drain current of M1 is thus more stable because of resilient biasing design scheme.

3.2.1 Threshold Voltage Degradation

In this section, the V_T shift of 'M1' due to the degradation of both 'M1' and 'M2' is analyzed. A simple MOSFET drain current model [82] is used in the derivation of circuit behavior. Vtune is assumed to be constant and is smaller than the supply voltage V_{DD}. The KCL to solve for V_B is given as

$$I_{R1} \approx \frac{\beta'}{2}(V_B - V_{tune} - V_T')^2 \tag{3.1}$$

$$I_{R1}R1 + V_B = V_{DD} \tag{3.2}$$

where $\beta' = u_n C_{ox} W / L$ is MOSFET structure dimension and material related coefficient for M2. V_T' is the threshold voltage of M2.

From (3.1) and (3.2), node voltage V_B is determined.

$$\frac{\beta' R1}{2}(V_B - V_{tune} - V_T')^2 + V_B = V_{DD} \tag{3.3}$$

From (3.3) one obtains

$$V_B = V_{tune} + V_T' + \frac{\sqrt{2\beta' R1(V_{DD} - V_{tune} - V_T') + 1} - 1}{\beta' R1} \tag{3.4}$$

Using (3.4) the $\delta V_T'$ variation yields the body voltage fluctuation as follows:

$$
\begin{aligned}
\delta V_B &\approx \frac{\partial V_B}{\partial V_T'}\delta V_T' \\
&= (1 + \frac{-2\beta' R1}{2\beta' R1\sqrt{2\beta' R1(V_{DD} - V_{tune} - V_T') + 1}})\delta V_T' \\
&= \delta V_T' - \frac{\delta V_T'}{\sqrt{2\beta' R1(V_{DD} - V_{tune} - V_T') + 1}}
\end{aligned}
\tag{3.5}
$$

Due to the body effect, the V_T of M1 can be described by the following expression

$$
\begin{aligned}
& V_T = V_{T0} + \gamma(\sqrt{2\phi_{FP} - V_B} - \sqrt{2\phi_{FP}}) \\
\Rightarrow \quad & \Delta V_T \approx \frac{\partial V_T}{\partial V_{T0}}\Delta V_{T0} + \frac{\partial V_T}{\partial V_B}\Delta V_B \\
& = \Delta V_{T0} + \frac{-\gamma}{2\sqrt{2\phi_{FP} - V_B}}\Delta V_B
\end{aligned}
\tag{3.6}
$$

where γ is the body effect coefficient of M1 ($= \sqrt{2q\varepsilon_{si}N_{sub}} / C_{ox}$), ϕ_{FP} represents the Fermi potential ($= (kT/q)\ln(N_{sub}/n_i)$), and N_{sub} is the p-substrate concentration.

The V_T shift of M1 due to degradation of both M1 and M2 is thus modeled by the fluctuation of V_{T0} and V_B:

$$
\delta V_T = \delta V_{T0} - \frac{\gamma \cdot \delta V_B}{2\sqrt{2\phi_{FP} - V_B}}
\tag{3.7}
$$

Combining (3.4) and (3.7) yields the V_T variation.

$$\delta V_T = \delta V_{T0} - \frac{\gamma \cdot \delta V_T^{'}}{2\sqrt{2\phi_{FP} - V_B}}(1 - \frac{1}{\sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1}}) \tag{3.8}$$

The first term δV_{T0} in (3.8) represents the threshold voltage shift of M1, while the second term in (3.8) accomplishes the canceling effect resulting from the combination of V_T shift of M2 and the body bias circuit of M1. Thus, the overall V_T shift of M1 due to process variability and reliability degradation is reduced. The level of reduction is related to the $\delta V_T^{'}$ of M2, body effect coefficient γ, MOSFET structure coefficient β, and resistor R1. To achieve an optimum resilience to the reliability, it is better to choose larger R1 and M2 channel width.

3.2.2 Mobility Degradation

The mobility degradation results in a decrease in drain current. The drain current of M1 is simplified as $I_D \approx \beta(V_{GS} - V_T)^2 / 2$, where β variation due to mobility degradation is given by

$$\delta\beta = C_{ox} \frac{W}{L} \delta\mu_n \tag{3.9}$$

Clearly, β variation is linearly proportion to the electron mobility drift. The same relationship also applies to $\beta^{'}$. The node voltage V_B fluctuation due to mobility degradation is simplified as $\delta V_B \approx \frac{\partial V_B}{\partial \beta^{'}} \delta\beta^{'}$. Using (3.4) $\frac{\partial V_B}{\partial \beta^{'}}$ is derived below:

$$\frac{\partial V_B}{\partial \beta^{'}} = \frac{1}{(\beta^{'} R1)^2} \left(\frac{2R1(V_{DD} - V_{tune} - V_T^{'})\beta^{'} R1}{2\sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1}} - \right.$$

$$\left. \sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1} \cdot R1 \right)$$

$$= \frac{\beta^{'} R1^2 (V_{DD} - V_{tune} - V_T^{'}) - 2\beta^{'} R1^2 (V_{DD} - V_{tune} - V_T^{'}) - R1^{'}}{(\beta^{'} R1)^2 \sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1}} \tag{3.10}$$

$$= \frac{-R1(\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1)}{(\beta^{'} R1)^2 \sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1}}.$$

From the result in (3.10), one therefore finds δV_B as

$$\delta V_B = -\frac{R1(\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1)}{(\beta^{'} R1)^2 \sqrt{2\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) + 1}} \delta \beta^{'} \tag{3.11}$$

Assuming $\beta^{'} R1(V_{DD} - V_{tune} - V_T^{'}) >> 1$, (12) reduces to

$$\delta V_B \approx -\sqrt{\frac{V_{DD} - V_{tune} - V_T^{'}}{2\beta^{'3} R1}} \delta \beta^{'} \tag{3.12}$$

The threshold voltage variation in M1 due to body voltage fluctuation resulting from the mobility degradation in M2 is approximately as

$$\delta V_T \approx -\frac{\gamma \cdot \delta V_B}{2\sqrt{2\phi_{FP} - V_B}} \tag{3.13}$$

The drain current fluctuation subject to key transistor parametric drifts ($\delta\beta$ and δV_T) is given by

$$\delta I_D = \frac{\partial I_D}{\partial \beta} \delta \beta + \frac{\partial I_D}{\partial V_T} \delta V_T \tag{3.14}$$

In the derivation of $\frac{\partial I_D}{\partial \beta}$ and $\frac{\partial I_D}{\partial V_T}$, a simple drain current equation ($I_D \approx \frac{\beta}{2}(V_{GS} - V_T)^2$) is used. Thus,

$$\frac{\partial I_D}{\partial \beta} = \frac{1}{2}(V_{GS} - V_T)^2 \tag{3.15}$$

$$\frac{\partial I_D}{\partial V_T} = -\beta(V_{GS} - V_T) \tag{3.16}$$

Using (3.14), (3.15), and (3.16) one obtains the drain current variation as

$$\delta I_D = \frac{1}{2}(V_{GS} - V_T)^2 \delta\beta - \beta(V_{GS} - V_T)\delta V_T \tag{3.17}$$

Combining (3.7), (3.12), and (3.17), the fluctuation of drain current of M1 is expressed below

$$\delta I_D = \frac{1}{2}(V_{GS} - V_T)^2 \delta\beta - \beta(V_{GS} - V_T)\frac{\gamma\sqrt{\frac{V_{DD} - V_{tune} - V_T^{'}}{2\beta^{'3}R1}}\delta\beta^{'}}{2\sqrt{2\phi_{FP} - V_B}}. \tag{3.18}$$

Note that the variation $\delta\beta$ reflects the fluctuation resulting from the electron mobility degradation of M1. $\delta\beta^{'}$ represents the fluctuation caused by the electron mobility degradation of M2. The reduction of M1's mobility will decrease the drain current in M1, while the reduction of M2's mobility will increase the drain current in M1. To maximize the canceling effect, larger value of R1 as well as larger size of M2 are expected.

3.2.3 Tuning for Variability

The V_T shift of M1 due to Vtune change is described as follows. From (4) the body voltage values corresponding to the two different tuning voltages are determined by the equations in (3.19) and (3.20). Here the V_T of M2 is supposed to be constant.

$$V_{B1} = V_{tune1} + V_T^{'} + \frac{\sqrt{2\beta R1(V_{DD} - V_{tune1} - V_T^{'}) + 1} - 1}{\beta R1} \tag{3.19}$$

$$V_{B2} = V_{tune2} + V_T^{'} + \frac{\sqrt{2\beta R1(V_{DD} - V_{tune2} - V_T^{'}) + 1} - 1}{\beta R1} \tag{3.20}$$

where V_{tune1} and V_{tune2} represent the two different tuning voltages.

The threshold voltage of M1 under the two different Vtune voltages can be written as:

$$V_{T1} = V_{T0} + \gamma(\sqrt{2\phi_{FP} - V_{B1}} - \sqrt{2\phi_{FP}}) \tag{3.21}$$

$$V_{T2} = V_{T0} + \gamma(\sqrt{2\phi_{FP} - V_{B2}} - \sqrt{2\phi_{FP}}) \tag{3.22}$$

The difference between two tuning voltage is marked as ΔV_T.

$$\Delta V_T = V_{T2} - V_{T1} \tag{3.23}$$

Combining (3.21) to (3.23), the sensitivity of V_T in M1 due to the tuning voltage of the circuit is derived as

$$\Delta V_T = \gamma[(2\phi_{FP} - V_{B2})^{\frac{1}{2}} - (2\phi_{FP} - V_{B1})^{\frac{1}{2}}] \quad (3.24)$$

A complete expression of (3.24) is complicated when substituting V_{B1} and V_{B2} with (3.19) and (3.20). Using (3.24) and the PTM 65nm nMOSFET model parameters, the relationship between the threshold voltage and tuning voltage is calculated and plotted in Fig. 3.6.

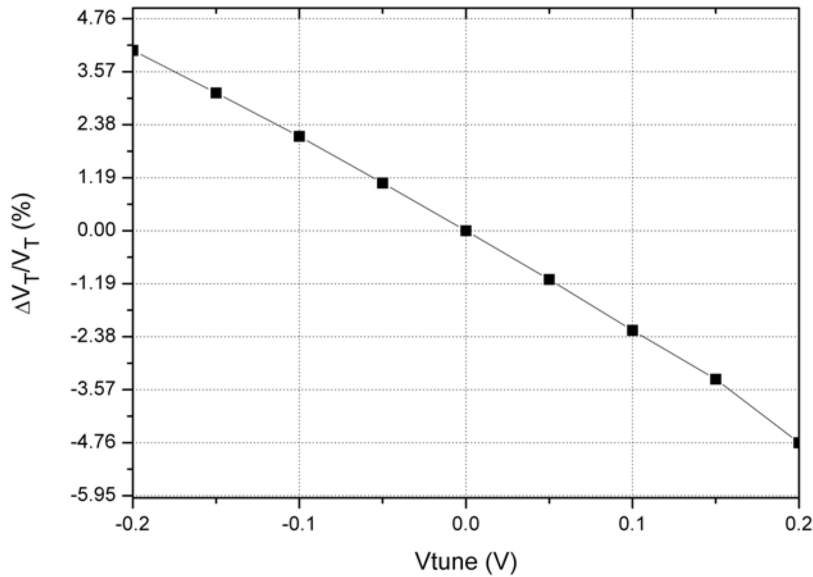


Figure 3. 6. Normalized V_T versus Vtune

The V_T of M1 decreases linearly from 4.05% to -4.76% as Vtune increases from -0.2 V to 0.2 V. This property can serve as post-fabrication calibration to compensate for the V_T deviation of M1 due to process variability.

3.3 Chapter Outline

The novel adaptive body biasing design scheme proposed in this chapter has the advantage of immediate fit into the state-of-art RF circuits. Unlike scheme proposed by other groups, the design does not affect the performance of the circuits. Further performance enhancement will be examined by evaluation of the typical RF transceiver circuits in the following chapters.

CHAPTER FOUR: RF CLASS-AB POWER AMPLIFIER DESIGN FOR VARIABILITY AND RELIABILITY

4.1 RF Class-AB Power Amplifier

Generally power amplifier (PA) can be classified by the operation mode of the transistor into seven categories: A, AB, B, C, D, E, F. Class A, AB, B, C are distinguished by their conduction angle. Class A PA has full conduction angle, while class B PA has only half or 180 degree conduction angle. Class AB PA has the angle between class A and class B. Class C PA has less than 180 degree conduction angle during the operation. It is reported [83, 84] that class A PA has the highest linearity performance while class C PA outputs highest power added efficiency. Class D, E, and F are switching mode PA [85-88]. Due to the linearity operation requirement of most commercial communication applications, class AB PA is the most popular one applied in the RF transceiver architecture for civil and commercial application, which compromises the power efficiency and linearity performance of power amplification.

4.1.1 Power Amplifier Performance Parameters

The most important parameters evaluating the performance of PA are gain, output power, power added efficiency (PAE), and third order intercept point (IP3). PAE is defined by (4.1).

$$PAE = 100 \cdot \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (4.1)$$

It differs from the most used efficiency description since it considers the input drive power level, which is important when gain is low.

The third-order intercept point (TOI) is an important parameter reflecting the device nonlinearity. When the signals passing the actual transistor are modulated sinusoidal voltage waveforms (e.g., RF PA), MOSFET nonlinearities can be expressed in terms of how they affect individual sine signal components. For example, say the input voltage is the sine wave.

$$V_{in}(t) = V\cos(\omega t) \tag{4.2}$$

The output signal can be written as

$$O[V_{in}(t)] = G \cdot V_{in}(t) - D_3 V_{in}^3(t) + \cdots \tag{4.3}$$

where cosine wave cubic can be expressed in (4.4)

$$\cos^3(t) = \frac{3}{4}\cos(t) + \frac{1}{4}\cos(3t) \tag{4.4}$$

The output wave is then deducted as (4.5)

$$O[V_{in}(t)] = (G \cdot V - \frac{3}{4}D_3 V^3)\cos(\omega t) - (D_3 \frac{V^3}{4})\cos(3\omega t) \tag{4.5}$$

The IIP3 point can be reached by equaling the first term to zero, that is the IP3 voltage for input signal as shown in (4.6). The IP3 is also illustrated in figure 4.1, which is the intercept point of first order output and third order output signal.

$$V^2 = \frac{4G}{3D_3} \qquad (4.6)$$

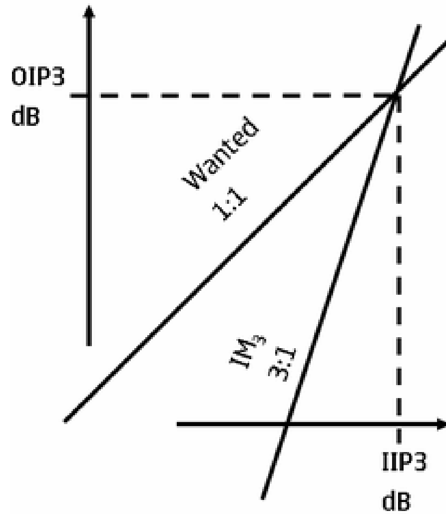


Figure 4. 1. IP3 illustration

4.1.2 Power Amplifier Design

A typical Class-AB PA is composed of input matching network, MOSFET transistor, and output matching network as presented in figure 4.2. The input matching network serves for the best input conjugate signal matching between input port and input terminal of MOSFET. The output matching network tries to deliver the maximum power to the load.

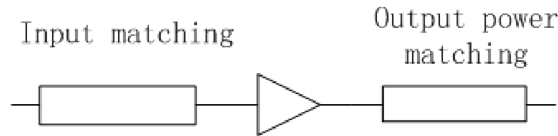
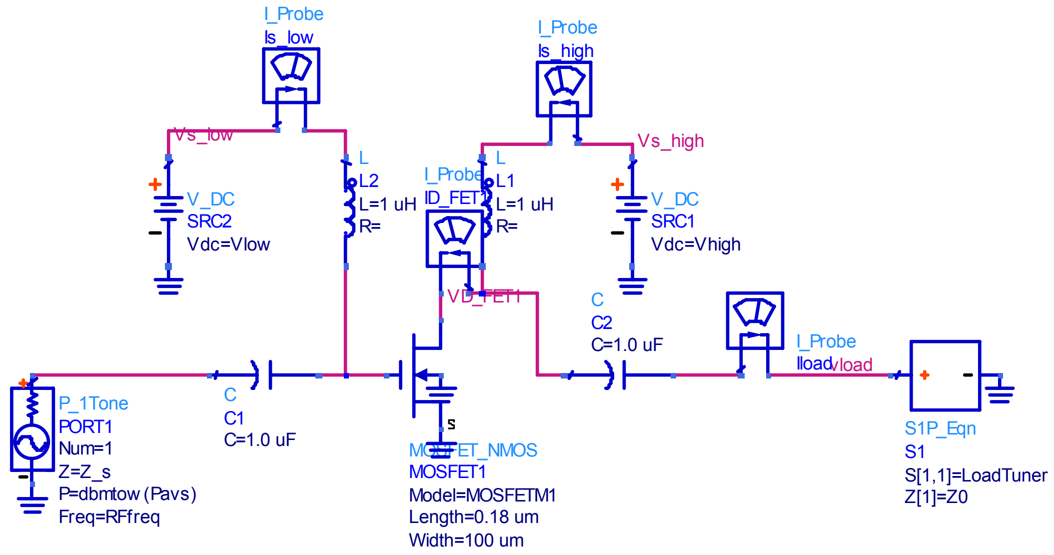
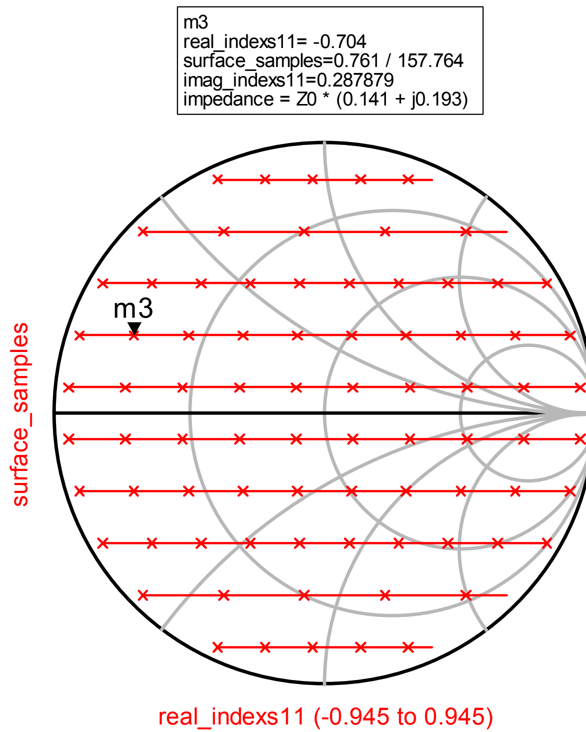


Figure 4. 2. PA stage description

The output matching network stage is usually tuned by load-pull instrument, which is achieved by automatically search the impedance value in the smith impedance chart. The corresponding PAE and output power contour are obtained by the load-pull instrument as displayed in the smith chart. One example procedure is described in figure 4.3. Figure 4.3 (a) shows a sample ADS circuit simulation setup for load pull instrument. The tuner will search the entire possible value in the smith chart as shown in Figure 4.3 (b). After the search and calculation, an output power and PAE contour plot are depicted in Figure 4.3 (c). Once the optimum point is selected, the load impedance is settled correspondingly. Constructing a load matching network that matches the calculated value will lead to the PA with optimum output power and PAE.



(a)



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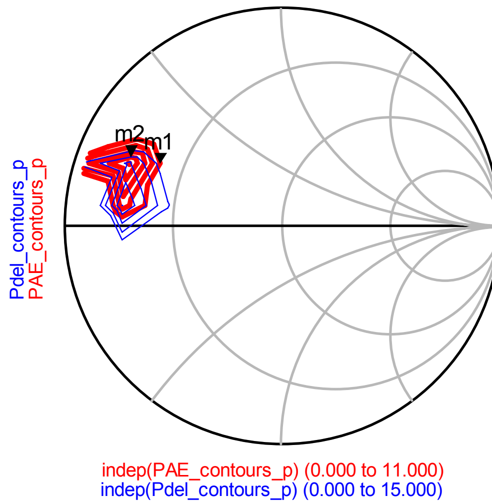


(c)

Figure 4. 3. Load-pull (a) ADS circuit setup; (b) search plane in smith chart; (c) PAE and output power contour

4.2 RF Power Amplifier Performance Sensitivity

Both the fabrication process-induced fluctuation and time-dependent degradation cause the MOSFET model parameter shifts. V_T is the most significant parameter for the

MOSFET suffering from variability and reliability degradations. Static post-fabrication calibration and dynamic V_T adjustment are considered using the resilient biasing design.

Fig. 4.4 shows a 24 GHz class-AB PA topology. The resilient biasing is circled in this plot. The output matching network is tuned using ADS load-pull instrument to obtain the optimum value. The 65 nm NMOS transistors are modeled by the PTM equivalent BSIM4 model card. The transistor sizes, capacitor and inductor values, and supply voltage are given in this figure.

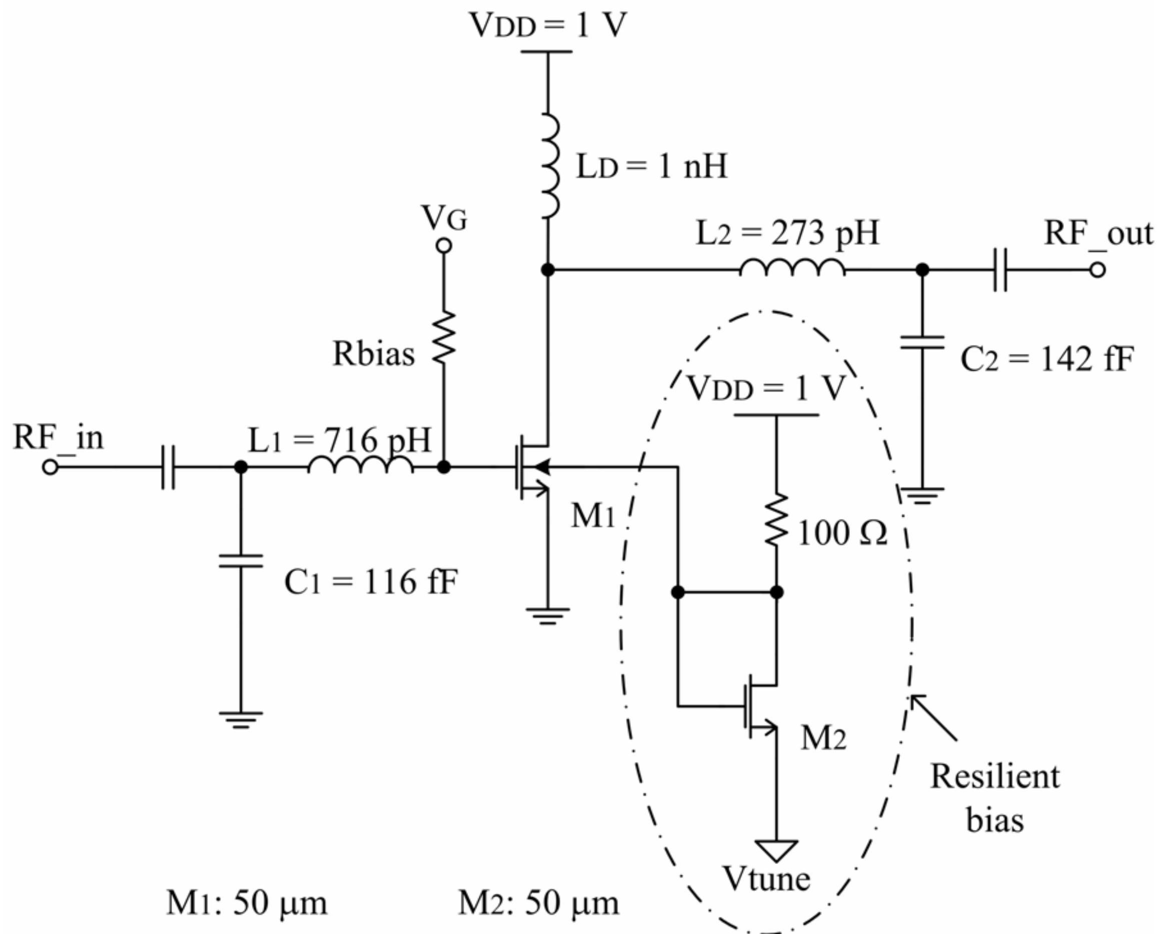
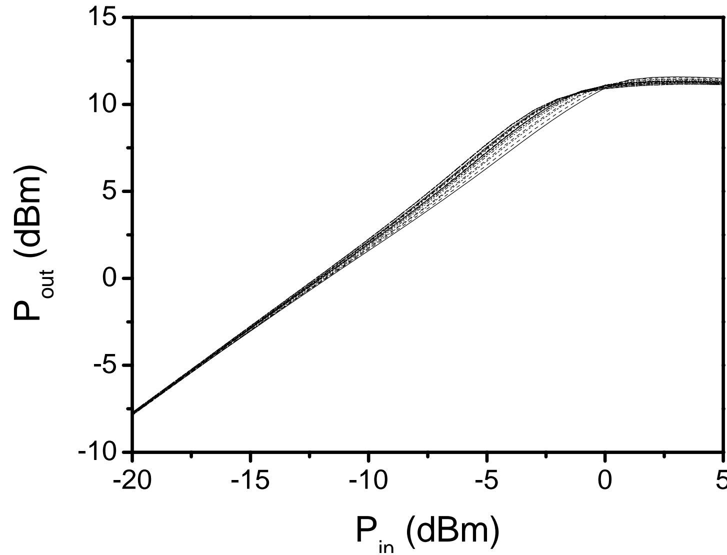


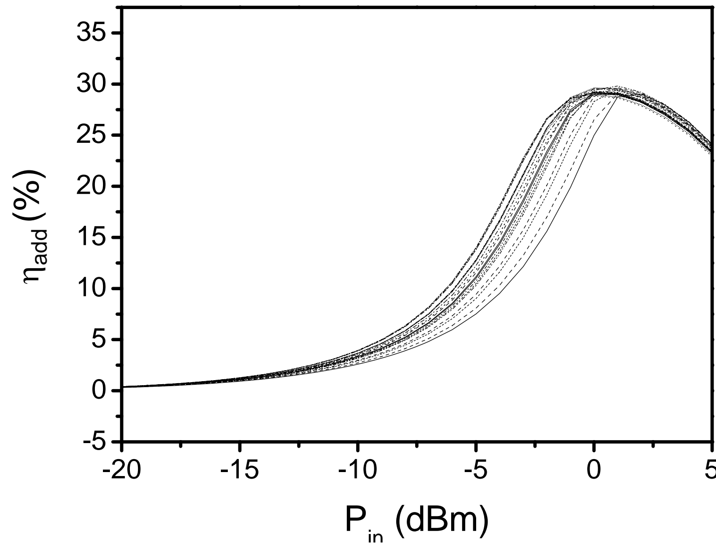
Figure 4. 4. Schematic of a 24 GHz class-AB power amplifier with resilient biasing

The P_{1dB}, P_{sat}, and η_{add} of the PA without resilient biasing are 10.28 dBm, 10.96 dBm, and 34.25%, while the corresponding values of the resilient design shown in Fig. 4.4 reach 10.95 dBm, 11.34 dBm, and 29.44%, respectively. The matching network remains the same between the two PA schematics.

Fig. 4.5 shows 20 overlapping samples of the output power and power-added efficiency variations due to process fluctuation. It is observed from the Monte Carlo simulations that a 10% of V_T spread (STD/Mean) will lead to 1.11% P_{sat} spread and 7.11% η_{add} spread. It is also seen from the simulation that the ±0.2 V lead to 1.38% ~ -1.37% P_{sat} deviation and 5.88% ~ -7.94% η_{add} spread. The ±0.25 V Vtune correspond to the 1.69% ~ -1.72% P_{sat} deviation and 7.29% ~ -10.20% η_{add} spread. So the spread fits into the compensation range of the ±0.25 V Vtune for post-process calibration.



(a)

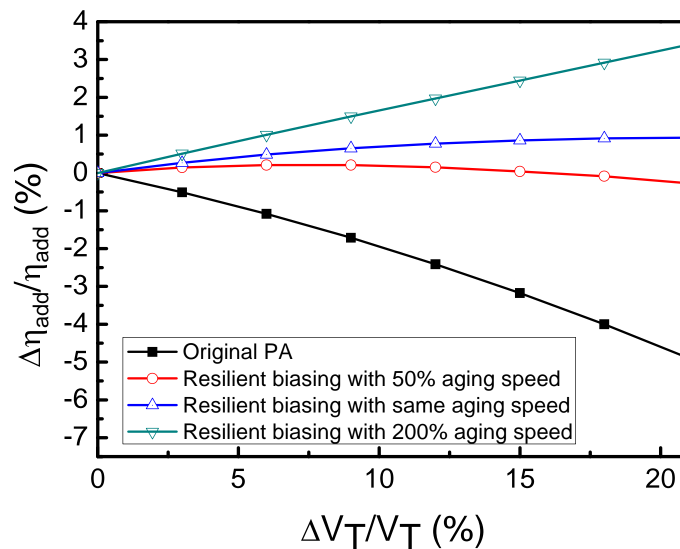


(b)

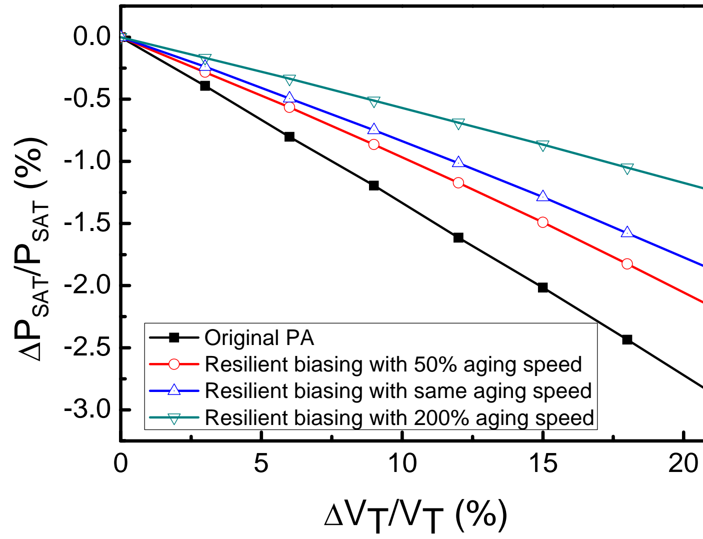
Figure 4. 5. PA performance fluctuation of (a) output power and (b) power-added efficiency versus input power

The power amplifiers with and without resilient biasing technique are compared. The drain-source voltage of MOS transistor M2 is around 0.5 V, which is half of the drain-source voltage of MOS transistor M1. Thus, the degradation rates of both transistors may be different. Thus the impact of mismatch between the degradation or aging rates of the two transistors is investigated. Fig. 4.6(a) shows normalized power-added efficiency to normalized threshold voltage variation under various aging rate. The resilient biasing reduces power-added efficiency of the whole PA due to the additional DC power consumption of the biasing circuit branch. But with the aging of the MOS transistor in the biasing circuit, the DC power of the biasing circuit branch reduces and the power-added efficiency boosts significantly. It is also noted that the accelerated aging

of MOS transistor M2 in the biasing circuit will lead to extra boosting of the power-added efficiency. For the normalized P_{sat} and P_{1dB} variations shown in Fig. 4.6(b) and Fig 4.6(c), the resilient biasing design reduces the sensitivity of P_{SAT} and P_{1dB} against the threshold voltage shift dramatically, especially for the output power at the 1dB compression point (e.g., $\Delta P_{1dB/}P_{1dB}$ reduces from about -12% to -2% at $\Delta V_T/V_T$ = 21%). Also the accelerated aging of MOS transistor M2 in the biasing circuit reduces the sensitivity of the normalized P_{sat} and P_{1dB}. Fig 4.6(d) shows the linearity performance of IIP3 sensitivity of the PA due to the threshold voltage shift. It is shown that the linearity sensitivity of PA is reduced by the increased degradation of M2. So for reliability degradation induced dynamic V_T shift, the resilient biasing design helps improve the reliability of the PA by cutting the sensitivity by three to four times for the normalized output power at 1dB compression point and power-added efficiency.



(a)



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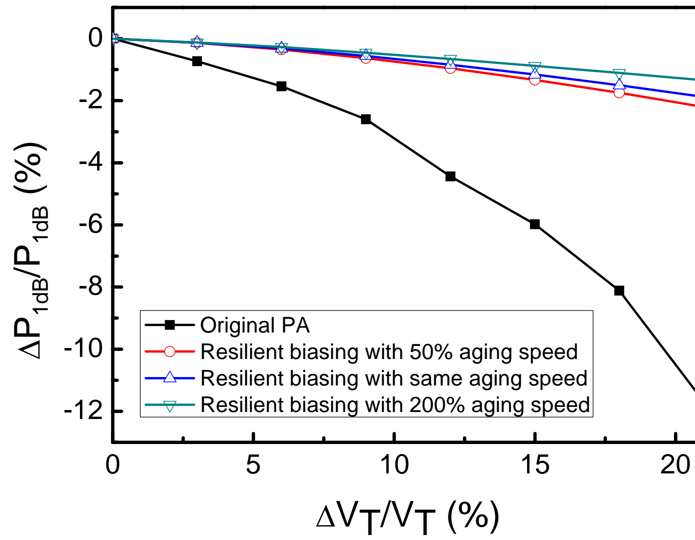

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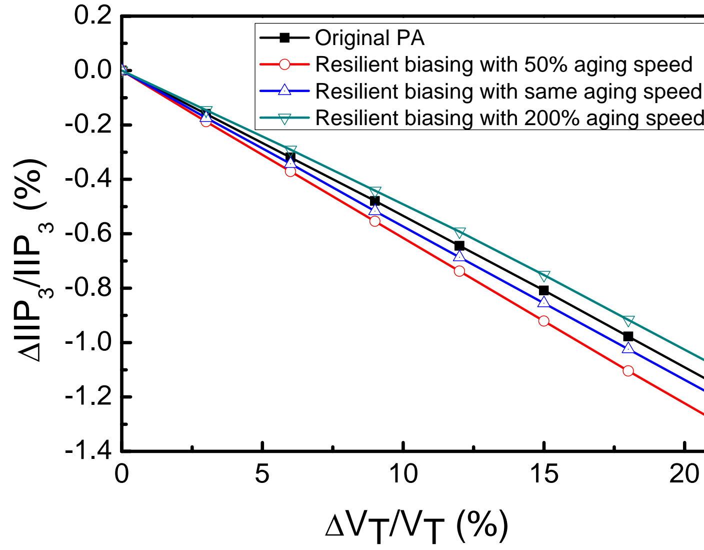
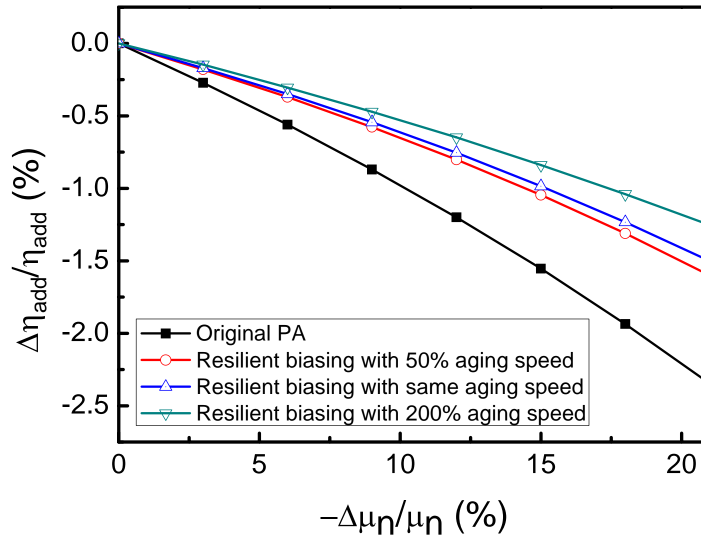


(d)

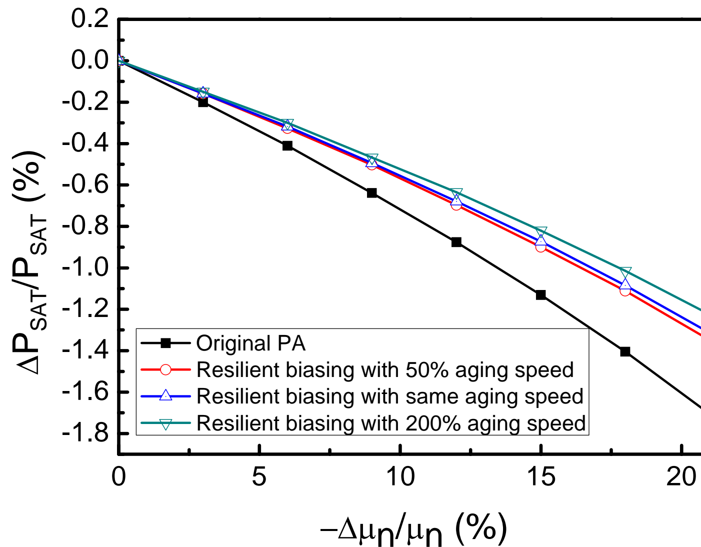
Figure 4. 6. Normalized (a) power-added efficiency variation, (b) P_{sat} , (c) P_{1dB} , and (d) IIP3 variation versus normalized V_T shift considered various MOS aging rate

The reliability degradation also reduces the electron mobility, which is another important parameter for drain current characteristic. Fig. 4.7(a) shows normalized power-added efficiency versus normalized electron mobility reduction for PA with and without resilient biasing design considered the degradation rate mismatches. The resilient biasing scheme reduces the sensitivity of normalized power-added efficiency by more than 25%. The faster aging of MOS transistor M2 in the biasing circuit is helpful in reducing the sensitivity of power-added efficiency and boosting the drain efficiency. Fig. 4.7(b) and (c) present the normalized P_{sat} and P_{1dB} variations versus normalized mobility shift under various aging speed. The resilient design reduces the sensitivity of P_{sat} and P_{1dB} by 34.7% and 83.9%, respectively. The accelerated degradation speed of MOS transistor M2 in biasing circuit also helps reduce the sensitivity of P_{sat} and P_{1dB} to the electron mobility

degradation. For IIP3 shown in Fig 4.7(d), it appears the similar trend with the effort in threshold voltage shift. The accelerated electron mobility degradation of MOS transistor M2 will lead to less sensitivity of the PA IIP3 or linearity. The resilient biasing design is obviously successful in reducing the power amplifier sensitivity against process variations and reliability degradations.



(a)



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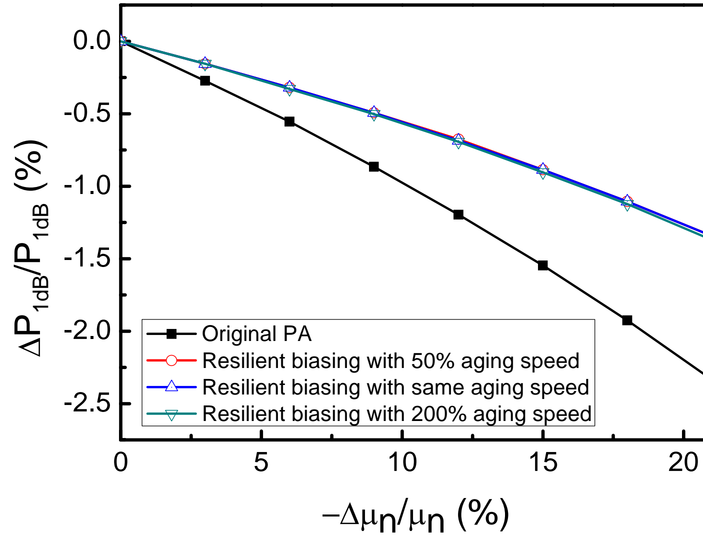

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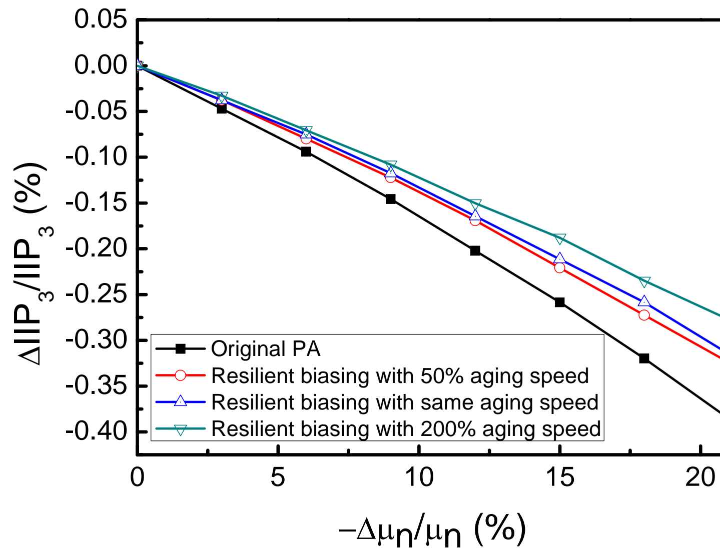


(d)

Figure 4. 7. Normalized (a) power-added efficiency, (b) P_{sat} , (c) P_{1dB} , and (d) IIP3 variation -8versus normalized mobility shift considered various MOS aging speed.

4.3 Chapter Outline

The novel resilient biasing design is applied to PA against process induced variability and time-dependent reliability problems. At the mean while, the novel resilient biasing design does not degrade PA performance. Analytical model of the resilient biasing is developed for design insight. A 24 GHz class-AB power amplifier with resilient biasing is compared with the PA without resilient biasing design. The RF circuit simulation results show that the resilient biasing design is capable for post-process calibration through small tuning range of voltage source. The adaptive scheme of the design makes the power-added efficiency and output power at the 1dB compression point much less sensitive to process- and stress-induced threshold voltage shifts. Also the impact of MOS transistors aging mismatches on the PA performance sensitivity is investigated. The accelerated degradation speed of MOS transistor in the biasing circuit is helpful in reducing the performance sensitivity of PA in most cases. The resilient biasing design makes the PA less sensitive to electron mobility shift for long term reliability.

CHAPTER FIVE: RF LOW NOISE AMPLIFIER RESILIENT DESIGN ANALYSIS

5.1 Low Noise Amplifier

In this chapter, we investigate the noise performance degradation of LNA. LNA is the sensing block placed at the front-end of the RF receiver circuit [89, 90], which amplifies the very weak input signal. Due to the weak input signal power level, the noise power is close to the signal power. LNA would add minimum noise to the source while amplify the signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system.

5.1.1 LNAPerformance Parameters

Noise figure (NF) and S21 are the major parameters evaluating the LNA performance. NF is a measure of degradation of the signal-to-noise ratio (SNR), caused by components in a RF signal chain. The noise figure is defined as the ratio of the output noise power of a device to the portion thereof attributable to thermal noise in the input termination at standard noise temperature T_0 (usually 290 K). The noise figure is thus the ratio of actual output noise to that which would remain if the device itself did not introduce noise. The NF definition can be viewed in the following equation.

$$NF = 10\log(\frac{SNR_{in}}{SNR_{out}}) = SNR_{in,dB} - SNR_{out,dB} \tag{5.1}$$

The NF is the noise factor (F) in dB:

$$NF = 10\log(F) \tag{5.2}$$

For cascading system, the total noise factor can be described by Friis's Formula.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_n} \tag{5.3}$$

where G_n is the power gain of the n-th device.

S21 is the forward transmission gain with the output port terminated by characteristic impedance of 50 Ω. For a 2-port system, the definition of S-parameters is described as the follows.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{5.4}$$

where a_n is the incident power wave; b_n is the reflected power wave.

The bigger S21 the larger the signal gain is obtain through the LNA stage. There are also other parameters like S11 in the design of LNA, which together will lead to optimized LNA topology.

5.1.2 Narrow Band LNA Topology

Simplified schematics of typical single-stage cascode LNA is shown in figure 5.1. The topologies utilize inductive degeneration for input matching to 50 Ω. Source

degenerated inductive matching has the benefit of low noise. At the mean time, source degeneration also improves the linearity by forming a negative series feedback.

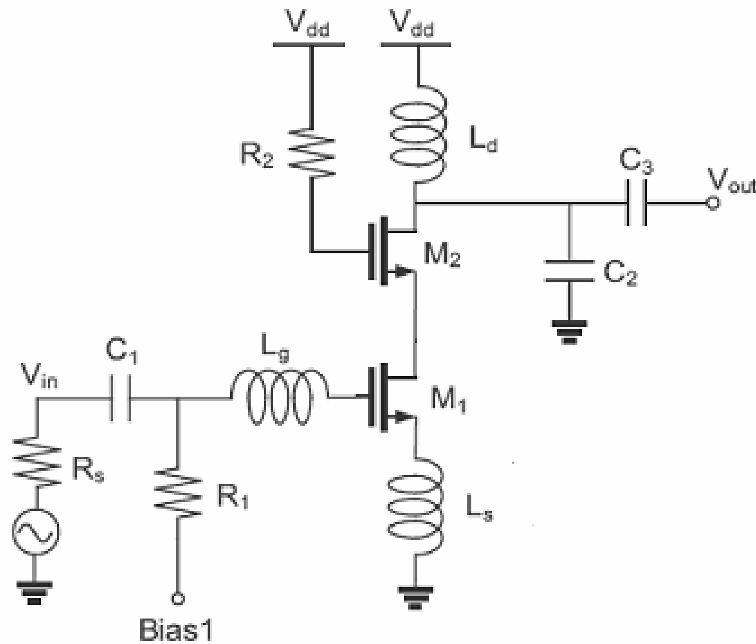


Figure 5. 1. Single-stage cascode LNA schematic

In single-stage LNA of figure 5.1, the impedance seen through the drain of M1 could be modeled by Rp in parallel with Cp, as shown in figure 5.2. At high frequencies, the parasitic capacitance at the drain node of M1 significantly reduces the overall impedance to ground and thus raises the noise contribution from cascode transistor. Ignoring Cgd, the input impedance Zin is given by

$$Z_{in} \cong \frac{1}{sC_{gs}} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs}} \tag{5.5}$$

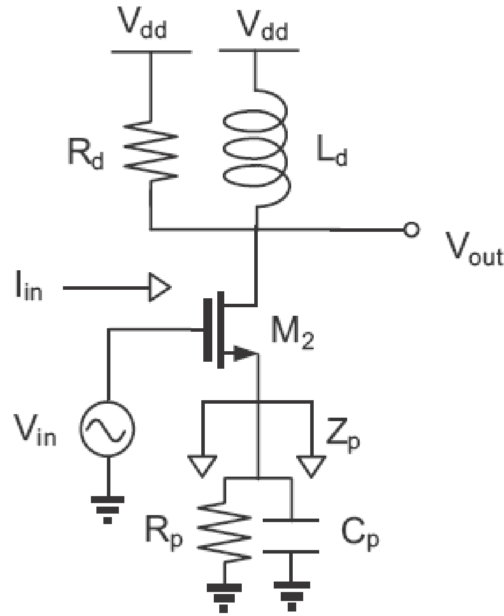


Figure 5. 2. Input impedance seen at the gate of the cascode transistor.

To improve the noise performance of the cascode design, the parasitic capacitance at the drain of M1 is resonated out by adding an inductor to the source of casode. This improves the noise performance of the cascode considerably, as shown in figure 5.1. This inductor should be sized carefully in order to resonate the unwanted capacitances at the desired frequency of operation.

There are also a lot of design guidelines for narrowband LNA such as power constrained LNA in Lee's book [91], which helps the understanding of LNA circuit.

5.2 LNA Resilient Design

5.2.1 Threshold Voltage Shift to Noise

The small fluctuation in transconductance will result in small variation in NFmin.

$$\delta NF_{\min} = -\pi K_f f (C_{gs} + C_{gd}) \sqrt{\frac{R_G + R_S}{g_m^3}} \cdot \delta g_m \tag{5.6}$$

Transconductance of transistor is

$$g_m = \beta (V_{GS} - V_T) \tag{5.7}$$

$\beta = u_n \cdot C_{ox} \frac{W}{L}$ is MOSFET structure dimension and material related coefficient marked here for simplification.

The transistor transconductance small variation caused by small variation of V_T is given in (5.8).

$$\delta g_m = -\beta \cdot \delta V_T \tag{5.8}$$

Combining (5.6) and (5.8), the small variation in V_T will lead to NFmin fluctuation.

$$\delta NF_{\min} = \pi \cdot \beta \cdot K_f \cdot f (C_{gs} + C_{gd}) \cdot \sqrt{\frac{R_G + R_S}{g_m^3}} \cdot \delta V_T \tag{5.9}$$

The KCL to solve 'VB' can be listed as (5.10) and (5.11). All the variables can be referenced from circuit schematic in figure 1.

$$I_{R1} = \frac{\beta}{2}(V_B - V_{GND} - V_T^{'})^2 \tag{5.10}$$

$$I_{R1} \cdot R1 + V_B = V_{DD} \tag{5.11}$$

where $V_T^{'}$ is the V_T of 'M2'.

From (5.10) and (5.11), node voltage V_B is solved.

$$\frac{\beta \cdot R1}{2}(V_B - V_{GND} - V_T^{'})^2 + V_B = V_{DD} \tag{5.12}$$

$$V_B = V_{tune} + V_T^{'} + \frac{\sqrt{2\beta \cdot R1(V_{DD} - V_{GND} - V_T^{'}) + 1} - 1}{\beta \cdot R1} \tag{5.13}$$

The small shift of $V_T^{'}$ will cause fluctuation in V_B as solved in previous equation.

$$\delta V_B = \delta V_{T1}^{'} - \frac{\delta V_{T1}^{'}}{\sqrt{2\beta \cdot R1(V_{DD} - V_{GND} - V_{T1}^{'}) + 1}} \tag{5.14}$$

Due to the body effect, the V_T of 'M1' can be described by (5.15).

$$V_T = V_{T0} + \gamma\sqrt{2\phi_{FP} - V_B} \tag{5.15}$$

where $\gamma = \sqrt{2q\varepsilon_{si}N_{sub}} / C_{ox}$ is body effect coefficient of 'M1'; $\phi_{FP} = \frac{kT}{q}\ln\frac{N_{sub}}{n_i}$ represents Fermi potential; N_{sub} is the p-substrate doping concentration.

The V_T shift of 'M1' due to degradation of both 'M1' and 'M2' transistor can be modeled by variable V_{T0} and V_B from (5.15).

$$\delta V_T = \delta V_{T0} - \frac{\gamma \cdot \delta V_B}{2\sqrt{2\phi_{FP} - V_B}} \tag{5.16}$$

Combining (5.13) and (5.16), the V_T shift approximation can be described.

$$\delta V_T = \delta V_{T0} - \frac{\gamma \cdot \delta V_T^{'}}{2\sqrt{2\phi_{FP} - V_B}} \cdot \left(1 - \frac{1}{\sqrt{2\beta \cdot R1(V_{DD} - V_{GND} - V_{T1}^{'}) + 1}}\right) \tag{5.17}$$

The first term δV_{T0} in (5.17) represents the V_T shift of 'M1' while the second term achieves the canceling effect resulting from the combination of V_T shift of 'M2' and the body bias circuit design. So the overall V_T shift of MOSFET 'M1' due to reliability degradation is reduced. The reduction in the V_T shift of 'M1' or the second term is related to the 'M2' V_T shift $\delta V_T^{'}$, body effect coefficient γ, and MOSFET structure coefficient β, and resistor R1. To make the second term bigger in order to achieve optimum resilience to the reliability, it is better to choose larger R1 resistance and 'M2' size. It is also observed that the more sever the 'M2' is degraded, the smaller the overall V_T shifts. From (5.17), the smaller overall V_T shifts will lead to the smaller NFmin fluctuation.

5.2.2 Mobility Degradation to Noise

The μn shift will result in the drain current variations. The drain current fluctuation will also cause small variation in transistor transconductance.

$$\delta g_m = \frac{g_m}{2 \cdot I_D} \cdot \delta I_D \tag{5.18}$$

So NFmin can be affected by the μ_n seen from (5.6), (5.7), and (5.18). In order to minimize the fluctuation of NFmin, drain current variation need to be minimized.

The drain current of 'M1' can be written as

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{5.19}$$

where β variation due to μn degradation is

$$\delta\beta = C_{ox}\frac{W}{L} \cdot \delta\mu_n \tag{5.20}$$

Thus β is linearly proportion to the μn. The mobility degradation of 'M2' will cause node voltage V_B fluctuation observed from (5.13).

$$\delta V_B = -\frac{R1(\beta' \cdot R1(V_{DD} - V_{GND} - V'_{T1}) + 1)}{\sqrt{2\beta' \cdot R1(V_{DD} - V_{GND} - V'_{T1}) + 1}} \cdot \delta\beta' \tag{5.21}$$

With assumption of

$\beta' \cdot R1(V_{DD} - V_{GND} - V'_{T1}) >> 1$

(5.21) can be simplified into

$$\delta V_B = -R1 \cdot \sqrt{\frac{\beta' \cdot R1(V_{DD} - V_{GND} - V'_{T1})}{2}} \cdot \delta\beta' \tag{5.22}$$

According to (5.16), the node voltage fluctuation leads to the V_T fluctuation of 'M1'.

$$\delta V_T = -\frac{\gamma \cdot \delta V_B}{2\sqrt{2\phi_{FP} - V_B}} \tag{5.23}$$

Thus mobility degradation of 'M1' and 'M2' will cause drain current fluctuation.

$$\delta I_D = \frac{\delta\beta}{2}(V_{GS} - V_T)^2 - \beta(V_{GS} - V_T) \cdot \delta V_T \tag{5.24}$$

Combining (5.22), (5.23), and (5.24), the fluctuation of drain current of 'M1' can be expressed in (5.25).

$$\delta I_D = \frac{\delta\beta}{2}(V_{GS} - V_T)^2 - \beta(V_{GS} - V_T) \cdot \frac{\gamma \cdot R1 \cdot \sqrt{\frac{\beta' \cdot R1(V_{DD} - V_{GND} - V_{T1}')}{2}} \cdot \delta\beta'}{2\sqrt{2\phi_{FP} - V_B}} \tag{5.25}$$

where the structure coefficient variation $\delta\beta$ reflects fluctuation caused by n degradation of 'M1'; $\delta\beta'$ reflects the fluctuation caused by electron mobility degradation of 'M2'.

Thus, these two variables change the drain current in opposite directions. The reduction of 'M1' n will decrease the current, while the reduction of 'M2' μn will increase the current according to (5.25). To maximize the canceling effect, large R1 and 'M2' size is expected. This is the same effort in maximizing the resilience to V_T degradation. So the adaptive body biasing design works for both device parameter degradations.

5.3 Small Signal Analysis

5.3.1 Minimum Noise Figure

The noise factor is a measure of the degradation in signal-to-noise ratio that a system introduces. Equation (5.26) expresses the noise factor defined in the two-port network with noise sources and a noiseless circuit [91]. The noise figure is the noise factor expressed in decibels. The noise factor is written as

$$F = \frac{\overline{i_s^2} + \overline{\left| i_n + (Y_c + Y_s) e_n \right|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_n^2} + | Y_c + Y_s |^2 \, \overline{e_n^2}}{\overline{i_s^2}} \tag{5.26}$$

where i_s is the noise current from the source, Y_s is the source admittance, i_n is the device noise current, e_n is the device noise voltage, and Y_c is the correlation admittance.

For n-channel MOS transistor M1 at high frequency, the small-signal equivalent circuit model with noise currents is displayed in Fig. 5.3. The $1/f$ flicker noise is ignored at high frequency. The nMOSFET consists of the drain current noise and gate noise. The drain current noise and gate noise in Fig. 5.3 can be written as [92, 93]

$$\overline{i_{nd1}^2} = 4kT\gamma_1 g_{d01} \Delta f \tag{5.27}$$

$$\overline{i_{ng1}^2} = 4kT\theta \frac{\omega^2 C_{gs1}^2}{5 g_{d01}} \Delta f \tag{5.28}$$

where k is the Boltzmanns' constant, T is the absolute temperature, ω is the radian frequency, g_{d01} is the output conductance of M1, C_{gs1} is the gate-source capacitance of

M1, Δf is the offset frequency, $\gamma_1 = 2/3$ for long channel MOSFET and can be 2 to 3 times larger in short-channel devices, and θ is the gate noise coefficient.

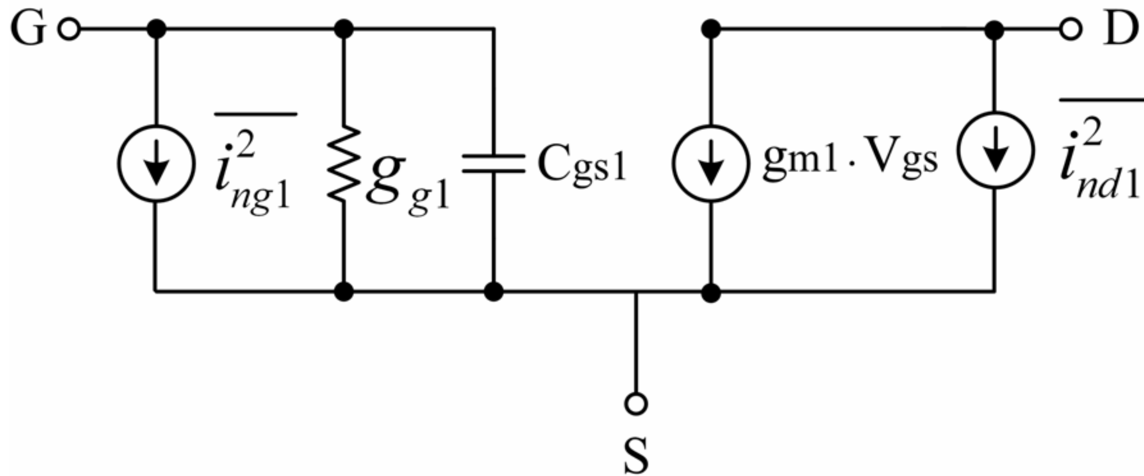


Figure 5. 3. nMOSFET noise model

For the DFR biasing circuit, the drain of nMOSFET M2 is shorted to its gate as seen in Fig. 5.4. Thus, the noise looking into the node B consists of the two noise sources R1 and M2 drain current noise. The resistor R1 thermal noise and M2 drain current noise are modeled as:

$$\overline{i_{R1}^2} = 4kT\frac{1}{R1}\Delta f \tag{5.29}$$

$$\overline{i_{nd2}^2} = 4kT\gamma_2 g_{d02}\Delta f \tag{5.30}$$

where g_{d2} is the output conductance of M2. Thus, the total mean squared noise voltage is

$$\overline{e_{B1}^2} = 4kT \frac{R1}{1 + R1\gamma_2 g_{d02}} \Delta f \ . \tag{5.31}$$

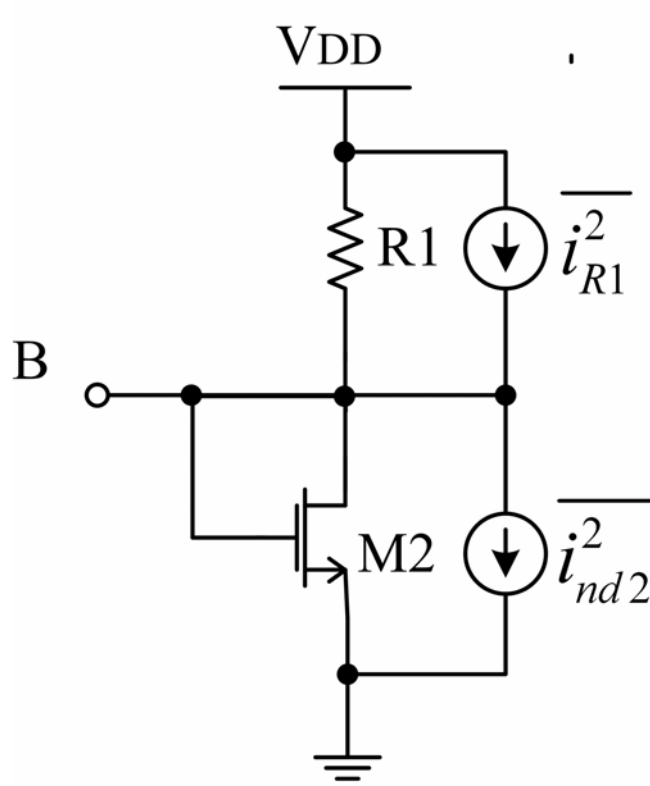


Figure 5. 4. DFR biasing circuit noise model

The reflected drain current noise due to noise voltage in the body node is determined by a ratio of body transconductance g_{mb1}.

$$\overline{i_{nB1}^2} = 4kT \frac{R1}{1 + R1\gamma_2 g_{d02}} g_{mb1}^2 \Delta f \tag{5.32}$$

Due to the body effect of M1, the drain current noise is a combination of noise originated from the drain current and reflected from the body node B.

$$\overline{i_{n1}^2} = \overline{i_{nB1}^2} + \overline{i_{nd1}^2} = 4kT\left[\frac{R1}{1+R1\gamma_2 g_{d02}} g_{mb1}^2 + \gamma_1 g_{d01}\right]\Delta f \tag{5.33}$$

The noise can be reflected back to the input gate of M1 by g_{m1}.

$$\overline{e_{n1}^2} = \frac{\overline{i_{n1}^2}}{g_{m1}^2} = 4kT\left[\frac{R1}{1+R1\gamma_2 g_{d02}} \frac{g_{mb1}^2}{g_{m1}^2} + \frac{\gamma_1 g_{d01}}{g_{m1}^2}\right]\Delta f \tag{5.34}$$

The equivalent input noise voltage is completely correlated with the drain current noise. Thus, the noise resistance is

$$R_{n1} = \frac{\overline{e_{n1}^2}}{4kT\Delta f} = \frac{R1}{1+R1\gamma_2 g_{d02}} \frac{g_{mb1}^2}{g_{m1}^2} + \frac{\gamma_1 g_{d01}}{g_{m1}^2} \tag{5.35}$$

The equivalent input noise voltage generator by itself does not fully account for the drain current noise. A noisy drain current also flows when the input is open-circuited. Under this condition, the equivalent input voltage obtained from dividing the drain current noise by the transconductance. When multiplying the input admittance, $\overline{e_{n1}^2}$ gives an equivalent input current noise as

$$\overline{i_{n1'}^2} = \overline{e_{n1}^2}(j\omega C_{gs1})^2 \tag{5.36}$$

Here, it is assumed that the input admittance of M1 is purely capacitive, which is good approximation when the operating frequency is below the cutoff frequency.

The drain noise and gate noise of M1 is correlated with a correlation coefficient c_1 defined as

$$c_1 = \frac{\overline{i_{ng1} \cdot i_{n1}^*}}{\sqrt{\overline{i_{ng1}^2} \cdot \overline{i_{n1}^2}}} \tag{5.37}$$

The total equivalent input current noise consists of the reflected drain noise and the induced gate current noise. The induced gate noise current itself has two parts. One part, i_{ngc1}, is fully correlated with the drain current noise of M1, while the other, i_{ngu1}, is uncorrelated with the drain current noise. The correlation admittance is expressed as follows:

$$\begin{aligned} Y_c &= \frac{i_{n1'} + i_{ngc1}}{e_{n1}} = j\omega C_{gs1} + \frac{i_{ngc1}}{e_{n1}} \\ &= j\omega C_{gs1} + g_{m1} \frac{i_{ngc1}}{i_{n1}} \end{aligned} \tag{5.38}$$

The last term must be manipulated in terms of cross-correlations by multiplying both numerator and denominator by the conjugate of the drain current noise:

$$g_{m1} \frac{i_{ngc1}}{i_{n1}} = g_{m1} \frac{\overline{i_{ngc1} \cdot i_{n1}^*}}{\overline{i_{n1} \cdot i_{n1}^*}} = g_{m1} \frac{\overline{i_{ng1} \cdot i_{n1}^*}}{\overline{i_{n1}^2}} \tag{5.39}$$

Using the above equation, the correlation admittance can be rewritten as

$$\begin{aligned} Y_c &= j\omega C_{gs1} + g_{m1} \frac{\overline{i_{ng1} \cdot i_{n1}^*}}{\overline{i_{n1}^2}} \\ &= j\omega C_{gs1} + g_{m1} \frac{\overline{i_{ng1} \cdot i_{n1}^*}}{\sqrt{\overline{i_{ng1}^2}}\sqrt{\overline{i_{n1}^2}}} \sqrt{\frac{\overline{i_{ng1}^2}}{\overline{i_{n1}^2}}} = j\omega C_{gs1} + g_{m1} c_1 \sqrt{\frac{\overline{i_{ng1}^2}}{\overline{i_{n1}^2}}} \end{aligned} \tag{5.40}$$

Inserting (5.28) and (5.33) into (5.40) yields

$$
\begin{aligned}
Y_c &= j\omega C_{gs1} + g_{m1} c_1 \sqrt{\frac{\theta}{\frac{R1}{1+R1\gamma_2 g_{d02}} \frac{g_{mb1}^2 5 g_{m1}^2}{\omega^2 C_{gs1}^2} + \gamma_1 g_{d01} \frac{5 g_{m1}^2}{\omega^2 C_{gs1}^2}}} \\
&= j\omega C_{gs1} + \omega C_{gs1} \frac{c_1}{\sqrt{5}} \sqrt{\frac{\theta}{\frac{R1 g_{mb1}^2}{1+R1\gamma_2 g_{d02}} + \gamma_1 g_{d01}}}
\end{aligned}
\tag{5.41}
$$

Note that the correlation coefficient c_1 is purely imaginary [91]. Thus, G_c (the real part of Y_c) equals zero. Using the definition of the correlation coefficient, the expression of the gate induced noise is written as

$$
\overline{i_{ng1}^2} = \overline{(i_{ngc1} + i_{ngu1})^2} = 4kT\Delta f \left(\frac{\theta\omega^2 C_{gs1}^2 |c_1|^2}{5 g_{d01}} + \frac{\theta\omega^2 C_{gs1}^2 (1-|c_1|^2)}{5 g_{d01}} \right). \tag{5.42}
$$

Thus, the uncorrelated portion of the gate noise is

$$
G_{u1} = \frac{\overline{i_{u1}^2}}{4kT\Delta f} = \frac{\theta\omega^2 C_{gs1}^2 (1-|c_1|^2)}{5 g_{d01}}. \tag{5.43}
$$

The minimum noise figure is given by

$$
\begin{aligned}
F_{\min} &= 1 + 2R_{n1}\left[G_{opt} + G_c\right] \approx 1 + 2R_{n1}\sqrt{\frac{G_{u1}}{R_{n1}}} \\
&= 1 + \frac{2}{\sqrt{5}} \frac{\omega C_{gs1}}{g_{m1}} \sqrt{\theta(1-|c|^2)\left[\frac{R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]}
\end{aligned}
\tag{5.44}
$$

Using (5.44) the minimum noise figure fluctuation is derived as

$$\Delta F_{\min} = -\frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}^2}\sqrt{\theta(1-|c|^2)\left[\frac{R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02})g_{d01}}+\gamma_1\right]}\Delta g_{m1}$$

$$+\frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1-|c|^2)R1 g_{mb1}}{(1+R1\gamma_2 g_{d02})g_{d01}\sqrt{\theta(1-|c|^2)\left[\frac{R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02})g_{d01}}+\gamma_1\right]}}\Delta g_{mb1}$$

$$-\frac{1}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1-|c|^2)R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02})g_{d01}{}^2\sqrt{\theta(1-|c|^2)\left[\frac{R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02})g_{d01}}+\gamma_1\right]}}\Delta g_{d01}$$

$$-\frac{1}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1-|c|^2)R1 g_{mb1}^2 R1\gamma_2}{(1+R1\gamma_2 g_{d02})^2 g_{d01}\sqrt{\theta(1-|c|^2)\left[\frac{R1 g_{mb1}^2}{(1+R1\gamma_2 g_{d02})g_{d01}}+\gamma_1\right]}}\Delta g_{d02} \tag{5.45}$$

In (5.45) the second term leads to the reduction of minimum noise figure sensitivity due to the body effect of MOSFET M1.

5.3.2 Small-Signal Gain

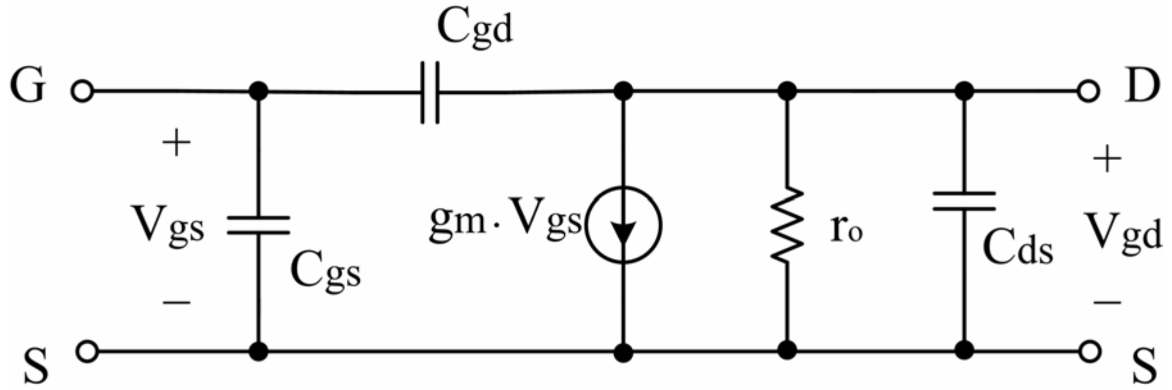
Small-signal gain S_{21} is related to the transconductance and gate-drain capacitance of M1. A detailed derivation of small-signal model is given in the following.

$$S_{21} = \frac{-2Y_{21}\sqrt{Z_{01}Z_{02}}}{\Delta_1} \tag{5.46}$$

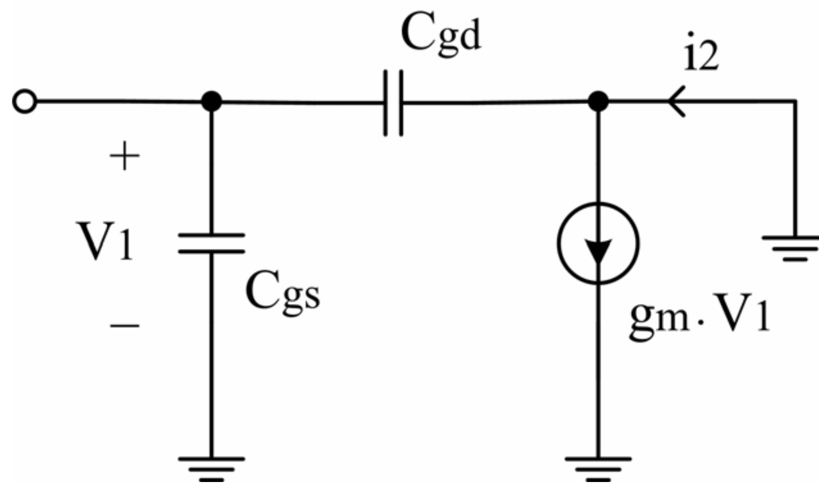
$$\Delta_1 = (1+Y_{11}Z_{01})(1+Y_{22}Z_{02}) - Y_{21}Z_{01}Y_{12}Z_{02} \tag{5.47}$$

In the following discussion, we will see how Y_{21} fluctuates due to transconductance variation. Firstly, high frequency small-signal model for nMOSFET is

shown in Fig 5.5(a). When the node D is tied to the ground terminal S, Fig. 5.5(a) reduces to Fig. 5.5(b).



(a)



(b)

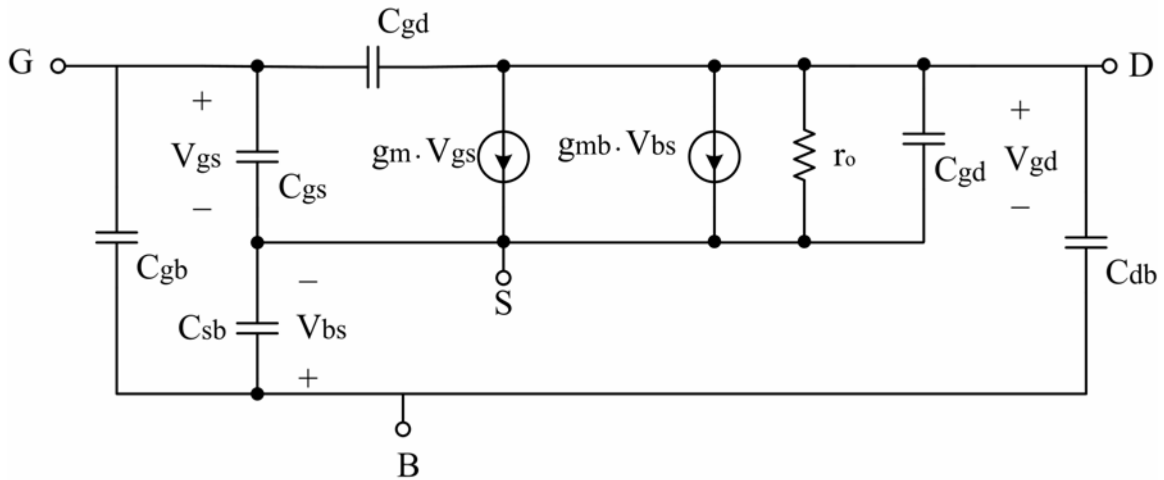
Figure 5. 5. (a) High frequency small-signal model of nMOSFET; (b) simplified equivalent circuit for *Y21* derivation.

Y_{21} for single nMOSFET without body effect is derived from Fig. 5.5(b). In Fig. 5.5 V_1 refers to Vgs in terminal 1 (between G and S) and V_2 refers to Vgd in terminal 2 (between D and S). Using Fig. 5.5(b) Y_{21} without body biasing is given by

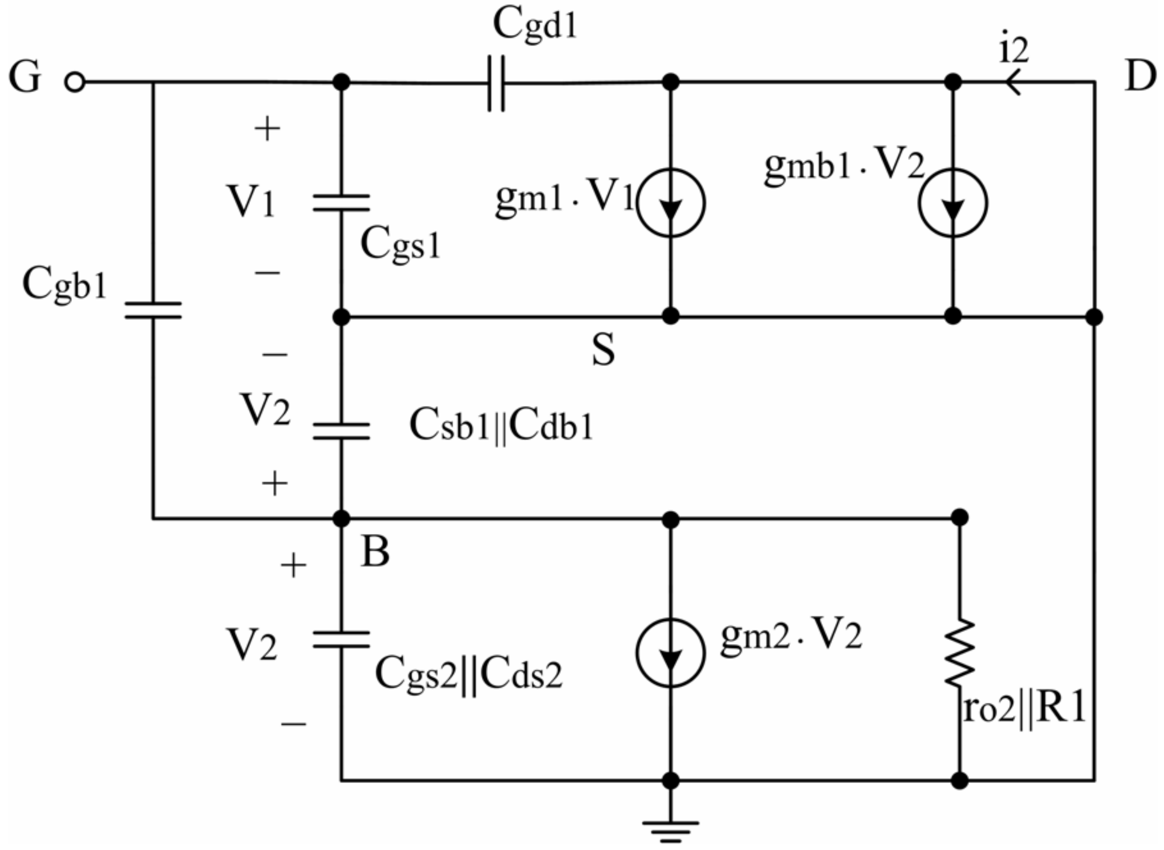
$$Y_{21}(f) = \frac{i_2(f)}{V_1(f)}|_{V_2=0} = -j\omega C_{gd} + g_m \tag{5.48}$$

Thus, the transconductance fluctuation results in Y_{21} variation:

$$\Delta Y21(f) = \Delta g_m \tag{5.49}$$



(a)



(b)

Figure 5. 6. (a) High frequency small-signal model of nMOSFET with body terminal and (b) small-signal model for Y_{21} derivation including substrate biasing circuit.

Fig. 5.6(a) shows small-signal model for nMOSFET with body bias terminal. When D of M1 is tied to ground with S of both M1 and M2 in the substrate biasing circuit in Fig. 1, a simplified equivalent circuit model is displayed in Fig. 5.6(b). Using Fig. 5.6(b) one can write the current i_2

$$i_2 = g_m V_1 + g_{mb1} V_2 - V_1 j\omega C_{gd1}. \tag{5.50}$$

At the node B in Fig. 5.6(b) the KCL equation results in

$$V_2 j\omega(C_{sb1} + C_{db1}) + V_2 j\omega(C_{gs2} + C_{ds2}) + g_{m2}V_2 + \frac{V_2}{R1 \| r_{o2}} = (V_1 - V_2) j\omega C_{gb1} \tag{5.51}$$

Combining (5.50) and (5.51), Y_{21} is obtained:

$$Y_{21}(f) = \frac{i_2(f)}{V_1(f)}|_{V_2'=0} = -j\omega C_{gd1} + g_{m1} + \frac{j\omega C_{gb1} g_{mb1}}{j\omega C_{tot} + g_{m2} + \frac{1}{R1\|r_{o2}}} \tag{5.52}$$

where $C_{tot} = C_{sb1} + C_{db1} + C_{gs2} + C_{ds2}$.

Note that $V_{2'}$ in (5.52) represents what V_2 means in (5.48).

From (5.53) one can derive the fluctuation of Y_{21} as a function of g_{m1}, g_{mb1}, and g_{m2} as

$$\Delta Y_{21}(f) = \Delta g_{m1} - \frac{j\omega C_{gb1} g_{mb1}}{(j\omega C_{tot} + g_{m2} + \frac{1}{R1\|r_{o2}})^2} \Delta g_{m2} + \frac{j\omega C_{gb1}}{j\omega C_{tot} + g_{m2} + \frac{1}{R1\|r_{o2}}} \Delta g_{mb1} \tag{5.53}$$

The second term in (5.53) will reduce Y_{21} sensitivity due to M2 in the DFR design. However, the third term in (5.53) due to the body effect of M1 will increase the fluctuation of Y_{21}. Thus, the transconductance of M2 helps reduce Y_{21} sensitivity, while the body transconductance of M1 may degrade Y_{21} sensitivity. Examining (5.45) and (5.53) together, the best sensitivity of noise figure and small-signal gain subject to body bias cannot be obtained simultaneously.

5.4 LNA Degradation Resilience

A narrow-band cascode LNA designed at 24 GHz with adaptive body biasing is shown in Fig. 5.7. The main input transistor (M1) is connected with source degenerated inductor for better input matching and noise reduction. The cascode transistor (M3) provides the output to input isolation. All n-channel transistors are modeled using the PTM 65 nm technology [12]. The inductor values, MOS channel widths, and R1 are given in Fig. 5.7. V_{DD} = 1.0 V, V_{bias} = 0.7 V, and R_{bias} = 5 kΩ. The NF, NF_{min}, and S_{21} of the LNA without resilient biasing are 1.414 dB, 1.226 dB, and 12.124 dB at 24 GHz, while the corresponding values of the resilient design are 1.369 dB, 1.327 dB, and 11.531 dB, respectively.

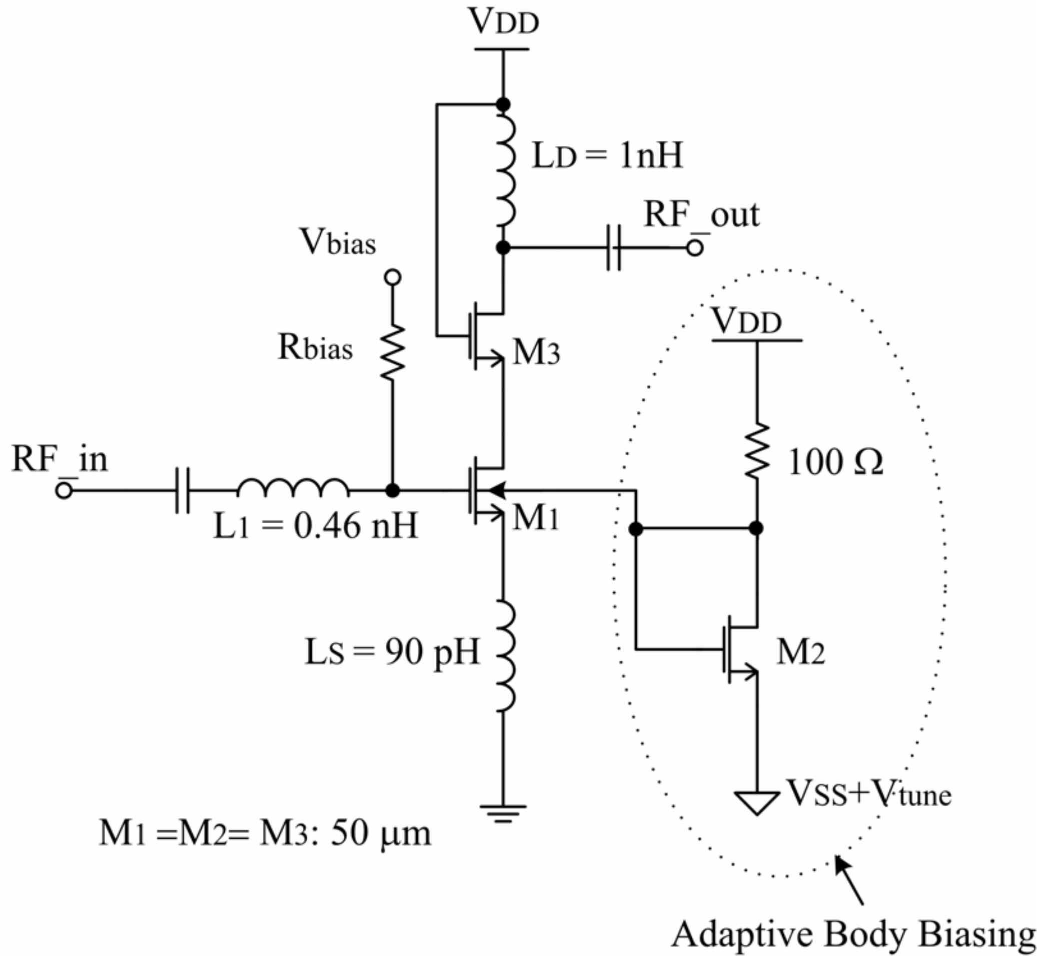


Figure 5. 7. A cascode low-noise amplifier with adaptive substrate biasing

Figs. 5.8 and 5.9 and show Monte Carlo simulation of the *NF*, NF_{min}, and S_{21} sensitivity subject to process variability. Monte Carlo simulation results demonstrate that a 10% of V_T spread (STD/Mean) for the LNA without substrate biasing scheme yields 6.63% *NF* spread and 5.58% NF_{min} spread. A 10% of V_T spread (STD/Mean) of the LNA with adaptive substrate biasing gives 3.85% *NF* spread and 3.52% NF_{min} spread. Comparing Fig. 5.8 and Fig. 5.9 it is apparent that the adaptive body biasing reduces the process variation effect significantly. It is also obtained that the ±0.2 volt V_{tune}

corresponds to the +5.41% to -4.16% NF deviation and +5.20% to -3.92% NF_{min} deviation. This spread fits into the compensation range for post-process V_{tune} calibration.

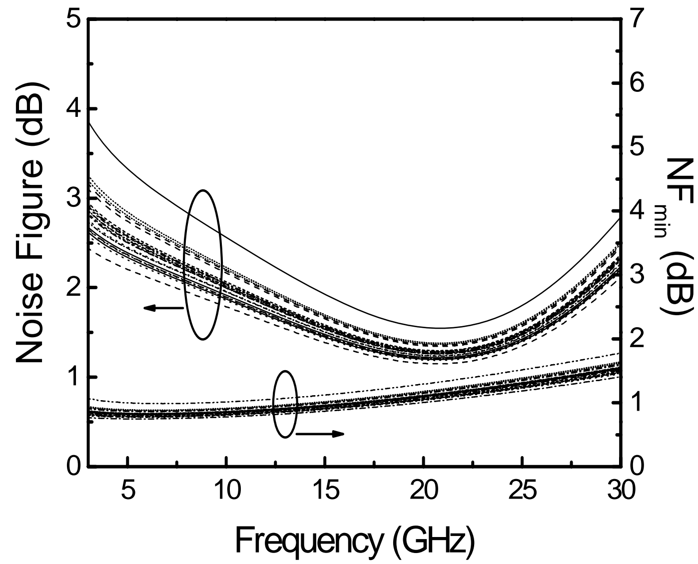


Figure 5. 8. Monte Carlo simulation of the LNA without substrate biasing technique

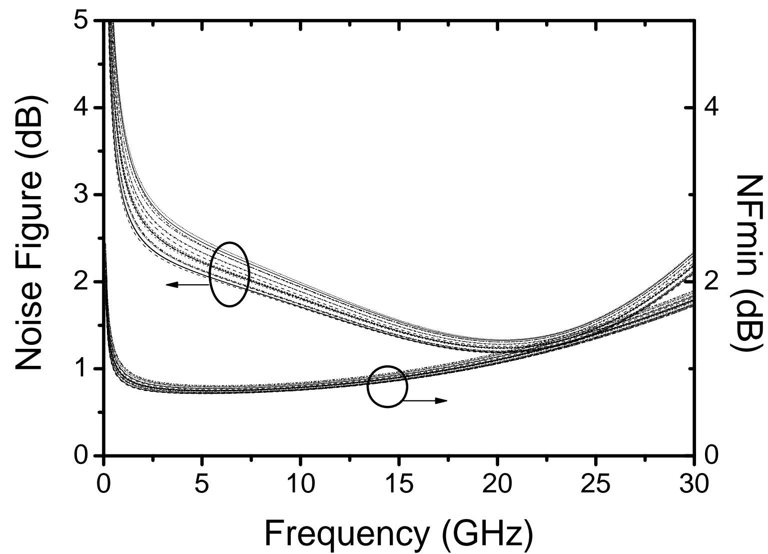
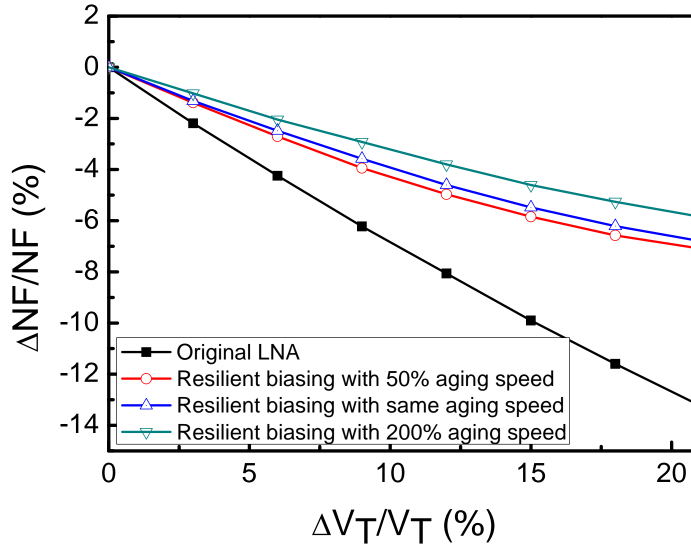
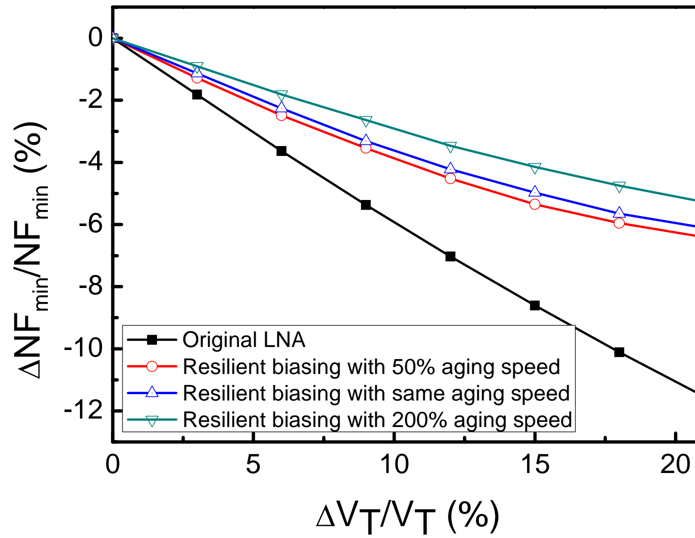


Figure 5. 9. Monte Carlo simulation of the LNA with the substrate biasing technique

The reliability effect such as threshold voltage shift and mobility degradation on the LNA with or without adaptive substrate biasing is further evaluated. Figure 5.10 shows the normalized *NF* and NF_{min} to normalized threshold voltage shift for the original LNA compared to LNA with adaptive biasing design at different degradation or aging rate. Since both Vds of the input MOS transistor and the transistor in biasing circuit is around 0.5 V, the MOS transistor in the biasing circuit is under similar stress as the input MOS transistor. But the different degradation rate is also investigated to include the possibility of various aging in the real chip. As seen in Fig. 5.10 the adaptive body biasing reduces the variation of normalized *NF* and NF_{min} significantly. Also with the degradation of the biasing MOS transistor faster than the input MOS transistor, the sensitivity of LNA NF and NFmin to the threshold voltage is further reduced.



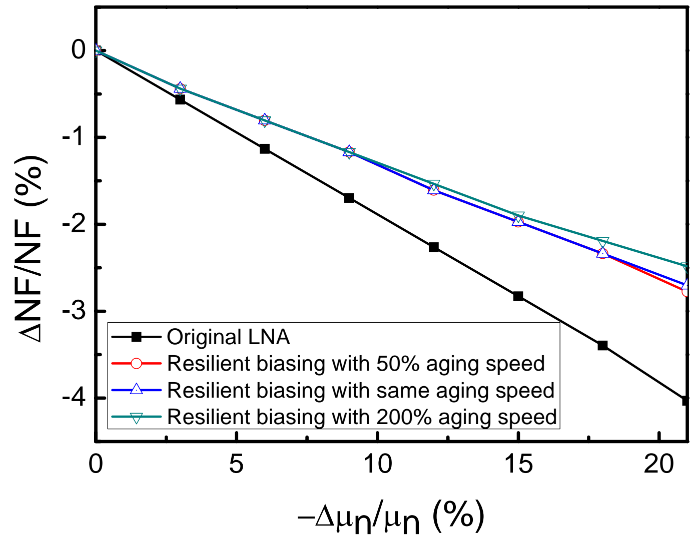
(a)



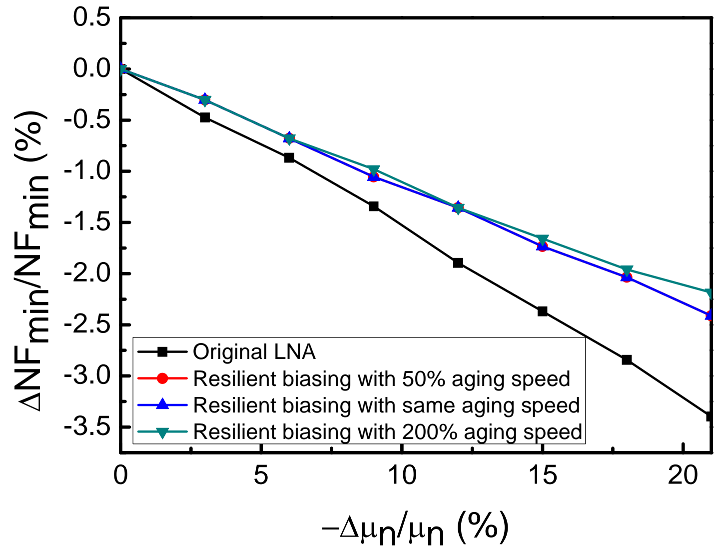
(b)

Figure 5. 10. Normalized (a) NF and (b) NF_{min} versus normalized V_T shift of the original LNA compared to the LNA with adaptive body biasing at different degradation rate

Figure 5.11 shows the normalized NF and NF_{min} variation versus normalized mobility degradation for the original LNA compared to the LNA with adaptive body biasing at different degradation rate. The adaptive body biasing also reduces the sensitivity of normalized NF and NF_{min} against mobility degradation, though its effect is not as large as that in threshold voltage shift. With the faster aging rate of MOS transistor in the biasing circuit, the sensitivity of LNA to the mobility shift is slightly reduced.



(a)



(b)

Figure 5. 11. Normalized (a) *NF* and (b) NF_{min} versus normalized μ_n degradation of the original LNA compared to the LNA with adaptive body biasing at different degradation rate

The small-signal gain sensitivity versus V_T shift considered different aging rate is examined in Fig. 5.12. In this figure the adaptive substrate biasing does not help reduce S_{21} sensitivity as indicted by Eq. (5.53). Figure 5.13 displays normalized S21 sensitivity versus mobility degradation for the LNA with or without adaptive biasing scheme considered different aging rate. The adaptive body biasing increases the S_{21} sensitivity slightly subject to electron mobility degradation.

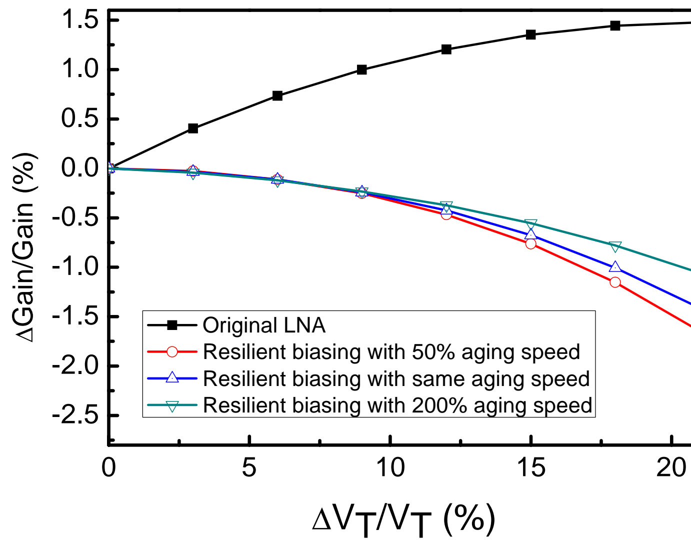


Figure 5. 12. Gain sensitivity versus threshold voltage shift considered different aging rate

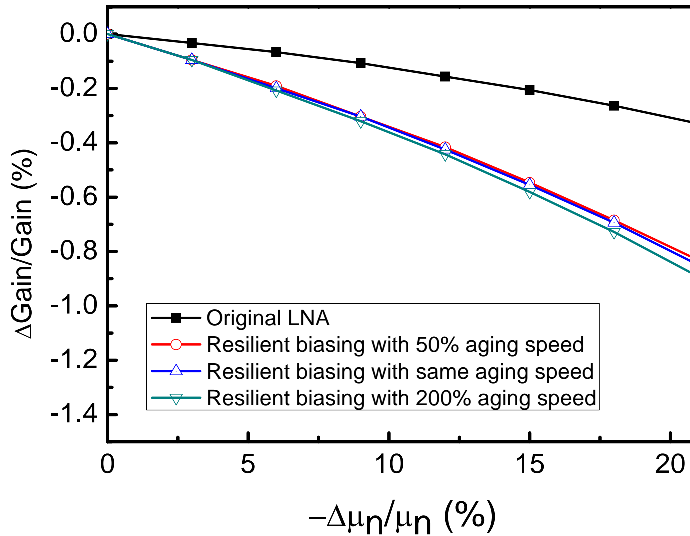


Figure 5. 13. Gain sensitivity versus electron mobility variation considered different aging rate

5.4 Chapter Outline

The adaptive body biasing technique is proposed for CMOS RF LNA against process variation and device reliability degradation. Small-signal equivalent circuit models including body biasing effect for noise and gain analysis have been developed. The LNA performances with adaptive body biasing considered different aging rate are compared with those of the LNA without body biasing technique. The adaptive body biasing makes the LNA more resilient to process variations as demonstrated by Monte Carlo simulation. The adaptive body biasing also reduces noise figure and minimum noise figure sensitivity against device aging such as threshold voltage shift and mobility degradation. The impact of various MOS transistors degradation mismatches on LNA performance degradation is studied. It is observed that with the faster aging of biasing

circuit, the sensitivity of LNA is further reduced. The body biasing, however, does not help reduce small-signal gain sensitivity.

CHAPTER SIX: CONCLUSIONS

6.1 Accomplishment

In this work, a novel adaptive body biasing design is proposed for RF transmitter and receiver circuits. With the semiconductor industry entering submicron regime, the active transistor is more sensitive to the process fluctuation such as random doping profile. Also the device is more vulnerable to electric and thermal stress induced reliability degradation like hot electron, TDDB, and BTI. The deviation of device behavior will lead to the whole RF circuit performance degradation as presented in many previous research works [94-100]. After the background introduction and some premium simulation results about device random doping fluctuation, a novel adaptive body biasing scheme is presented. The theory of negative feedback is applied in the design of such biasing topology. Analytical model is deducted in explaining the reason why such design helps the RF circuits robust against long term stress induced degradation. Case by case study of different RF circuit modules are investigated such as class-AB RF PA and LNA using PTM 65 nm technology device. After the mathematic modeling and simulation comparison between the circuits with the biasing scheme and the original circuits, the improvement in the performance against degradation is observed. Generally speaking, the adaptive body biasing scheme helps reduce the major performance sensitivity of most RF circuits. Performance robustness enhancement includes the parameters like Pout, IIP3, and PAE of PA, NF and S21 of LNA. For example, the Pout and PAE of PA are about 50% less sensitive to the V_T shift and 25% less sensitive to electron mobility degradation.

For LNA, the sensitivity of majority parameters are reduced as described in previous chapters. So the novel design succeeds in helping the RFICs against the device degradation and making the circuit more robust and healthy. The situation of possible various stress induced device degradation mismatches has been studied. It is shown that the accelerated aging speed of MOS transistor in the biasing circuit further reduces the performance sensitivity of PA and LNA.

6.2 Future Work

The work in this dissertation is not full picture yet. Further lab sample should be fabricated for real sample test and comparison for reliability degradation resilience. Performance for different circuits should be measured from these experiments to support the theory and simulations done in this work. Also there will be a lot fabrication issue beyond expectation, especially process and model related issues. While in the process of overcoming the difficulty of process, novel ideas will emerge.

Further topology optimization like better biasing structure need to be considered for specific application, for example, high frequency power amplification application. Also smaller chip size, cheaper on cost, and better RF FOM is the important design considerations in the RFIC optimization.

APPENDIX A: MICROWAVE NETWORK

Scattering parameters (S –parameters) is utilized in the description of the microwave network, which describe the property of the network based on the incident power waves and reflected power wave from the ports. Y-parameters are another set of parameters used to describe the electric network based on the voltages and currents at the ports.

The definition of Y-parameters and S-parameters for two-port network is:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{A1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{A2}$$

where, a1, a2 are incident power wave;b1, b2 are reflected power wave; usually characteristic impedance of 50 Ω is assumed.

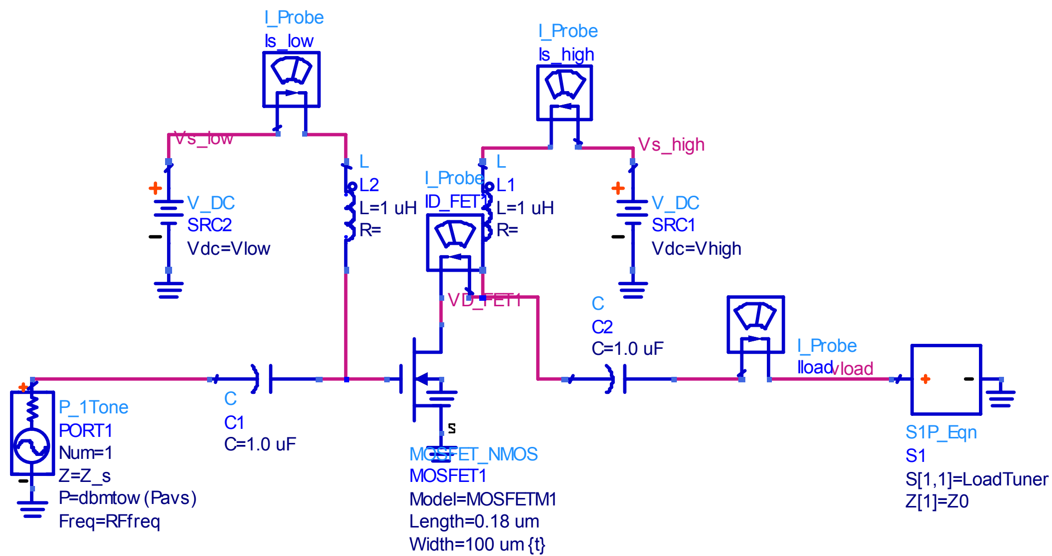
The transformation between Y_{21} and S-parameters for two-port network used in the work [101-103] is:

$$S_{21} = \frac{-2Y_{21}\sqrt{Z_{01}Z_{02}}}{\Delta_1} \tag{A3}$$

$$\Delta_1 = (1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{21}Z_{01}Y_{12}Z_{02} \tag{A4}$$

APPENDIX B: LOAD-PULL INSTRUMENT

The load-pull instrument is the common method to achieve optimum output power and power added efficiency for RF power amplifier. The load-pull automatically searches the optimum load impedance plane through smith chart for the PA to reach a contour output power and efficiency plot. A sample load-pull setup in ADS is shown in the following. The LoadTuner will automatically calculate the contour plot in smith chart, which the designers can pick up the optimum value for their own design specification.



APPENDIX C: PTM BSIM4 MODEL CARD

The predictive technology model (PTM) developed by Arizona State University [12] provides accurate, customizable, and predictive model files for future transistor and interconnect technologies. These predictive model files are compatible with standard circuit simulators, such as SPICE, and scalable with a wide range of process variations.

A complete nMOSFET 65nm BSIM4 model card used in this work is attached in the following.

```
* PTM 65nm NMOS

.model  nmos  nmos  level = 54


+version = 4.0      binunit = 1       paramchk= 1       mobmod  = 0
+capmod  = 2        igcmod  = 1       igbmod  = 1       geomod  = 1
+diomod  = 1        rdsmod  = 0       rbodymod= 1       rgatemod= 1
+permod  = 1        acnqsmod= 0       trnqsmod= 0


+tnom    = 27       toxe    = 1.85e-9   toxp    = 1.2e-9    toxm    = 1.85e-9
+dtox    = 0.65e-9  epsrox  = 3.9       wint    = 5e-009    lint    = 5.25e-009
+ll      = 0        wl      = 0         lln     = 1         wln     = 1
+lw      = 0        ww      = 0         lwn     = 1         wwn     = 1
+lwl     = 0        wwl     = 0         xpart   = 0         toxref  = 1.85e-9
+xl      = -30e-9
+vth0    = 0.423    k1      = 0.4       k2      = 0.01      k3      = 0
+k3b     = 0        w0      = 2.5e-006  dvt0    = 1         dvt1    = 2
```

```
+dvt2    = -0.032     dvt0w   = 0          dvt1w   = 0          dvt2w   = 0
+dsub    = 0.1        minv    = 0.05       voffl   = 0          dvtp0   = 1.0e-009
+dvtp1   = 0.1        lpe0    = 0          lpeb    = 0          xj      = 1.96e-008
+ngate   = 2e+020     ndep    = 2.54e+018  nsd     = 2e+020     phin    = 0
+cdsc    = 0.000      cdscb   = 0          cdscd   = 0          cit     = 0
+voff    = -0.13      nfactor = 1.9        eta0    = 0.0058     etab    = 0
+vfb     = -0.55      u0      = 0.0491     ua      = 6e-010     ub      = 1.2e-018
+uc      = 0          vsat    = 124340     a0      = 1.0        ags     = 1e-020
+a1      = 0          a2      = 1.0        b0      = 0          b1      = 0
+keta    = 0.04       dwg     = 0          dwb     = 0          pclm    = 0.04
+pdiblc1 = 0.001      pdiblc2 = 0.001      pdiblcb = -0.005     drout   = 0.5
+pvag    = 1e-020     delta   = 0.01       pscbe1  = 8.14e+008  pscbe2  = 1e-007
+fprout  = 0.2        pdits   = 0.08       pditsd  = 0.23       pditsl  = 2.3e+006
+rsh     = 5          rdsw    = 165        rsw     = 85         rdw     = 85
+rdswmin = 0          rdwmin  = 0          rswmin  = 0          prwg    = 0
+prwb    = 6.8e-011   wr      = 1          alpha0  = 0.074      alpha1  = 0.005
+beta0   = 30         agidl   = 0.0002     bgidl   = 2.1e+009   cgidl   = 0.0002
+egidl   = 0.8

+aigbacc = 0.012      bigbacc = 0.0028     cigbacc = 0.002
+nigbacc = 1          aigbinv = 0.014      bigbinv = 0.004      cigbinv = 0.004
+eigbinv = 1.1        nigbinv = 3          aigc    = 0.012      bigc    = 0.0028
+cigc    = 0.002      aigsd   = 0.012      bigsd   = 0.0028     cigsd   = 0.002
```

```
+nigc    = 1           poxedge = 1           pigcd   = 1           ntox    = 1

+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 1.5e-010    cgdo    = 1.5e-010    cgbo    = 2.56e-011   cgdl    = 2.653e-10
+cgsl    = 2.653e-10   ckappas = 0.03        ckappad = 0.03        acde    = 1
+moin    = 15          noff    = 0.9         voffcv  = 0.02

+kt1     = -0.11       kt1l    = 0           kt2     = 0.022       ute     = -1.5
+ua1     = 4.31e-009   ub1     = 7.61e-018   uc1     = -5.6e-011   prt     = 0
+at      = 33000

+fnoimod = 1           tnoimod = 0

+jss     = 0.0001      jsws    = 1e-011      jswgs   = 1e-010      njs     = 1
+ijthsfwd= 0.01        ijthsrev= 0.001       bvs     = 10          xjbvs   = 1
+jsd     = 0.0001      jswd    = 1e-011      jswgd   = 1e-010      njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001       bvd     = 10          xjbvd   = 1
+pbs     = 1           cjs     = 0.0005      mjs     = 0.5         pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33        pbswgs  = 1           cjswgs  = 3e-010
+mjswgs  = 0.33        pbd     = 1           cjd     = 0.0005      mjd     = 0.5
+pbswd   = 1           cjswd   = 5e-010      mjswd   = 0.33        pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33        tpb     = 0.005       tcj     = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001       tpbswg  = 0.005       tcjswg  = 0.001
```

```
+xtis    = 3            xtid    = 3

+dmcg    = 0e-006       dmci    = 0e-006       dmdg    = 0e-006       dmcgt   = 0e-007
+dwj     = 0.0e-008     xgw     = 0e-007       xgl     = 0e-008

+rshg    = 0.4          gbmin   = 1e-010       rbpb    = 5            rbpd    = 15
     +rbps    = 15           rbdb    = 15           rbsb    = 15           ngcon   = 1
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