2012

A New Quasi Resonant Dc-link For Photovoltaic Micro-inverters

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A NEW QUASI RESONANT DC-LINK FOR PHOTOVOLTAIC MICRO-INVERTERS

by

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A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the Department of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Summer Term
2012

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ABSTRACT

PV Inverters have the task of tracking the maximum power point (MPP), and regulating the solar energy generation to this optimal operation point. The second task is the conversion of direct current produced by the solar modules into alternating current compatible with the grid.

A new inverter approach such as a single phase micro inverter is emerging aimed to overcome some of the challenges of centralized inverters. As a counterpart to the central inverter, a micro inverter is a small compact module attached directly to each solar panel.

To provide for the constantly increasing demand for a small size, light weight and high efficiency micro inverter, soft switching power conversion technologies have been employed. The switching stress can be minimized by turning on/off each switch when the voltage across it or the current through it is zero at the switching transition. With the addition of auxiliary circuits such as auxiliary switches and LC resonant components the so called soft switching condition can be achieved for semiconductor devices.

Four main purposes to investigate the soft switching technologies for single-phase micro-inverter are:

(1) to improve overall efficiency by creating the favorable operating conditions for power devices using soft-switching techniques;

(2) to shrink the reactive components by pushing the switching frequency to a higher range with decent efficiency.

(3) to ensure soft switching does not exacerbate inverter performance, meaning all conventional PWM algorithms can be applied in order to meet IEEE standards.

(4) to investigate which soft switching techniques offer the cheapest topology and control strategy as cost and simple control are crucial for low power inverter applications.

An overview on the existing soft-switching inverter topologies for single phase inverter technology is summarized.

A new quasi resonant DC link that allows for pulse- width- modulation (PWM) is presented in this thesis. The proposed quasi resonant DC link provides zero-voltage switching (ZVS) condition for the main devices by resonating the DC-link voltage to zero via three auxiliary switches and LC components. The operating principle and mode analysis are given. The simulation was carried out to verify the proposed soft switching technique. A 150W 120VAC single-phase prototype was built. The experimental results show that the soft switching for four main switches can be realized under different load conditions and the peak efficiency can reach 95.6%. The proposed quasi DC link can be applied to both single-phase and three-phase DC/AC micro inverter.

In order to boost efficiency and increase power density it is important to evaluate the power loss mechanism in each stage of operation of the micro inverter. Using the datasheet parameters of the commercially available semiconductor switches, conduction and switching losses were estimated. This thesis presents a method to analyze power losses of the new resonant DC link inverter which alleviates topology

optimization and MOSFET selection. An analytical, yet simple model for calculating the conduction and switching losses was developed. With this model a rough calculation of efficiency can be done, which helps to speed up the design process and to increase efficiency.

To my dearest parents:

My Father, Mikhail Vasilievich Grishin and
My mother, Elena Borisovna Grishina

For their endless support, love and encouragement

Моим замечательным родителям

Моемн отцу, Гришину Михаилу Васильевичу и
Моей матери, Гришиной Елене Борисовне

За их бесконечную поддержку, любовь и ободрение

ACKNOWLEDGMENTS

I would like to convey my thanks to my advisors, Dr. John Shen and Dr. Issa Batarseh for their tremendous support and continuous motivation for my work. I am very thankful to Dr.Batarseh and Dr.Shen for their trust and for providing me with an invaluable opportunity to be a research assistant at the University of Central Florida. It is a great honor and precious memory to me to be part of the Florida Power Electronics Center.

I am grateful to my advisor Dr. Nasser Kutkut for his feedback on this work and his endless suggestions on the research project.

I would like to acknowledge my great debt to my mentor Haibing Hu for introducing me to Power Electronics and guiding me throughout the two years at Florida Power Electronics Center. If not for his support, patience and kind suggestions none of this work would be possible.

I wish to express my sincere gratitude to my early mentor Dehua Zhang for her supervision and help on the theoretical side of this work.

I would like to acknowledge my peers and scholars, colleagues from Florida Power Electronics Center, Petra Solar and Apecor including Ahmadreza Amirahmadi, Xiang Fang, Ala al-Haj Hussein, Qian Zhang, Frank Chen, Somani Utsav, Ross Kerley, Mia Ma, Charlie Jordan, Khalid Rustom, Arthur Him, Jesus Barrios, Rene Kersten and

Michael Pepper for their useful discussions during the course of research and for making this work enjoyable.

Last but not least, I would like to thank my best friend Marina Lebedeva for her everlasting encouragement through the entire course of studies.

This work is part of the project “Three-phase Micro Inverter” which has been financially supported by the Department of Energy. This support is gratefully acknowledged.

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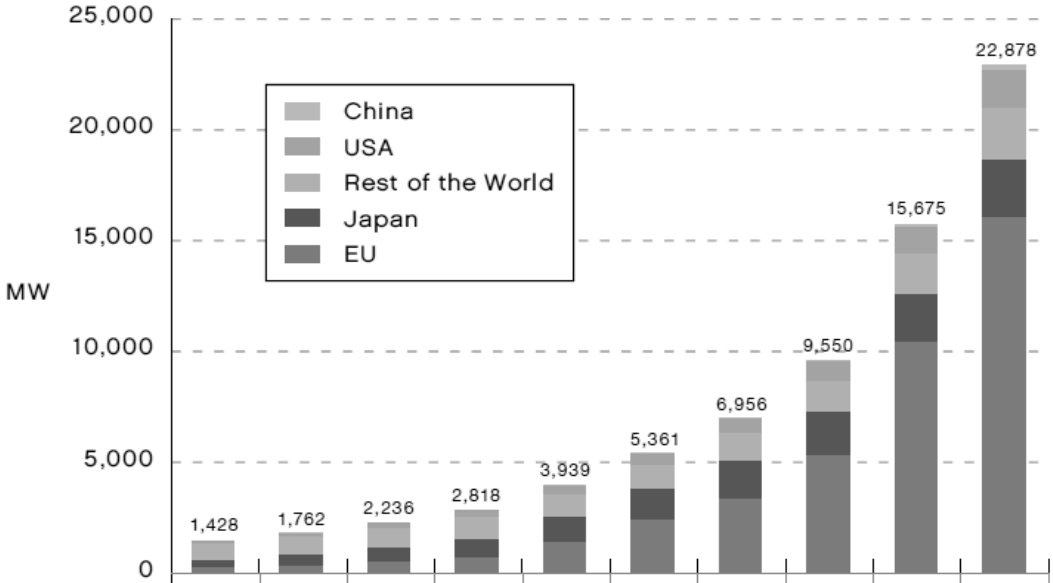
CHAPTER ONE: INTRODUCTION

1.1 Thesis Background: Renewable Energy. Research Motivation

The global energy demand is constantly increasing due to industrial advancement, emergence of new technologies, steady increase in population and global infrastructure. Since there is a limit on the non-renewable natural resources available new types of energy need to be found [1]. The constant improvement of power electronics, advancement of power semiconductor devices and government incentives for renewable energy encourage the development of photovoltaic (PV) solar power systems. The core technology in those systems are PV cells that convert sun light (photons) to electrical energy though photovoltaic effect.

Photovoltaic systems have been rapidly growing both in public and private sectors in the past decade. According to EPIA (European Photovoltaic Industry Association) in 2011, the world PV installation increased by 7.2GW (Figure 1) [2][1]. These installations include two types of photovoltaic systems: stand-alone and grid – connected. If stand-alone systems are preferred only for remote/mobile area applications, grid tied systems account for 85% of the PV market and spreading relatively fast [3].

Power electronics converter is the major player in photovoltaic power systems. As known photovoltaic modules output DC and thus, grid tied systems require an intelligent interface between the PV panel and the grid to convert the DC into 60Hz AC which is compatible with the grid. DC/AC converter (inverter) is the key technology that enables the PV generation systems to be connected to the grid.



	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009
China	19	30	45	55	64	68	80	100	145	305
USA	139	168	212	275	365	479	624	831	1,173	1,650
ROW	763	825	913	1,000	1,044	1,051	1,235	1,422	1,870	2,347
Japan	318	452	637	860	1,132	1,422	1,708	1,919	2,149	2,633
EU	189	286	429	628	1,334	2,341	3,309	5,279	10,338	15,943
Total	1,428	1,762	2,236	2,818	3,939	5,361	6,956	9,550	15,675	22,878

Figure 1 Solar PV installations in 2009

1.2 Current Architectures for PV Power Systems

PV Inverters have the task of tracking the maximum power point (MPP), and regulating the solar energy generation to this optimal operation point. The second task

is the conversion of direct current produced by the solar modules into alternating current compatible with the grid.

Depending on the PV panel arrangement; there are three types of the inverters' architecture [4]:

- central inverters,
- string inverters
- micro inverters.

In central inverter architecture as shown in Figure 2, a series of strings are connected to a central inverter. This architecture has become conventional for 100 kilowatt peak solar plants. Currently the largest central inverter units have an output of above ten megawatts [5], [6].

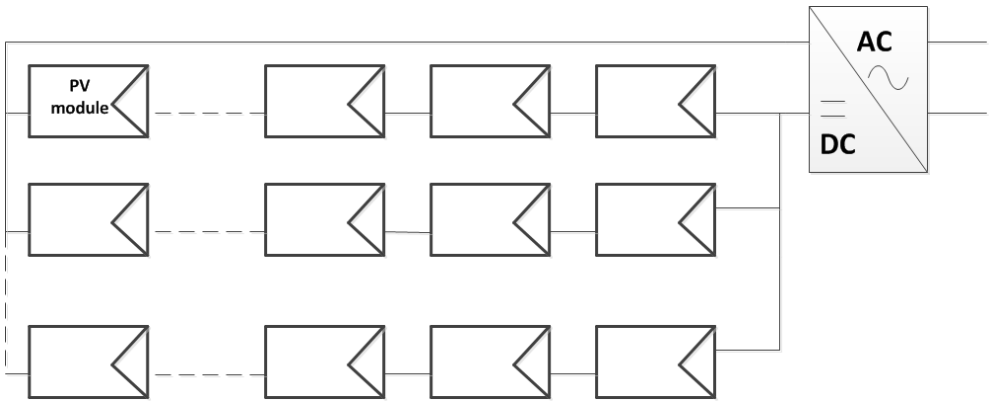


Figure 2 Central inverter architecture

In a string inverter concept (Figure 3), a few strings are connected to many small inverters. Tracking systems in particular generally have one inverter per module table. This concept has become established for solar parks in an output range of one megawatt or more [5], [6]. There are therefore many applications where it is unclear

which technology should be preferable. Taking into consideration the actual investment costs will, in most cases help to establish which solution is best in a particular case.

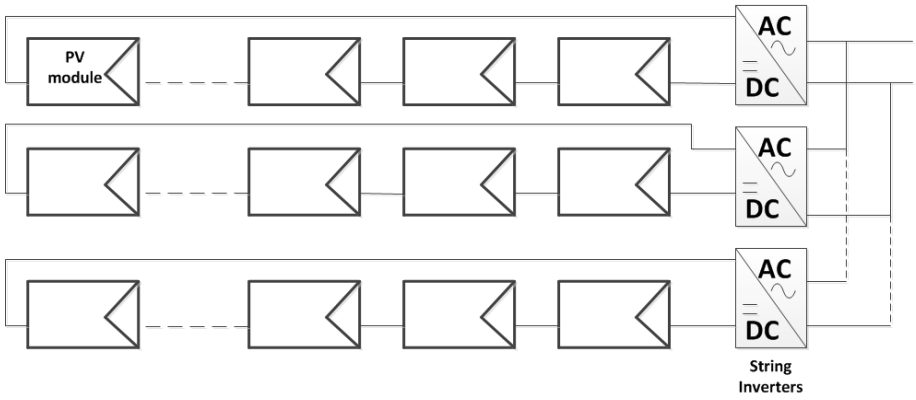


Figure 3 String inverter structure

A new inverter approach such as single phase micro inverter is introduced aimed to overcome some of the challenges of a large, centralized inverter. As a counterpart to central inverter, a micro inverter is a small compact module attached directly to each solar panel [6] (Figure 4).

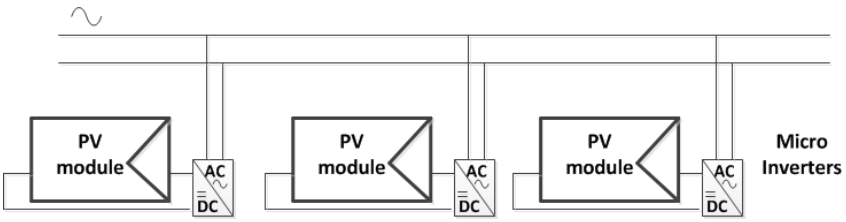


Figure 4 Micro inverter architecture

1.3 Central Inverters vs. Micro Inverters

Advantages of micro inverter

Enhanced Productivity

In conventional inverter architecture the MPPT algorithm views the entire string (string inverter architecture) or the entire plant (centralized inverter architecture) as a single module. This allows the performance of the entire solar power system to be determined by the weakest module. For this reason shading of a single panel decreases the performance of the entire system, resulting in the loss of energy generated by the plant.

The micro inverter performs MPPT at each solar module, and therefore has an capability to handle the shading of the panels [7]. Therefore, if one panel is shaded, the rest of the panels still have an ability to operate to their maximum potential.

Overall Reliability

Micro inverters create no single point of failure, meaning each panel can still generate power even if one of the inverters goes out of service [8], [9].

Safety

Micro inverter has an advantage of a lower DC voltage, compared to central inverters, which is less inclined to arcing and therefore safer[8], [9].

Simplicity and flexibility

With micro-inverters being attached to each panel, it has no limitation on the design and wiring of the entire plant. Additional panels can be mounted at any time in the future without the need for redesigning the current architecture or purchase of the new large central inverter. Moreover it eliminates the space requirement for a large inverter and the need for installation of the DC bus. Each inverter can be easily replaced if it is damaged of goes out of service [9].

Disadvantages of micro inverter

Reliability issue for a micro-inverter

Each component in a micro inverter, just as in a central or string inverter, is susceptible to failure. It is also important to note that micro inverters are difficult to repair as swapping of the single parts is impossible. [8]

High- temperature operation conditions

Micro inverters are subject to work on the backside of the inverter where the temperature can reach up to 60 degrees Celsius. It is well known that harsh temperature conditions degrade the life time of the components of micro inverter.

High Cost

Even though the price of the micro inverter is gradually decreasing with the introduction of the new technologies and the decrease of cost of semiconductor devices it is still double the price of the large-size inverter pricing and is approximately $1 per watt [3], [10], [11], [12].

1.4 PV Modules

In order to make a selection on the topology of the micro inverter, it is essential to identify the type of panel it will be interfacing to as the panels have distinct featured characteristics such as power ratings, output voltage and efficiency.

Currently there are two types of most widely adopted semiconductor technologies available for photovoltaic solar panels: *crystalline silicon* (mono and multi) and *thin film* (Cadmium Telluride; amorphous silicon; and Copper Indium Gallium Selenide).

It is interesting to note that Mono Crystalline panels are the most efficient and most expensive on the market [14]. Thin Film offer the lowest manufacturing costs yet

are the least efficient. Therefore multi crystalline panel is an interesting compromising solution being less expensive than mono crystalline silicon and more efficient than Thin Film [5].

Besides the efficiency, temperature coefficient is a notable quality of PV cells. In general, all the cells have a negative temperature coefficient, resulting in a decrease in power production with an increase in temperature. Silicon modules are inferior to Cadmium telluride (CdTe) technology, significantly refined over the past few years, in performance at the high temperatures and in light absorption properties under cloudy and diffuse light conditions [14].

Table 1 shows the comparison of different type of crystalline and thin film modules [13]. Analysis of the table shows a trade- off between efficiency and performance in high temperatures or shady conditions.

Table 1 PV modules performance comparison

Technology		Efficiency	Temperature coefficient
Crystalline Silicon	Monocrystalline Silicon	13-19	highest
	Multicrystalline Silicon	*11-15*	*highest*
Thin Film	*Cadmium Telluride (CdTe)*	*4-8*	*low*
	Amorphous Silicon (aSi)	10-11	lowest
	Copper, Indium, Gallium, Selenide (CIGS)	7-11	high

As the solar panel represents the largest part of the cost of the photovoltaic power plant, the pricing of the entire system largely depends on the price of the single

module. As of September 2010, a multi crystalline silicon solar module is $1.99/W; a mono crystalline silicon module is $2.17/W; and the thin film module is $1.07/W [15].

For the past decade thin-film CdTe showed fast growing production and manufacturing rates, however the crystalline silicon remains the most common technology representing about 80% of the market today.

The electrical features from PV panel datasheets of the top 10 photovoltaic cells and module manufactures which represent about 45% share of the total global production were investigated and presented in a table 2 [13].

Table 2 PV Modules

Company	Type	Maximum Power PMPP [W]	MPP Voltage VMPP [V]
First Solar	Thin-film	70 – 80	48.1 - 71.2
Suntech Power	Monocrystalline	175 - 190	35.2 - 36.5
	Multicrystalline	205 - 280	26.4 - 35.2
q-cells	Multicrystalline	205 - 245	28.05 - 30.55
yinglisolar	Multicrystalline	165 - 280	23 - 35.5
JA Solar	Monocrystalline	165 - 240	28.09 - 37.88
	Multicrystalline	200 - 240	28.13 - 29.72
Kyocera	Multicrystalline	135 - 235	17.7 - 29.8
Trina Solar	Monocrystalline	175 - 245	29.4 - 36.8
	Multicrystalline	220 - 240	29 - 30.4
Sunpower	Monocrystalline	200 - 410	40 - 72.9
Sharp	Multicrystalline	170 - 235	23.42 - 36.6
	Thin-film	115 - 142	174 - 192

Thin film PV panels with low cost are preferable for the large PV plants, where conversion efficiency does not matter as much due to the fact that PV plants are usually constructed in deserted regions and expansion of the PV fields are not a big deal for investment, while the crystalline panels may be a reasonable choice for the commercial or residential applications where the higher efficiency outweighs the initial cost due to limitation on the available spaces [13], [14], [15].

Although the PV cell module represents 45 % cost of the PV system technology, the cost of grid tie inverter allocates the significant portion of the whole PV system and is around 15% of the total cost [16] (Figure 5 PV System Cost Breakdown [17]). Thus, to reduce the cost and increase the performance of the photovoltaic power system grid tie inverter with high efficiency and high power density is desired.

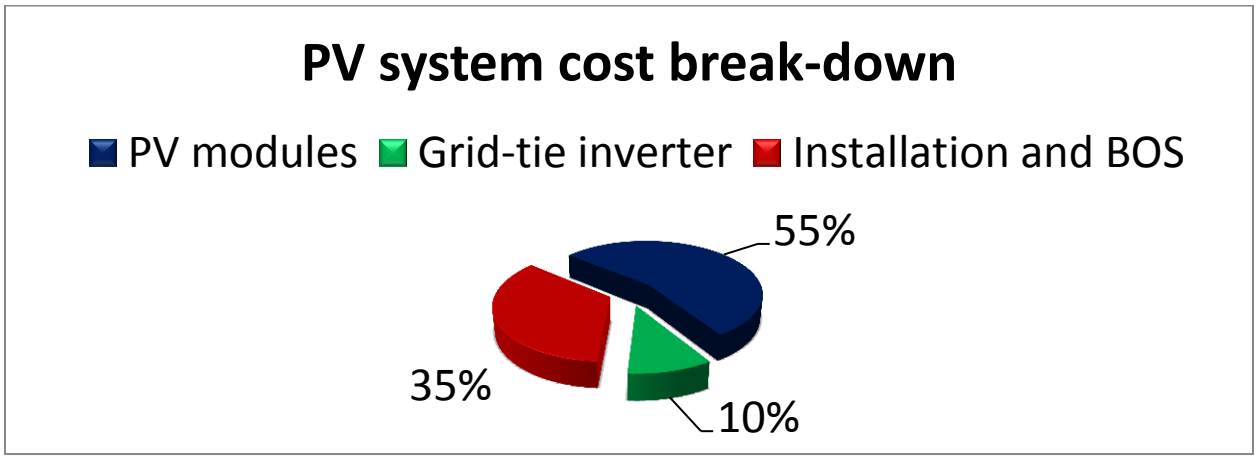


Figure 5 PV System Cost Breakdown

1.5 Basic Topologies For Single Phase Inverter

Inverter topologies can be basically classified into three basic types:

- voltage source inverters (VSI);

- current source inverters(CSI);
- Z-source inverter, which can be viewed as a hybrid of the first two types.

1.5.1 Voltage source inverter

Most practical inverter applications use voltage-source circuits (Figure 6) that have a step down characteristic and require a boost converter to meet the voltage requirements. To interface the crystalline PV panel's output voltage and to fulfill the voltage requirement of the inverter a high step-up high efficiency DC/DC stage is required. VSI are preferred because dc filter energy can be stored in capacitors rather than in inductors which are more expensive and less efficient.

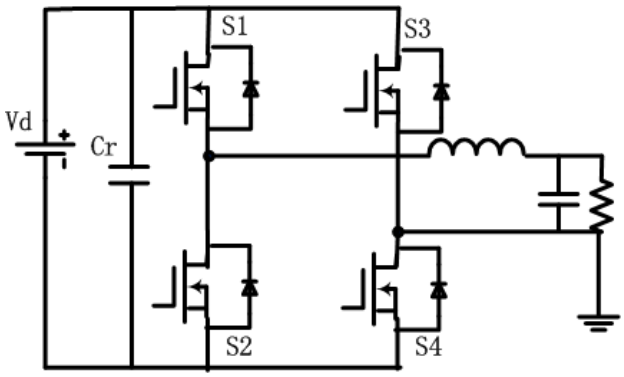


Figure 6 Voltage Source Inverter (VSI)

Voltage source inverter has its numerous advantages and disadvantages as follows [17]:

Advantages

- Standard semiconductor devices and drivers can be used

Disadvantages

- High step up front stage converter is required
- Shoot through issue

1.5.2 Current source inverter

The main advantage of current-source inverters (Figure 7) is in the reduction of the transient fault current by the dc link inductor [18]. The current-source inverters are less investigated and applied than the voltage source inverters; nevertheless, the recent technological improvements achieved for the switching devices as well as for digital signal processors have made the CSIs more attractive in several applications. [20].

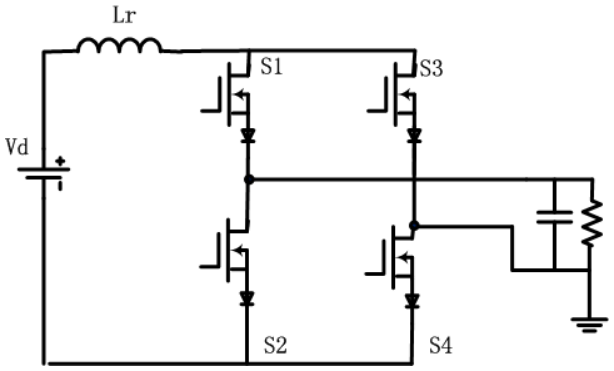


Figure 7 Current Source Inverter (CSI)

Since CSI has a voltage step-up characteristic, implementation of current-source inverter to photovoltaic power conversion eliminates the necessity in the DC/DC conversion stage or reduces the conversion ratio of a high step up DC/DC converter which is supposed to be more efficient in the conversion stage.

Current source inverter has its numerous advantages and disadvantages as follows [17]:

Advantages

- Elimination of the front stage boost converter
- Does not require anti-parallel diode for the switches
- Better current shape
- Inherent short circuit protection

Disadvantages

- Restricted range of the input voltage
- Additional loss due to series diodes
- Requires special devices/drivers
- Potential open-circuit problem

1.5.3 Z- Source inverter

To overcome the above problems of the traditional inverters, an impedance-source (abbreviated as Z-source converter) was proposed by Fangzheng Peng as shown in Figure 8 [21].

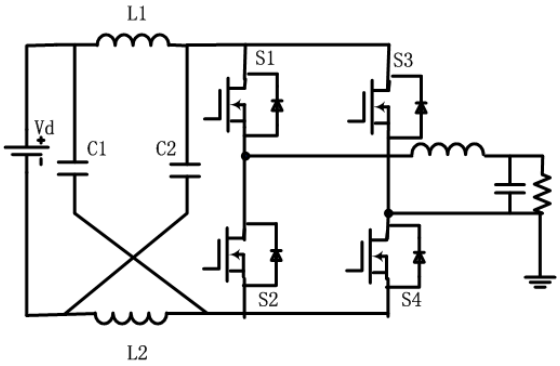


Figure 8 Z-source Inverter (ZSI)

The unique feature of the Z-source inverter is its buck-boost characteristic, meaning wide range of operating voltage. Another advantage of the z-source inverter is reduced input current and voltage ripples due to second-order filtering at the front stage. It is important to note that the addition of extra capacitor/inductor does not mean the increase in cost and/or size since smaller components can be selected due to second-order filtering.

CHAPTER TWO: REVIEW OF SOFT SWITCHING TECHNIQUES FOR SINGLE PHASE INVERTERS

In all PWM inverters the semiconductor switches turn on and turn off the current at each switching transition and are subject to high switching stress and high switching power loss that increases with the switching frequency.

From the power loss perspective it would be reasonable to decrease the switching frequency; however, the switching frequency is crucial to the design of the magnetic components. In micro inverter applications the highest possible switching frequencies are preferred in order to reduce the size of passive components and improve the system ripple and control bandwidth.

Another significant problem of the switch-mode operation is the electro magnetic interference (EMI) caused by high di/dt and dv/dt. It is favorable to slow down the turn on/turn off of the power semiconductor devices to comply with the EMI standards. Switching the power devices on full voltage/full load causes high spikes and high di/dt and dv/dt which is not a favorable condition in accordance to EMI standards.

To provide for the constantly - increasing demand for small size, light weight and high efficiency micro inverter, soft switching power conversion technologies have been employed. The switching stress can be minimized by decreasing the voltage across it or current through it to zero at the switching transition. With the addition of auxiliary circuits

such as auxiliary switches and LC resonant components the so called soft switching condition can be achieved for semiconductor devices.

Four main purposes to investigate the soft switching technologies for single-phase micro-inverter are:

(1) to improve overall efficiency by creating the favorable operating conditions for power devices using soft-switching techniques;

(2) to shrink the reactive components by pushing the switching frequency to a higher range with decent efficiency.

(3) to ensure soft switching does not exacerbate inverter performance, meaning all conventional PWM algorithms can be applied in order to meet IEEE standards.

(4) to investigate which soft switching techniques offer the cheapest topology and control strategy as cost and simple control are crucial for low power inverter applications.

The switching strategies for the voltage source inverter, which result in zero-voltage and/or zero-current switching, are classified into four families of techniques such as:

1. RCD snubber,
2. Auxiliary resonant commuted pole (ARCP),
3. Resonant DC link.
4. Quasi-resonant DC link inverters

Soft switching techniques are key techniques to achieve both high power density and high efficiency. Many efforts have been made to explore various soft switching

techniques for DC-AC inverters. In most soft switching techniques resonant components and auxiliary devices are employed to create either zero voltage or zero current across the device prior to the switching instance. An overview on the existing soft-switching inverter topologies for single phase grid tied inverter technology is provided in the following section.

2.1 The RCD Charge-Discharge Snubber

The evolution of soft switching resonant converters has started with the RCD charge- discharge snubber. In order to give a quick idea of the snubber it is applied to a basic semiconductor bridge - step down buck converter (Figure 9). The objective of the snubber is to control dv/dt or di/dt in a way to reduce the time duration of the switching interval as well as to reduce current/voltage overshoots [22], [23], [24]. One of such snubbers is the capacitive snubber which aims to decrease overvoltage resulted from the stray inductances at turn off [22].

Without a snubber at switch turn off the current of the device S1 is diverted to the diode D1 only when the diode is in forward bias state which means that the voltage across the switch needs to rise to the source voltage before the current starts falling. By adding the capacitor in parallel with the switch, a part of switch current will be diverted to it at turn off, which means current fall and voltage rise can start simultaneously. Due to the soft characteristic of the switching waveforms it is referred to as soft switching.

Even though introduction of the capacitive snubber results in favorable turn off, it exacerbates turn on waveform as addition of the capacitor brings additional current stress to the device [22], [23], [24]. The problem of the turn on is in current overshoot due to the phenomena of reverse recovery of the diode. The reverse recovery refers to

the negative current flowing through the diode for a short period of time caused by minority carriers being swept out of the pn junction after it becomes reversed biased. The capacitor is fully charged prior to the turn on instance of the device meaning that the voltage across the device cannot decrease before the diode becomes reverse biased. The moment of the diode becomes reverse biased falls on the peak of the reverse recovery current which increases the current stress on the device turn on. Therefore, the switch has to carry excessive amount of current as it is the only path for the capacitor discharge.

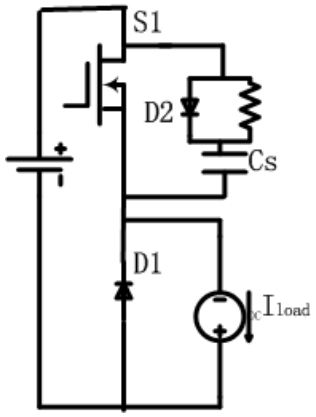


Figure 9 RCD snubber

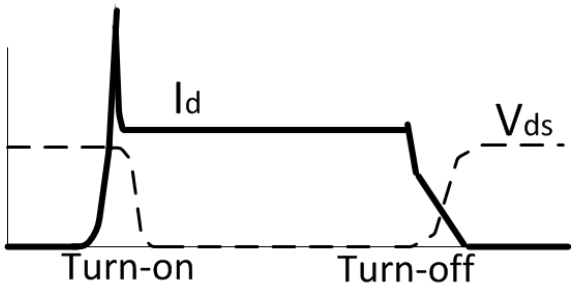


Figure 10 Switching waveform with RCD snubber

To limit the capacitor current at discharge the resistor in parallel with the diode is added to the capacitor path. The purpose of the diode is to preserve the favorable turn off behavior and avoid the possible loss increase on the added resistor. The combination of resistor – diode – capacitor is meant to soften the switching characteristic of the semiconductor device and is called the RCD snubber [22].

Besides RCD snubbers there are other types that assist turn on and turn off commutation [23],[24]. Most of them alleviate the switching and somewhat improve the switching characteristic but do not completely eliminate the power loss.

2.2 Resonant DC Link Inverters

2.2.1 Resonant DC link by Divan [24]

For the inverter application the RCD snubber is very bulky as one per each switch is required. Divan has made a giant leap to overcome this problem by introducing the Resonant DC link inverter topology where he shifts the snubbing circuit to DC link. It requires one LC component to make the DC link voltage oscillate providing for a “soft” DC bus at switching transitions. This topology seems very attractive since there is only one resonant circuit to provide soft switching condition for all the semiconductor devices of the inverter.

Resonant DC link applied to a single phase inverter is shown in Figure 11. The key waveform for the link voltage and line to line output voltage are shown in fig. The DC link resonant circuit is composed of an inductor Lr and capacitor Cr that resonate at certain frequency.

The main idea is to switch the mail devices at zero voltage instants of the DC bus. However, that brings undesirable harmonic distortion as Discrete Pulse Modulation has to be applied. In order to bring the THD close to the one obtained by conventional carrier based PWM the link has to resonate at the higher frequencies. Moreover, in order to resonate DC link voltage to zero it has to resonate up to 2- 2.5 times the source voltage that imposes additional voltage stress on the main devices. Thus higher voltage rated devices have to be chosen which adds additional cost to the inverter.

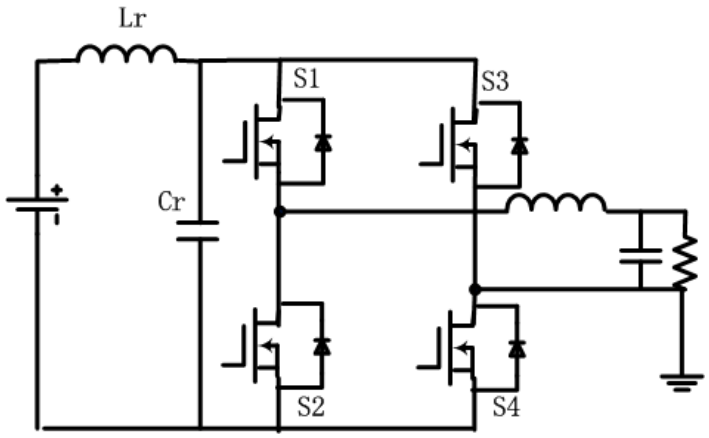


Figure 11 Resonant DC link [25]

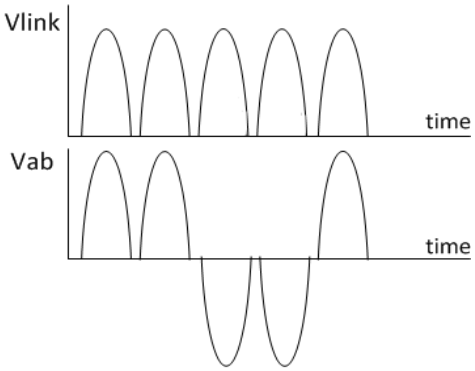


Figure 12 DC link and line to line Vab voltage waveform

2.2.2 Active Clamped Resonant DC link [25], [26]

Several ways to deal with DC link voltage overshoot and high harmonic distortion can be found in the literature. High voltage stress can be reduced to 1.4 Vd by applying a clamped circuit which involves one additional switch. The circuit diagram is presented in Figure 13. The overvoltage is predetermined by the clamp capacitor Cc as the diode of the switch Sa starts conducting whenever the link voltage Vr reaches the voltage K*Vd.

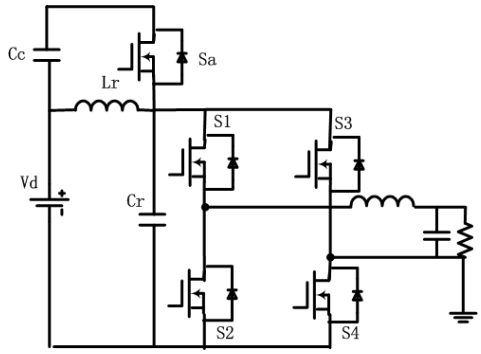


Figure 13 Active Clamped Resonant DC link [25]

Even though, the voltage stress has been reduced, it is still higher than the source voltage, so the problem of the high THD remains and the addition of the clamp switch increases the cost and reduces reliability.

2.2.3 Passive Clamped Resonant DC link [27]

Another way to implement a clamp circuit is to use a passive clamp such as coupled inductor shown in Figure 14 to accomplish the reduced DC link voltage. The main idea of this circuit is to clamp the voltage at the lower level by using the clamping diode Da and setting up the coupled inductor ratio. However, there are two problems associated with this circuit: 1. The voltage can only be clamped to 2 Vdc since the coupled inductor ratio has a limitation to provide the zero voltage across the capacitor Cr. 2. The clamping diode must withstand a high voltage of 3*Vdc.

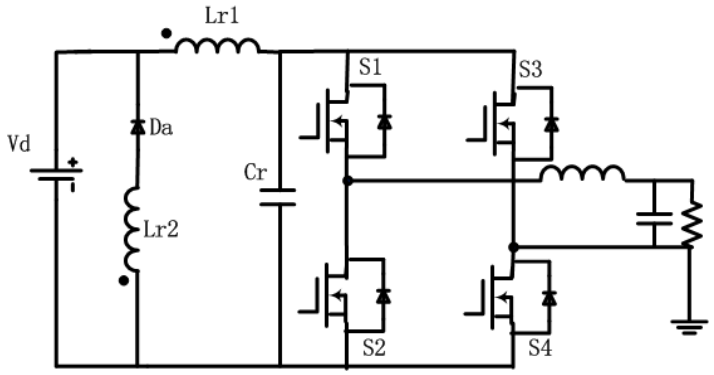


Figure 14 Passively Clamped Resonant DC link [27]

2.2.4 Two switch Passive Clamped Resonant DC link [28]

In an attempt to eliminate a sub harmonic problem in a passive clamp converter, a two switch resonant inverter realizing PWM was presented in [28] (Figure 15). The

clamping voltage is reduced to 1.1-1.3 Vdc and any type of PWM can be applied to the inverter.

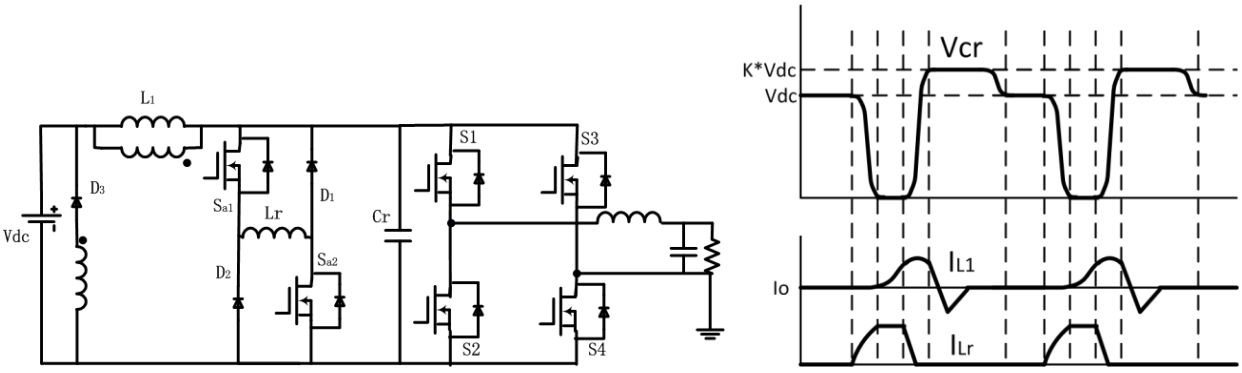


Figure 15 Passively- clamped two switch QRDCL [28]

The main circuit waveforms are shown in the figure 15. Preceding the switching transition of the inverter the passively –clamped two switch link is activated, first by the turning on of Sa1 and Sa2. The current of the inductor Lr starts building up and initiates the resonance of L1, Lr and C. The capacitor C releases its energy to Lr and forces the link voltage to zero. During the zero voltage period the inverter switches can perform the transition at the soft condition.

After the inverter finishes the change of state the DC link voltage must be returned to the source voltage to resume the operation of the inverter. The switches Sa1 and Sa2 turn off and the current of the inductor Lr returns back to the source, and the resonance between L1 and C will make the link voltage increase until it gets clamped by the passive clamp circuit L, D3 to K*Vdc. After the energy is returned to the source, inductor L1 continues to supply the output current and the normal operation of the inverter begins.

2.2.5 One Switch Passive Clamped Resonant DC link [30]

A passively clamped switch is further developed by Chen (Figure 16) to obtain just one auxiliary switch. Moreover, instead of the separate inductor, one additional coil is used. As long as the auxiliary circuit is off, the voltage of the link remains at Vdc. It initially ramps up to K*Vdc, however it gradually reduces to Vdc due to resonance losses.

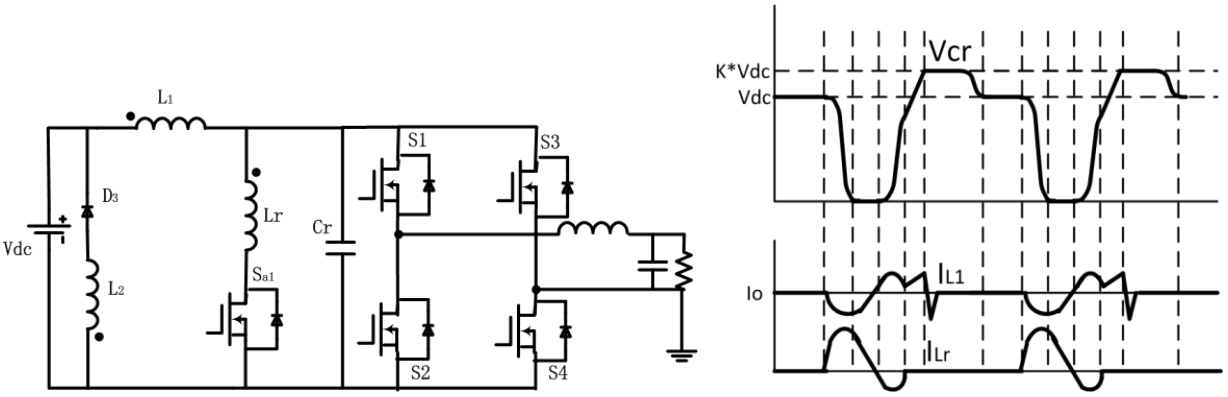


Figure 16 The passively clamped one switch QRDCL [30]

Auxiliary switch Sa1 turns on to bring the link voltage to zero through the resonance between L1, Lr and C. The voltage will be clamped to zero by the anti-parallel diodes of the main bridge. After the inverter performs the switching the link voltage is brought up to K*Vdc by turning off Sa1 and by resonating the link capacitor with L1 and L2.

2.3 Auxiliary Resonant Commutated Pole Inverter [31], [32]

The Auxiliary Resonant Commutated Pole (ARCP) technique, proposed by McMurray, can fully achieve soft switching by adding two auxiliary switches and one inductor for each phase. The circuit topology is presented in fig. with the key waveforms shown in Figure 17.

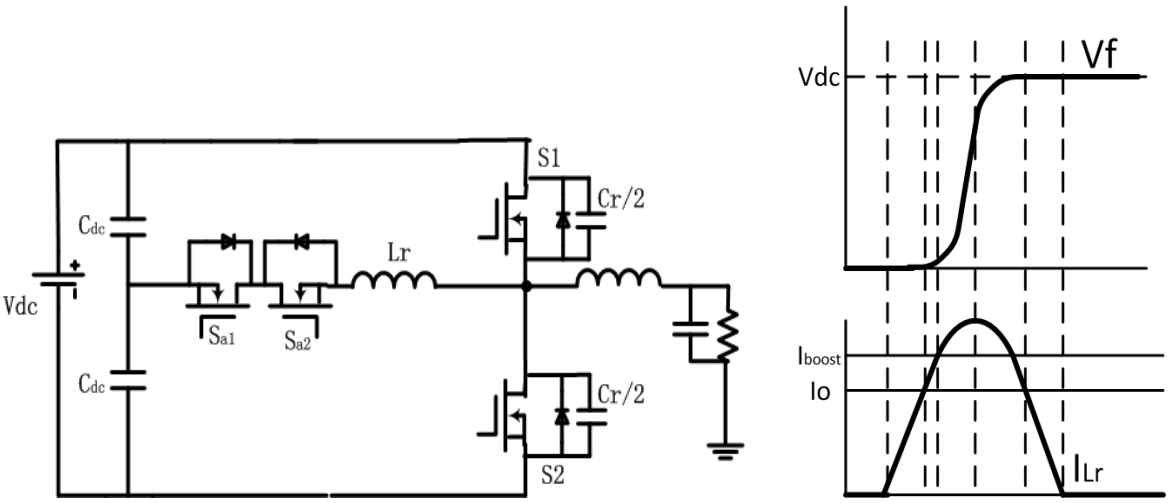


Figure 17 Auxiliary Resonant Commutated Pole Inverter and its waveforms [31]

The main switches are zero voltage turn on and the auxiliary switches operate at zero current turn on. The turn off loss is reduced due with the assistance of the snubber capacitors.

ARCP requires the addition of an extra inductor and two switches per each phase that makes the topology and control complicated and costly, especially for low power micro inverter applications, where low cost and simple control are preferred.

The complexity increases with the overvoltage protection that is essential to ARCP since its auxiliary switches are connected back to back and there is no path for the inductor current to return to the source. Furthermore, ARCP suffers from charge imbalance in the bulky input capacitors.

2.4 Quasi Resonant DC link Converters

In this section an alternative way to realize soft switching, a so-called quasi resonant DC link converter is introduced. Quasi resonant DC link circuit topologies offer lower component stress that is limited to DC voltage supply and enable implementation of conventional carrier based PWM. The way to realize QRDCL is to place a switch in the main power flow and use it to control when to provide short zero voltage instances in the dc link. QRDCL also consists of some resonant network and auxiliary devices that make the dc link resonate to zero and keep it at zero for the duration of time required for the switching transition in the PWM inverter. In this manner the occurrence of zero voltage condition is synchronized with the main semiconductor device switching of the PWM inverter.

2.4.1 Parallel Quasi- Resonant DC Link [33]

The first circuit investigated is the parallel resonant DC link proposed by He and is shown in Figure 18. It consists of the DC rail switch Sa1, LC resonant network Lr, Cr, C1, and three auxiliary switches Sa2, Sa3, and Sa4.

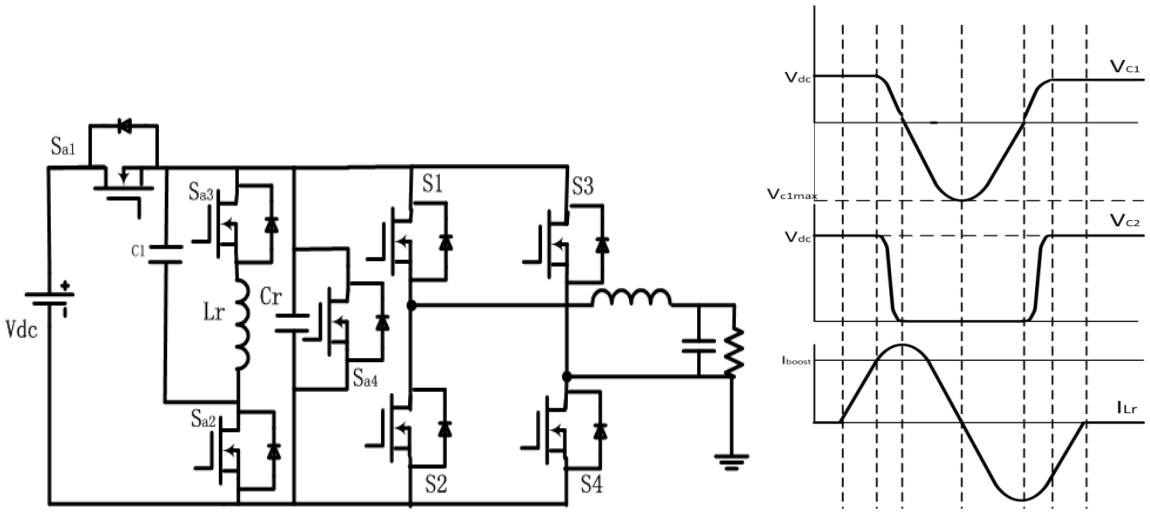


Figure 18 Parallel Resonant DC link [33]

Prior to the switching instance in the main circuit switches Sa1 and Sa2 are on and the converter operates as a conventional voltage source inverter. Whenever the switching transition is required the PRDCL is activated first by turning on the switch Sa3 to pre charge the inductor Lr. The current in inductor Lr starts ramping up linearly until it reaches the value required for the Vcr to resonate all the way to zero and then return to Vdc. Sa1 is then turned off and the resonance between Lr, Cr and C1 is initiated to discharge Cr and C1. Once the voltage across Vcr discharges to zero, the main switches can be turned on and off at the soft condition. The operation of PRDCL proceeds with turning off Sa2 and turning on of Sa4. The purpose of Sa4 is to keep the voltage across the DC link for a prolonged period of time and to separate the PRDCL from the main circuit in order to let Vc1 oscillate from its negative value to zero.

In order to resume the operation of the inverter Cr and C1 need to be charged to Vdc. It is accomplished by turning on Sa2 and turning off Sa4 which is proceeded by turning on of Sa1 whenever Vc2=Vdc. The operation of PRDCL is finished with the

resonant inductor being linearly discharged to zero and with the turning off of the switch S3.

Notice that switch Sa3 is turned on and off at zero current since the current iL is decreased to zero, Sa1 turns on and off at zero voltage as Vc1 is charged to Vdc, and Sa2 turns on and off at zero voltage whenever Vcr is discharged to zero.

This PRDCL topology utilizes four auxiliary switches, some of them have a high current stress, and the switch S2 must withstand a high voltage stress of 1.5-2 times of Vdc.

2.4.2 Parallel Quasi- Resonant DC link by Cho [34]

Another version of parallel resonant DC link that was proposed by Cho is shown in Figure 19. It has an LC link resonant circuit – Lr, Cr, reduced number of auxiliary switches – Sa1, Sa2 and Sa3, however needs two additional diodes D1 and D2.

The initial state of the PRDCL is similar to the previous converter – Sa1 is turned on and the main power flows from the source to the main bridge, capacitor Cr is charged to Vcr and the current in the resonant inductor is zero.

The operation of PRDCL starts prior to switching in the main bridge by gating on Sa2 and Sa3 and linearly pre charging the resonant inductor to the reference value. It is important to ensure that value is enough to bring the voltage of the link to zero. In order to activate the PRDCL the main power flow needs to be interrupted by turning off Sa1. The resonant inductor starts resonating with the link capacitor until the voltage Vcr is decreased to zero and the inductor current starts freewheeling through auxiliary switches and diodes. During this time the commutations in the main circuit take place at the zero voltage condition.

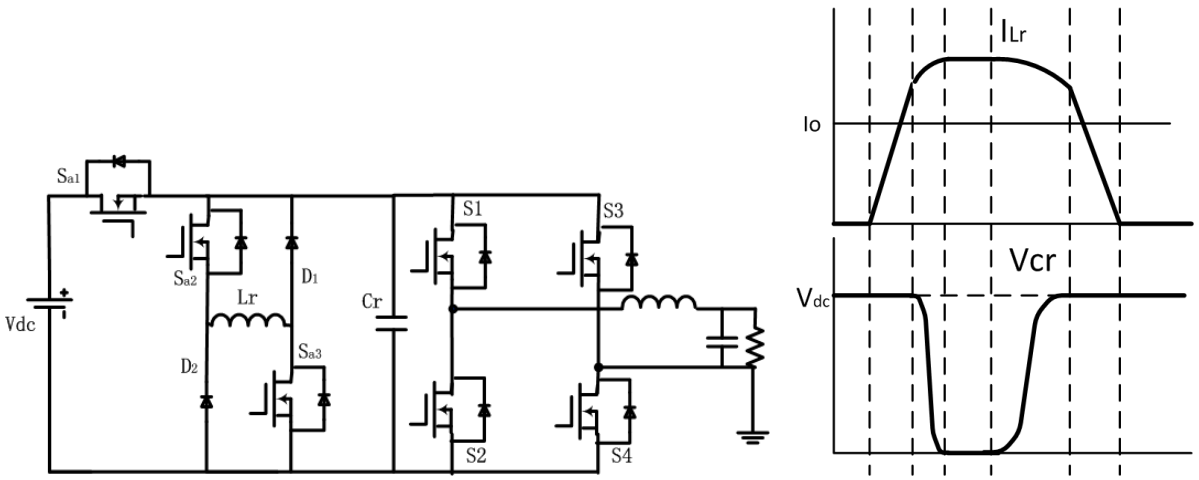


Figure 19 Parallel Quasi Resonant DC link [34]

In order to return the DC link voltage back to source voltage Vdc the switches Sa2 and Sa3 are gated off. Another resonance is initiated between Lr and Cr as the current path is diverted to the auxiliary diodes D1 and D2. Once the voltage of Vcr is increased to Vdc it gets clamped by the body diode of Sa1. The remaining current of the resonant inductor linearly decreases to zero and is returned to the source.

Note that the voltage stress of all the devices is limited to the source voltage Vdc. The switches Sa2 and Sa3 turn on with zero current and are turned off at zero voltage, Sa1 is turned on and off at zero voltage as the voltage across the dc link is Vcr, and the diodes D1 and D2 are turned off at zero current condition.

This slight modification of PRDCL is better than the previous as far as the component stress is concerned, however, the large component count – five auxiliary semiconductor devices – 3 switches and 2 diodes - is not desirable for the micro inverter.

2.4.3 Auxiliary Quasi Resonant DC link [35]

A slightly modified version of the ARCP inverter, the auxiliary QRDCL inverter proposed by DeDoncker is illustrated in Figure 20. The switch Sa3 serves the purpose of the dc rail switch that is disconnected to actuate the auxiliary circuit. For the low load current auxiliary switches Sa1 (for positive IL) and Sa2 (for negative IL) can be gated on prior to turn off of Sa3 to give the inductor Lr some boost current that is required to ensure Cr can resonate to zero volts.

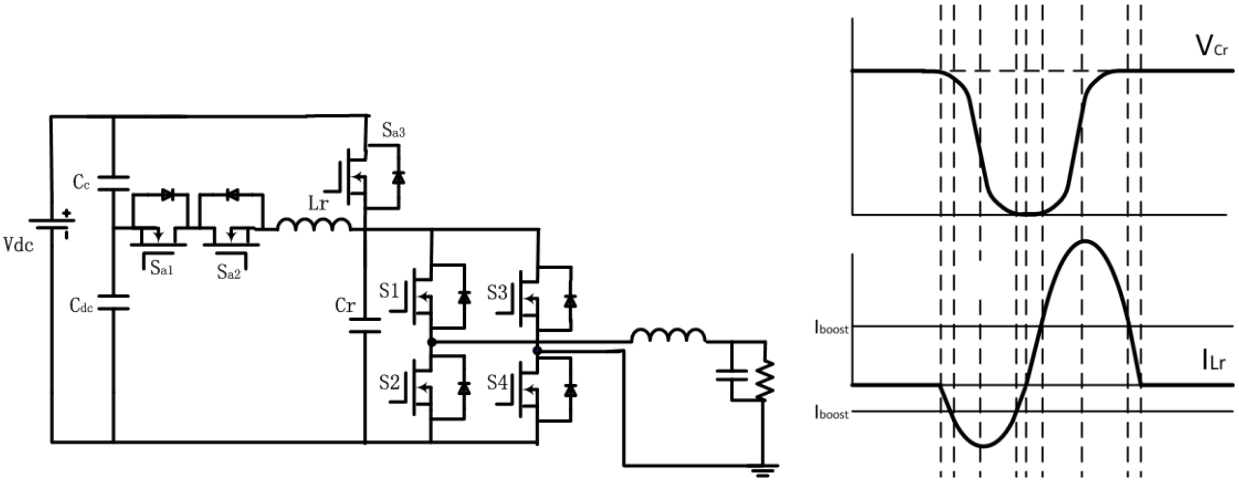


Figure 20 Auxiliary Resonant Commutated Pole QRDCL [35]

After the switch Sa3 is turned off the resonance process starts and the voltage of Cr is decreased to zero. Once it reaches zero, the diodes of the inverter bridge become forward biased and clamp the link voltage to zero. The operation proceeds with turn on of all the inverter switches and Sa2. Since inverter switches are shorting the bus and there is a potential of Vdc across the resonant inductor Lr, the current Ir starts ramping up linearly. The current increases until it reaches the value of the next stage load current plus some required boost current. After that the converter may change its state

which removes the short of capacitor Cr and another resonance starts immediately. The voltage across Cr resonates until the diode of Sa3 clamps it to Vdc. Switch Sa3 is turned on whenever the current of Lr falls below the current of the link. As Ir decreases linearly forced by a potential of Vc, the link current diverts to the dc rail switch Sa3. As the current decreases to zero the switch Sa2 is turned off.

In addition to the disadvantages quasi-resonant dc link converters, the auxiliary QRDCL inverter proposed by DeDoncker has a charge balance problem in the capacitors Cc and Cdc. The charge is extracted from Cdc by the auxiliary circuit (Sa2 turns on to increase the current to the link plus boost current) to assist the resonance of Cr to the source voltage Vdc. To solve this problem the switch Sa3 is kept on longer when the switch Sa1 turns on (Sa1 turns on to give some boost current) prior to Vcr resonating to zero. That results in the increased current stress of the switch Sa3. Another solution to better DC bus utilization is to increase the resonant frequency, however that increases the peak current and results in higher conduction loss.

2.4.4 Parallel Quasi- Resonant DC link by Malesani [36]

A few attempts have been made to reduce the number of DC link auxiliary switches to minimum. One of the circuit topologies that utilizes only one dc rail switch Sa1 and one auxiliary switch Sa2 and LC resonant components was proposed by Malesani and is presented in Figure 21. Instead of using one large link capacitor, it is distributed to the switches S1-S4 in snubber way fashion.

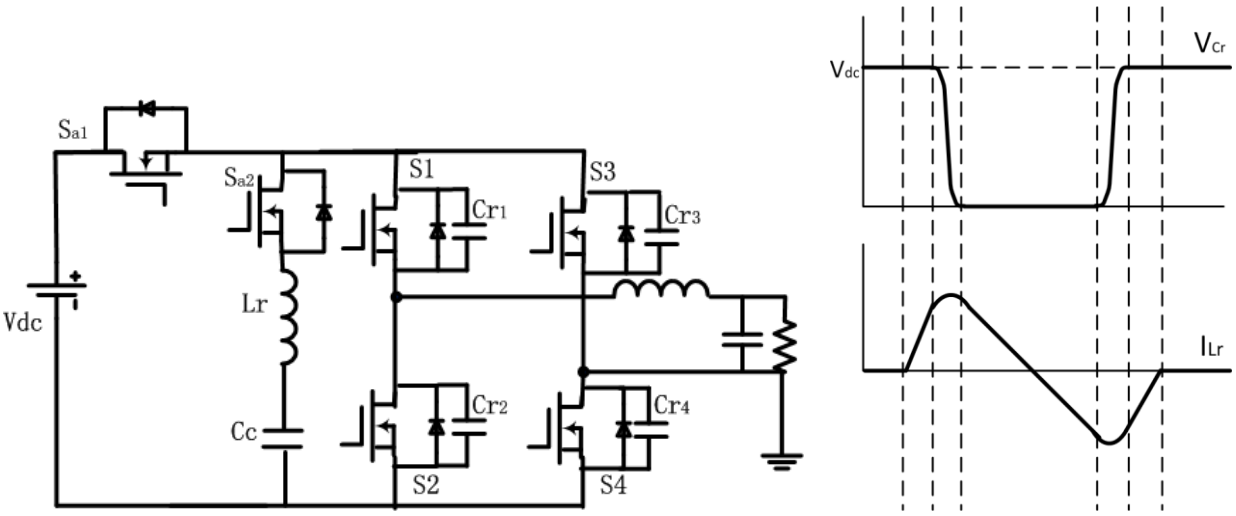


Figure 21 Parallel QRDCL by Malesani [36]

As in previous converters Sa1 is a dc rail switch that carries the input current and disconnects the inverter from the source before the change of state in the converter. The capacitor Cc is a large storage capacitor which is pre charged to Vdc/2. The auxiliary circuit initiates by pre charging the inductor Lr to some required boost value (switches Sa1 and Sa2 are on). Once the current ramps up the switch Sa1 turns off to start the resonance between Lr, Cc and snubber capacitors and brings the voltage of Vi to zero. At this point the converter changes the state and the resonance continues between Cc and Lr. The current in Lr starts decreasing. Once the current reverses and passes through the body diode of Sa2, the switch Sa2 can be turned off. Ir continues to decrease and once it reaches the proper value, a new resonance occurs which brings the link voltage Vi back to dc link voltage. The operation of the link finishes with Sa1 being gated on to remain the power flow to the main bridge.

Even though the switches Sa1 and Sa2 operate at zero voltage and the maximum stress on the semiconductor devices is limited to Vdc, the control timing is

complicated and quite challenging to adjust the location and duration of zero voltage for a wide operation range.

2.4.5 Quasi- Resonant DC link by Chen [37]

Another DC link circuit that minimizes the number of auxiliary switches to two is a QRDCL proposed by Chen. Figure 22 shows the link circuit diagram that consists of a dc rail switch Sa1, one auxiliary switch Sa2 two diodes D1, D2, LC resonant circuit, auxiliary capacitor Cc and a magnetically coupled inductor Lr1.

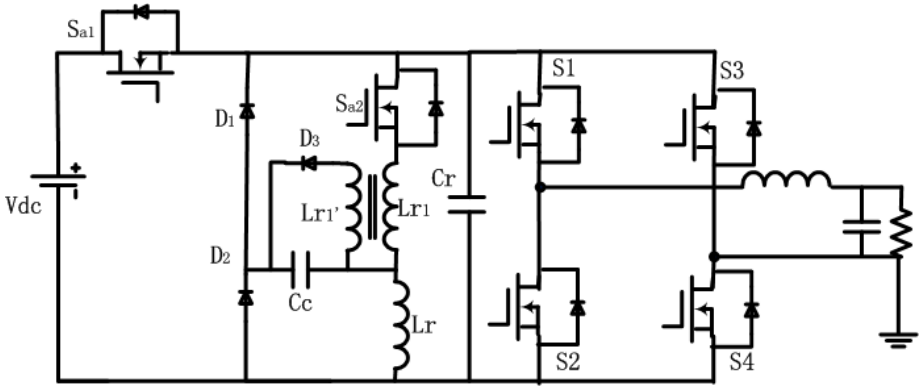


Figure 22 QRDCL by Chen [37]

The initial state of the QRDCL: dc rail switch is on, auxiliary switch is off, link capacitor is charged to the source voltage, Cc is pre charged to a preset value Vo, inductor currents are zero.

As Sa2 turns on, the resonance starts between Cc, Lr1, and Lr. The currents of inductors increase until ILr reaches the preset value. At this moment the dc rail switch turns off the voltage across Cr which decreases to zero due to resonance between Cr,

Lr1 and Lr. As the voltage clamps to zero by the freewheeling diodes, the capacitor Cc, Lr1 and Lr continue to resonate. The voltage of the capacitor Cc decreases to zero. The converter may change the state at any time during this period as the link voltage is kept at zero. The current of inductor Lr freewheels through the diode D2, the inductor current of Lr1 freewheels through the diode D1.

To start bringing the link voltage back to the source voltage Sa2 turns off, and the resonance process starts between Lr1', Lr and Cc. It continues until the inductor currents reduce to zero. As soon as the current of Lr reverses direction, the resonance between Lr, Cc and Cr brings the link voltage back to the source value. At this moment Sa1 can be turned on, however the resonance between Cc, Lr continues until the inductor current is completely discharged.

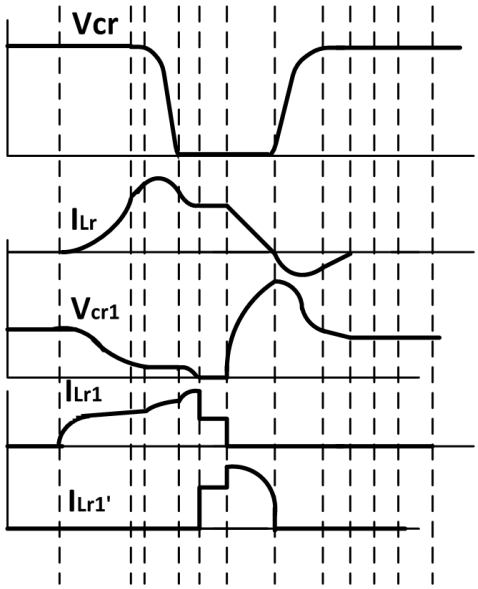


Figure 23 Operation waveforms of the QPRDCL [37]

In this QRDCL switch Sa2 is zero current turn on, and zero voltage turn on, Sa1 is zero voltage turn on/off, however, the circuit requires the addition of three diodes, capacitor Cc and inductor Lr1. The magnetically coupled inductor is bulky which reduces the power density, and moreover brings additional magnetic loss.

CHAPTER THREE: A NEW RESONANT DC LINK FOR SINGLE PHASE MICRO INVERTER WITH THREE AUXILIARY SWITCHES

The survey of the existing inverter topologies has revealed that the ones that have a potential to achieve high efficiency usually employ complicated control strategies and a large number of components; and the ones that have simpler topologies do not meet the expectations on the performance and components stress.

Resonant DC link and Active Clamped Resonant DC Link (ACRDCL), proposed by D.M. Divan [25], [26] use auxiliary switch and resonant components to periodically resonate the DC bus voltage to zero, achieving ZVS for the main switches. However this technique has two major disadvantages: (1) high DC voltage stress on the devices; and (2) high total harmonic distortion caused by difficulties in PWM implementation due to switching at a fixed interval.

The Auxiliary Resonant Commutated Pole (ARCP) technique, proposed by McMurray, can fully achieve soft switching by adding two auxiliary switches and one inductor for each phase [31], [32]. However, the addition of extra components makes the topology and control complicated and costly, especially for low power micro inverter applications, where low cost and simple control are preferred.

The auxiliary quasi-resonant DC link inverter proposed by DeDoncker utilizes three switches; however it has a charge balance problem in DC bus capacitors [35]. The parallel resonant DC link (PRDCL) topology uses four auxiliary switches, but these

switches are turned off with high current and one of them still has a high voltage stress [33].

In order to have a soft switching inverter topology with a simple control and low cost a new quasi resonant DC link with only three auxiliary switches and one LC component is proposed. Since the zero voltage condition can be created anytime by the assistance of the auxiliary switches, there are no requirements on the switching time for main switches, and thus the conventional PWM technique can be easily employed. Furthermore, all these switches including auxiliary switches operate under soft switching conditions.

The operational principle and analysis of the current topology is described along with design considerations and optimization of device selection. The simulation and experimental results for a 150W inverter are presented to verify the circuit operation.

3.1 Derivation of the New Quasi Resonant DC Link Inverter

As illustrated in Figure 24 the philosophy behind quasi- resonant DC link topologies is to employ a dc-rail switch and a controlled LC network as a front stage to the main commutation network. The central part is the dc rail switch that is closed during the normal operation and passed the power to the main circuit. The main idea of quasi-resonant dc link is developed based on disconnecting the main bridge from the source using the dc rail switch during the switching transitions and providing zero voltage switching condition by controlling the resonant branch.

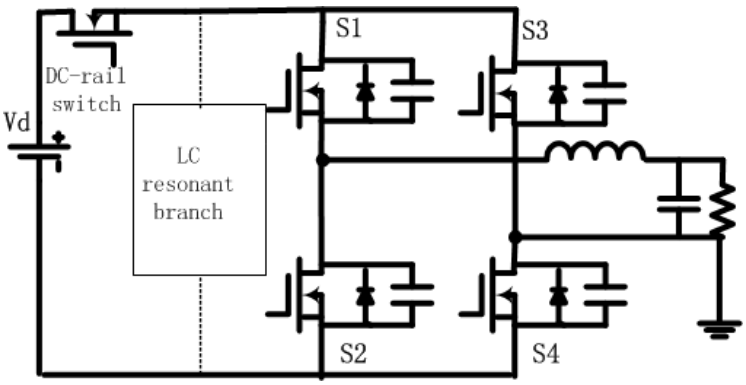


Figure 24 The concept of Quasi-resonant DC link family

3.2 Operational Principle of the New Quasi-resonant DC Link

To illustrate the operational principle, a new resonant DC link is applied to a single phase inverter as shown in

Figure 25. Figure 26 shows the key waveforms during main switch commutation. As seen from that figure, there are seven stages in each commutation period. The detailed explanation of each stage for commutation from S2/S3 to S1/S4 is as follows.

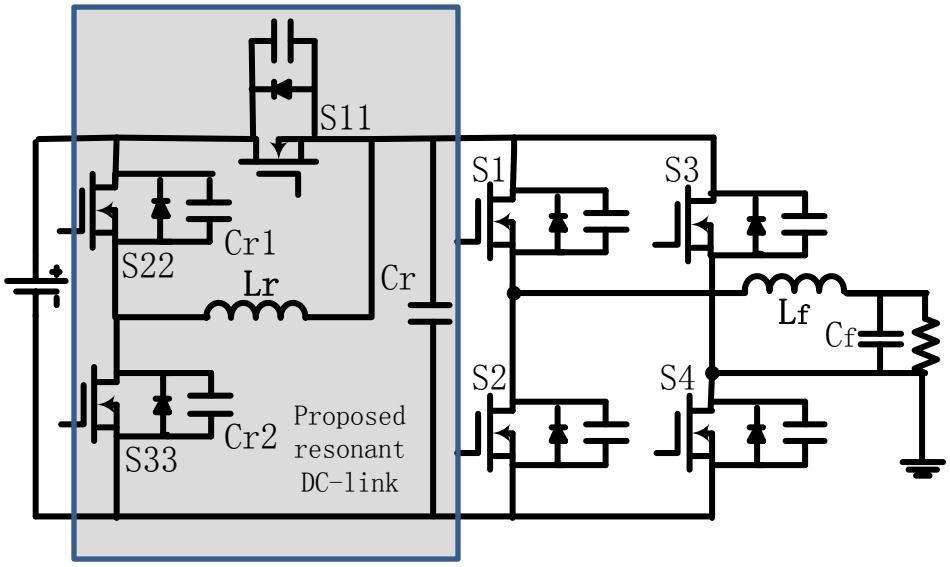


Figure 25 Single-phase inverter with a new resonant DC link

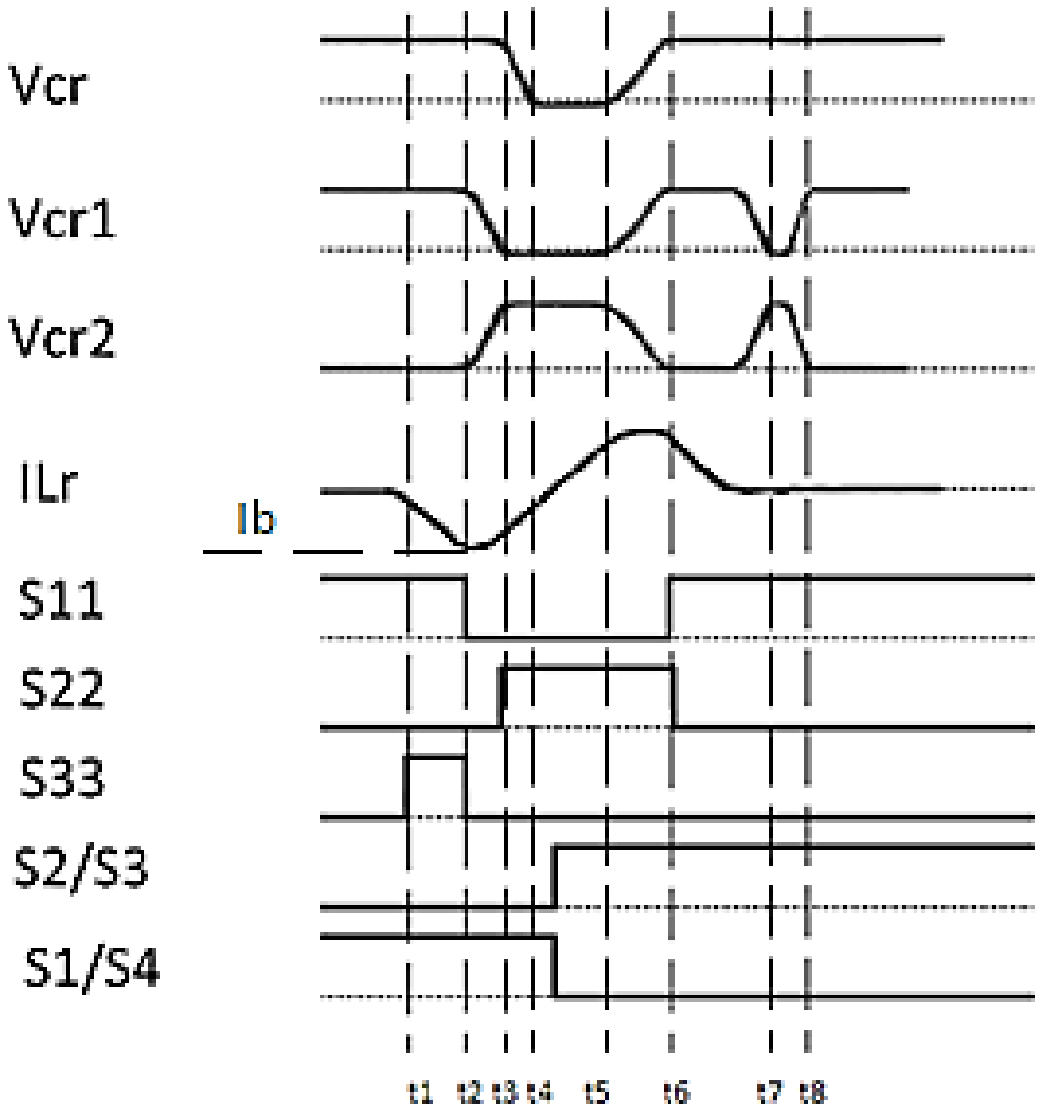


Figure 26 Commutation waveforms

Stage 1(t1-t2):

As shown in Figure 27, in this stage the inductor current is linearly charged by turning on S33. Once the current through Lr reaches the boost current Ib, the switch S33 and

S11 are turned off simultaneously. The current Ib should be sufficient to fully discharge the resonant capacitor Cr. The time duration of this stage can be found from (1):

$$T1 = \frac{Ib \cdot Lr}{Vd} \quad (1)$$

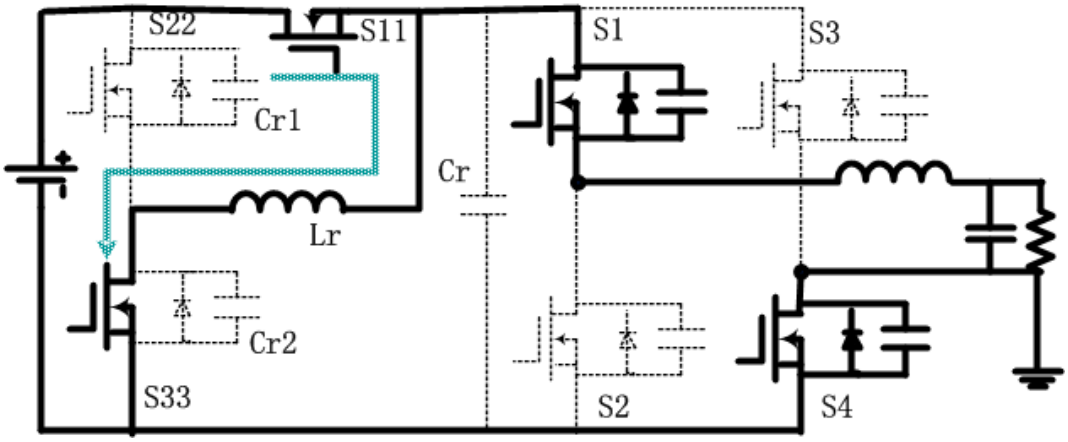


Figure 27 Stage 1 (t1-t2)

Stage 2(t2-t3):

As shown in Figure 28, in this stage, the capacitors Cr1 and Cr2, which are the parasitic capacitors of MOSFETS S22 and S33, are charged and discharged respectively by inductor current Ib. Since the voltage across the Cr1 reaches zero and the body diode of S22 starts conducting (Figure 29), S22 can be turned on with zero-voltage condition. This stage ends once the switch S22 turns on. The time duration of this stage can be expressed by:

$$T2 = \frac{(C_{r1}+C_{r2})Vd}{Ib} \quad (2)$$

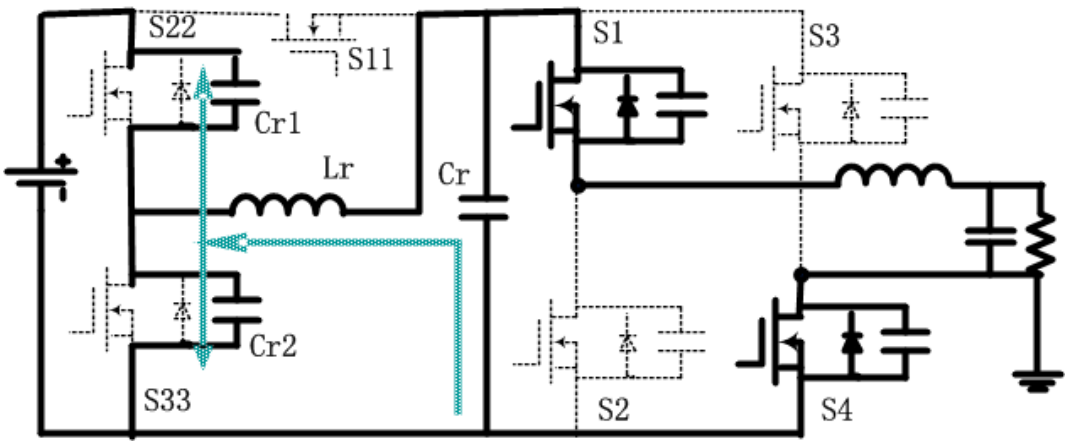


Figure 28 Stage 2 (t2-t3)

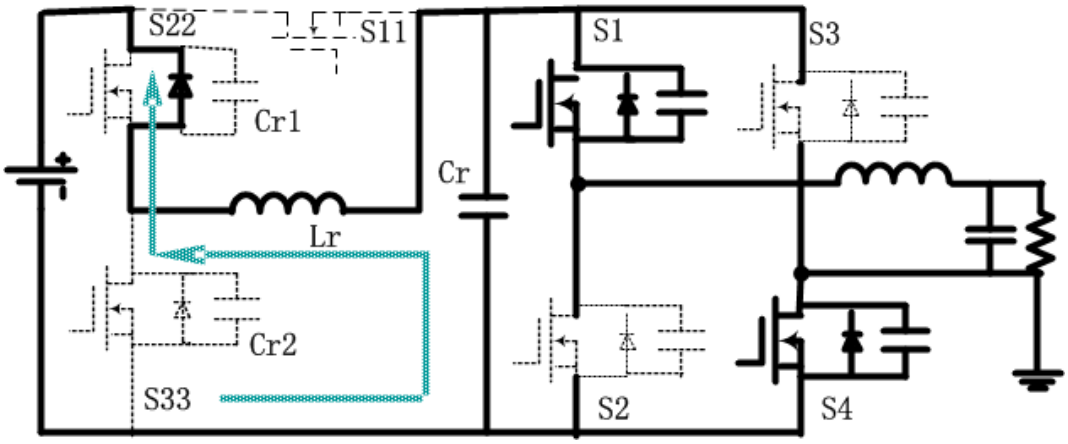


Figure 29 Stage 2 (t2-t3)

Stage3(t3-t4):

During this stage, shown in Figure 30, Lr and Cr begin to resonate. The voltage across Cr decreases as the current in the resonant inductor Lr is negative. In this stage, the load current affects the time duration to resonate the Cr voltage to zero. A positive load

current shortens the time duration, while a negative load current prolongs the time duration. This stage finishes when the voltage across Cr reaches zero. Considering the load current effect, the time duration can be calculated using equations (3), and (4):

$$\mathrm{Vd} + \frac{Ib \pm Iom}{Cr \cdot \omega_d} \cdot e^{-\alpha \cdot T_3} \sin(\omega_d \cdot T_3) = 0 \qquad (3)$$

$$\omega_o = \frac{1}{\sqrt{LC}} \qquad (4)$$

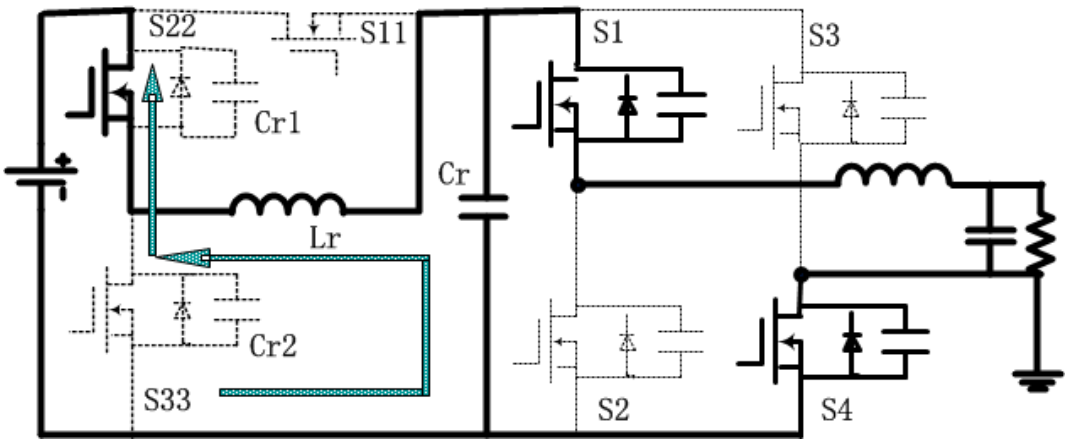


Figure 30 Stage 3 (t3-t4)

Stage4 (t4-t5):

During this stage (Figure 31), the voltage across Cr is clamped to zero as the resonant current flows through the body diodes of the main switches. Because the voltage across the resonant inductor is the constant DC bus voltage, the resonant current linearly decreases to zero. Since the voltage across Cr is maintained at zero, it creates the zero

voltage soft switching condition for the main switches. The main switches can commutate at any time during this stage. The time duration of this stage can be calculated as:

$$i_{lr1} \pm I_{om} = 0 \quad (5)$$

$$i_{lr1} \pm I_{om} = \frac{-Vd \cdot T_4}{Lr} - Id2 \quad (6)$$

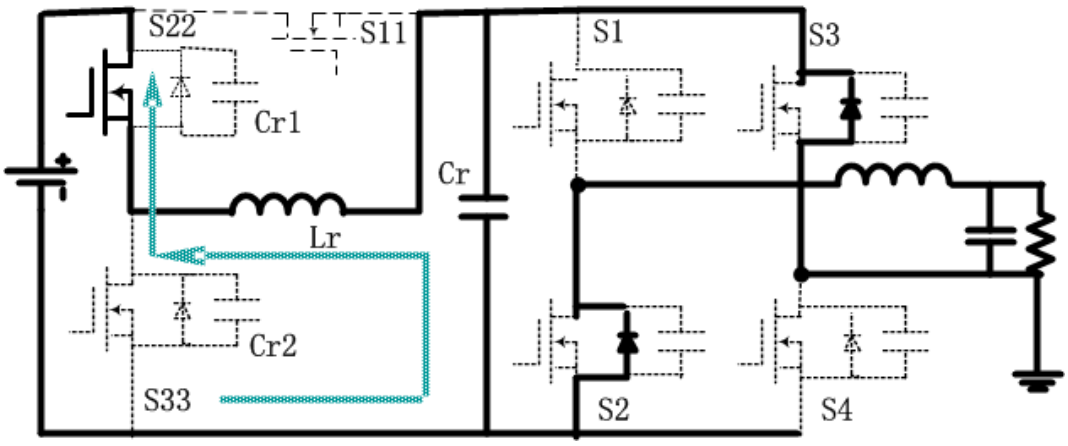


Figure 31 Stage 4 (t4-t5)

Stage5 (t5-t6):

Once the inductor current reaches zero, Lr and Cr will begin to resonate again (Figure 32). They will continue to resonate until the voltage across the Cr is clamped to DC bus voltage by the body diode of S11. The inductor current is circulated through S22 and S11 and remains nearly constant. During this stage, switch S11 turns on with a zero voltage switching condition. This stage ends when switch S22 turns off. The time this stage lasts can be calculated with the following equation:

$$\mathrm{Vd} - \mathrm{Vd} \cdot e^{-\alpha \cdot T_5} \cos(\omega_d \cdot T_5) + \frac{\frac{Ib_{2\pm Iom}}{Cr} + \alpha \cdot Vd}{\omega_d} \cdot e^{-\alpha \cdot T_5} \sin(\omega_d \cdot T_5) = V_d \quad (7)$$

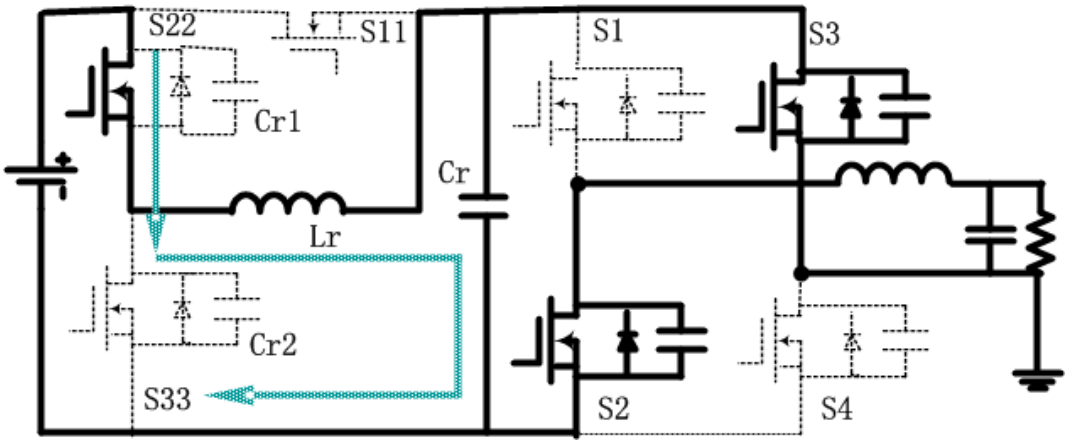


Figure 32 Stage 5 (t5-t6)

Stage 6(t6-t7):

When switch S22 turns off, the remaining current in inductor Lr will be discharged from Cr1 and charged to Cr2 respectively. (Figure 33) After the voltage across Cr1 reaches zero, the remaining energy in the inductor will be dumped to the source through body diode of S22 (Figure 34). This stage ends when the inductor current goes to zero.

$$i_1(T5) - \frac{V_d \cdot T6}{Lr} = 0 \quad (8)$$

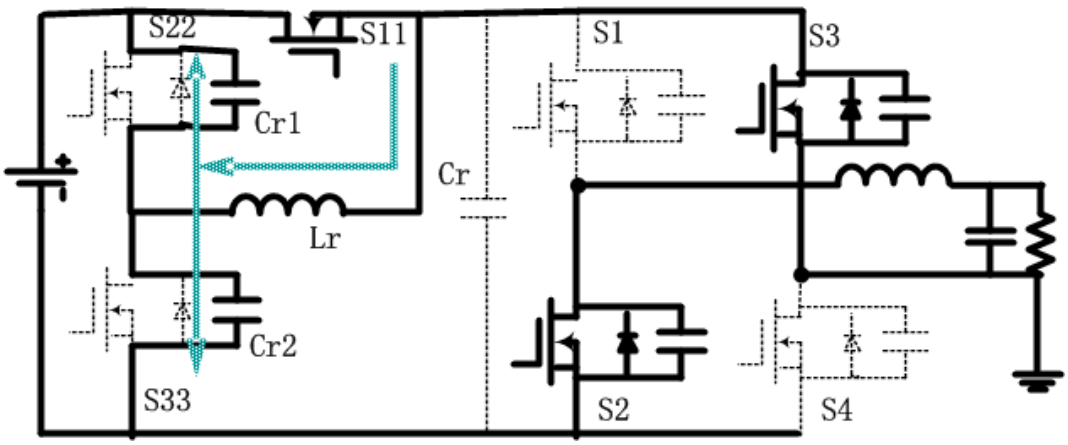


Figure 33 Stage 6 (t6-t7)

Stage 7(t7-t8):

Since the voltage across the S22 is zero at the beginning of this stage, the inductor will be charged and the energy in the inductor will be discharged through the resistance of S11 and S22 (Figure 34). When the energy in the inductor is completely damped, this stage ends and gets ready for next new switch commutation (Figure 35).

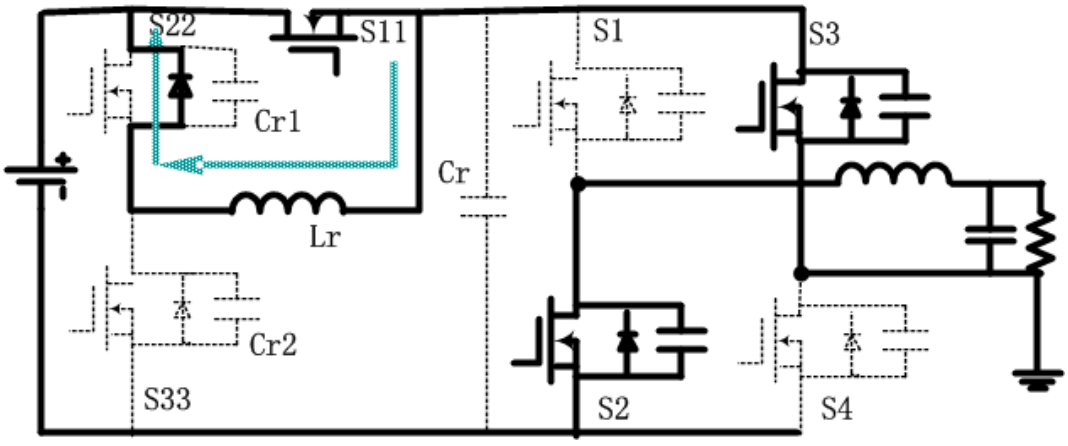


Figure 34 Stage 6 (t6-t7)

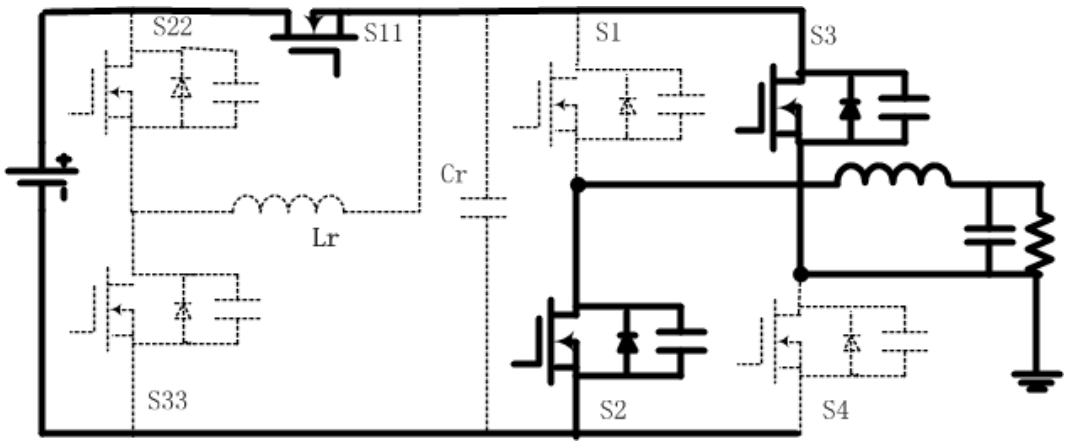


Figure 35 End of commutation

CHAPTER FOUR: POWER LOSS ANALYSIS AND DESIGN CONSIDERATIONS

4.1 Analysis of the Resonant Stages

To investigate the performance of a micro inverter, an accurate loss model is desired. With the use of the model, different design parameters can be compared, and optimized circuit parameters and devices can be selected. Three different loss models have been previously proposed, each one targeting for better precision and shorter calculation time.

The best accuracy can be achieved with the physics-based model. Simulation software, e.g. ISE and Medici perform the analysis using the physical parameters of the device, such as geometry and doping concentration. The results obtained with these type of software match the experimental results quite well. However, it is very inefficient since it takes days to calculate several switching cycles. Clearly, this method is not suitable for the optimization of the micro inverter since several design criteria needs to be evaluated.

The second method is to use the behavior model of the devices that is provided with simulation software such as PSpice/LTSpice and SABER. The parameters such as device parasitic capacitance and on-state resistance are input to the model. This

method presents relatively good results sufficient for comparison of the devices provided by different manufactures. However, it is still time-consuming and therefore not suitable for the evaluation of the micro inverter.

The third method is the mathematical model. Based on some equivalent circuits, and device datasheet parameters provided by manufactures, the power loss equations are derived. Compared to the aforementioned physics-based and behavioral methods, this one is the fastest and has a minimum calculation time. The major obstacle in applying such model is its accuracy. The most simple mathematical loss model uses a simplified turn-on and turn-off switching waveforms [38]. In this model voltage and current are changing in a linear fashion, which is not the case in resonant topologies. Therefore, the results obtained by such model normally do not match the experimental results very well.

In order to boost efficiency and increase power density it is important to evaluate the power loss mechanism in each stage of operation of the micro inverter. Using the datasheet parameters of the commercially available semiconductor switches, conduction and switching losses can be estimated. This chapter presents a method to analyze power losses of the new resonant DC link inverter which alleviates topology optimization and MOSFET selection. An analytical, yet simple model for calculating the conduction and switching losses was developed. With this model a rough calculation of efficiency can be done, which helps to speed up the design process and to increase efficiency.

The analysis of the topology was carried out using the simplified circuit diagram shown in Figure 36. The plots of inductor current (I_{Lr}) and capacitor voltage (V_{cr}) of first

resonance (stage3-t3-t4) and second resonance (stage 5 – t5-t6) are given in Figure 37. Since the operational principle of the new quasi resonant DC link is governed by two resonance processes it is essential to derive the equations of the current and voltage of those stages. Neglecting the output capacitances of the MOSFETs as they are relatively small comparing to dc link capacitor the equations can be generated by analyzing the step response of the series underdamped RLC circuit.

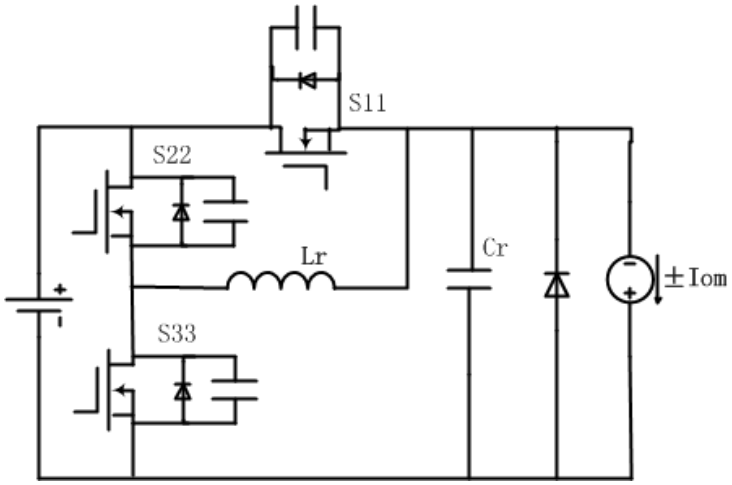


Figure 36 Resonant DC link simplified diagram

First resonance stage (stage 3-t3-t4)

Assuming initial current of the inductor to be equal to Ib (I_{Lr}=Ib) and the capacitor is pre charged to the source voltage (V_{cr}=V_{dc}) the solution of the first resonance [stage 3 (t3-t4)] can be written in the form of equations (1), (2), where

$\alpha = \frac{R}{2L}$ is a damping factor

R- resistance of the resonant circuit (parasitic resistance of inductor and capacitor)

$\omega_0 = \frac{1}{\sqrt{LC}}$ - resonant frequency

$\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ - damped radian frequency

$$\mathrm{Vcr1(t)} = \mathrm{Vd} + \frac{Ib \pm Iom}{Cr \cdot \omega_d} \cdot e^{-\alpha \cdot t} \sin(\omega_d \cdot t) \quad (1)$$

$$I_{lr1}(\mathrm{t}) = \mathrm{Ib} \cdot e^{-\alpha \cdot t} \cos(\omega_d \cdot t) + \frac{\alpha \cdot Ib}{\omega_d} \cdot e^{-\alpha \cdot t} \sin(\omega_d \cdot t) \quad (2)$$

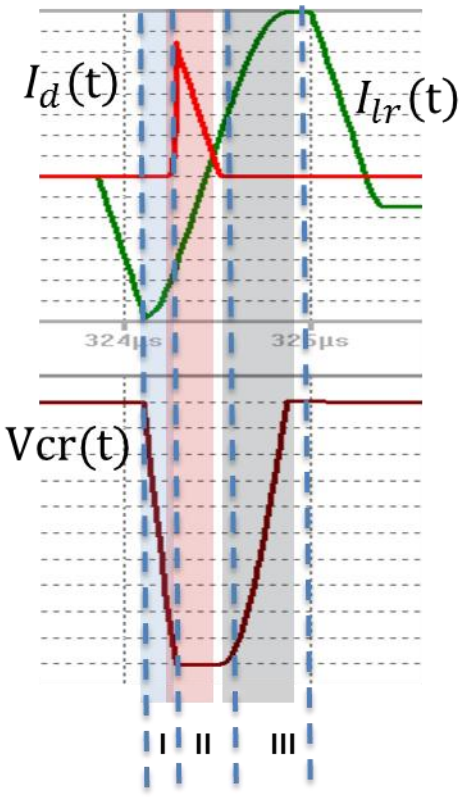


Figure 37 Inductor Current Lr and Capacitor Voltage Vcr (I – first resonance stage (stage 3-t3-t4); II – zero voltage stage (stage 4-t4-t5; III – second resonance stage (stage 5 – t5-t6))

Second resonance stage (stage 3-t3-t4)

For the second resonance [stage 5 (t5-t6)] the initial inductor current is the final value of the inductor current of the zero voltage stage (I_{Lr}=Ib_2) and capacitor is discharged to zero (V_{cr} = 0). Thus, the solution for the second resonance takes the form of equations (3), (4).

$$\mathrm{Vcr2(t)} = \mathrm{Vd} - \mathrm{Vd} \cdot e^{-\alpha \cdot t}\cos(\omega_d \cdot t) + \frac{\frac{Ib_{2\pm Iom}}{Cr} + \alpha \cdot Vd}{\omega_d} \cdot e^{-\alpha \cdot t}\sin(\omega_d \cdot t) \quad (3)$$

$$I_{lr2}(\mathrm{t}) = \mathrm{Ib_2} \cdot e^{-\alpha \cdot t}\cos(\omega_d \cdot t) + \frac{\frac{Vd - \mathrm{Ib_2} * Rlr}{Lr} + \alpha \cdot \mathrm{Ib_2}}{\omega_d} \cdot e^{-\alpha \cdot t}\sin(\omega_d \cdot t) \quad (4)$$

Since the simplified circuit is used for the analysis it can be assumed that for commutation from S2/S3 to S1/S4 the load current, denoted here as Iom, is positive and for commutation from S1/S4 to S2/S3 Iom is negative. The plots of inductor current (I_{Lr}) and capacitor voltage (V_{cr}) of first resonance (stage 3-t3-t4) and second resonance (stage 5 – t5-t6) based on equations (1), (2), (3), and (4) are shown in Figure 38 and Figure 39. It can be seen that commutation from S1/S4 to S2/S3 is much shorter because the load current assists the charging and discharging of the resonant capacitor.

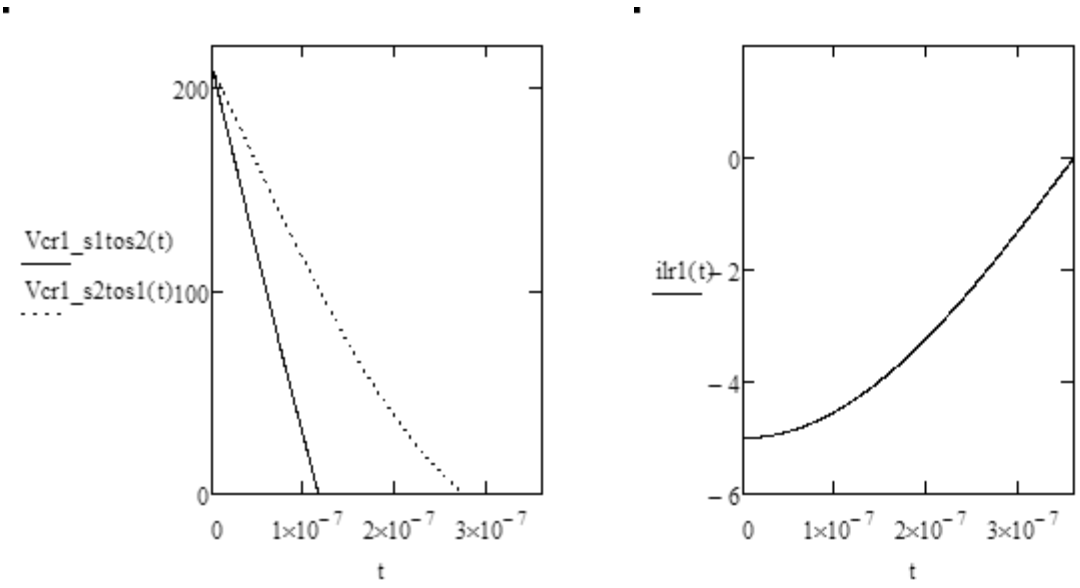


Figure 38 First Resonance (stage 3- t3-t4)

Power loss of a new resonant dc-link inverter consists of four major parts of losses:

conduction losses of main switches (Ponm),

conduction losses of auxiliary switches (Pona),

switching losses of main switches (Pswm),

switching losses of auxiliary switches (Pswa)

core loss of the inductor (Lr).

Conduction loss is resulting from the loss on the Mosfet switch inherent resistance (Rdson) whenever the current passes through it in the on- state. Switching loss is the outcome of the non-ideality of the Mosfet switching waveforms and thus, current and voltage overlap during the switching.

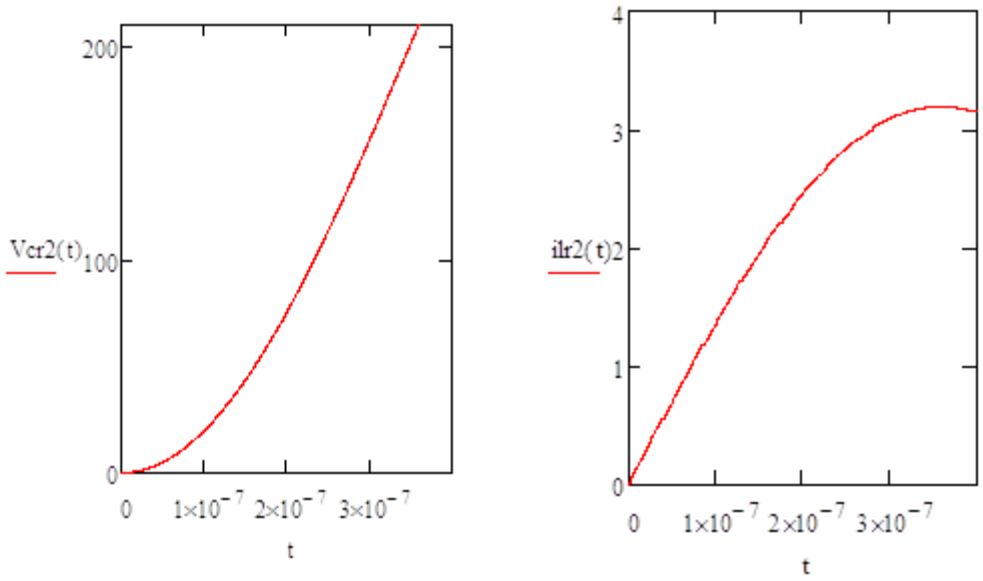


Figure 39 Second Resonance (stage 5- t5-t6)

4.2 Calculation of the Inductor Charging/Discharging, Resonant and Linear Stage Time

Power loss calculation of the new quasi- resonant dc-link inverter requires the knowledge of the time it takes to resonate the dc-link capacitor voltage to zero (t3-t4) and then resonate it back to source voltage (t5-t6), as well as the time of pre charging the inductor (t1-t2) and discharging it back to zero (t6-t7) [Figure 40].

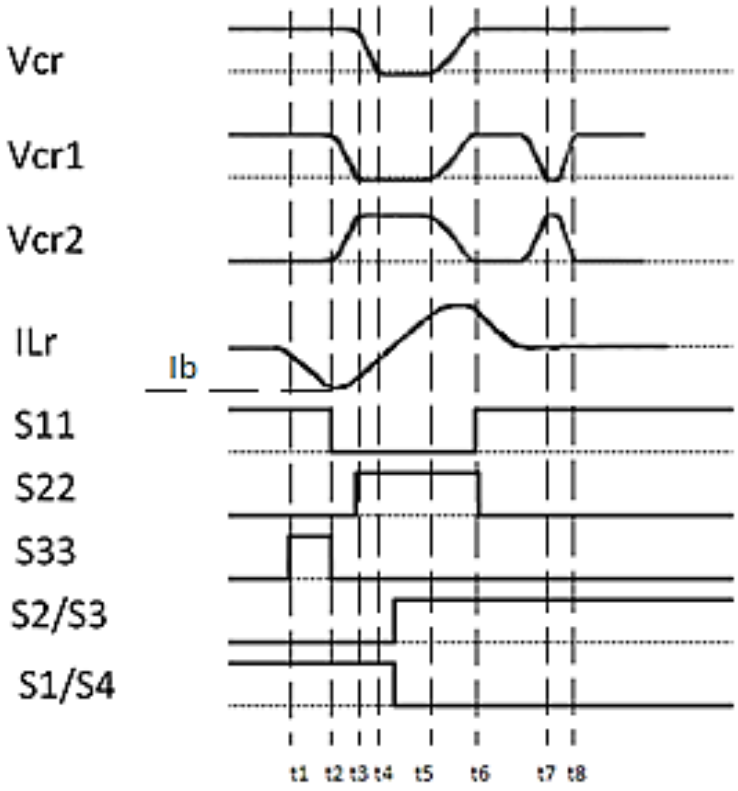


Figure 40 Timing diagram of the operation

Recalling that the first stage time T1 (t1-t2) is the time once the inductor current reaches Ib, the boost time T1 can be calculated by (5)

$$\frac{V_d \cdot T_1}{Lr} = I_b \tag{5}$$

As in stage 2, the capacitors Cr1 and Cr2, which are the parasitic capacitors of MOSFETS S22 and S33, are charged and discharged respectively by inductor current Ib the time duration of this stage can be expressed by:

$$T_2 = \frac{(C_{r1}+C_{r2})Vd}{Ib}$$

The first resonance stage time T3 (t3-t4) is the time once the voltage across the resonant capacitor Cr reaches zero, therefore the resonant stage period T3 can be obtained by (6)

$$\mathrm{Vd} + \frac{Ib \pm Iom}{Cr \cdot \omega_d} \cdot e^{-\alpha \cdot T_3} \sin(\omega_d \cdot T_3) = 0 \quad (6)$$

The third stage (which is denoted here as the linear process, stage 4) time T4 (t4-t5) is the time of the zero voltage stage. The dc link capacitor won't start charging to dc link voltage until the inductor current reaches the output current. The voltage Vd is applied across the inductor in this stage and the current increases linearly, therefore the time of this stage can be found considering (7) and (8)

$$i_{lr1} \pm I_{om} = 0 \quad (7)$$

$$i_{lr1} \pm I_{om} = \frac{-Vd \cdot T_4}{Lr} - Id2 \quad (8)$$

The fourth stage time T5 (t5-t6) is the time the voltage across the resonant capacitor Cr reaches Vdc and calculated by (9)

$$\mathrm{Vd} - \mathrm{Vd} \cdot e^{-\alpha \cdot T_5} \cos(\omega_d \cdot T_5) + \frac{\frac{Ib_2 \pm Iom}{Cr} + \alpha \cdot Vd}{\omega_d} \cdot e^{-\alpha \cdot T_5} \sin(\omega_d \cdot T_5) = V_d \quad (9)$$

The fifth stage time T6 (t6-t7) is the time once the inductor current goes down to zero thus time period T6 could be found solving the equation (10).

$$i_1(T5) - \frac{V_d \cdot T6}{Lr} = 0 \quad (10)$$

4.3 Conduction Loss Calculation

Main switches

Conduction loss of the main switches is resultant from the loss on the Mosfet switch inherent resistance (Rds on) whenever the output current passes through it in the on-state and is obtained by (11), where io(t)-ouput current, d(t)-duty cycle, md – modulation index and can be obtained by (12) and (13), and (14) respectively.

$$Ponm = 4 \cdot Rdson \cdot fo \cdot \int_0^{\frac{\pi}{\omega}} (i_0(t))^2 \cdot d(t) \quad (11)$$

$$io(t) = Iom \cdot \sin(\omega t) \quad (12)$$

$$d(t) = \frac{1}{2}(1 + m_d \sin(2 \cdot \pi \cdot f_0 \cdot t)) \quad (13)$$

$$m_d = \sqrt{2}\frac{V_0}{V_d} \quad (14)$$

Auxiliary switches:

Conduction loss of auxiliary switch S11 consists of pre-charging and discharging of inductor current and output current losses (15).

$$Pons11 = Rdson \cdot Io^2 + \frac{4}{3} \cdot fsw \cdot Rdson \cdot (\frac{Vd}{Lr})^2 \cdot T1^3 + \frac{4}{3} \cdot fsw \cdot Rdson \cdot (\frac{Vd}{Lr})^2 \cdot T5^3 \quad (15)$$

Conduction loss of auxiliary switch S22 is from carrying second resonance current and is obtained by (16).

$$Pons22 = 2 \cdot fsw \cdot Ron \cdot \left[\int_0^{T3} (i_{lr2}(t))^2 dt\right] \quad (16)$$

Conduction loss of auxiliary switch S33 is of pre-charging stage and is easily calculated from (17).

$$Pons33 = \frac{2}{3} \cdot fsw \cdot Ron \cdot (\frac{Vd}{Lr})^2 \quad (17)$$

4.4 Switching Loss Calculation

Main switches

Since the main switches turn on and turn off at zero voltage, main switch loss is eliminated.

Auxiliary switches

Switches S11 and S22 are ZVS turn on and turn off.

The total switching loss (Psws33) of s33 consists of Turn on loss (Pswon), Output capacitor loss (Pswc), Turn off loss (Pswoff) (18).

$$Psws33 = 2 \cdot fsw(Pswon + Pswc + Pswoff) \quad (18)$$

$$Pswc = \frac{1}{2} \cdot Coss \cdot \left(\frac{Vd}{2}\right)^2 \quad (19)$$

$$Pswon = \int_0^{tri} u_a(t) \cdot i_a(t) \cdot dt \quad (20)$$

$$Pswoff = \int_0^{tri} u(t) \cdot i(t) \cdot dt \quad (21)$$

Turn on, turn off and output capacitance losses can be found from (18), (19), (20) and (21), where

Coss – output capacitance of the Mosfets and can be obtained from the datasheet

$\mathrm{i_a(t)}$, $\mathrm{u_a(t)}$- expression of the current and voltage during turn on (22), (23)

$$i(t) = \frac{Vd \cdot t^2}{2 \cdot Lr \cdot tri}) \quad (22)$$

$$u(t) = Vd \cdot (1 - \frac{t}{tri}) \quad (23)$$

$\mathrm{i(t)}$, $\mathrm{u(t)}$- expression of the current and voltage during turn off (24), (25)

$$i(t) = -Ib(1 - \frac{t}{tfi}) \quad (24)$$

$$u(t) = -(\frac{Ib - Iom}{Cr \cdot \omega d} \cdot e^{-\alpha t} \cdot sin(\omega d \cdot t)) \quad (25)$$

4.5 Inductor Core Loss

The core loss is caused by the hysteresis loss. For the calculation of the core loss, the empirical formula described by (26) is frequently used in industry [39].

$$Pc = k \cdot Vc \cdot f^n \cdot B^m, \quad (26)$$

where Vc – volume of the core,

f – switching frequency,

B- maximum flux density,

k, n, m – inherent material constants,

4.6 Power Loss Calculation Result and Design Considerations

The power loss estimation was done for 210W inverter by using simulation and mathematical calculation method. The parameters for the calculation were obtained from the datasheets of the commercially available semiconductor switches. The characteristics of the power mosfet used for calculations are given next.

N-channel MDmesh Power MOSFET STB42n65m5

ID Drain current (continuous) at TC = 100 °C - 20.8A

V(BR)DSS Drain-source breakdown voltage - 650 V

RDS(on Static drain-source on resistance - 0.070 Ω

Coss Output capacitance at VDS = 100 V - 110pF

Tr Rise time - 24ns

Tf Fall time - 13ns

The core loss was calculated for TDK PC40 material. The empirical formula for core loss Pc (W/m3) was found from the manufacture's application notes and is presented in (27) with B – maximum flux density (200 Tesla).

$Pc = 2.72 \cdot 10^{-5} \cdot B^{2.85}$ (f=50KHz, t=80℃) (27)

The calculation result shows that inverter still has a very good efficiency of above 98%:

Switching main – 0W

Switching auxiliary - .261W

Conduction main – 0.938W

Conduction auxiliary – 0.287W

Core loss – 0.105 W

Total loss – 1.591W

Figure 41 shows loss chart for the given inverter switching frequency *f* =20 kHz (boost current Ib=7A, resonant frequency fr=700kHz).

Considering only the switching and the conduction loss of main and auxiliary components the overall new resonant Dc-link inverter loss results in 1.5W; and that corresponds to 99% efficiency.

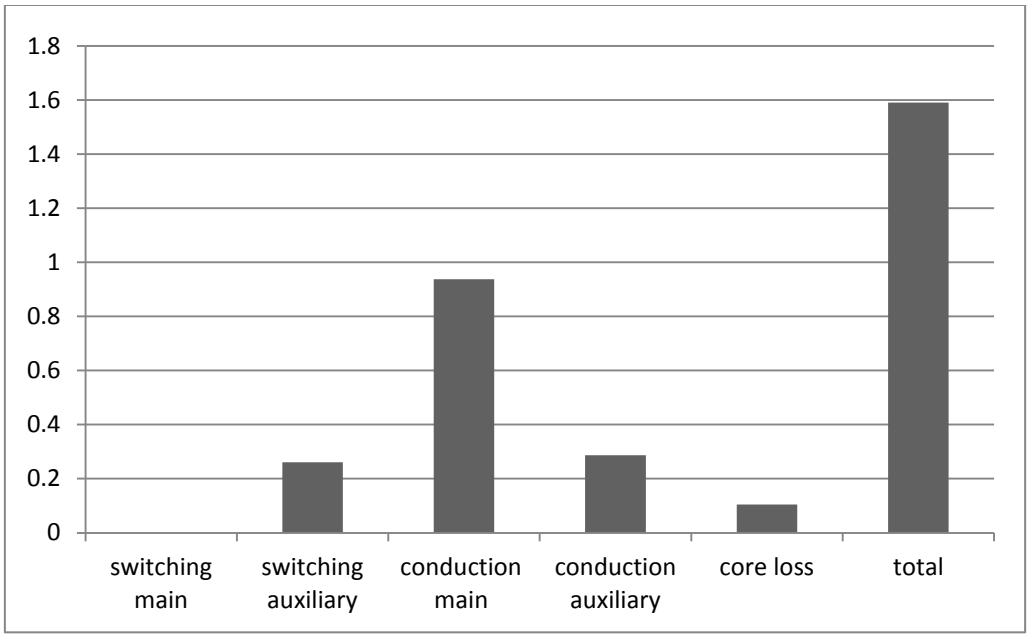


Figure 41 Losses of resonant dc - link inverter

CHAPTER FIVE: SIMULATION AND EXPERIMENTAL RESULTS

5.1 Simulation Results

To verify the proposed quasi resonant DC link, the simulation was carried out using LTspice circuit simulation software.

The key circuit parameters in this simulation are:

DC Voltage - 210V,

power rating - 150W,

switching frequency - 20kHz,

resonant frequency – 700kHz,

resonant inductor Lr - 15uH,

resonant capacitor - 3.3nF.

Figure 42 shows the key waveforms for dc link capacitor voltage V_{cr}, inductor current I_{Lr} as well as gate signals of auxiliary devices (S11, S22 and S33) during the main switch commutation. The figure shows that by triggering the auxiliary switches in the way discussed in the operational principle, zero voltage is created across the DC link capacitor Vcr.

As seen from Figure 43, where S1 and S2 are main switch signals and Vs1 and Vs2 is the voltage across them, during the interval when the voltage across Cr goes to zero which means the voltage across the main switches (Vs1 and Vs2) becomes zero,

main switches S1 and S2 turn on and off respectively, resulting in zero-voltage switching.

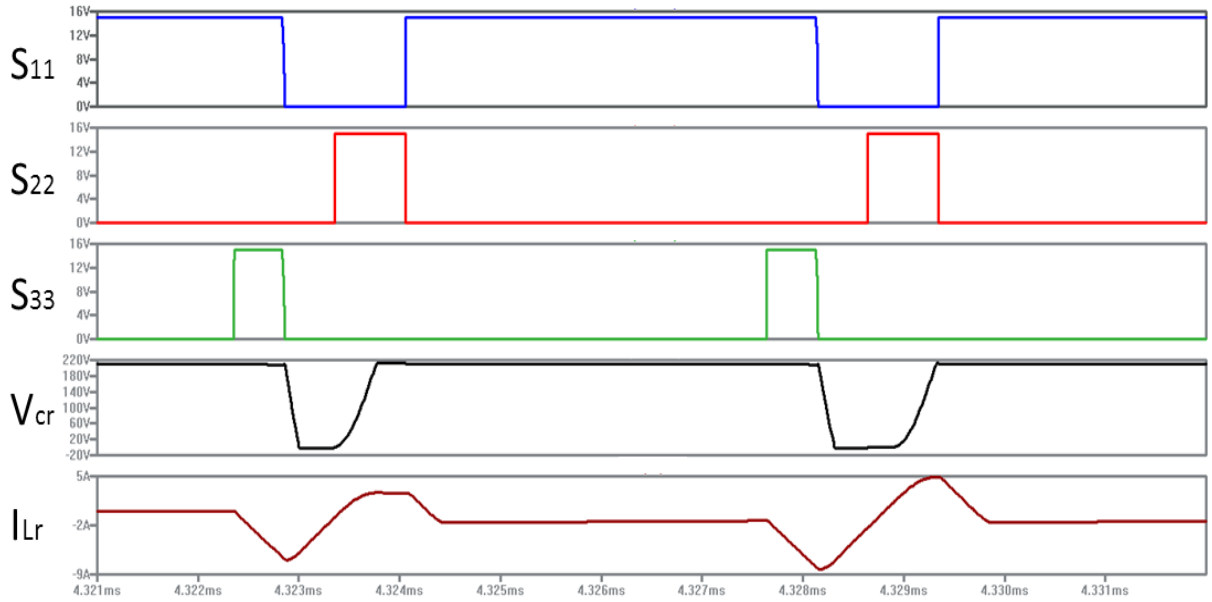


Figure 42 Auxiliary switch signals (S11,S22 and S33), DC link capacitor voltage Vcr and inductor current ILr

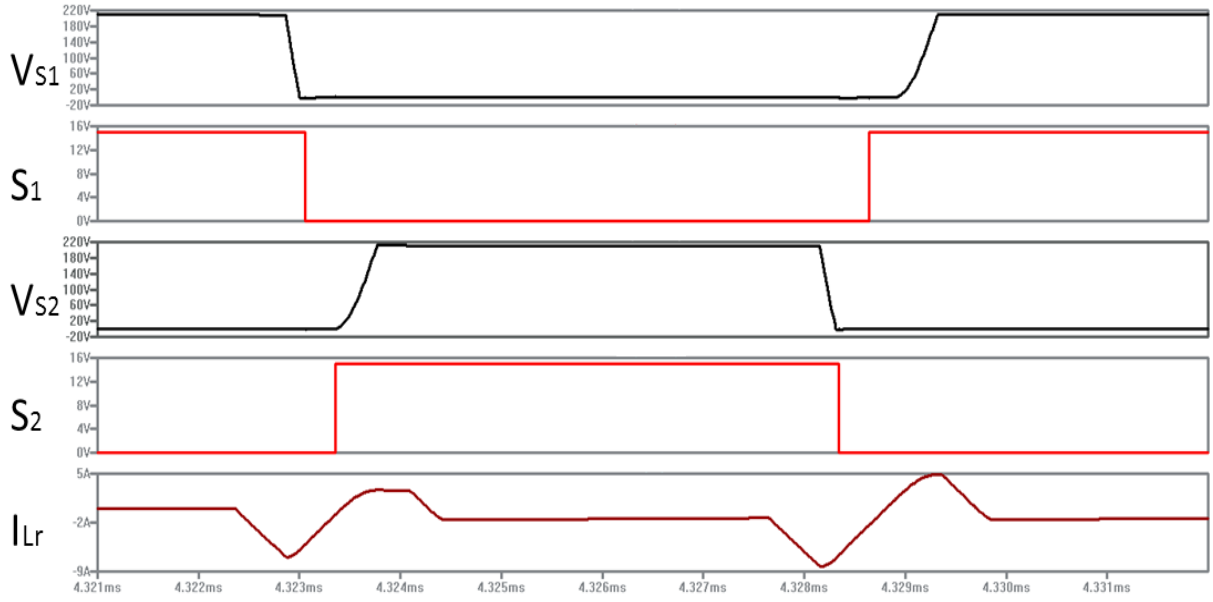


Figure 43 Inductor current ILr, main switch signals S1, S2 and voltage across them Vs1 and Vs2

Since for the new quasi – resonant DC link the resonant cycles can be triggered any time the switching is required in the main bridge circuit, the conventional sinusoidal PWM was applied. As a result, the output is pure sinusoidal with low THD as illustrated in Figure 44.

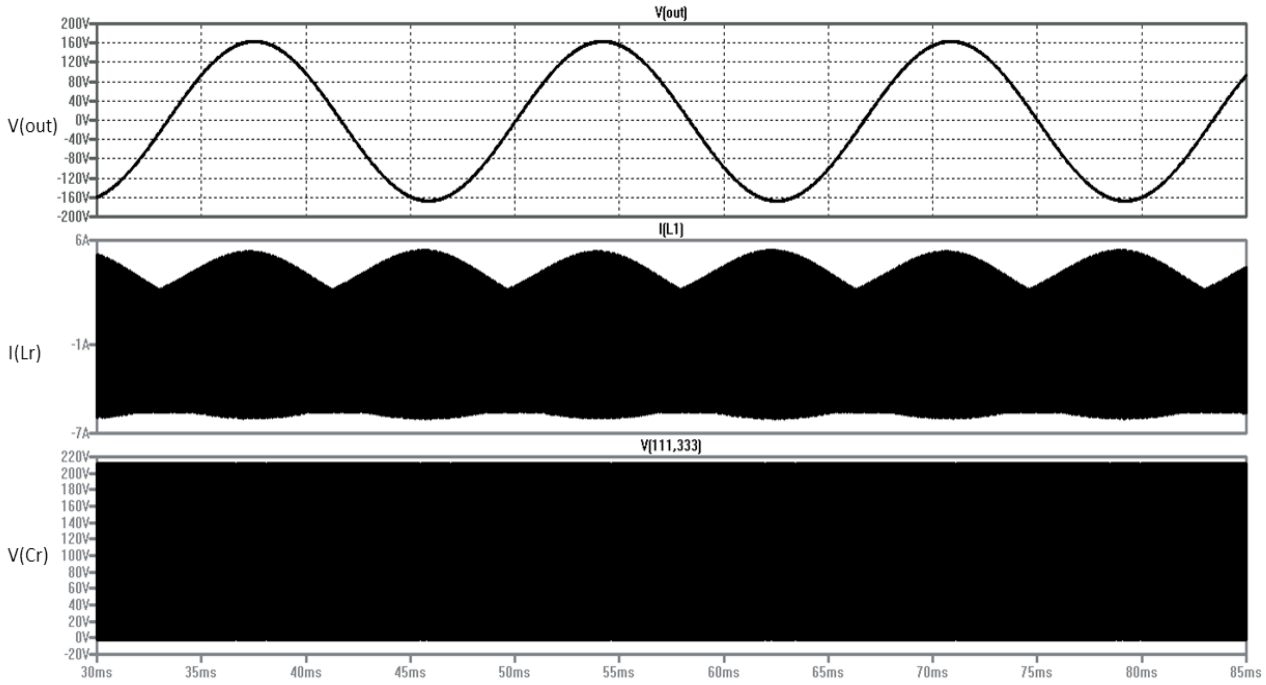


Figure 44 Output voltage, inductor current(Ilr), dc link capacitor voltage (Vcr)

Constant vs. Variable Time Control Strategies

Control timing for auxiliary devices S11, S22 and S33 is presented in Figure 45. The time duration of the switch S33 should be enough to pre-charge the inductor Lr to the value sufficient for the capacitor voltage Cr resonates to zero. From the simulation the minimum gate time for S33 is 500ns and the minimum initial current is 7A. The time durations of the first resonance stages at the peak of the output current is 300ns, and that matches the result obtained from the analysis. The dead time set to 300ns.

As analyzed in Chapter 4, the load current will change the time duration of the second resonance stage. Figure 45 shows that switching from S1 to S2 (on the left) is much shorter than from S2 to S1. It can be seen that in the second case the voltage of the capacitor Cr does not start resonating as soon as the switch S22 is gated on. The resonant process begins as soon as the inductor current rises above the value of the output current.

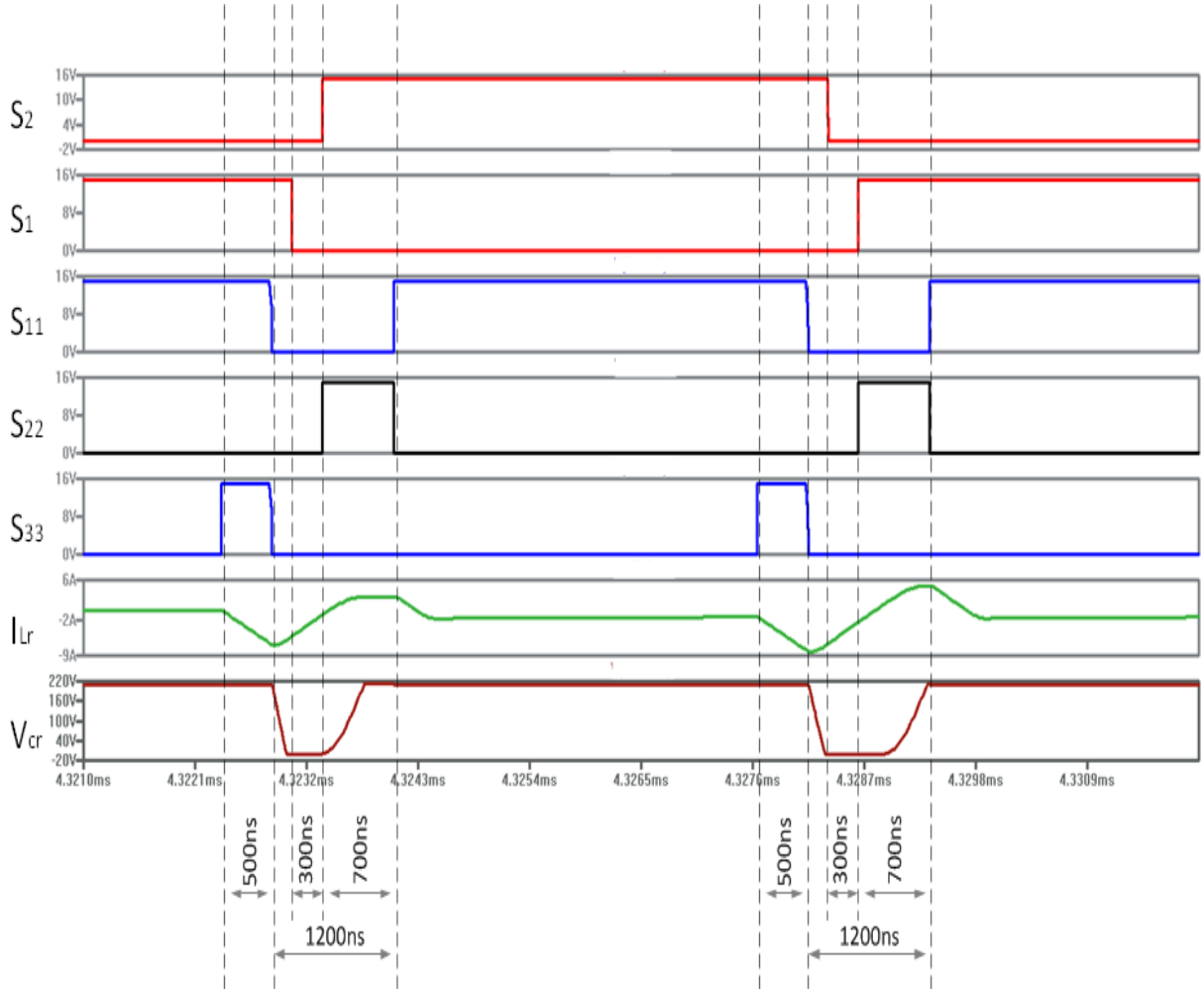


Figure 45 Control timing for main (S1, S2) and auxiliary switches (S11, S22 and S33)

The simulation shows the time of the second resonance is 500ns for the case of commutation from S1 to S2 and 700ns for the commutation from S2 to S1. Therefore, the time duration for the switch S22 is set to 700ns to ensure the voltage of the capacitor Cr has enough time to reach DC bus value (210V) in both case scenarios.

Since the time duration of the second resonance significantly varies depending on the commutation, a variable time control strategy can be implemented. As shown in Figure 46 the switch S22 is gated on for only 500ns for the case of switching from S1 to S2.

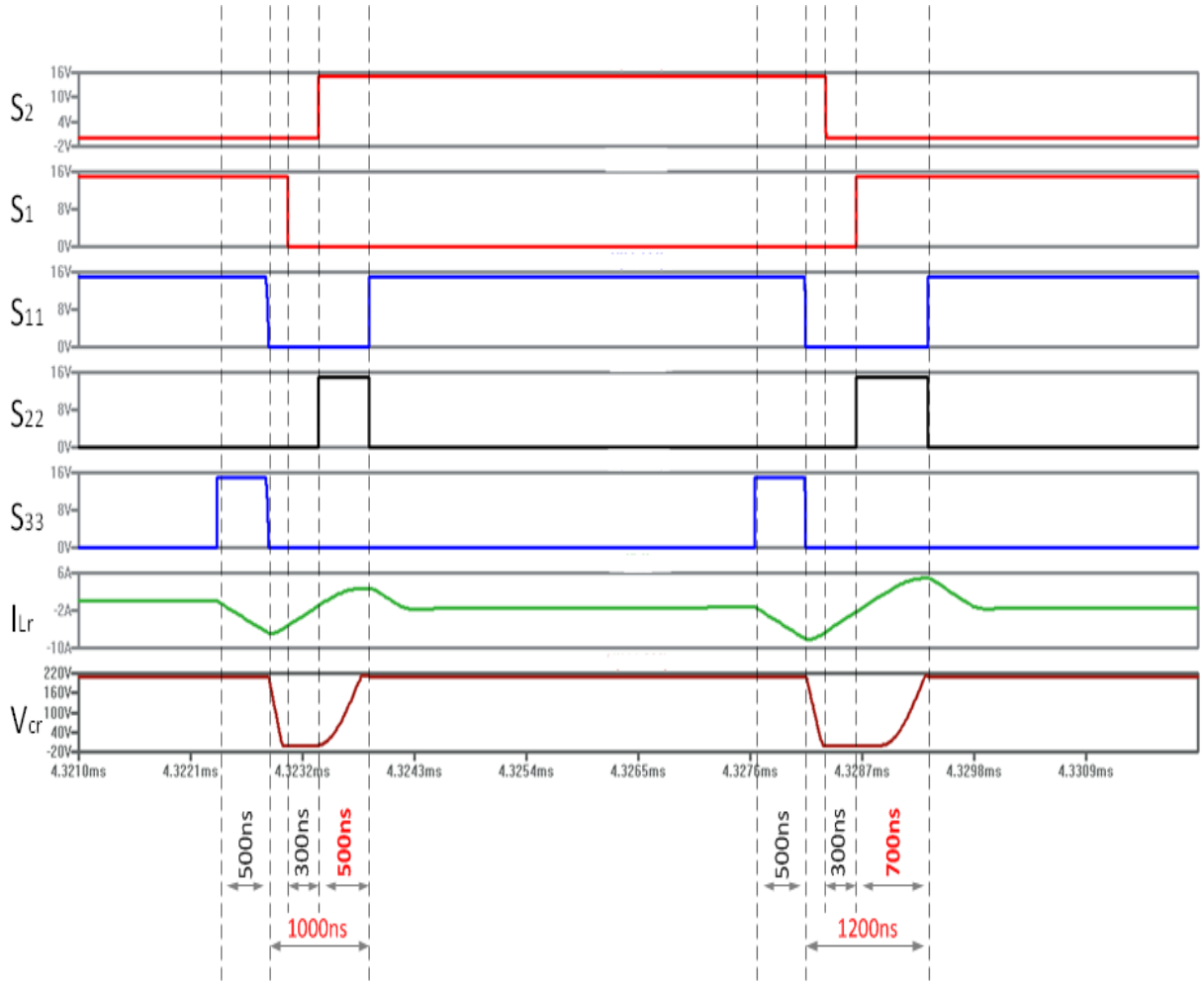


Figure 46 Control timing for main (S1, S2) and auxiliary switches (S11,S22 and S33) with variable time control strategy

As the switch S22 is carrying the resonant current, the reduction of the gating time by 200ns can tremendously reduce the conduction loss. As analyzed in chapter 4 the significant portion of the losses comes from the conduction of the auxiliary switches, thus by adopting the variable time control strategy the overall efficiency can be considerably increased.

The control strategy can be further improved by incorporating the output current sensing and implementing the adaptive control strategy in which the time duration of the auxiliary switches will vary depending on the value of the output current.

The time duration of the auxiliary switch signals can be also optimized by changing the resonant frequency and optimizing the values of L and C. Table 3 shows optimization example. For low resonant frequency the time duration of the resonant stages is prolonged which results in decrease of efficiency. By intuition the designer would want to increase the resonant frequency to shorten the conduction time of the auxiliary circuit. However, there is a limitation caused by the insertion of the dead time between the main switch commutation. Inverter has to maintain zero voltage stage for a time set by dead time in order to ensure both turn on and turn off of the switches are at the zero voltage condition. Thus, with high resonant frequency it is only possible with high initial boost current which increases the current stress on the auxiliary switches and decreases efficiency.

Table 3 Optimization of the resonant frequency

f_res	L	C	S11	S22/2nd resonance	S33	total	Ib	Pin	Pout	efficiency
500K	22uH	4.5nF	1900ns	1200ns	700ns	2500ns	8A	148.21	144.21	97.3
			1800ns	1400ns	900ns	2800ns	9A	149.24	144.4	96.7
700K	15uH	3.3nF	1250ns	750ns	500ns	1750ns	8A	149.21	145.48	97.5
1000K	11uH	2.3nF	1200ns	700ns	600ns	1800ns	12A	151.41	145.65	96.2

Since LTSpice software includes the models of commercially available devices, it is possible to estimate conduction and switching losses and evaluate the efficiency. The simulation was performed with SPA11N60C3 from Infineon (Vds=650V, Id=11A, Rdson=340mOhm) and STP8NM60 from STMicroelectronics (Vds=650V, Id=8A, Rdson=900mOhm). Analysis of the simulation shows that the proposed soft switching technique can achieve up to 97% efficiency, excluding inductor losses and driver losses. Implementation of the variable time control strategy showed the reduction of the power loss and boost of efficiency by almost 1%.

5.2 Experimental Results

A 150W 120VAC single-phase inverter prototype as shown in Figure 47 is built to verify the feasibility of the proposed topology.

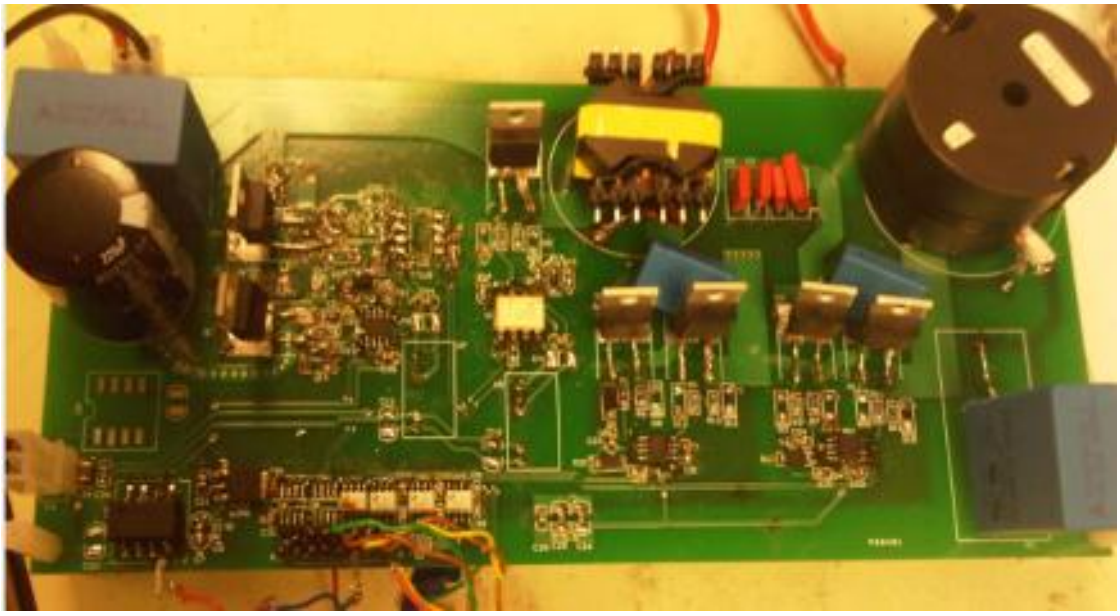


Figure 47 150W 120VAC prototype

The key hardware prototype parameters for the experiment are:

DC Voltage - 210V,

power rating - 150W,

switching frequency - 20kHz,

resonant frequency – 700kHz,

resonant inductor Lr - 15uH,

resonant capacitor - 3.3nF.

All of the main and auxiliary switches used in this prototype are *21N65M5*. The parameters of the LC filter are 2.3mH and 2.2uF respectively.

The control is implemented in a DSP (TMS320F28335 from Texas Instrument). TI DSP has a feature of pulse placement that allows for setting of the rising and falling edges of the pulse anywhere within PWM cycle. This is achieved by configuring the

compare values (CMPA and CMPB) of each of the PWM modules. Once the PWM counter reaches compare value CMPA the pulse initiates; and the pulse ends at the compare value of CMPB.

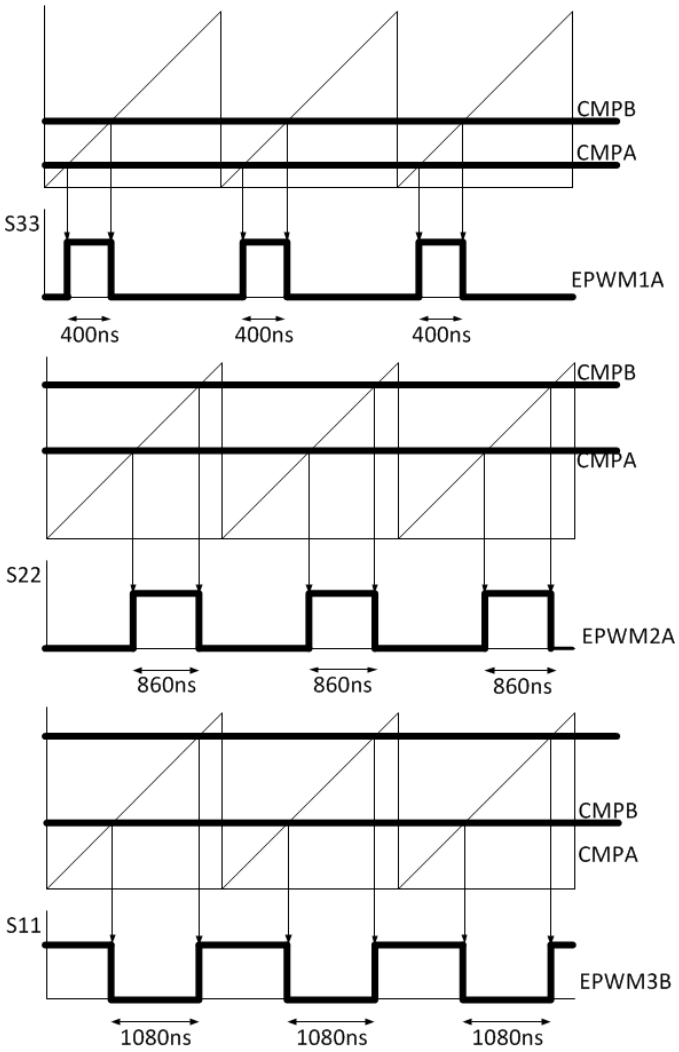


Figure 48 Implementation of the pulse positioning and the control timing diagram of auxiliary switches S11, S22 and S33

Figure 48 shows the implementation of the pulse placement for the new quasi resonant dc link. The driver signals for the auxiliary switches S11, S22 and S33 are

calculated according to the main switch commutation point and time durations are given in Figure 48.

Figure 49 shows the commutation waveforms for the driver signals of auxiliary switches S11 (channel 1), S33 (channel 3), S22 (channel 4) and the voltage across the DC link capacitor Cr (channel 2). The experimental results show that ZVS is achieved for the switches S11 and S22.

Figure 50 shows the current of inductor Lr and the driver signals of the switches S11 (channel2), S22 (channel1) and S33 (channel4). One can see that ZCS is achieved for the auxiliary switch S33 as the inductor current completely discharges prior to the next switching instance of the switch S33.

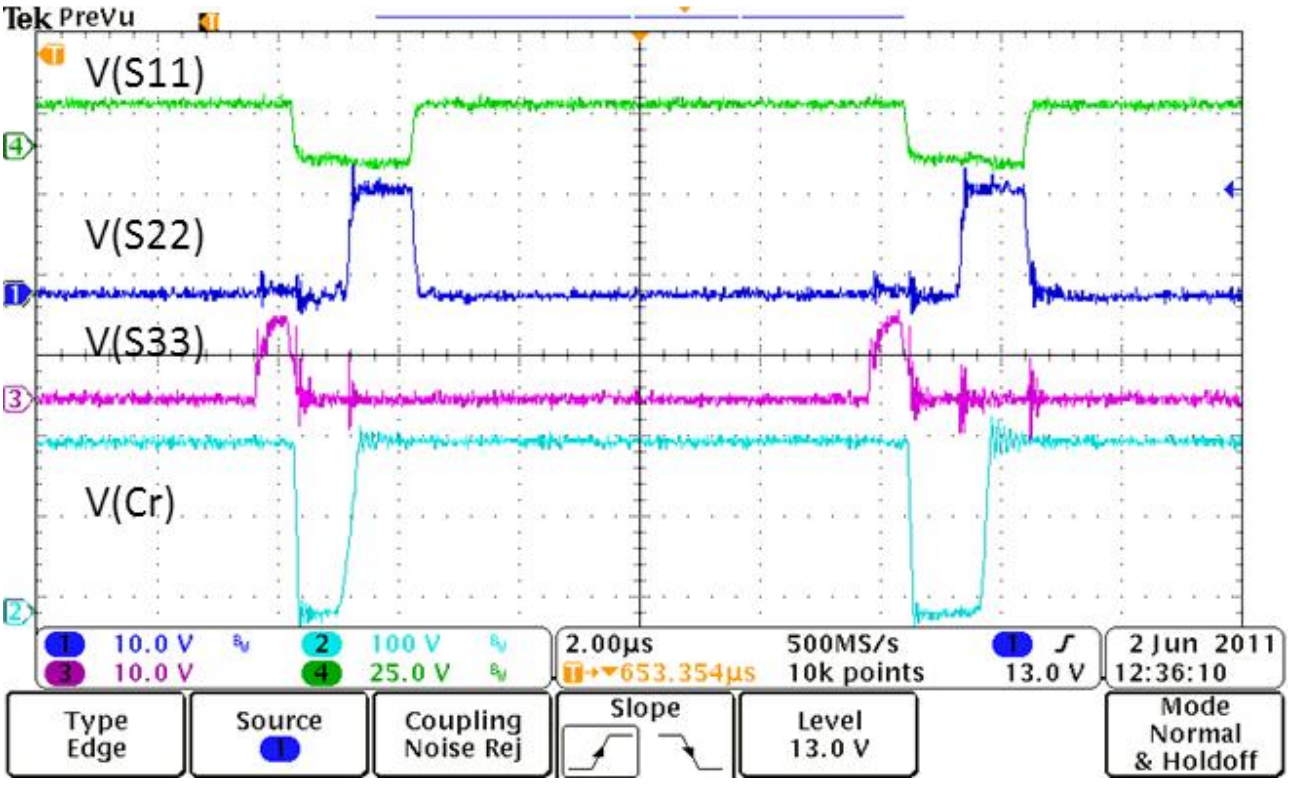


Figure 49 Auxiliary switches driver signals and Voltage across Cr

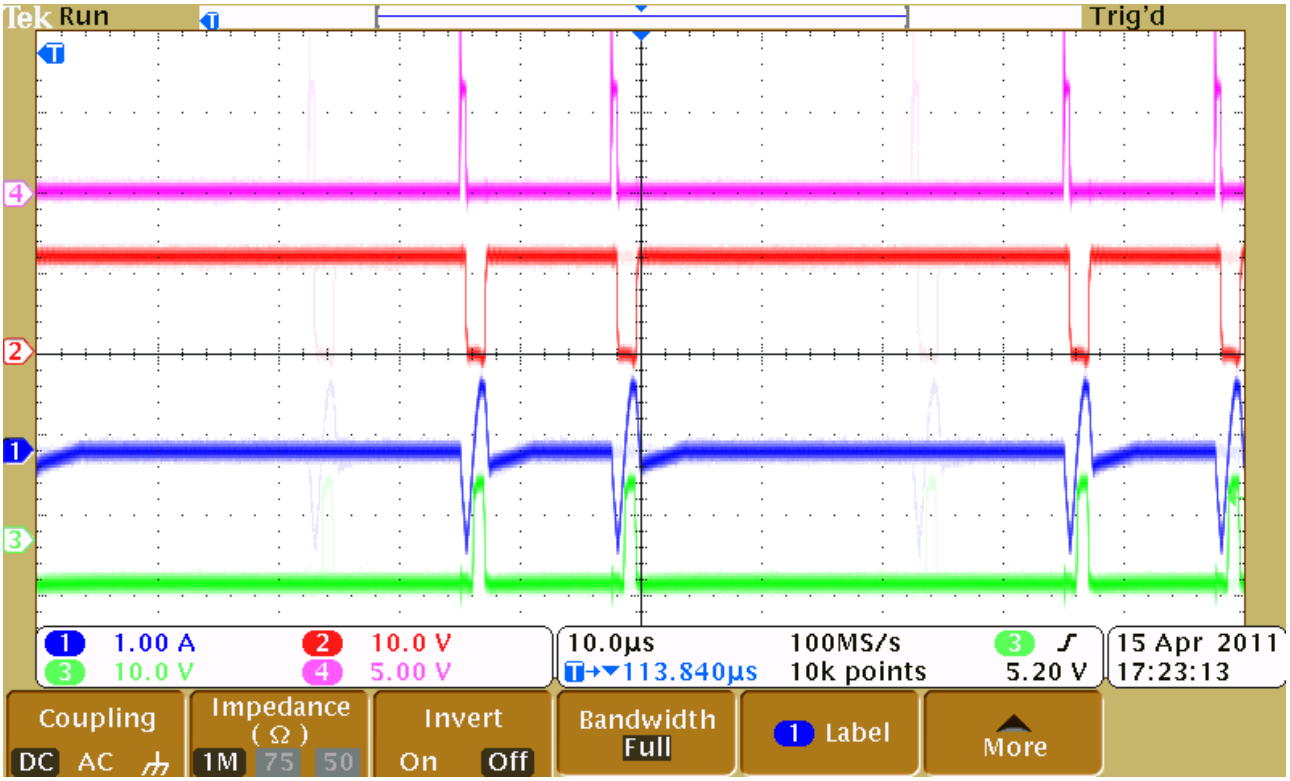


Figure 50 Inductor current, driver signals of S11, S22 and S33

Fig.7 shows the main switch driver signals S1 (channel 3) and S2 (channel 4), the current of the inductor Lr (channel 1) and the voltage across the link capacitor Cr (channel 2). The experimental results show that the voltage across Cr resonates and maintains at zero, which indicates that the zero voltage switching condition is created for the main switches. Therefore, the switching loss for the new quasi resonant DC link inverter is considerably reduced. The efficiency obtained with the soft-switching inverter is 2.5% higher than its hard switched counterpart.

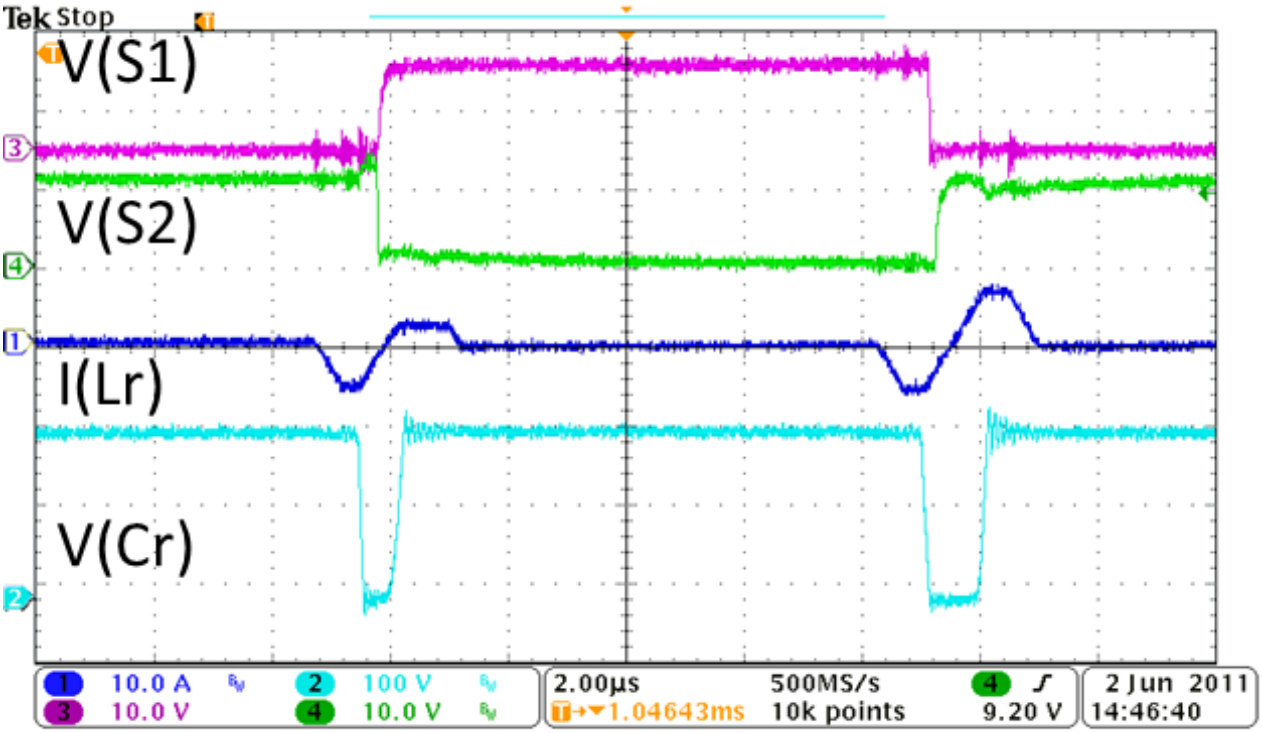


Figure 51 Main switches driver signals and Voltage across Cr

The experimental waveforms during the commutation period closely match the ones obtained by simulation. Since the PWM is easily employed, the output voltage is almost pure sinusoidal and has low THD as shown in Fig.8.

The measured peak efficiency is 95.8%, which does not include the auxiliary power. Fig.9 shows the efficiency curve comparison for the proposed quasi resonant DC link and hard switched inverter using Mosfets *21N65M5* and for the proposed quasi resonant DC link with IGBT IRGI4061DPbF (The efficiency data is measured by power analyzer PZ4000). As a result, the proposed quasi resonant DC link inverter has a significantly better performance than its hard-switching counterpart as the turn- on and

turn- off switching loss are eliminated. There is still some gap between the experimental efficiency and the simulated efficiency. More work will be done to improve the efficiency.

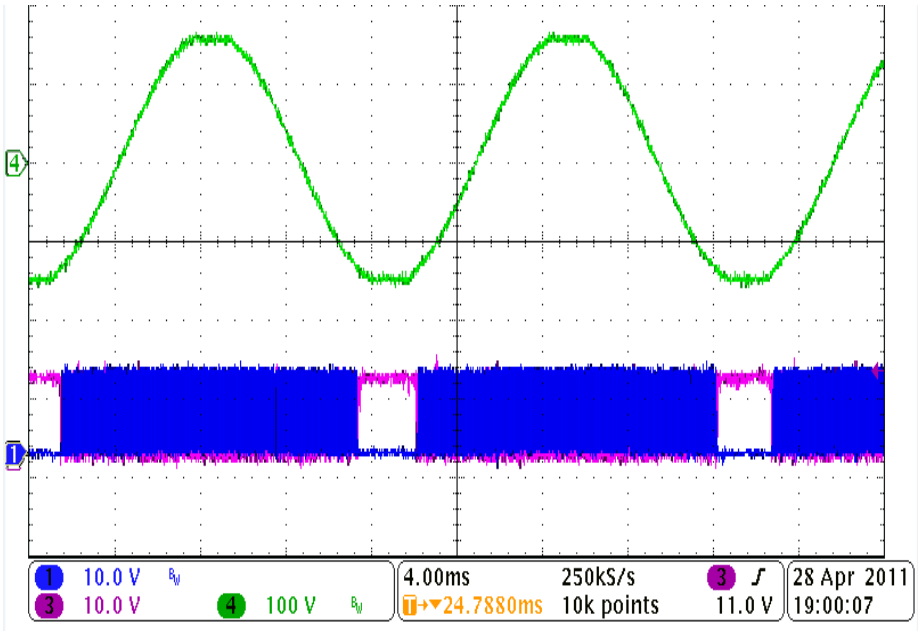


Figure 52 Output voltage waveform

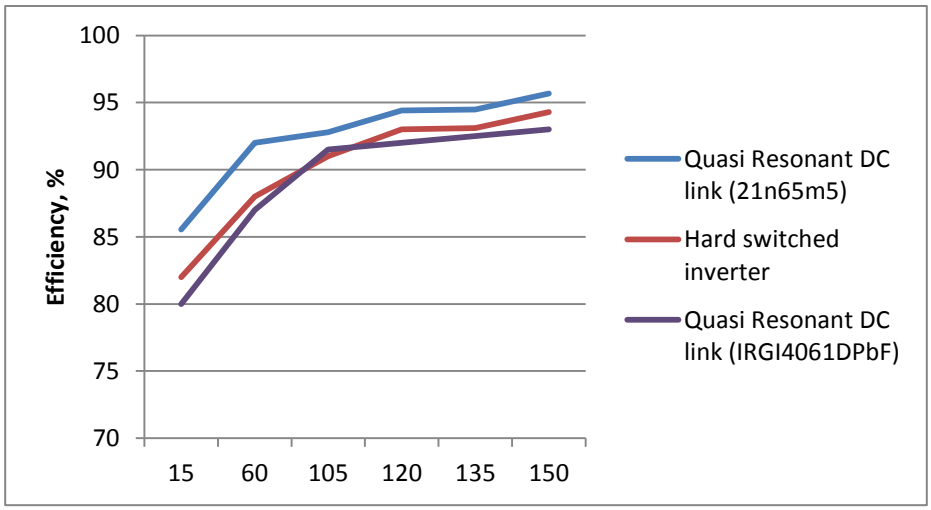


Figure 53 Efficiency curves

CHAPTER SIX: CONCLUSION

Since the introduction of the new inverter approach such as the micro inverter, there have been many major advances in technology in terms of semiconductor devices, power ICs, digital signal processors (DPS) and circuit topologies. A number of soft switching power conversion topologies have been discovered and implemented in today's inverter technologies. In most soft switching techniques resonant components and auxiliary devices are employed to create either zero voltage or zero current across the device prior to the switching instance. An overview on the existing soft-switching inverter topologies for single phase grid tied inverter technology was provided and evaluated in this work.

In this thesis, a new quasi resonant DC link is presented to realize zero-voltage switching and is applied to a single phase inverter, where the conventional PWM technique can be easily employed. Detailed operation is given to illustrate the operation principle of the proposed technique.

In order to boost efficiency and increase power density an analytical model for calculating the conduction and switching losses was developed using the datasheet parameters of the commercially available semiconductor switches. A rough calculation of efficiency was completed and comparison between soft and hard switching inverter was presented.

Simulated and experimental results are presented to prove the feasibility of the proposed quasi resonant DC link. The new quasi resonant DC-link inverter shows a significant decrease of main switch losses as a result of soft switching capabilities.

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