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Reliability Study Of Ingap/gaas Heterojunction Bipolar Transistor Mmic Technology By Characterization, Modeling And Simulation

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RELIABILITY STUDY OF INGAP/GAAS HETEROJUNCTION BIPOLAR TRANSISTOR MMIC TECHNOLOGY BY CHARACTERIZATION, MODELING AND SIMULATION

by

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ABSTRACT

Recent years have shown real advances of microwave monolithic integrated circuits (MMICs) for millimeter-wave frequency systems, such as wireless communication, advanced imaging, remote sensing and automotive radar systems, as MMICs can provide the size, weight and performance required for these systems.

Traditionally, GaAs pseudomorphic high electron mobility transistor (pHEMT) or InP based MMIC technology has dominated in millimeter-wave frequency applications because of their high f_T and f_{max} as well as their superior noise performance. But these technologies are very expensive. Thus, for low cost and high performance applications, InGaP/GaAs heterojunction bipolar transistors (HBTs) are quickly becoming the preferred technology to be used due to their inherently excellent characteristics. These features, together with the need for only one power supply to bias the device, make InGaP/GaAs HBTs very attractive for the design of high performance fully integrated MMICs.

With the smaller dimensions for improving speed and functionality of InGaP/GaAs HBTs, which dissipate large amount of power and result in heat flux accumulated in the device junction, technology reliability issues are the first concern for the commercialization. As the thermally triggered instabilities often seen in InGaP/GaAs HBTs, a carefully derived technique to define the stress conditions of accelerated life test has been employed in our study to acquire post-stress device characteristics for the projection of long-term device performance degradation pattern. To identify the possible origins of the post-stress device behaviors observed experimentally, a two

dimensional (2-D) TCAD numerical device simulation has been carried out. Using this approach, it is suggested that the acceptor-type trapping states located in the emitter bulk are responsible for the commonly seen post-stress base current instability over the moderate base-emitter voltage region.

HBT-based MMIC performance is very sensitive to the variation of core device characteristics and the reliability issues put the limit on its radio frequency (RF) behaviors. While many researchers have reported the observed stress-induced degradations of GaAs HBT characteristics, there has been little published data on the full understanding of stress impact on the GaAs HBT-based MMICs. If care is not taken to understand this issue, stress-induced degradation paths can lead to built-in circuit failure during regular operations. However, detection of this failure may be difficult due to the circuit complexity and lead to erroneous data or output conditions. Thus, a practical and analytical methodology has been developed to predict the stress impacts on HBT-based MMICs. It provides a quick way and guidance for the RF design engineer to evaluate the circuit performance with reliability considerations. Using the present existing EDA tools (Cadance SpectreRF and Agilent ADS) with the extracted pre- and post-stress transistor models, the electrothermal stress effects on InGaP/GaAs HBT-based RF building blocks including power amplifier (PA), low-noise amplifier (LNA) and oscillator have been systematically evaluated. This provides a potential way for the RF/microwave industry to save tens of millions of dollars annually in testing costs.

The world now stands at the threshold of the age of advanced GaAs HBT MMIC technology and researchers have been exploring here for years. The reliability of GaAs HBT technology is no longer the post-design evaluation, but the pre-design consideration. The successful and fruitful results of this dissertation provide methods and guidance for the RF designers to achieve more reliable RF circuits with advanced GaAs HBT technology in the future.

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I would like to express my sincere gratitude to my major advisor, Professor Juin J. Liou, for his constant warm and approachable support, as well as his patience and encouragement throughout my graduate studies. He gave me many critical directions and suggestions to this study while offering freedom to pursue and manage my own research. His technical and editorial advice was essential to the completion of this dissertation and has provided me innumerable insights of academic research in general. The knowledge and philosophy that he taught me will be the guidance of my future professional life.

I specially thank Professor Jiann S. Yuan because I have discussed a lot of research issues with him about the device stress testing, device model extraction and analysis, design and optimization of GaAs HBT-based RF building blocks. In particular, he gave me plenty of comments, training and advising and helps on the equipment setup for the experiments. We have collaborated in many research papers and I have learned a lot from him.

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LIST OF ACRONYMS/ABBREVIATIONS

2-D	Two-Dimensional
AC	Alternating Current
ADS	Advanced Design System
B-C	Base-Collector
B-E	Base-Emitter
BJT	Bipolar Junction Transistor
CE	Common-Emitter
DC	Direct Current
DUT	Device Under Test
EDA	Electronic Design Automation
FOM	Figure Of Merits
GSMs	Global Systems for Mobile communications
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
IIP3	Input Third-Order Intercept Point
I-V	Current versus Voltage
LNA	Low-Noise Amplifier
MMICs	Monolithic Microwave Integrated Circuits
MOCVD	Metal Organic Chemical Vapor Deposition
MTTF	Median Time To Failure
NF	Noise Figure
NF_{min}	Minimum Noise Figure

PA	Power Amplifier
PAE	Power-Added Efficiency
PCSs	Personal Communications Systems
pHEMT	pseudomorphic High Electron Mobility Transistor
PLL	Phase-Locked Loop
RF	Radio Frequency
RFICs	Radio Frequency Integrated Circuits
SCR	Space-Charge Region
SGP	SPICE Gummel-Poon
SNR	Signal-to-Noise Ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology Computer Aided Design
UMS	United Monolithic Semiconductors
US	United States
VCO	Voltage-Controlled Oscillator
WLANs	Wireless Local Area Networks

CHAPTER 1: INTRODUCTION

This chapter introduces the background of GaAs heterojunction bipolar transistors (HBTs) used in radio frequency (RF) and microwave applications and the motivation of this study with the outlines of this dissertation.

1.1 Background of GaAs Heterojunction Bipolar Transistors

During the early 1980s, the US government approached manufacturers to develop a new technology for its military and space programs -- GaAs HBT technology. The initial crop of wafers appeared promising, demonstrating high current gain. Figure 1.1 illustrates the lattice match of two different semiconductor materials forming a heterojunction interface of emitter and base in the HBT device structure. Despite the higher cost of material and processing, HBTs grown on GaAs substrates are being utilized as a superior solution for the demanding needs of communication standard in a variety of microwave systems. The block diagram of a modern RF transceiver is given in Figure 1.2. Typical characteristics of HBT devices are high efficiency, high linearity, low phase noise, thermal ruggedness and low cost. Usually, HBTs have a higher breakdown voltage which eliminates possible problems with high voltages, making them ideal for battery operated applications. Their bipolar structure allows them to operate from a single positive biasing supply.

However, various problems associated with parasitic effects must be solved to realize the full performance of HBTs. One of the most critical problems facing the successful utilization of GaAs HBTs is the long-term base current instability shown in Figure 1.3. Unfortunately, GaAs-based devices in general have a shorter lifetime than their silicon counterparts. This is due to the fact that GaAs is more susceptible to stress and has a poorer thermal conductivity. The former will lead to a higher number of defects being generated during stress, and the latter will result in higher lattice temperature during operation. As the device geometry is further scaled down to improve performance, GaAs HBTs are often operated under high current density. Thus, keys to successful use of this device in high-speed and high-frequency applications of high level of reliability are the ability of device engineers and circuit designers to understand the GaAs HBT degradation mechanisms and to predict the HBT-based MMICs long-term performance shifts.

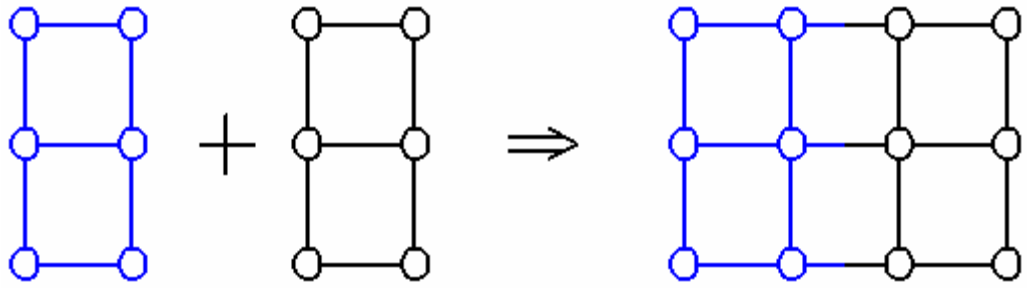


Figure 1.1 Lattice match of two different semiconductors forming a heterojunction interface.

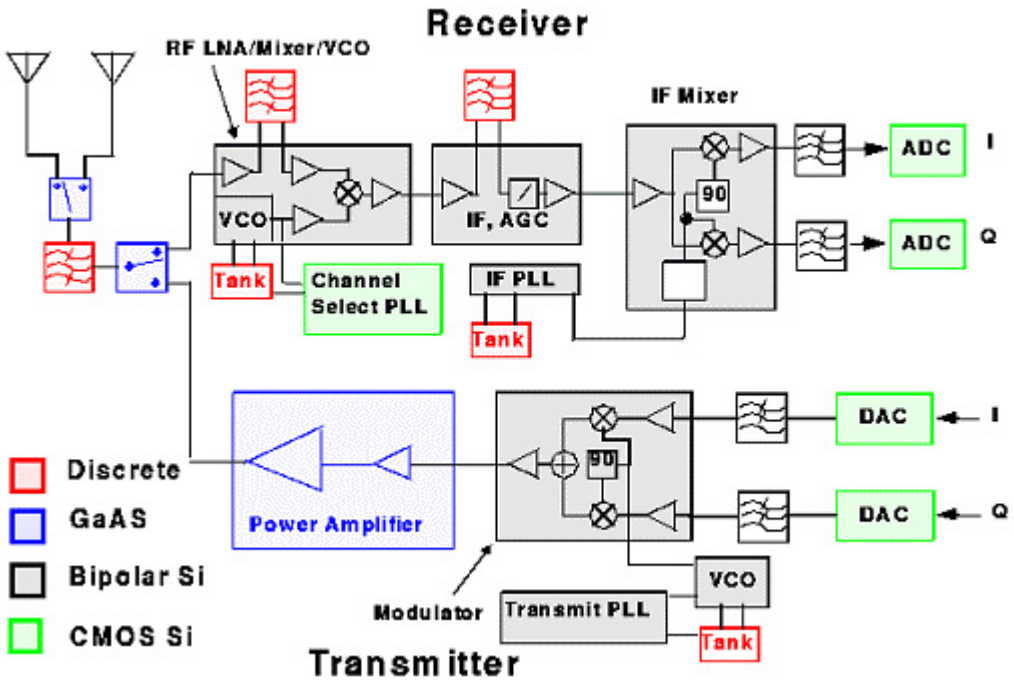


Figure 1.2 The block diagram of a modern RF transceiver.

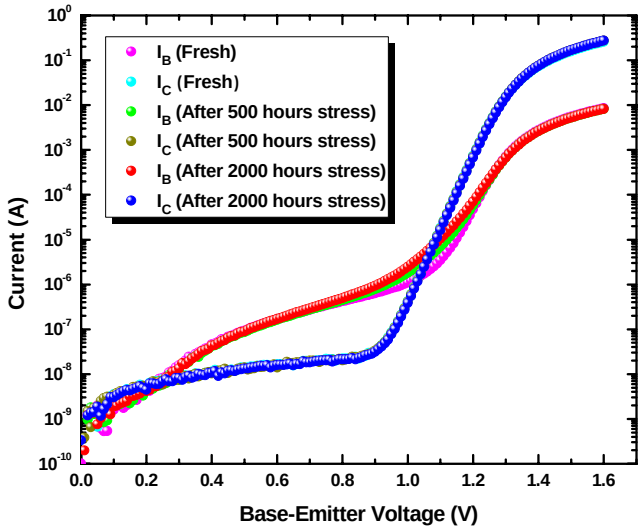


Figure 1.3 Long-term base current instability of GaAs HBTs.

1.2 Research Objectives

InGaP/GaAs HBTs are now gradually replacing the traditional AlGaAs/GaAs HBTs as the backbone in building blocks of microwave transceivers. The reliability of InGaP/GaAs HBTs is of great interest. Stress impacts on device-level degradation of advanced InGaP/GaAs HBTs have received widespread attentions [1-6], but little is understood of the circuit-level reliability of InGaP/GaAs HBT-based MMICs subject to the electrothermal stress.

Therefore, we first developed analytical device electrothermal stress testing methods and performed DC and small-signal RF pre- and post-stress device characterizations. Then, we evaluated the device performance degradations against the stress conditions and effectively investigated the possible origins of post-stress device behavior instabilities by applying 2-D TCAD device simulation methodologies. By developing empirical time-dependent models, we were able to effectively project the stress-induced device long-term performance degradation patterns by efficiently extrapolating the short-term accelerated stress testing data. To fully understand the circuit-level reliability performances of InGaP/GaAs HBT-based MMICs, we extracted and analyzed the fresh and aged SGP models from measurement data and developed a practical methodology to adopt the experimentally obtained pre- and post-stress device behaviors with EDA tools and analytical equations to efficiently evaluate the long-term stress-induced MMICs performance degradations, which is very useful for circuit designers to develop more reliable integrated circuits.

1.3 Outlines of Dissertation

A brief introduction to an advanced InGaP/GaAs HBT MMIC technology will be presented in Chapter 2. Then, the development of analytical device-level stress testing methods with pre- and post-stress DC and RF characterizations and empirical time-dependent models to project the stress-induced long-term device performance degradations are given in Chapter 3. 2-D TCAD numerical simulation methodologies are then used to figure out the possible origins of device behavior instabilities in Chapter 4. In Chapter 5 and Chapter 6, the SGP model extractions for fresh and aged DUTs and analysis are presented, and a practical methodology is used to evaluate the long-term stress impacts on 1.575 GHz InGaP HBT-based RF PA, 2.4 GHz InGaP HBT-based cascode LNA and 2.4 GHz InGaP HBT-based VCO. Finally, the conclusion and future work are drawn in Chapter 7.

CHAPTER 2: UMS INGAP/GAAS HBT TECHNOLOGY

2.1 AlGaAs/GaAs HBTs vs InGaP/GaAs HBTs

In 1980s, various heterojunction structures were laid out for the realization of improved bipolar transistor performance [7]. The most successful exploited of these structures to date has been the wide-bandgap emitter. That means bipolar device operation at high frequency relies on the use of an emitter material whose bandgap is wide compared with that used in the base layer. The valence band discontinuity at the B-E heterojunction blocks holes in the base from flowing into the emitter when the junction is forward biased. This allows the maintenance of high emitter injection efficiency at increased levels of base doping, thereby reducing the series resistance of the base. This series resistance has been one of the performance-limiting parameters in bipolar devices due to the extremely thin base widths. This further allows for a high level doping within the base layer giving a low parasitic base resistance and high switching speed and high cutoff frequency [8]. A typical energy bandgap diagram of an HBT is given in Figure 2.1.

In modern high-performance bipolar transistors, the highest frequency response to date has been achieved by vertical transistor structures [9-11]. This is because ultra thin base dimensions are more readily realized as the result of the growth thickness of an epitaxial layer, or the difference in depth of two diffusion profiles, than they are by a dimension defined in a photolithographic pattern. In addition, in the modern AlGaAs HBTs, vertical current flow is amenable to vertical bandgap engineering of the epitaxial layers during growth. As a result, the vertical HBT has

achieved high-frequency performance with f_T in excess of 100 GHz by grading the bandgap within the base region and at the emitter-base junction [12-14].

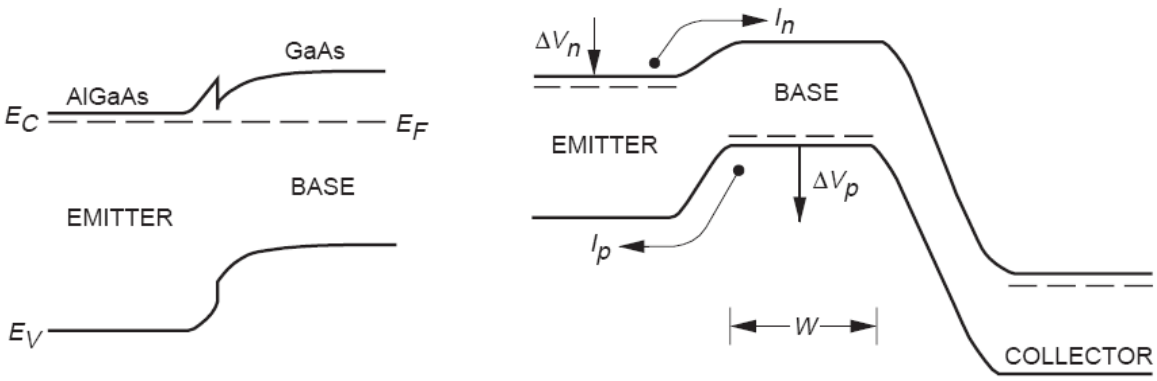


Figure 2.1 Energy bandgap diagram of a typical HBT.

InGaP/GaAs HBTs are now becoming a good alternative to AlGaAs/GaAs HBTs for manufacturing microwave and communication components. The advantages of InGaP/GaAs HBT-based MMIC technology over AlGaAs/GaAs have been demonstrated by several groups [15-18]. They include among other improved processing due to material etching selectivity and high injection efficiency due to the large valence band discontinuity. Several attempts have been reported in the past for reducing the B-C capacitance for improvement of the frequency performance and various technologies such as ion-implantation, polycrystal isolation and buried SiO_2 have been used for this purpose [19-20]. There is also evidence of improved reliability characteristics which combined with the other features makes InGaP HBT technology very suitable for manufacturing. For example, InGaP does not suffer from the oxygen related impurities which are easily incorporated during the epitaxy of AlGaAs.

For the last few years, the InGaP/GaAs HBT technology has reached a certain maturity. The large volume production and the utilization of statistical process control have greatly reduced the infant mortality population without having to impose traditional high reliability part specifications. However, reproducibility of a product does not gurarantee reliability in the intended application. Thus, it is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in those applications.

2.2 HB20S InGaP/GaAs HBT Technology

United Monolithic Semiconductors (UMS) has developed an industrial InGaP/GaAs HBT process (HB20S) especially dedicated to high performance MMICs applications [21]. The HB20S technology is an evolution of the X-band HB20P process, which is designed to address high power densities [22]. The device possesses a collector-emitter breakdown voltage BV_{CEO} > 32 V and a collector-base breakdown voltage BV_{CBO} > 65 V. This is achieved by increasing collector thickness as well as reducing collector doping density. Large collector thickness means high topology and leads to technological problems. Collector doping, on the other hand, is limited by background effects and epitaxial growth conditions. Therefore, bearing in mind the trade-off between these limitations and processing efforts, the device structure is completed by a 3100-nm thick n-GaAs collector with a uniform doping level of 5.5×10^{15} cm^{-3}, a 20-nm n-InGaP etch stop layer and a 100-μm thick n^{+}-GaAs subcollector (5×10^{18} cm^{-3}).

The epitaxial design consists of a non-alloyed emitter-contact by a 100-nm heavily doped n-InGaAs layer (1×10^{20} cm^{-3}) and a 150-nm heavily doped n-GaAs layer (5×10^{18} cm^{-3}). Moreover, in order to ensure thermal stability and to prevent gain collapse due to current concentration on single fingers, appropriate ballasting is mandatory. This is realized inside the emitter structure by incorporating a 600-nm lightly doped n-InGaP graded layer to provide integrated emitter ballast resistances to increase the DC power that can be dissipated in the device before encountering current collapse (one emitter finger tends to draw a significant portion of the total current, which can lead to failure through excessive local heating). This technique also avoids the use of bulky external base ballast resistances and decoupling capacitors, which would be otherwise mandatory for thermal stability.

Furthermore, the transistor incorporates a depleted emitter passivation ledge of a 20-nm n-GaAs layer and a 40-nm n-InGaP layer to enhance improved current gain and reliability. Then is a 140-nm uniformly heavily-doped p-GaAs base layer at 4×10^{19} cm^{-3} concentration. A self-aligned emitter-base fabrication process is used to consistently fabricate base contact away from emitter mesa edge. The extrinsic base surface is passivated with a thick silicon nitride layer as the dielectric of the MIM capacitors.

Besides this, a thick layer of gold is used to interconnect the emitter fingers and provide an efficient heat removal from the active area for the emitter air-bridge contacts, which plays the role of an efficient channel for heat sinking and reduces the thermal resistance by conducting the heat to the backside of the component as well as increasing the thermal homogeneity among the

fingers to reduce risks of thermal instabilities The heat is extracted from the top emitter contacts, transported by the high conductivity gold interconnect and dissipated through the substrate far away from the active intrinsic junctions of the transistors. These gold thermal drains reduce significantly the junction temperatures and contribute dramatically to the thermal capability of the devices which are fabricated on the low thermal conductivity GaAs substrate. These emitter ballast resistances and thermal drains have been optimized to warrant thermal stability and prevent thermal runaway (the so-called current crunch effect) and not to degrade significantly the microwave gains of the transistors.

This InGaP/GaAs HBT technology provides 16 emitter fingers, each with an area of $2\times70\ \mu m^2$. The device cross-sectional structure is shown in Figure 2.2. While the compositions of the different uniform-concentration layers in the HBT are given in Table 2.1. The frequency performance, on the other hand, has been compromised and reduced to a cut-off frequency f_T = 10 GHz, making the devices capable of operating between the L and S bands and perhaps even C band.

The process uses a conventional mesa approach and a non-self aligned base contact. All optical lithography steps are performed by stepper lithography. Selective dry etching steps are used extensively, resulting in excellent uniformity and reproducibility of the critical parameters and deep high dose proton isolation is also applied. Devices are fabricated on 4 inch InGaP/GaAs HBT epitaxial wafers grown by high quality metal organic chemical vapor deposition (MOCVD) technique.

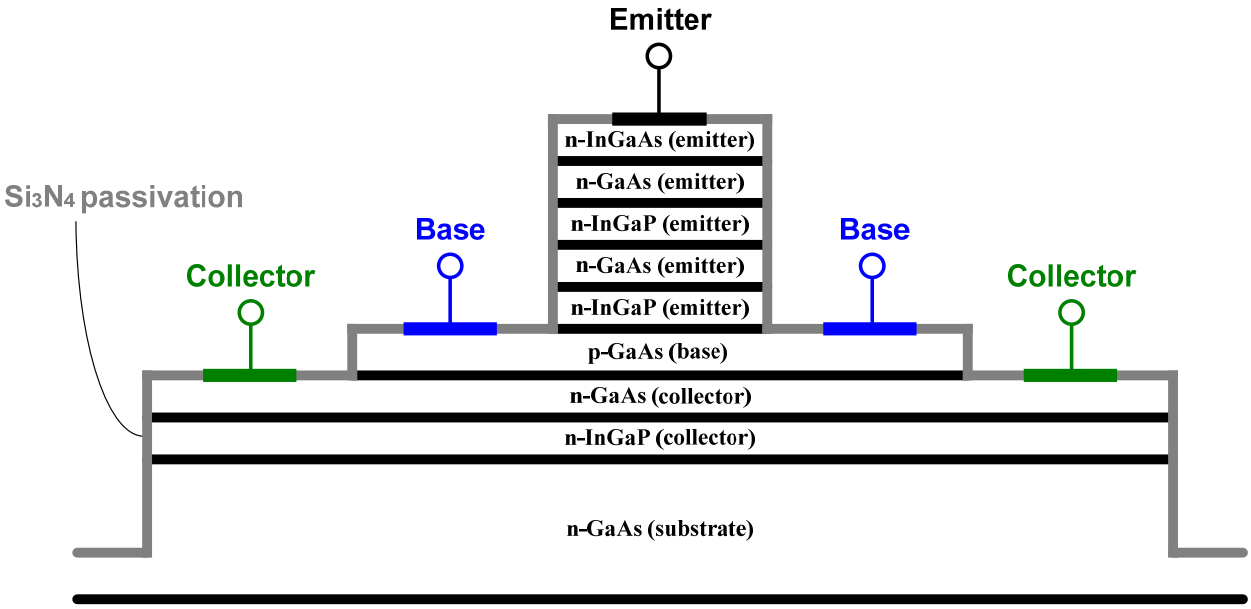


Figure 2.2 Schematic of the InGaP/GaAs HBT cross-sectional structure.

Table 2.1 Layer compositions of InGaP/GaAs HBT from the emitter to the substrate.

Material	Thickness (nm)	Doping (cm^{-3})
n-InGaAs	100	1×10^{20}
n-GaAs	150	5×10^{18}
n-InGaP	100	1×10^{18}
n-InGaP	400	9×10^{16}
n-InGaP	100	3×10^{17}
n-GaAs	20	3×10^{17}
n-InGaP	40	3×10^{17}
p-GaAs	140	4×10^{19}
n-GaAs	3100	5.5×10^{15}
n-GaAs	100	5×10^{18}
n-InGaP	20	5×10^{18}
n-GaAs	1×10^{5}	5×10^{18}

CHAPTER 3: STRESS-INDUCED INGAP/GAAS HBT PERFORMANCE DEGRADATIONS

3.1 Thermal Limitations of InGaP/GaAs HBTs

The performance of most commercial communication systems is limited by the capability and the reliability of its transmitter. A major concern for the transmitter is the reliability of the device whose intrinsic characteristics must be satisfactory. Therefore, the application of InGaP/GaAs HBTs requires a thorough assessment of its reliability. An examination of this technology from a reliability point of view is needed to identify critical design and fabrication issues that may limit its future use.

Thermal instability is a phenomenon peculiar to bipolar transistors. It has been extensively described for Si bipolar junction transistors (BJTs) [23]. The nature of this phenomenon is that of a tendency for hot spots to bloom because of a positive feedback between temperature and locally increased current, which causes self-destruction of the transistor. The positive feedback is: local high temperature causes lower base bandgap, which causes a lower turn-on voltage thus causing more current and more local heat. The most effective cure is to ensure a low thermal resistance which will weaken the positive feedback. Thermal instability can also be controlled by adding a little negative feedback in the form of emitter resistance. This is the ballast resistance, which determines the threshold level of dissipated power density which will trigger a device failure through thermal instability. The equation governing the bias condition at which the thermal instability occurs in Si BJTs is identical to the equation determined for GaAs HBTs [24].

Despite this similarity, the transistor behaviors upon entering the thermal instability region are drastically different. In Si BJTs where the current gain increases with temperature, the non-uniform current conduction among the fingers as a result of thermal instability leads to thermal runaway. These are believed to be inaccurate descriptions for GaAs HBTs. Instead of thermal runaway, the direct result of thermal instability in GaAs HBTs is the collapse of current gain, in which both the hot and cold fingers maintain stabilized current distribution at a given bias condition. Therefore, unlike in Si BJTs, thermal instability does not cause intrinsic second breakdown in GaAs HBTs.

For vertical oriented devices such as InGaP/GaAs HBTs, there is an electronic limit which can be taken as the power density per emitter area. Because the low base resistance in GaAs HBTs allows the use of large emitter areas with high emitter utility factor, high device currents can be achieved for a given emitter length. Again, because of low base resistance and the high electron saturation velocity in GaAs, current gain degradation due to Kirk effects does not occur until very high current density is reached [8]. Such high current density coupled with high collector voltages can bring GaAs HBTs close to the ultimate electronic performance limitations mentioned above. However, the high power density results in device self-heating so that the device performance is often limited by thermal effects rather than the electronic properties of the device. Thus, GaAs HBTs operating is known to be thermally limited devices. In other words, the temperature rise due to self-heating limits the device performance of GaAs HBTs before the electronic limitations are reached.

The thermal limitation can take many forms [8]. In its most common form, the temperature rises in the device due to dissipated power and the substrate temperature can cause electrical failures due to destructive or non-destructive changes in device properties. This sets the upper limit for the temperature rise from device reliability point of view. Among non-destructive thermal limitations we can consider temperature effects on the device electronic performance. For example, when the junction temperature increases above the intrinsic temperature, the majority and minority carrier concentration become equal and therefore transistor action ceases. Again, at high temperatures the HBT current gain approaches unity rendering the device unsuitable for amplification applications. These thermal limitations normally occur when the device temperature is uniformly increased. e.g., by external sources. If the device temperature rise is due to self-heating of a large device, non-uniform temperature distribution can occur due to positive temperature coefficient in the I-V characteristics of the B-E diode [8]. This is most common among multi-emitter finger devices operating under constant base current or constant B-E voltage conditions and depending on device designs, it can be the most prominent temperature limitation of bipolar transistors.

Thermal reliability of InGaP/GaAs HBT has been studied extensively and shown a steady improvement over the last decades [25]. The short-term instability due to the thermal runaway is addressed by thermal and electrical management and poses no difficulty in today's InGaP/GaAs HBT-based MMICs design. However, HBT long-term instability due to various failure mechanisms is still under investigation. Most of the failure mechanisms are attributed to the dopant diffusion, crystalline quality, excessive leakage current, and contacts as well as

passivation layer failure [25]. State of the art HBTs have achieved median time to failure (MTTF) in the order of 10^9 hours at junction temperature of 120 °C. The improvement in reliability characteristics has been achieved by various techniques including but not limited to:

1) Device growing at a lower temperature to suppress positively charged interstitial dopants and avoid redistribution of charges under stress conditions [26].
2) Improved passivation techniques in addition to the use of ledge to suppress non-ideal base current [27].
3) Using non-alloyed contacts and also the InGaAs emitter cap to improve ohmic contact stability [28].
4) Indium co-doping of the base [29].
5) Employment of carbon-doped InGaP emitter in conjunction with carbon-doped GaAs base to suppress performance sensitivity to dopant redistribution [30].

However, beyond these device-level reliability improvement techniques, there are no studies performed to evaluate the long-term electrothermal stress-induced device characteristics degradations. To investigate how time-dependent electrothermal stress affects device performance, a series of carefully derived methodology was explained in next section.

3.2 Development of Stress Testing Methods

Device reliability involves probability statistics time and a definition of failure. Given a failure criterion, the most direct way to determine reliability is to submit a large number of samples to actual use conditions and monitor their performance against the failure criteria over time. This is

a well known and proven assessment called “lifetime test”. Since most applications require device lifetime of many years, this approach is not very practical because a major drawback is the significant long time taken to complete the tests and obtain the desired data.

As regard to the thermally triggered instabilities often seen in HBTs and degradations due to eletrothermal stress, a useful technique to define the stress conditions has been employed in our study to acquire reliability data for the projection of its degradation pattern in a reasonable amount of time. The technique is based on the observation that most failure mechanisms for the HBTs are thermally activated. The combination of the high current density during the operation and the relatively low thermal conductivity of the GaAs substrate elevate the device junction temperature severely, which may lead to the failure of the device [31]. By exposing the sample devices to high junction temperatures, it is possible to reduce the time to failure of the DUTs, thereby enabling data to be obtained in a shorter time than would otherwise be required.

The graph presented in Figure 3.1 depicts the thermal distribution on each emitter finger of the DUT simulated to estimate the thermal resistance as a function of base plate temperature for the elementary cell and the whole packaging environment. For symmetry reasons, only half of the structure has been simulated. It is shown that the center fingers are the hottest, and depending on the position of the finger as well as the finger geometry, the thermal gradient can reach 10 °C (edge effect). To investigate the correlation between the stress conditions and self-heating effect, a carefully derived methodology is developed and stated below.

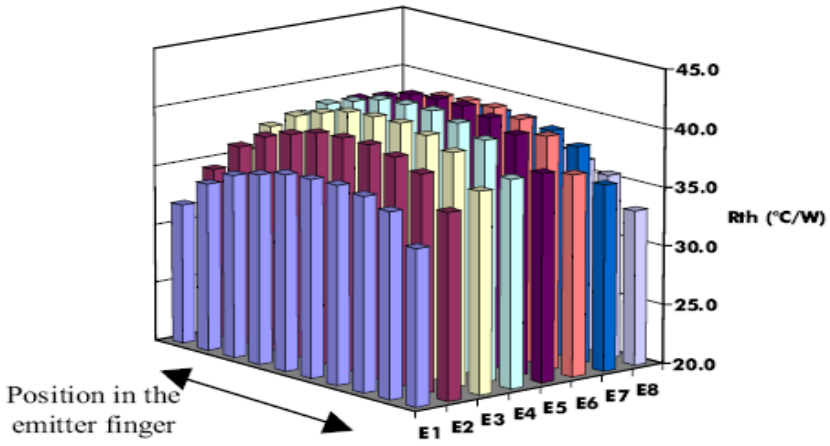


Figure 3.1 Thermal distribution in HBT having 8 emitter fingers.

On the basis of these results, the evolution of R_{th} has been reached about 46.07 °C/W. A simple expression to correlate the junction temperature T_J and R_{th} is given by

$$T_J = T_A + R_{th} \times P_{diss} \tag{1}$$

where T_A is the ambient temperature, and P_{diss} is the dissipated power given as

$$P_{diss} = I_C V_{CE} + I_B V_{BE} = I_C V_{CE} + \frac{I_C}{\beta} V_{BE} \tag{2}$$

As $\frac{I_C}{\beta} V_{BE}$ is much less than $I_C V_{CE}$, we can neglect this term and arrive at

$$P_{diss} \approx I_C V_{CE} \tag{3}$$

Combining these equations, we can determine the current and voltage levels required for a particular junction temperature stress. For example, for a desirable $T_J = 200°C$ with $T_A = 30°C$, we can calculate from Equation 2 and find $P_{diss} = I_C V_{CE} = 3.69W$ considering a collector-emitter voltage $V_{CE} = 15V$ and collector current $I_C = 246mA$. This is the way how we produce stress conditions in our study. Figure 3.2 shows the junction temperature as a function of power

dissipation model which demonstrates the utility and accuracy of the correlation between T_J and P_{diss}.

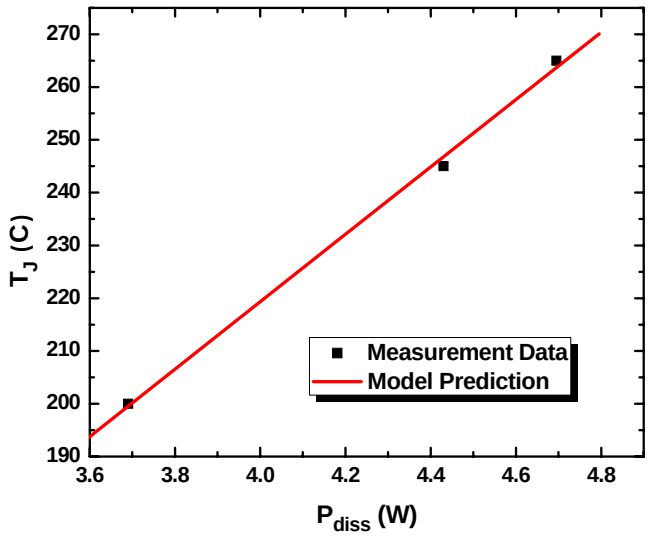


Figure 3.2 Measured and simulated junction temperature as a function of power dissipation.

3.3 Electrothermal Stress Testing Results

To avoid potential recombination enhanced defect diffusion induced device failure, accelerated junction temperatures were kept below 270 °C in this investigation. Therefore, V_{CE} and I_C were selected to bias the devices and set the enhanced junction temperature at 200 °C, 245 °C and 265 °C, respectively, given in Figure 3.3. Once the devices were stressed, all characteristics were obtained under normal bias conditions.

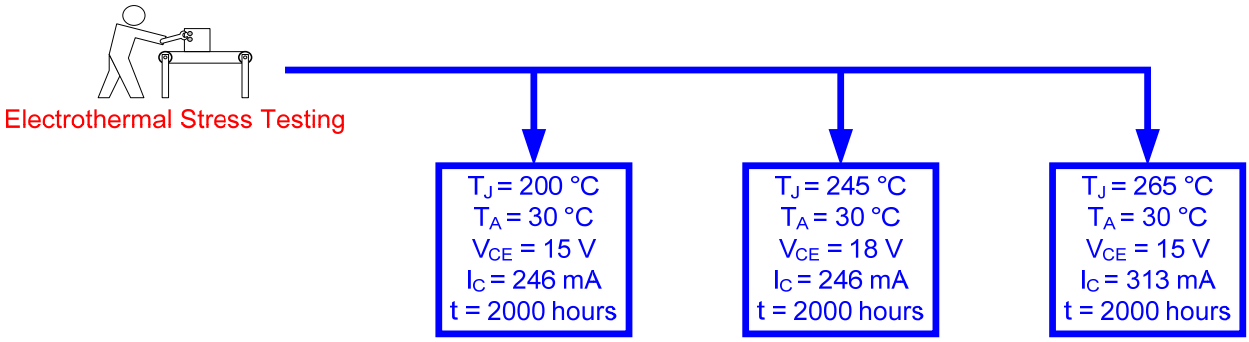


Figure 3.3 Electrothermal stress testing conditions.

All experiments were performed on the DUT modules specially designed in the frame of the evaluation for degradation mechanisms shown in Figure 3.4 and 3.5. A discrete power bar is mounted in the hybrid circuit sharing a single 30 μm thick gold thermal drain connected to the emitter fingers at the upper side and joining the backside metal through via holes. In front of each elementary cell, a pre-matching circuit has also been included.

DC performances were characterized, analyzed and evaluated before and after stress. HP 4156B Precision Semiconductor Parameter Analyzer and HP 16442A Test Fixture were used for the stress testing as well as the I-V characterizations shown in Figure 3.6.

Figure 3.7 displays the normalized percentage changes of base current and the DC current gain as a function of cumulative stress time at three different eletrothermal stress conditions. The normalized degradations of collector current along with the cumulative stress time are shown in Table 3.1.

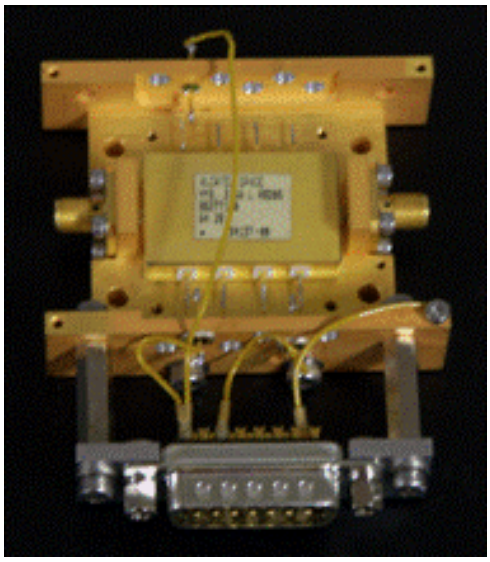


Figure 3.4 Specially designed DUT module.

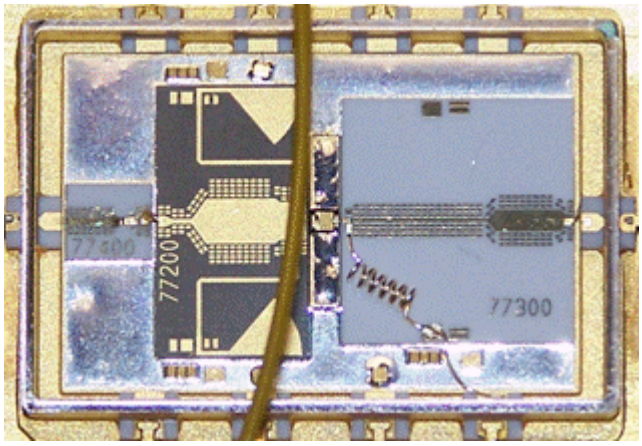


Figure 3.5 Enlarged discrete power bar.

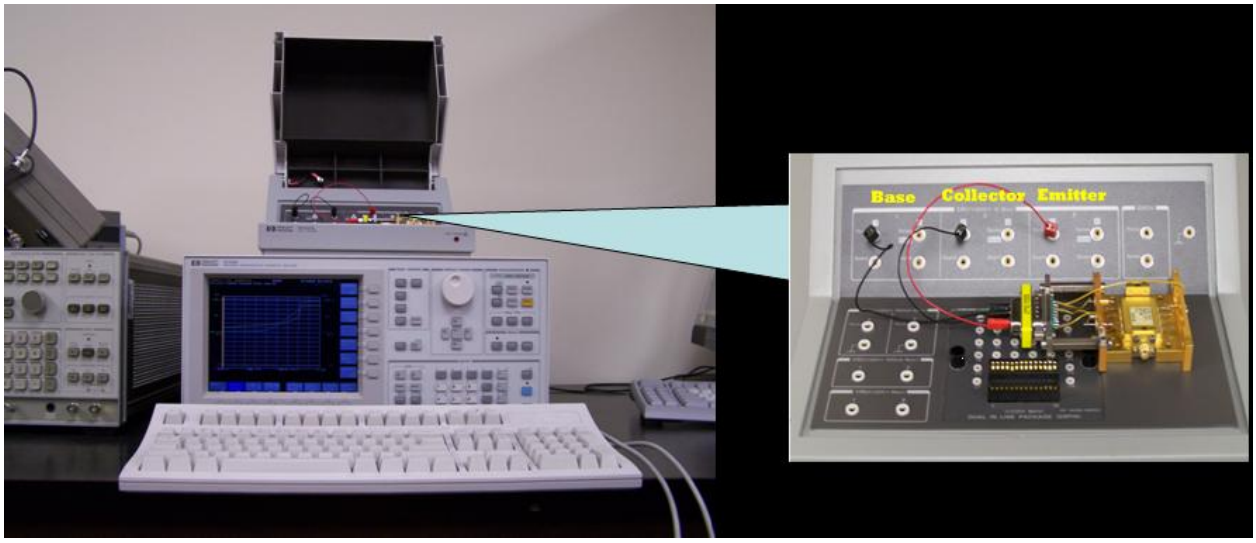
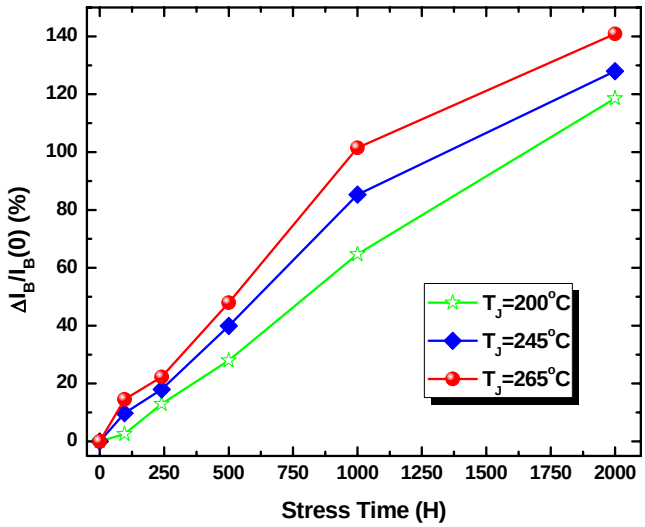
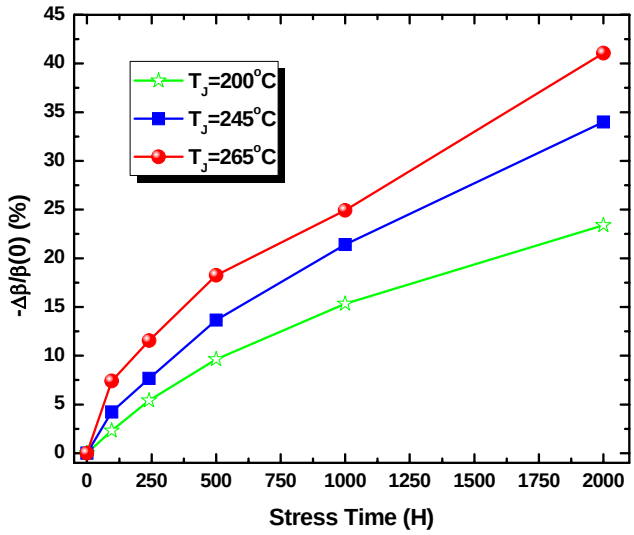


Figure 3.6 Equipment setup for stress testing and DC characterizations.



(a)



(b)

Figure 3.7 (a) Base current degradations vs. stress time; (b) DC current gain degradations vs. stress time.

Table 3.1 Normalized collector current shifts vs. stress time.

Stress Time (Hour)	**$\Delta I_C/I_C(0)$ (%)**		
	T_J=200 °C	**T_J=245 °C**	**T_J=265 °C**
0	0.00	0.00	0.00
96	-3.28	-2.70	-1.19
240	-2.14	-0.50	-1.13
500	2.67	-0.74	-0.11
1000	-2.84	-2.13	-0.87
2000	1.16	-2.94	0.20

Clearly, the post-stress base current degradations were increased with the elevated junction temperatures and accumulated stress time. While the DC current gain also shows the same

tendency with stress time and junction temperatures as base current does, and this is verified by the almost unchanged post-stress collector current. After 2000-hour stress, the base current increased 140.88% and DC current gain decreased 41.07% at the junction temperature of 265 °C. All curves shifted upward after stress.

Now let's look at the stress-induced DUT's RF characteristics. The stress test condition is given in Figure 3.8. It comprises an accelerated stress test at a very high junction temperature of 265 °C to find out the electrothermal stress impact on DUT's RF performances. Since the two-port S-parameters are relatively easy to obtain at high frequencies by measuring the voltage traveling waves using a vector network analyzer, we can measure the pre- and post-stress S-parameters and then employ those data to further determine the DUT's RF gain, loss and reflection coefficient etc before and after stress. The two-port network diagram with the definition of S-parameters is shown in Figure 3.9. The DUT should be properly biased at the desired Q-point and small-signal conditions must be maintained throughout RF characterizations performed by Agilent N5230A Network Analyzer with HP 4156B Precision Semiconductor Parameter Analyzer and HP 16442A Test Fixture for the DC biasing shown in Figure 3.10.

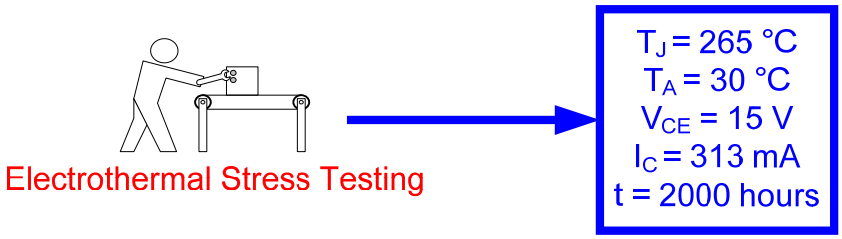
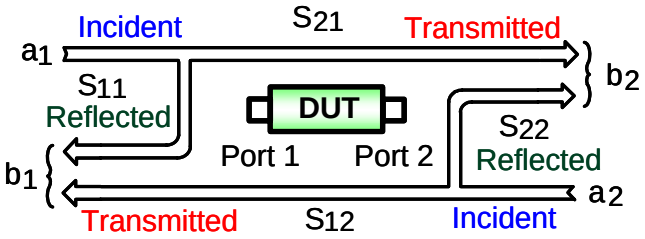


Figure 3.8 Stress test condition of post-stress RF characterizations.



$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

$$S_{11} = \frac{\text{Reflected}}{\text{Incident}} = \frac{b_1}{a_1}\Big|_{a_2=0} \qquad S_{21} = \frac{\text{Transmitted}}{\text{Incident}} = \frac{b_2}{a_1}\Big|_{a_2=0}$$

$$S_{22} = \frac{\text{Reflected}}{\text{Incident}} = \frac{b_2}{a_2}\Big|_{a_1=0} \qquad S_{12} = \frac{\text{Transmitted}}{\text{Incident}} = \frac{b_1}{a_2}\Big|_{a_1=0}$$

Figure 3.9 The diagram and definitions of two port S-parameters.

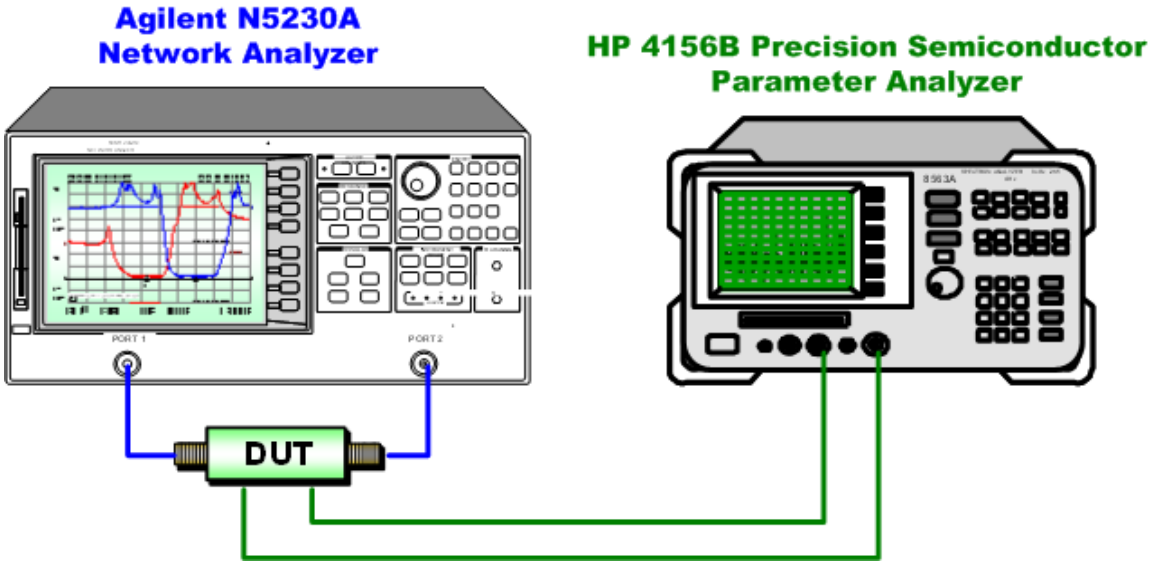


Figure 3.10 The schematic of S-parameters measurement setup.

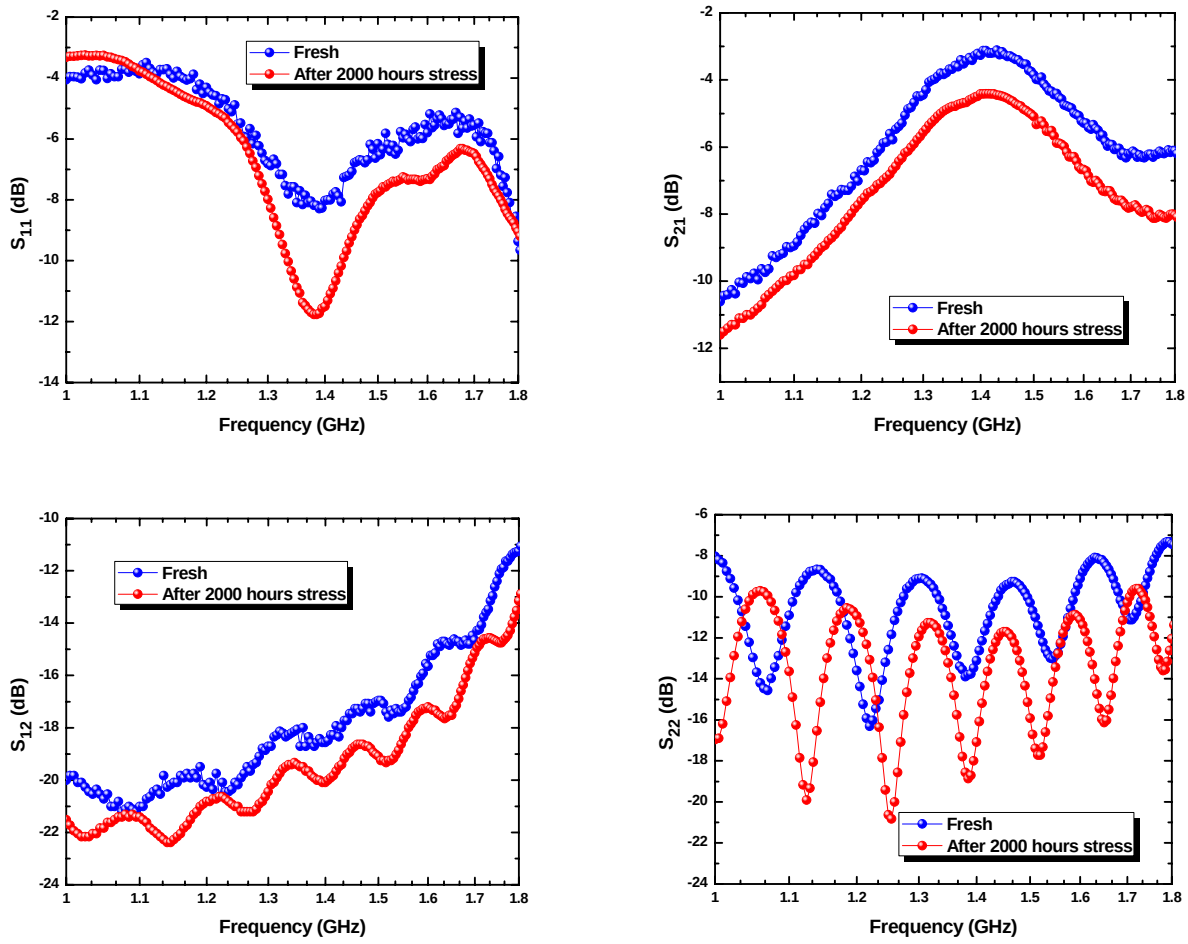


Figure 3.11 Measured pre- and post-stress S-parameters.

The pre- and post-stress S-parameters shown in Figure 3.11 were characterized from 1 GHz to 1.8 GHz of the L-band frequency range at a collector-emitter voltage V_{CE} = 14 V and a base-emitter voltage V_{BE} = 1.3 V, then the measurement data were analyzed and evaluated before and after stress test. All measurements were done at room temperature. The magnitude of S_{21} at 1.575 GHz decreased from -3.29 dB to -4.55 dB after 2000-hour stress, post-stress S_{11} at 1.575 GHz

decreased from -7.07 dB to -9.22 dB, and S_{22} at 1.575 GHz changed from -9.53 dB to -11.71 dB after stress and S_{12} at 1.575 GHz changed from -17.46 dB to -18.79 dB.

3.4 Projection of Post-stress Device Degradation Patterns

The impact of high junction temperatures and different cumulative stress time can be characterized as the degradation of major device behaviors. The combination effect has been indicated by experiment results.

On the other hand, the stress duration we performed was relatively short (up to 2000 hours) compared to industrial standard of MTTF. In order to project the long-term performance shifts of the DUTs, we developed an empirical model based on power-law using the short-term measured data in the following paragraphs.

Stress tests are normally carried out within a relatively short time frame to observe the change of device behaviors (i.e., DC current gain shifts after stress), to characterize the DUT's long-term degradation patterns, the time-dependent degradation models are then applied to project the post-stress long-term performance shifts. Several time-dependent laws have been reported in the literature and the most widely used is the power law proposed in the 1980s [32]. However, so far there is no time-dependent degradation law available to predict the post-stress performance of GaAs HBTs. Hence we derived an empirical model for the projection of InGaP/GaAs HBT's post-stress performance shift based on the conventional power law.

In general, the DC current gain shift of the HBT can be described by the power-law relationship:

$$\frac{\Delta\beta(t)}{\beta(0)} = A \times t^{n} \tag{4}$$

where A and n are the fitting parameters which can be extracted by fitting Equation 4 to the short-term $\frac{\Delta\beta(t)}{\beta(0)} - t$ measured data. Consider a sample DUT and its short-term data given in Figure 3.12, A and n can be extracted as A = 0.00002 and n = 0.90662 for the best curve fitting result.

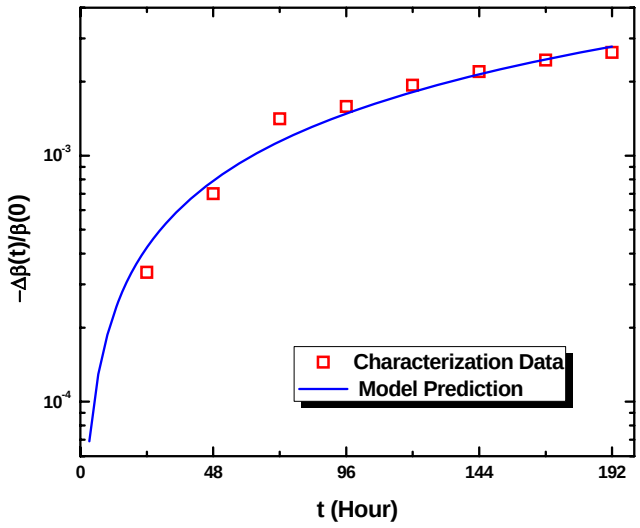


Figure 3.12 Time-dependent empirical model extraction based on power law relationship.

Thus, for this sample, the long-term time-dependent degradation model can be expressed as

$$\frac{\Delta\beta(t)}{\beta(0)} = 0.00002 \times t^{0.90662} \tag{5}$$

This allows one to project the DC current gain shift at any time point. Figure 3.13 shows the projected normalized DC current gain for this DUT sample up to 20 years. For example, after 4 years, the DC current gain shift is projected to be decreased -32% from its initial value after stress.

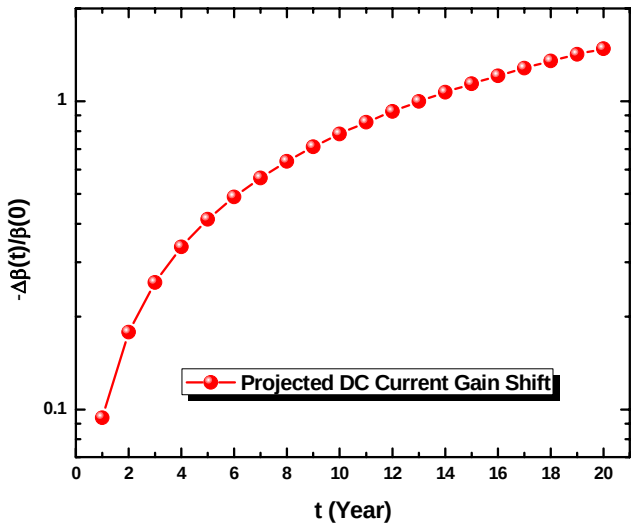


Figure 3.13 Projection of normalized long-term DC current gain degradation.

Based on this approach, we can obtain the empirical time-dependent degradation models to predict other long-term device characteristics shifts as well.

CHAPTER 4: RELIABILITY ANALYSIS OF INGAP/GAAS HBT TECHNOLOGY BY 2-D TCAD NUMERICAL SIMULATION METHODOLOGIES

4.1 Introduction

Although the base current in InGaP/GaAs HBTs with ledge is relatively stable compared to that in GaAs HBTs without ledge, the base current increase in these passivated HBTs is still noticeable. Since the increase of base current has adverse effects on circuit performance, it becomes one of the key concerns in HBT circuit reliability [33]. To fully realize the potential of HBTs, an in-depth understanding of the base current degradation mechanisms is essential. In this chapter, we will investigate the possible mechanisms contributing to this experimentally observed HBT pre- and post-stress behavior instabilities due to the electrothermal stress effect based on TCAD device simulations. First, the HBT device structure and physical parameters used in the simulations are presented. This is followed by the simulations of pre-stress HBT DC performance. Finally, device simulations with defects added in the HBTs to emulate the post-stress conditions are carried out.

4.2 InGaP/GaAs HBT Device Structure in TCAD

The first stage was to construct the InGaP/GaAs HBT device structure geometry, material layers, doping profiles and electrodes.

From the layer compositions of InGaP/GaAs HBT in Chapter 2, we found that we couldn't define the device structure only by some very simple syntax and we have to generate thousands of pairs of coordinates to construct this complex cross section profile. Then the mesh was generated automatically by specifying the basic mesh constraints and refining it along the x- and y-directions in the critical areas of device. After the mesh was created, a command file was saved. Figure 4.1 shows the entire device structure created, while Figure 4.2 shows the enlarged schematic for the layer structure in the emitter region, which consists of 8 layers and three different materials. Figure 4.3 shows the doping profile and the net doping density in the device.

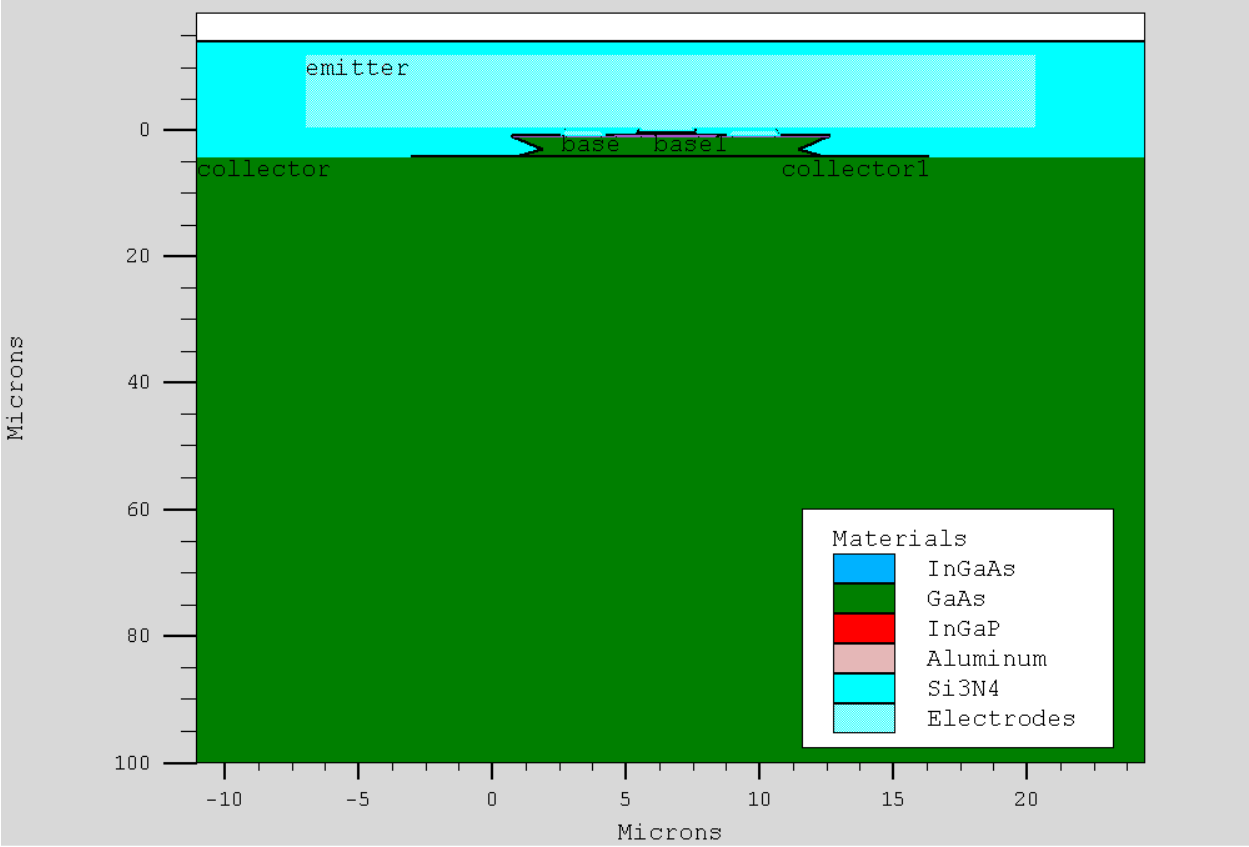


Figure 4.1 HBT device structure constructed in device simulator.

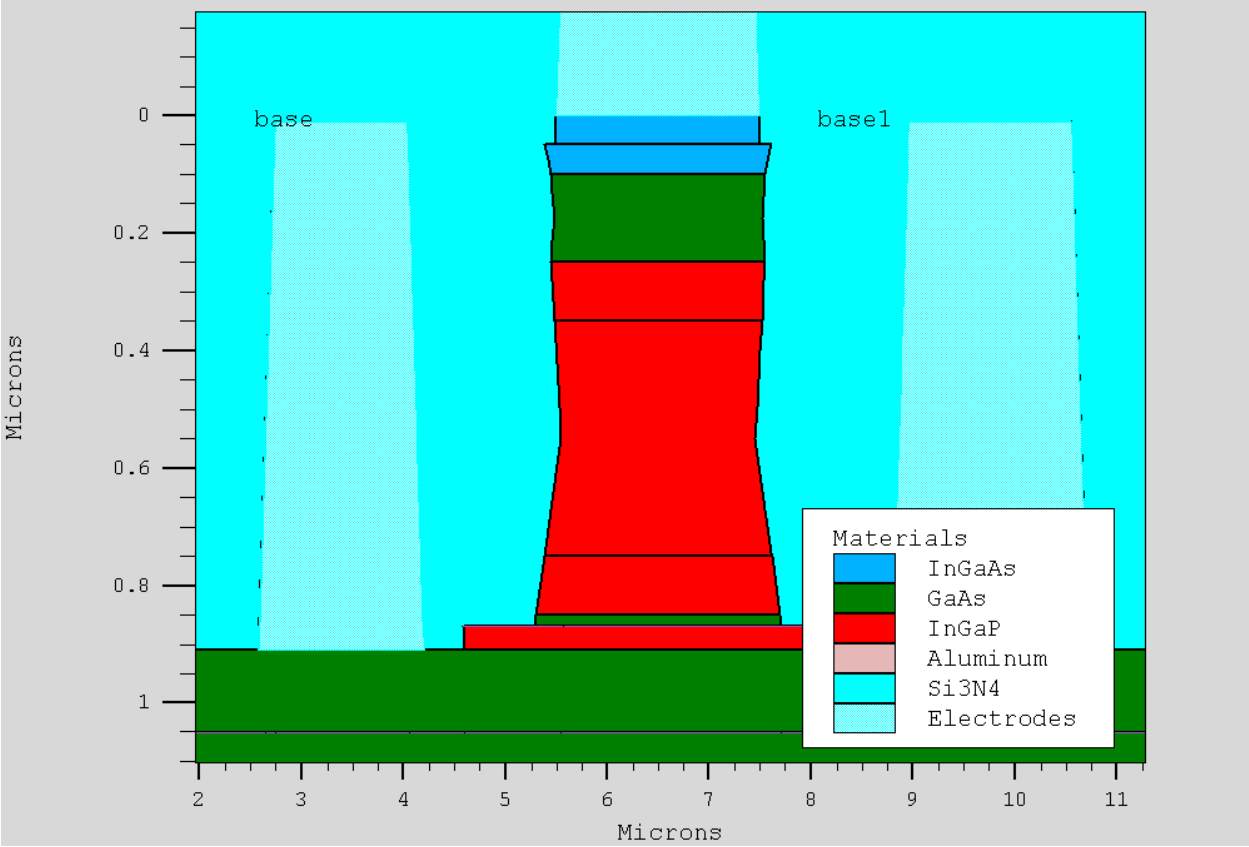


Figure 4.2 Enlarged layer structure for the emitter region.

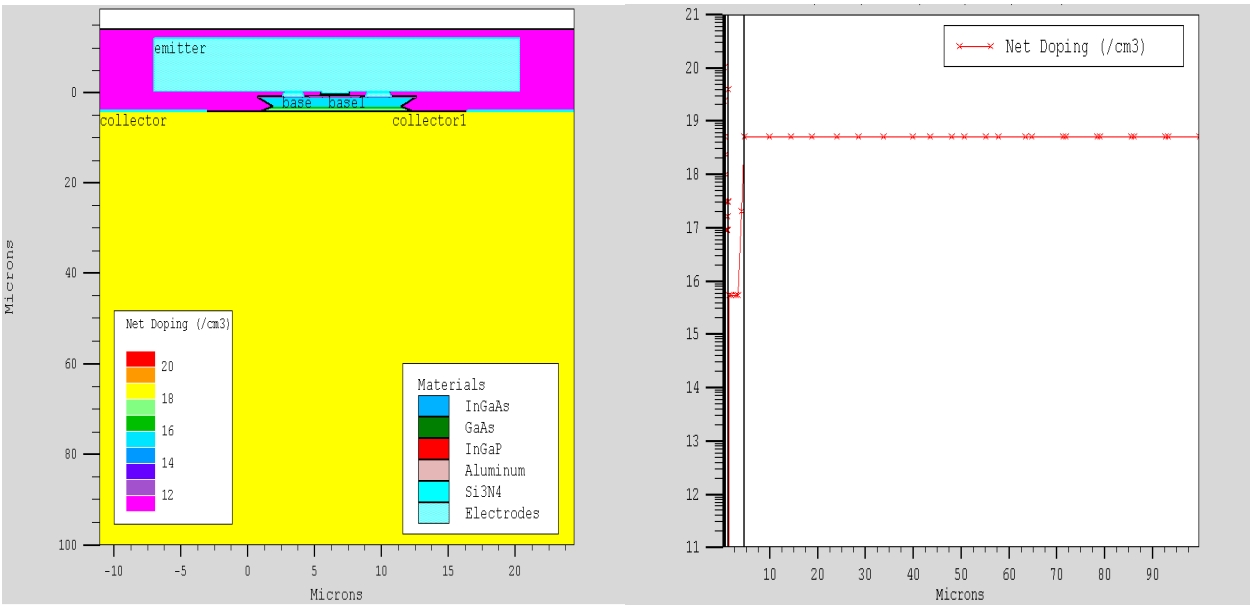


Figure 4.3 Doping profile and net doping density of DUT.

4.3 InGaP/GaAs HBT Material Parameters and Device Models

It is known that the material parameters are particularly important for accurate device simulations. For compound materials with variable composition fractions, their material parameters can be calculated from parameter models which are functions of x and y compositions. Table 4.1 shows the material parameters in each layer of the device.

The mainly material we used for the project is the $In_{(1-x)}Ga_{(x)}As_{(y)}P_{(1-y)}$ system, and its material parameter (energy bandgaps, conduction band offsets, effective electron and hole masses, and dielectric permittivities) models are given below:

$$E_g\left(InGaAsP\right)=1.35+x.comp\times\left[0.642+\left(0.758\times x.comp\right)\right]+\left(0.101\times y.comp-1.101\right)\times y.comp-\left(0.28\times x.comp-0.109\times y.comp+0.159\right)\times x.comp\times y.comp \quad (6)$$

$$\Delta E_c=0.268\times y.comp+0.003\times\left(y.comp\right)^2 \quad (7)$$

$$m_e^*=0.08-\left(0.116\times y.comp\right)+\left(0.026\times x.comp\right)-0.059\times\left(x.comp\times y.comp\right)+\left(0.064-0.02\times y.comp\right)\times\left(x.comp\right)^2+\left(0.06+0.032\times x.comp\right)\times\left(y.comp\right)^2 \quad (8)$$

$$m_h^*=\left(m_{lh}^{1.5}+m_{hh}^{1.5}\right)^{\frac{2}{3}}$$
$$m_{lh}=0.120-\left(0.116\times y.comp\right)+0.03\times\left(x.comp\right)^2 \quad (9)$$
$$m_{hh}=0.46$$

$$\varepsilon_{InGaAsP}=\left[14.6\times\left(1-x.comp\right)\times y.comp\right]+12.5\times\left(1-x.comp\right)\times\left(1-y.comp\right)+13.18\times x.comp\times y.comp+11.11\times x.comp\times\left(1-y.comp\right) \quad (10)$$

Table 4.1 Material physical parameters of InGaP/GaAs HBT.

Region No.	1	2	3	4	5	6	7	8	9	10	11	12	13
Material	InGaAs	InGaAs	GaAs	InGaP	InGaP	InGaP	GaAs	InGaP	GaAs	GaAs	GaAs	InGaP	GaAs
Epsilon	13.9	13.9	13.2	11.8	11.8	11.8	13.2	11.8	13.2	13.2	13.2	11.8	13.2
Eg (eV)	0.766	0.766	1.42	1.85	1.85	1.85	1.42	1.85	1.42	1.42	1.42	1.85	1.42
Chi (eV)	4.13	4.13	4.07	4.4	4.4	4.4	4.07	4.4	4.07	4.07	4.07	4.4	4.07
Nc (per cc)	1.61E+17	1.61E+17	4.35E+17	8.92E+17	8.92E+17	8.92E+17	4.35E+17	8.92E+17	4.35E+17	4.35E+17	4.35E+17	8.92E+17	4.35E+17
Nv (per cc)	8.12E+18	8.12E+18	1.29E+19	8.87E+18	8.87E+18	8.87E+18	1.29E+19	8.87E+18	1.29E+19	1.29E+19	1.29E+19	8.87E+18	1.29E+19
ni (per cc)	4.21E+11	4.21E+11	2.67E+06	813	813	813	2.67E+06	813	2.67E+06	2.67E+06	2.67E+06	813	2.67E+06
Gc	2	2	2	2	2	2	2	2	2	2	2	2	2
Gv	4	4	4	4	4	4	4	4	4	4	4	4	4
Ed (eV)	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044	0.044
Ea (eV)	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045	0.045
taun0	5.00E-10	5.00E-10	1.00E-09	4.00E-17	4.00E-17	4.00E-17	1.00E-09	4.00E-17	1.00E-09	1.00E-09	1.00E-09	4.00E-17	1.00E-09
taup0	1.00E-09	1.00E-09	2.00E-08	4.00E-17	4.00E-17	4.00E-17	2.00E-08	4.00E-17	2.00E-08	2.00E-08	2.00E-08	4.00E-17	2.00E-08
nsrhn	-1.00E+03	-1.00E+03	5.00E+16	-1.00E+03	-1.00E+03	-1.00E+03	5.00E+16	-1.00E+03	5.00E+16	5.00E+16	5.00E+16	-1.00E+03	5.00E+16
nsrhp	-1.00E+03	-1.00E+03	5.00E+16	-1.00E+03	-1.00E+03	-1.00E+03	5.00E+16	-1.00E+03	5.00E+16	5.00E+16	5.00E+16	-1.00E+03	5.00E+16
vsatn (cm/s)	2.50E+07	2.50E+07	7.70E+06	2.00E+11	2.00E+11	2.00E+11	7.70E+06	2.00E+11	7.70E+06	7.70E+06	7.70E+06	2.00E+11	7.70E+06
vsatp (cm/s)	2.50E+07	2.50E+07	7.70E+06	2.00E+11	2.00E+11	2.00E+11	7.70E+06	2.00E+11	7.70E+06	7.70E+06	7.70E+06	2.00E+11	7.70E+06
mun (cm^2/Vs)	4.00E+03	4.00E+03	8.00E+03	3.00E+04	3.00E+04	3.00E+04	8.00E+03	3.00E+04	8.00E+03	8.00E+03	8.00E+03	3.00E+04	8.00E+03
mup (cm^2/Vs)	2.00E+02	2.00E+02	4.00E+02	2.00E+05	2.00E+05	2.00E+05	4.00E+02	2.00E+05	4.00E+02	4.00E+02	4.00E+02	2.00E+05	4.00E+02

Giving the device structure, doping profile and material parameters, we can solve numerically the five fundamental equations as electron and hole current equations, Poisson equation and electron and hole continuity equations. In our simulation process, two modules were used specifically for our project. One module is called "BLAZE", which is a general purpose 2-D device simulator for III-V materials and devices with position dependent band structure (i.e., heterojunctions). "BLAZE" accounts for the effects of position-dependent band structure by modifications to the charge transport equations. The other module is "GIGA", which extends to account for the lattice heat flow (i.e., self heating), an important effect of relatively low thermal conductivity coefficient materials, such as GaAs.

Some important device models unique to "BLAZE" are covered below. These models include those for correlating the compound elemental concentrations and bandgap, free-carrier mobilities, recombination mechanisms, and free-carrier transport.

Drift-Diffusion Transport Model $\begin{aligned}\overrightarrow{J_n} &= qn\mu_n\overrightarrow{E_n} + qD_n\nabla n \\ \overrightarrow{J_p} &= qp\mu_p\overrightarrow{E_p} + qD_p\nabla p\end{aligned}$ for all materials and regions;

Constant Low Field Mobility Model $\begin{aligned}\mu_{n0} &= MUN\left(\frac{T_L}{300}\right)^{-TMUN} \\ \mu_{p0} &= MUP\left(\frac{T_L}{300}\right)^{-TMUP}\end{aligned}$ for all materials and regions;

Parallel Electric Field-Dependent Mobility Model

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}E}{VSATN}\right)^{BETAN}}\right]^{\frac{1}{BETAN}}$$

$$\mu_p(E) = \mu_{p0}\left[\frac{1}{1+\left(\frac{\mu_{p0}E}{VSATP}\right)^{BETAP}}\right]^{\frac{1}{BETAP}}$$

$$VSATN = \frac{ALPHAN.FLD}{1+THETAN.FLD\exp\left(\frac{T_L}{TNOMN.FLD}\right)}$$

$$VSATP = \frac{ALPHAP.FLD}{1+THETAP.FLD\exp\left(\frac{T_L}{TNOMP.FLD}\right)}$$ for all regions;

Shockley-Read-Hall (SRH) Recombination Model

$$R_{SRH} = \frac{pn - n_{ie}^{\ 2}}{TAUP0\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + TAUN0\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]}$$ for all materials and regions;

Optical Recombination Model $R_{np}^{\ OPT} = C_C^{\ OPT}\left(np - n_{ie}^{\ 2}\right)$, for III-V devices;

The Thermionic Emission Transport Model $\overrightarrow{J_n} = qv_n(1+\delta)\left[n^+ - n^- \exp\left(\frac{-\Delta E_C}{kT_L}\right)\right]$ $\overrightarrow{J_p} = (-q)v_p(1+\delta)\left[p^+ - p^- \exp\left(\frac{-\Delta E_V}{kT_L}\right)\right]$ for the current in abrupt heterojunctions;

The Lattice Heat Flow Model $C\frac{\partial T_L}{\partial t} = \nabla(K\nabla T_L) + H$ for all materials;

Trap-Assisted Tunneling Model

$$R_{SRH} = \frac{pn - n_{ie}^2}{\frac{TAUP0}{1+\Gamma_p^{DIRAC}}\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \frac{TAUN0}{1+\Gamma_n^{DIRAC}}\left[p + n_{ie}\exp\left(\frac{-ETRAP}{kT_L}\right)\right]}$$ for all materials.

4.4 Pre- and Post-stress TCAD Simulation Results

We now present the TCAD simulation results for the HBT without any defects added in the device, as the case of a pre-stress condition. Figure 4.4 compares the measured data with I-V characteristics simulated using the Thermionic Emission Transport Model (self heating). Good agreement between the simulation results and measurement data from moderate to high B-E biases was obtained. Although the simulation predicted quite accurately the stressed I-V behaviors in middle as well as high injection levels, it nonetheless failed to describe the large leakage current at the low B-E voltage region (below 0.9 V). We speculated this discrepancy was caused by extra current components generated from the damaged GaAs nitride interface at the

HBT peripheries (isolation regions etc.), which were not accounted in the device simulation. This leakage mechanism needs a more detailed study to understand such a phenomenon.

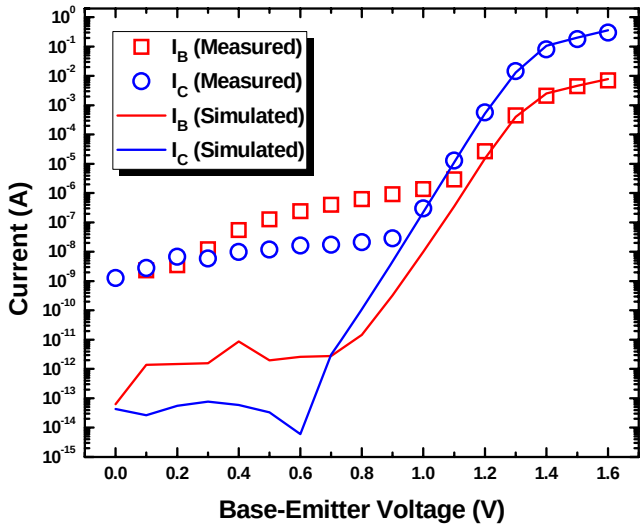


Figure 4.4 Pre-stress forward Gummel plots of measured data and simulation results.

To identify the possible origins contributing to the experimentally observed pre- and post-stress DUT behaviors, we need to simulate the current instability of the post-stress HBT. Stress-induced defects of different types, densities and locations were placed in the device structure to emulate the post-stress behaviors. As shown in Figure 4.5, the possible locations at which traps could be generated due to the stress include ledge sidewall, emitter sidewall, extrinsic base surface, heterojunction interface, emitter bulk and base bulk.

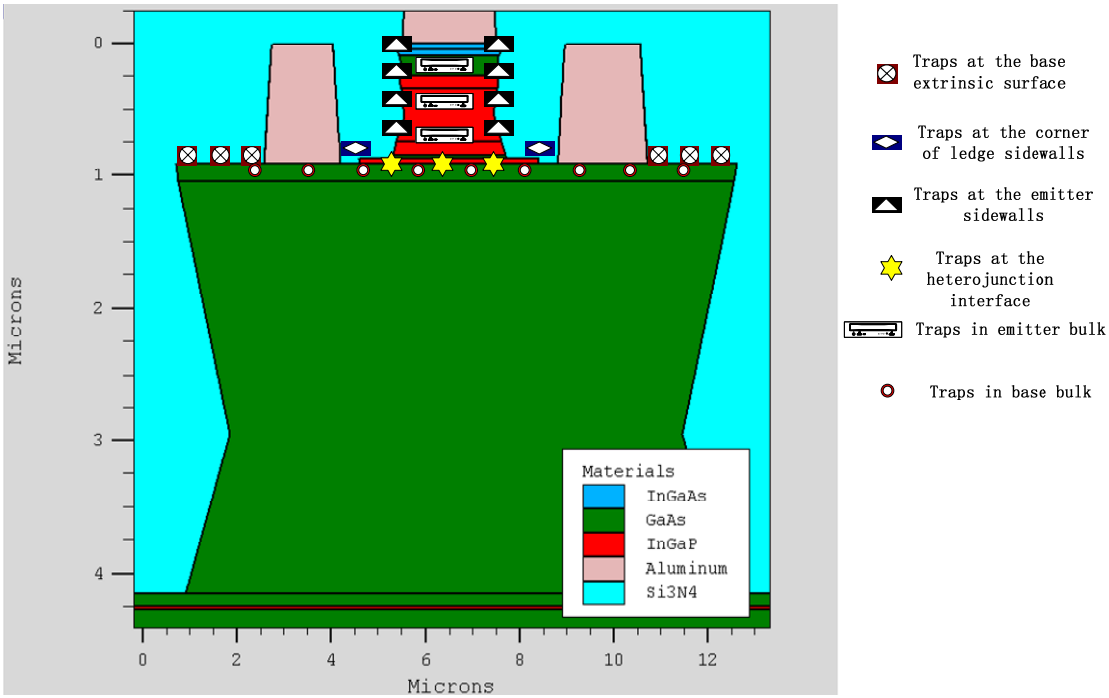


Figure 4.5 Device structure indicating the six possible locations for stress-induced defects.

Furthermore, both the donor-type and acceptor-type traps were considered. A donor-type trap is negatively charged when empty and becomes neural when emitting an electron. While the acceptor-type trap is positively charged when empty and becomes neutral when capturing an electron. We assumed the energy level of traps was located near the middle of energy bandgap, because this is the location where electron-hole recombination is most active via SRH recombination statistics. To make our simulation results sensible, we also considered trapping density within a range of a few orders higher or lower than the doping concentrations of emitter and base. In addition, the length of trapping distribution was chosen to be a value beyond which the current characteristics become insensitive to the length variation.

The effects of trapping states at the ledge sidewall were first examined, and a uniform acceptor-type trapping distribution with a density of $N = 3 \times 10^{16} / cm^2$ and length $L = 0.04 \mu m$ was considered. Figure 4.6 compares the simulated pre- and post-stress I-V characteristics.

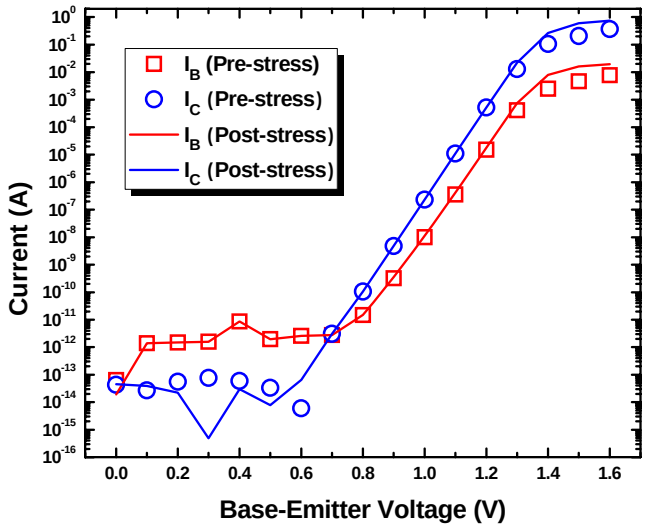


Figure 4.6 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located at the ledge sidewall.

As you can see from the figure, the collector current increased slightly while the base current increased notably due to the presence of such traps.

Next, trapping states at the emitter sidewall were considered, and acceptor-type traps with a distribution length $L = 0.87 \mu m$ were used. Figure 4.7 shows the simulated pre- and post-stress I-V characteristics. Again, the collector current increased very slightly while the base current over the intermediate and high voltage regions increased significantly. This phenomenon is commonly

observed in post-stress HBTs, and it suggests that the traps generated at the emitter sidewall play an important role in the HBT current gain degradation.

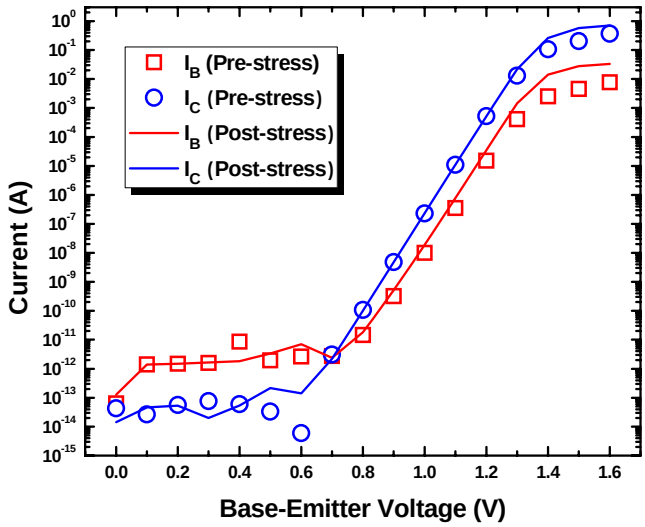


Figure 4.7 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located at the emitter sidewall.

As the highest temperature normally takes place in the heterojunction, stress-induced defects generated in this region are very likely. We now considered the effects of traps located near the B-E heterointerface. The distribution of traps was uniform in the x-axis covering the entire interface. Figure 4.8 presents simulated pre- and post-stress forward Gummel plots for the acceptor-type traps. Similar trends as those in Figure 4.7 were found, that is, both collector and base current increased, but with base current increased more significantly over the intermediate and high voltage regions. Further, no notable difference was found between the cases of acceptor-type and donor-type traps. This means the base current is not sensitive to the type of traps at the heterointerface.

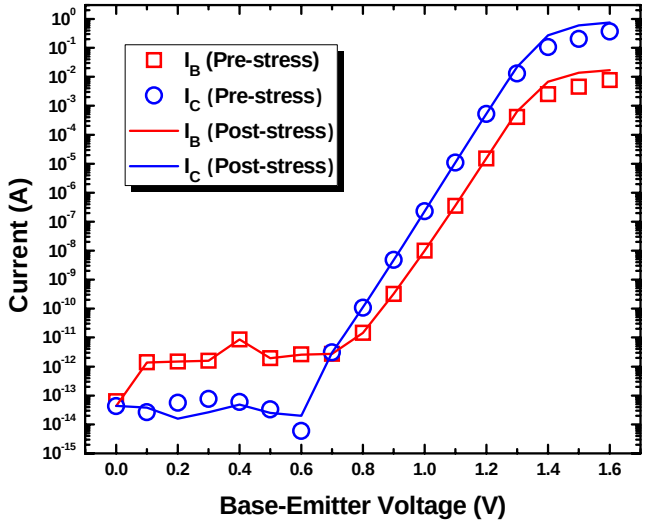


Figure 4.8 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located at the heterointerface.

The I-V characteristics of the HBT subjected to the presence of trapping states in the bulk of base was quite similar to those shown in Figure 4.8. As shown in Figure 4.9, the post-stress collector and base currents increased slightly in the high voltage region. The traps were assumed distributed uniformly in the base with a trapping density $N = 4 \times 10^{18} / cm^2$.

Then the traps generated at the extrinsic base surface were considered, and a uniform trap distribution with a density $N = 4 \times 10^{18} / cm^2$ and length located between the edge of base and base contact and between the emitter sidewall and base contact was implemented in the simulation. Figure 4.10 shows the simulated results for the cases of acceptor-type traps. Again, trends similar to those in Figure 4.8 and 4.9 were found.

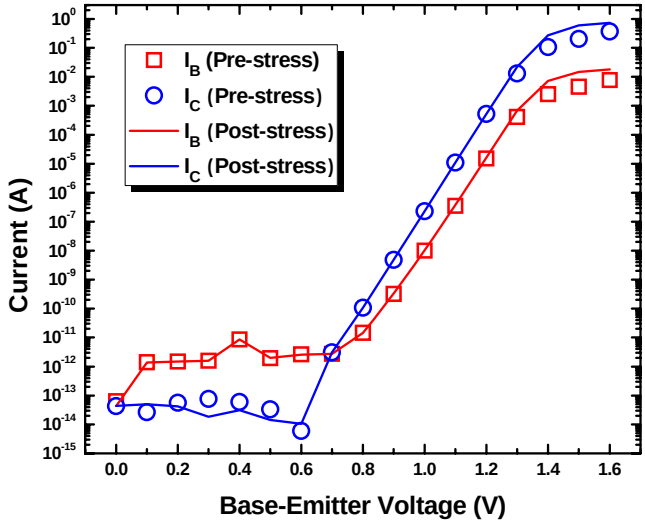


Figure 4.9 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located in the base bulk.

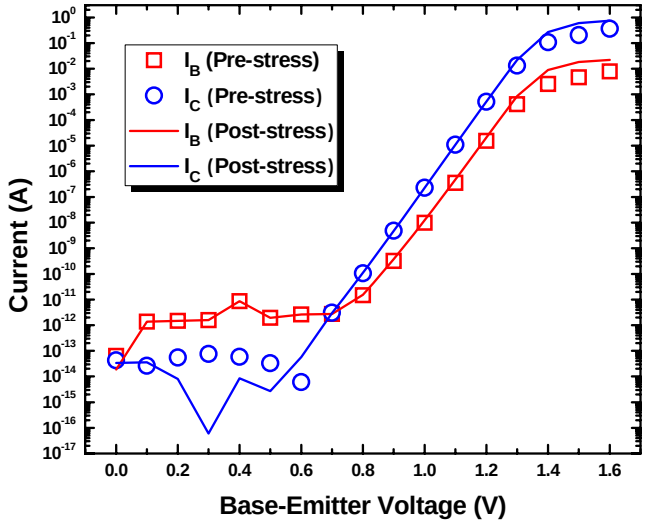


Figure 4.10 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located in the extrinsic base surface.

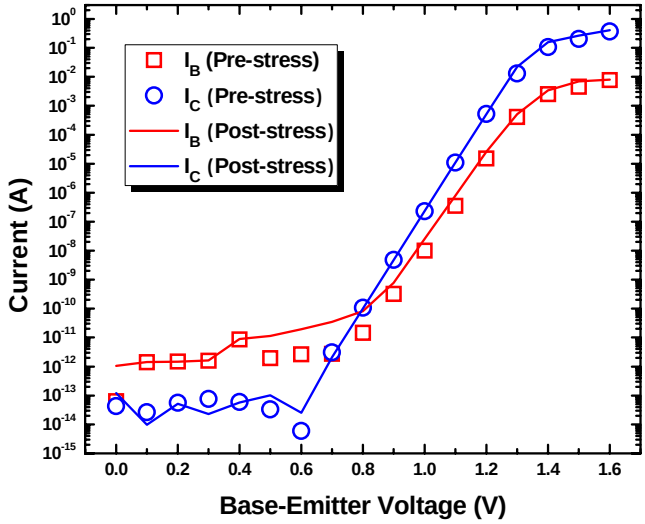


Figure 4.11 Simulated pre- and post-stress forward Gummel plots considering acceptor-type traps located in the emitter bulk.

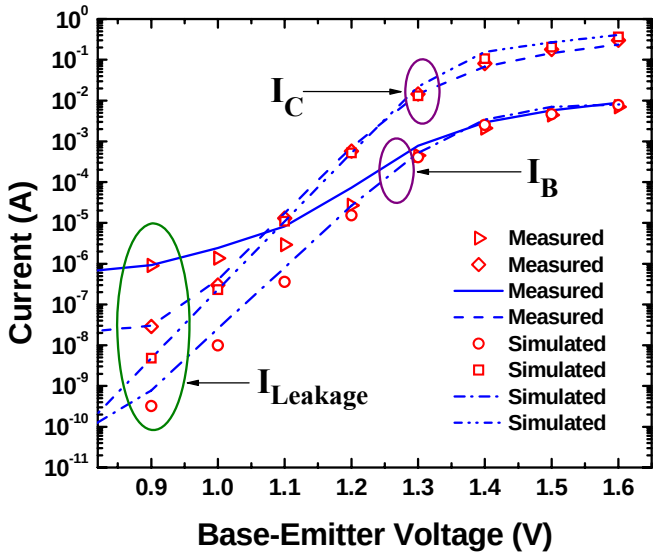


Figure 4.12 Pre- and post-stress measured and simulated forward Gummel plots considering acceptor-type traps in the emitter bulk. Symbols: pre-stress data, lines: post-stress results.

From this approach, finally we found the presence of acceptor-type defects in the emitter bulk with a density of $N = 10^{15} / cm^2$ gave rise to the trend observed in our experiments, that is, the collector current is almost unchanged while the base current over the intermediate voltage range is increased notably in Figure 4.11. Figure 4.12 shows very good agreement between the simulation results and measurement data. Thus, it is suggested that the acceptor-type trapping states located in the emitter bulk are responsible for the commonly seen post-stress base current instability over the moderate base-emitter voltage region.

4.5 Conclusion

In our 2-D TCAD device simulations, trapping energy levels were set to be very close to the bottom of conduction band, so it is quite easy for the trapping centers to recombine the electrons from the bottom of the conduction band, which accelerates the recombination rate in the emitter as well as the electron injection rate from the negative terminal of voltage supply, which results in base current increase.

When trapping density is set a few orders lower than the emitter doping concentration, at low V_{BE} (low injection level), the degradation is not significant because the recombination rate in the emitter is not very high at that time.

However, when in mid-voltage range of V_{BE} (moderate injection level), the trapping centers begin to recombine the electrons in the emitter significantly and electron injection rate from

negative terminal of voltage supplier becomes increasing, base current therefore increases significantly. When in high V_{BE} (high injection level), as the number of trapping centers decreases significantly, the recombination rate in the emitter also decreases a lot, the base current therefore increases very slightly. The base is p-type heavily doped with connection to the positive terminal of voltage supply, which can provide a huge bunch of holes to recombine the electrons injected from the emitter, the collector current therefore only increases a little.

Therefore, the change of bulk recombination current in the emitter bulk is identified as a primary degradation mechanism confirmed by 2-D TCAD device simulations.

CHAPTER 5: COMPREHENSIVE COMPACT MODELING OF ELECTROTHERMAL STRESS-INDUCED INGAP/GAAS HBT DEVICE PERFORMANCE DEGRADATIONS

5.1 SPICE Gummel-Poon Model and Equivalent Circuits

Accurate extraction of device models is essential for modeling and simulation of integrated circuits. It is also important for device reliability studies where changes in the device characteristics are monitored to determine the degradation mechanisms in the device. Within this context, the InGaP/GaAs HBT is of growing importance for applications in various areas including analog and MMICs. However, device characteristics and operation of InGaP/GaAs HBTs differ in several respects from those of conventional Si BJTs. The determination of HBT device models, therefore, requires additional considerations and the procedures used for analysis must deviate from those conventionally used for BJTs.

SPICE Gummel-Poon (SGP) model is a physics-based, accurate, scalable, robust and predictive bipolar transistor model for circuit simulations. It has been widely used by many semiconductor and IC design companies worldwide. This model will be adopted for our InGaP/GaAs HBT reliability study.

There are four operating modes of an InGaP/GaAs HBT as illustrated in Figure 5.1, and our analysis will focus on the forward active mode. Figure 5.2 shows the physical components in an NPN HBT, and Figure 5.3 shows the large-signal equivalent circuit of the SGP model. From

Figure 5.3, the small-signal equivalent circuit for high frequency simulations can also be derived. This means that all the model components are linearized at a given AC operating point, and the small-signal equivalent circuit is shown in Figure 5.4. Such a schematic will be used for our compact modeling, and the values of the model parameters will be extracted in the next section.

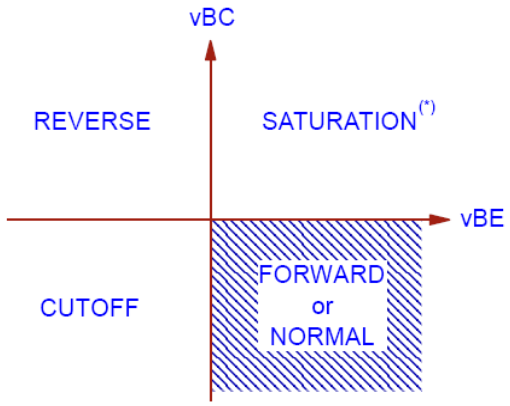


Figure 5.1 Operation modes of the NPN InGaP/GaAs HBT.

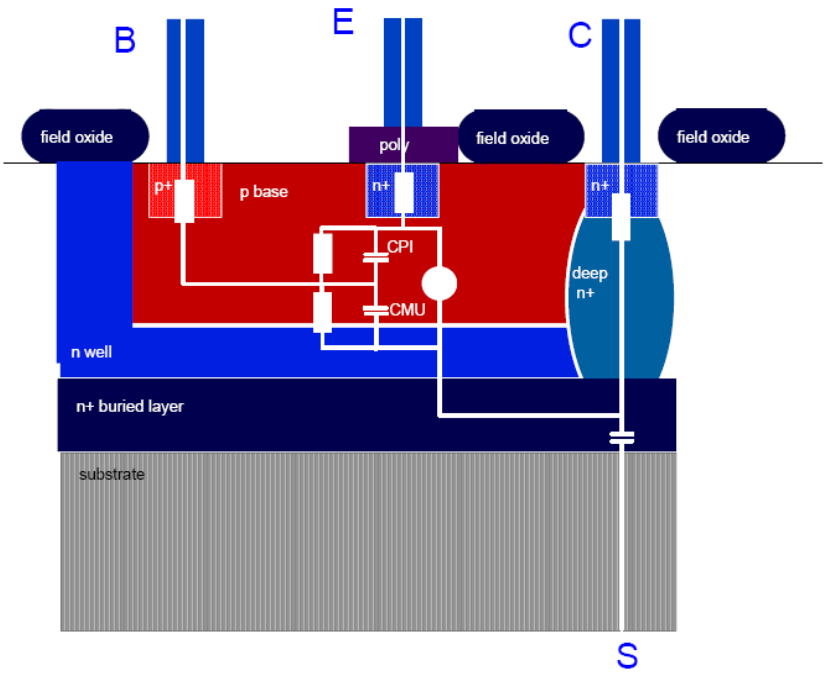


Figure 5.2 Physical components in the NPN InGaP/GaAs HBT.

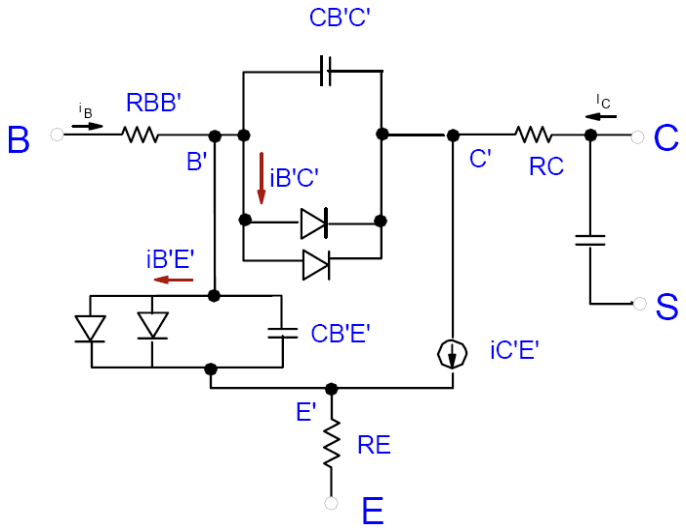


Figure 5.3 SGP large-signal equivalent circuit of the InGaP/GaAs HBT.

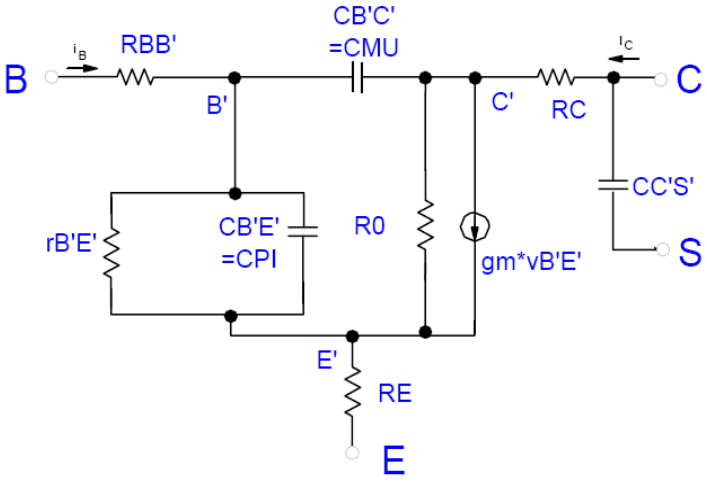


Figure 5.4 SGP small-signal equivalent circuit of the InGaP/GaAs HBT.

5.2 Development of SGP Model Extraction Methodology

SGP models can be used to accurately simulate the ideal (constant current gain) region and the non-ideal regions of BJT operation in which the effects of base recombination current, high-level injection, and parasitic resistances are significant. However, HBTs do not exhibit a region of operation where the DC current gain is constant. Due to strong and dominant recombination in the base-emitter SCR, the base current ideality factor takes on the values in the range of 1.4 to 2.0 over the bias range, for normal operation of HBT devices. As a result, to use the SGP models to represent an HBT and, in particular, apply them to analytical calculations such as simulation of MMICs incorporating HBTs, a model extraction technique needs to be developed. In order to extract SGP model accurately from the pre- and post-stress measurement data, we have developed a MathCAD-based modeling tool. The model equations used in our model extraction tool are summarized in the following list [34]:

Ideal forward diffusion current $$i_f = IS \times \left[\exp\left(\frac{VBE}{NF \times VT} \right) - 1 \right] \quad (11)$$

Ideal reverse diffusion current $$i_r = IS \times \left[\exp\left(\frac{VBC}{NR \times VT} \right) - 1 \right] \quad (12)$$

B-E recombination effect $$i_{BErec} = ISE \times \left[\exp\left(\frac{VBE}{NE \times VT} \right) - 1 \right] \quad (13)$$

B-C recombination effect $$i_{BCrec} = ISC \times \left[\exp\left(\frac{VBC}{NC \times VT} \right) - 1 \right] \quad (14)$$

The above equations give $$i_B = \frac{i_f}{BF} + i_{BErec} + \frac{i_r}{BR} + i_{BCrec} \quad (15)$$

Non-ideality for the base width modulation $q_1 = \dfrac{1}{1 - \dfrac{VBE}{VAR} - \dfrac{VBC}{VAF}}$ (16)

Non-ideality for the high level injection effect

$$q_2 = \frac{IS}{IKF} \times \left[\exp\left(\frac{VBE}{NF \times VT} \right) - 1 \right] + \frac{IS}{IKR} \times \left[\exp\left(\frac{VBC}{NR \times VT} \right) - 1 \right] \quad (17)$$

The base charge $q_b = \dfrac{q_1}{2}\left(1 + \sqrt{1 + 4q_2}\right)$ (18)

The above equations give $i_C = \dfrac{1}{q_b}\left(i_f - i_r\right) - \dfrac{i_r}{BR} - i_{BCrec}$ (19)

The proposed SGP model extraction and optimization approach is described as follows: Extract *VAR* and *VAF* from the measured output characteristics; Then, extract *IS*, *NF*, *ISE*, *NE* and *BF* from the measured forward Gummel plot; Optimize the simulated Gummel plot for *IS*, *NF*, *ISE* and *NE* well before the ohmic effect takes place; Extract *IKF* from the measured current gain plot; Extract the parasitic resistors *RE*, *RB* and *RC* from the DC measurements; Optimize *RE* in the upper region of the simulated Gummel plot; Optimize *BF* and *IKF* in the simulated beta plot at high bias; Check fitting results and fine-tune parameters if necessary.

5.3 SPICE Gummel-Poon Compact Modeling Results

First, the SGP model equations were solved and then the values of the model parameters for a best curve fitting result were obtained by non-linear regression analysis. Figure 5.5 and 5.6 are comparisons between measurement data and SGP model predictions of pre- and post-stress

forward Gummel plot and forward β plot at $T_J = 200°C$, respectively. Good agreement between the measured data and SGP models demonstrates the model validity and accuracy of the approach proposed.

The electrothermal stress-induced increase in base current at the moderate B-E voltage region was quite significant, while collector currents were relatively unchanged after stress. Consequently, the post-stress current gain decreased significantly as a function of stress time.

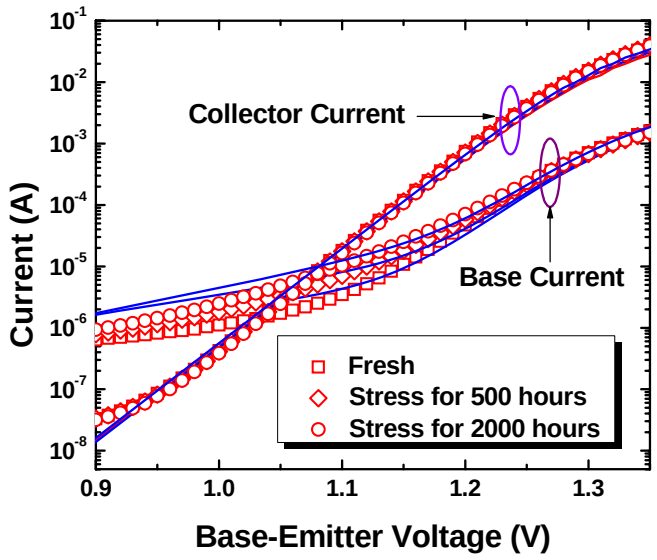


Figure 5.5 Comparison between measured data and model predictions of forward Gummel plot before and after stress @ T_J = 200 °C. Symbols: experimental data; lines: model prediction results using SGP model equations.

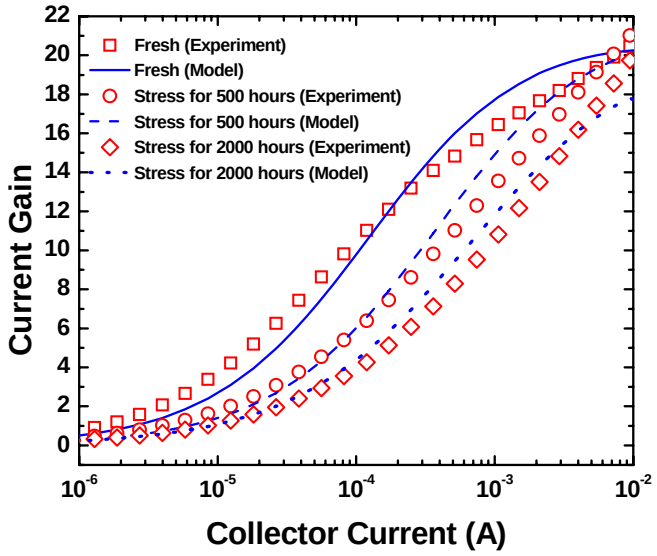


Figure 5.6 Comparisons between measured data and model predictions of forward current gain before and after stress @ $T_J = 200$ °C.

Table 5.1 to 5.3 show the extracted pre- and post-stress SGP models at $T_J = 200°C$, $T_J = 245°C$ and $T_J = 265°C$, respectively.

Clearly, the forward current gain *BF* decreased along with the accumulative stress time and its degradations increased with the elevated junction temperatures. While the B-E leakage emission coefficient *NE*, the B-E leakage saturation current *ISE* and the forward knee current *IKF* increased with the accumulative stress time and the degradations also increased with the elevated junction temperature. The parasitic resistances *RB*, *RE* and *RC* changed after stress as well.

Table 5.1 Extracted pre- and post-stress SGP models @ T_J = 200 °C.

Notation	Parameter Name	Pre-stress (0 hour)	Post-stress (500 hours)	Post-stress (2000 hours)	Percentage Shift
IS	transport saturation current (A)	2.3×10^{-22}	2.3×10^{-22}	2.3×10^{-22}	0.00%
BF	ideal forward maximum current gain	25	22	16	-36.00%
BR	ideal reverse maximum current gain	0.9	0.9	0.9	0.00%
VAF	forward Early voltage (V)	100	100	100	0.00%
VAR	reverse Early voltage (V)	50	50	50	0.00%
NF	forward current emission coefficient	1.097	1.097	1.097	0.00%
NR	reverse current emission coefficient	1.01	1.01	1.01	0.00%
NE	B-E leakage emission coefficient	9.4	9.8	11	17.02%
NC	B-C leakage emission coefficient	1.3	1.3	1.3	0.00%
ISE	B-E leakage saturation current (A)	1.5×10^{-8}	1.6×10^{-8}	1.8×10^{-8}	20.00%
ISC	B-C leakage saturation current (A)	2.1×10^{-13}	2.1×10^{-13}	2.1×10^{-13}	0.00%
IKF	forward Knee current (A)	1.2	1.4	1.5	25.00%
IKR	reverse Knee current (A)	0.55	0.55	0.55	0.00%
RB	zero bias base resistance (Ω)	12	14	15	25.00%
RE	emitter resistance (Ω)	0.5	0.45	0.45	-10.00%
RC	collector resistance (Ω)	3	2	3	0.00%

Table 5.2 Extracted pre- and post-stress SGP models @ T_J = 245 °C.

Notation	Parameter Name	Pre-stress (0 hour)	Post-stress (500 hours)	Post-stress (2000 hours)	Percentage Shift
IS	transport saturation current (A)	2.3×10^{-22}	2.3×10^{-22}	2.3×10^{-22}	0.00%
BF	ideal forward maximum current gain	25	18	14	-44.00%
BR	ideal reverse maximum current gain	0.9	0.9	0.9	0.00%
VAF	forward Early voltage (V)	100	100	100	0.00%
VAR	reverse Early voltage (V)	50	50	50	0.00%
NF	forward current emission coefficient	1.097	1.097	1.097	0.00%
NR	reverse current emission coefficient	1.01	1.01	1.01	0.00%
NE	B-E leakage emission coefficient	9.4	10.7	13.2	40.43%
NC	B-C leakage emission coefficient	1.3	1.3	1.3	0.00%
ISE	B-E leakage saturation current (A)	1.5×10^{-8}	1.65×10^{-8}	2.2×10^{-8}	46.70%
ISC	B-C leakage saturation current (A)	2.1×10^{-13}	2.1×10^{-13}	2.1×10^{-13}	0.00%
IKF	forward Knee current (A)	1.2	1.6	1.71	42.50%
IKR	reverse Knee current (A)	0.55	0.55	0.55	0.00%
RB	zero bias base resistance (Ω)	12	17.5	18	50.00%
RE	emitter resistance (Ω)	0.5	0.36	0.35	-30.00%
RC	collector resistance (Ω)	3	2.8	2.5	-16.67%

Table 5.3 Extracted pre- and post-stress SGP models @ T_J = 265 °C.

Notation	Parameter Name	Pre-stress (0 hour)	Post-stress (500 hours)	Post-stress (2000 hours)	Percentage Shift
IS	transport saturation current (A)	2.3×10^{-22}	2.3×10^{-22}	2.3×10^{-22}	0.00%
BF	ideal forward maximum current gain	25	16	12	-52.00%
BR	ideal reverse maximum current gain	0.9	0.9	0.9	0.00%
VAF	forward Early voltage (V)	100	100	100	0.00%
VAR	reverse Early voltage (V)	50	50	50	0.00%
NF	forward current emission coefficient	1.097	1.097	1.097	0.00%
NR	reverse current emission coefficient	1.01	1.01	1.01	0.00%
NE	B-E leakage emission coefficient	9.4	12.7	15.5	64.89%
NC	B-C leakage emission coefficient	1.3	1.3	1.3	0.00%
ISE	B-E leakage saturation current (A)	1.5×10^{-8}	1.85×10^{-8}	2.6×10^{-8}	73.30%
ISC	B-C leakage saturation current (A)	2.1×10^{-13}	2.1×10^{-13}	2.1×10^{-13}	0.00%
IKF	forward Knee current (A)	1.2	2	2	66.67%
IKR	reverse Knee current (A)	0.55	0.55	0.55	0.00%
RB	zero bias base resistance (Ω)	12	16	17.5	45.83%
RE	emitter resistance (Ω)	0.5	0.41	0.37	-26.00%
RC	collector resistance (Ω)	3	2.8	1.8	-40.00%

CHAPTER 6: STRESS-INDUCED INGAP/GAAS HBT-BASED MMICS PERFORMANCE DEGRADATIONS

6.1 Stress-induced HBT-based MMICs Performance Prediction Methodology

While many studies have been devoted to the field of GaAs HBT reliability, most of the works were focused only on the device characteristics analysis and not much attention was paid to study the reliability of GaAs HBT-based MMICs. Furthermore, there is no systematic methodology to evaluate the HBT circuit performance degradations due to the stress effects. To improve the HBT-based circuit reliability, it is desirable to evaluate the impact of stress effect on circuit performance during the design phase. Therefore, we proposed a practical approach shown in Figure 6.1 to synthesize the device characterization data with EDA tools and analytical equations to perform the analysis of the stress-induced performance degradation of the InGaP/GaAs HBT-based MMICs. This methodology is accurate and it is a helpful tool for the design of more reliable HBT-based RF circuits. In this method, the DUTs are first stressed under different stress conditions and SGP models are then extracted from both the pre- and post-stress measured data. This is followed by importing the fresh and stressed device models into RF EDA tools, such as ADS, from which the degraded MMIC performance can be obtained.

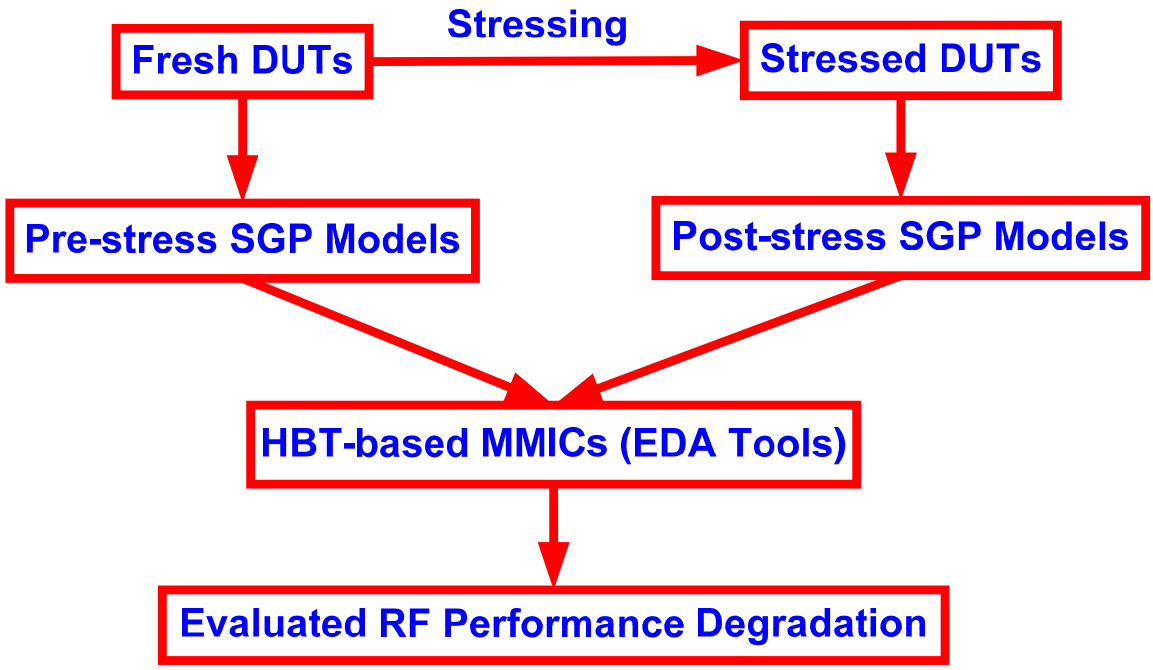


Figure 6.1 Flow chart of the stress-induced HBT-based MMICs degraded performance evaluation methodology.

6.2 InGaP/GaAs HBT-based RF Power Amplifier Performance

6.2.1 Introduction

It has been illustrated in Chapter 3 that InGaP/GaAs HBT DC performance degraded significantly after the electrothermal stress. It would be of great interest and importance to know how much the InGaP/GaAs HBT-based MMIC circuit performances would degrade after the stress. For applications where the operation of the circuit hinges on the lifetime and performance of a single device, it is important that all aspects of the reliability and the various known degradation modes and mechanisms be addressed prior to the insertion of such a device into a

circuit. Thus, reliability analysis and detailed knowledge of the circuit applications are necessary in order to determine the suitability of the selected device. Only by proving a high degree of reliability can InGaP/GaAs HBTs then be used in MMICs.

Power amplifiers, used in the transmitter of RF circuits to amplify a sufficiently large signal to the antenna, have trade-off between the efficiency and linearity. Higher efficiency leads to extended battery life, an important issue in the portable electronics. Several recent studies have highlighted the difficulty in achieving high efficiency and linearity in power amplifiers. The linearity and efficiency can be varied in such an amplifier by adjusting the input bias level to be either close to class-A biasing or close to class-B biasing. If a class-AB circuit is biased toward class-A, higher linearity and lower efficiency will be obtained, and vice versa. This useful compromise between the linearity and efficiency makes class-AB circuit a popular choice for power amplifiers. Several class-AB amplifiers have been reported in the literature with efficiencies between 30% and 60% [35-38]. Here, we consider a class-AB RF PA in our study for its optimal performance.

6.2.2 1.575 GHz Class-AB InGaP/GaAs HBT-based RF PA

Figure 6.2 shows the circuit diagram of a class-AB InGaP/GaAs HBT-based RF power amplifier. A single-ended topology has been chosen, and the input matching network is a high-pass filter consisting of a series capacitor C_1 to fulfill the criterion of DC blocking and two inductors L_1 and L_2 connected to the bias supply source to bias the base of the HBT (i.e. DUT). So L_1 and L_2 serve as biasing elements as well as a part of the matching network. The input matching network

transforms the input impedance of the DUT to a 50-Ω source impedance. The DUT is in the CE configuration with an off-chip RF choke L_3 connected to the collector. The RF choke L_3 functions like a current source, and the advantage of the RF choke over an on-chip current source is that it does not impose any limit on the collector voltage swing of the transistor so the collector voltage can go higher than the supply voltage to achieve a higher efficiency. In the output stage, a parallel-tuned LC network (C_3 and L_4) is used to provide a zero conductance (that is, infinite impedance) at the tuning operation frequency and infinite conductance (zero impedance) for any other frequency. When connected in parallel to a load resistor R_L, the parallel-tuned LC network only allows a sinusoidal current with the operation frequency to flow through the load. The voltage across the RLC parallel group is sinusoidal, while the total current (that is, the sum of the current through load and the current through the LC tank) may have any waveform. The values of the circuit components are: RF_{in} = 1.575 GHz, C_1 = 2 μF, C_2 = 1 μF, C_3 = 10 pF, R_1 = R_2 = 50 Ω, L_1 = L_2 = 1 nH, L_3 = 200 nH, L_4 = 1 nH, R_L = 50 Ω. The HBT biases are V_1 = 1.3 V and V_{CC} = 14 V.

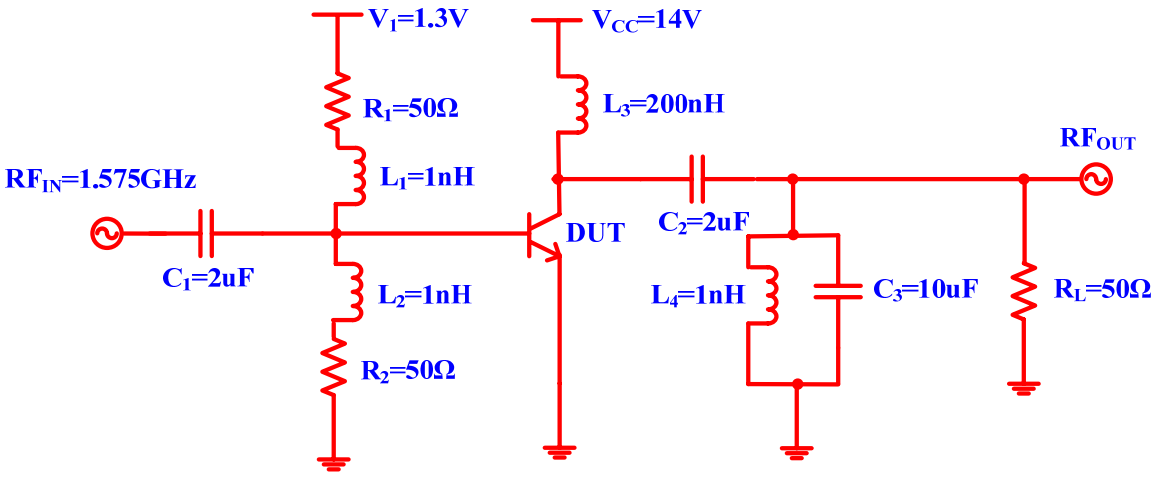
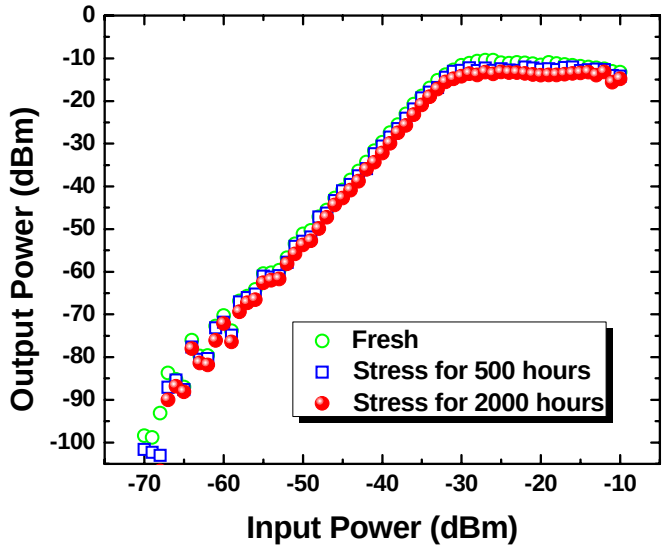
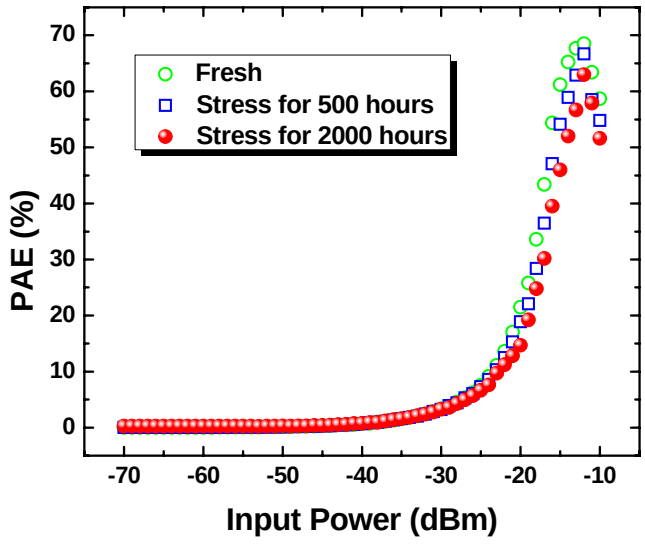


Figure 6.2 A class-AB power amplifier used in this study.

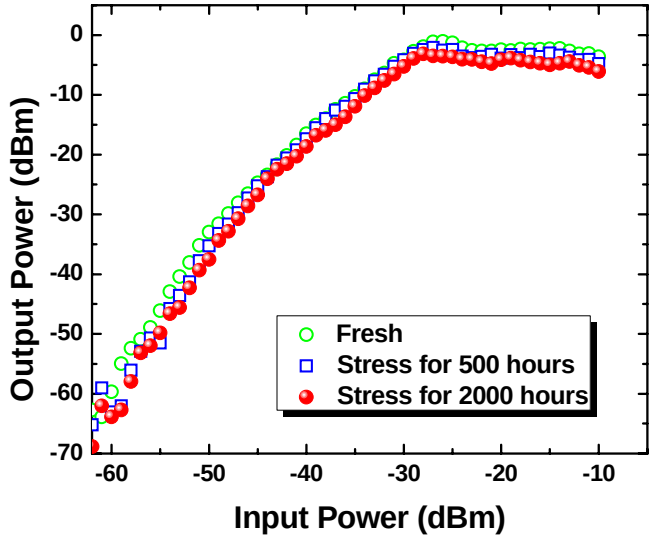


(a)

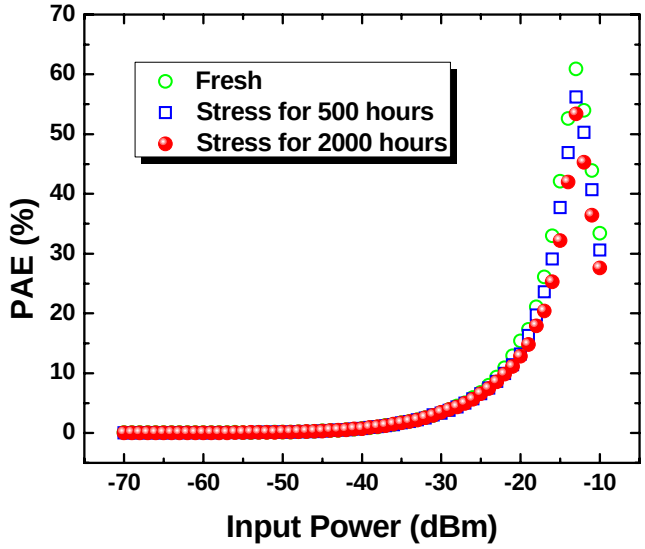


(b)

Figure 6.3 (a) Simulated output power vs. input power; (b) Simulated power-added efficiency vs. input power at $T_J = 200°C$.



(a)



(b)

Figure 6.4 (a) Simulated output power vs. input power; (b) Simulated power-added efficiency vs. input power at $T_J = 265°C$.

RF PA circuit simulations were carried out using Cadence SpectreRF simulator with the fresh and stressed SGP models extracted and discussed in the previous chapter. The simulated pre- and post-stress output power and power-added efficiency as a function of the input power are given in Figure 6.3 (a) and (b) for $T_J = 200°C$, and Figure 6.4 (a) and (b) for $T_J = 265°C$, respectively.

The results indicated that the RF performance degradations of the InGaP/GaAs HBT-based PA subject to the long-term electrothermal stress were very minimal even though the core device DC current gain decreased significantly.

6.2.3 Conclusion

The RF performances of an InGaP/GaAs HBT-based class-AB RF PA were simulated and analyzed in Cadence SpectreRF circuit simulator. It was interesting to find that the PA's post-stress output power and power-added efficiency changed only slightly even though the post-stress core device DC current gain decreased significantly. Thus, it can be suggested from this study that there is no direct correlation between the HBT device characteristics degradations and HBT-based RF PA performance shifts.

6.3 InGaP/GaAs HBT-based Low-Noise Amplifier Performance

6.3.1 Introduction

The LNA is a fundamental building block in all communications systems and plays an important role in any receiver chain. This block has a large impact on the overall system sensitivity and dynamic range performance. Its main function is to amplify extremely low signals without adding noise, thus preserving the required signal-to-noise ratio (SNR) of the system at low power levels. Additionally, for large-signal levels, the LNA amplifies received signal without introducing any distortions, which eliminates channel interference. Proper LNA design is crucial in today's communication technology. Because of the complexity of the signals in today's digital communications, additional design considerations need to be addressed during an LNA design procedure.

The design of a LNA is quite awkward because it is a trade-off among a lot of circuit characteristics. For instance, an LNA must provide a certain amount of power gain while maintaining a minimum noise figure (NF). Moreover, power consumption must be kept as low as possible and occupation of die area limited. The number of external components must also be minimized.

There are several options on designing an LNA. It can be either single-ended or differential. It can also be either single-stage or multi-stage. There are always trade-offs in these design options. For example, the single-ended LNA has at least one important shortcoming that it is sensitive to

the parasitic ground inductance. The differential LNA can solve this problem, but for a given power consumption, the NF of a differential LNA is much higher than its single-ended counterpart [39]. A multi-stage LNA has a larger gain, however, its stability is more difficult to handle than that of the single-stage LNA.

6.3.2 2.4 GHz InGaP/GaAs HBT-based LNA

The base of InGaP/GaAs HBT is heavily doped for high linearity and high frequency performance and it is preferred for the design of power amplifiers. In result, the base resistance of InGaP/GaAs HBT shows low noise figure, and for this reason, it can be suitable for not only PA, but also LNA. And the industrial InGaP/GaAs HBT-based LNA shows excellent linearity and noise characteristics because of its high base doping concentration.

A two-stage, single-ended InGaP/GaAs HBT-based LNA for the IEEE 802.11g standard operating at 2.4 GHz [40] has been chosen in our reliability study. Figure 6.5 shows the schematic of the LNA including the input and output matching networks. The capacitors C_1 and C_2 fulfill the criterion of DC voltage blocking. They also tune out the inductors to serve as part of the matching networks to transform the input and output impedances to 50-Ω source impedance. Transistor Q_1 forms the inductively-degenerated common-emitter transconductance stage, which converts the RF input power into current. Transistor Q_3 is used to bias the base of Q_1, and resistor R_1 is designed to isolate the bias circuitry from the input of the transconductance stage. R_1 is typically designed to have a large resistance in order to reduce the noise contribution from the bias circuitry and avoid significant loading on the RF input port, which would increase

the noise figure. On the other hand, a small resistance is needed to improve the linearity of the transconductance stage. Hence, there is a trade-off between NF and linearity in choosing the value of R_1. Transistor Q_2 eliminates the Miller effect on the B-C parasitic capacitor, making input and output matching simple and almost independent to each other to enable a good reverse isolation and thereby providing excellent stability [41]. L_1 and L_3 are used to optimize the input and output matching conditions, whereas L_2 is the degeneration inductor to provide noise matching and gain matching at the same time, improve linearity and reduce internal noise by feedback. All the components are designed to optimize the figure of merits (FOM) for the LNA under the fresh condition. The values of these circuit components are: RF_{in} = 2.4 GHz, P_{in} = -50 dBm, C_1 = 0.33 µF, C_2 = 0.33 µF, R_1 = R_2 = 500 Ω, R_3 = 400 Ω, L_1 = 300 pH, L_2 = 15 pH, L_3 = 20 nH, and supply voltage V_{CC} = 5 V.

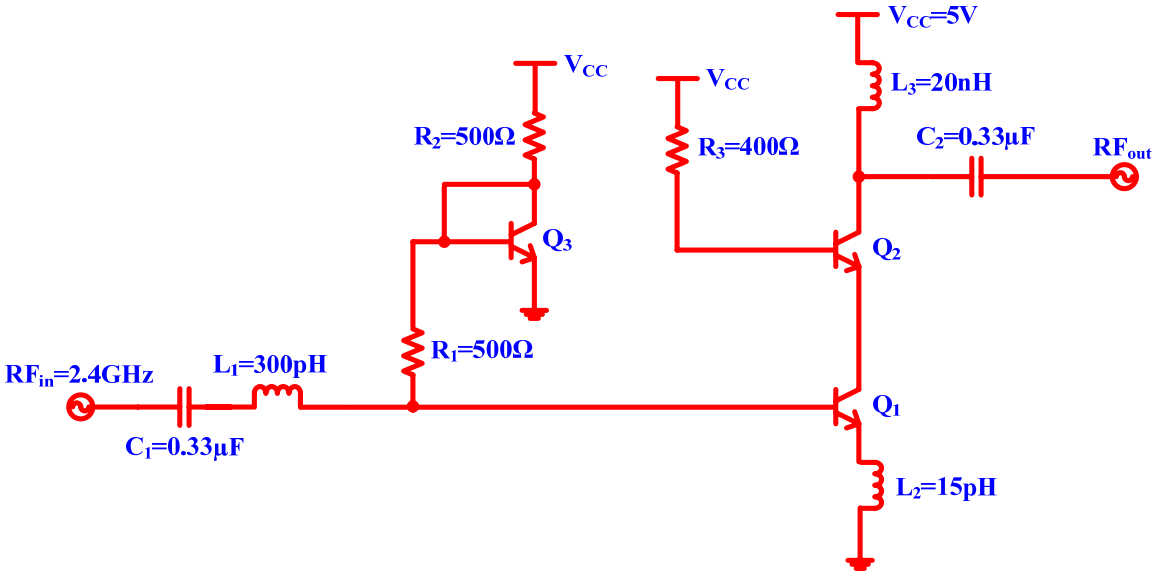


Figure 6.5 Two-stage single-ended InGaP/GaAs HBT-based RF low-noise amplifier.

The LNA is primarily characterized by the power gain, NF, and input 3rd-order intercept point (IIP3). The post-stress SGP models can alter the optimized matching point and degrade the LNA circuit performance. The 2.4 GHz LNA's S-parameters, NF and IIP3 shifts as a function of the cumulative stress time at $T_J = 200°C$ are given in Table 6.1.

Table 6.1 Simulated stress-induced InGaP/GaAs HBT-based LNA's RF performance shifts.

Parameter @ 2.4 GHz	**Stress Time**		
	Fresh	**500 Hours**	**2000 Hours**
S_{11} (dB)	-45.31	-43.59	-42.57
S_{12} (dB)	-87.33	-87.37	-87.57
S_{21} (dB)	13.08	12.67	11.33
S_{22} (dB)	-101.3	-97.82	-92.05
NF (dB)	2.71	2.73	3.04
NF_{min} (dB)	2.61	2.62	2.89
IIP3 (dBm)	5.33	4.89	3.16

At the operating frequency of 2.4 GHz, S_{11} and S_{12} changed slightly, the amplitude of the input return loss degraded 6%, and the output return loss degraded only 0.27% after 2000-hour of stress. On the other hand, the forward transducer gain S_{21} diminished 13.4% and the reverse isolation changed 23% after stress. Considering the 2000-hour long-term stress time and a significant decrease in the HBT's DC current gain, the power gain S_{21} degradation was still quite limited. The NF and the NF_{min} degraded 12.2% and 10.7%, respectively, at 2.4 GHz after 2000-hour of stress. Figure 6.6 shows the pre- and post-stress NF_{min} as a function of frequency. Since the noise performance of the LNA dominates the NF of a RF receiver and the DUT Q_1 dominates

the NF of the LNA [42], the primary noise sources in Q_1 come from its base current I_B, base resistance R_B and collector current I_C. Their respective noise spectral densities are $2qI_B$, $4kT/R_B$ and $2qI_C$. After the stress, the base current increased significantly and the collector current remains unchanged, while the base resistance also increased. Thus, the noise spectral density associated with the base current increased, while the base resistance thermal noise spectral density decreased after stress. This made the overall NF increased by 12.2%.

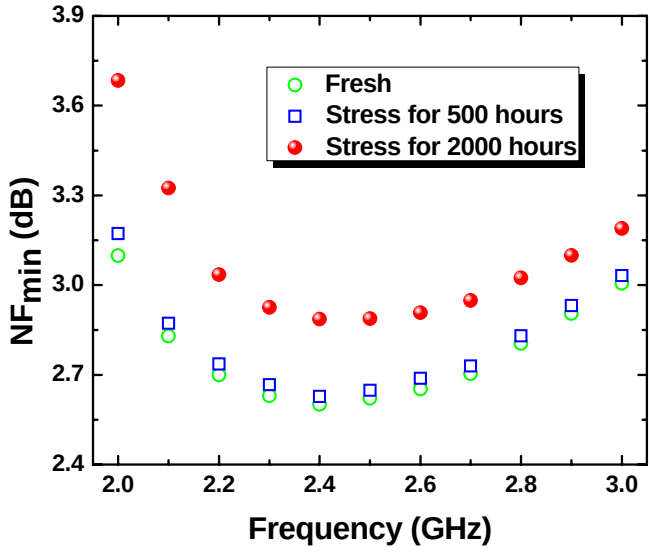


Figure 6.6 Simulated pre- and post-stress NF_{min} of the InGaP/GaAs HBT-based LNA.

From analytical point of view, the noise figure equation is given as $NF = NF_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|$ [43], where R_n is the noise resistance, Y_s is the source termination admittance and $Y_{s,opt}$ is the optimum noise matching source admittance. The noise resistance determines the sensitivity of noise figure to derivations from the optimum noise source admittance. If Y_s is equal to $Y_{s,opt}$, the NF of Q_1 reaches its minimal value NF_{min}. In our case, the values of NF were quite close to that

of NF_{min}, indicating the source was noise matched. After the long-term stress, the reduction of current gain increased the value of NF_{min}. The increase in NF_{min} together with the increases in R_n and I_B changed the real part of the complex input impedance from the optimum noise matching condition and therefore degraded the NF after stress.

To evaluate the linearity degradation, two-tone simulation was performed for the LNA at 2.4 GHz. Volterra series analysis shows that the linearity performance relates to the device parameters of Q_1 (i.e. impedance at the base and emitter, transconductance, dynamic base resistance and parasitic capacitances). The simulated IIP3 changed from 5.33 dBm for the fresh condition to 3.16 dBm after the 2000-hour stress, suggesting a considerable degradation in the linearity of LNA.

6.3.3 Conclusion

A 2.4 GHz cascode InGaP/GaAs HBT-based LNA subject to the electrothermal stress was studied and its stress-induced RF performance degradations at $T_J = 200°C$ were evaluated using the extracted SGP models and Cadence SpectreRF simulator. The cascode LNA's post-stress small-signal power gain, NF and linearity showed moderate to significant degradations after a 2000-hour stress.

6.4 InGaP/GaAs HBT-based Voltage-controlled Oscillator Performance

6.4.1 Introduction

The increased demands for high speed data communications drive the development of PLL based frequency synthesizer [44]. Voltage-controlled oscillator (VCO) is the critical block in the PLL and it dominates almost all spectral purity performance. It is desirable for the VCO to generate low-noise signal with sufficient output power, wide tuning range and high stability.

Traditionally, GaAs pseudomorphic high electron mobility transistor (pHEMT) or InP based MMIC technology has dominated in millimeter-wave oscillators because of their high f_T and f_{max} as well as their superior low noise performance [45-46]. But these technologies are very expensive. Thus, for low phase noise millimeter-wave VCO application, InGaP/GaAs HBTs are quickly becoming the preferred technology to be used due to their inherently low device 1/f noise characteristics, reliable fabrication process and low manufacturing cost. These features, together with the need for only one power supply to bias the device, make InGaP/GaAs HBTs very attractive for reaching low phase noise of fully integrated VCOs [47].

On the other hand, the VCO performance is very sensitive to the variation of device characteristics and the reliability issues put the limit for its RF performance. With the smaller dimensions for improving speed and functionality of the InGaP/GaAs HBT, which dissipates large amount of power and results in heat flux accumulated in the junction, requires sophisticated thermal management for reliability.

Stress-induced base current instability is one of the major reliability issues for InGaP/GaAs HBTs, which is caused by the internal traps under high junction temperatures [6]. While several researchers have reported on the observed degradations of HBT characteristics under electrothermal stress [48-49], there has been little published data on the HBT behaviors under long-term electrothermal stress and the full understanding of stress-induced degradation of InGaP/GaAs HBT-based VCO is therefore subject to further research. If care is not taken to understand this issue, degradation paths can lead to built-in circuit failure during VCO field operations. Detection of this failure may be difficult due to the circuit complexity and lead to erroneous data or output conditions.

This work was the first attempt to characterize and analyze the effects of electrothermal stress on the RF characteristics of InGaP/GaAs HBT-based VCO. Transistor models obtained in Chapter 5 were used in ADS (state-of-art RFIC/MMIC simulator from Agilent Technologies) to examine VCO performances such as phase noise, tuning range and output amplitude, etc. Combined measured data and the simulated results with the extracted models, the stress-induced effects on the HBT-based VCO circuit performance were systematically evaluated.

6.4.2 2.4 GHz InGaP/GaAs HBT-based VCO

Many research efforts have been devoted to fully integrated VCOs in 0.8-2.5 GHz for mobile communication systems such as personal communications systems (PCSs), global systems for mobile communications (GSMs), wireless local area networks (WLANs). Therefore, a single-ended InGaP/GaAs HBT-based VCO designed for the IEEE 802.11g standard at the 2.4 GHz has

been chosen in our study to predict the stress-induced RF performance degradations. Figure 6.7 shows the proposed circuit topology of a negative-resistance oscillator.

In most VCOs, capacitive feedback topologies are used to generate negative-resistance, which can employ the merits of a VCO, such as high output voltage swing and high energy efficiency, as well as low common-mode noise. So in our design approach, the method of negative-resistance was implemented and the ADS MMIC simulator was used to optimize and simulate the performance of the designed VCO.

To achieve the required large tuning range of capacitance, an external varactor consisting of an RLC network was used. And the adjustable DC power supply V_{DC} was used to provide tuning voltage to control the oscillation frequency of the successive LC tank.

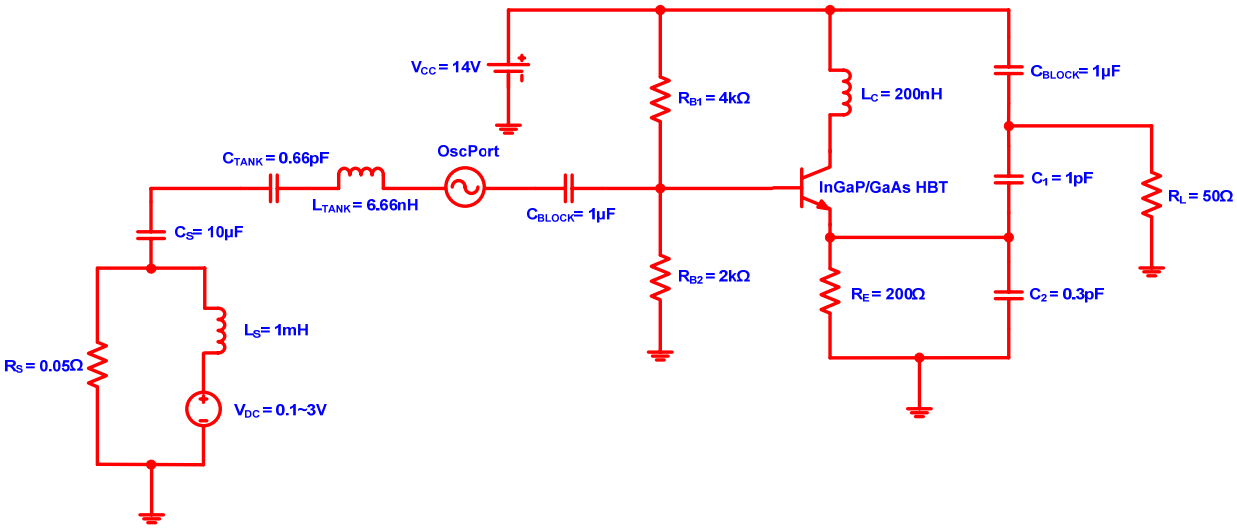


Figure 6.7 Detailed schematic of the monolithic InGaP/GaAs HBT-based VCO design.

To obtain the low phase noise performance, the optimizations of high Q-factor resonator and core current are the most important points in VCO design. As concerned with the LC tank, the on-chip inductor and capacitor form a resonator, therefore the Q-factor must be carefully considered. In our design approach, the Q-factor of the resonator was obtained at 100, which improves both phase noise and bandwidth performance. An oscillation port was added and placed such that it separated the negative-resistance portion of the VCO from the LC resonator.

To oscillate a VCO, the magnitude of the negative-resistance has to be equal or larger than that of the LC tank to compensate the loss of the tank. The negative-resistor can be realized easily by a three terminals active device with proper feedback to cancel out the loss from the LC resonator. Here, the InGaP/GaAs HBT is the suitable active device selected in our negative-resistance design to satisfy the oscillation conditions of the resonator.

The transistor was constructed as a CE capacitive feedback circuit to produce a negative-resistance. The DC bias of the core InGaP/GaAs HBT was provided by a voltage power supply V_{CC} connected to the collector and base terminals through RF choke L_C, and series resistors R_{B1} and R_{B2}. As the phase noise depends on the current passing through the VCO core [50], the bias point of the HBT has been optimized for low phase noise and the base voltage was adjusted to achieve a quiescent collector current of 15 mA.

An emitter degeneration resistor R_E was employed to stabilize the DC biasing of the VCO and is critical in providing matched RF performance, which ensures high-performance oscillator operation and improves the output power at the LC tank resonated frequency of 2.4 GHz.

The capacitive voltage divider composed of C_1 and C_2 was used to optimize the loop gain by maximizing the tank swing and the values were selected to deliver the maximum power to the load R_L.

All the components were designed to optimize the FOM of the VCO with the fresh device. The designed values of the circuit components are: V_{DC} = 0.1 V ~ 3.0 V, R_S = 0.05 Ω, L_S = 1 mH, C_S = 10 μF, C_{TANK} = 0.66 pF, L_{TANK} = 6.6 nH, C_{BLOCK} = 1 μF, R_{B1} = 4 KΩ, R_{B2} = 2 KΩ, R_E = 200 Ω, L_C = 200 nH, C_1 = 1 pF, C_2 = 0.3 pF and R_L = 50 Ω. The HBT bias voltage is V_{CC} = 14 V.

The VCO is primarily characterized by phase noise, tuning range and output power. By combining the negative-resistance and the resonator, all the RF characteristics of the VCO were systematically evaluated by Harmonic Balance (HB) simulation.

A. Phase Noise

Phase noise simulations include a non-linear large-signal model and HB simulation. Although these are available to predict the accurate phase noise, they are too complex to understand the VCO operations and phase noises. Thus, the linear phase noise model is a simple way to give

good insight into phase noises [51]. The linear phase noise physical model of HBT has three main noise sources:

I. The base resistance noise $\overline{v^2_{nb}} = 4kT \cdot r_b \cdot \Delta f$ (20)

II. The shot noise from collector current $\overline{i^2_{nc}} = 2q \cdot I_C \cdot \Delta f$ (21)

III. The shot noise from base current and flicker noise $\overline{i^2_{nb}} = 2q \cdot I_B \cdot \Delta f + K_1 \cdot \frac{I_B^{\alpha}}{f} \cdot \Delta f$ (22)

where I_B is the base current, I_C is the collector current, r_b is the base resistance, K_1 is the flicker noise factor and α is the flicker noise exponent. All the noises are independent of each other because they arise from spatially separated and independent physical mechanisms [52]. At the single-sideband carrier-to-phase-noise offset frequency of 1 MHz, the predicted phase noise changes due to the long-term eletrothermal stress effect are shown in Table 6.2 and the normalized phase noise degradation results as functions of cumulative stress time are shown in Figure 6.8. It is clear that the phase noise increased dramatically along with the high stress conditions and accumulated stress time. At the high junction temperature of 265 °C, the phase noise degradation shows the worst case with the normalized percentage shift of -35.94% after 2000-hour stress. We find that this may relate to the stress-induced device model degradation as the base resistance increased significantly, while the base current also shifted higher and collector current remained almost unchanged after stress. Thus, the post-stress base resistance noise $\overline{v^2_{nb}}$ and the shot noise from the base current and flicker noise $\overline{i^2_{nb}}$ both increased a lot, which made the overall post-stress phase noise increase, while the shot noise from the collector current was almost unchanged.

Table 6.2 Predicted phase noise changes @ 1 MHz offset frequency as a function of stress time.

Stress Time (Hour)	Phase Noise @ f_{off} = 1 MHz (dBc/Hz)		
	T_J=200 °C	T_J=245 °C	T_J=265 °C
0	-128.00	-128.00	-128.00
96	-126.00	-125.00	-121.00
240	-125.00	-123.00	-117.00
500	-121.00	-118.00	-104.00
1000	-113.00	-109.00	-96.00
2000	-105.00	-102.00	-82.00

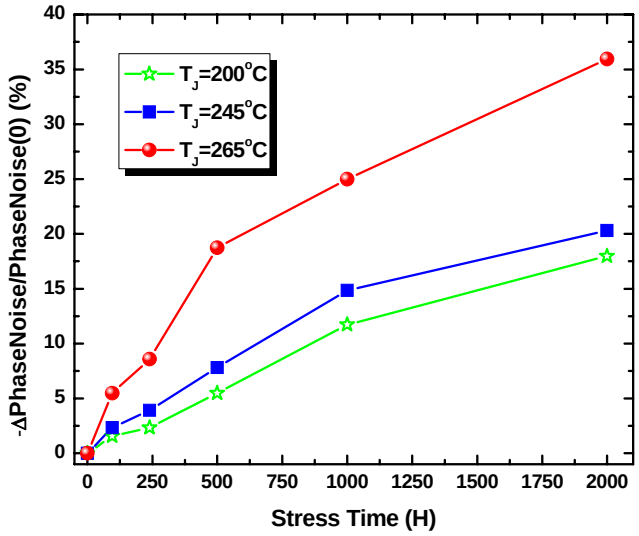


Figure 6.8 Simulated phase noise degradations vs. stress time.

B. Tuning Range

The optimized matching points of the VCO were altered after stress, which resulted in the degradation of the tuning range. The predicted tuning range shifts before and after stress are

shown in Table 6.3 and the normalized tuning range degradation as functions of the cumulative stress time are shown in Figure 6.9. It shows that the degradations of tuning range diminished slightly by only -9.48% after high electrothermal stress of 265 °C. Considering the long-term stress (2000 hours) and the significantly decreased VCO core device's DC characteristics, the tuning range degradation subject to the high junction temperature stress was inconsiderable. This phenomenon can be explained as the advantages of the external varactor with a large tuning range of capacitance, which provides more stable tuning performance compared to the traditional junction tuning capacitors of the VCO core device.

C. Output Power

The amplitude of the output power also diminished significantly shown in Table 6.4. After 2000-hour stress, the output power of the VCO decreased about 69.17%, 74.97% and 89.86% at high junction temperatures of 200 °C, 245 °C and 265 °C, respectively, shown in Figure 6.10. Again, this shows the long-term eletrothermal stress degrades the VCO performance dramatically.

Table 6.3 Predicted tuning range shifts as a function of stress time.

Stress Time (Hour)	**Tuning Range (MHz/V)**		
	T_J=200 °C	**T_J=245 °C**	**T_J=265 °C**
0	517.00	517.00	517.00
96	516.00	515.00	513.00
240	514.00	512.00	506.00
500	513.00	510.00	497.00
1000	509.00	507.00	485.00
2000	504.00	501.00	468.00

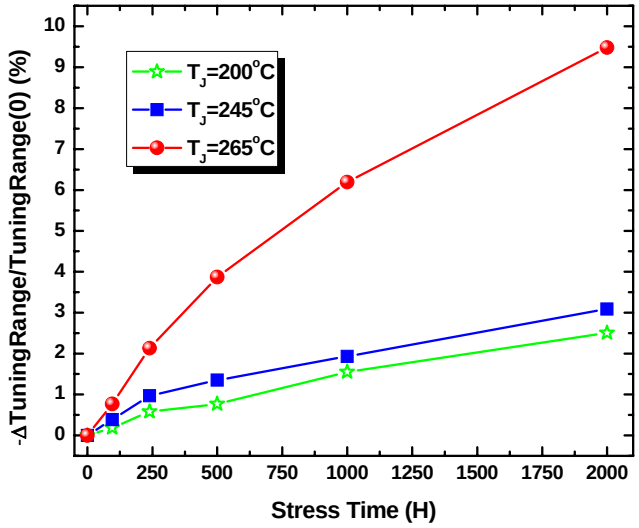


Figure 6.9 Simulated tuning range degradations vs. stress time.

Table 6.4 Predicted output power decreases as a function of stress time.

Stress Time (Hour)	Output Power (dBm)		
	T_J=200 °C	T_J=245 °C	T_J=265 °C
0	4.78	4.78	4.78
96	4.21	3.66	3.00
240	3.67	3.08	2.38
500	3.17	2.53	1.77
1000	2.18	2.00	1.05
2000	1.47	1.20	0.48

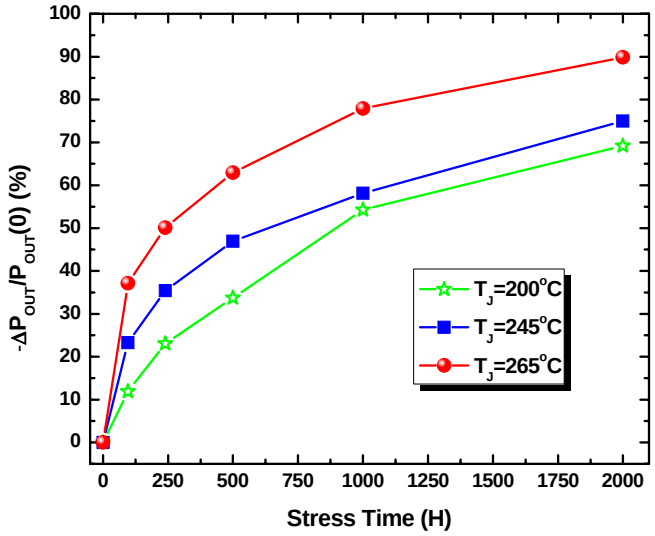


Figure 6.10 Simulated output power degradation vs. stress time.

D. Figure of Merit

The oscillator design entails considerations of phase noise, power consumption, oscillation frequency, tuning range, etc. Therefore, the FOM is a widely used definition for fair comparison of VCO performances at different frequencies and different power consumptions as follows [53]:

$$FOM = \Phi\left(f_{off}\right) - 20\log\left(\frac{f_{osc}}{f_{off}}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{23}$$

where $\Phi\left(f_{off}\right)$ is the phase noise at the offset frequency f_{off}, f_{osc} is the oscillation frequency, P_{diss} is the power dissipation in the VCO core. Although it does not include any information about the tuning range and output power, it gives good comparative insights into the VCO performances. The predicted FOM shifts before and after stress are shown in Table 6.5 and the

normalized FOM degradations as functions of the cumulative stress time are shown in Figure 6.11. After 2000-hour stress, the FOM of VCO decreased about 13.29%, 15.03% and 26.59% at the junction temperatures of 200 °C, 245 °C and 265 °C, respectively.

Table 6.5 Predicted FOM degradations as a function of stress time.

Stress Time (Hour)	FOM (dBc/Hz)		
	T_J=200 °C	T_J=245 °C	T_J=265 °C
0	-173.00	-173.00	-173.00
96	-171.00	-170.00	-166.00
240	-170.00	-168.00	-162.00
500	-166.00	-163.00	-149.00
1000	-158.00	-154.00	-141.00
2000	-150.00	-147.00	-127.00

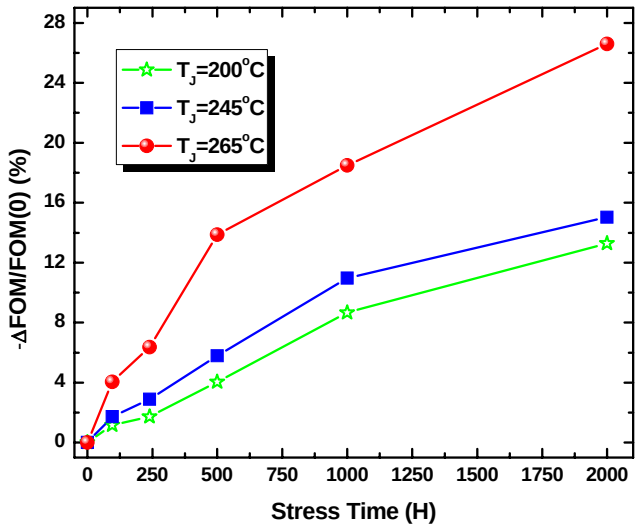


Figure 6.11 Simulated FOM degradations vs. stress time.

The VCO RF characteristics degradations affect the performance of the PLL, and then the whole receiver performance. For example, the increased phase noise degrades the selectivity of the receiver and the lowered tuning range and output power impact the locking time and stability of the receiver.

6.4.3 Conclusion

An integrated InGaP/GaAs HBT-based VCO with low phase noise performance was designed and evaluated for 2.4 GHz applications by Agilent ADS MMIC simulator. The post-stress phase noise, output power and FOM all degraded significantly, while the VCO tuning range showed very limited vulnerability with respect to electrothermal stress conditions. These results are very useful for MMIC designers to build more reliable HBT-based VCOs.

CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This study summarized the observed long-term electrothermal stress-induced performance degradations of InGaP/GaAs HBT MMIC technology. The significant changes in the post-stress device characteristics was the increased base current that resulted in a monotonic reduction in DC current gain. Both theoretical TCAD device simulations and experimental stress testing results have been obtained and evaluated. Good agreement between the measurement and simulation has verified the accuracy of the extracted fresh and stressed SGP models

The stress-induced circuit performance degradations of integrated 1.575 GHz InGaP/GaAs HBT-based RF PA, 2.4 GHz InGaP HBT-base LNA and monolithic 2.4 GHz VCO were systematically evaluated by Cadence SpectreRF and Agilent ADS MMIC simulation tools with the extracted pre- and post-stress transistor models. The post-stress power gain, PAE, linearity, NF and phase noise of InGaP/GaAs HBT-based MMICs have shown degradations in different significant degree with respect to the stress conditions. These results are very useful for RF/microwave industry to build more reliable HBT-based RF building blocks.

7.2 Future Work

The traditional characterization techniques used to study the reliability of InGaP/GaAs HBTs consist of applying static DC stresses or ramped electrical stresses. However, the high frequency dynamic stress-induced effects on the HBT MMIC technology are practical and important with the devices scaling down into sub-micron, as the MMICs are usually biased under time-varying conditions. Thus, it is worth studying the performance degradations of the DUT under dynamic stress. So far, these issues have not been studied systematically yet. One of the possible reasons is that it is really difficult to determine which parts of the system suffer from the stress-induced effects. It is also not practical to study the reliability issues when the high frequency stress is on the whole MMIC system. Therefore, the simulation methodology presents a suitable way to study these kinds of effects.

LIST OF REFERENCES

[1] Hafizi M. E., L. M. Pawlowicz, L. T. Tran, D. K. Umemoto, D. C. Streit, A. K. Oki et al., "Reliability Analysis of GaAs/AlGaAs HBT's Under Forward Current/Temperature Stress", Digest IEEE GaAs IC Symp., p. 329, 1990.

[2] C. Maneux, N. Labat, N. Saysset, A. Touboul, and T. Danto, "Experimental analysis and 2D simulation of AlGaAs/GaAs HBT base leakage current", Microelectronics and Reliability, vol. 37, p. 1707, 1997.

[3] J. J. Liou, C. I. Huang, B. Bayraktaroglu, D. C. Williamson, and K. B. Parab, "Base and collector leakage currents of AlGaAs/GaAs heterojunction bipolar transistors", Journal of Applied Physics, vol. 76, pp. 3187-3193, 1994.

[4] Y. H. Chang and G. P. Li, "Degradation mechanism of base current increase under forward current stress in AlGaAs/GaAs heterojunction bipolar transistors", Applied Physics Letter, vol. 66, pp. 2721-2723, 1995.

[5] J. J. Liou and C. I. Huang, "Base and collector currents of pre- and post-burn-in AlGaAs/GaAs heterojunction bipolar transistors", Solid-State Electronics, vol. 37, No. 7, pp. 1349-1352, 1994.

[6] A. Rezazadeh, et al., "Reliability investigation of InGaP/GaAs HBTs under current and temperature stress", Microelectronics and Reliability, vol. 39, pp. 1809-1816, 1999.

[7] H. K. Kroemer, "Hetero bipolar transistors and integrated circuits", Proc. IEEE, vol. 70, pp. 13-25, 1982.

[8] Juin J. Liou, "Principle and Analysis of AlGaAs/GaAs Heterojunction Bipolar Transistors", 1996.

[9] P. M. Asbeck et al., "Heterojunction bipolar transistors for microwave and millimeter-wave integrated circuits", IEEE Trans. Electron Devices, vol. ED-34, P. 1462, 1987.

[10] K. Nagata, O. Nakajima, Y. Yamauchi, and T. Ishibashi, "A new self-aligned structure AlGaAs/GaAs HBT for high speed digital circuits", in Proc. 12th Int. Symp. GaAs and Rel. Comp., Inst. Phys. Conf. Series, no. 79, 1986, pp 589-594.

[11] M. C. F. Chang et al., "AlGaAs/GaAs heterojunction bipolar transistors fabricated using a self-aligned dual-lift-off process", IEEE Electron Device Lett., vol. EDL-8, pp. 303-305, 1987.

[12] J. R. Hayes, F. Capasso, A. C. Gossard, R. J. Malik and W. Weigmann, "Bipolar transistor with graded bandgap base", Electron. Lett., vol. 19, p. 410, 1983.

[13] D. L. Miller, P. M. Asbeck, R. J. Anderson, and F. H. Eisen, "AlGaAs/GaAs heterojunction bipolar transistors with graded composition in the base", Electron. Lett., vol. 19, p. 367, 1983.

[14] J. Yoshida, M. Kurata, K. Morizuka and A. Hojo, "Emitter-base bandgap grading effects on GaAlAs/GaAs heterojunction bipolar transistor characteristics", IEEE Trans. Electron Devices, vol. ED-32, pp. 1714, 1985.

[15] M. Razeghi, F. Omnes, M. Defour, Ph. Maurel, J. Hu, D. Pavlidis, "High performance GaAs/GaInP HBTs grown by MOCVD", Sem. Sci. and Tec. vol. 5, pp. 278-280, 1990.

[16] J. W. Park, D. Pavlidis, S. Mohammadi, C. Dua, J. C. Garcia, "Improved High Frequency Performance by Composite Emitter AlGaAs/GaInP HBTs Fabricated using CBE", Proceedings of 24th Int. Sym. on Compund Semiconductor. San Diego, pp. 439-442, 1997.

[17] M. T. Fresina, D. A. Ahmari, P. J. Mares, Q. J. Hartmann, M. FENA, G. E. Stillman, "High-spped, low-noise InGaP/GaAs HBTs", IEEE Electrón Dev. Lett., vol. 16, pp. 540-541. Dec. 1995.

[18] S. Kobayashi, T. Fujita, T. Yakihara, S. Oka, A. Miura, "Ultrahigh-speed InGaP/AlGaAs/Ingaes HBTs using Mg as the base dopant", Proceedings of the IPRM, pp. 58-61, 1997.

[19] K. Mochizuki, K. Ouchi, K. Hirata, T. Tanoue, T. Oka, H. Masuda, "Polycrystal Isolation of InGaP/GaAs HBT's to reduce collector capacitance", IEEE Electron Dev. Lett., vol. 19, no. 2, pp. 47-49, Feb. 1998.

[20] T. Oka, K. Ouchi, H. Uchiyama, T. Taniguchi, K. Mochizuki, T. Nakamura, "High-speed InGaP/GaAs HBTs with buried SiO_2 using WSi as the base electrode", IEEE Electron Dev. Lett., vol. 18, no. 4, pp. 154-156, April, 1997.

[21] H. Blanck, K. J. Riepe, W. Doser, P. Auxemery and D. Pons, "Industrial InGaP/GaAs Power HBT MMIC Process", GaAs Symposium Digest, pp. 113-116, October 2000.

[22] N. LeGallou, J. Y. Touchais, J. F. Vilemazet, A. Darbandi, J. L. Cazaux, A. Mallet, and L. Lapierre, "High Efficiency 45W HPA for Space Application", 34th European Microwave Conference, Amsterdam, 2004.

[23] L. I. Liou et al., "Thermal stability analysis of multiple emitter AlGaAs/GaAs HBTs", MTTS-Symp. Dig., p. 281, 1993.

[24] W. Liu, S. Nelson, D. Hill and A. Khatibzadeh, "Current gain collapse in microwave multi-finger heterojunction bipolar transistors operated at very high power density", IEEE Trans. Electron Dev., vol. 40, pp. 1917-1927, 1993.

[25] W. Liu, "Handbook of III-V Heterojunction Bipolar Transistors", New York: Wiley, 1998.

[26] F. Alexandre, J. L. Benchimol, P. Launay, J. Dangla, and C. Dubon-Chevallier, "Modern epitaxial techniques for HBT structures", Solid-State Electron., vol. 38, pp. 1667-1674, Sept. 1995.

[27] T. S. Henderson and P. K. Ikalainen, "Reliability of self-aligned, ledge passivated 7.5 GHz GaAs/AlGaAs HBTs", in Proc. 1997 35th Annu. IEEE Int. Reliability Physics Symp., 1997.

[28] S. A. Ding, T. Fan, Z. Xu, and C. C. Hsu, "In-based metal ohmic contacts to n-GaAs", in Proc. MRS Symp., San Francisco, CA, 1994, pp. 404-408.

[29] H. Sugahara, J. Nagano, T. Nittono, and K. Ogawa, "Improved reliability of AlGaAs/GaAs heterojunction bipolar transistors with a strain-relaxed base", in Tech. Dig. GaAs IC Symp., 1993, pp. 115-118.

[30] C. Maneux et al., "Analysis of the surface base current drift in GaAs HBTs", in Proceedings of the 1996 7th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 96), 1996.

[31] J. A. Higgins, "Thermal properties of power HBTs", IEEE Trans. Electron Devices, vol. 40, pp. 2171-2177, Dec. 1993.

[32] E. Takeda and N. Suzuki, "An empirical model for device degradation due to hot carrier injection" IEEE Electron. Device Lett., vol. EDL-4, pp. 111-113, 1983.

[33] T. S. Henderson and T. S. Kim, "Improved reliability C/X-band monolithic power HBT amplifiers fabricated with low stress process", Proc. of GaAs IC symposium, pp. 27-30, 1996.

[34] P.Antognetti G. Massobrio, “Semiconductor Device Modeling with SPICE”, McGraw-Hill, 1988, ISBN 0-07-002107-4.

[35] S. Makioka, et al., “High Efficiency GaAs MCM Power Amplifier for 1.9GHz Digital Cordless Telephones”, IEEE Microwave and Millimeter Wave Monolithic Circuits Symposium, pp. 51-54, 1994.

[36] M. Nagaoka, et al., “High Efficiency Monolithic GaAs Power MESFET Amplifier Operating with a Single Low Voltage Supply for 1.9 GHz Digital Mobile Communication Applications”, IEEE MMT-S, pp. 577-580, 1994.

[37] E. Camargo and R. M. Steinberg, “A Compact High Power Amplifier for Handy Phones”, IEEE MMT-S, pp. 565-568, 1994.

[38] S-J. Maeng, et al., “A GaAs Power Amplifier for 3.3V CDMA/AMPS Dual-Mode Cellular Phones”, IEEE Transactions on Microwave Theory and Techniques, vol. 43, pp. 2839-2843, December 1995.

[39] T. Lee, “The design of CMOS radio-frequency integrated circuits”, Cambridge University Press, 1998.

[40] B. Klepser, M. Punzenberger, T. Ruhlicke and M. Zannoth, “5-GHz and 2.4-GHz dual-band RF-transceiver for WLAN 802.11 a/b/g applications”, 2003 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 37-40.

[41] G. Girlando and G. Palmisano, “Noise figure and impedance matching in RF cascode amplifiers”, IEEE Trans. Circuits and Systems-II Analog and Digital Signal Processing, pp. 1388-1396, November 1999.

[42] K. L. Fong, “High-frequency analysis of linearity improvement technique of common-emitter transconductance stage using a low-frequency-trap network”, IEEE J. Solid-State Circuits, pp. 1249-1252, Aug. 2000.

[43] A. van der Ziel, “Representation of noise in linear two ports”, Proc. IEEE, p. 1211, June 1969.

[44] S.-A. Yu, C.-C. Meng and S.-S. Lu, “A 5.7 GHz interpolative VCO using InGaP/GaAs HBT technology”, IEEE Microwave Wireless Components Lett., vol. 12, pp. 37-38, Feb. 2002.

[45] A. Boudiaf, M. Ahdjoudj, and P. Pouvil, “Low phase noise pHEMT-based MMIC VCO’s for LMDS applications”, IEEE MTT-S Dig., vol. 2, pp. 1559-1562, 2001.

[46] V. Schwarz, T. Morf, A. Huber, H. Jackel, and H. R. Benedickter, “Differential InP-HBT current controlled LC-oscillator with center frequencies of 43 and 67 GHz”, Electron. Lett., pp. 1197-1198, 1999.

[47] M.E. Kim, A.K. Oki, G.M. Gorman, D.K. Umemoto and J.B. Camou, “GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications”, IEEE Transactions on Microwave Theory and Techniques, vol. 37, pp. 1286-1303, 1989.

[48] T. Henderson, D. Hill, W. Liu, D. Costa, H.-F. Chau, T. Kim and A. Khatibzadeh, “Characterization of bias-stressed carbon-doped GaAs/AlGaAs power heterojunction bipolar transistors”, in IEDM Tech. Dig., pp. 187-190, 1994.

[49] T. Takahashi, S. Saga, A. Kawano, T. Iwai and T. Fujii, “High-reliability InGaP/GaAs HBT’s fabricated by self-aligned process”, in IEDM Tech. Dig., pp. 191-194, 1994.

[50] A. Kyranas and Y. Papananos, “A 5 GHz fully integrated VCO in a SiGe bipolar technology”, in Proc. ISCAS, pp. 193-196, 2000.

[51] B. Razavi, “A study of phase noise in CMOS oscillators”, IEEE J. Solid-State Circuits, vol. 31, pp. 331-343, Mar. 1996.

[52] R. Aparicio and A. Hajimiri, “A noise-shifting differential Colpitts VCO”, IEEE J. Solid-State Circuits, vol. 37, pp. 1728-1736, Dec. 2002.

[53] J.-O. Plouchart, H. Ainspan, M. Soyuer and A. Ruehli, “A fully-monolithic SiGe differential voltage-controlled oscillator for 5 GHz wireless applications”, in Proc. IEEE Radio Frequency IC Symp., pp. 57-60, 2000.