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Advanced Metrology and Diagnostic Loss Analytics for Crystalline Silicon Photovoltaics.

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ADVANCED METROLOGY AND DIAGNOSTIC LOSS ANALYTICS FOR CRYSTALLINE SILCION PHOTOVOLTAICS

by

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ABSTRACT

Characterization plays a key role in developing a comprehensive understanding of the structure and performance of photovoltaic devices. High quality characterization methods enable researchers to assess material choices and processing steps, ultimately giving way to improved device performance and reduced manufacturing costs. In this work, several aspects of advanced metrology for crystalline silicon photovoltaic are investigated including in-line applications for manufacturing, off-line applications for research and development, and module/system level applications to evaluate long-term reliability.

A frame work was developed to assess the cost and potential value of metrology within a manufacturing line. This framework has been published to an on-line calculator in an effort to provide the solar industry with an intuitive and transparent method of evaluating the economics of in-line metrology. One important use of metrology is in evaluating spatial non-uniformities, as localized defects in large area solar cells often reduce overall device performance. Techniques that probe spatial uniformity were explored and analysis algorithms were developed that provide insights regarding process non-uniformity and its impact on device performance. Finally, a comprehensive suite of module level characterization was developed to accurately evaluate performance and identify degradation mechanisms in field deployed photovoltaic modules. For each of these applications, case-studies were used to demonstrate the value of these techniques and to highlight potential use cases.

ACKNOWLEDGMENTS

This dissertation represents the culmination of a long, wonderful journey that has both humbled and inspired me along the way. I would not be where I am today were it not for all of the guidance, support and encouragement I have received from many people.

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Finally, I would like to thank my family for providing me with the foundation on which all of this was possible, and most importantly to AnnMarie who has been there to support me every step of the way.

"Anyone who has never made a mistake has never tried anything new." - Albert Einstein

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LIST OF SYMBOLS

Symbol	*Description (Common Units)*
A_{ARC}	*Absorption within Anti-Reflective Coating*
α	*Absorption Coefficient (cm^{-1})*
c	*Speed of Light (m/s)*
f_{metal}	*Metal Fraction of Cell Area*
f_{eff}	*Effective Shading Fraction*
h	*Plank's Constant*
I_{mp}	*Maximum Power Current (A)*
I_{sc}	*Short-Circuit Current (A)*
$I_{AM1.5}$	*Intensity of Standard Air Mass 1.5 Solar Spectrum (W/m^2)*
iV_{oc}	*Implied Open Circuit Voltage (mV)*
J_o	*Dark Saturation Current Density (mA/cm^2)*
J_{sc}	*Short Circuit Current Density (mA/cm^2)*
k	*Boltzmann's Constant*
$L_{d,base}$	*Diffusion Length in the Base (μm)*
$L_{d,emitter}$	*Diffusion Length in the Emitter (μm)*
$L_{d,eff}$	*Effective Diffusion Length (μm)*
L_{α}	*Absorption Length in Silicon (cm)*
P_{mp}	*Maximum Power Point (W)*
M	*Measurand*
η	*Efficiency (%)*
n	*Refractive Index*
q	*Charge of Electron (eV)*
R_{active}	*Reflectance of the Active Area of the Cell*
R_{ARC}	*Reflectance of the Anti-Reflective Coating*
R_{meas}	*Measured Reflectance*
R_{escape}	*Escape Reflectance*
R_{metal}	*Reflectance of Metallic Front Contact*
R_{series}	*Series Resistance (Ohm cm^2)*
R_{shunt}	*Shunt Resistance (Ohm)*
S_{front}	*Front Surface Recombination Velocity*
S_{rear}	*Rear Surface Recombination Velocity*
t	*Film Thickness (nm)*
τ	*Carrier Lifetime(μsec)*
V_{oc}	*Open-Circuit Voltage (mV)*
V_{mp}	*Maximum Power Voltage (mV)*
V_T	*Thermal Voltage*
W_d	*Dead-Layer Thickness (cm)*
λ	*Wavelength (nm)*
Φ_{ph}	*Incident Photon Flux ($cm^{-2} \cdot s^{-1}$)*

LIST OF ABBREVIATIONS

Abbreviation	*Description*
Al-BSF	*Aluminum Back Surface Field*
ARC	*Anti-Reflective Coating*
BSF	*Back Surface Field*
c-Si	*Crystalline Silicon*
EL	*Electroluminescence*
EQE	*External Quantum Efficiency*
FTIR	*Fourier Transform Infrared Spectroscopy*
IQE	*Internal Quantum Efficiency*
I-V	*Current-Voltage*
LCOE	*Leveled Cost of Energy*
LED	*Light Emitting Diode*
LID	*Light Induced Degradation*
NIR	*Near-Infrared*
O&M	*Operation and Maintenance*
PERC	*Passivated Emitter and Rear Cell*
PID	*Potential Induced Degradation*
PL	*Photoluminescence*
PV	*Photovoltaic*
SEM	*Scanning Electron Microscopy*
SNR	*Signal to Noise Ratio*
STC	*Standard Test Conditions*

CHAPTER 1: INTRODUCTION

1.1 Trends within the Energy Industry

Worldwide energy demand is expected to increase over the next several decades [1]. Even with significant advances in energy efficiency, the electrification of countries such as India and China will require the deployment of new energy generation capacity around the world. Because of the potential risks due to increased carbon dioxide in the atmosphere, the world is looking to carbon free alternatives for supplying this energy demand. With recent cost reductions in both wind and solar energy technologies, renewables are now considered a viable, cost competitive alternative to fossil fuels in many markets. In fact, in the United States more than half of all new electricity generation comes from renewable sources. Projections from the U.S. Energy Information Administration have solar and natural gas as the two dominant technologies that will be deployed for the coming decades [2].

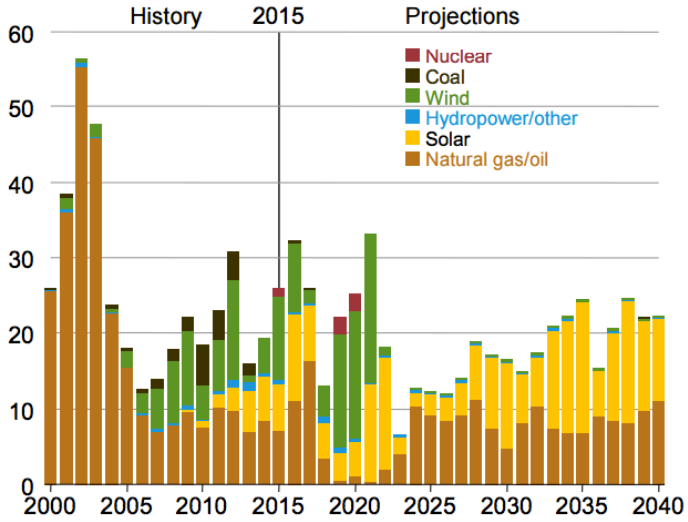


Figure 1. Historic and projected electricity generation capacity installations (in Gigawatts) in the U.S. by fuel type [2].

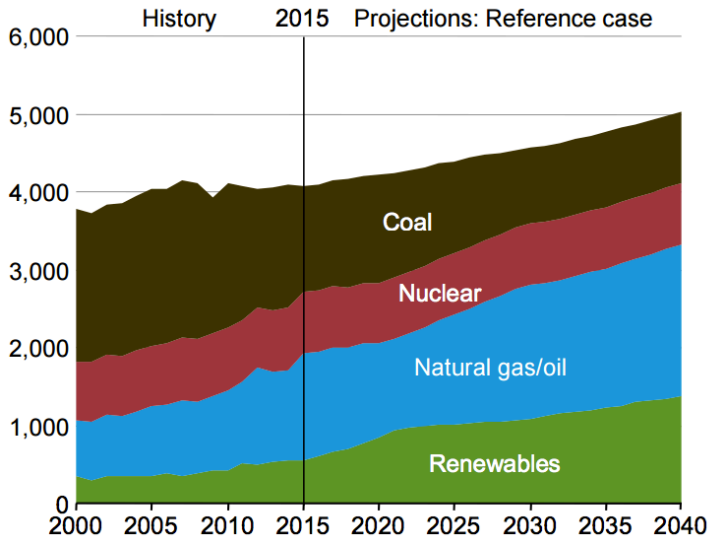


Figure 2. Cumulative electricity generation capacity (in billion kilowatthours) within the U.S. by fuel type [2].

This deployment of renewables is promising, but it is important to realize that existing generation capacity consists largely of coal, nuclear, and natural gas. In terms of cumulative generation capacity, renewables remain only a fraction of the total energy mix. Even though government policy, such as the enactment of the U.S. Clean Power Plan, may affect the rate of deployment, significant changes to these projections require further cost reductions for these technologies.

The price of renewable energy technologies, particularly photovoltaic (PV) technologies, have declined rapidly in the past decade. This has caught many international agencies off guard. For example, in 2004 the International Energy Agency predicted that renewables (excluding hydro) would account for only 4% of global electricity generation by 2030 [3]. Less than ten years later this 4% mark has been exceeded. Another example would be the U.S. Energy Information Administration projections provided each year in their Annual Energy Outlook report [4]. As seen

in Figure 3, estimates have greatly underestimated the rate of PV deployment in the U.S. for several consecutive years. The takeaway here is that large shifts in the economics of specific technologies can change the global outlook in extraordinary ways.

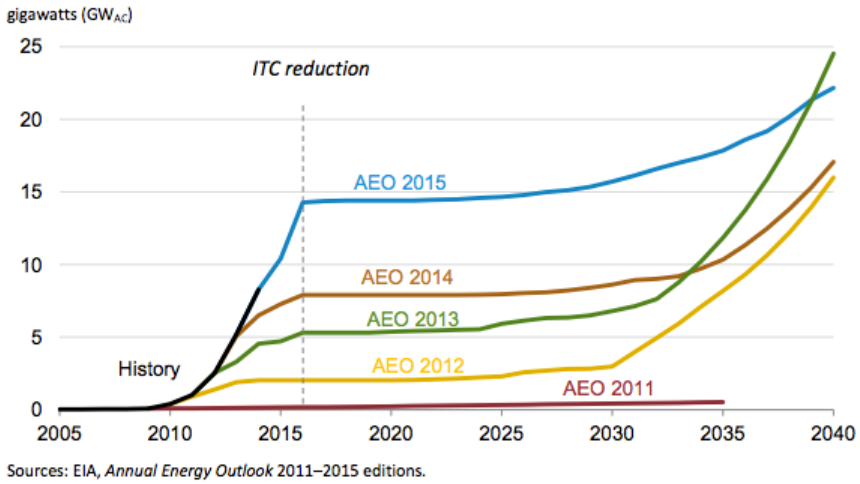


Figure 3. Utility-Scale solar PV capacity projections (in gigawatts) from the Annual Energy Outlook 2011 to 2015 [4].

1.2 Photovoltaic Energy

1.2.1 Brief History

Photovoltaic solar cells were first explored in the mid-20th century, with the world's first crystalline Silicon (c-Si) based solar cell developed in 1954 at Bell Laboratories [5]. Space applications quickly became a major market for these devices. In 1958, the Vanguard I became the first satellite to utilize PV cells to power its radio communications. To this day, PV cells continues to be the go-to energy source for space applications. This early market allowed for developments to continue, however the high costs remained prohibitive for many terrestrial

applications. Slowly, efficiency of these devices continued to increase while prices continued to decline.

During the 1970's and 80's deployment of flat-plate PV systems became a reality. c-Si became the dominant technology for terrestrial applications, however higher efficiency alternatives including Gallium Arsenide (GaAs) and multijunction cells took over the space industry. As costs continued to decline for PV, new applications emerged. For remote locations where it was expensive or impossible to connect to the grid, PV became a viable alternative. In terms of solar resource, the amount of energy incident on our planet in one year is ~7000 times more than the current global energy demand [6]. Because of the tremendous potential, harnessing the power of the sun to meet the electricity demands of the world remained a dream for many. Until recently, this was only a dream. Today, after 50 years of innovation, PV is now a cost competitive alternative to traditional fossil fuel sources.

The cost of PV has been declining continuously for many years. When the module sale price is plotted against the cumulative module production on a log-log scale, as shown in Figure 4, a linear trend is observed. Here you can see early modules prices above 20 $/W and where prices stand today at about 0.55 $/W. It is important to note that this represents only the module cost, and does not represent the true cost of energy, or the levelized cost of electricity (LCOE). The LCOE depends on many factors including the system configuration and geographic location. This variability is what ultimately determines the local economics of PV deployment [7]. Either way, module costs continue to decline as manufacturing improves and capacity expands. More importantly, there is no reason to believe this trend will not continue well into the future.

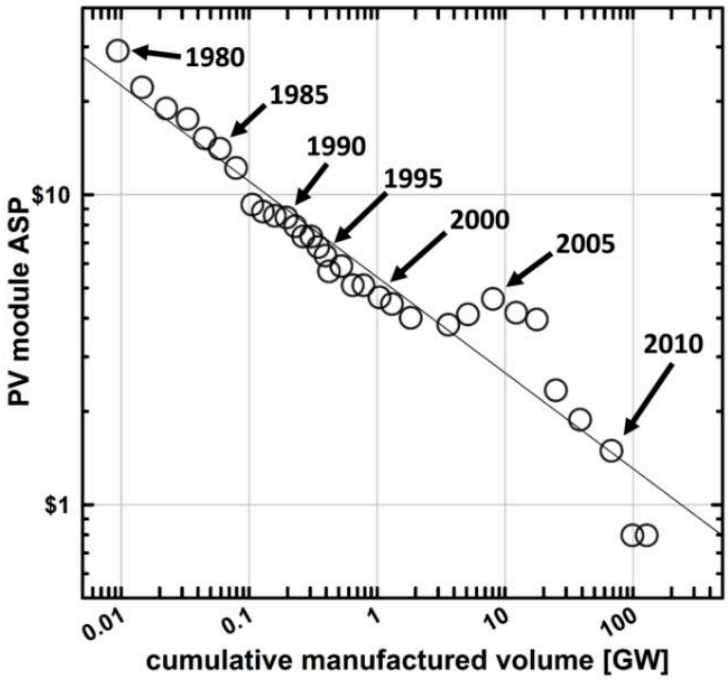


Figure 4. PV module manufacturing cost learning curve.

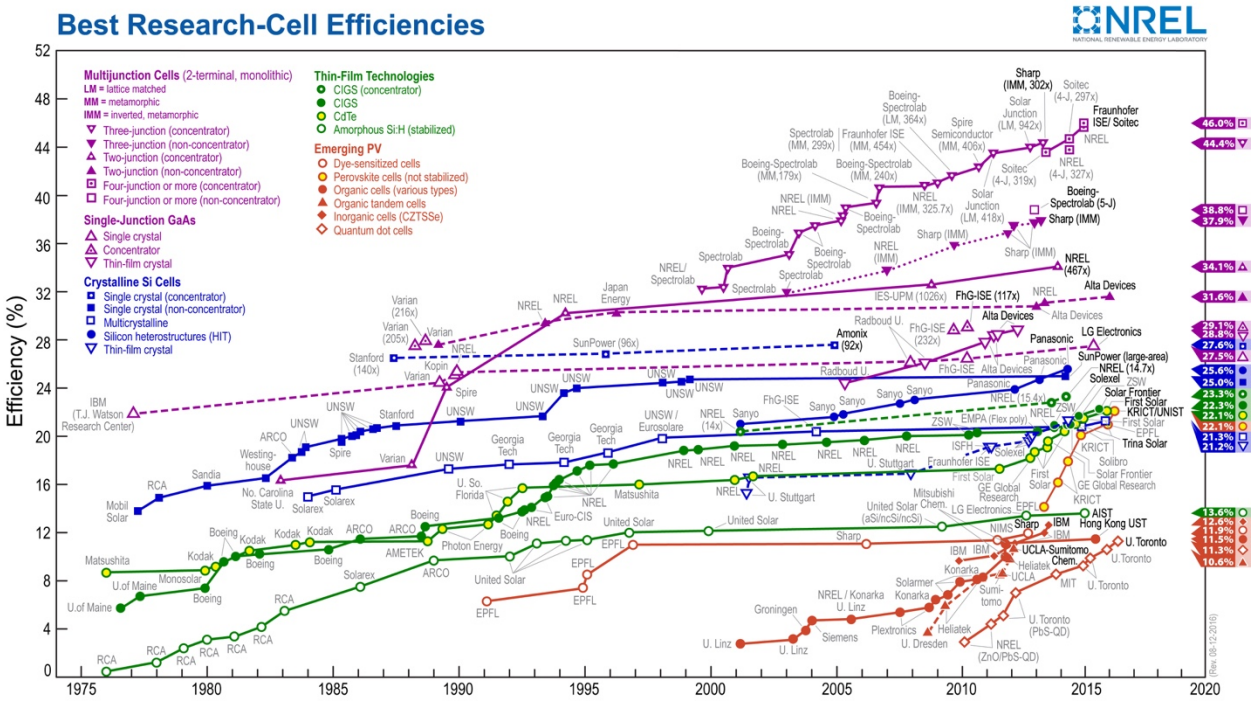


Figure 5. Record efficiencies for various PV technologies over time.

1.2.2 Conversion Technologies

In an effort to reduce cost and improve efficiency, a wide range of PV technologies have been explored over the years. Figure 5 shows the record efficiencies for all technologies that have been pursued. Interestingly one of the first materials investigated, c-Si, continues to be the dominant PV technology today [8]. Silicon was viewed as less than ideal choice for many decades because it was an indirect band-gap material and required expensive purification and crystal growth methods.

Standard single junction PV devices rely on a semiconductor material that has a band-gap in the range of 1.0-1.75 eV. Direct band-gap semiconductors have the advantage of strong optical absorption, and can therefore be much thinner than c-Si cells. As an alternative to c-Si, thin-film technologies were developed in an attempt to reduce manufacturing costs. Here the cells would be directly deposited on to glass substrates, eliminating the costly crystal growth process inherent to c-Si. Successful candidates included hydrogenated amorphous-Silicon (a-Si:H), Cadmium Telluride (CdTe), and Copper Indium Gallium DiSelenide (CIGS) and required only a few microns of material. Because these devices are fabricated using chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques the resulting thin-film was either polycrystalline or amorphous. The presence of crystal defects (*e.g.* grain boundaries) often lead to lower efficiencies than monocrystalline Silicon devices. The greatly reduced manufacturing cost were expected to outweigh these efficiency penalties. Unfortunately, only a few companies have successfully scaled up production using these thin-film technologies, accounting for only a small percentage of PV installations overall. It should be noted that at the cell level, CdTe and CIGS have achieved efficiencies at or above those achieved with multicrystalline Silicon devices as

shown in Figure 5. Many of these technologies have also been fabricated on flexible substrates, opening up unique applications in niche markets.

The highest single-junction device efficiency has been achieved using GaAs. The current record sits at 27.6% under 1-sun illumination. To push the limits even further, multijunction devices have been developed that consist of multiple PV cells stacked on top of each other (*i.e.* in tandem). The spectral response of each cell is tuned to capture a unique region of the spectrum maximizing the amount of light that can be collected. These devices are also designed with III-V semiconductors. Here, the record efficiencies have been push up to 38.8% for 1-sun conditions and up to 46.0% under concentration. An amazing feat of science and engineering, however the cost remains extremely high. This is due to the expensive substrates and low throughput epitaxial growth techniques. The use of concentrated light has been the most attractive approach to reduce LCOE cost for these devices. An optical concentrator, typically a Fresnel lens, is used to focus a large area of sunlight onto a small area device. This reduces the amount of active area (*i.e.* PV cell area) that is required. Only direct sunlight can be concentrated, so tracking is required to follow the sun throughout the day. These systems are considerably more complex than standard flat-plate fixed-tilt solar arrays and have yet to compete on a large scale. In space applications, where cost is of less concern, these III-V devices are the standard.

Finally, organic PV devices have been explored as an extremely lost cost alternative. Efficiencies have remained low for these type of devices that employ organic polymers as the active absorber layers. In recent years, perovskite based cells, a type of organic/inorganic blend have reached efficiencies up to 22.1%. When examining the efficiencies in Figure 5, the rise in efficiencies of these perovskite devices is unprecedented. In just a few years these devices have

made significant improvements in performance. Concerns related to the stability of these materials remain the largest challenge for these technologies if they are going to be commercialized.

1.2.3 Economic Driving Forces

Evaluating the cost of solar energy requires an understanding of several key metrics. These can be broken down into to two areas; (1) cost considerations and (2) performance.

Performance of PV is generally defined in terms of conversion efficiency (η) under what is known as standard test conditions (STC). These conditions refer to an irradiance of 1000 W/m2 using the standard air-mass 1.5 solar spectrum ($I_{AM1.5}$) with the cell at 25 degrees Celsius. These conditions are what determined the efficiencies presented in Figure 5 (excluding concentration results). The 1000W/m^2 value is referred to as 1-Sun conditions throughout this work. This standard provides the industry with a clear method to define the performance of a particular solar cell or module. Efficiency is calculated from Eq. (1) using the peak output power (P_{mp}), the input irradiance, and the cell area (A).

$$\eta = \frac{P_{mp}}{I_{AM1.5} * A} \qquad (1)$$

A simple cost metric can be determined from the measured power at STC and the manufacturing costs according to Eq. (2). This cost per watt peak ($\$/W_p$), allows for simple cost comparison of various PV technologies. Notice how power, as opposed to conversion efficiency, is the critical factor. Here, even a low efficiency technology can be competitive if manufactured at sufficiently low costs.

$$Cost\ per\ Watt\ Peak = \frac{Cost\ of\ Manufacturing}{Performance\ at\ STC} \quad (2)$$

This simple cost metric, although useful, does not necessarily provide information on the cost of energy in terms of dollars per kilowatthours (*$/kWh*). This more complete metric, defined as the levelized cost of electricity (LCOE), is needed to compare costs against traditional energy source like fossil fuels. There are many factors that influence this metric, making it harder to accurately determine. The LCOE is defined in Eq. (3).

$$Levelized\ Cost\ of\ Electricity = \frac{Total\ Lifecycle\ Cost}{Total\ Lifetime\ Energy\ Production} \quad (3)$$

To determine the total lifetime energy production, much more than performance at STC is required [9]. This requires the quantification of several factor that are both technology specific and system/site specific. At a given site the amount of energy produced is dependent on the array orientation, the tilt angle, potential shading, and the regional climate conditions such as the temperature and irradiance profile. A simple observation of field deployed systems will show that STC conditions (1000 W/m^2, 25°C) rarely exist. In fact, when the intensity of the sun is at its maximum, module temperatures can exceed 50°C. Alternatively, most of the useful daylight hours have intensities well below 1000 W/m^2, with the angle of incidence varying over a wide range. These factor depend significantly on the geographic location. These consideration underscore how limited efficiency measurements at STC are at describing the full story.

Measurements of efficiency over a wide range of temperatures and irradiance conditions are needed to provide a more comprehensive evaluation of performance.

The total lifetime cost of the system is also influenced by a wide variety of factors. Here, the cost can be broken down into two aspects; (1) upfront costs and (2) operation and maintenance (O&M). Upfront costs include standard items like the cost of components (*e.g.* modules, racking, inverters) and the cost of labor for installation. There are other factors, particularly for large scale systems, like the cost of capital and interconnection fees that also must be accounted for. Once the system is operational, the ongoing cost are referred to as O&M costs. This refers to regular trimming of vegetation, repair work, and in some cases module cleaning.

Finally, after considering all of these factors, there is still one more critical aspect impacting LCOE. This factor is the lifetime of the system. For PV modules, manufacturers regularly provide warranties up to 25 years. This is often assumed to be the system lifetime, however, this is not necessarily determined from empirical data. This is of great importance. Consider if the lifetime of the system was doubled from 25 to 50 years. This could cut the overall LCOE in half. This has sparked tremendous interest from investors, as the reliability of the system is potentially the most important factor influencing LCOE. Electronic components such as transformers and inverters can be replaced, but a field of several thousand failed modules presents a much larger risk.

Reliability of PV modules has been an active area of study since the first systems were deployed in the 1970's [10, 11]. The only true way to test reliability is to deploy the system and monitor the results. Unfortunately, to verify a 25-year lifetime, one would have to wait 25 years. Although some systems do exist that have been deployed for a considerable amount of time [12],

a method to evaluate new materials and technologies is required. To evaluate module reliability, modules are exposed to environmental stresses at an accelerated rate within a laboratory [13]. A qualification standard has been developed to replicate several real-world stressors within a time frame of only a few months. These accelerated aging tests provide some level of confidence that modules will not fail prematurely in the field, however, these test do not provide quantitative details on the module lifetime. Since these qualification test do not characterize long-term wear out mechanisms, they are unable to quantify the rate of module degradation. Module degradation rates are a critical factor in evaluating how the system will perform over time. Lastly, even if a particular module design is effective in ensuring a long operational lifetime, poor quality management within the manufacturing environment could result in unexpected field failures, undermining the success of the initial module design.

When you go back and consider the dollar per watt assessment, it is evident that this metric is often inadequate in accurately capturing the cost of energy from PV. As manufacturers continue on the downward trend of reducing manufacturing costs, it is essential that the integrity of the module is not compromised. Although new technologies may present themselves as cheaper alternatives based of STC measurements, it may in fact be the long-term performance that determines LCOE. This may, in part, provide an explanation as to why c-Si is the dominant PV technology today. Large scale investment requires confidence on the part of the investor and with the long, successful track record of c-Si modules, it has been difficult for other technologies to compete.

1.3 Motivation

Although photovoltaic solar energy systems have become a viable energy source in many markets, more work is required. Further reductions in cost will accelerate the rate of deployment which would have tremendous implications on the use of energy around the world. Although research work continues in an effort to identify new materials and to develop new cell architectures, c-Si based solar cells are having an impact in today's world. From this perspective, research focused on incremental improvements on existing c-Si technologies would be the most effective route to impact the economics of solar energy in the near term.

This work intends to identify how advanced metrology can be used to improve the economics of PV, focusing on several unique aspects of the cost structure. Within manufacturing, in-line metrology strategies are investigated to establish methods that could improve manufacturing yield and production line efficiencies. To assist research and development teams, spatially resolved cell analysis methods are developed to identify process non-uniformities and quantify their impact on cell performance. Finally, at the module level, a systematic loss analysis is presented that can be used to quantify various aspects of module reliability. In the never ending quest to reduce manufacturing cost and improve device performance, this work aims to provide the PV industry with innovative metrology solutions that can assist in achieving this goal.

CHAPTER 2: OVERVIEW OF CRYSTALLINE SILICON PHOTOVOLTAICS

2.1 Photovoltaic Cells

2.1.1 Device Operation

The fundamental operation of a photovoltaic (PV) cell it to convert incident light into usable power. In a semiconductor, photons with an energy greater than or equal to the band gap energy (E_g) can be absorbed by an electron, pushing it from valence band to the conduction band. The rate, and depth, at which this absorption occurs is a described by the absorption coefficient (α), or alternatively the absorption length (L_α), which varies as a function of wavelength. Fundamentally, as the photon energy increases beyond E_g, electrons deeper within the valence band can be excited, increasing the probability of absorption. This means that shorter wavelengths will be absorbed closer to the surface as compared to longer wavelengths.

Once carriers are generated, these carriers need to be extracted from the device to generate electricity. To achieve this, a *p*-*n* junction is used. This junction generates an internal electric field, sweeping carriers across the junction. Once across the junction, metal contacts are required to extract carriers from the device. On the front side, a metal grid is required to allow for both illumination and conduction.

To increase the amount of carriers generated within the device, it is important to minimize reflection. This is achieved through the use of surface texture and anti-reflective coatings (ARC). Surface texture refers to geometrical structures that increase the probability of reflected light hitting the surface more than once. An ARC is a thin dielectric layer intended to cause destructive interference of the incoming optical wave maximizing light transmission into the device. For standard silicon devices, Silicon Nitride (SiN_x) is used with a thickness of about

75nm. These two methods reduce reflection considerably when compared to a planar silicon surface.

Because of the indirect band gap of silicon, absorption of photons is weak near the band edge. This requires the use of a relatively thick (~200μm) device in order to ensure maximum absorption. Surface texture has the added advantage of directing light at an angle through the device allowing it to cover more distance before reaching the rear surface. The distance at which light travels through the device is described as the optical path length. The optical path length can be further enhanced by designing a highly reflective back surface to allow light to pass through the cell a second time. An optimal rear reflector would be a Lambertian rear surface where reflected light is randomized, increasing the occurrence of total internal reflection.

Once carriers are generated within the device, they need to make their way to the junction in order to be extracted. Transport to the junction relies on carrier diffusion. One important metric for solar cells is the minority carrier diffusion length (L_d). This refers to the average distance a carrier travels before a recombination event occurs. Alternatively, this could be describe in terms of the carrier lifetime (τ), as in the average time it takes for a generated carrier to recombine. The lifetime is defined by Eq. (4) using the excess carrier density (Δn), also referred to as the injection level, and the total recombination rate (U). The longer the carrier lifetime, or diffusion length, the more likely a carrier will find its way to the junction.

$$\tau = \frac{\Delta n}{U} \qquad (4)$$

Minimizing recombination is essential for high quality c-Si devices. Recombination can occur both in the volume of the semiconductor and at the surfaces. There are three main mechanisms for recombination which include radiative recombination, Auger recombination and Shockley Read Hall (SRH) recombination. Because of the indirect band gap in silicon, radiative recombination rates are relatively low. This recombination is critical, however, and will be discussed in subsequent chapters in the context of luminescence imaging.

SRH recombination refers to any defect that creates an energy level within the band gap of the material. Carriers encounter these defects and become “trapped” in this lower energy state. The carrier will stay there until it is thermally excited back into the conduction band or an oppositely charge carrier causes recombination. Here the closer the energy level is to the middle of the band gap, the more detrimental this defect is. A defect with an energy level closer to the band edge will allow the carrier back into the conduction band more easily, reducing the rate of recombination at that site. SRH recombination occurs at any point in which the crystal lattice is disturbed. This can be point defects, dislocations, grain boundaries and surfaces. A large part of c-Si cell device research revolves around eliminating or passivating these defects.

Auger recombination is an inherent mechanism within any semiconductor. Auger recombination relies on the interaction of a third charge carrier. In this case the energy released from the recombination process is transferred to the third carrier. That energy is eventually released back to the lattice through thermal relaxation. This process cannot be avoided and therefore represents the absolute upper limit for carrier lifetimes. This process, which relies on the presence of a third carrier, increases with increasing excess carrier density.

The effective carrier lifetime (τ_{eff}) is a combination of all of these factors and is the focus of many studies in this field. The carrier lifetime can be determined through a number of techniques including photoluminescence, microwave photoconductance and quantum efficiency measurements. The most widely used technique is quasi-steady-state photoconductance measurements [14, 15]. For this technique a wafer, generally with surface passivation, is exposed to illumination and the wafer conductivity, which relates directly to the excess carrier density, is measured. Under steady state conditions the generation of carriers must balance with the recombination of carriers, allowing the use of Eq. (4) to calculate the effective lifetime.

Another way to refer to recombination is to think in terms of dark-saturation currents. This approach relates directly to the current-voltage characteristics of the cell and is described in the following section.

2.1.2 Diode Equations

The basic structure of a solar cell involves the presence of a semiconductor diode created from the interaction between a *p*-type and *n*-type material. This junction creates an in-built electric field and the Current-Voltage (*I*-*V*) behavior is described using the Shockley's ideal diode equation [16].

$$I = I_0 \left[exp\left(\frac{V}{V_T}\right) - 1 \right] \quad (5)$$

$$V_T = \frac{kT}{q} \quad (6)$$

Here, I_0 is known as the dark-saturation current and V_T represents the thermal voltage define in Eq. (6) using the Boltzmann's constant k, the temperature T, and the electron charge q. The magnitude of I_0 under thermal equilibrium is equivalent to the recombination current. This parameter, often represented in terms of current density (J_0), is commonly referred to as the recombination parameter [17]. Recombination current in this equation generally refers to SRH recombination. Under illumination, carriers are generated within the device and contribute to the diffusion current of the device. A light generated current component (I_L) can then be added to Eq. (5).

$$I = I_L - I_0 \left[exp\left(\frac{V}{V_T}\right) - 1 \right] \quad (7)$$

This equation represents the ideal equation for a single *p-n* junction under illumination. Deviations from this ideal equation are due to the presence of finite series resistance (R_s), shunt resistance (R_{sh}) and recombination mechanisms other than SRH. Series resistance is introduced as charge carriers are extracted from the device from metal contacts on both the front and rear surface. Shunt resistance represents current flow, or leakage, through alternative paths within the device. These resistive effects are accounted for in Eq. (8).

$$I = I_L - I_0 \, exp\left(\frac{V+IR_S}{V_T}\right) + \frac{V+IR_S}{R_{sh}} \quad (8)$$

To account for non-ideal behavior, it is common to incorporate addition parameters. To account for recombination due to mechanisms other than bulk SRH, a second diode is often incorporated into this device. In this case I_{01} and I_{02} represent the saturation current for specific recombination mechanisms. An ideality factor is often incorporated as a method to describe which mechanisms is being accounted for. Standard bulk SRH recombination would have an ideality factor of 1. Other mechanism, such as edge or surface recombination, have been associated with ideality factors up to 2. A two diode model including ideality factors (m_1 and m_2) and resistive effects is expressed in Eq. (9).

$$I = I_L - I_{01}\left[exp\left(\frac{V+IR_S}{m_1 V_T}\right) - 1\right] - I_{02}\left[exp\left(\frac{V+IR_S}{m_2 V_T}\right) - 1\right] + \frac{V+IR_S}{R_{sh}} \quad (9)$$

The ideal diode equation described in this work are useful in understanding how basic device mechanisms, such as resistance and recombination impact device performance. Often these models are fit to experimental data in order to extract relevant device parameters.

2.1.3 I-V Characteristics

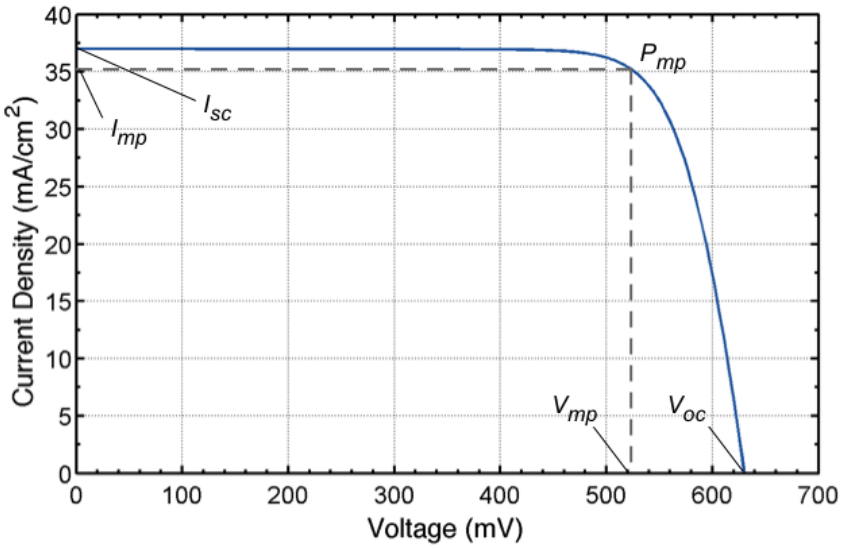


Figure 6. Example J-V characteristics representative of conventional c-Si device performance.

Current-Voltage measurements are performed to characterize the performance of the solar cell. As mentioned in the first chapter, the *official* efficiency of a solar cell is determined from illuminated *I-V* measurements using standard test conditions (1000 W/m^2, 25°C). A typical *I-V* curve is shown in Figure 6. There are several key parameters determined from these *I-V* characteristics including the short circuit current (I_{sc}), the open circuit voltage(V_{oc}), the maximum power point (P_{mp}), the current at maximum power (I_{mp}) and the voltage at maximum power (V_{mp}). Each of these parameters are shown in Figure 6. Current is often normalized for area, defined in term of current density (*J*), in order to compare devices of different area.

The fill factor (*FF*) is another common metric that describes the "squareness" of the *I-V* curve. The fill factor is influenced largely by non-ideal resistive and recombination affects. Record efficiency c-Si devices have achieved fill factors above 80%. The fill factor is calculated from Eq. (10)

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \qquad (10)$$

These parameters all relate to the fundamental mechanisms governing device performance. When performance is near ideal, experimentally measured I-V characteristic can be described quite well using the ideal diode equations in the previous section. Deviations are a result of various loss mechanisms. These loss mechanisms are often defined as either optical, resistive, or recombination related. Understanding these various loss mechanism, and being able to quantify them, is critical for improving device performance.

2.2 Cell Design

2.2.1 Conventional Cell Designs

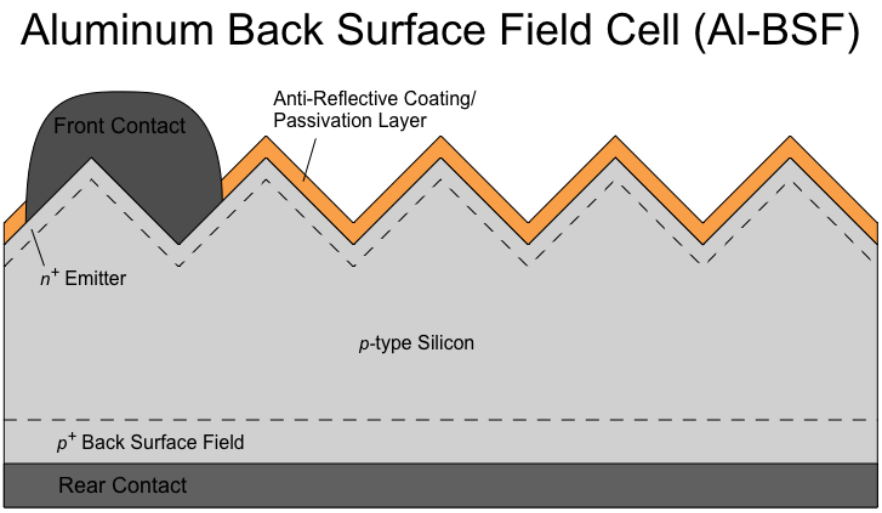


Figure 7. Figure of Al-BSF cell architecture

The most common cell architecture is the Aluminum back surface field (Al-BSF) design. This design has been the industry standard for several decades. This device, as shown in Figure

7, utilizes *p*-type Silicon, either monocrystalline or multicrystalline, as the base and a thin phosphorus doped *n*-type region as the emitter. SiN_x behaves both as an ARC and a passivating film for the emitter and is has a thickness of typically 75nm. During metallization, Aluminum is incorporated within the Silicon to form a highly doped p^+ region at the rear surface. This doped region shields majority carriers, in this case holes, from the surface helping to reduce surface recombination in this area and is referred to as the back surface field (BSF). This device typically achieves efficiencies between 16-19% in production. The lower end refers to multicrystalline wafers, with higher efficiencies possible for devices fabricated from monocrystalline wafers.

The conversion of incoming p-type c-Si wafers into Al-BSF cells can be divided into four primary process areas: (1) wet chemical processes; (2) emitter formation (*e.g.* P diffusion); (3) ARC/passivation deposition; and (4) metallization. The process flow for cell manufacturing is depicted in Figure 7. Several wet chemical processes are carried out after wafer production including post-wafering cleaning (*i.e.* saw damage removal) and texturing, and after emitter formation including edge isolation and phosphosilicate glass (PSG) removal. The emitter is typically formed through a high temperature diffusion of phosphorus into the crystal lattice. The SiN_x ARC/passivation layer is then deposited by plasma-enhanced chemical vapor deposition (PECVD). Finally, contacts are formed through the screen-printing and co-firing process. Typically, Ag is used for the front contact and Al is used as the rear contact. To ensure efficient extraction of photogenerated carriers, metallization must provide good electrical contact with low interfacial recombination velocity between the silicon wafer and metal contacts. Because the Ag paste is printed on top of the SiN_x, additives are included within the paste to allow the paste to eat through the ARC during firing and make good contact with emitter.

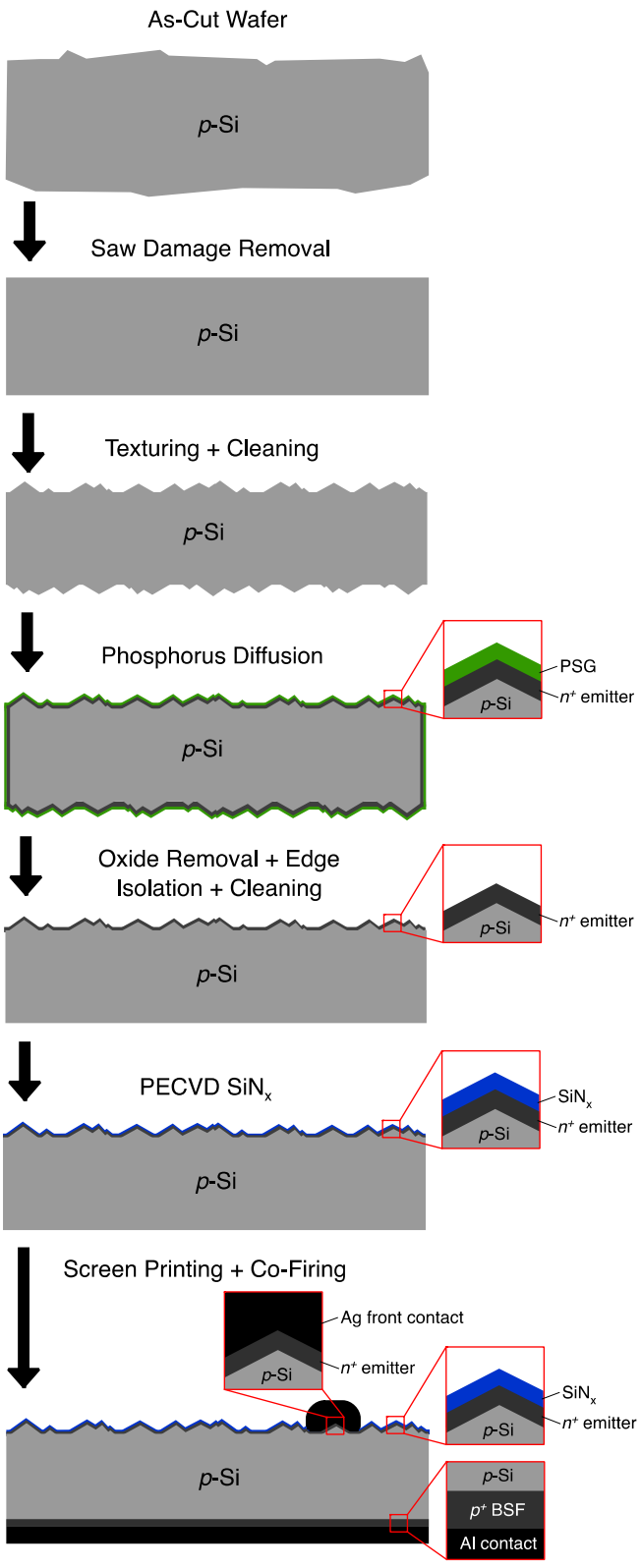


Figure 8. Process Flow for a standard Al-BSF solar cell.

2.2.2 Advanced Cell Designs

To increase the efficiency of c-Si devices a number of techniques have been established. The first and most important consideration is the starting wafer quality. Controlling the number of crystallographic defects, limiting the concentration of metal impurities, and optimizing the background doping densities (*i.e.* wafer resistivity) are critical for establishing high quality devices. Czochralzki (CZ) crystal growth methods have generally been the most cost effective route to produce *p*-type silicon ingots. As an alternative to CZ, multicrystalline ingot growth has been explored as a method to reduce cost while maintaining sufficient quality. Recent efforts have shown that efficiencies of 20.8% can be achieved through improved defect engineering of the starting multicrystalline ingot [18]. Alternatively, there are high cost crystal growth methods, such as float-zone processes that enable extremely pure and very low resistivity wafers. Often, n-type wafers are fabricated from these processes.

After optimizing the wafer quality, the next logical path to efficiency improvements is through reducing the surface, or interface, recombination. The rear surface BSF in conventional cells limits recombination by shielding majority carriers. Because both an electron and hole is required for recombination to take place, limiting the concentration of one carrier reduces the overall recombination rate. Another, more direct, route to reduce surface recombination is through chemical passivation which can actually reduce the concentration of defects at an interface. Many cell designs involve the use of a rear passivating film to reduce recombination at this interface, in turn increasing the V_{oc} of the cell. The most prominent example is the passivated emitter and rear cell (PERC). Here a dielectric film, typically Aluminum Oxide (Al_2O_3), is deposited

on the rear surface and local openings are made to allow the conduction to the Al back contact. This device design is shown in Figure 9.

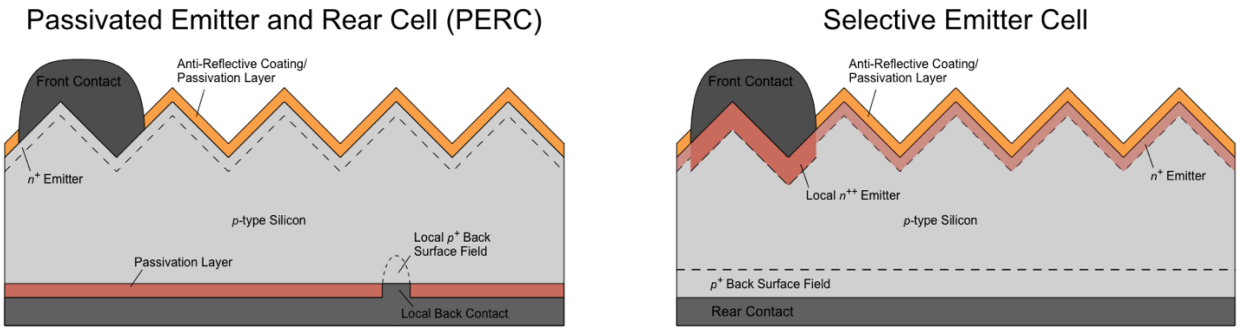


Figure 9. Design for a PERC cell (left) and a selective emitter cell (right).

Another method to reduce recombination is to modify the emitter of the device. Typical emitter design requires a trade off in terms of contact resistivity and SRH recombination, both of which increase with higher doping concentrations. Lower contact resistivity is achieved for metals in contact with a highly doped semiconductor (*i.e.* high conductivity) This higher doping concentration is only required directly under the metal contacts, whereas lower doping densities elsewhere would be beneficial in reducing the recombination. Traditional diffusion processes do not allow for this selectivity, however a wide range of patterning methods have been developed to address this issue. The selective emitter design is shown in Figure 9.

2.3 Module Design

2.3.1 Manufacturing Process

Photovoltaic (PV) module manufacturing is the process of converting completed solar cells into a single, functional unit that is ready for field deployment. For PV modules based on

standard c-Si solar cells this process can be divided into three primary categories: (1) stringing and tabbing, (2) lamination, and (3) integration of the junction box and bypass diode(s). This module fabrication process has been in use for over three decades and is effective in producing standardized solar panels with sufficient power and durability for use in a variety of applications.

Because the power produced from a single solar cell is relatively small, several cells must be electrically connected together to form a practical PV module. Typical configurations involve the serial connection of cells, with the front contact of one cell connected to the back contact of the adjacent cell. This interconnection process is known as stringing and tabbing. Once the cells are electrically configured, they are encapsulated within a protective package to ensure reliable operation in the outdoor environment. This packaging scheme includes a frontsheet, backsheet, and encapsulant secured together during a lamination step. Finally, a junction box is secured to the backside of the module. The junction box is typically where string interconnections are made, module connector leads are attached, and bypass diodes are incorporated. A cross section of a typical module is shown in Figure 10.

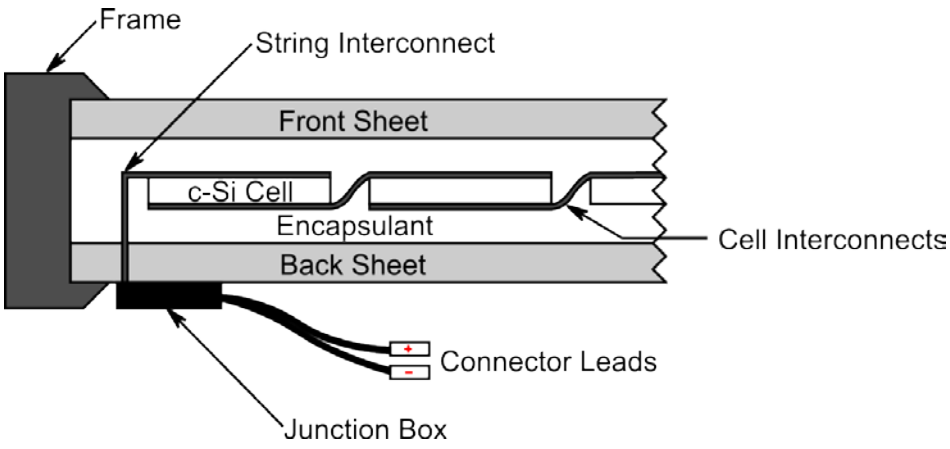


Figure 10. Typical structure of a PV module.

2.3.2 Reliability Concerns

Once a module is deployed, reliability refers to how that module will perform overtime. Although the module fabrication process is simple, there are a number of potential failure modes and degradation mechanisms that could impact the long term performance of the module. These issues are discussed in this section.

Several different failure modes can develop during or as a result of the cell interconnection processes. The failure modes include microcrack formation and cell fracture, solder bond failure, ribbon or interconnect failure, and corrosion. Microcracks, which may lead to cell fracture and increased module series resistance, can develop due to stresses caused by differences in coefficient of thermal expansion or applied pressure from soldering. Methods to avoid cell damage during soldering include using a low yield strength ribbon to allow for expansion during cooling and simultaneous stringing and tabbing reducing the thermal stress induced from the two soldering processes. Increased resistance also results from solder bond failure, which can be a result of poor solderability of the cell metallization, incompatible solder metal alloys, inappropriately sized solder joints, or metal diffusion from the solder. Ribbons can fail as a result of thermally-driven stresses, resulting in increased resistance and current crowding. Corrosion, although driven generally by moisture and other contaminants within the laminate, has also been linked to the laminate conductivity and both negative and positive biases during operation.

A number of metrology techniques including methods for individual component as well entire modules have been used to characterize and predict durability issues during the stringing and tabbing process step. Interconnect degradation can be determined through measurements

of module series resistance, which can be measured using illuminated or dark I-V curves or qualitatively through electroluminescence imaging. Electroluminescence imaging has also been used to identify grid-finger failures, cell fracture, and interconnect failure. Infrared thermography, both steady sate and lock-in, can be used to evaluate hot spots that form due to weak or failed solder bonds resulting in Joule heating of the solder ribbon. Additionally, thermal cycling can be used as a method to stress solder bonds and interconnects, to screen modules for issues related to thermal expansion.

There are also several component level tests that can be used to quantify properties of materials used and determine the quality of solder bonds or interconnects. The peel test can be used to determine the adhesion between the cell interconnect and the silicon substrate. The pull test can be used to determine the maximum stress level before failure. Dynamic mechanical analysis is useful in determining ribbon cycle lifetime. Information about solder bond quality can be obtained through electron microscopy techniques.

Lamination is the process of encapsulating interconnected cells to provide mechanical support, offer protection from environmental stresses, and ensure safe and reliable operation. A typical packaging scheme, or laminate, utilizes a glass front cover, multilayer polymer backsheet, and internal encapsulant such as EVA. Failure of the fundamental functions of the module packaging can lead to safety hazards, degradation of internal components or complete failure of the module. The failure modes for the module packaging itself are discoloration, delamination, mechanical failure, and backsheet degradation. Examples of these failures are shown in Figure 11. The laminate also has a significant influence on degradation mechanisms of the active internal

components including potential induced degradation within the cell and corrosion of the cell interconnects, metallic front or rear contacts, and cell antireflection coatings.

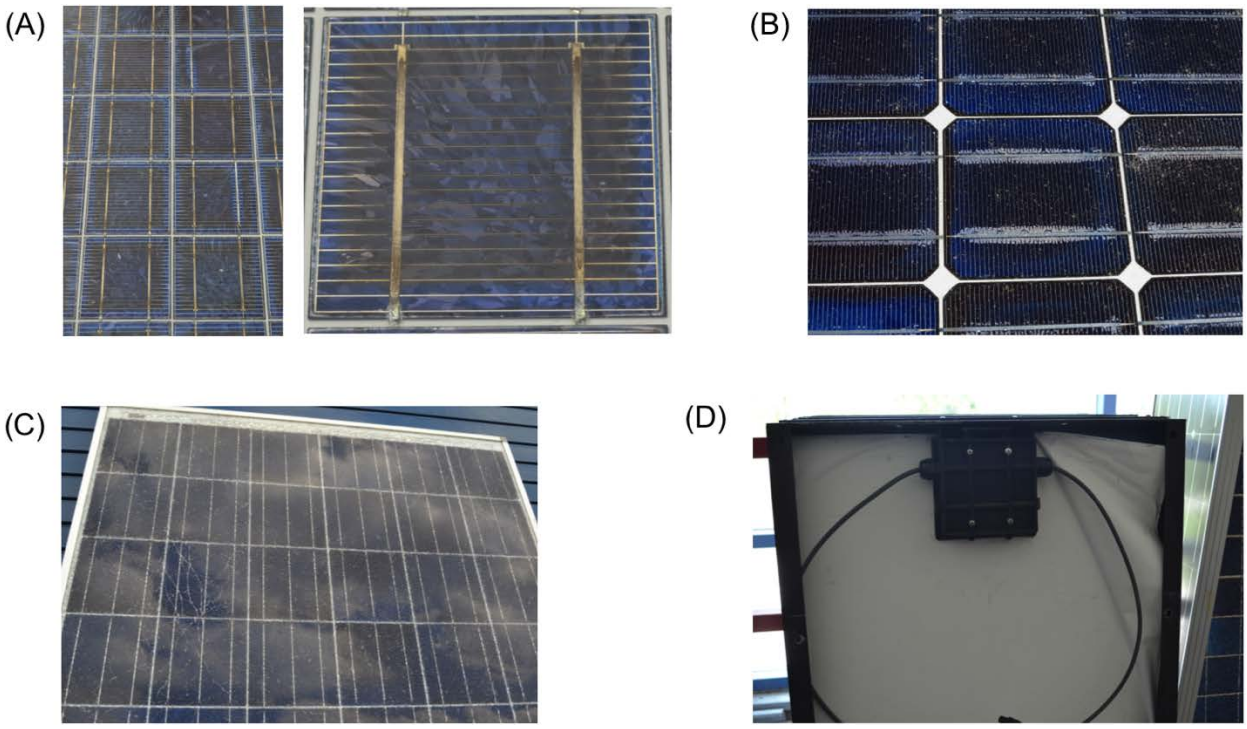


Figure 11. Example of module packaging degradation and failures. (a) browning or discoloration of the encapsulant, (b) delamination of the encapsulant near the busbars, (c) glass breakage and (d) back sheet delamination.

Breakdown of the basic functionality of the module junction box and protective bypass diodes can have a significant impact on the reliability and durability of the PV module. Junction box delamination can result in electrical shorting, ground faults, or corrosion. Series arcing within the junction box is also a potential result when there is an open circuit condition between two nearby points. This can be caused by poor solder joints between string interconnects or module connector leads, failure of bypass diodes, corrosion of electrical contacts, or degradation of

electrical insulation. There are a number of mechanisms that result in bypass diode failure, which include electrostatic discharge (ESD), thermal runaway, and thermal fatigue. Bypass diodes are sensitive to ESD, which can occur within a module manufacturing facility and lead to premature failure of a PV module if proper ESD precautions are not taken. The properties of the diode must also be considered, including the current-voltage characteristics and junction operating temperature, to avoid thermal runaway when the diode rapidly returns to reverse bias from a high temperature forward bias state and to avoid thermal fatigue if extended hot-spot conditions occur in the field. In the field, the operating condition of bypass diodes can be identified (including identification of failed diodes), through the use of infrared thermography, module current-voltage measurements, or with a non-contact voltage tester

Until only recently, reports on the field performance and reliability of bypass diodes have been missing from the literature. Several techniques have been discussed that allow one to monitor the functionality of bypass diodes in order to prevent catastrophic failure of the module through overheating or arcing. Additionally, new techniques to monitor the performance of bypass diodes in the field, prior to failure, need to be developed. There is also a need to qualify the use of diodes based on their resistance to failure as well as their compatibility with the junction box system and module electrical characteristics. In general, testing of individual components and materials along with evaluation of the entire system is essential to ensure reliable performance of c-Si PV modules.

CHAPTER 3: EVALUATING THE VALUE OF METROLOGY

3.1 Introduction

Metrology is defined as the "science of measurement and its application" according to the *International vocabulary of metrology — Basic and general concepts and associated terms (VIM)* [19]. In this definition, metrology is a general term that refers not only to the act of measurement itself, but also to the way that measurements are used within a larger scope to create information. It is important to realize that measurement data alone does not contain any inherent value. Value is only created when that measurement data is used to draw conclusions and to make decisions. Throughout the scientific community, metrology is key component to any credible research in that it provides object evidence and helps to establish relevant correlations.

Metrology can also be valuable in a manufacturing environment. In this case, metrology is used to increase production efficiency and improve product quality. When considering the PV manufacturing industry, metrology has consistently provided a broad range of benefits and appears in many different forms. One example would be process equipment that include sensors and control algorithms to reduce variability. Another example would be the I-V measurements performed on finished cells to group similar performing cells (known as binning) prior to module manufacturing. This enables manufacturers to sell higher performing cells/modules at a higher price. These applications of metrology have provided tremendous economic value to PV manufacturers, greatly outweighing the cost of the measurement tool itself.

Unfortunately, in many cases in-line metrology is viewed as an unnecessary added cost as opposed to something that provides value to production [20]. This is especially true in low margin industries such as PV manufacturing. The challenge is that there is no clear methodology

in place to evaluate the economic impact of in-line metrology. Although the cost of the metrology equipment is relatively easy to define, the benefit is not always immediately quantifiable. This often leads to the value being defined in qualitative terms. In this study a framework is developed to evaluate the economic value of metrology in manufacturing. Furthermore, this framework was made publicly available in the form of an on-line calculator. The goal was to create a comprehensive and transparent methodology to conduct a cost-benefit analysis for metrology and to encourage adoption through a simple and intuitive user interface.

The calculator can be found at https://pvlighthouse.com.au/cost-metrology . The calculator is intended to answer question such as these:

- Is it cost-effective to install a metrology tool that rejects poor wafers at the start of a production line?
- If a metrology tool helps to improve process control, does that improvement justify the installation and running costs of the tool?
- What number of sorting bins will maximize profit?

3.2 The Value of Metrology

3.2.1 Defining Value

In general terms, a product's value is assessed using a quality function. This quality function is based on defining characteristic of the product. For example, a fruit farmer may judge a fruit based on its size, shape, color or ripeness. Often as the product becomes more complex, the quality function also becomes more complex. The quality function may consist of pass-fail criteria or may include a grading scale where higher graded products are sold at a premium.

Understanding what defines this quality function is essential in understanding how metrology can be used effectively.

The quality of a solar cell is defined largely by its efficiency, or power output per unit area. Solar modules are marketed and sold based on the price-per-watt ($/W). Therefore, the more watts a cell produces the higher its value. This is why the end of the line I-V measurements are an integral part of any manufacturing environment. Higher performing cells will be put in higher end products commanding a higher per-unit price. In this way the quality function of a solar cell is defined by a single metric (power) on a graded scale. Figure 12 shows the "staircase" function that governs the market price of a cell as a function of cell power.

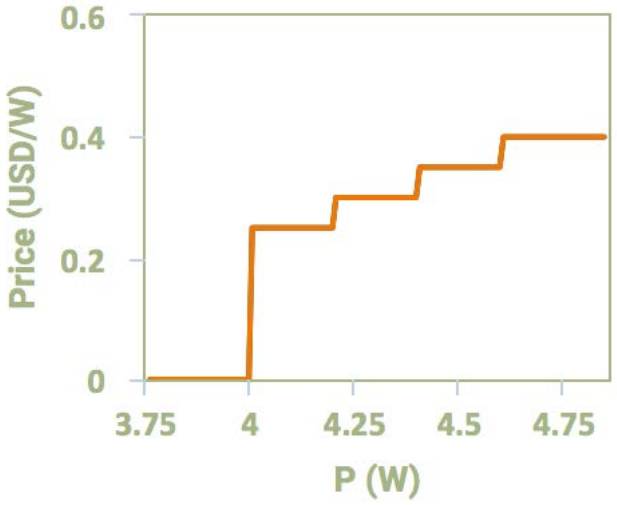


Figure 12. Example of a price per watt function for c-Si PV cells.

All cells fabricated from the same production line are manufactured at the same cost. On the other hand, not all cells from the same production line will have the same efficiency. Therefore, it is important to reduce variability and maximize the average cell efficiency. This is often the main function of metrology.

Lastly, there are other factor that influence the final market price for a solar module. As discussed previously the LCOE is the most appropriate metric for assessing the cost of solar energy. Therefore, any factor that would increase the LCOE should also increase the value. An example of this would be screening for reliability related defects at the cell level. Although this process may increase the $/W production cost, the increase in the lifetime of the product may reduce the overall LCOE. Another example would be design improvement to maximize efficiency under low light conditions, thereby increasing the total energy yield of the module. Since this improvement would not be captured by a standard 1-Sun I-V measurement, it would appear only as an increase in the production cost. Although these impacts are not directly addressed in the on-line calculator, the framework does allow for their consideration. Simply, a new quality function would be required that could incorporate these additional factors. Future version of the calculator may include features to address this.

3.2.2 Quality Control

There are several different applications for metrology each having its own unique economic impact, with some applications having more than one potential benefit. The most direct use of metrology is for quality control. Essentially, this would include any metrology that could trigger an action to improve the quality of that unit or any future unit. Because the quality function for c-Si solar cells is defined only by its efficiency, anything that improves the efficiency would be considered in this category. In the case of solar cell processing this may include (1) cell or wafer rejection, (2) sorting/binning wafers, or (3) direct feedback for process control. Each of these three applications are directly addressed within the calculator.

Wafer rejection is used to eliminate lower quality wafers from incurring any further processing cost. To illustrate this, consider the fact that nearly half the cost of cell fabrication is due to the silver consumption during the metallization process. If a poor quality wafer is rejected before these contact formation steps are performed, the economic penalty of that low quality cell is reduced by half [21].

Wafer sorting is used to achieve efficiency gains by separating wafers of different characteristics into different production lines or different unit process steps. For example, wafers with a high concentration of iron may benefit from different phosphorus diffusion process parameters than wafers with a lower concentration in iron. By sorting wafers based on their iron concentration and using the appropriate defect engineering (*e.g.* gettering) process parameters [22, 23], the efficiency of these more heavily contaminated wafers can be increased.

Process control is considered any use of metrology in which a feedback loop is used to reduce process variability and ultimately increase the average cell efficiency for a given production line. One example of this would be optical inspection of cells after screen printing. Because screen printing is a mechanical process, it is prone to wear over time. An optical inspection system that identifies defects in the metallization could alert a technician to replace or clean a screen once the defect severity reaches some pre-defined critical level. This would reduce the number of defective cells, resulting in a positive impact on overall cell efficiencies.

3.2.3 Opportunity Cost

The other broad category in which metrology could provide economic value is in terms of opportunity cost. Opportunity cost is defined as a benefit, profit, or value of something that must be given up to acquire or achieve something else. This may manifest itself in several ways,

however the true economic impact is difficult to quantify. One of the simplest examples of an opportunity cost would be the loss in production due to equipment failure. Equipment failure diverts time and resources that could have been used to create products. Any metrology tool that could expedite failure analysis and troubleshoot manufacturing problems could add economic value by reducing opportunity cost.

Within the PV industry, as is the case with nearly all industries, innovation is required to succeed in a competitive landscape. Companies that accelerate product development are able to differentiate themselves from their competition and have the potential to gain market share. Although difficult to quantify, the opportunity cost here would be for companies that fail to innovate and miss an opportunity to gain a competitive advantage. In this way any metrology that assists research and development teams, has the potential to provide economic value overtime.

Opportunity cost is inherently difficult to define in quantitative terms. In certain cases, reasonable estimates could be considered within this cost analysis. For example, expected equipment downtime could be used to estimate the yearly production capacity for a line with or without a particular metrology tool. In many cases, however, the direct economic impact is purely speculative and is impossible to predict. Because of this, opportunity cost is not directly addressed within this calculator. This factor could, however, be considered as a source of indirect "added value" when considering in-line metrology.

3.3 Calculator Methodology

3.3.1 Terminology

It is important to maintain consistency when discussing the various aspect of this metrology cost-benefit analysis. The ***measurand*** *(M)* refers to the quantity or metric being measured by the metrology tool. When discussing ***cost***, this is from the perspective of the manufacturer, referring to the cost incurred by the manufacturer during production. On the other hand, ***price*** refers the dollar amount that the manufacturer can expect to receive for selling a particular cell.

3.3.2 Overview

To quantifying the economic impact of metrology, a program was developed to simulate the production of a batch of cells. Within this simulation various inputs are used to define factors that influence performance and cost. Using these inputs, batches of wafers are processed into solar cells and sold. Specifically, two batches are considered side-by-side including a ***baseline case*** and a ***test case***. The baseline case is used to represent a production line without the incorporation of a particular metrology tool and the test case represents that same production line with metrology. Finally, the profits for each case are compared to establish the cost-effectiveness of a given metrology tool. As is the case for any simulation, the validity of any conclusions depends on the accuracy of the inputs and the validity of the assumptions used.

The economic analysis for in-line metrology is based on two fundamental relationships. The first relationship is between the measurand and the power of the cell (referred to as the dependence of *P* on *M*, or simply *P*(*M)* function). The second relationship is between the power of the cell and the price at which that cell can be sold (referred to as the Price per Watt Function).

On a very basic level, these two relationships create a direct link between the measurand and the final price of the cell. Although it is not always public, the price per cell information is a fairly straightforward relationship to determine. On the other hand, determining the relationships between the measurand and power is not trivial. It is rare for any single cell or wafer parameter to have a high predictive capability with respect to the final cell performance. Additionally, many relationships are influenced by the specific process flow and fabrication equipment used, requiring each manufacturer to obtain these relationships independently. The calculator is design with this uncertainty in mind, allowing several opportunities to add sources of variation.

Other key inputs include the expected distribution of the measurand, as well as the costs associated with production. A variety of additional inputs are available and are all discussed in detail below. Although a generic case including all possible inputs is available, the calculator has been optimized to assess metrology for two specific applications. These include wafer rejection or sorting and process control.

For **wafer sorting**, the user defines cutoff values for *M* and can input a new set of performance and cost considerations representing a new process flow for those wafers. Alternatively, the cutoff values can be used to reject wafers and eliminate any future costs that may have been associated with those wafers. **Process control** is simulated by assuming a shift or change in the distribution of the *M*. Here, the baseline case would include the distribution of *M* that existed prior to metrology insertion. By inserting metrology for process control, the distribution of the *M* can be altered with the intent to improve the average cell efficiency.

An example of the process control use case is shown in Figure 13. This is not meant to represent a specific metrology tool, but is instead intended to explain how this methodology is

applied for process control. In this figure, the top left input parameter represents the distribution of *M* both before and after metrology insertion. Here, it is assumed that a new metrology tool created a process feedback mechanism that increased the average value of the *M*. Because this measurand has a direct relationship with power, this shift results in an increase in the average power of that batch. There is, however, an added cost associated with this metrology step as shown in the bottom right input. The dependence of *P* on *M*, as well as the sale price, does not change between the two cases. As described in the output table, a larger fraction of cells in the test case appear in the more lucrative power grades. In this case, this increase outweighs the added cost resulting in a higher average profit per cell overall.

In Figure 13 many of the detailed inputs are neglected in order to express a simplified view of how the methodology works. The remainder of this section will focus on the various inputs and their impact.

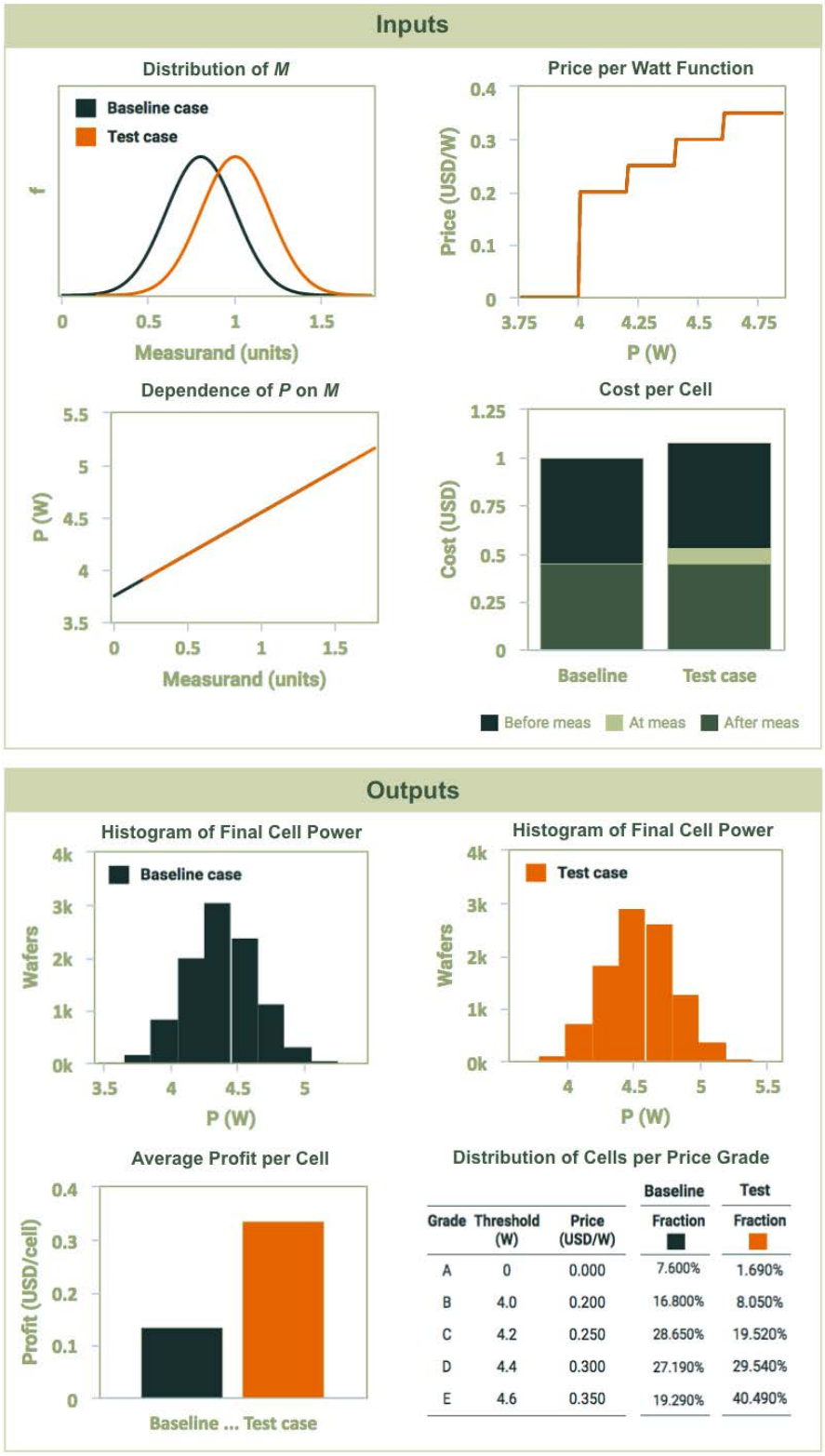


Figure 13. Example of essential inputs and simulation outputs considering a process control application of metrology. Notice the variation in the distribution of the measurand between the two cases (top-left) and how this impacts the distribution of the final cell power.

3.3.3 *Inputs*

3.3.3.1 *Distribution of M*

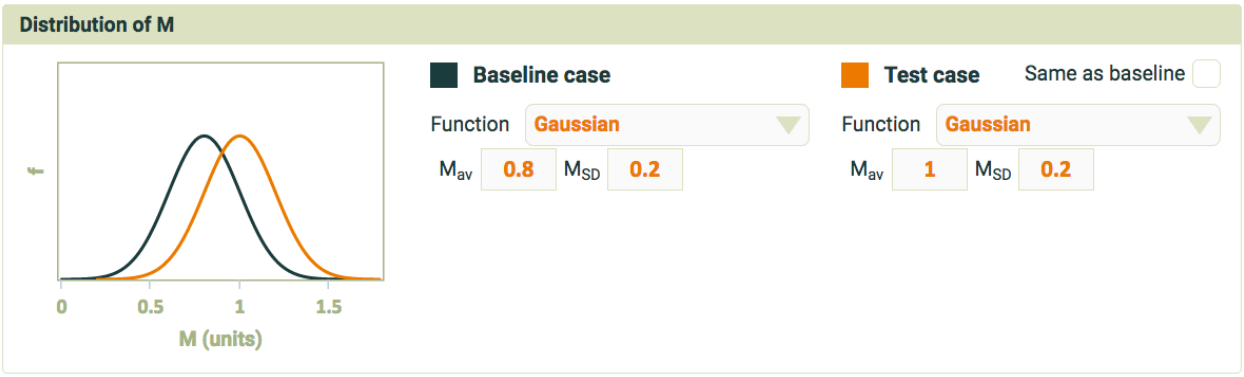


Figure 14. Input dialog for the distribution of the M

The measurand (*M*) represents a metric being assessed by a particular metrology tool. This can be a direct measurement result or a derived metric from one or measurement inputs. A list of parameters relevant to c-Si manufacturing are provided in Table 1. *M* will normally vary from wafer to wafer with the variation in *M* described using a distribution function. This function describes the range of possible values for *M* and the probability that any wafer will have a particular value of *M.* In this calculator, users can choose from different types of distribution functions or load their own data that the calculator will use (*i.e.* lookup table). When choosing from the available distribution functions, users input the pertinent characteristics for that function (*e.g.* average, standard deviation). Figure 14 is an example of the input dialog when using a Gaussian distribution. Figure 15 shows the different distribution functions built in to the calculator.

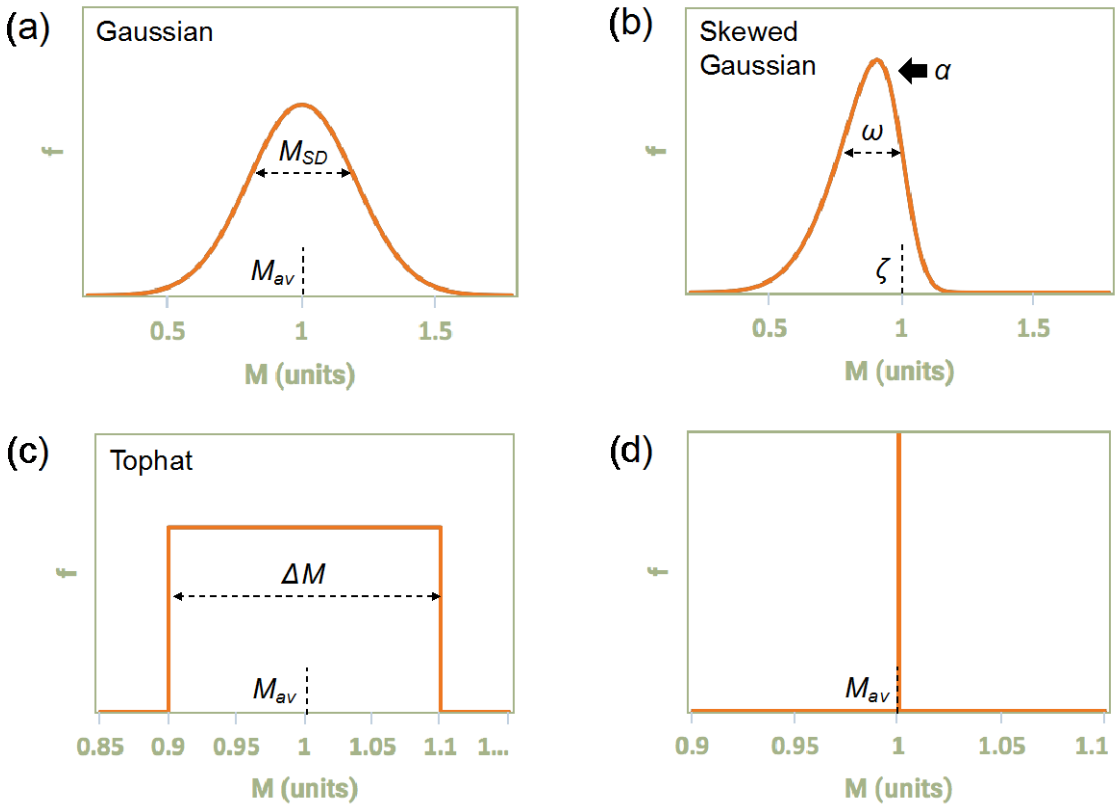


Figure 15. Possible distribution functions including the parameters used to describe each function.

Table 1. List of parameters relevant to c-Si PV manufacturing along with the appropriate insertion points in the manufacturing process flow.

Insertion Point(s)	***Parameter or Measurand***
As-cut wafer	Wafer resistivity Wafer physical dimensions Presence of cracks and chips Presence of oxygen-related defects Bulk carrier lifetime Presence of metal impurities (*e.g.* Fe)
After saw damage removal	Etch depth Presence of striations
After texturing	Etch depth Pyramid size and uniformity (mono-Si) Reflectance
After phosphorus diffusion	Sheet resistance Doping profile Effective carrier lifetime
After PECVD SiN_x	SiN_x thickness SiN_x complex refractive index Reflectance Color uniformity Effective carrier lifetime Presence of cracks
After screen-printing	Line width Paste laydown (via cell mass) Presence of printing irregularities
After co-firing (*i.e.* finished cell)	Illuminated *I-V* characteristics Presence of cracks Presence of metallization defects Presence and severity of hot spots Non-STC *I-V* characteristics (*e.g.* Suns-V_{OC}) Wafer bow Mechanical strength Spectral response, quantum efficiency

3.3.3.2 *Measurement of M*

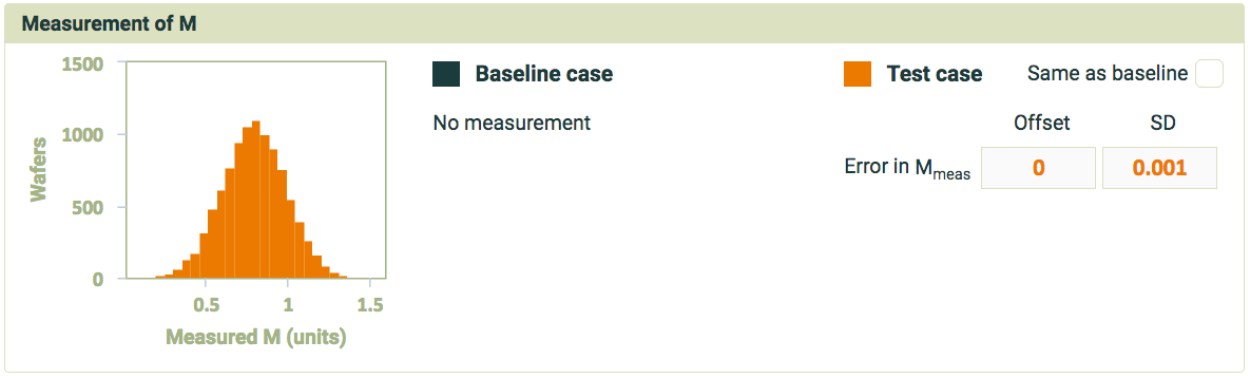


Figure 16. Input dialog for measurement of M.

For any given *M*, the actual value is an inherent property of the object being measured. When a measurement is performed, an expected value of *M* is defined with some level of precision. This input panel allows the user to define exactly how precise (or uncertain) a metrology tool is. A probability function is used to describe the range of possible measurements results for a given *M*.

In this calculator, the distribution due to measurement uncertainty is assumed to be Gaussian described using a standard deviation. Users can also input a systematic error (*i.e.* offset) that represents a consistent and unintentional shift in the expected value from the mean of the measurement's probability distribution. In practical cases, this offset error is either unknown or, if known, can be eliminated via calibration. This factor is included within the calculator so that users can understand the impact of systematic error on profitability. When not considering metrology, both the standard deviation and offset are set to zero.

When the running the simulation, measurement uncertainty is applied to the measurement of each cell. This is intended to replicate real world scenarios in which metrology tools provide inaccurate results. This can be critical in when considering metrology for wafer

rejection. If the measurement uncertainty is high, there is a potential to reject “good” wafers. This input enables users to answer questions about what level of precision is required for a particular metrology tool and how inaccurate measurements will affect their bottom line.

3.3.3.3 *Sort by Measured M*

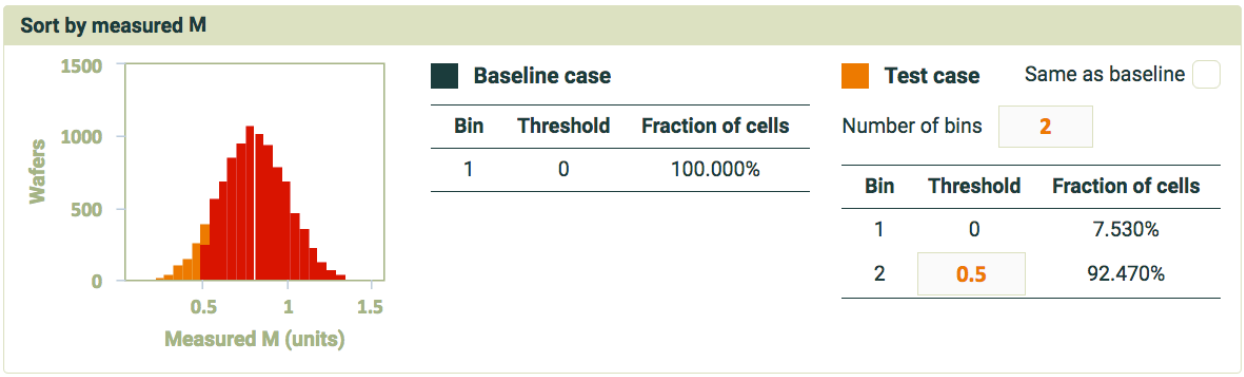


Figure 17. Input dialog for sort by measured M.

Binning of cells is required whenever a metrology tool is used to sort or reject wafers. In this panel users are provided with options to define the number of bins and the threshold for each bin based on the measured value of *M*. As soon as these are defined, the fraction of cells found in each bin is calculated and displayed. A key aspect to this methodology is that each bin can have unique performance, cost, and price considerations. This enables the user simulate a wide variety of potential applications.

Manufacturers may choose to reject “bad” wafers and prevent them from continuing through the manufacturing process flow. In this case, “bad” might mean a low bulk carrier lifetime that will ultimately lead to a cell with a very low *P*, or a mechanically fragile wafer that will likely break during handling or processing. By eliminating these wafer, they do not incur any further costs downstream.

Alternatively, manufacturers may wish to sort wafers in an attempt to optimize production. Large manufacturers, for example, may have multiple production lines each with a unique cell architecture. Incoming wafers may be screened in order to direct higher quality wafers to the more efficient cell line (e.g. rear passivated), while lower quality wafers are directed to the more standard cell production line (e.g. Al-BSF). In this case quality may refer to the bulk lifetime, the resistivity, defect concentration, or some combination of parameters.

3.3.3.4 *Variability in P at constant M*

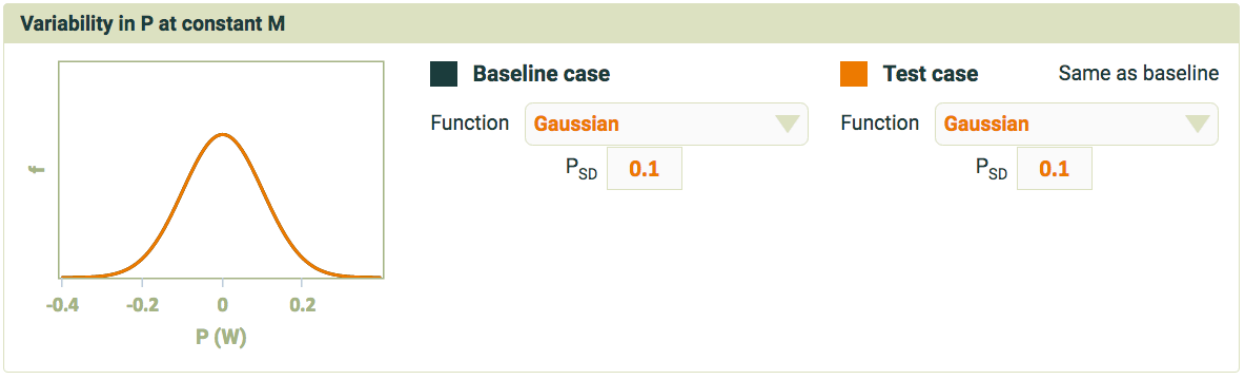


Figure 18. Input dialog for variability in P at a constant M

Not all *M* values will have a well-defined relationship with *P* as the final cell efficiency is impacted by many separate variables. Within this methodology, this is considered variability in *P* that is external to, or independent of, *M*. To address this, the user defines a distribution that represents power at a given, or constant value, of M. This could be determined experimentally by running a batch of cells, selecting a group of cells within a small range of *M* values, and observing the variation in P for that group.

As an example of this, consider a technique that accurately measures recombination in the emitter (*e.g.* injection-level dependent photoconductance). This technique will capture variability due to the $POCl_3$ process, but other factors like the texturing process, SiN_x deposition,

and metallization will also influence P and each will have some variability. This external variability is captured using the probability function described in this panel.

3.3.3.5 *Dependence of P on M*

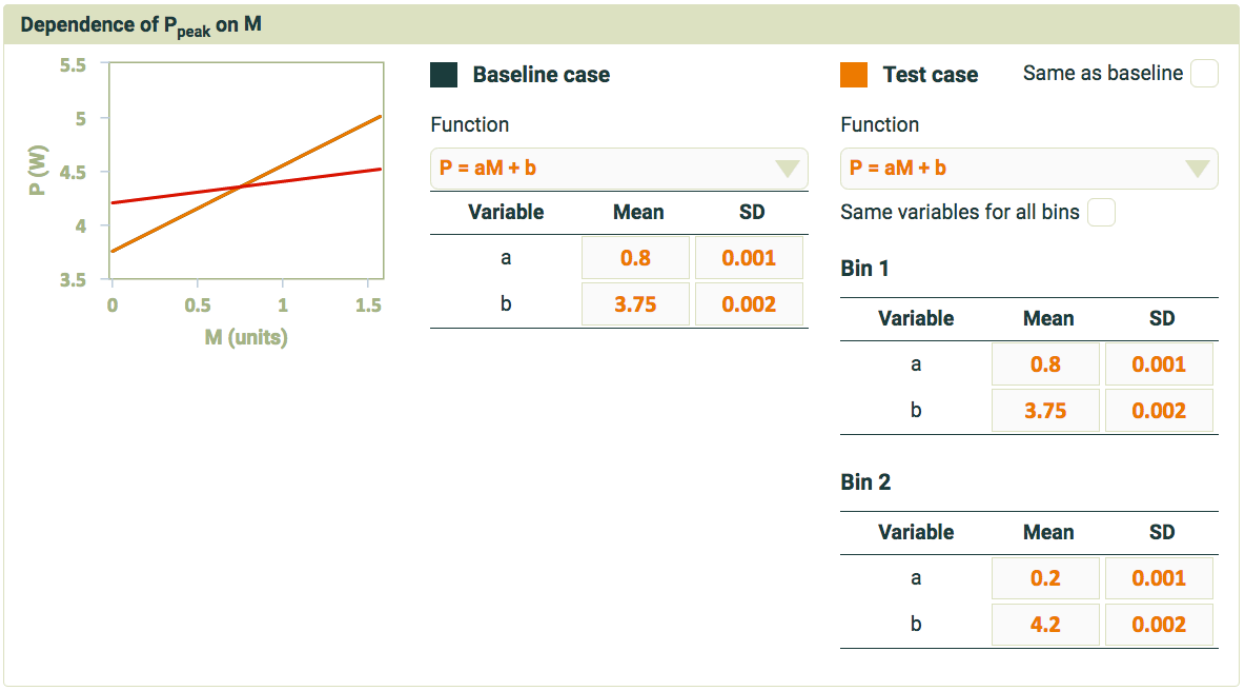


Figure 19. Input dialog for dependence of P on M

A key component to this cost-benefit analysis is understanding how a given *M* influences the final cell efficiency. This is described using a *P(M)* function. A unique function can be defined for each case and each bin. Built in function include linear, polynomial, exponential, and logarithmic. The user inputs a value for each constant within the function to describe the relationship. A standard deviation input is also available so that the user can explore how uncertainty in this relationship impacts the results. This is important because some relationships are easier to define than others and real uncertainty will exist when trying to determining this function. When considering a wafer rejection scenario, the power of all cells in that bin should be set to zero.

Determining this relationship would often require the use of track trials. This would include running a statistically significant number of samples through a particular production line and using the end-of-line power measurements to generate a correlation. Another approach to determining this relationship would involve device modelling. Here, a simulation software such as PC1D or Quokka [24] could be used to assess how one particular property impacts efficiency. Because device simulation is a cheaper alternative to track trials, this may be best suited for preliminary evaluations.

3.3.3.6 Cost per Cell

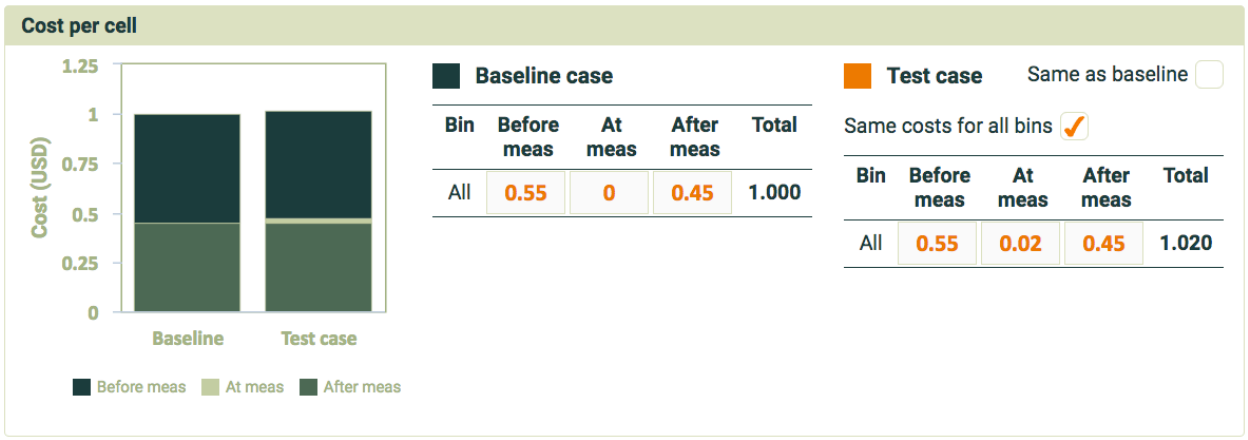


Figure 20. Input dialog for production costs per cell.

Cost refers to the expense incurred during the manufacturing of each cell. These cost consist of upfront equipment cost, operating expenses, material cost and others. Because reducing cost is such an essential aspect of photovoltaic manufacturing, several publications address this issue [25-30]. In this calculator the cost of the cell must be defined for processing performed before the metrology step, for processing performed after the metrology step, and for the metrology step itself. As mentioned previously, different cost structures can be defined

for each bin to simulate different process flows. When the baseline case does not include metrology, as shown in Figure 20, the cost of the metrology step is set to zero.

Because the insertion point of the metrology step will vary from case to case, it is important to quantify costs associated with each process step. A cost model developed by Basore works especially well in this scenario [26]. In this approach, cost points are associated with each step and are adjusted for various factors influencing each process. The idea is to start with a known process flow with an established cost structure. As an example, the breakdown of cost points for a typical Al-BSF process flow is shown in Table 2. If the overall cost of the cell is known, then the cost per point can be determined. For this case, if the overall cost per cell is $1.00, then the cost per point would be 2.94¢. From this, it is possible to determine the cost associated with each step and ultimately, the cost both before and after the metrology insertion point can be calculated.

Table 2. Cost point allocation for a typical Al-BSF process sequence [26]

Process	***Points***
Wafer cost	*19*
Texturing	*1*
Wet Cleaning	*1*
$POCl_3$ diffusion	*1*
PSG removal	*1*
Single-side etch on the rear	*1*
PECVD SiN_x front	*2*
Screen print Ag front	*4*
Screen print Ag:Al rear	*2*
Screen print Al rear	*1*
Belt fire	*1*
Total	***34***

3.3.3.7 *Price per Watt*

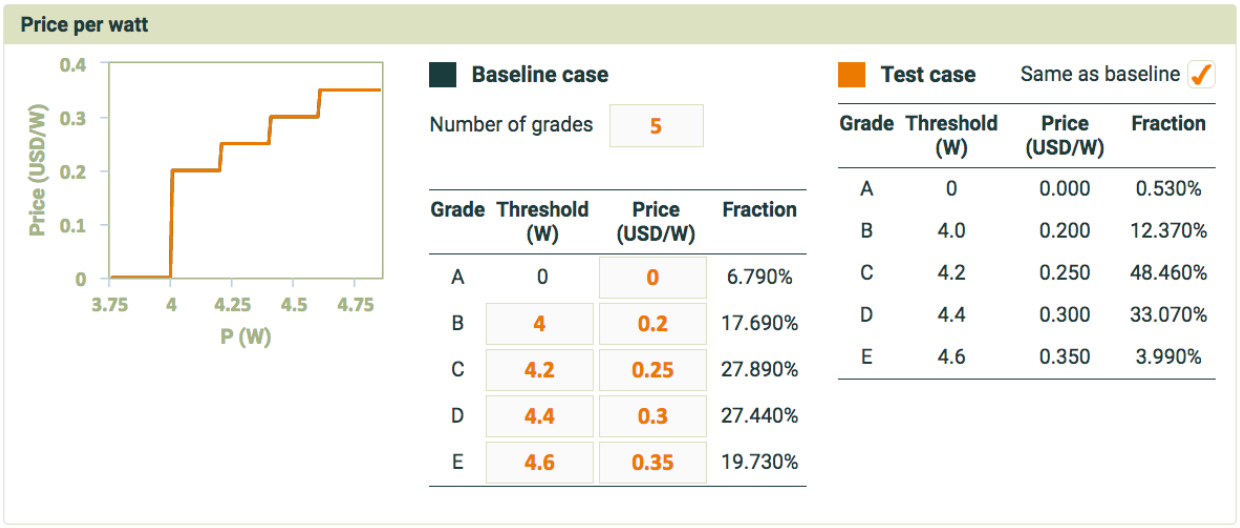


Figure 21. Input dialog for defining the sale price of cells.

The price refers to the selling price for a given cell. This is typically defined in terms of $/W. As the performance of the cell increases the selling price for that cell also increases. Cells are binned at the end of a line based on their power. A staircase function, as shown in Figure 21, is used to define the price associated with each power bin. The percentage of cells in each power bin is shown in this panel.

As discussed in section 3.2.1, the quality function for solar cells may evolve to include more than just efficiency. In this case, any metrology tool that improves "quality" would potentially impact the price function. If, for example, improved LCOE was considered as valuable, factors such as low-light performance, weight or reliability would command a higher price. Another example would be aesthetics. Residential customers regularly pay more for a visually pleasing module, where utility or commercial customers would not. To address this the user could consider assigning price premiums for each of these factors. Price premiums would be applied to each power bin equally.

3.3.3.8 *Mechanical Yield*

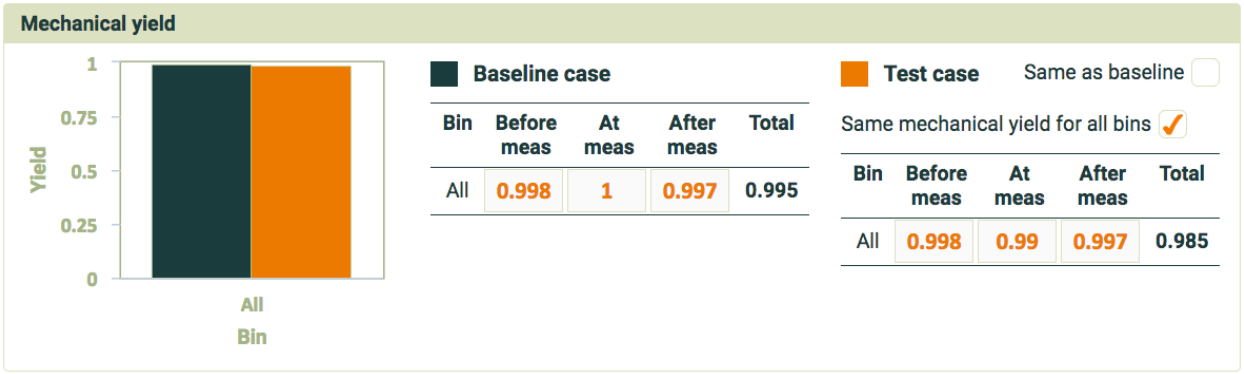
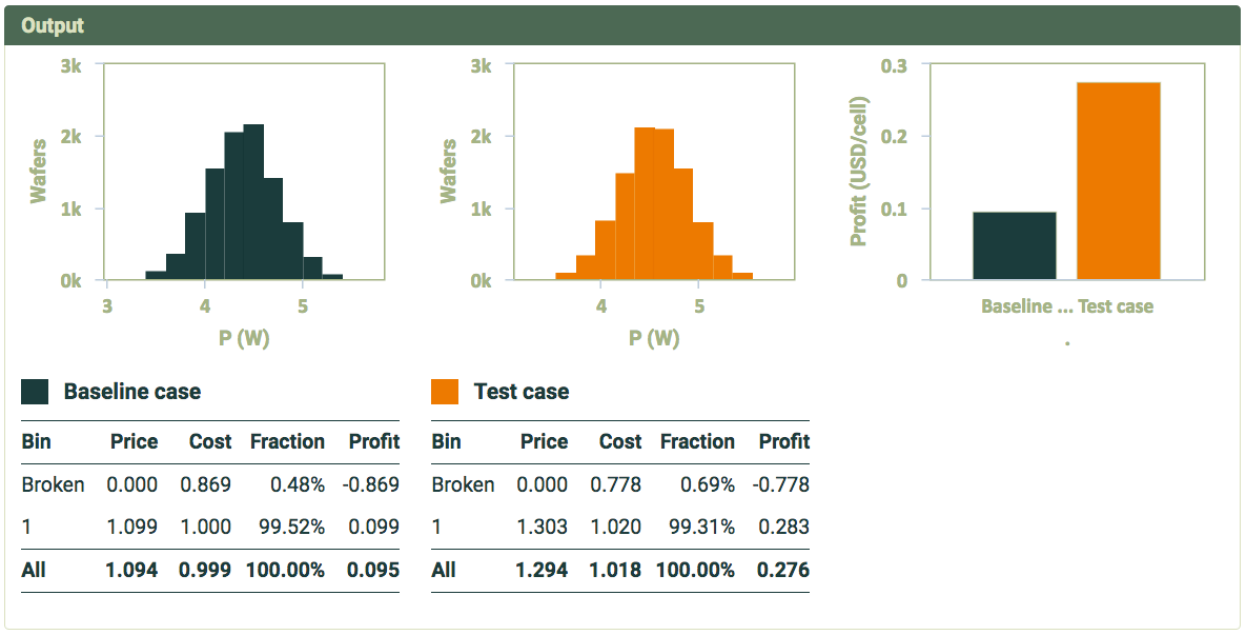


Figure 22. Input dialog for mechanical yield.

Mechanical yield is a term that describes the percentage of wafers that are successfully processed without mechanical damage. Since Silicon is a brittle material, any mechanical damage will lead to wafer fracture. Mechanical yield is defined for processing prior to the metrology step, for processing after the metrology step, and for the metrology step itself. For each new process step introduced, the probability of wafer breakage increases. This has the potential to reduce the economic value for metrology, especially for metrology techniques that requires physical contact with the wafer or cell.

3.3.4 *Outputs*



Baseline case

Bin	Price	Cost	Fraction	Profit
Broken	0.000	0.869	0.48%	-0.869
1	1.099	1.000	99.52%	0.099
All	**1.094**	**0.999**	**100.00%**	**0.095**

Test case

Bin	Price	Cost	Fraction	Profit
Broken	0.000	0.778	0.69%	-0.778
1	1.303	1.020	99.31%	0.283
All	**1.294**	**1.018**	**100.00%**	**0.276**

Figure 23. Cost-Benefit Calculator Outputs

The input probability distributions are used to assign specific characteristics to individual cells. Using these characteristics, cells are “manufactured” according to all of the relevant inputs and are “sold”. The simulation will consider a batch of up to 10,000 cells. The results are tabulated and the statistics are calculated. The histograms of cell power are shown for both cases. The profit details are displayed for each sorting bin and an averaged is calculated for each case. Finally, a bar graph compares the two batches of cells using the average profit per cell. It should also be noted that outputs regarding the number of cell in each price bin are shown in the *Price per watt* Panel.

3.3.5 Discussion

As a summary, the basic steps to use the calculator are listed:

(1) Determine how the selected metrology will be applied to improve manufacturing (*e.g.* process control, rejection).

(2) Identify the specific measurand (*M*) being evaluated and determine a probability function that represents the baseline variability in *M*. If process control is considered, determine how this probability distribution will be altered.

(3) If binning, sorting or rejecting is considered, determine relevant cutoff values of *M* for each bin.

(4) Establish a function that describes the relationship between *M* and *P* (*i.e. P(M) function).* Define this separately for each bin if appropriate.

(5) Determine the cost associated with manufacturing. Breakdown these cost in terms of before, after and during the metrology step.

(6) Identify the price function that is most appropriate for these cell. Consider price premiums if appropriate.

(7) Quantify the impact of metrology in terms of mechanical yield (*i.e.* what fraction of cells are likely to break).

(8) Add sources of variability where appropriate. The most critical source of variability is the variation in *P* that is independent of M (‘*Variability in P at constant M’* panel). Other sources include measurement error and uncertainty in the *P(M)* function.

Once all appropriate probability distributions are set and each function is defined, the user can start to ask critical question regarding the use of metrology. It is advised that all variability be included only after all the critical inputs are established. As new sources of uncertainty are incorporated within the model, the economic impacts can be evaluated. Because the simulation updates in real time, any adjustment in input parameters will immediately change the results.

Some possible inquiries to explore might include:

- What is the maximum profit one could expect for a given metrology application?
- What is an appropriate per-unit cost target for a given metrology tool?
- For a given metrology step, what is the per-unit cost in which the economics become unfavorable?
- How does measurement uncertainty impact the results?
- What is the optimal threshold for wafer rejection to maximize profit?
- If the distribution of *M* is narrowed as a result of process control, are the economics improved?
- If there is low confidence (*i.e.* high uncertainty) in the *P(M)* function, does the insertion of metrology still have a positive impact?
- What type of price premiums would be required to make a reliability related metrology tool viable?

There are many different aspects that could be considered and this list is certainly not comprehensive. It is important to realize that any derived conclusions are only as good as the inputs that were selected. The next section will discuss several examples of how this calculator could be used.

3.4 Case Studies

3.4.1 Wafer Rejection Based on iV_{OC} Prior to Metallization

For both Al-BSF and PERC cells, screen-printing and contact firing (*i.e.* metallization) represent nearly half the cost of manufacturing a cell. Before metallization, wafers in PERC manufacturing feature a passivated front and rear side, unlike pre-metallized wafers in Al-BSF manufacturing that have an unpassivated rear. Because of the low surface recombination on both sides of these partially-processed wafers, the implied open-circuit voltage (iV_{OC}) measured at this point in the PERC process flow is a good indicator of what the final cell's V_{OC} and efficiency will be. For underperforming wafers, the economic may favor rejecting these cells to eliminate the cost incurred from the metallization steps.

In this case study, the measurement of iV_{OC} following front and rear passivation in PERC cell manufacturing is used as a test case to evaluate the cost/benefit tradeoff of metrology in PV cell manufacturing. Several methods exist to determine iV_{oc} including photoconductance or photoluminescence measurements, however this methodology is not specific to any particular metrology technique.

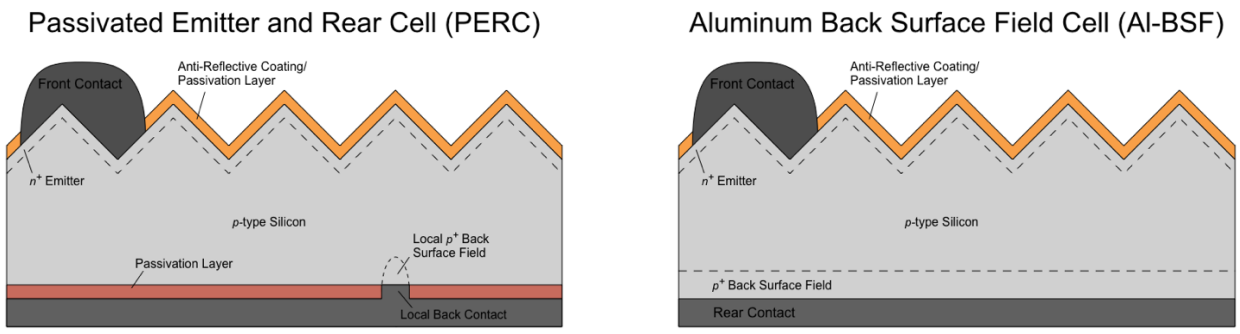


Figure 24. Cell architecture for PERC and Al-BSF cells. The front surface is highlighted in orange and the rear surface passivated of the PERC cell is highlighted in red.

The dependence of the final cell Power on iV_{oc} , $P(iV_{OC})$, is assumed to be linear in this case with coefficients of a = 8.307 and b = -0.989. Uncertainty in both the slope and intercept can adjusted by the user. A low uncertainty in the $P(iV_{OC})$ function means iV_{OC} is a good predictor of the final cell efficiency. Here the standard deviation in a and b is assumed to be 0.002 for simplicity. For the reject bin, a and b are set to zero, meaning all the rejected wafers have P = 0. The variability in P at a fixed iV_{OC}, is assumed to be a normal distribution with a standard deviation of 0.1 W_p. This represents the small variation in power due to other aspects of cell processing (*e.g.* emitter properties, local non-uniformities).

The cost per cell is defined for a three points: (1) the cost before the measurement, \$0.75/cell; (2) cost for the measurement and automation, \$0.06/cell; and (3) the cost after the measurement, \$0.25/cell. These costs were defined by assuming a final manufacturing cost \$1.00/cell and applying the cost points system (described in Section 3.3.3.6) to distribute the \$1.00/cell appropriately. The cost for the baseline case line doesn't include the \$0.02/cell for metrology. The reject bin in the metrology test case assumes zero cost is incurred after the measurement takes place, since the wafers aren't processed further. The pass bin for the metrology production line includes all three costs. All relevant inputs are shown in Figure 25.

The assumptions in this simulation are only estimates based on literature sources and are only meant to demonstrate how this calculator works. The results are not intended to make the business case for or against any specific metrology. The economics based on these specific inputs assumptions are favorable, suggesting that this may be a viable solution under certain circumstances.

Baseline case

Bin	Price	Cost	Fraction	Profit
Broken	0.000	0.885	0.52%	-0.885
1	1.259	1.000	99.48%	0.259
All	**1.252**	**0.999**	**100.00%**	**0.253**

Test case

Bin	Price	Cost	Fraction	Profit
Broken	0.000	0.904	0.56%	-0.904
1	0.000	0.760	8.65%	-0.760
2	1.380	1.010	90.79%	0.370
All	**1.253**	**0.988**	**100.00%**	**0.266**

Figure 25. Critical inputs for simulating wafer rejection from iV_{oc} measurements for.

Now that all model input parameters have been developed, the calculator can be used to optimize profits. For example:

- What is the optimal rejection threshold?
- What is an appropriate per-unit cost target for this metrology tool?

To answer these questions, five simulations are performed with 10,000 wafers for both production lines. The reported profit per cell is given as the mean of the five simulations with error bars representing the standard deviation. As more variation that is introduced to the model, the variability from run-to-run will increase.

The influence of the iV_{OC} rejection threshold on the profit per cell and the wafer rejection rate is shown in Figure 26. Wafers with iV_{OC} above the threshold "pass" and continue to be processed into PERC cells, while wafers with an iV_{OC} below the threshold are "rejected" and are not processed any further.

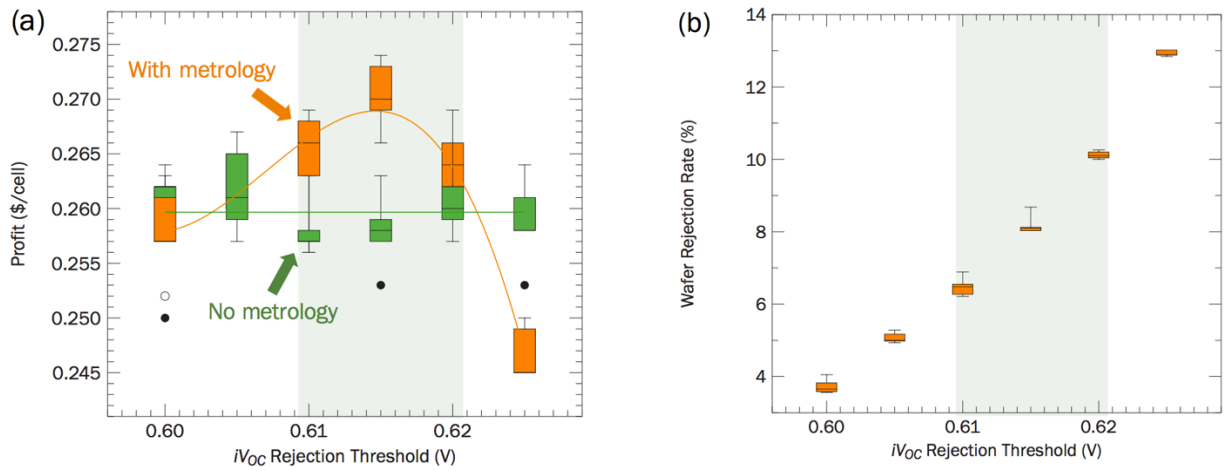


Figure 26. Influence of the rejection threshold on the (a) profit per cell and (b) wafer rejection rate.

As the rejection threshold increases from 0.600 V to 0.625 V, the wafer rejection rate will also increase. If the threshold is too low, then poor quality wafer will still be processed incurring cost. If the threshold is too high, good wafers will get rejected prematurely. For this specific example an optimum is found in the range of 610-620 mV.

For metrology cost suppliers it is important to understand what an appropriate cost target should be. To investigate this, the cost of the metrology step was varied while maintaining a fixed rejection threshold. The point at which the economic benefits outweigh the cost of the metrology insertion is identified at $0.02/cell. A metrology cost lower than this make the PERC line more profitable, and a metrology cost higher than this makes the PERC line less profitable. Approximate costs for two unit processes used in Al-BSF and PERC manufacturing are shown as reference points.

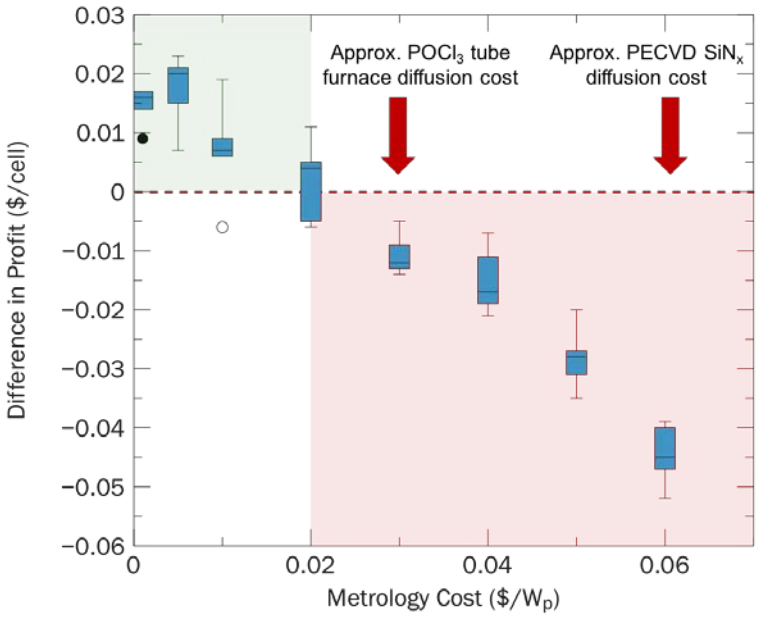


Figure 27. Impact of metrology cost on profit for wafer rejection.

3.4.2 *Advanced Optical Inspection for Screen Printing Process Control*

To demonstrate the effect of process control, consider the use of an optical inspection system after metallization [31]. Manufacturers are often considering methods to reduce silver consumption during metallization to reduce costs. This has resulted in a reduction of the line width of metal fingers, pushing screen printing methods to their limit [32]. Because screen printing is a mechanical process, it is possible for screens to get damaged or clogged resulting in metallization defects. Figure 28 shows an example of two cells in which there are several defects in the metallization. Here, defects refer to gaps in the continuity of the grid lines that impact current conduction in select regions of the cells. These defects appear as dark horizontal lines in electroluminescence images. When these electroluminescence images are magnified, as shown in Figure 29, the discontinuity of the grid lines becomes visible. These defects lead directly to an increase in the series resistance of the cell, reducing cell efficiency.

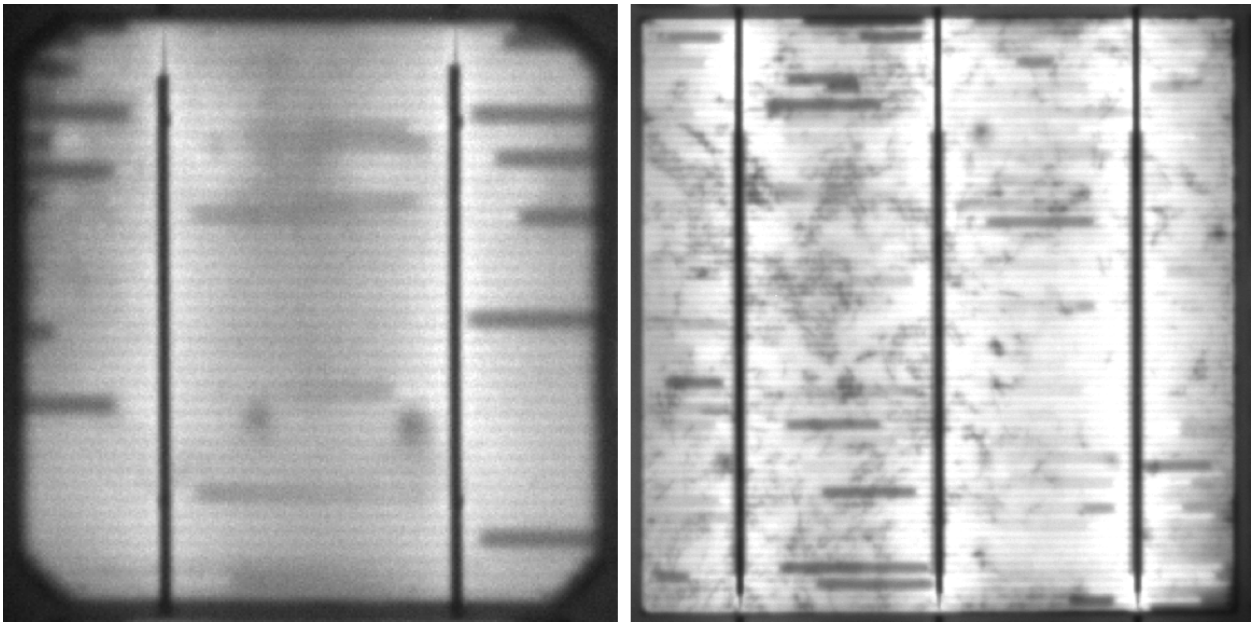


Figure 28. Electroluminescence image of a monocrystalline cell (left) and a multicrystalline cell (right) with a high number of metallization defects.

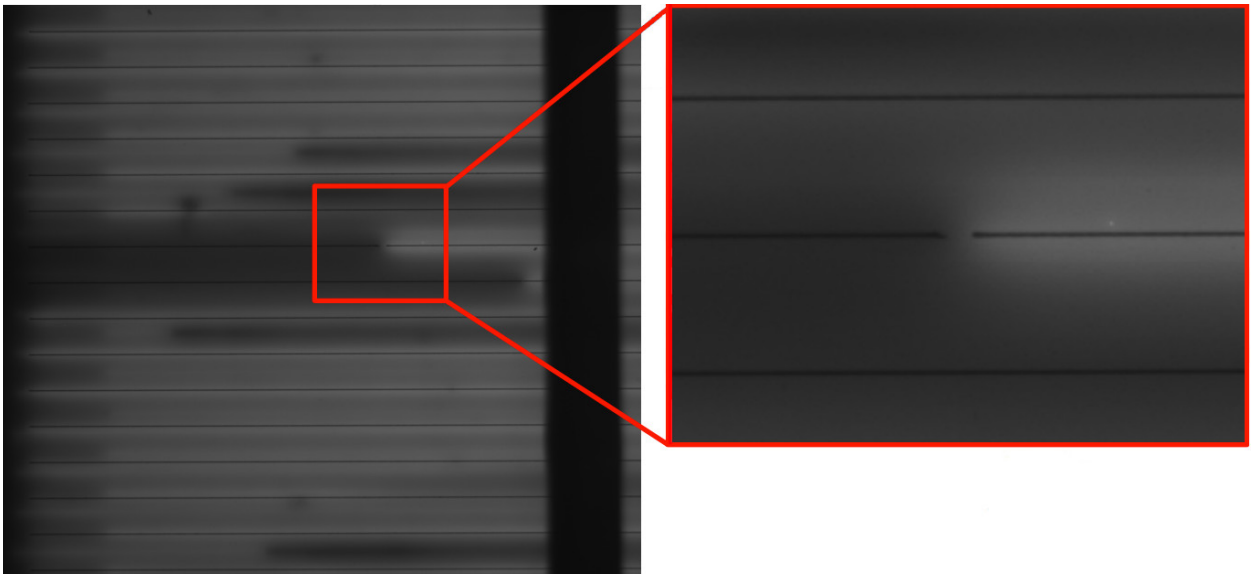


Figure 29. Zoomed in electroluminescence image of a metallization defect clearly showing the discontinuity.

For this case study, an optical inspection system is explored as a method to reduce the number of print defect in a production line. This system would be inserted following the screen print step. This metrology system would take a high resolution image of the cell and use a defect detection algorithm to identify the number of print defects. The system will momentarily pause the process and alert a technician if the number of defects exceeds a certain threshold. This will allow the technician to quickly clean or replace the screen. The goal of this metrology would be to reduce the overall number of metallization defects for a given manufacturing line.

For this metrology step, *M* refers to the number of print defects. *M* can be any positive integer and the distribution function will decrease with increasing *M*. In general, it is more likely that a cell will have fewer defects and is less likely to have a lot of defects. This type of distribution was achieved using a skewed Gaussian. To simulate the effects of process control, the distribution of *M* was altered for the test case so that there were fewer defects overall. This is shown in Figure 30.

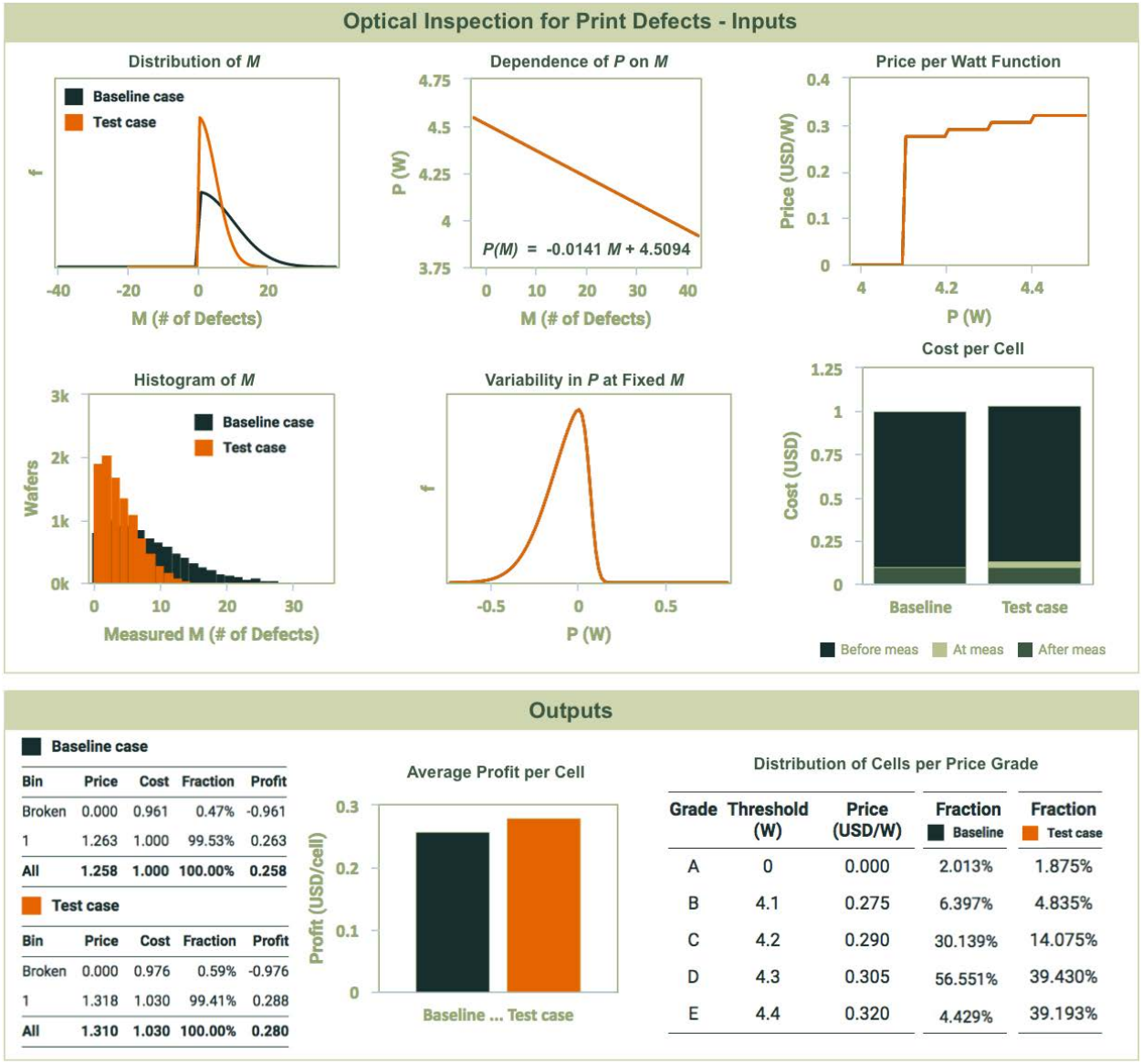


Figure 30. Relevant Input and outputs from the cost-benefit analysis for the use of optical inspection after the screen printing step.

The *P(M)* function was determined from device modelling. The basic assumption is that metallization defects impact series resistance directly. Using a 2-diode model, the efficiency was calculated over a range of series resistance values, while all other device parameters were held constant. This relationship is shown in Figure 31. For this study it was assumed that each defect

increases the cell series resistance by 0.05 Ω cm^2, and that lowest possible series resistance is 0.1 Ω cm^2 for a cell with no print defects. From this assumption, it was possible to determine the relationship between efficiency and the number of print defects. In reality, this relationship is likely more complex. Factors such as the defect location or severity may influence the extent of efficiency reduction. To establish a more reliable relationship, experimental data would be required. The efficiency was converted to power using the standard cell area of 243 cm^2 and a linear fit was applied to determine the coefficient: a = -0.0141 and b = 4.5094.

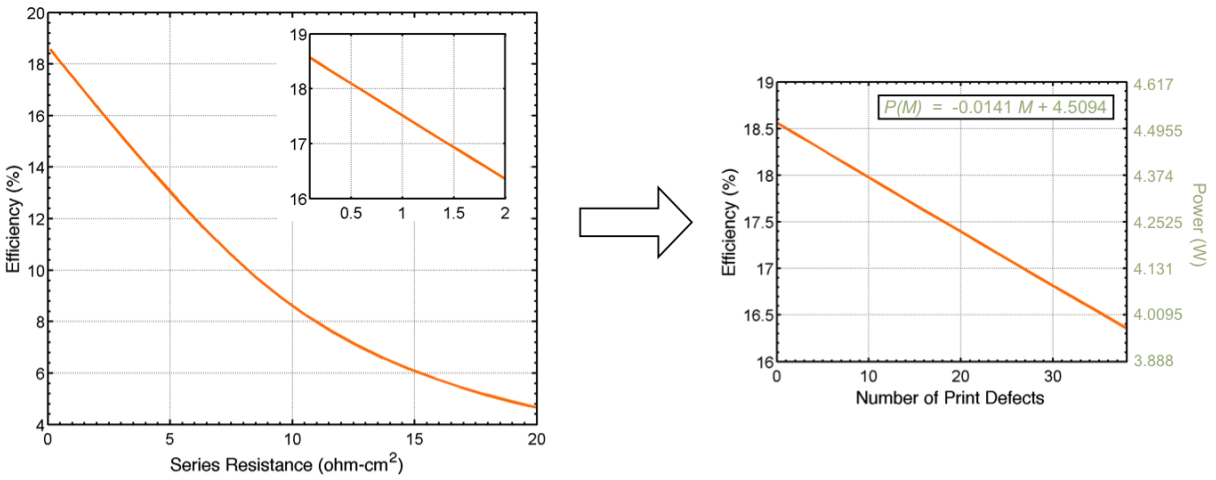


Figure 31. Relationship between cell efficiency and series resistance (left) with the range of interest highlighted in the inset. Assuming that each defect increases the series resistance by 0.05 ohm cm^2, the relationship between cell power and number of defects is determined (right).

The simulation was run using these assumptions with typical cost considerations as shown in Figure 30. It is important to realize this type of defect is not the only factor influencing cell efficiency. A skewed Gaussian was used to represent variation external to these metallization defect (*i.e.* Variability in *P* at Fixed *M*). Under these conditions, the economics favor the

introduction of this metrology tool. The assumption is that process control will reduce the maximum number of print defect to below ~15 defect per cell, with a majority of cell having between 0-5 defects. The baseline condition considered that cells could have as many as 30 defects. Because of this, the percentage of cells in the highest power bin went from 4.429% to 39.193%.

The economics will change as the level of process control is adjusted. To probe further one may ask what is the optimal distribution for these defects? To answer this several cases were investigated using the same inputs and varying the probability functions for *M*. The different distribution functions are shown in Figure 32(A). The profit per cell was determined in each case and the results are shown in Figure 32(B). From this approach we can see that there is a minimum amount of process control required to offset the cost of the metrology tool itself.

From this Figure 32(B) it appears that the level of process control should be increased as much as possible, because the profit continues to increase. This is potentially misleading. Implementation of this process control relies on a technician to stop the screen printer to address the issue. The more intervention required, the lower to overall utilization rate of the tool. This will lead to fewer cells produced over a given period. To model this, an exponential function is used to describe the relationship between the utilization rate as a function of the level of process control, as shown in Figure 33(A). Using the utilization rate and the profit per cell, a normalized average daily profit can be calculated. It is now apparent that there is an optimal range in which the economic impact is greatest. This range is highlighted in green in Figure 33(B).

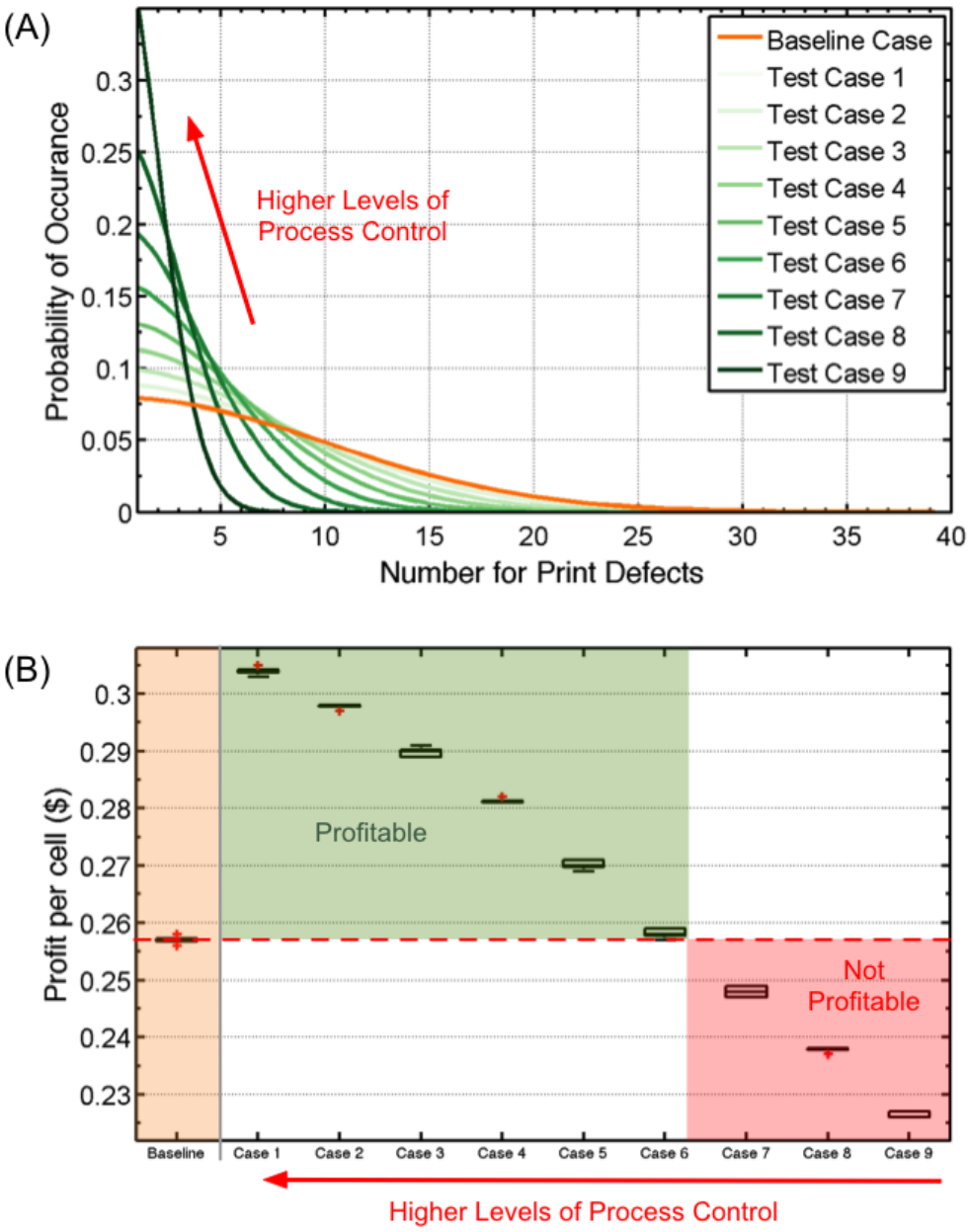


Figure 32. Cost analysis considering several variations in the distribution of M.

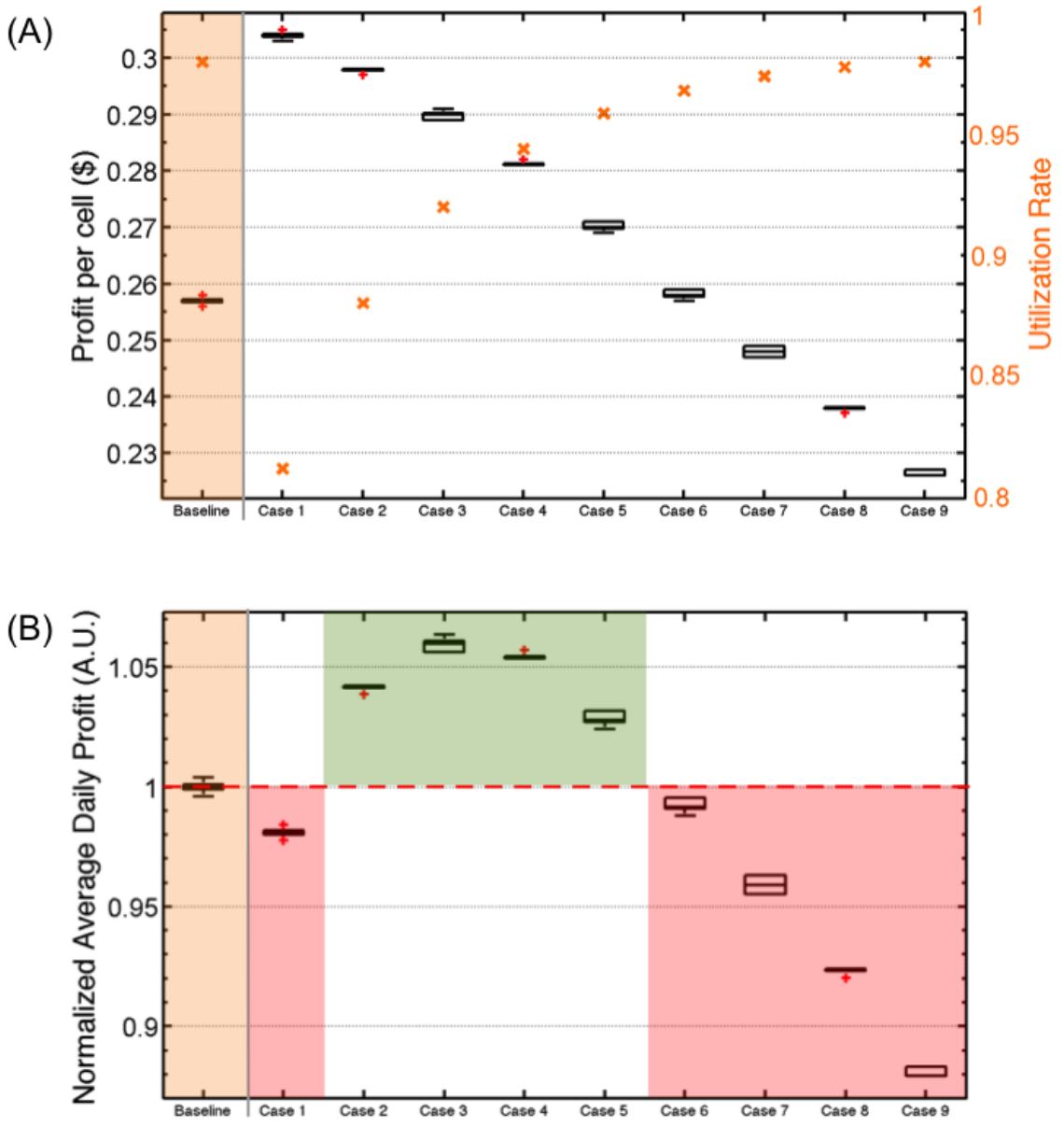


Figure 33. Cost analysis considering the influence of utilization rate (A) on the profitability of each process control case (B).

3.5 Conclusions

This chapter discussed the various ways that metrology can be used to add value to a production line. Quantifying the impact of this value in economic terms has been a challenge.

This work presented a methodology to assess metrology for specific applications in c-Si solar cell manufacturing. This methodology has been implemented into a free online calculator to make it easy for researchers and industry professionals to utilize. This calculator attempts to quantify any use of metrology that impacts the efficiency of the solar cell.

Several examples were explored to highlight the way in which the calculator could be used to answer questions regarding the economic viability of specific metrology scenarios. Wafer rejection using implied open-circuit voltage measurements was investigated in PERC manufacturing. By rejecting poor quality wafers before metallization, the cost associated with silver consumption could be avoided. It was identified that both the cost of the tool and the rejection threshold have a direct impact on the profitability. Optical inspection after metallization was also explored as a method to reduce process variation in the screen printing process. In this case, the metrology was used to reduce print defects and ultimately increase efficiency. It was noted that even if the average profit per cell increases, metrology that impacts the utilization rate (*i.e.* downtime) of specific process tools may have an economic penalty.

This work is intended to equip metrology suppliers and PV manufacturers with the tools required to make sound decisions regarding in-line metrology. This allows equipment suppliers to answer questions regarding the optimal measurement uncertainty or cost for a particular metrology application. For manufacturers this could be used to optimize economic value of existing metrology or to evaluate the potential value of new metrology.

CHAPTER 4: SPATIALLY RESOLVED CELL CHARACTERIZATION

4.1 Introduction

Characterization plays a key role in developing a comprehensive understanding of the structure and performance photovoltaic devices. High quality characterization methods enable researchers to assess material choices and processing steps, ultimately giving way to improved device performance and reduced manufacturing costs.

4.1.1 Quantum Efficiency Measurements

External quantum efficiency (EQE) is a metric derived from spectral responsivity measurement. Spectral Responsivity (*SR*) is a measurement of the current generated per incident power at a particular wavelength typically reported in A/W. From this, EQE is calculated using the charge of an electron (q) and the energy at that particular wavelength (hc/λ).

$$EQE(\lambda) = \frac{SR(\lambda)}{q}\frac{hc}{\lambda} \qquad (11)$$

A typical measurement set-up includes a broadband light source and a monochromator to select individual wavelengths. The EQE spectra is collected by measuring the short circuit of the device one wavelength at a time. To determine the incident photon flux, the measurement if first performed on a sample with a known EQE or, in some cases, simultaneously with the use of a beam splitter. This device is referred to as a reference cell. Because this measurement requires scanning across the entire wavelength range, it take several minutes to complete the entire measurement. This limitation has prevented measurements from being incorporated in-

line during manufacturing. Also, because the illumination spot size is typically only a few mm in diameter, there has been a lack of data as to the spatial variations of this measurement across large area devices.

Internal quantum efficiency (IQE) refers to the response of the device accounting only for light that has penetrated within the device. This requires correcting the EQE response by considering light that has been reflected off of the front surface of the device. This is accomplished through a measurement of diffuse reflectance, using an integrating sphere. Once both the EQE and the reflectance is known the IQE can be calculated at each wavelength. An example of EQE, IQE and reflectance data is shown in Figure 34 for a high quality monocrystalline *p*PERC cell.

$$IQE(\lambda) = \frac{EQE(\lambda)}{1-R(\lambda)} \qquad (12)$$

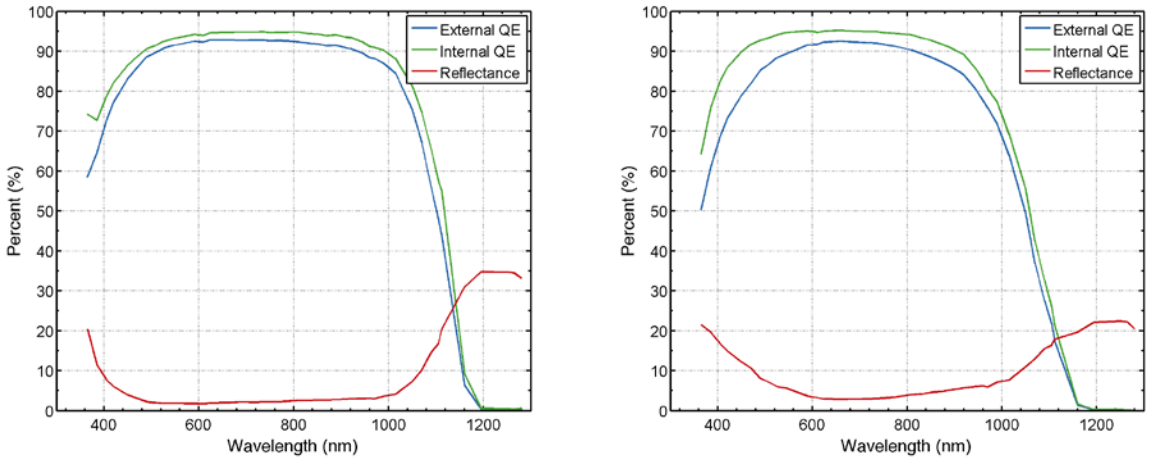


Figure 34. Example EQE, IQE and reflectance spectra for two cells monocrystalline PERC (left) and multicrystalline Al-BSF (right).

An example of EQE, IQE and reflectance data is shown in Figure 34 for a high efficiency (~20%) monocrystalline PERC cell and a lower efficiency (~16%) multicrystalline Al-BSF cell. QE measurements have long been a central tool in c-Si device development, providing valuable insight into critical performance parameters and material properties. Basore identified IQE spectra could be used to extract recombination parameters and light trapping details [33]. This analysis has been extended by others to evaluate additional device architectures and provide more accurate device parameters [34-38]. These analysis methods allow a quantitative determination of the base diffusion length ($L_{d,base}$), emitter diffusion lengths ($L_{d,emitter}$), emitter saturation current density ($J_{o,emitter}$), and the front and rear surface recombination velocities (S_{front}, S_{rear}) among others. These insights have led to the development of improved passivation layers, better light trapping structures and overall device improvements. Until recently, spectrally dependent QE characterization has been limited by the long measurements times and the lack of spatial resolution.

4.2 Luminescence Imaging

Luminescence is the emission of light through radiative recombination of excess charge carriers within the device. The carriers can be injected through either electric bias, known as electroluminescence (EL), or from illumination, known as photoluminescence (PL). In the base of the device, the luminescence intensity (I) as a function of the excess charge carrier distribution *n(z)* is given by Eq. (13)

$$I = \int_0^d w(z)n(z)dz \qquad (13)$$

Here, *z* represents the spatial coordinate in one-dimension perpendicular to the cell surface, *d* is the thickness of the base, and *w(z)* the probability that a carrier recombines radiatively and the emitted photon escapes from the cell. It has been shown by Glatthar *et al.* that the excess charge carrier distribution is proportional to the exponential of the local voltage *V(x,y)[39].* In this way the intensity of any pixel *I(x,y)* under electrical bias is represented by Eq.(14)

$$I(x,y) = C(x,y)\, exp(\frac{V(x,y)}{V_T}) \qquad (14)$$

where *C(x,y)* represents a constant that is dependent on the shape of the excess carrier distribution as a function of depth which is impacted by surface recombination velocities and the bulk diffusion length. Under illumination an additional constant is need to describe spatial variations in the generation current B*(x,y)* at a particular illumination intensity I_L.

$$I(x,y) = C(x,y)\, exp\left(\frac{V(x,y)}{V_T}\right) + B(x,y)I_L \qquad (15)$$

Using these basic equation, luminescence images can be converted to maps of local voltage. When a simple diode model is applied to each pixel, additional parameters such as local series resistance and local recombination currents can be determined [40-46]. For these methods both electrical bias and illumination are required and is often referred to as biased-PL imaging.

Illumination can also be used to stimulate luminescence in wafers than have no electrical contacts. This provides a powerful non-contact method to evaluate bulk wafer properties and passivation quality. When combined with photoconductance, techniques have been developed to calibrate photoluminescence images for passivated wafers in order to map effective diffusion length ($L_{d,eff}$) and implied open circuit voltage (iV_{oc}) [47-49].

The energy of the photons emitted depends on the band-gap energy of the semiconductor. For Silicon this corresponds to 1.12eV. This NIR light can be captured using a Silicon CCD camera, however, the efficiency of collection in this energy range is relatively poor, requiring extended exposures. InGaAs detectors can be used to reduce exposure times, however these cameras are often much more expensive. If a silicon CCD is used, a filter must be used to block any light that may be reflected off of the cell from the illumination source. Typically, an 808nm laser diode is used as the excitation source and a 1000nm filter is used. PL characterization using variable wavelength excitation have so far been limited to single point measurements with a lack of spatial resolution [50-52].

4.2.1 Luminescence Imaging for Defect Detection.

As described by Eq. (14), luminescence images are generally related to the local voltage, which is affected by both resistive and recombination processes. In this way qualitative assessments have been used to spot a variety of process related defects. Figure 35 shows examples of several types of defects impacting cell performance. Although these images are only qualitative in nature, it is possible in many cases to identify the source of the spatial non-uniformity. For example, the pattern shown in (e) is typical of the variation in the local temperature cause from the belt that carries the cell during the firing process

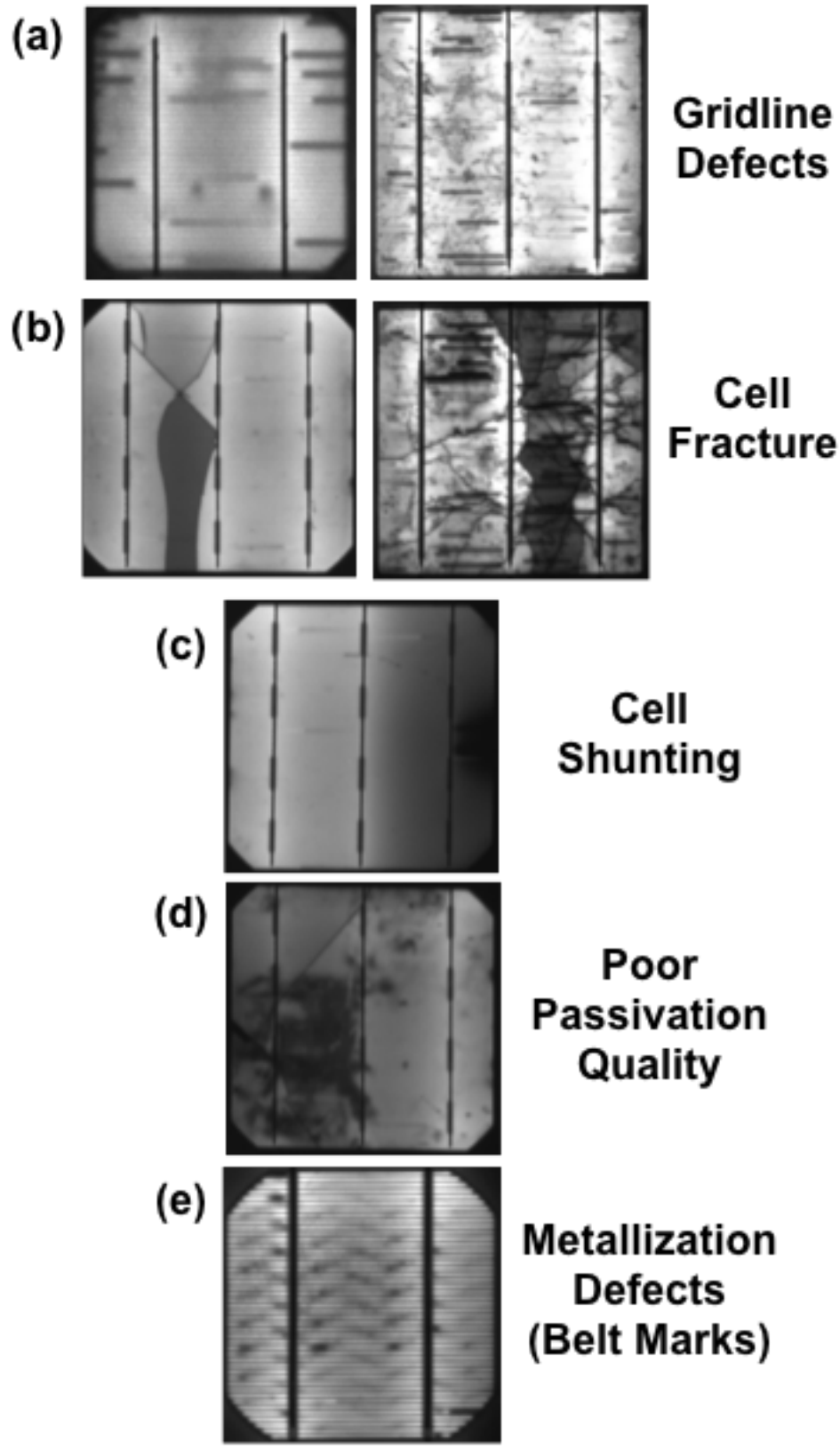


Figure 35. EL images exhibiting various spatially resolved defects impacting performance.

Although qualitative measurements are useful, understanding the impact of a particular defects is particularly critical when allocating resources to address a problem in manufacturing. As discussed above, by collecting luminescence images under a range of illumination and bias conditions the extract of calibrated parameter images is possible.

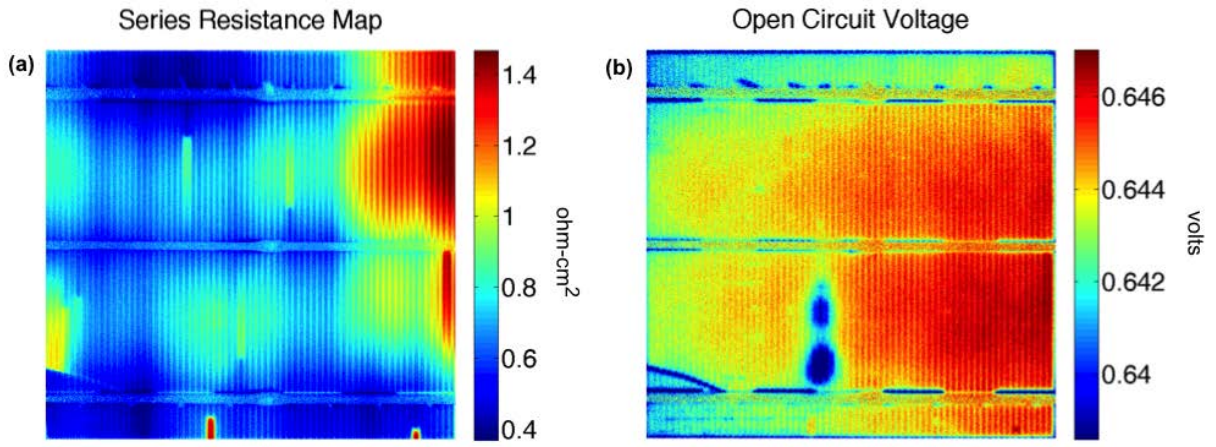


Figure 36. Parameter maps derived from PL imaging.

By applying the diode model to each pixel, quantitative details can be extracted. As shown in Figure 36, this allows us to decouple the effects of series resistance from recombination effects resulting in two very different images. In Figure 36 (a), the metallization defects (*i.e.* discontinuities) described in Section 3.4.1 can now be quantified in terms of their direct impact on the local series resistance. In this cell, there also appears to be variations in the emitter sheet resistance causing more gradual changes in series resistance across the device. From the open-circuit voltage map in Figure 36 (b), a circular defect is identified near the center of the device. This defect has a significant impact on open circuit voltage, but not on series resistance indicating that this is an area of relatively high recombination.

PL and EL imaging are valuable methods that provide details on the spatial uniformity of device performance. Because these are an imaging based technique, it can be performed in only a few seconds opening up opportunities for in-line characterization. To perform more detailed analysis, including extraction of local series resistance or voltage, a series of images is required. This more advanced analysis is better suited for off-line characterization. These methods have proven to be very reliable for investigating resistive and recombination related defects and inhomogeneities. These methods do not provide any details regarding the spatial variation in the generation current. To investigate current related device properties, techniques other than luminescence imaging are required, this will be discussed in the next section.

4.3 Quantum Efficiency Mapping

4.3.1 Measurement System

To overcome the limitations of traditional EQE/IQE measurement systems, an approach using light emitting diodes was developed. In this case each diode represents a single wavelength. This eliminates the need of a mechanical monochromator to isolate individual wavelengths from a broadband light source. Additionally, a Fourier transform approach, similar to what is used in Fourier transform infrared spectroscopy (FTIR), can be used to measure the response of the device from all LEDs simultaneously. This technique was commercialized by Tau Science as the FlashQE measurement system [53].

This system used in this work utilizes an array of 41 independent LEDs representing 41 different wavelengths. During a measurement all LEDs illuminate the cell simultaneously, while each LED is modulated on and off at a unique frequency. During illumination, the current

response of the cell is measured as a function of time. A fast Fourier transform is performed on the time-domain measurement data to convert the data into the frequency-domain. By correlating each modulation frequency to its associated LED, the current response resulting from each LED can be determined. This process takes approximately 1 second for each measurement. The illumination spot size is 4mm in diameter and the light engine is attached to an X-Y gantry capable of measuring any site on a 156 x 156 mm solar cell. Light bias up to 0.2 suns is possible on an area approximately 5 cm in diameter surrounding the location being measured. In addition to the EQE, an integrating sphere is attached to the gantry enabling simultaneous measurement of diffuse reflectance. The system is shown in Figure 37. An average QE spectrum is obtained by taking the spatially resolved average, excluding edge regions and busbars.

Because the spot size is generally larger than the spacing between gridlines, it is essential to maintain consistency in the shaded fraction for each measurement. Because of this constraint, the step size is typically equivalent to the gridline spacing to simplify the analysis. Generally, the gridline spacing for commercially screen printed silicon solar cells is near 2mm [54, 55], leading to minimal overlap between the illumination area of two adjacent spots.

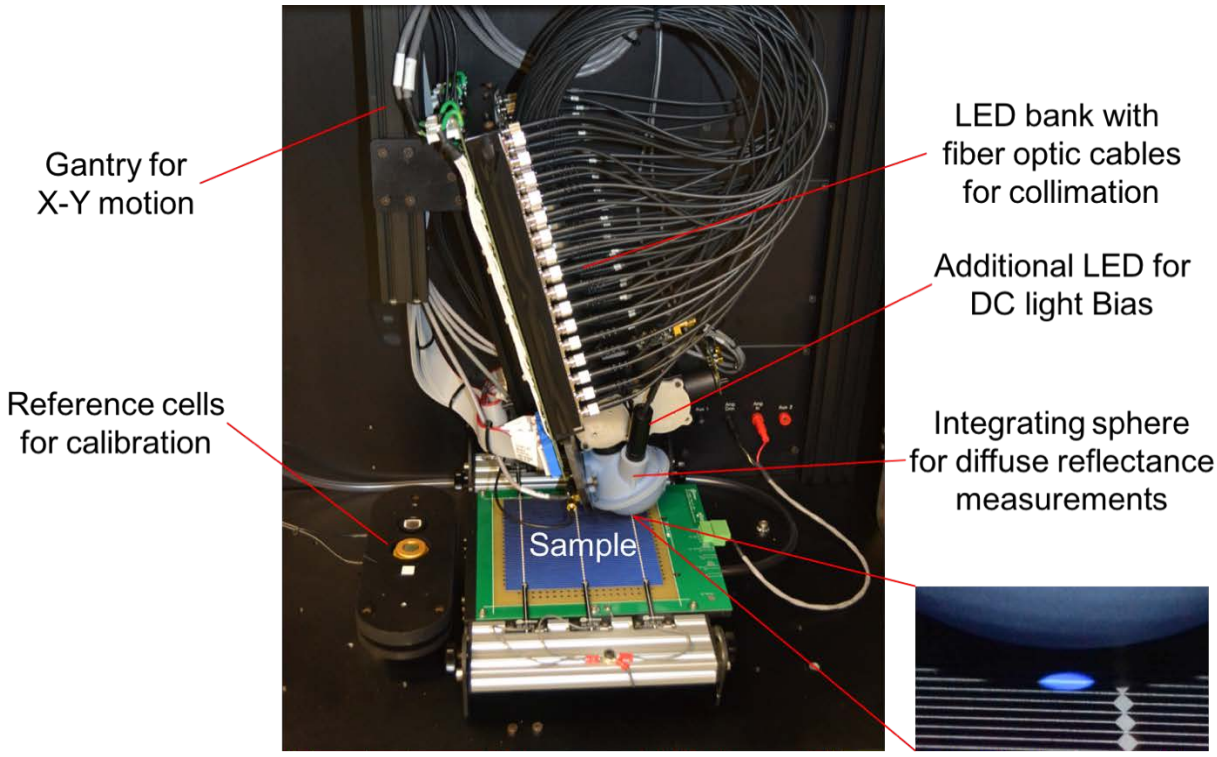


Figure 37. FlashQE Measurement System

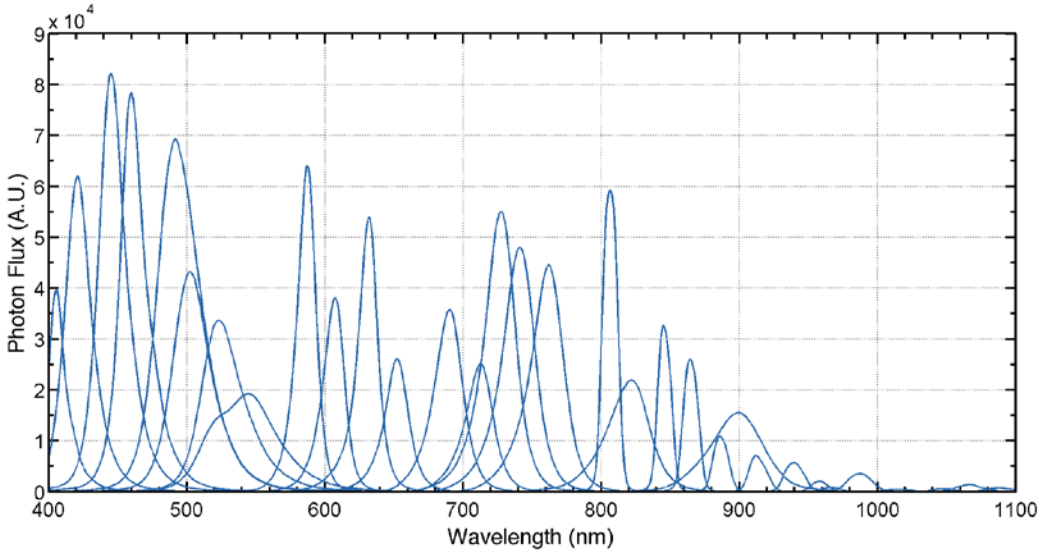


Figure 38. Spectra of LED's in the FlashQE system.

Measurement errors may arise when using a non-monochromatic light source such as an LED. A discussion of the influence of measurement related uncertainty is provided in Section

4.3.6. The spectra of each LED is unique in terms of its maximum intensity and full width at half max, with some LEDs exhibiting asymmetric intensity profiles. To increase the intensity of lower power LED, specifically in the NIR region, multiple LEDs can be used. Additionally, in cases where there may be multiple peaks within the LED spectra band pass filters were used. The spectra for many of the LEDs in this system are shown in Figure 38.

A large focus of this work was to convert the raw data provided from the FlashQE system into actionable information. Because of the large amount of data, translating this into simple metrics that govern device performance is required to effectively use this in a manufacturing environment. As an example, Figure 39 shows the EQE and reflectance maps for 3 of the 41 possible wavelengths. From this figure it is evident that the response of the cell exhibits variations in the patterns as a function of wavelength. What is unclear from these images is what caused these variations and what is their influence on the device performance. The remainder of this section will focus on answering these questions.

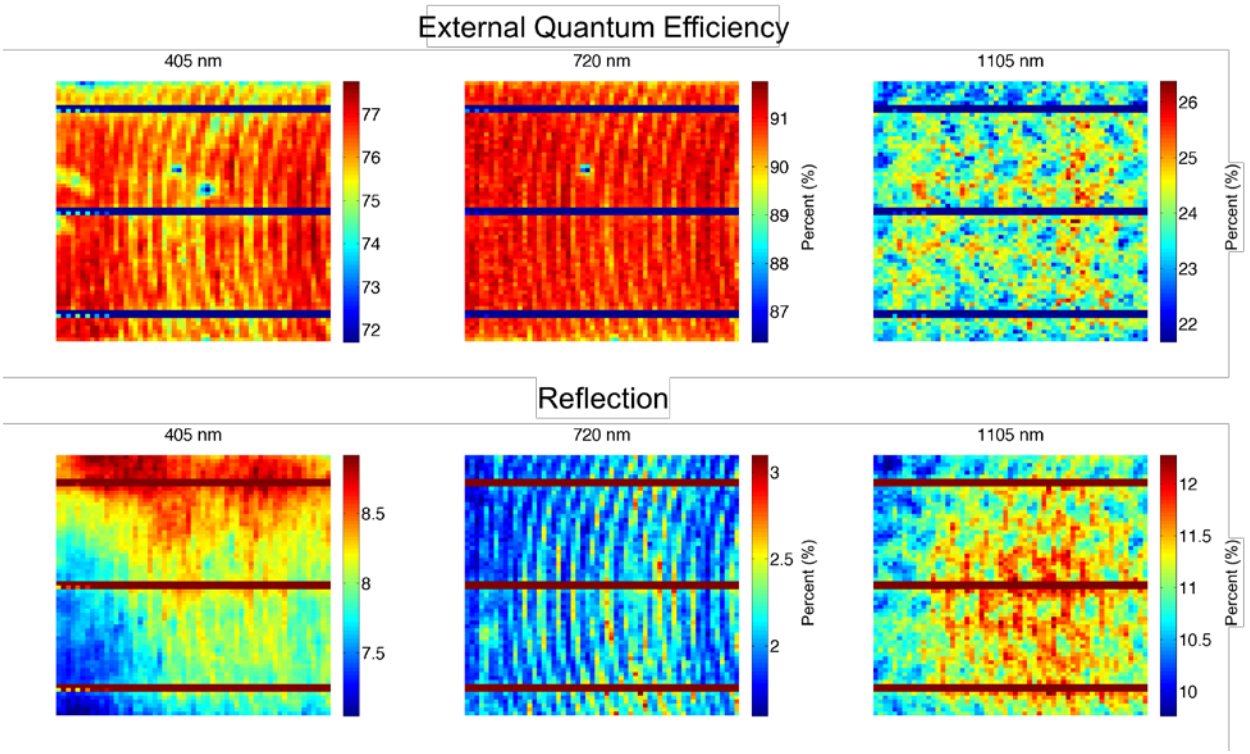


Figure 39. EQE and reflectance maps of one cell at several wavelengths.

4.3.2 Quantification of Loss Mechanisms

Quantifying the various photon interaction mechanisms within the cell is fundamental to evaluating where improvements in device design can be made. Typically, optical losses are separated into front surface reflection loss, parasitic absorption in the ARC, emitter, bulk, and rear surface, and front surface escape. These mechanisms represent various losses that limit the total generation current within the device. Often these losses can only be separated by device modelling or ray-tracing methods [36, 37, 56]. In this work we employ simple data analysis techniques that use reflection, EQE and IQE spectra from finished cells to decouple the various loss mechanisms, with the goal of applying these techniques to visualize spatial variations.

The first step in the analysis process is to quantify the spatial variation of each data set. A simple, yet powerful, method to visualize this data is to transform the EQE dataset into a single value of short-circuit current density (J_{sc}) using Eq. (16).

$$J_{sc} = \int SR(\lambda) * I_{AM1.5}(\lambda) d\lambda \qquad (16)$$

$SR(\lambda)$ denotes the spectral responsivity of the device as a function of wavelength and $I_{AM1.5}(\lambda)$ denotes the intensity of the standard air mass 1.5 solar spectrum as a function of wavelength. Because the measurement is performed at only a selected number of wavelengths, as defined by the specific LEDs in the system, the EQE at intermediate wavelengths is determined through linear interpolation. The wavelength range over which this integral is defined can be used to distinguish the current contribution resulting from a defined spectral region.

In addition to analyzing EQE, the spectral responsivity can be replaced with a similar term representing the spectrally resolved loss mechanisms such as reflection or parasitic absorption. This results in a current density value that represents an effective loss in generation current due to each mechanism.

When Eq.(16) is used to calculate the generation current from EQE data, the limits of integration are defined from zero to ∞. When this equation is used to calculate loss in generation current, the limits should be defined to account only for photons that could potentially contribute to current generation. For this case, the lower bound would be where the solar spectrum drops to zero and the upper bound would be when the absorption length in silicon is much larger than the cell thickness, generally near 1200nm. For this work, limits are defined by a lower bound of

365nm, set by the shortest wavelength LED, and an upper bound of 1195nm as a reasonable approximation of the maximum wavelength at which photons will be absorbed in the cell. The wavelength of 1195nm was selected as this was the closest LED to 1200nm available in this system, although there are three additional LEDs above 1200nm (1250nm, 1265nm, 1280nm). The total available current in this spectral range (365-1195nm) is 45.667 mA/cm^2.

It is instructive to first identify the loss due to shading which is considered to be constant across the entire spectrum. It should be noted that there is a difference in the geometrical shaded fraction and the effective (optical) shaded fraction depending on the surface profile and reflectivity of the metallic gridlines. For typical screen printed silver gridlines the effective shaded fraction, in terms of percentage of the geometrically determined value, can be as low as 35% for encapsulated cells and is typically near 70% for unencapsulated cells [57-59]. When considering evaporated metallic contacts on the other hand, the effective width of gridlines is assumed to be equivalent to the geometric width because of their uniform thickness and flat surface profile. This effect may also be dependent on the incident angle of the incoming light, however for this work the light is maintained as normal to the surface of the cell. Once the effective shaded fraction is determined, this parameter is considered constant across the cell. A cross sectional SEM image of a screen printed gridline is shown in Figure 40.

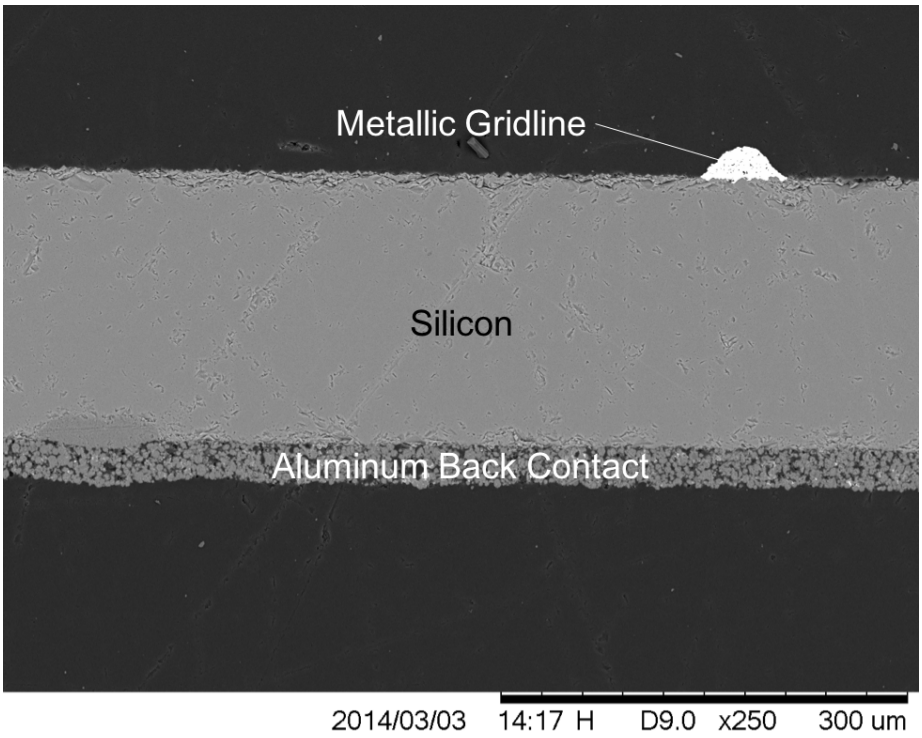


Figure 40. Cross Sectional SEM of monocrystalline PERC device

Next, the reflectance measurements are corrected to eliminate the influence of reflectance from the metallic gridlines. To determine the reflectance of metallic gridlines from a finished cell, a series of reflectance measurements are made with varying metal fractions. For each wavelength, a plot of reflectance vs. metallic fraction is created and a linear fit is applied. The value of metal reflectance is determined from the intercept of the fit with 100% metallic fraction. Using this value, along with the geometrically determined shaded fraction, the reflectance data at each measurement location is corrected using the following equation:

$$R_{active} = R_{meas} - R_{metal} f_{metal} \qquad (17)$$

R_{active} is the corrected reflectance of the active area, R_{meas} is the measured reflectance, R_{metal} is the metal reflectance, and f_{metal} is the geometrically determined metal fraction. IQE can then be calculated from Eq. (18) using the measured EQE, the corrected reflectance, the effective (optical) shaded fraction (f_{eff}), and the absorption in the ARC (A_{ARC}).

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - f_{eff} - R_{active} - A_{ARC}(\lambda)} \qquad (18)$$

In the following analysis, the absorption in the ARC is set to zero because additional knowledge is required, such as the thickness and index of refraction of the ARC. This leads to a relatively small uncertainty in the short wavelength region of the IQE. It was suggested by Fisher *et al.* that the ARC absorption can be determined by choosing an $A_{ARC}(\lambda)$ spectra that results in the short wavelength range of the IQE (below 380nm) to be constant [60]. For the instrument used in this study there is only one LED with a wavelength in this range at 365nm. The instrument could include additional LEDs in this low wavelength regime in order to utilize this approach.

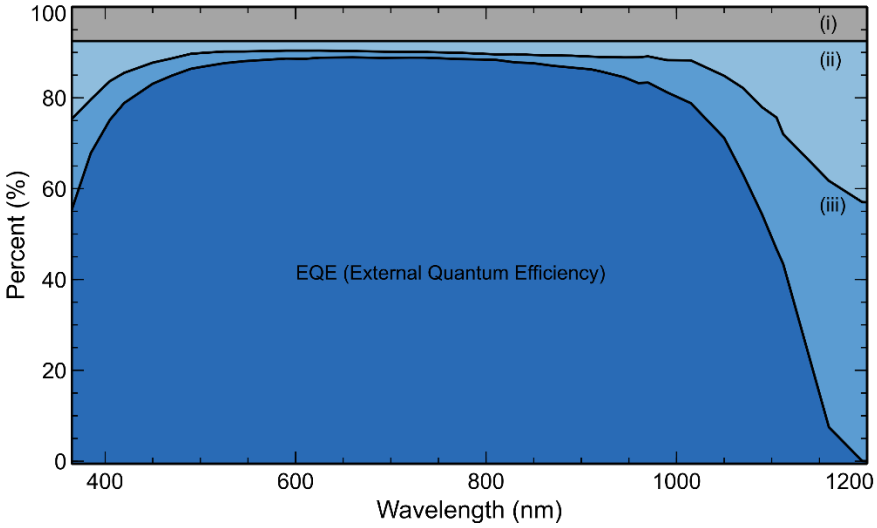


Figure 41. EQE of a high quality monocrystalline pPERC

The space between the EQE curve and 100 percent can be broken down into the various spectrally dependent loss mechanisms as shown in Figure 41. These losses include shading (i), reflectance (ii), and parasitic absorption(iii). Parasitic absorption refers to any light that is absorbed within the cell that does not contribute to the short circuit current. This may be due to optical loss (e.g. absorption within the metal at the back surface) or collection losses due to less than ideal diffusion lengths in both the emitter and in the base of the cell. The remainder of this section focuses on the techniques used to isolate the spectrally dependent loss mechanisms. The analysis is intended for typical *p*-type c-Si devices with a front junction, although some aspects may apply to other device architectures. The following analysis considers only the active area of the cell through a normalization of the EQE data using the effective shading fraction. Additionally, only the active area (i.e. corrected) reflectance is considered beyond this point.

Cell reflectance data (R_{active}) regularly deviates from the predicted ARC reflectance (R_{ARC}) in the long wavelength range due to escape reflectance (R_{escape}). This consists of light that passes through the cell, reflects off the back surface, passes back through the thickness of the cell, and

exits the front surface. The wavelengths that contribute to this behavior are dependent on the front surface texture, cell thickness, and the rear surface properties. In this work the impact of this behavior is determined through a linear extrapolation of the reflectance data beyond 950 nm. Any additional reflection above this linear extrapolation is attributed to escape reflectance.

The remaining region between the reflectance spectra and the EQE is attributed to parasitic absorption. This parasitic absorption can be further separated into emitter, bulk, and rear surface effects. Absorption in the shorter wavelength regime is generally attributed to emitter losses, and in the longer wavelength regime is attributed to bulk and rear losses. Although a simple method of attributing all losses below a predefined wavelength to emitter loss can be qualitatively useful, a more comprehensive method was proposed by Fisher *et al.* [60] For this method the emitter is modelled as a hypothetical dead layer with a thickness Wd. It is important to note that this does not correspond to the physical dead layer described in other experimental work resulting from excessive phosphorus doping [61]. This model assumes all photons generated in this "dead layer" do not contribute to current generation. In essence, it is saying that when generation is homogeneous within the emitter, a constant fraction of generated carriers within the emitter will recombine and not contribute to the short circuit current. This model can be used to describe the measured IQE data over relatively wide wavelength range according to the following equation.

$$IQE(\lambda) = \frac{1}{k} exp(-\frac{W_d}{L_\alpha(\lambda)}) \frac{1}{1+L_\alpha(\lambda)/L_{eff}} \quad (19)$$

Here L_{eff} represents the effective diffusion length in the base, $L_\alpha(\lambda)$ the absorption length, and k a scaling factor. The absorption length is often corrected by $\cos\theta$ to account for surface texture. For random pyramidal texturing, this angle is assumed as 54 degrees. The reader is referred to other works that discuss how the geometry of the surface texture impacts the angle at which light travels through the cell [62, 63]. A more rigorous approach would be to use ray tracing methods to define an absorption length for each wavelength that consider all possible light paths as opposed to only the most dominant. For this work a simple $\cos\theta$ correction was used and when referring to absorption length, this correction is assumed. The model described by Eq. (19) is a good approximation when the absorption length is large enough to consider generation within the emitter as uniform, and small enough to exclude the influence of rear surface effects. For standard monocrystalline cells with random pyramidal texture and a thickness of 180 μm this will correspond to the range of wavelengths between 500nm and 900nm.

A simple iterative process is used to extract W_d, L_{eff}, and k starting with nearly any estimation of L_{eff}. The slope and intercept of the plot $ln\,[IQE*(1+L_\alpha/L_{eff})]$ vs. $1/L_\alpha$ provide values for W_d and k. These values are used to plot $IQE^{-1}*exp\,(W_d/L_\alpha)$ vs. L_α which in turn provides values for L_{eff} and k. After a few iterations a consistent set of W_d, L_{eff}, and k are found. It should be noted that the second plot is an extension of the classical method for the determination of the effective base diffusion length presented in the work of Basore [33]. In this modification, the inverse IQE is corrected for emitter loss enabling a broader range of applicable wavelengths, as shown in Figure 42, which results in a more accurate determination of L_{eff}.

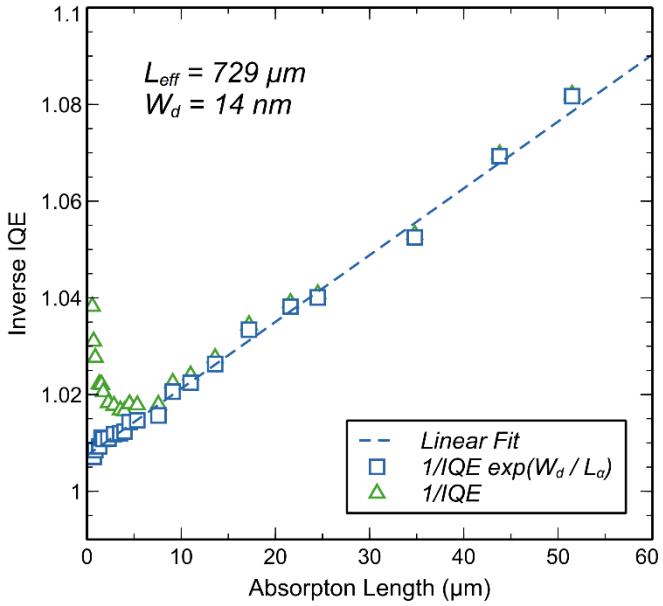


Figure 42. Inverse IQE as a function of absorption length in a mono-crystalline pPERC cell.

The scaling factor *k* was introduced by Fisher as a method to correct deviations in the measured IQE, independent of wavelength, resulting from a number of experimentally introduced factors [64]. For this work it was identified that if the procedure to account for the reflectance and effective shading of the metallized region was applied correctly, the experimentally determined scaling factor was consistently in the range of 1±0.02 and had very minimal spatial variation.

With these variables it is now possible to decouple loss in the base versus loss in the emitter. The contribution of parasitic emitter absorption is calculated using two discrete regimes. The first regime, where the dead layer approximation is inadequate, we can assign emitter loss using a small correction to the measured IQE for base loss using Eq. (20). In the second regime, for which the dead layer approximation is reasonable, the emitter loss is defined by Eq. (21). These two losses are joined at 500nm for a standard monocrystalline cell with random pyramidal texture.

$$A_{emi.loss,I}(\lambda) = 1 - IQE(\lambda) * (1 - L_{\alpha}(\lambda)/L_{eff}) \quad (20)$$

$$A_{emi.loss,II}(\lambda) = 1 - exp(-W_d/L_{\alpha}(\lambda)) \quad (21)$$

The remaining parasitic absorption is associated with loss in the base of the cell, which account for both bulk and rear surface effects. Although methods have been proposed to separate these effects, they often require complex optical models and device modeling. Although this is possible in principle, it does not lend itself to fast numerical calculations that can be applied to each point in this spatially resolved analysis. This extension may be explored in future work.

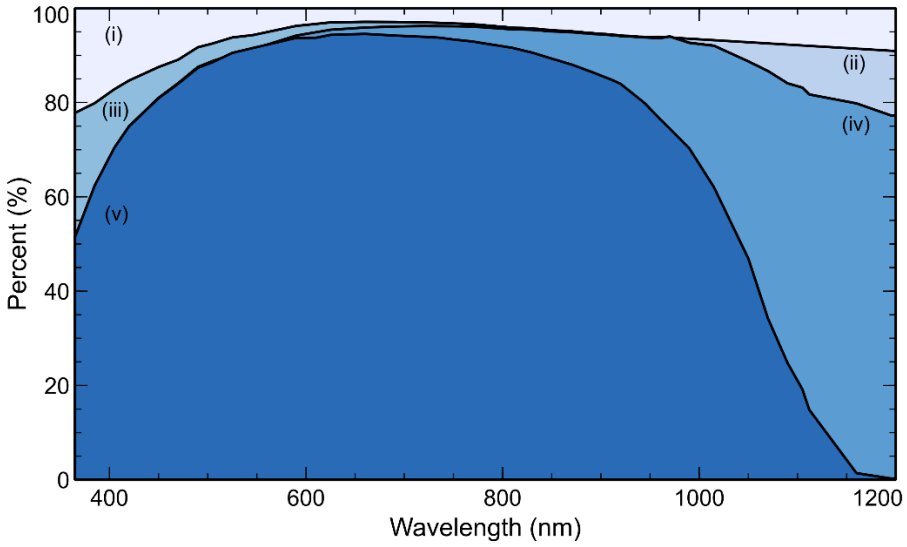


Figure 43. EQE of a multicrystalline Al-BSF cell with several loss mechanisms identified.

The analysis presented in this section allows for the separation of four basic current generation loss mechanisms shown in Figure 43. These include front surface reflectance (i), escape reflectance (ii), emitter loss (iii) and base (combination of bulk and rear) loss (iv).

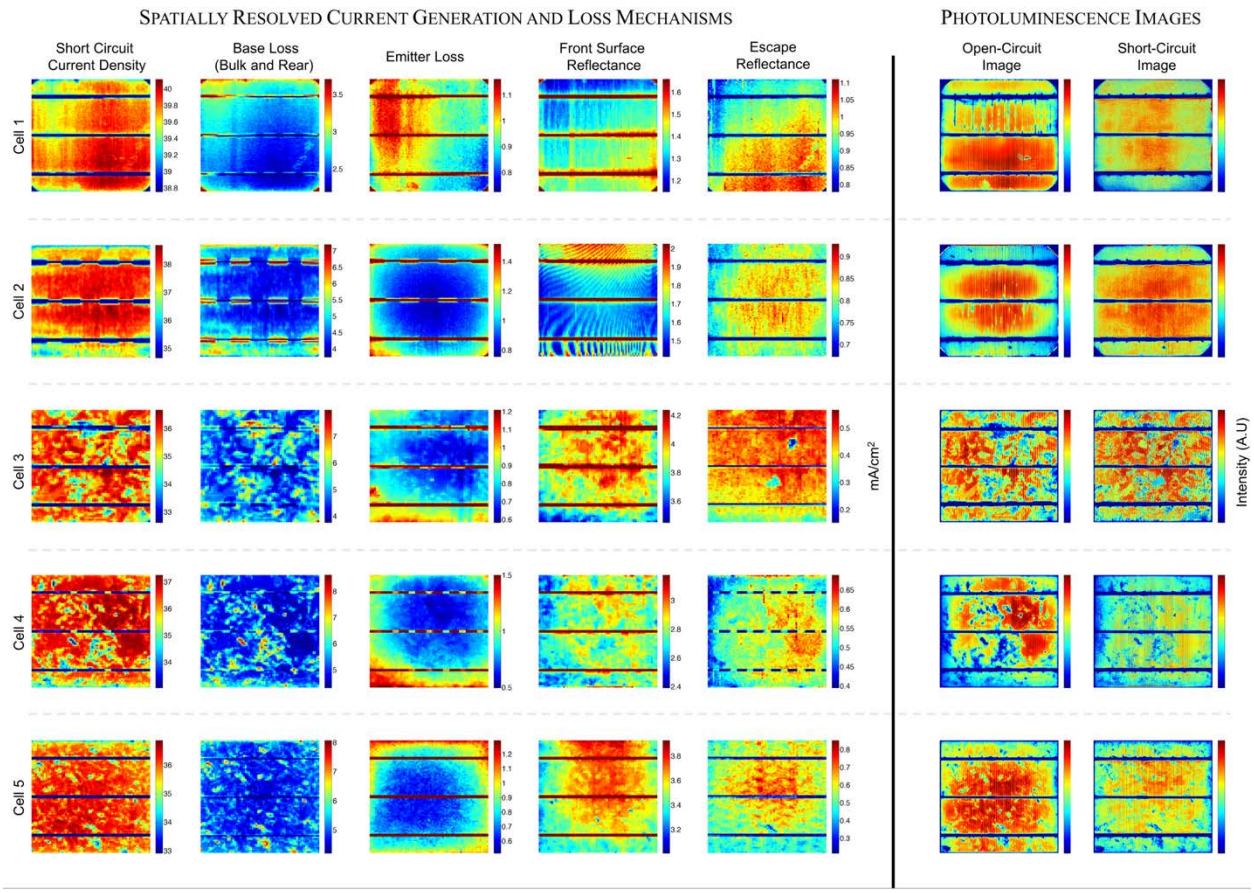


Figure 44. Spatially resolved J_{sc} along with each of the current loss mechanisms measurements for five cells.

4.3.3 Spatially Resolved Current Loss Analysis

The analysis described in the previous section was applied to several cells as shown in Figure 44. This figure displays a short-circuit current density map along with maps for each of the short-circuit current loss mechanisms discussed above. For comparison the open-circuit and short-circuit photoluminescence images were taken under 1 sun illumination for each of the corresponding cells.

The cells were fabricated at different processing sites to highlight the breadth of knowledge that can be gained using this analysis. These images provide valuable insights on how

the various processing steps impact current generation in the cell. This section will discuss the various features that were identified and how these features impact performance.

Loss in the base was identified to be the dominant loss mechanism in all cases. Not only is the magnitude the largest (in terms of mA/cm^2), but the current generation map is nearly an inverse image of the loss in the base of the cell. This implies that a map of short-circuit current alone will not clearly distinguish other factors impacting current generation such as front surface texture, ARC uniformity, emitter uniformity, or rear surface optics.

In industrially produced *p*-type solar cells, the emitter is generally formed with a high temperature drive-in process using a large diameter tube furnace and $POCl_3$ gas as the phosphorus source. In this scenario, it is reasonable to assume the edges of the cell will reach temperatures slightly higher than those seen at the center of the cell. These higher temperatures will result in higher diffusion coefficients and higher concentrations of phosphorus in the cell. These higher concentrations, although beneficial in the reducing the sheet resistance, lead to higher recombination rates and lower carrier lifetimes within the emitter. This trend was observed in cells 2-5 as shown by the circular pattern in the emitter loss maps. These maps imply that when the number of carriers generated in the emitter are the same, fewer carriers will diffuse across the junction and be extracted near the edge of the cell. The magnitude of this difference in the worst case is approximately 1 mA/cm^2 (cell 4), but otherwise is in the range of 0.5-0.8 mA/cm^2. It is interesting to note that this circular pattern is also seen in several of the open-circuit photoluminescence images. In particular cells 4 and 5 show distinctly similar circular regions alongside the grain-to-grain variation in the PL images, where higher PL intensity corresponds to the more lightly doped regions.

Reflection off of the front surface of a cell is governed by the front surface texture and the properties of the ARC film. For monocrystalline wafers an alkaline texturing process is used to create a random array of pyramidal structures on the surface. This process is generally very uniform, resulting in only minor variations over the cell area. Multicrystalline wafers require an alternative approach because each grain will have a unique orientation. For this, an isotexture approach is used that creates a structure resembling inverted semi-spherical caps. The effectiveness of this process will vary from grain to grain. This is evident in the maps for front surface reflectance loss on cells 3-5 as the grain structure of the wafer remains the dominate feature in these images.

The amount of current loss due to front surface reflectance in the multicrystalline cells is nearly double the loss observed in the monocrystalline cells. For the monocrystalline cells with adequate texturing, the spatial variation of the ARC could become the dominate factor influencing front surface reflectance. This is very clear in the case of cell 2 where a non-optimized PECVD process lead to a unique pattern across the cell. This pattern, which is visible to the eye, affects the local reflectance (and subsequently the J_{sc} of the cell) by approximately 0.5 mA/cm^2. It should be noted that PL images of this cell fail to identify this defect. This is likely due to the fact that the PL image is illuminated using a single wavelength excitation, in this case 808 nm. The variation in reflectance at 808 nm may be negligible, whereas the influence of this variation when aggregated over the entire spectrum may be significant in terms of current generation.

Examination of the escape reflectance maps can provide us information in regards to the rear side optics. For example, cell 3 shows us a very low escape reflectance in two grains near the center of the cell. In this case it is likely that a large fraction of light incident on the rear surface

is being absorbed within the aluminum as compared to other regions of the cell. This could be a result of a unique interaction between aluminum and silicon at that particular grain orientation, or it could be that the rear side texture of those grains is affecting the optical properties of the aluminum-silicon interface. Additionally, cell 5 exhibits a traditional belt mark pattern caused by variation in the local temperature of the cell during firing of the rear side metallization.

The maps derived in this work provide a complementary dataset to PL images that provide insights while quantifying the impact and identifying the root cause of various defects. Cell 1 is a great example of this. A series of PL images were taken for this cell and the procedure defined by Glatthar *et al.* was followed to extract parameter maps of series resistance, open-circuit voltage, and dark saturation current as shown in Figure 45.

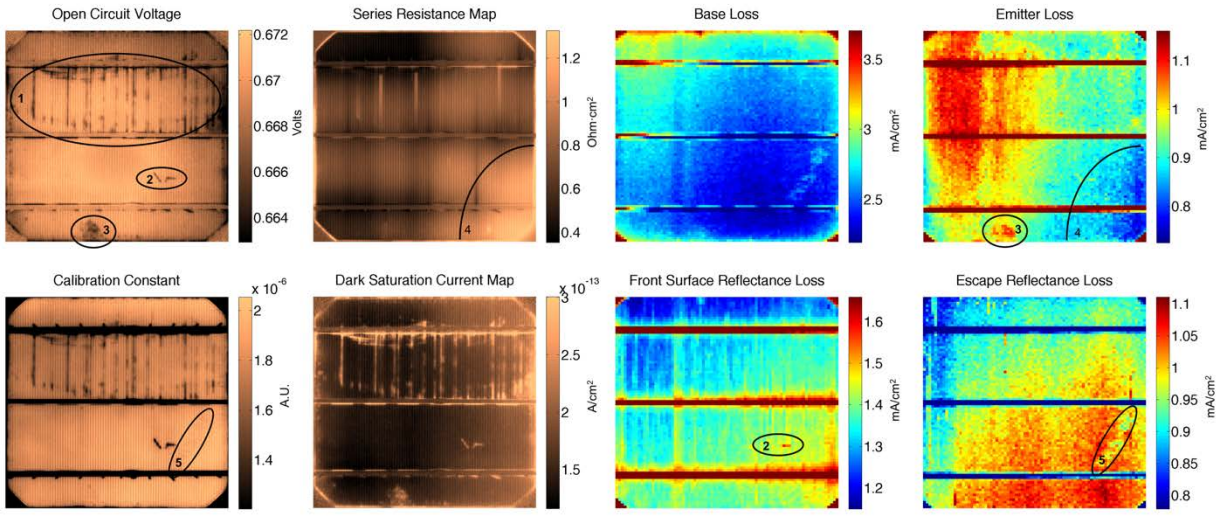


Figure 45. Comparison of defects using both photoluminescence imaging techniques and spatially resolved current loss analysis.

There are several defects identified in the biased PL images in Figure 45 which can be better understood by looking at the corresponding regions of the current loss images. Feature 1 is a large area of line type defects that are not present in the series resistance map or any of the

current loss maps. These defects are likely voids at the local back contacts leading to recombination under open-circuit conditions [65]. Feature 2 is present in the front surface reflectance map, clearly showing this is a defect or scratch on the front surface of the cell. Feature 3 is visible in the emitter loss map, suggesting that there is a defect near the front surface of the cell limiting the emitter diffusion lengths in this area. Feature 4 represents the lower right region of the cell in which the series resistance is relatively higher. This region corresponds to the same region in which there is a lower emitter loss. As discussed above, reduced emitter loss could be a result of a lower doping concentration. This lower doping concentration would also result in a higher sheet resistance in the emitter, increasing the local series resistance in this area. Finally, feature 5 is faintly identified in both the standard open-circuit PL image as well as in the calibration constant map. This feature is most prominent in the escape reflectance image, suggesting this is a defect on the rear side of the cell impacted the quality of the passivation layer. This was in fact verified as a sample marking on the rear side of the cell.

This analysis highlights the value of current loss mapping, in conjunction with PL imaging techniques, to diagnose problems within the cell. Not only do the images identify the potential root-cause of a defect, they also provide a relative magnitude in terms of mA/cm^2. The PL dataset also provides a relative magnitude in terms of voltage and series resistance. This combination allows researchers to quickly identify a problem, assess its impact on performance, and implement corrective actions in manufacturing.

4.3.4 Base and Emitter Properties

As discussed previously, the method used to separate base and emitter effects enables extraction of the base diffusion length. This parameter incorporates the impact of the bulk and

rear surface recombination, however it does not consider the impact of front surface recombination or recombination within the emitter. As an example, this could be utilized in isolating the impact of a rear side passivation process when using similar quality bulk wafers, without the need of fabricating specialized symmetrical test samples.

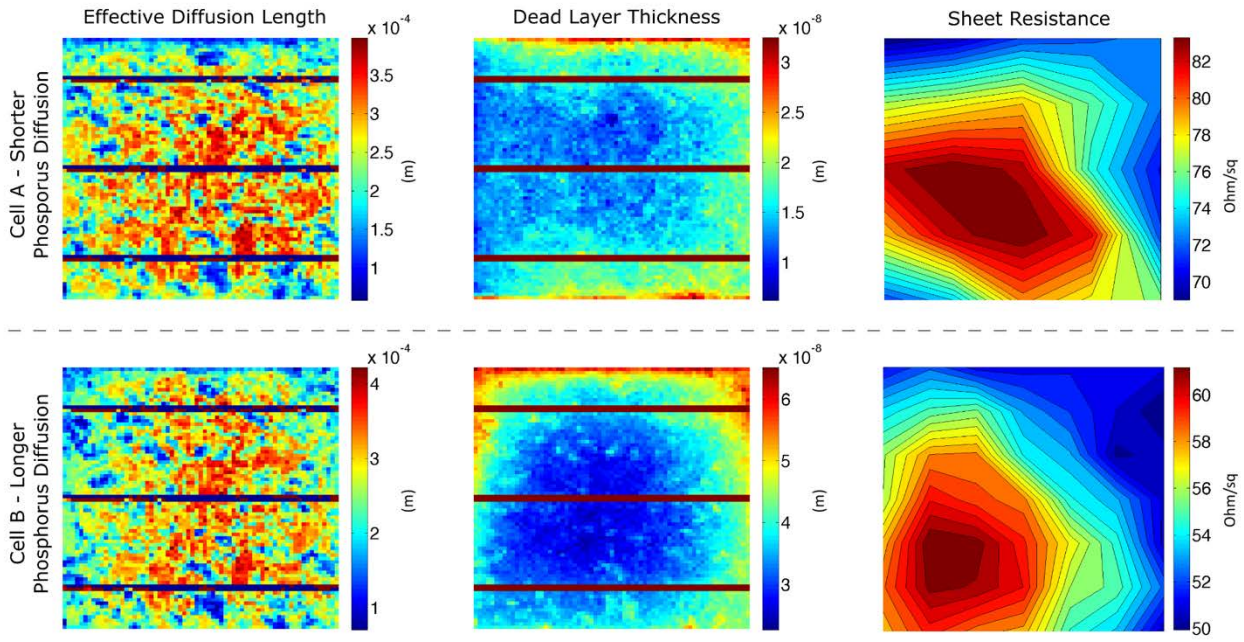


Figure 46: Maps for base diffusion length, dead layer thickness and sheet resistance.

Figure 46 shows the diffusion length maps for two multicrystalline Al-BSF cells fabricated from sister wafers, using identical processing except for the phosphorus diffusion step. There is no discernable sample-to-sample difference in the base diffusion length: the values range from 100μm to 350μm with an average near 200μm. In this case the variation is driven by the bulk properties of individual grains, and not the diffusion.

The model used in this work relies on a fit parameter defined as the dead layer thickness. This parameter has no direct correlation with any physical property of the emitter. Its purpose is only to replicate the behavior of current extraction within the emitter. In general, the larger this

parameter, the higher the concentration of phosphorus within the cell. Converting this parameter into a physical parameter that represents the emitter depth or surface concentration would require additional information.

An emitter is generally defined by the depth profile of phosphorus (including the surface concentration) and the sheet resistance. Figure 46 shows two samples that utilized two different phosphorus diffusion steps. The sheet resistance was measured on separate wafers that underwent identical processing. The dead layer thickness maps correspond quite well to the sheet resistance maps, with a circular pattern seen in both measurements. In this case the shorter diffusion step which resulted in an average sheet resistance of 76 Ω/sq, corresponded to a dead layer thickness in the range of 10-30nm. In contrast, the emitter with an average sheet resistance of 55 Ω/sq corresponded to a dead layer thickness in the range of 30-60nm. In this case the dead layer thickness provides a relative parameter that can be used in a qualitative assessment of the doping concentration.

4.3.5 Extended ARC Analysis

The extinction coefficient and refractive index as a function of wavelength are the defining characteristics of an ARC film [66]. Additionally, reflectance spectra for ARC films exhibit characteristic minima that are defined by Eq. (22).

$$t = \lambda_0/4n \qquad (22)$$

In this equation, t represents the thickness of the ARC, λ_o represents the characteristic minima, and n represents the index of refraction. The challenge in determining the ARC thickness

is that the index of refraction varies as a function of deposition process conditions. The true refractive index can be determined through careful measurements on polished wafers. For processed cells, only an estimate of ARC thickness can be determined through this process assuming a known and constant value for the refractive index across the cell.

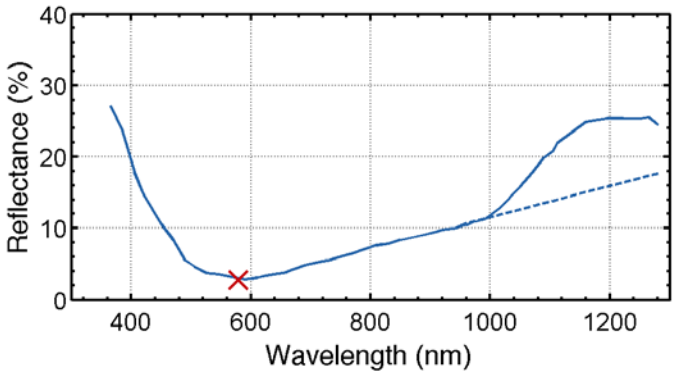


Figure 47. Reflectance spectra for a multicrystalline Al-BSF cell. The characteristic minimum is marked in red and the extrapolated ARC reflectance is shown with the dotted line.

The spatial uniformity of the ARC film can be investigated by mapping the characteristic minima across the cell. This map is displayed for cells 3, 4 and 5 in Figure 48. These maps exhibit a very unique pattern that does not match any other parameter map, highlighting the unique information available from this metric. Consider cell 3 in which there is a range in the characteristic minima from 560-600 nm. If a refractive index of 2 is assumed, this represents a thickness variation of 70-75nm. Alternatively, if a thickness of 75nm is assumed the index of refraction will vary from roughly 1.85-2. Distinguishing exactly which factor is varying would require additional measurements, such as ellipsometry or electron microscopy, which may not be feasible on finished cells. In a manufacturing environment this could be utilized as a quality control metric to assess process stability.

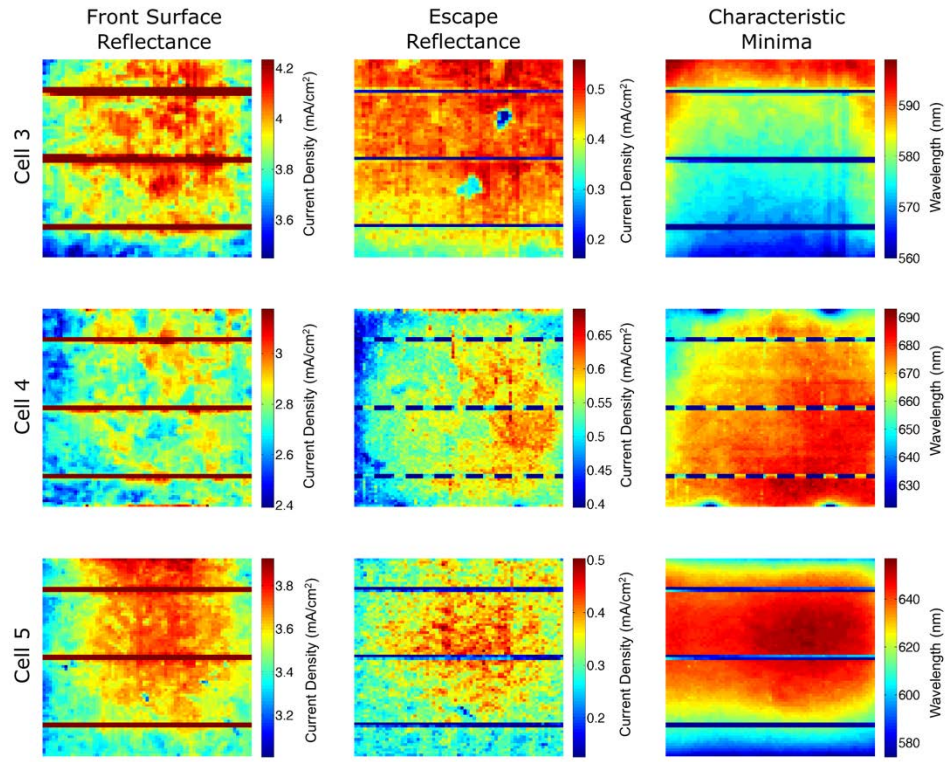


Figure 48: Maps of front surface reflectance, escape reflectance and characteristic minima for three cells.

4.3.6 *Assessment of Measurement Uncertainty*

EQE at a particular wavelength is determined from Eq. (23).

$$EQE(\lambda_0) = \frac{I_{sc}(\lambda_0)}{q * \phi_{\lambda_0}(\lambda)} \qquad (23)$$

where I_{sc} is the short circuit current density of the device with an incident photon flux of ϕ. The photon flux for a given wavelength (λ_0) is determined through a calibration procedure using a reference cell with a known EQE spectra. Ideally the photon flux would be comprised of monochromatic light, however in practice there is a finite bandwidth associated with the light source. Because the photon flux is assigned to a single wavelength, a potential source of error is

introduced to the measured EQE. The magnitude of this error will be dependent on the bandwidth and intensity profile of the light source as well as the relative difference in the EQE of the device under test with respect to the reference cell. The measured EQE (EQE_{meas}) of the device under test at a particular wavelength λ_0 is therefore defined in Eq. (24) with EQE_{actual} representing the true EQE of the device under test and $EQE_{reference}$ representing the EQE of the reference device.

$$EQE_{meas}(\lambda_0) = \frac{\int_0^{\infty} EQE_{actual}(\lambda) * \phi_{\lambda_0}(\lambda) d\lambda}{\int_0^{\infty} EQE_{reference}(\lambda) * \phi_{\lambda_0}(\lambda) d\lambda} \quad (24)$$

The absolute error is then calculated as the difference between the measured EQE and the true EQE of the device under test. This error is comparable to the source of error in standard current-voltage (I-V) measurements of solar cells when determining the equivalent 1 sun conditions for a solar simulator with a light source that deviates from the standard terrestrial solar spectrum. As is the case for I-V measurements, the larger the deviation between the EQE of the reference cell and the device under test, the larger the uncertainty in the current response of the cell. Therefore, to minimize uncertainty, it is critical to use a reference cell that closely matches the device under test to calibrate the photon flux at each wavelength.

Additional sources of error can arise from the instrument itself. These errors can be categorized as either random or systematic. A thorough calibration procedure should be effective in eliminating any additional sources of systematic error. Random errors arise due to sources of noise within the instrument. A signal to noise ratio (SNR) is commonly used to assess this affect. For the instrument used in this study, each data point will have a unique SNR. The signal is

impacted both by the LED intensity and the spectral response of the cell in that spectral range. Although multiple LEDs can be used to increase signal strength, the general trend is that longer wavelength LEDs are weaker than LEDs in the visible range. This, coupled with poor response in the NIR region for silicon devices, leads to lower SNR in the long wavelength region. The SNR could be reduced further if longer integrations times are used, however this would impact the overall measurement time.

This work also relies on reflectance measurements to obtain quantitative results, adding yet another source of uncertainty. Reflectance measurements suffer from the same issues described above, along with a few additional considerations. When measuring diffuse hemispherical reflectance, an integrating sphere is used. To practically raster the light source across the cell, the integrating sphere must remain slightly above the cell surface. This distance effectively reduces the collection efficiency of reflected light. The collection efficiency will depend both on the distance between the cell and the integrating sphere as well as the angular dependence of reflected light. Because the angular dependence is largely dependent on the properties of the texturing [67], this collection efficiency may vary from sample to sample.

Because typical monochromator based QE systems are often cumbersome and time consuming, measurements are performed at only one location on a cell. As shown in this work, there can be large variations in both the EQE and reflectance across the cell. Although a monochromator based system may provide a slight improvement in measurement accuracy, the assumption that any single point is an accurate representation of the entire device may be misleading. By measuring at multiple locations on the cell, a more comprehensive evaluation of the spectral response is achieved. Additionally, by averaging the results across the device, any

outlying datasets are effectively offset. Alternatively, filter based QE systems illuminate the entire device, providing a more accurate representation of the full device area. These measurement do not, however, reveal spatial non-uniformities.

With proper calibration and consideration of the factors discussed above, the measurement uncertainty can be reduced considerably. When comparing the measurement results of this system with more traditional methods, very good agreement was found. A comparison of data collected with the FlashQE system with data from a calibration laboratory is shown in Figure 49.

To confirm the accuracy of the measurement results, the short-circuit current density was calculated from Eq. (16) using the spatially resolved average of EQE for several cells. The same cells were measured using two independent high quality solar simulators with the results shown in Figure 50. These measurements are in very good agreement with each other, showing only minor deviations from the one-to-one relationship. There seems to be a slight under prediction of the short-circuit current using the Flash QE. This may be a result of the integration in Eq. (16) starting at 365nm while the standard solar spectrum extends deeper into the UV.

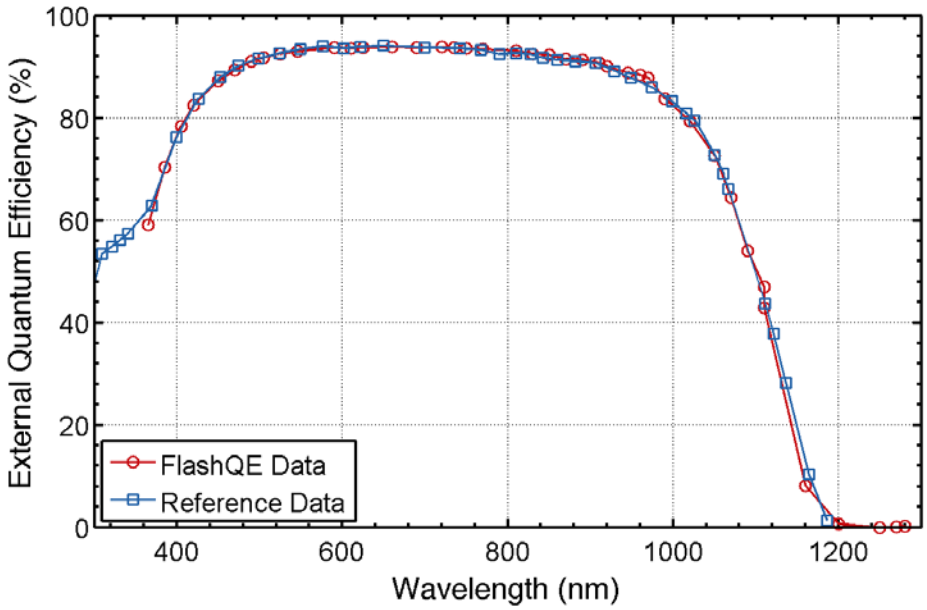


Figure 49. Comparison of Flash QE data with results from a calibration laboratory.

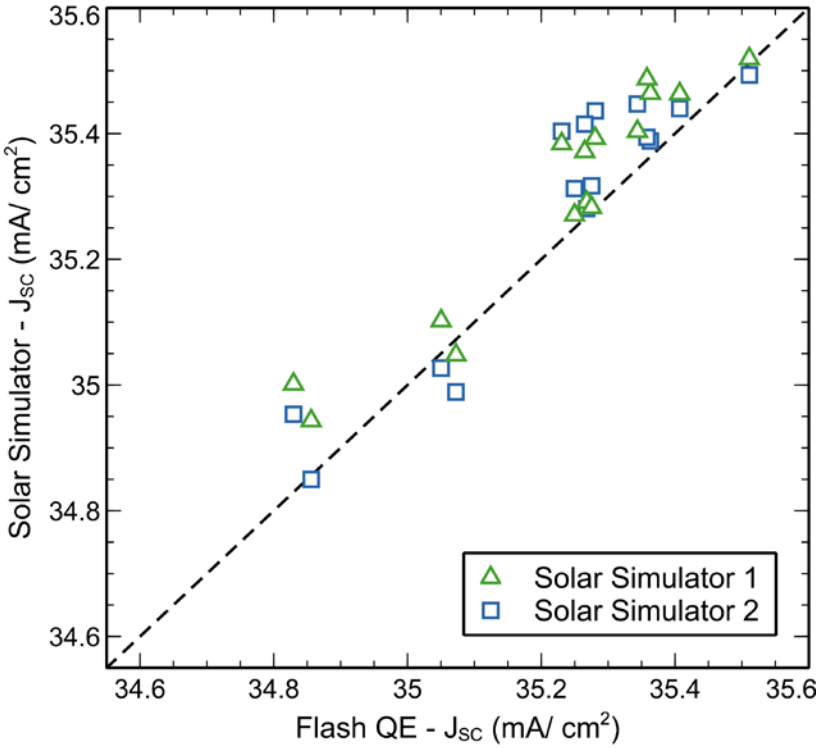


Figure 50. Comparison of FlashQE J_{sc} measurements with Solar Simulator results.

4.4 Case Studies

Metrology as it has been discussed within this chapter has focused on identification of loss mechanisms in a spatially resolved way. This section highlights how these characterization methods can be used during process development to improve the overall device performance. As evident in the following case studies, the spatially resolved analysis was essential in understanding how the various processes impacted performance. In this way, the metrology was used to generate a deeper understanding of process variability and has the potential to improve cell performance by providing a more thorough optimization for each specific process step.

4.4.1 Impact of Diamond Wire Sawing

The photovoltaic industry utilizes a multi wire slurry saw process to slice silicon ingots into wafers of appropriate thickness for cell manufacturing [68]. This process, although effective, exhibits several drawbacks including excessive waste and relatively slows processing speeds. To overcome these shortcomings, diamond wire sawing processes have been developed in recent years [69-71]. Alternatively, the downsides of diamond wire sawing are the high cost of the wire itself and the extensive damage created at the surface of the wafers. The damage has been shown to vary greatly from wire to wire and from one sawing process to another. The generated damage consists of amorphization of the silicon, pits, and periodic structures (known as pilgrim waves). It was recently suggested that these pilgrim waves could have an impact on cell performance [72]. It is critical to understand more about these features, particularly as it pertains to surface texturing, where the standard industrial texturing process has been less effective for wafers cut using diamond wire techniques as compared to wafers cut from standard slurry-based techniques [73].

Pilgrim waves were observed in some, but not all, wafer investigated in this study. It appears that the choice of wire, in terms of diamond particle size and distribution, impact both the frequency and magnitude of these pilgrim wave features. This may impact manufacturers that have an established unvarying process that also source wafers from multiple suppliers. Because each supplier evidently employs a different diamond wire and sawing process, cell manufacturers may need to look into adequate specifications for incoming wafer surface properties with respect to the dominant pilgrim wave type in addition to the usual specifications such as lifetime, average thickness, and total thickness variation.

Several studies have suggested that the damage induced during the diamond wire sawing process may impact the cell performance. Additional studies have shown that an appropriate etching process, referred to as the saw damage removal, can effectively eliminate the micro-scale (μm scale) damage due to the diamond wire saw process [74]. Other studies have indicated, in agreement with the results in this work, that a relatively larger (mm scale) periodic structure may remain even after the saw damage etch. These features are a result of the forward to reverse variation in the wire pulling direction as it slices through the ingot. These features have been referred to as a pilgrim waves resulting from the various pilgrim modes of the diamond wire during sawing. Although the micro-scale damage can be eliminated during the saw damage etching process, these larger periodic features on the surface of the wafer can remain throughout the cell fabrication process. In this work select cells were identified for advanced spatially resolved analysis to understand what impact these pilgrim waves have on the various performance parameters.

Photoluminescence (PL) images were taken using a BT Imaging PL system with an 808 nm laser as the illumination source. Maps of open-circuit voltage, dark saturation current density and series resistance were calculated. All parameter maps were analyzed to identify which parameters are most affected by the diamond wire defects. FlashQE measurements were also carried out and the current loss analysis was applied.

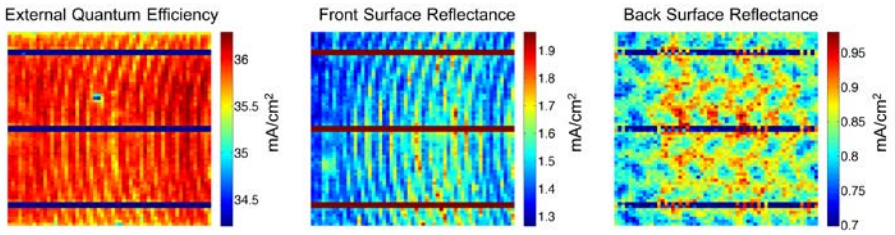


Figure 51: Short-circuit current density (left), front surface reflectance loss (center), escape reflectance loss (right) maps for a cell exhibiting pilgrim wave features as a result of the diamond wire sawing process.

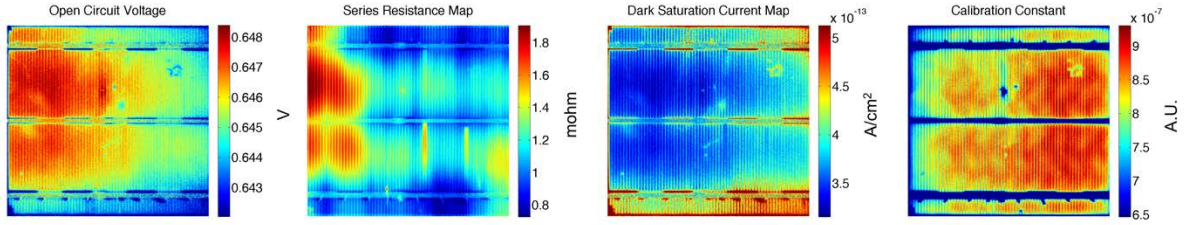


Figure 52: Parameters maps derived from photoluminescence imaging.

Figure 51 displays the quantum efficiency and reflectance results for a cell with saw marks. These defects led to approximately 0.5 mA/cm^2 variation in J_{sc} in a regular pattern across the cell. The affected area was estimated to be approximately 40% of the cell resulting in an absolute loss in J_{sc} of approximately 0.2 mA/cm^2. After inspection of the reflectance data it was observed that this loss was largely due to reflectance off of the front surface. This suggests that the pilgrim wave features on the surface of the wafer influence the uniformity of the surface

texturing leading to enhanced reflection. In addition to the reflectance loss, there may also be some increased parasitic absorption within the anti-reflection coating or within the emitter. The magnitude of the parasitic absorption is much smaller than the effect of the reflectance.

The electrical properties of the same cell were investigated using PL imaging as shown in Figure 52. There is little to no impact of the striations on the electrical performance of the cell in terms of J_o, V_{oc} and R_s. The calibration constant used in the PL calculations is also shown to compare the belt marks that are observed in the back surface reflectance map. These results suggest that only the optical properties of the front surface are affected impacting only the short-circuit current of the device. These defects do not appear to be recombination active or associated with resistive effects.

A decrease in short circuit current density in the range of 0.2 mA/cm^2 would be very difficult to observed in standard current-voltage measurements because of the variability introduced from solar simulators. In this case we quickly identified the defect and assessed its impact on performance using Flash QE and PL techniques.

4.4.2 *Optimization of Selective Emitter Etch-Back Process*

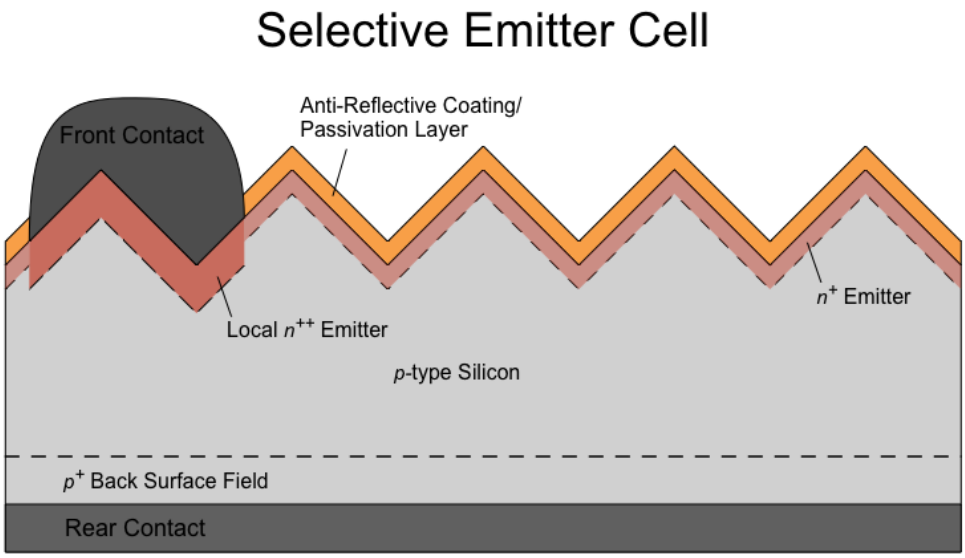


Figure 53. Structure of a selective emitter cell architecture with the two distinct emitter regions highlighted in red.

Forming a high quality emitter requires balancing the effects of series resistance and carrier recombination. A high sheet resistance, or higher phosphorus concentration, is favorable to reduce the contact resistance between the emitter region and the contacts. Unfortunately, higher phosphorus concentrations also result in higher recombination rates due to an increase in the defect density. Therefore, a homogeneous emitter (i.e. uniform across the cell) is optimized to provide adequate contact resistance while minimizing recombination as much as possible. An alternative approach would be to design an emitter that has higher doping concentrations near the contact and lower doping concentrations elsewhere. This approach is called a selective emitter and is shown in Figure 53.

There are several ways to achieve this design including localized laser doping or a two-step diffusion process with a patterned ARC. In this work, an etch-back process was utilized [75]. After the standard texturing and cleaning steps, the entire wafer is heavily doped using a high

temperature phosphorus diffusion step. After diffusion, a phosphorus silicate glass (PSG) layer remains on the cell. An etching paste is then screen printed on the cell in a pattern that is the inverse of the metallization pattern. The etchant is activated using a firing process. The etch depth is controlled by the time-temperature profile of the furnace. The PSG layer is then removed from the remaining regions using a standard PSG removal process. Finally, the cell is completed with ARC deposition and metallization. This leaves a higher doped region under the contact and a lower doped region elsewhere on the cell.

In this study, four groups of ~25 cells were fabricated from near identical wafers. The only difference in the groups was in the emitter diffusion step. Groups A and B consisted of homogenous emitters and groups C and D consisted of selective emitter structures using the etch-back process described above. Group A utilized the optimized homogeneous emitter process with an emitter sheet resistance of 80 Ω/sq. Group B utilized a slightly higher doped emitter, from a slower phosphorus drive-in process than Group A, with a sheet resistance of 50 Ω/sq. Group C consisted of the optimized etch-back process that had a starting sheet resistance of ~50 Ω/sq that was etched back to 90 Ω/sq. Finally, Group D had a starting sheet resistance of ~50 Ω/sq that was etched back to 90 Ω/sq. Group D utilized a slower phosphorus drive-in process than Group C, however both had a similar starting sheet resistance value. The sheet resistance is dependent on both the concentration of phosphorus at the surface and the depth profile. Therefore, it is possible to have emitters with unique concentration profiles that have similar sheet resistance values.

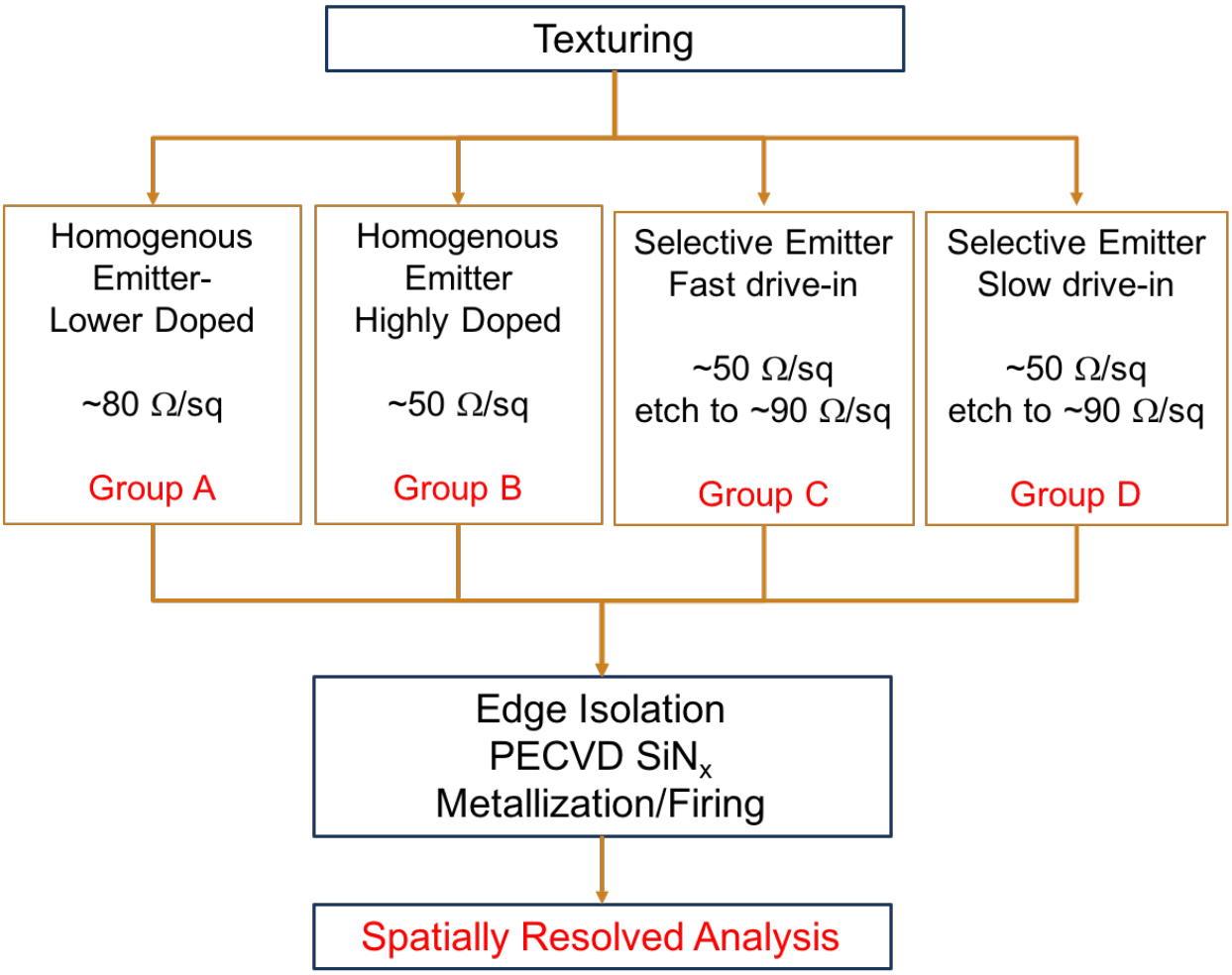


Figure 54. Process flow and process variation for selective emitter study.

Current-Voltage measurements were performed using a Sinton Instruments FCT-450 cell tester. From the I-V data, standard PV performance parameters were calculated. The results are shown in Figure 55. The data shows that group C yielded the highest efficiency averaging just below 17.6%. This is a 0.15% absolute increase as compared to the optimized homogenous emitter Group A. This increased efficiency is due to the enhanced open-circuit voltage achieved with the selective emitter. This is a result of reduced recombination within the emitter. Also there was a small improvement in the series resistance. Group B showed the largest improvement in series resistance due to the significantly reduced emitter sheet resistance creating a lower

contact resistance. This also led to an increased fill factor, but the short-circuit current was negatively impacted as the phosphorus concentration extended deeper into the device. This resulted in a lower efficiency overall. Although the I-V analysis was valuable in identifying performance trends, insight into the uniformity and spatial variation of cells performance is absent. For this both Biased PL and Flash QE measurements were utilized.

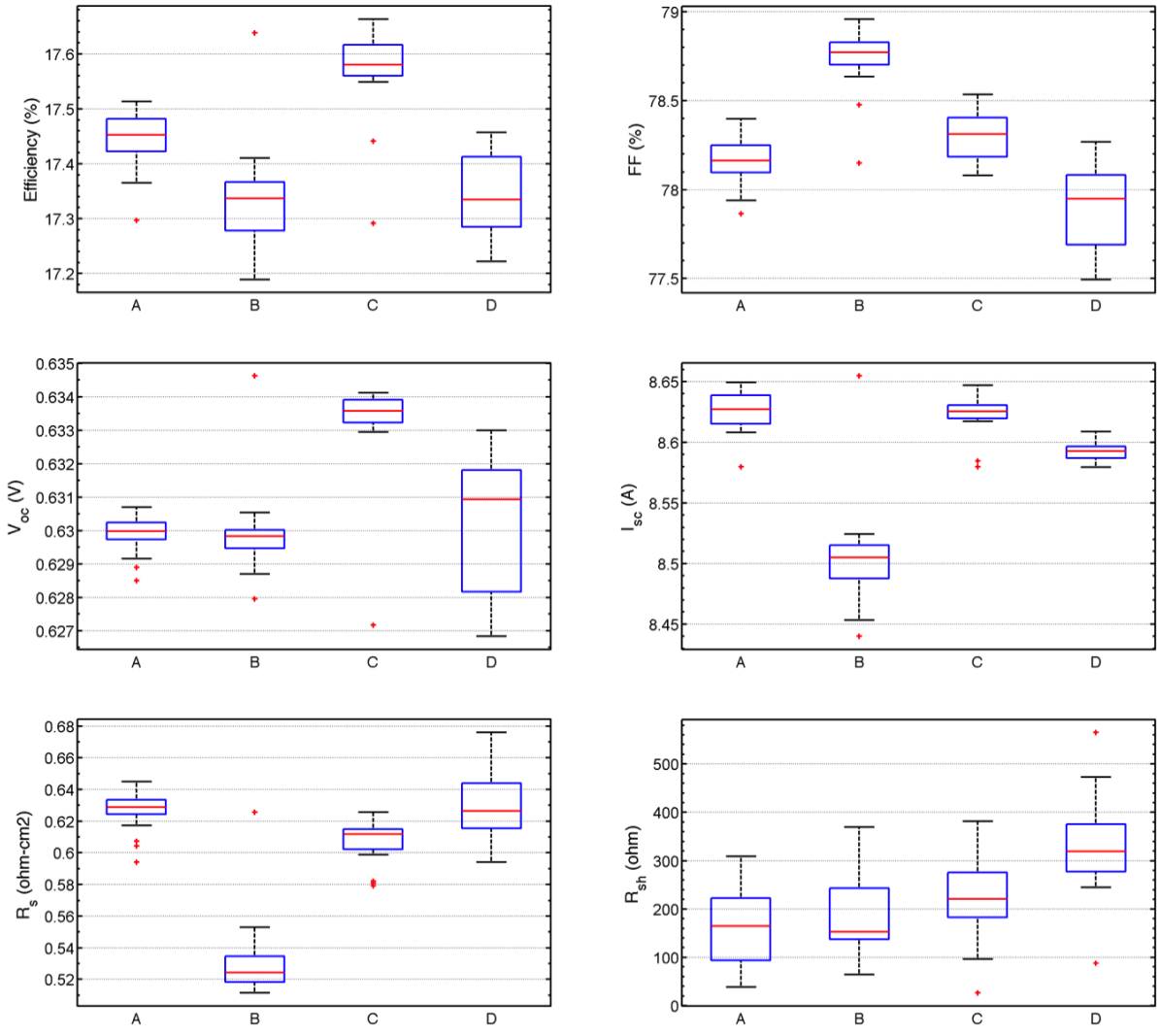


Figure 55. Summary of I-V analysis for selective emitter study. Box-plots were constructed using the 25 cells in each the four groups.

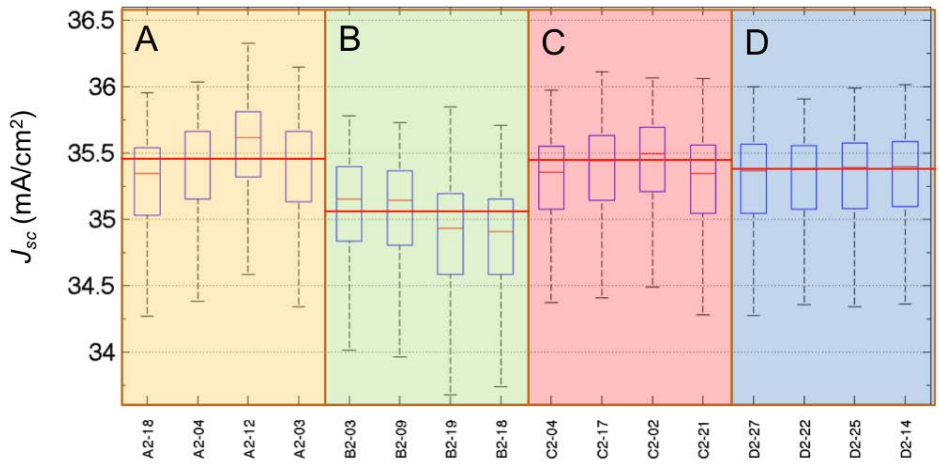


Figure 56. Spatially resolved J_{sc} as calculated from Eq. (16) for 16 cells.

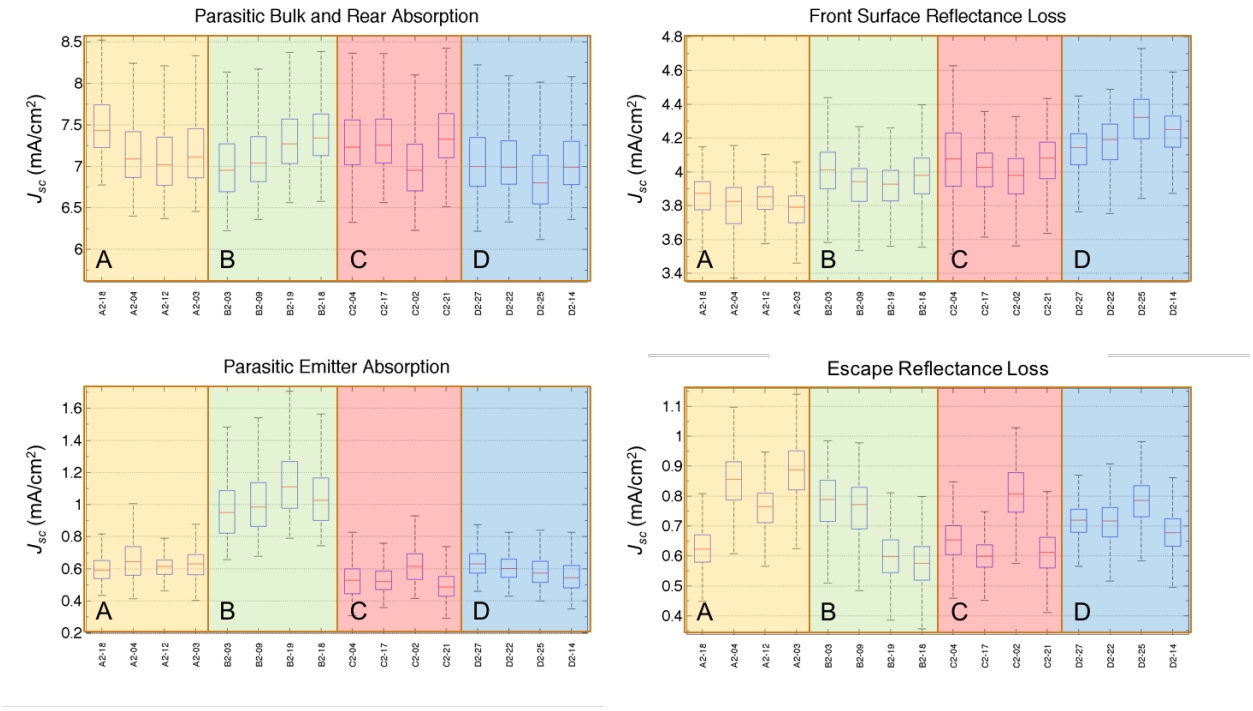


Figure 57. Box-plots for each of the current loss mechanisms as determined from FlashQE measurements, with the distribution for each cell generated from the spatially resolved analysis.

Four cells from each group were selected for spatially resolved analysis. FlashQE measurements were performed and the current loss analysis was applied to each pixel. Box-plots were constructed using the spatial variation for each cell. The results are shown in Figure 56 and

Figure 57. The overall short-circuit current density, as shown in Figure 56, exhibits a very similar trend to the I-V results. Again, Group B was significantly lower than the other groups and Groups A and B slightly out performed Group D. The usefulness of the current loss analysis is apparent in Figure 57 where each of the four loss mechanism are compared. Very clearly, the parasitic emitter absorption is highest for Group B, proving that it was indeed the responsible for reducing the J_{sc}. There was no apparent difference in the bulk and rear properties across all groups as was expected. The wafers quality and rear side processing of the cells was uniform throughout the experiment. There was, however, a variation in the front surface reflection between the various groups. This difference was not anticipated and is likely a result of the texturing process becoming less and less effective over time as each group was processed. Even though there was a slight reduction in the emitter loss of Group C as compared to Group A, the overall J_{sc} of the two groups remain similar because of an increase in the front surface reflectance in Group C. It is important to note that this increase is not related to the emitter processing and is experimental artifact. This implies that further enhancements in the performance of the selective emitter cells is possible. This conclusion would not be possible with measurements of short-circuit current alone. By isolating the loss mechanisms due to the emitter, other unintended process variations can be identified and excluded resulting in a more accurate picture of device performance.

When looking at the actual parameter maps, even more information can be extracted from this dataset. Figure 58 shows the maps for emitter loss and effective diffusion length derived from Flash QE measurements and maps for open-circuit voltage derived from PL imaging. The maps are shown twice; On the left each image is individually scaled for maximum contrast and on the right the same scale is used for all cells to highlight the variation between groups. The

effective diffusion length, which accounts for base and rear recombination effects is constant throughout all of the cells. This was expected as all cells were fabricated using near identical wafers and rear side processing. In both the emitter loss and open-circuit voltage maps there is a clear circular pattern for Groups A and B. This effect is a result of the phosphorus diffusion process caused from the non-uniform heating produced in a circular tube furnace. This effect is less pronounced in Group C and is nearly non-existent in Group D. There is however a larger grain-to-grain variation in these two groups. These results suggest that the spatial variation (i.e. circular pattern) of the emitter is dominated by variations in phosphorus concentration only near the surface. By etching a thin layer near the surface of the wafer, a more uniform emitter layer is achieved. The grain orientation appears to have a significant impact on the rate at which etching occurs. Because of this variation in etch-depth, some grains end up more heavily doped as compared to other grains. These effects are more pronounced in Group D than in Group C. Indeed, the etch-back time was longer for Group D as compared to Group C, reinforcing these conclusions.

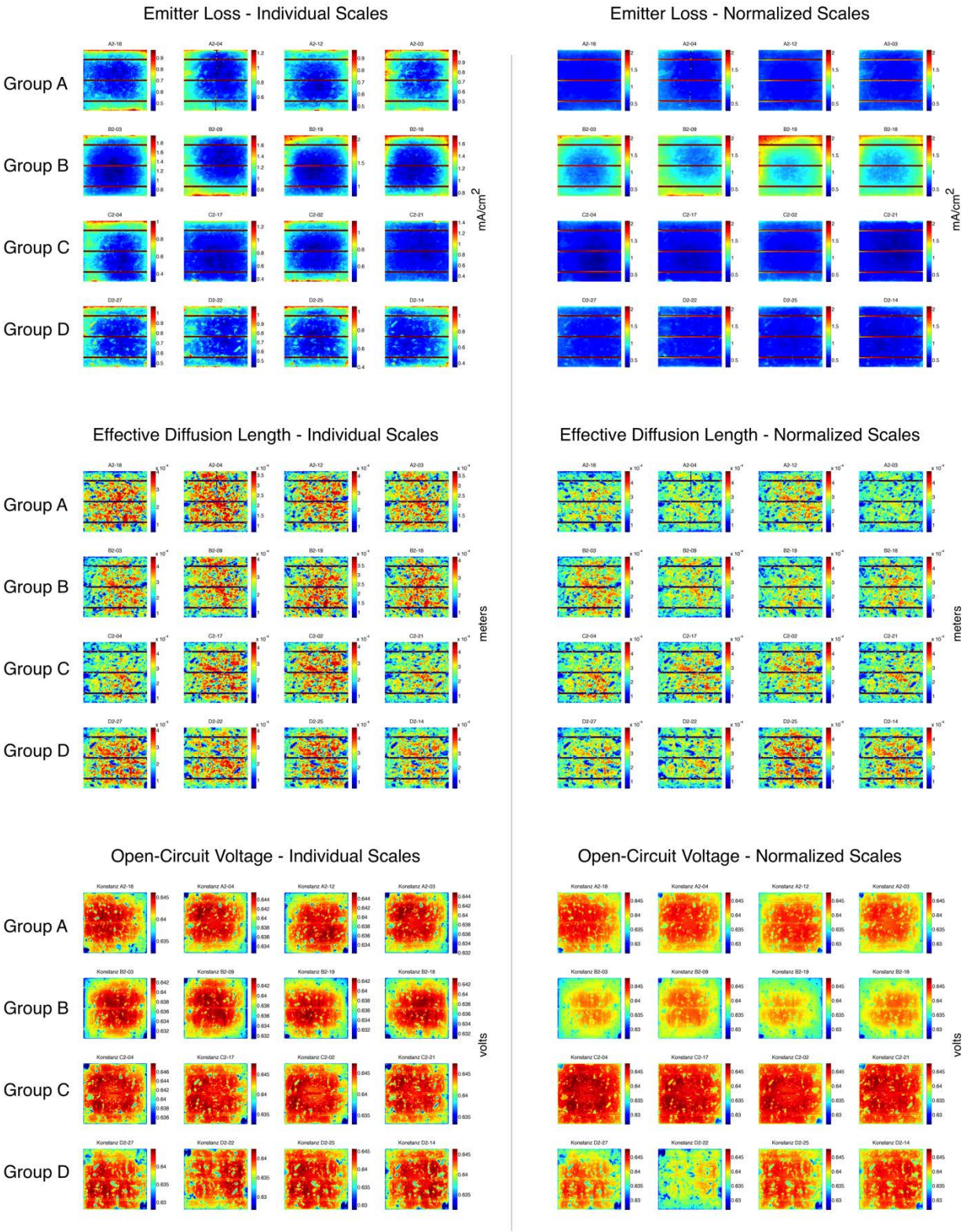


Figure 58. Parameter maps derived from Flash QE and PL imaging.

4.4.3 Cell Fracture Analysis

Cell cracking is an important issue in PV manufacturing. It directly affects both yield and cost while also preventing further reductions in wafer thickness. It has been reported that a 1% increase in cracked cells could cost nearly 500,000 euros per year for an 80 megawatt per year production line [76]. Concerns about long-term performance have pushed manufacturers to remove and discard affected wafers from their line and only ship “crack-free” modules to their customers.

Not all cracks impact performance equally and their impact on long term performance is not clear. Crack initiation often occurs during soldering or lamination although it is not easily measureable [77]. As the module experiences mechanical loading in the field due to wind or snow, these cracks may propagate, further impacting performance. Some studies have shown that the direction of the crack with respect to the busbar is a critical factor in determining the impact [78]. It has also been shown that the impact of certain cracks will vary based on the load conditions during the measurement [79]. This implies that a fracture leaves the cell in a metastable state, and the impact depends on how well, if at all, current can conduct across a crack. This study investigated the use of spatially resolved characterization to assess the impact of cracks on the local cell parameters.

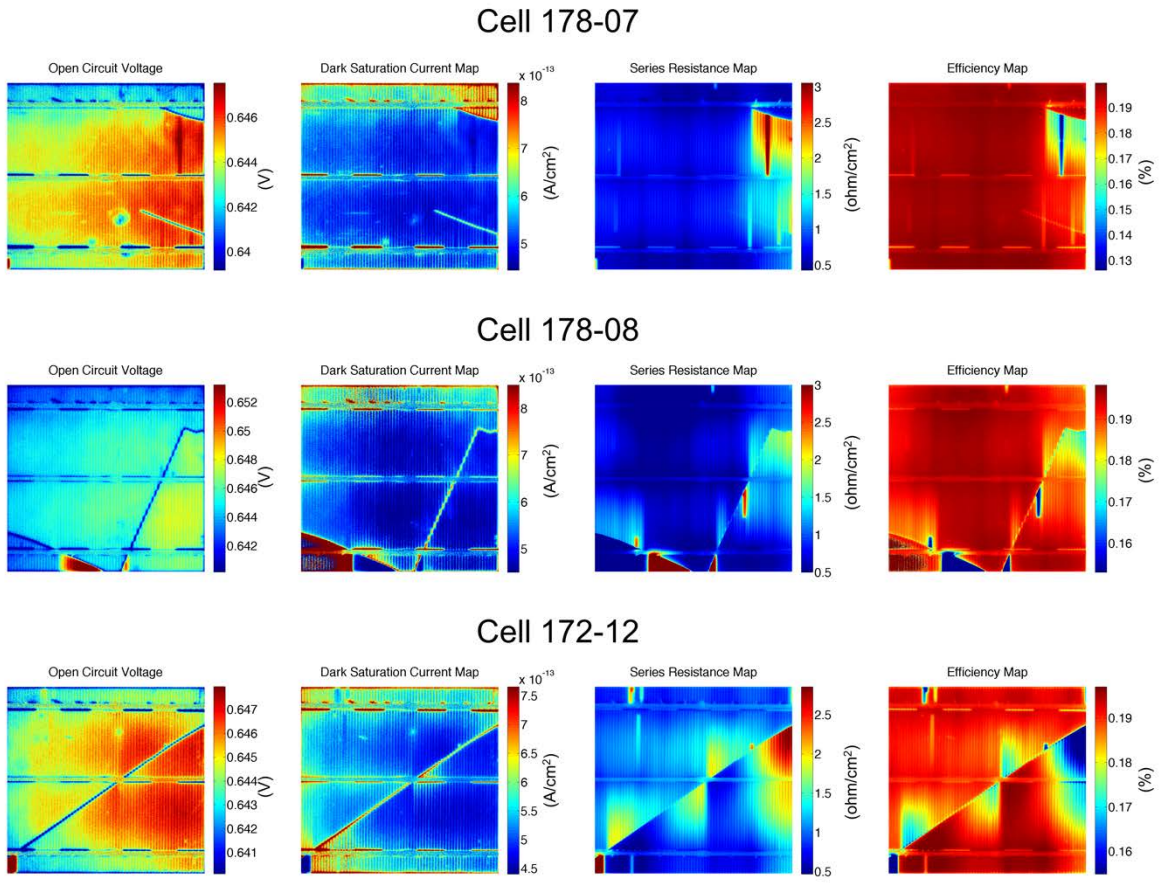


Figure 59. Parameter maps derived from PL imaging for three cells that exhibit cell fracture.

In cell 178-07, two cracks can clearly be observed from the dark saturation current and open-circuit voltage maps in Figure 59. The series resistance map tells a different story. While the top crack shows a significant increase in the series resistance, the bottom crack does not. Optical inspection confirmed that the metallic gridlines for the bottom cell were still intact, but were not for the top crack. From this, it is clear that the continuity of the metal gridlines is the key factor that determines how a crack will impact series resistance. Because the grid line was interrupted, current is forced to travel further to reach the busbars resulting in an increased series resistance. You can see that this increase in series resistance is reflected very strongly in the efficiency map.

Cell 172-12 has a single diagonal crack that extends across the entire cell area. When inspecting the open-circuit voltage map, a region in the lower left corner appears far higher than any other region. The voltage displayed for this region, as well as values in all other maps, are invalid because no current can be extracted from this region of the device. The fracture has prevented all grid lines in that region from establishing electrical contact with the busbar of the cell completely isolating this region. A similar effect is also seen on the bottom edge of cell 178-08. Other than completely disconnecting regions of the cell, cracks do not appear to influence the open circuit voltage, or saturation current, in areas away from the fracture. This is consistent with what would be expected. Because of the finite diffusion length of carriers in silicon, only carriers very near to these cracks will have an opportunity to recombine at this new surface.

When inspecting the series resistance image for cell 172-12, an interesting effect is observed. The series resistance is impacted the most when the crack is very near to the busbar. This, again, is because carriers generated in this region are now required to travel a longer distance to be extracted from the device. When the crack is near the center of two busbars, the impact is negligible. Here the carriers travel the same distance with or without the fracture.

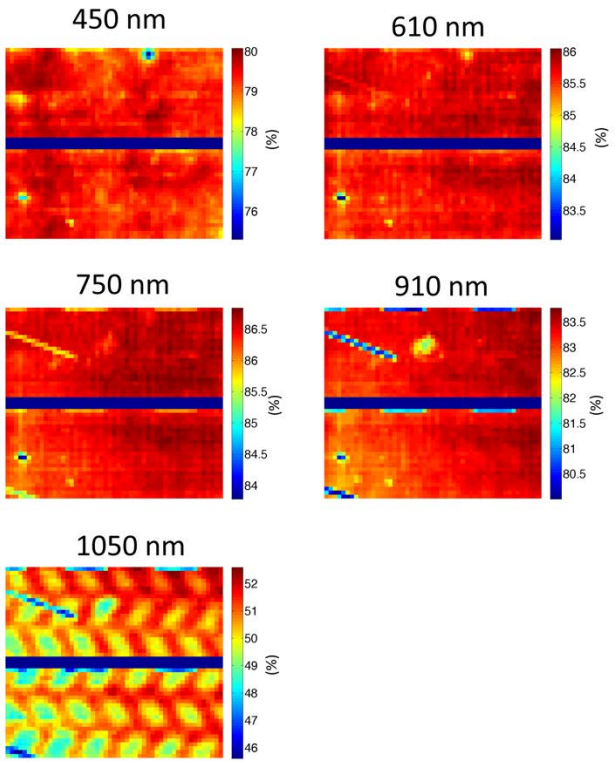


Figure 60. EQE maps at five distinct wavelengths for a partially fractured cell.

Spatially resolved QE analysis was also applied to a cell with several cracks that had not propagated completely through the cell. Figure 60 shows the EQE at selected wavelengths for this cell with two cracks. It is useful to analyze EQE data at specific wavelengths through the lens of the absorption depth within silicon for that wavelength. For example, longer wavelengths penetrate deeper into the device. Within Figure 60 for instance, the belt marks arising from the firing of the backside metallization can only be seen at 1050 nm. At 1050 nm the absorption depth is just below 1 mm, meaning that a large fraction of light interacts first with the rear surface optically before being absorbed within the base of the device. Therefore, the variation in the optical properties of the rear surface can be inferred.

From this data, it was observed that the cracks only impact the EQE at long wavelengths starting above ~600 nm. This implies that the fracture within the silicon is not impacting carriers generated at the front surface of the cell and within the emitter region. Because of the relatively high defect concentrations in the emitter and at the front surface of the device, the crack is not a dominate feature in terms of emitter collection efficiency. In other words, the emitter diffusion length is not significantly reduced with the introduction of an additional interface defect (*i.e.* fractured surface). On the other hand, the diffusion length of carriers in the base of the cell is much larger. In this case the addition of a fractured surface creates a large recombination current in this region, impacting carrier transport and ultimately reducing efficiency.

4.5 Conclusions

This chapter discussed the metrology methods that allow for spatially resolved analysis of large area solar cells. EL and PL techniques allow for fast characterization of resistive and recombination related performance. FlashQE measurements complement this approach by assessing the spatial variation in current generation. By probing the entire spectrum, specific loss mechanisms can be identified and traced back to specific process steps during fabrication. This comprehensive loss analysis can be used to quickly identify non-uniformities and assess their impact on performance. Several examples were explored to highlight the wealth of information that can be obtained using these spatially resolved methods that would not be apparent from standard (*i.e.* not spatially resolved) device performance characterization methods.

CHAPTER 5: MODULE LOSS ANALYSIS

As the focus of this work shifts from cell performance to module performance there are many things to consider. There are a multitude of factors influencing the performance of a module. There is the device physics as described in Section 2.1, but there are also issues related to cell mismatching, optical performance of the packaging, and resistive losses due to cell and string interconnects, to name a few. Because of the increased complexity, attributing performance loss to specific mechanisms can be a challenge. Even though this is valuable for evaluating new module designs, this loss analysis becomes even more critical when assessing module reliability. Only through a comprehensive understanding of the factors that influence module lifetimes can more reliable products be designed. This chapter focuses on advance module metrology and how these techniques can be used to diagnose module performance losses.

5.1 Module Performance Characterization

5.1.1 Current-Voltage Measurements

Illuminated current-voltage (*I-V*) measurements provide the basic performance metrics, such as maximum power output, that provide a general assessment of the module performance. These measurements are often used for reliability studies and are used as the criteria for module qualification standards such as IEC 61215. Obtaining accurate and repeatable results is often a challenge. Two solar simulators were used in this work for obtaining I-V characteristics and are shown in Figure 61 and Figure 62.

Figure 61. Sinton FMT-350 solar simulator; (left) view from the light source toward the module and (right) module during illumination.

Figure 62. Spire 4600 solar simulator. Modules are placed face down on the glass.

There are three main criteria used to characterize the quality of a solar simulator. These include temporal uniformity, spatial uniformity and spectral conformance. Temporal uniformity refers to the stability of the light source over relatively long periods of time. The idea is to utilize

a light source that does not fluctuate in intensity over the course of a day, with only minor changes over the course of months or years. Spectral conformance refers to how well the light source matches the standard solar spectrum. Lastly, spatial uniformity refers to the uniformity of the light source over the entire module area.

The spectral conformance is a very critical issue when performing illuminated *I-V* measurements. Efficiency, in a general sense, is a metric that quantifies the ratio between the power in and the power out. Unfortunately, the standard 1-sun condition of 1000 W/m^2 (*i.e.* power in) is not as universal as one may expect. As shown in the previous chapter with several quantum efficiency spectra, the response of a PV device has a strong dependence on wavelength. As the spectrum of a solar simulator deviates from the outdoor spectrum, error is introduced because of the variation in spectral response from module to module.

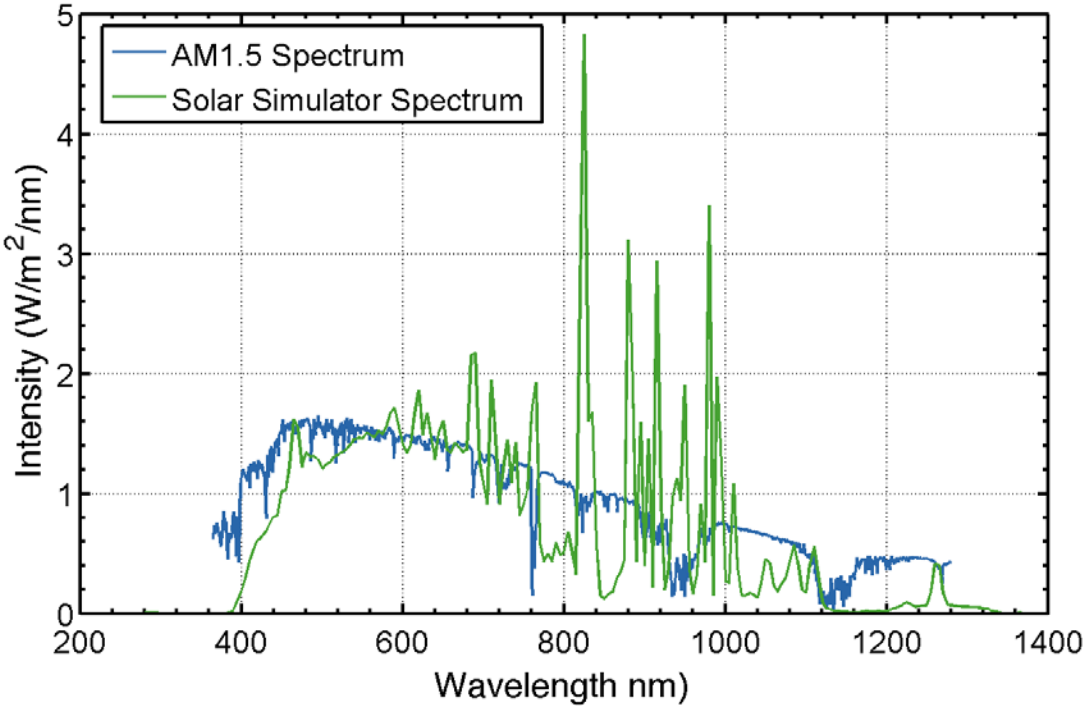


Figure 63. Comparison of the standard solar spectrum with a spectrum from a SPIRE 4600 solar simulator.

The standard AM1.5 solar spectrum and an example solar simulator spectrum are both shown in Figure 61. The general trend and magnitude of intensities agree to a first order, but there are a few discrepancies that may impact the accuracy of measurements. The first is in the short wavelength regime where the solar simulator has little to no intensity below 400nm. In this case two devices that differ only in terms of their spectral response in the 350-400nm range would show no discernable difference from this simulator. Conversely, in the long wavelength range (800-1000nm) there are large spikes in the simulator spectrum arising from the xenon lamp. In this case two devices that have only minor deviations from each other in this spectral range could result in large variations in performance.

Standards for solar simulators attempt to address this by requiring the average intensity over each 100nm band, starting at 400nm, (*e.g.*400-500nm, 500-600nm, etc.) to be within 25% of the average intensity determined from the standard spectrum. The spectrum in Figure 61 meets this criteria, however there is still room for significant error. There are a few methods to account for this error. The first method is to apply a spectral correction factor (*M*) to the *I-V* measurement [80, 81]. This method requires the spectral responsivity (SR_{DUT}) of the device to be known, and is calculated from the intensity of the standard spectrum ($I_{AM1.5}$) and the intensity of the incident spectrum (I_{inc}) using Eq. (25)

$$M = \frac{\int I_{AM1.5}(\lambda) SR_{DUT}(\lambda) d\lambda}{\int I_{inc}(\lambda) SR_{DUT}(\lambda) d\lambda} \qquad (25)$$

The other option is to normalize the intensity of the light source using a reference cell/module that has the same quantum efficiency as the device under test. This method does

not require any post processing of the *I-V* data, but does require the reference cell or module to have known performance characteristics that are typically determined from a calibration laboratory. In this case, the intensity of the simulator is adjusted so that the short-circuit current of the reference device matches its calibrated value. The challenge in using this method is in determining whether or not two modules have similar spectral response characteristics. This is particularly difficult to assess in aged modules.

Spatial uniformity is another variable that can introduce significant uncertainty into PV module *I-V* measurements. Because cells are connected in series within a module, the current is limited by the lowest performing cell. This is why when a single cell is shaded within a module, the entire power output of the module is severely affected. Shading is an extreme example of a non-uniform light source. It is important to realize that minor deviations in intensity could also have an impact.

To characterize uniformity, a single cell is sequentially moved throughout the test plane in a grid type pattern and the short-circuit current is measured in each location. The measured value is recorded and the variation is mapped as is shown in Figure 64. The map on the left is the uniformity obtained by the simulator shown in Figure 61. Because of the large distance between the light source and the module, there is only a small gradual change in the intensity over the module area. The simulator results in Figure 64 (right) represent the simulator shown in Figure 62. Because the light source is significantly closer to the module, this simulator requires complex optical elements including mirrors and diffusors to create a uniform intensity profile. This complexity leads to abrupt changes in the intensity of neighboring locations. In fact, if a smaller

area reference cell is used with a higher resolution grid (not shown), the variation increases even more.

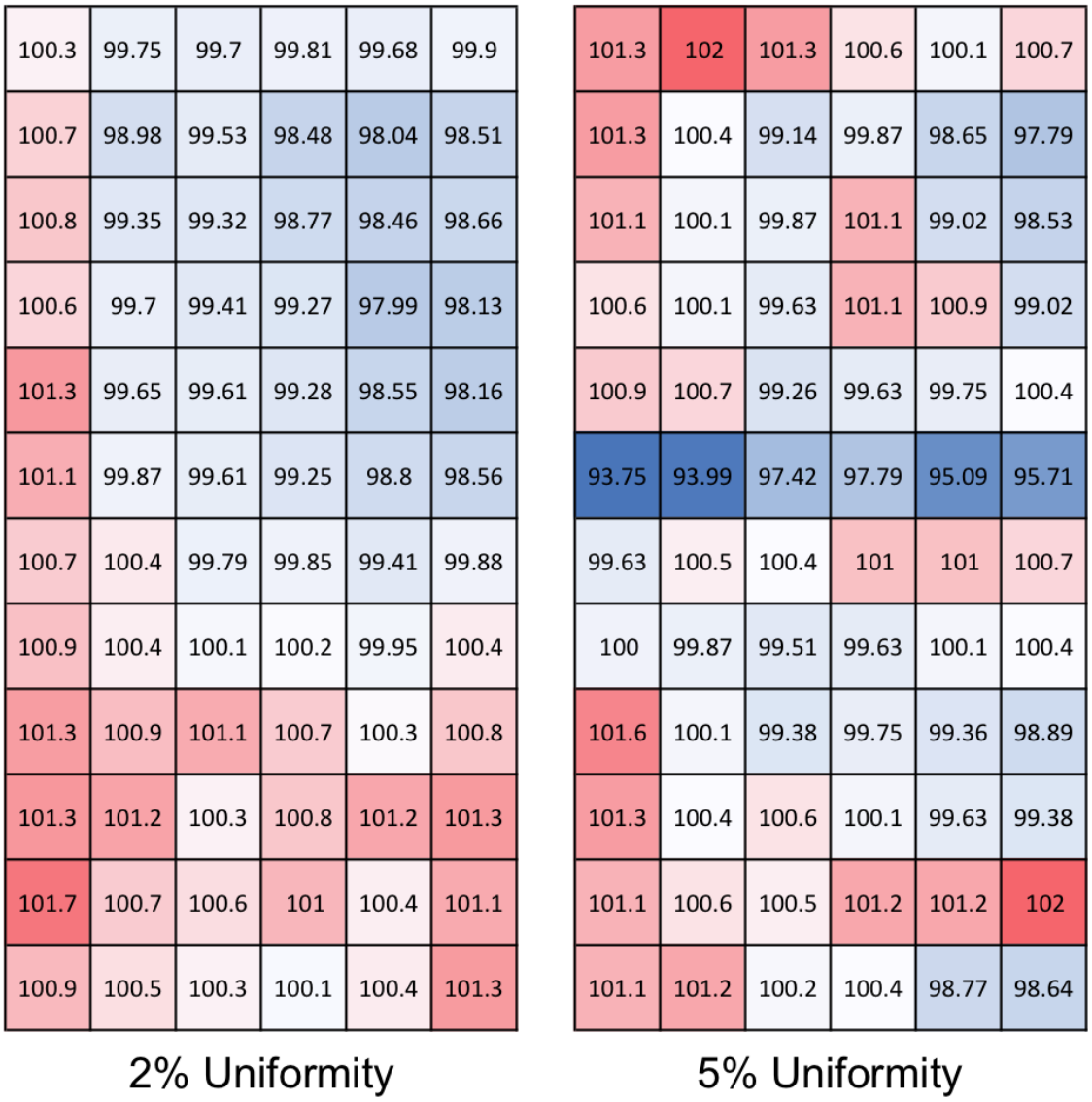


Figure 64. Uniformity profiles for two large area solar simulators used in this work. Each square represents a 6" by 6" area, with the units in percentages of the nominal 1000W/m^2 value.

Unlike spectral corrections, spatial non-uniformity is not something that can easily be corrected for. This is largely because the total variation (e.g. 2 or 5 %) is not the dominant factor.

It has more to do with how this non-uniformity is distributed, and how that compares to the module size and cell configuration. In this case it is important to minimize the non-uniformity as much as possible.

5.1.2 Electroluminescence Imaging

Just as with cells, luminescence imaging is also a powerful technique for visualizing defects and non-uniformities in modules. Because PV modules are large in area, it has been impractical to use illumination as the excitation source, so traditionally an electrical bias has been used. Generally, an image is taken with a forward current near the I_{mp} of the module. Similar to cells, qualitative assessments are used to identify defects as shown in Figure 65. A cell with one broken interconnect, highlighted in red, is shown in Figure 65 (A). In this region of the cell no voltage is being applied because of an electrical discontinuity somewhere in the cell interconnect ribbon. In Figure 65 (B) after aging the electrical conduction from the interconnect ribbon to the cell busbar has degraded. The cell on the left has a uniform luminescence intensity across the entire busbar whereas the cell on the right has high luminescence intensity only in particular regions. EL images can also be used to spot cell fracture, as shown in Figure 65 (C) where the soldering process itself appearss to have initiated several cracks.

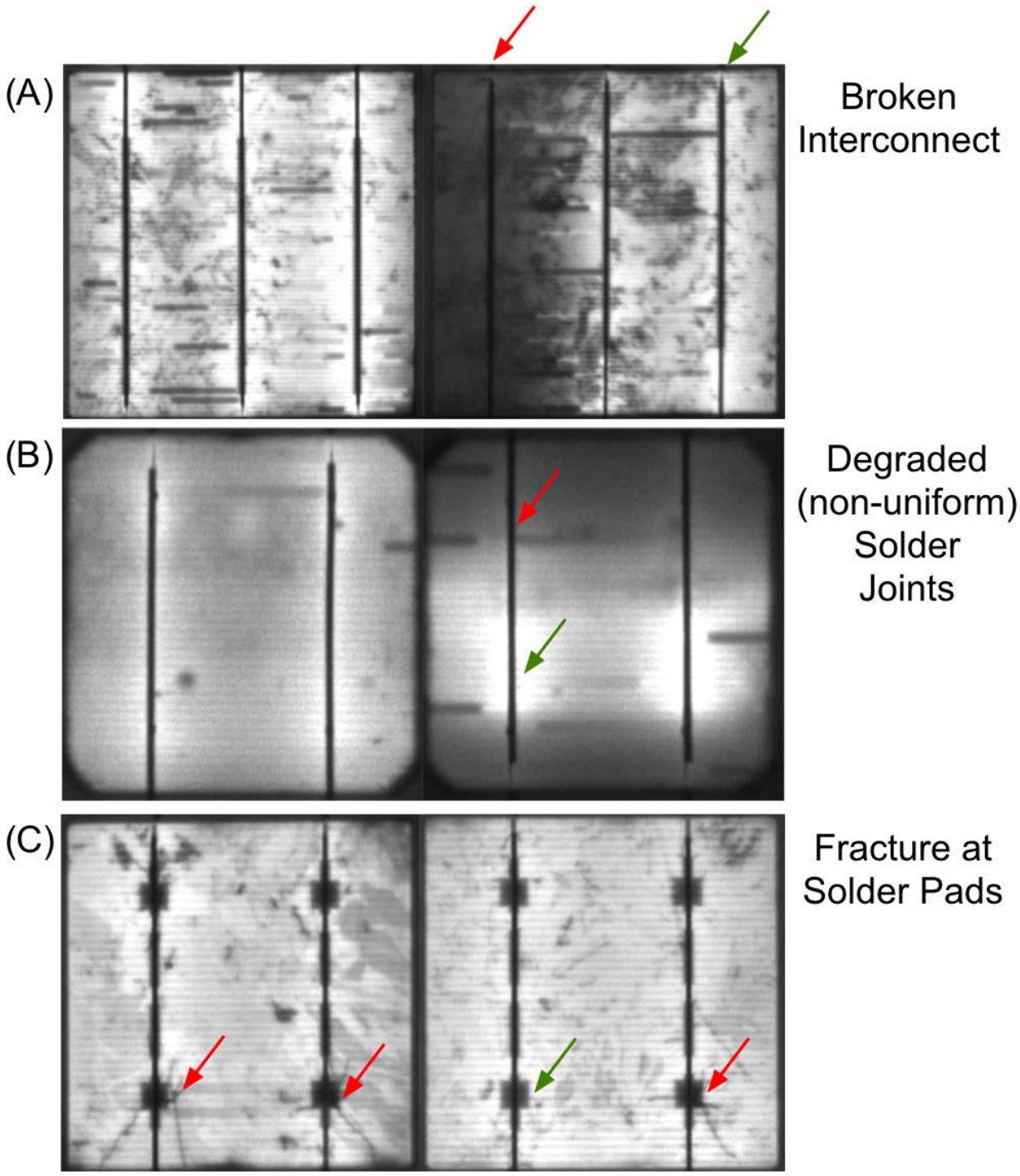


Figure 65. Example of module related defects; (A) broken interconnect highlighted in red, (B) degraded solder joint between the interconnect ribbon and the cell busbar, (C) cell fracture induced from the soldering process.

Although qualitative assessments are useful, it is difficult to assess the severity without some quantitative metric. In a module where cells are connected in series, it is not possible to

make a direct voltage measurement of individual cells. This restricts our ability to convert luminescence images into parameter maps as was done for individual cells. In a module, however, variation within a cell is not as critical. More important is evaluating the variation from cell to cell. When evaluating module loss, particularly in degradation studies, it is valuable to know if performance loss is due to one single cell, or is instead the result of uniform degradation of all cells.

To work towards a more a more quantitative evaluate consider again the basic luminescence equation.

$$I(x,y) = C(x,y)\, exp(\frac{V(x,y)}{V_T}) \qquad (26)$$

Instead of using the spatial dimensions, we will focus on using luminescence to quantify the operating voltage of each individual cell *i*. From the equation above there are two factors that influence luminescence. This includes the calibration constant, which generally accounts for optical variations, and the local voltage. For well contacted regions in the solar cell (*e.g.* near the busbar), the resistive losses in the emitter and contact fingers can be ignored. In essence, we are assuming that near to the busbar, the local voltage is equivalent to the cell operating voltage. As you move away from a busbar, the voltage will drop due to series resistance losses and this assumption becomes invalid. Pothoff *et al.* suggested that these locations, where resistive losses can be neglected, the highest intensity pixel is proportional to the operating voltage of the cell [82]. The second assumption needed is that the optical constant *C* is comparable on separate cells. This is reasonable in most cases.

Now we have a relationship between the highest intensity pixel (I^{i}_{max}) and the operating voltage of the cell (V_{op}). The sum of the operating voltage on all cells, including a small external resistance (*e.g*. leads, interconnects), equals the module voltage (V_{module}).

$$V_{module} = \sum_{i=1}^{N_{cell}} V_{op} = \sum_{i=1}^{N_{cell}} V_T ln\left(\frac{I^i_{max}}{C}\right) + R_{ext} I_{module} \qquad (27)$$

From this it is possible to determine the voltage of individual cells. Because all cells are in series, the current for each cell is equal to the module current. Furthermore, if this process is carried out at multiple operating points, *I-V* characteristics can be determined for individual cells. This presents a powerful use case for quantitative EL analysis; a non-destructive method to measure *I-V* characteristics for cells encapsulated within a module.

To test this method, the analysis was applied to two modules. The dark I-V characteristics were determined through the EL technique at a range of operating points. Then, using destructive methods, the actual characteristics were measured for each cell. The EL images for these modules are shown in Figure 66. These modules were unique in that there was extra space between cells that allowed us to easily contact the cells during the final destructive analysis.

After the destructive analysis was performed, the EL derived dark *I-V* characteristics were compared with the measured characteristics. For Module A, there is excellent agreement between the two. For module B, there is good agreement at high current values, but that relationship falls apart at lower currents. It appears that heavily shunted cells invalidate the basic assumptions of this model.

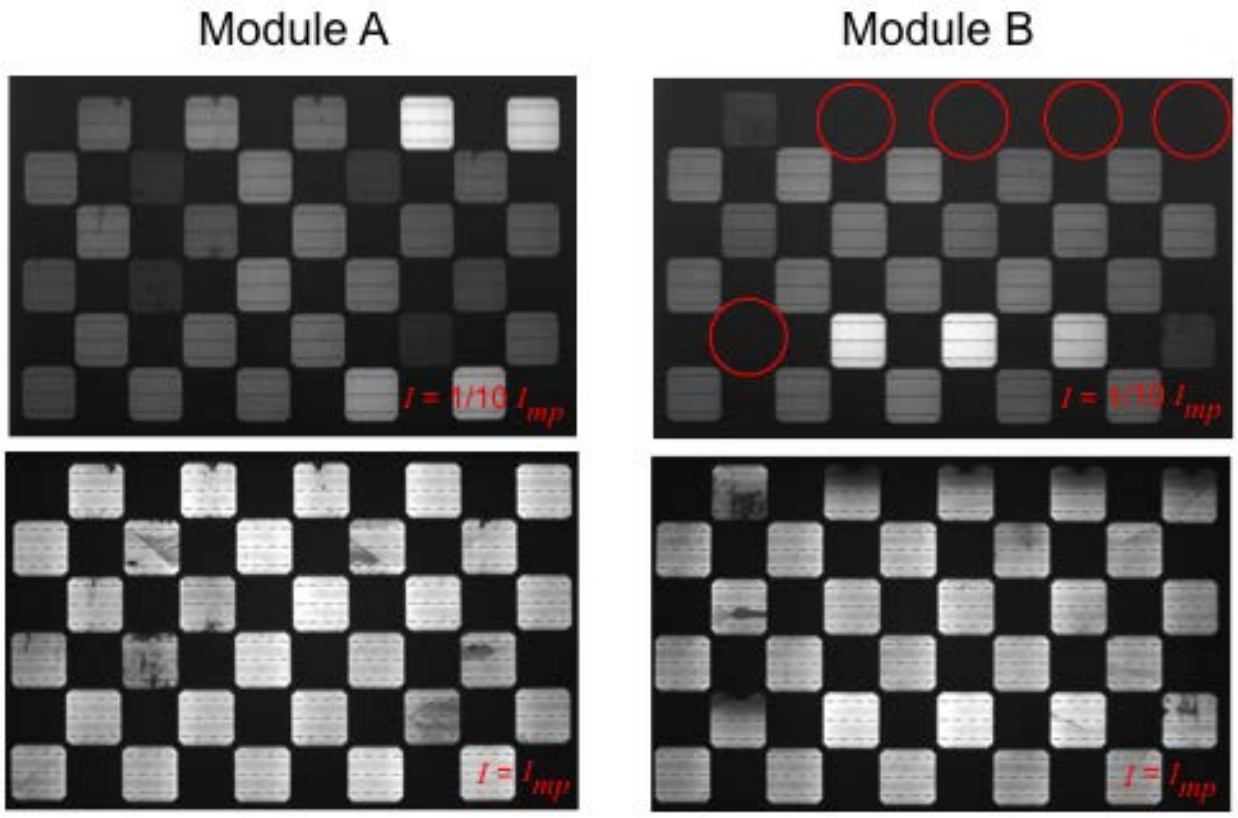


Figure 66. EL images at 1/10 I_{mp} and I_{mp} for both modules used in this study. The red circles highlight the 5 cells that have severe shunts.

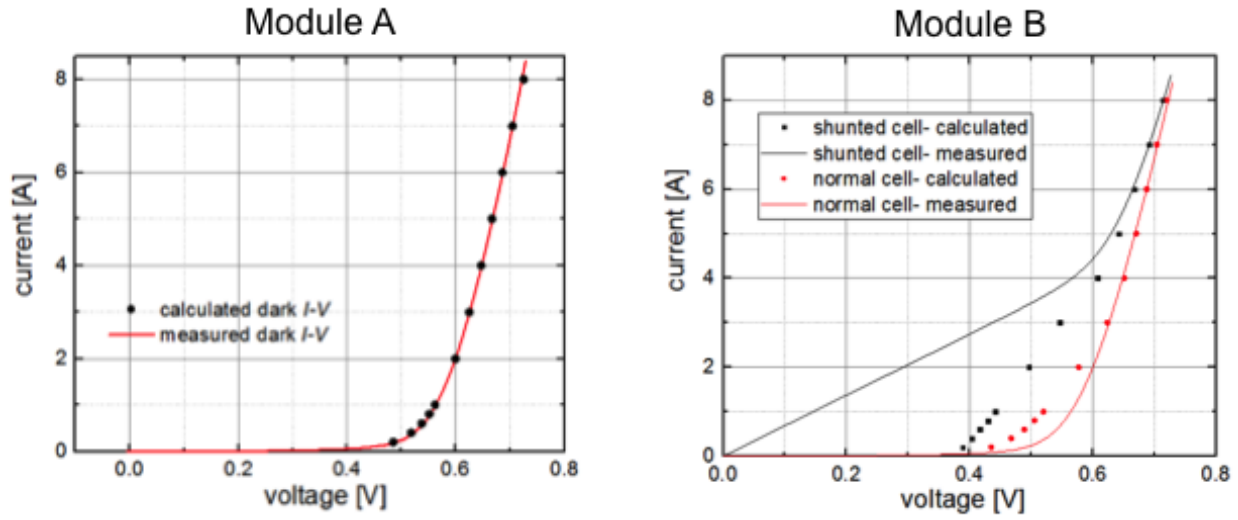


Figure 67. Comparison of electrical measurements with EL derived (calculated) data for select cells.

Along with general qualitative assessments, a series of EL images can be used to reconstruct dark *I-V* characteristics for individual cells. With the performance of each cell, a standard diode model can be applied to extract device performance parameters such as R_s and J_o. This cell level data is extremely valuable for quantifying module losses, allowing us to assign losses to individual cells if necessary.

5.2 Case Studies

5.2.1 Potential Induced Degradation

PV systems consist of one or more module strings, each made up of several modules connected in series, to reduce the balance of system costs. This arrangement leads to high system voltages that can reach up to 1000V. Safety requirements ensure that all exposed metal surfaces, including the module frame, are properly grounded. This results in some modules, specifically those at the end of each string, to experience a very high potential difference between the cell circuit and the module frame. Degradation arising from system voltage stress has been identified as a significant long-term failure mode in PV modules, known as Potential Induced Degradation (PID) [83, 84]. Studies have shown that the potential difference forces mobile ions, particular Na, from the glass into the cell [85, 86]. Once Na reaches the cell, it decorates crystal defects in the silicon (*e.g.* grain boundaries, stacking faults) creating shunt paths within the device and degrading performance.

A simple diagram is shown in Figure 68, where the conduction pathways are identified. It has been observed, in this work and others, that the cells nearest to the frame are most affected by PID. This is due to higher electric fields in this region, driving Na ions at a faster rate.

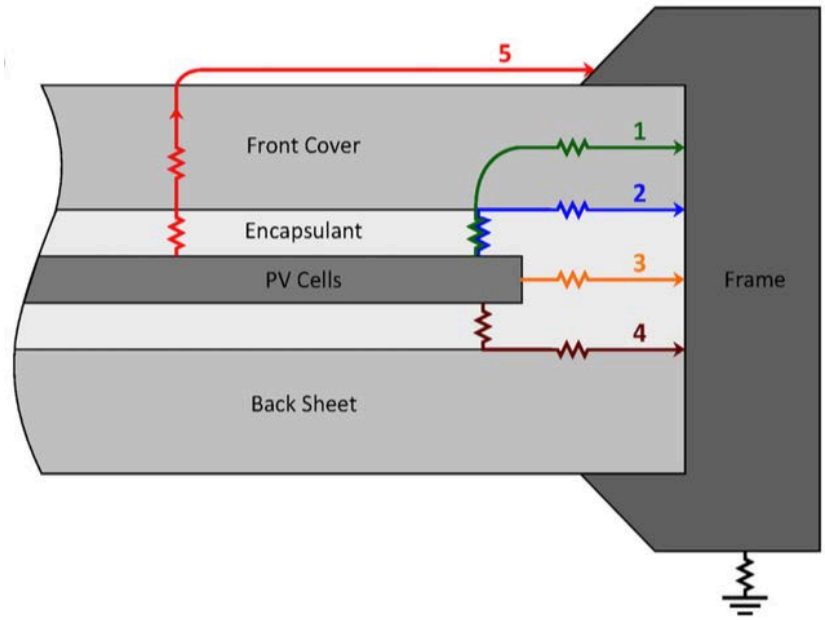


Figure 68. Cross section diagram of a PV showing the conduction pathways through the module packaging when a large potential exists.

Modules were deployed outdoors and an external voltage was applied to the module to replicate this type of potential difference. The performance of several module manufacturers was evaluated after 6 months of continuous application of voltage bias. This is an accelerated stress test because under normal operating conditions the voltage will only be present during daylight hours when the PV system is active.

Four types of modules of similar construction, using Al-BSF cells, EVA encapsulants, and standard backsheeets, were evaluated. For each type three modules were used. *I-V* characteristic both in the dark and with the solar simulator were carried out before and after the study. The performance analysis indicated that three module types were prone to this type of degradation, while one (type D) showed no loss in power. The power loss on the worst performing module was only 20% of its original value. The dark characteristics confirmed that this was indeed due to a reduction in the shunt resistance.

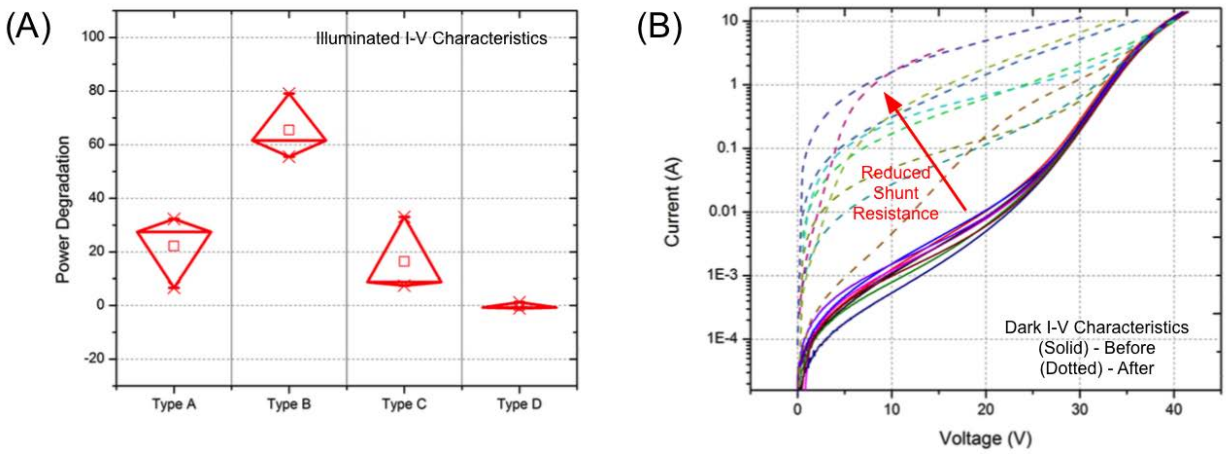


Figure 69. Performance of modules used in the PID study; (A) Power degradation for each module type, (B) Dark I-V characteristics showing a clear reduction in shunt resistance on all degraded modules.

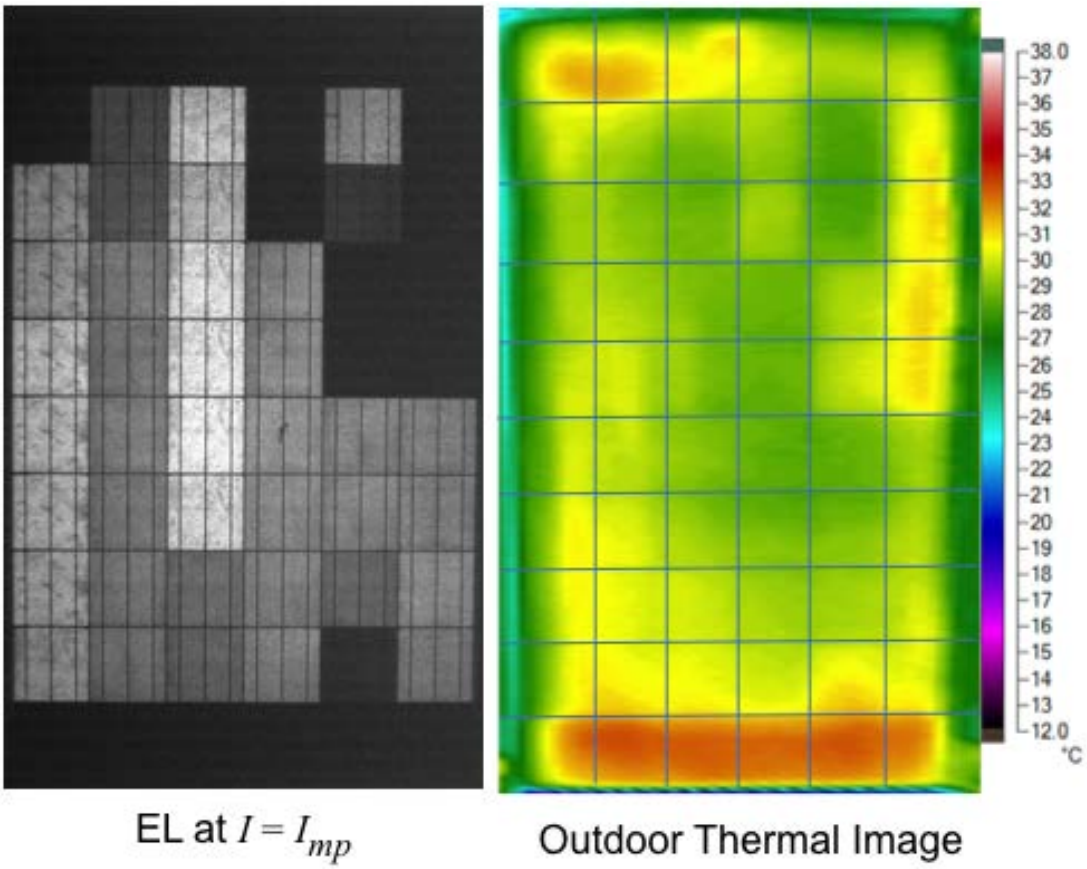


Figure 70. Electroluminescence image and thermal image of module showing PID degradation.

Imaging was carried out to identify which cells were most affected. As shown in Figure 70, the cells nearest to the edge of the modules where not visible in the EL image. These cells also exhibited excessive heating while operating in the field.

From this study it is clear that PID poses a clear reliability concern. At the time of this experiment, there was no qualification test that screened for this degradation mechanism. The performance of each module type used in this study varied drastically. It has been shown that modules of similar cost and construction do not perform similar with respect to system voltage stress. Of the modules tested, one group exhibited no degradation while another group degraded over 80%. The results from this study emphasized that the addition of a qualification test for PID was needed to verify the long-term reliability of the rapidly growing installation base of c-Si PV modules.

5.2.2 Ten-Year Aging Study

A system of approximately 150 modules were deployed at FSEC in 2004. After 10 years of operation these modules were uninstalled and characterized to quantify performance loss. The modules technology is very similar to that of today, utilizing a mono-crystalline Al-BSF cell architecture. The module packaging consists of an EVA encapsulant, tedlar backsheet, and low-iron soda-lime front glass. Since these older modules were manufactured a few design aspects have advanced. The size of the wafers has increased from 4-inch pseudo square to 6-inch pseudo square. Recent technologies also use at least 3 busbars, with many manufacturers opting for 4 or more. This helps with performance by reducing series resistance, while also creating a more durable fault tolerant design. Also, the cell thickness is likely much thicker than what is typical

today. This may imply that the cells within these older modules are more mechanically robust than more recent technologies. Lastly, the overall module size is much smaller than what is standard for new modules.

The typical PV performance characteristics were compared against their original values. As shown in Figure 71, the power has degraded to an average of 90.75% of their original performance. This degradation consists mainly of a loss in the short-circuit current and the fill factor, which is influenced by both the module maximum power voltage and maximum power current. The loss in fill factor was not consistent across all module; some modules showed a slight increase while the worst module exhibited a loss of 10%. There was also a small and consistent loss in open-circuit voltage on all modules. This performance can be summarized as an average loss in performance of just under 1% per year.

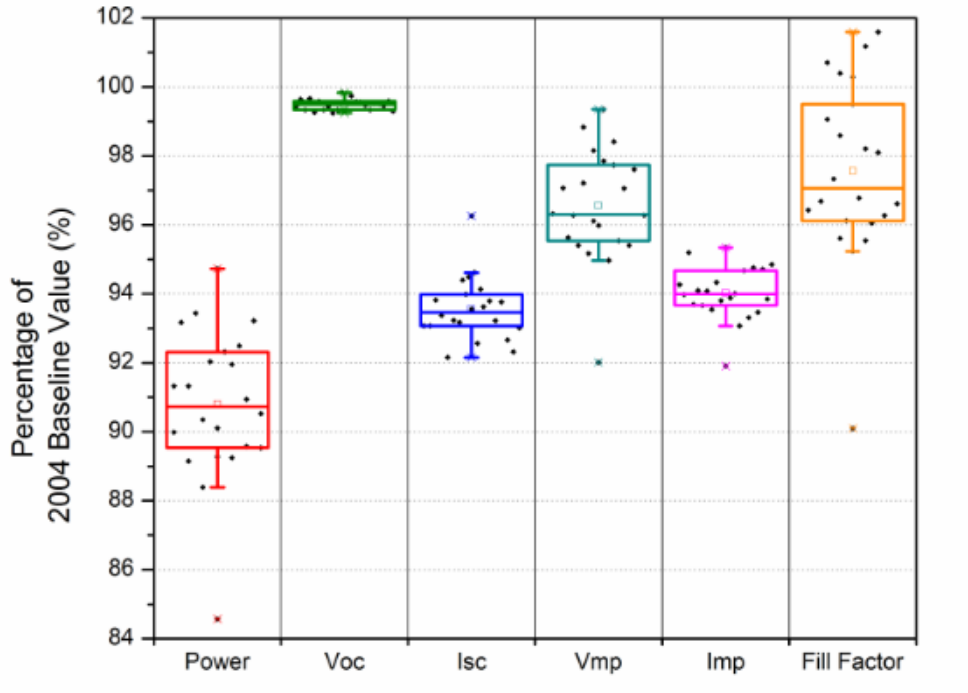


Figure 71. PV Performance parameters as a percentage of their original baseline values after 10 years of outdoor exposure.

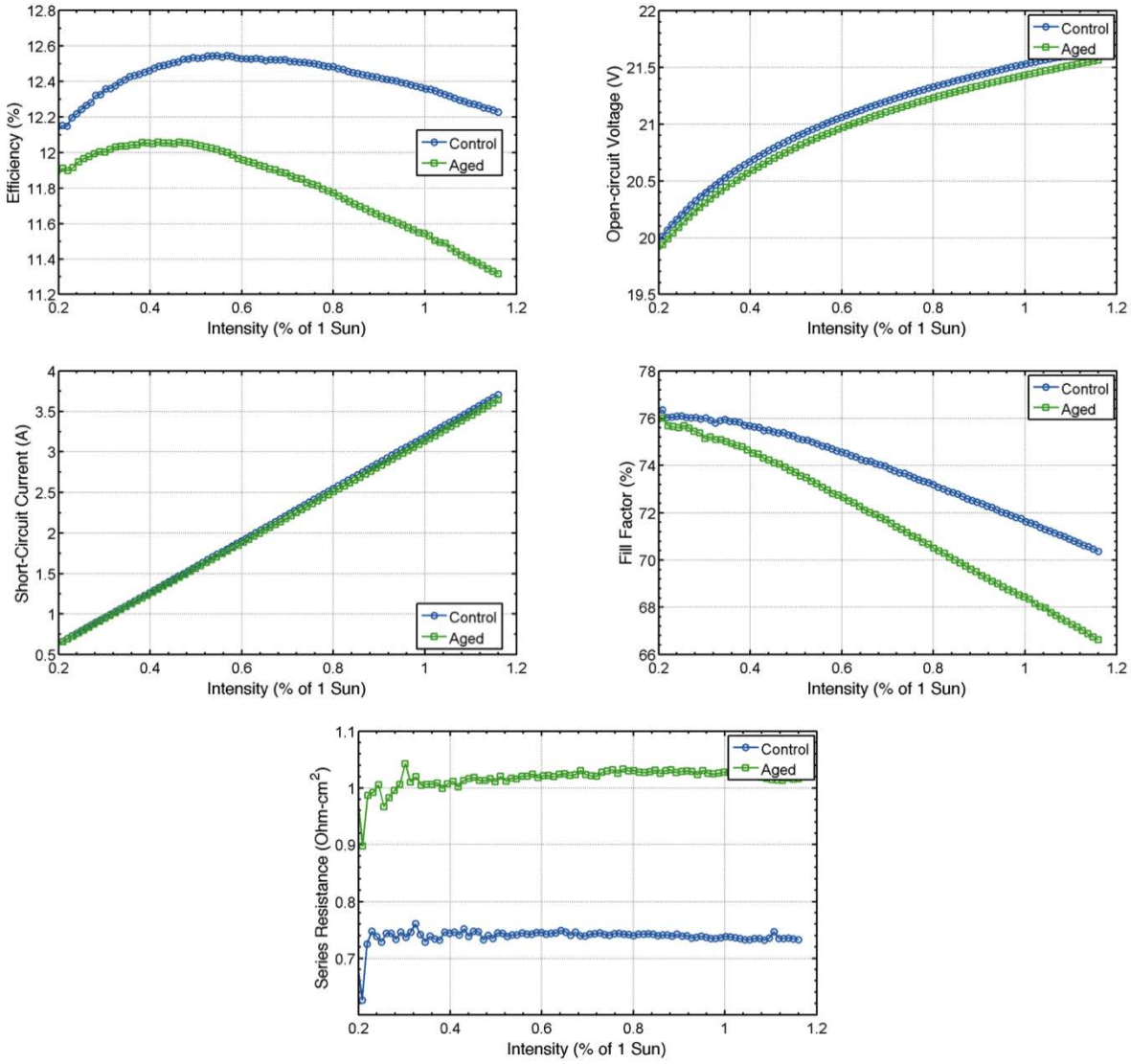


Figure 72. Analysis of two modules (control and aged) over a range of intensities for several performance parameters.

Several modules were kept indoors for the 10 year duration and were used as control modules in this study. Figure 72 shows the performance of a control module and an aged module over a range of intensities. This multi-irradiance analysis is valuable in identifying the particular degradation mechanisms impacting module performance. The open circuit voltage shows a small (0.5%) loss across all intensities. This is likely due to a mechanism referred to as Light Induced

Degradation (LID). LID refers to defect complexes, specifically Boron-Oxygen, that are activated as a result of extended exposure to illumination. These complexes are a bulk silicon defect that increase the recombination current within the device. The short-circuit current also shows a consistent ~5% loss over all intensities. A reduction in short-circuit current is indicative of optical losses. This typically occurs due to a degradation of the encapsulant, which is known to degrade after long term exposure to UV light. There is also a loss in the fill factor that increases along with the illumination intensity. The series resistance is the main reason for this loss. As the operating current increases (*i.e.* higher intensities), the voltage loss due to series resistance increases that in turn reduces the fill factor. All of these factors influence the efficiency reduction. The increase in series resistance appears to be the dominant loss mechanism, as indicated by the efficiency vs. intensity plot. At 1-sun the loss is nearly 10%, however this loss reduces at lower intensities. For example the reduction in efficiency at 0.2 suns is on 5%. This is critical to understand when assessing actual system performance in the field because the outdoor conditions are rarely at what is considered 1-sun.

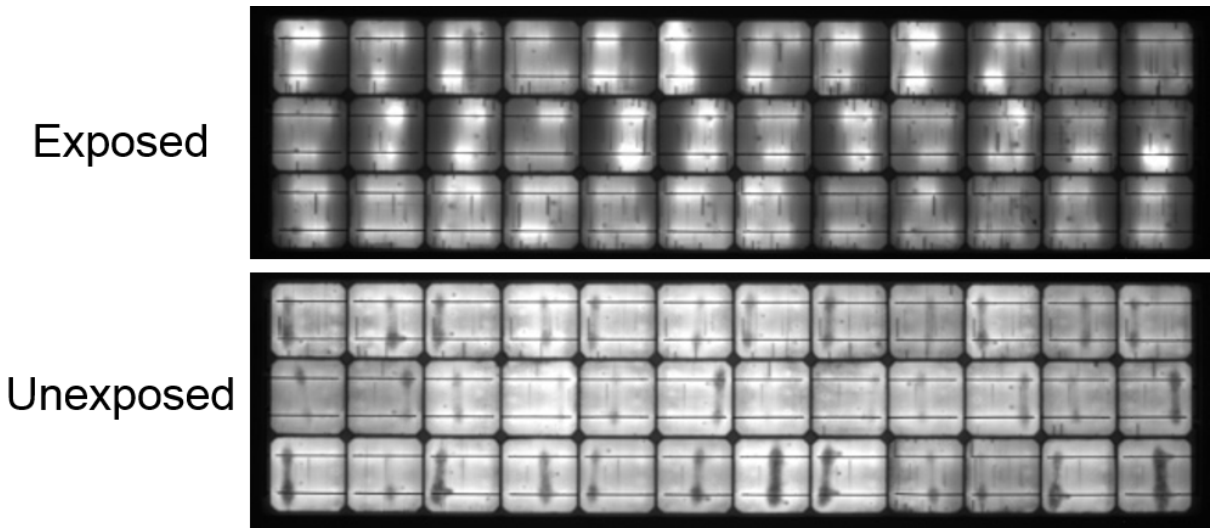


Figure 73. EL images taken with a forward current equal to I_{sc} for the control (unexposed) and aged (exposed) modules.

To identify the source of this series resistance loss, EL imaging was performed. The standard EL image for each module is shown in Figure 73. Here we can see a large reduction, and increased non-uniformity, of the luminescence intensity for each cell. This uniformity is the result of the degradation of the cell interconnect. This refers to the electrical contact between the cell busbar and the interconnect ribbon. The degradation is non-uniform both along the length of the busbar and from cell to cell. This explains the variation in fill factor loss observed among the larger group of modules.

To quantify this loss the multi-image EL analysis was performed to determine the dark *I-V* characteristics for each cell. The dark *I-V* characteristics are shown in Figure 74. The aged module shows a clear shift to the left for a majority of the cells as compared to the control module in Figure 74 (A). When an ideal diode equation is used to fit these *I-V* characteristics, performance parameters such as series resistance can be extracted. The series resistance for each cell is shown in the histogram in Figure 74 (B). From this analysis you can see that the series resistance has, on average, increased for all cells in the aged module. It is also clear that some cells exhibit more of an increase than others. The series resistance can then be mapped as shown in Figure 75 for the aged module. In this plot, red signifies higher series resistance and blue signifies lower series resistance. The cell with the highest series resistance and the cell with the lowest series resistance is also highlighted. It is now clear that the non-uniform illumination is a direct result of the increase in series resistance. Furthermore, the exact magnitude of this can be determined. For these two cells the difference is 0.56 ohm-cm^2. This study shows how the combination of mulit-suns *I-V* analysis and quantitative EL imaging can be used to identify the degradation mechanisms driving performance loss and quantify the impact on a cell-by-cell basis.

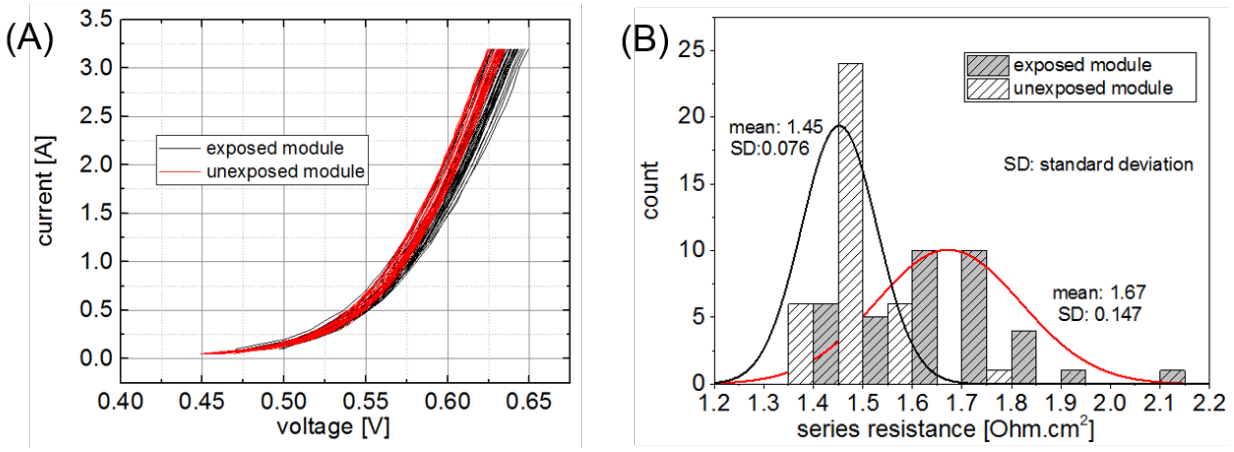


Figure 74. (A) I-V characteristics determined from the EL imaging technique for each cell in both modules and (B) the histogram of the series resistance for each cell as determined from fitting of the ideal diode equation to the curves in (A).

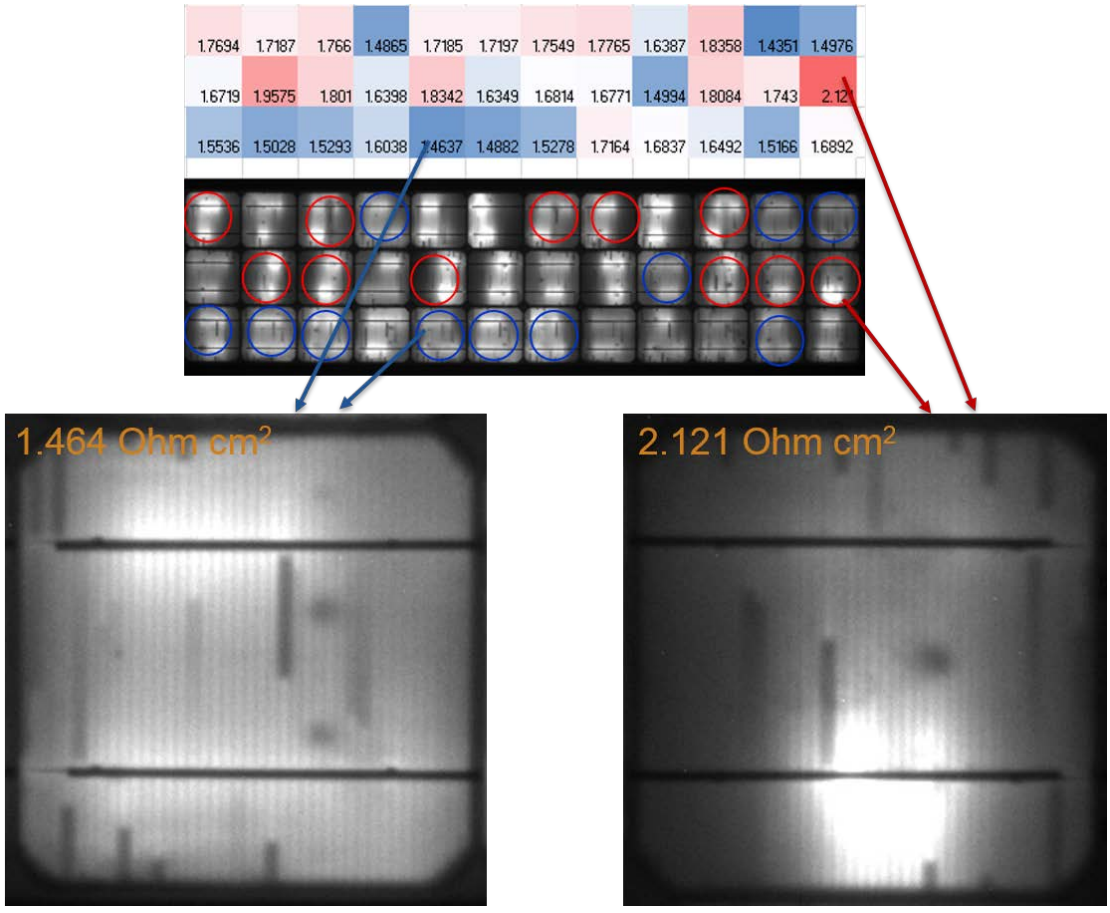


Figure 75. Map of series resistance for each cell, with the EL image for the cells with the highest and lowest series resistance.

5.3 *Conclusions*

This section identified the various challenges in obtaining accurate I-V performance characteristics in a laboratory setting. Specifically, illumination non-uniformity and spectral matching were identified as key drivers for high quality solar simulators. Additionally, the impact of multi-irradiance characterization was discussed in regards to its ability to pinpoint specific degradation mechanisms. Electroluminescence imaging was also explored as a method to capture cell-to-cell variation. A method of determining the dark *I-V* characteristics from a series of EL images was established and validated.

The analysis techniques were applied to two case studies. Accelerated aging with high voltage stress was used to investigate PID degradation. It was shown that modules of similar cost and construction did not perform equally in regards to PID. One module type showed little or no degradation while another module type exhibited degradation loss up to 80%. It was also shown through EL imaging that cells near the edge of the module degraded more than cells near the center.

A study investigating the performance of modules after ten years of exposure in the hot and humid environment of Florida was also carried out. The average degradation rate for this roof-top system was just under 1% power loss per year. Interconnect degradation was identified as the main driver for performance loss. Encapsulant degradation and LID also played a role in the reduction of performance. Finally, the quantitative EL analysis was performed to identify how interconnect degradation impacted the series resistance of individual cells. It was observed that degradation varied significantly from cell to cell with a maximum increase of 0.5 ohm-cm^2 for the lowest performing cells.

CHAPTER 6: CONCLUSION

Crystalline silicon photovoltaic technologies have enabled solar energy to become a viable source of electricity around the world. To drive further adoption, the cost of these PV technologies must continue to decline. This work explored the various ways in which metrology can be used to impact the economics of PV.

Advanced metrology is an essential element in the development of next generation c-Si PV technologies. In particular, spatially resolved methods allow for detailed analysis of local defects and their impact on device performance. This allows for a higher level of process optimization and will ultimately lead to better device performance. Metrology also has an important role in ensuring reliable long term performance of PV modules. With a deeper understanding of module degradation mechanisms and their impact on module performance, more robust module designs can be established.

Another critical function for metrology is in the optimization of the PV manufacturing processes itself. For manufacturers to reduce cost, maintaining high levels of product quality and production yield are critical. Understanding how metrology can be used for these purposes and quantifying their direct economic impact allows manufacturers to make informed decisions regarding the adoption and implementation of in-line metrology.

As the PV industry continues to look for new ways to improve performance and reduce cost, innovative metrology solutions are required. Several of these strategies are presented in this work. In addition, case studies were presented to highlight how these strategies can be implemented.

Key contributions of this work to the field of c-Si PV include:

- Development of an economic framework in which in-line metrology can be evaluated for PV manufacturing. This methodology was published to an online calculator in order to encourage adoption by the industry.
- Development of spatially resolved loss analysis methods to assess the impact of manufacturing defects on performance and to characterize process non-uniformity of finished cells.
- Development of advanced module performance characterization methods to identify degradation mechanisms and assess their impact on long-term performance.

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