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Investigation Of Breakdown Power During Electrical Breakdown Of Aligned Array Of Carbon Nanotubes

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INVESTIGATION OF BREAKDOWN POWER DURING ELECTRICAL BREAKDOWN OF ALIGNED ARRAY OF CARBON NANOTUBES

by

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ABSTRACT

Massively parallel arrays of single walled carbon nanotubes (SWNT) have attracted significant research interests because of their ability to (i) average out inhomogeneities of individual SWNTs, (ii) provide larger on currents, and (iii) reduce noise to provide higher cutoff frequency for radio frequency applications. However, the array contains both metallic and semiconducting SWNTs and the presence of metallic nanotube in an aligned array negatively affects the device properties. Therefore, it is essential to selectively remove metallic nanotubes to obtain better transistor properties. It was recently found that although such a selective removal can be effective for a low density array, it does not work in a high density array and lead to a correlated breakdown of the entire array giving rise to a nanofissure pattern.

In order to obtain a deeper understanding of such a correlated SWNT breakdown, we studied the breakdown power in the successive electrical breakdown of both low (< 2 /um) and high density (>10 /um) SWNT arrays. We show that the breakdown voltage in successive electrical breakdown increases for low density array while it decreases for high density arrays. The estimated power required for the breakdown remains constant for low density arrays while it decreases for high density arrays in successive electrical breakdowns. We also show that, while a simple model of parallel resistor network can explain the breakdown of low density array, it cannot explain the behavior for the high density array implying that the correlation between the closely spaced parallel nanotubes plays a big role in the successive breakdowns of the high density SWNTs.

dedicated to

my brothers and to my parents

ACKNOWLEDGMENTS

I'm very happy writing this page of my thesis. I have learnt a lot during these 2 years of graduate studies. Throughout this time I came across so many ups and downs in my life but my mentors, colleagues, friends and family members gave me strength to pass through these it.

First of all, I would like to thank to Dr. Saiful I. Khondaker who put the stepping stone in my research career. I have learned a lot from him not only about research but about life in general.

Secondly, I am thankful to my wonderful family for being so supportive all the time. My dad and mom have always been and will always be a source of inspiration for me. Whenever I felt low during these graduation days, I used to talk to them and they always infused energy in me.

Finally I would like to thank to all my group members Rakib, Feras, Daeha, Narae, Biddut, Shashank and Abrar who made lab environment cheerful and have always been so helpful to me.

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LIST OF ACRONYMS/ABBREVIATIONS

AFM	Atomic Force Microscopy
CNT	Carbon Nanotube
CNTFET	Carbon Nanotube Field Effect Transistor
DEP	Dielectrophoresis
DI – Water	Deionized Water
IPA	Iso Propyl Alcohol
MWNT	Multi Walled Carbon Nanotube
PMMA	Poly(methyl methacrylate)
RF	Radio Frequency
SEM	Scanning Electron Microscopy
SWNT	Single Walled Nanotube

CHAPTER 1: INTRODUCTION AND ORGANIZATION

1.1 Introduction

At California Institute of Technology, Richard Feynman envisioned the possibility of manipulating the material properties at atomic scale, manufacturing the objects that are nanometers (1nm = 10^{-9}m) in size, in his famous lecture 'There's plenty of room the bottom' in Dec 1959. [1]. He put the stepping stone for a field later become famous as "nanotechnology" in which size of object is so crucial that simply changing the size of the object one can actually change the electronics, optical, catalytic, chemical and magnetic properties of the material. Today, Nanoscience and Nanotechnology has emerged out as a major inter disciplinary field where Physics, Chemistry, Material Science, Biotechnology, Computational Science, Biology and Medicine all these fields converge. Here we are dealing with the object less that 100nm in size, it may only be few atomic layers thick, and/or it might have just few hundreds of atoms in it. After Feynman's lecture, a never ending quest of miniaturizing object and manufacturing devices at such a small scale got huge pace which led to new discoveries and developments of new instruments and techniques by which his vision became reality. This technological development led us to make electronic components much faster, increase the storage capacity of the devices and reduce the dissipation in the electronic devices [2]. Figure 1.1a show the first general-purpose electronic digital computer: ENIAC, developed by a team working for U.S. Ordnance Ballistic Research Laboratory (BRL). It weighed roughly 27 tones, occupied about 1800 square feet area and consumed 150kW of power. Figure 1.1b shows the Intel's recently launched atom processor which is much faster, smaller, lighter and cost effect.

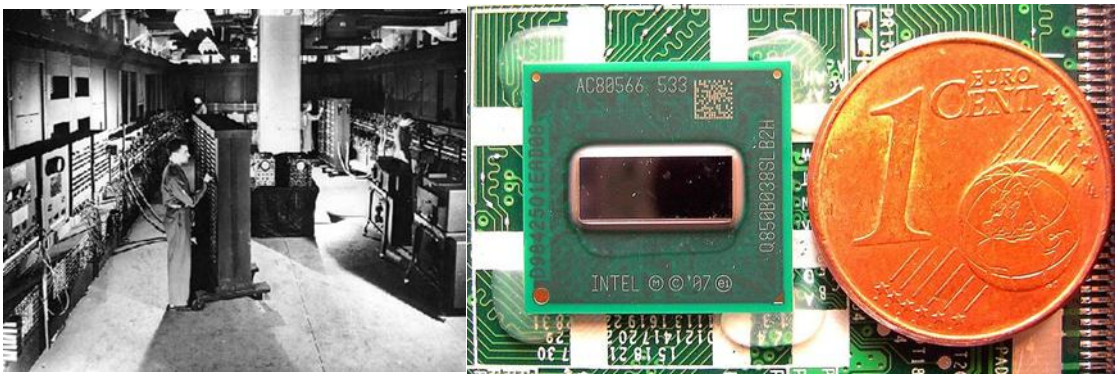

Figure 1-1 (a) The first general-purpose electronic digital computer: ENIAC. b) Intel's recently launched atom processor. For comparison of dimension, a Euro cent is shown next to it [3, 4].

All this miniaturization could happen because of the new tool and techniques that we developed in last 50 years which made us capable to fabricate the much smaller, faster and smarter transistors, which are the backbone of any electronic device. Field effect transistor which is a subpart of CMOS is the main point of interest and has been in focus since its invention in 1947. There had always been continuous efforts for make it smaller and smaller and faster in order to achieve ultimate goal of faster and better electronic components. According to Moore's law, the size of transistor reduces to its half in every 18 months. To keep this law valid, the semiconductor industry is going to hit 10 nm device ranges in this current decade. Figure 2.2 show a graph between time scale and device dimensions. As the size of Silicon based devices are decreasing, their fabrication cost is increasing exponentially. In addition to this, at nanoscale, charge leakage becomes predominant in such devices. So in order to overcome these limitations, current research has to think out of box and has to come up with non-conventional non silicon based devices which can perform at such small scale where quantum phenomenon are more important than classical laws of physics, where electron can tunnel through the nano gaps and where devices have the ability to show conductance near the transport limit [6, 13].

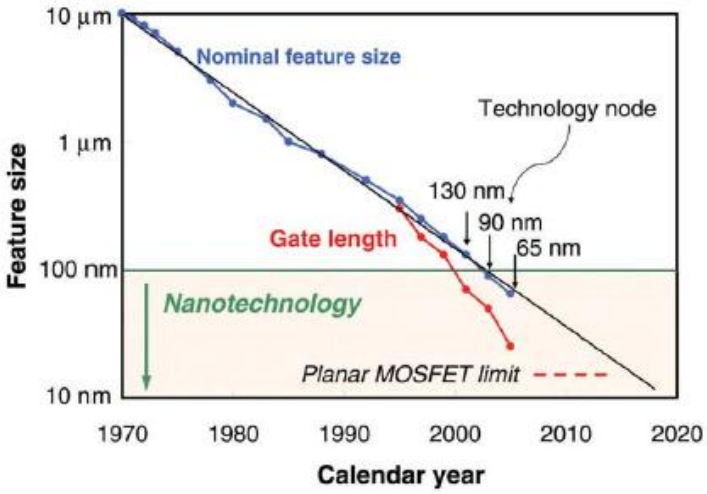

Figure 1-2 Moore's law showing the time scale vs. the transistor size [5]

In such scenario, carbon nanotubes based devices are seen as a potential candidate which could have the ability to function properly at such small scales. Aaron et.al have recently demonstrated low voltage performance of sub 10 nm transistor based carbon nanotubes [14]. Chuan et.al demonstrated carbon nanotube film transistor for flexible electronics which is not possible with Silicon based conventional TFT [16]. Kang et.al outperformed conventional silicon based transistor by aligned array CNTFET in terms of on current [9]. Another non silicon based transistor was demonstrated by Fuechsle et. al where they demonstrated double gate single atom transistor [15]. Although significant research have been done on CNTFET still there are many issues with non-silicon based transistor, for example there are a huge device to deceive fluctuations. Aligned array based transistors statistically eliminate such device to device fluctuations. In an aligned array CNTFET we electrical breakdown is commonly used to improve the device properties. In this thesis I have studied electrical breakdown in aligned array of nanotubes in details.

1.2 Organization of Thesis

In this thesis, I will first give a brief introduction and a general overview of the field followed by the motivation behind this work.

In chapter 2, I shall briefly discuss the current research on electrical breakdown, why electrical breakdown is important and some of its application in different areas. Here I shall compare other peoples' result/ techniques with mine.

In chapter 3, I will discuss various steps involved in fabrication of the device. Here I shall explain step by step all the processes starting from the choice of material, optical lithography, parameters for optical lithography, electron beam lithography, and design consideration for electrodes. After explaining the fabrication process, I shall further explain the assembly of carbon nanotubes by dielectrophoresis (DEP) method and its optimization. In the end of 3rd chapter I shall explain setup for measurement and analysis.

Chapter 4 will be focused on the results and discussion. Here I shall discuss the electrical breakdown in a low density aligned array and in high density aligned array, input power required per nanotube to break it electrically and the origin on correlated breakdown in sufficiently high density aligned array.

Finally, in 5th chapter of my thesis, I shall conclude all the results in brief and shall discuss the future scope and possibility of future research.

CHAPTER 2: MOTIVATION AND LITERATURE REVIEW

2.1 Motivation

Carbon nanotubes are considered as a potential candidate for the future nano electronic devices due to their exceptional electronic properties which includes near ballistic conduction [6, 21], very high mobility and resistance against electro migration [7, 8]. Figure 2.1a show a cartoon of a carbon nanotube field effect transistor (CNTFET) structure and figure 2.1b shows the scanning electron microscopy image of actual CNTFET device and it's zoomed in AFM image of channel showing single carbon nanotube in the channel. In this work, Javey et.al. showed room temperature conduction of single carbon nanotube device near ballistic transport limit ($4e^2/h$). However in the single carbon nanotube device, it is very difficult to control the chirality of carbon nanotube which causes large device to device fluctuations. One solution to get rid of this is to use an aligned array of carbon nano tubes which can statistically average out the device to device fluctuations in the devices [9, 19].

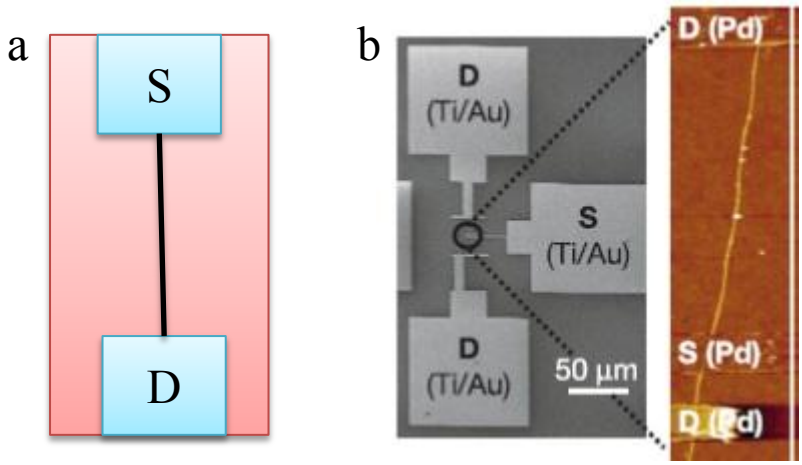

Figure 2-1 (a) A cartoon of single carbon nanotube Field effect transistor with global back gate geometry. (b) SEM image of actual CNTFET device and a zoomed in AFM image of the channel region in the device [6]

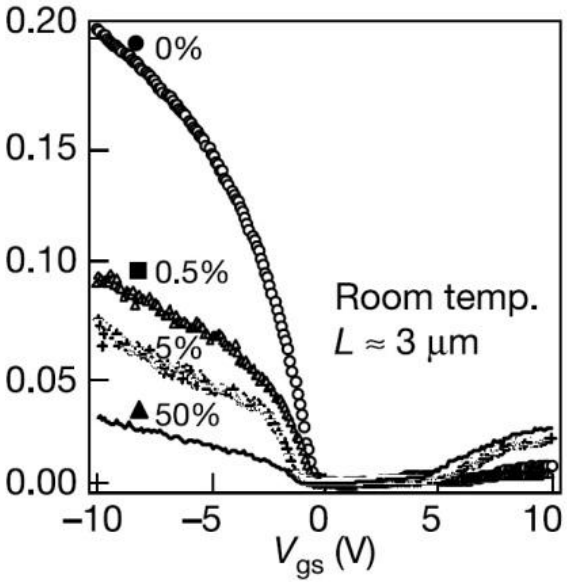

Figure 2-2 Transfer curve of single carbon nanotube device showing room temperature conductance near ballistic transport limit [6]

Figure 2.3 show a cartoon of aligned array device and figure 2.3 shows transfer curve of aligned array CNTFET. In addition to this, Kang et. al showed that aligned array devices provides us large ON current. A high ON current devices are also required for high frequency applications (RF applications). Compatibility of such devices with existing CMOS technology and freedom to choose a number of substrates make such devices even more promising for future applications. The disadvantage of aligned array of aligned array device is that the aligned array contains both metallic as well as semiconducting carbon nanotubes in it. The presence of metallic nanotubes hampers the device performance adversely because it is very hard to put them in OFF state. Hence it is of prime importance to eliminate metallic carbon nanotube selectively from the aligned array and to keep the high performance semiconductor carbon nanotubes in-between source and drain. Selective electrical breakdown has been suggested to eliminate the metallic

carbon nanotubes form aligned array [17, 20]. By selective elective breakdown, the on/off ration of the device can be improved by 10^3 orders of magnitude or more. Transfer curves before and after selective elective electrical breakdown are shown in figure 2.3b.

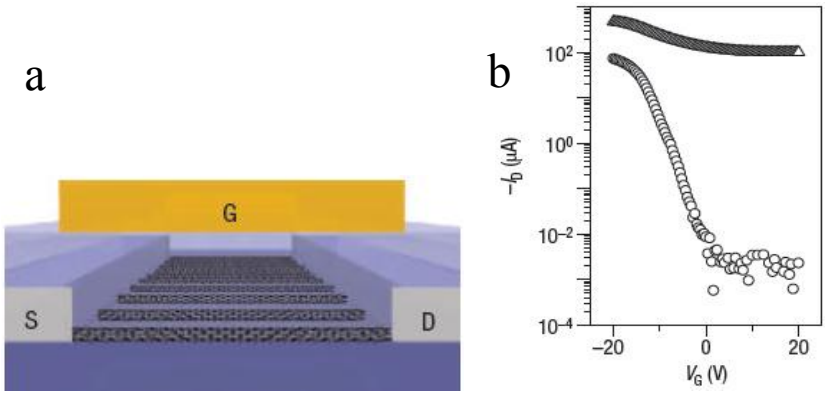

Figure 2-3 (a) cartoon of aligned array carbon nanotube FET device. (b) Transfer curve of aligned array device before and after electrical breakdown.

2.2 Assembly of Aligned Carbon Nanotubes

Alignment of carbon nanotubes in between source and drain is not a trivial task. There are many different methods by which CNT can be aligned. In this section I shall review two main techniques used to obtain aligned array of nanotubes.

2.2.1 Direct Growth Technique

Chemical Vapor deposition technique is widely used for the growth of aligned array of carbon nanotubes. This is a direct growth technique where the carbon nanotubes are grown directly onto the substrate with the help of metal catalyst [9]. First of all catalyst nano particles are patterned with the help of optical lithography or electron beam lithography and one desired pattern is obtained, a precursor gas is flown through the CVD chamber at 900^0C along with some inert

carrier gas (Ar or H_2). This method involves direct growth of CNT on to substrate but it involves high temperature processing and is not favorable for all kind of substrate and hence is not well compatible.

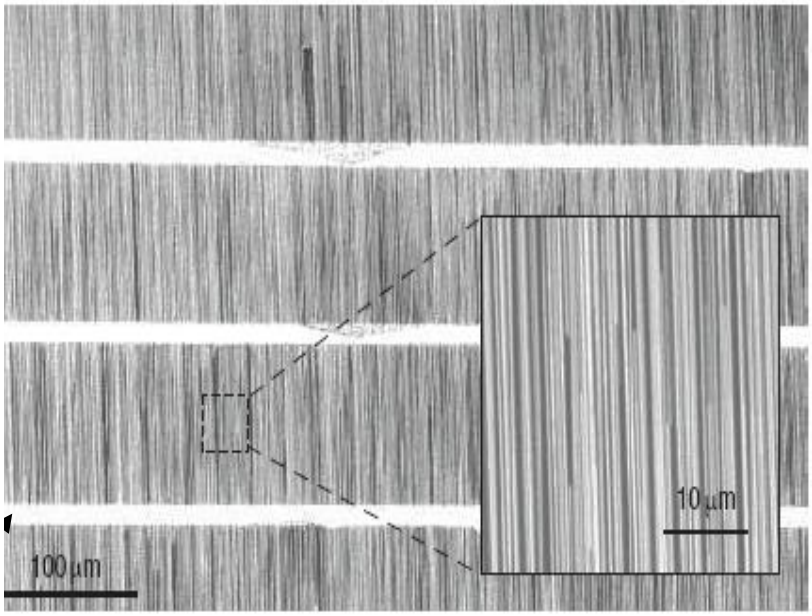

Figure 2-4 CVD grown aligned array of Carbon nanotubes [9]

2.2.2 Post Growth Technique For Alignment of CNT

Another technique widely used to align Carbon nanotubes in between source and drain is dielectrophoresis technique. Advantage of this technique is that it's less time consuming and it's very to assemble CNT. Also there is no high temperature processing involved in this method. This method has been explained in section 3.3 of chapter 3 in more details. Shashank et. al showed that by DEP method we can tune the density of Carbon nanotube by changing some of the parameter during the assembly. Figure 2.5 shows the aligned array assembled by DEP.

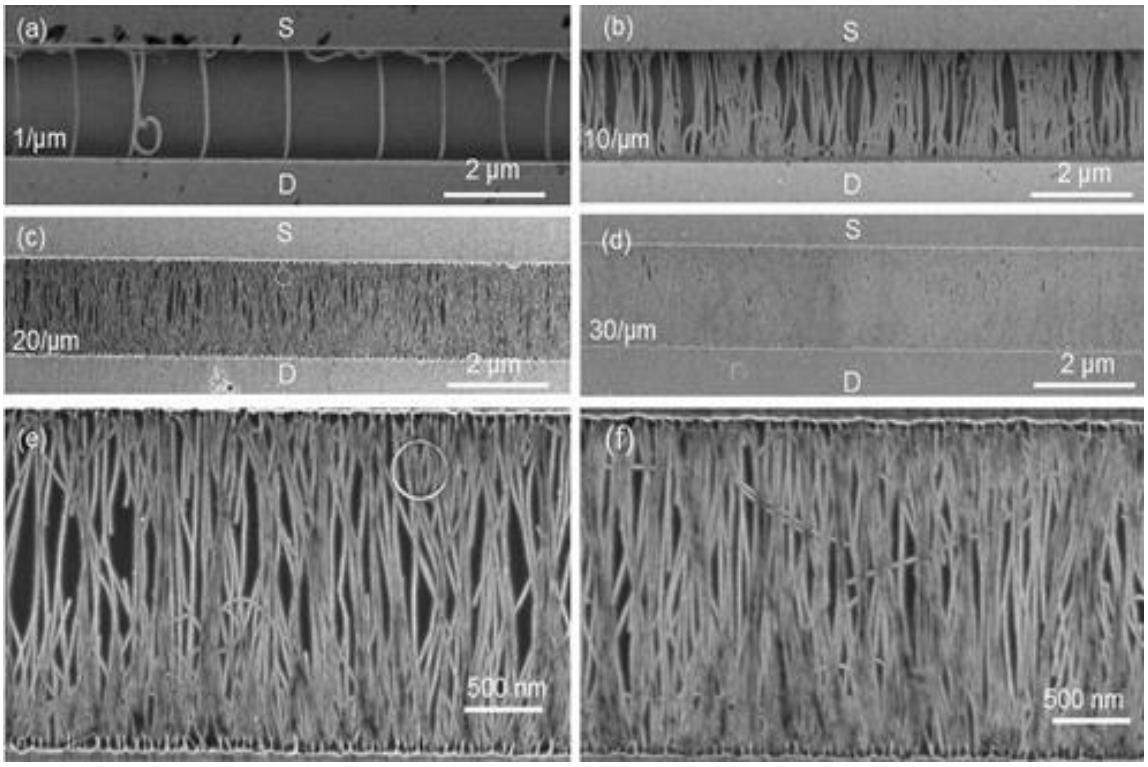

Figure 2-5 SEM image of aligned array of carbon nanotubes with varying nanotube density by DEP method [23]

2.3 Partial Electrical Breakdown of MWNT

Electrical breakdown has been suggested as tool to engineer the electrical circuits. Collins et. al showed the one by one removal of Carbon nanotube concentric shells in individual multiwalled Carbon nano tubes as well as in bundle of MWNT by controlled electrical breakdown [24]. Figure 2.6a shows partial electrical breakdown of MWNT at constant voltage stress proceeds in series of equally spaced discreet steps. With such a controlled partial breakdown, its possible to engineer the electronic properties of nanotubes

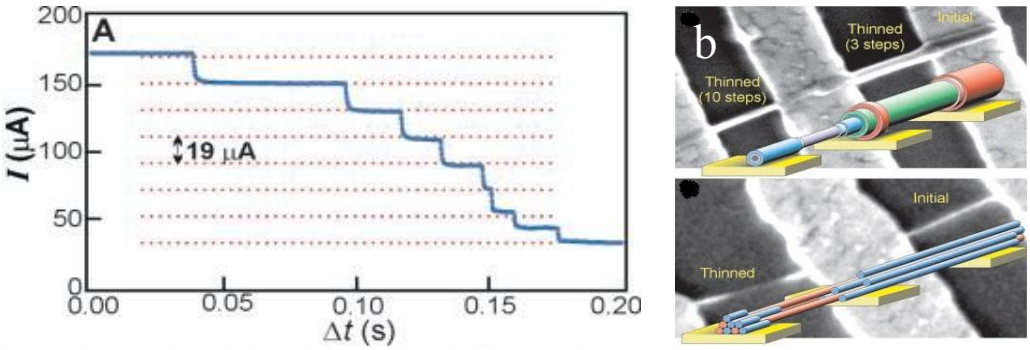

Figure 2-6 (a) Partial electrical breakdown of MWNT at constant voltage stress proceeds in a series of discreet steps. Each step corresponds to loss of one shell from MWNT. (b) Image of partially broken MWNT and a cartoon embedded in it.

2.4 Electrical Breakdown In An Aligned Array

There are several studies which show the improved device properties after selective electrical breakdown of carbon nanotubes [9, 18-20]. However In all of these studies, the CNT density per micrometer of channel length (D) was less than 3 CNT/μm [18]. So far none of studies has been done on devices with very high dense aligned array despite the continuous push to pack more and more CNT per micron in an aligned array [19, 20]. Also there is lack of information available that how many carbon nanotubes are getting broken and how many CNTs are intact, what will happen if D is very high, how breaking initiates in aligned array and how does it propagates, how much Joule heating is generated and how much power is required for this electrical breakdown. To answer these questions, we designed our experiment in such a way that we could shed some light on these problems. Shashank et. al showed that carbon nanotubes breaks at random site during electrical breakdown in an aligned array if the nanotubes density is less that 7 CNT/μm. If the CNT density is more than 7 /μm, there is a correlation among the breaking sites [23].

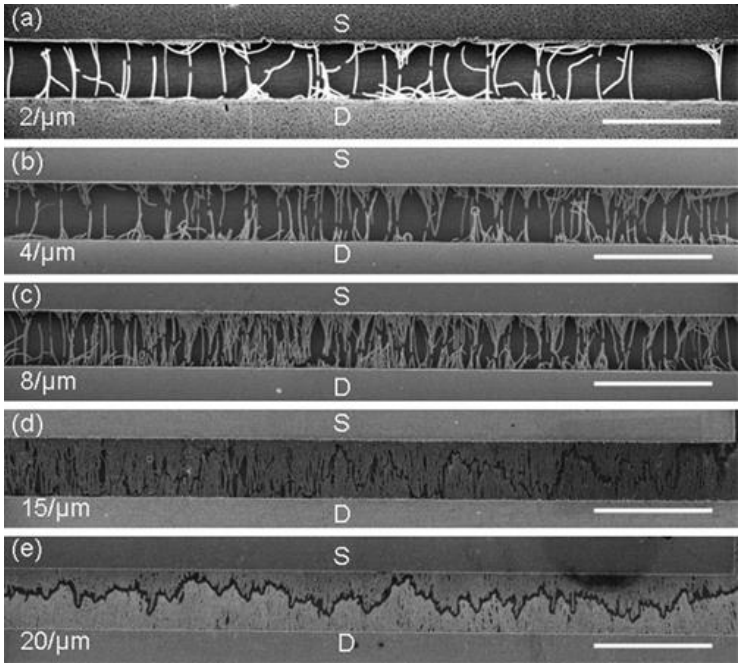

Figure 2-7 Electrical breakdown in an aligned array of different CNT density/μm. At low density (fig a & b) breaking happens at random sites whereas at high density (c, d & e) there is a correlated breakdown [23]

CHAPTER 3: DEVICE FABRICATION AND EXPERIMENTAL SETUP

3.1 Introduction

In this chapter first of all I shall discuss the fabrication of electrodes which involves two types of lithographies. 1) Photolithography and 2) electron beam lithography. I shall discuss all the steps involved in these two types of lithographies and our design consideration of electrodes. Later I shall talk about the choice of electrode material I have selected. After this I shall talk about the DEP method to assemble the carbon nanotubes onto the device and necessary parameter which must be considered while using this method. In the end I shall explain experimental setup for electrical breakdown

3.2 Fabrication of Electrodes

All the devices used for study in this thesis work were fabricated by Optical lithography, followed by electron beam lithography. In this way, we save time instead of fabrication the whole nano device with electron beam lithography. We have used the 3 inch (100) Si Wafer of sheet resistance 0.005 ohm Cm and of very high conductivity throughout for the fabrication of these devices in this work. The wafer had 250 nm SiO_2 layer on top of it and were micro-mechanically polished.

3.2.1 Photo Lithography

Photo lithography is a very powerful technique to fabricate the micro structures. Due to the wave length limitation of light and its diffraction, nanometer features size cannot be fabricated with photolithography alone. However photolithography provides a valuable platform to other nano – lithographies. We have used the single layer resist (Shipley S1318, from Micro Chem) spin coated at 5000 rpm and subsequently baked at 100^0C for 3 minutes for making optical patterns as

shown in figure 3(a). Shipley S1318 is a positive resist which means that we obtained exactly the same pattern on the wafer as we had on our optical mask. Karl Seuss mask aligner was used for UV light exposure to the wafer for 5 seconds. After the UV exposure, the wafer was developed in CD -26 developer for 30 seconds, rinsed in DI water and dried with dry nitrogen. All the steps involved in optically lithography process are chronologically shown in figure 3.

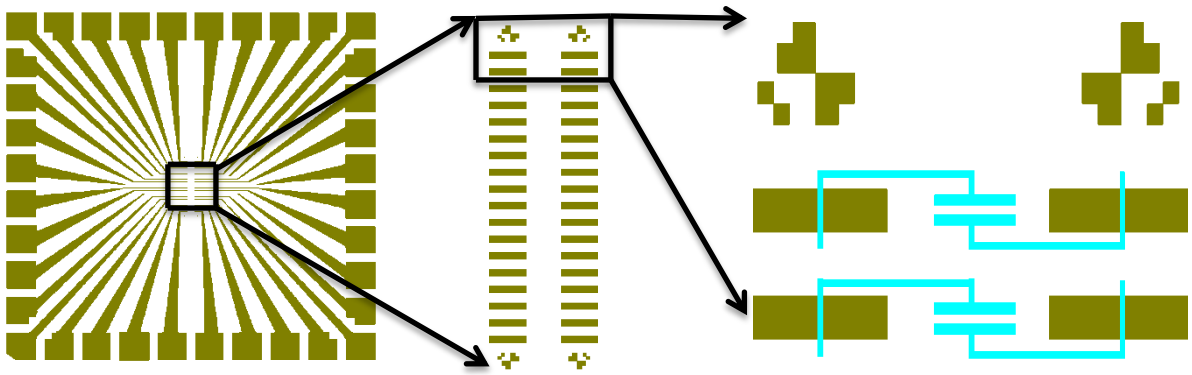

Figure 3-1 (a) Pattern of a chip after optical lithography. (b) Zoomed in image of the active area in figure 3a, (c) zoomed in area in figure 3b

3.2.1.1 Metallization

Once the wafer has been exposed to UV light and developed, I metallize the samples with Au. Since Au have less wettability to SiO_2 , it doesn't stick well with the surface. In order to overcome this difficulty I ve deposited 5 nm Cr layer as a sticky layer before evaporation of Au layer. By doing so I make sure that optical pattern doesn't peel off during the electrical measurement.

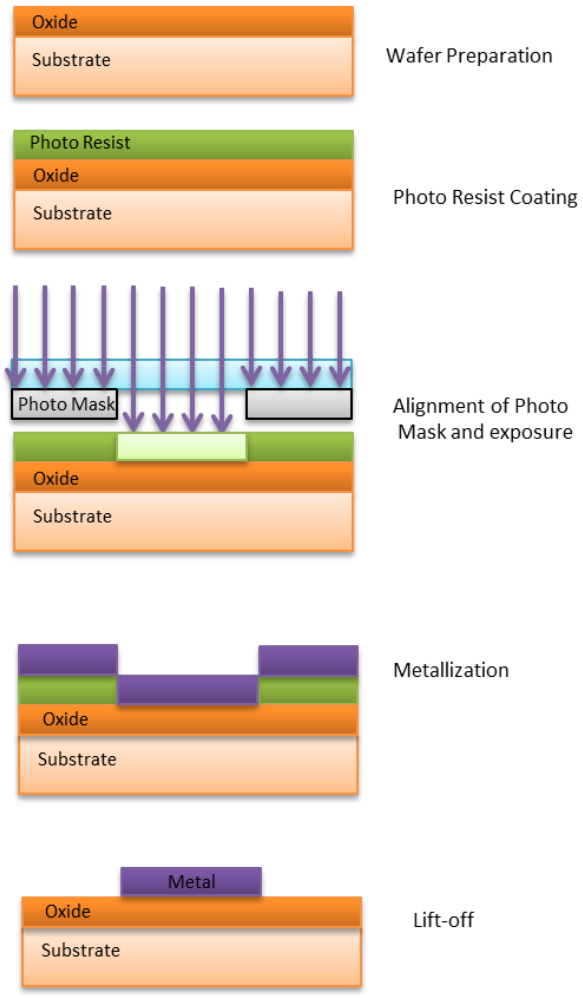

Figure 3-2 Systematic steps in optical lithography.

3.2.1.2 Lift Off

Lift off is done in PG remover (obtained for Micro Chem) for about 2-3 hours (depending upon life time of photo resist). While the wafer is still in PG remover, I check it under the optical microscope to make sure that the lift off is complete. If necessary I do the sonication for 10-20

seconds to have any extra metal removed. After the lift off is complete, I rinse the wafer with acetone, IPA and DI water and dry the wafer with dry nitrogen. Figure 3a shows an image of optical pattern image after liftoff.

3.2.2 Electron Beam Lithography

Electron beam lithography was used to make the smaller electrode patterns on previously optical lithographically made electrodes. I have made the electrodes of width 25 um and channel length varying from 2 um to 10 um. A single layer of Poly (methyl methacrylate) (PMMA 950K) was spin coated at 3000 rpm for 60 seconds which gives a thickness of 250 nm. PMMA is a positive resist and was purchased from MicroChem. After the PMMA spin coating, the devices were baked at 180^0C for 15 minutes. During the E Beam writing I exposed the sample with 300 uC/Cm^2 area dose at 28 KeV using the Zeiss Ultra 55 Electron Beam Lithography System in Material Characterization Facility, University of Central Florida. After the electron Beam writing, the samples were then developed with MIBK : IPA (1:3) developer solution for 70 seconds. I have used IPA alone as a stopper. After development, usual practice is to check the patter under optical microscope to make sure we got the right pattern at right place. The developed portion can be well distinguished from the undeveloped one from its optical contrast.

After this, the next step is metallization. I have used Electron beam evaporated for evaporation of Cr (as a sticky layer) 4nm at a rate of $0.1A^0$/m and 25nm Au at a rate of $0.4A^0$/m. Subsequent liftoff is done in acetone for about 3-4 hours (depending upon the life of resist).

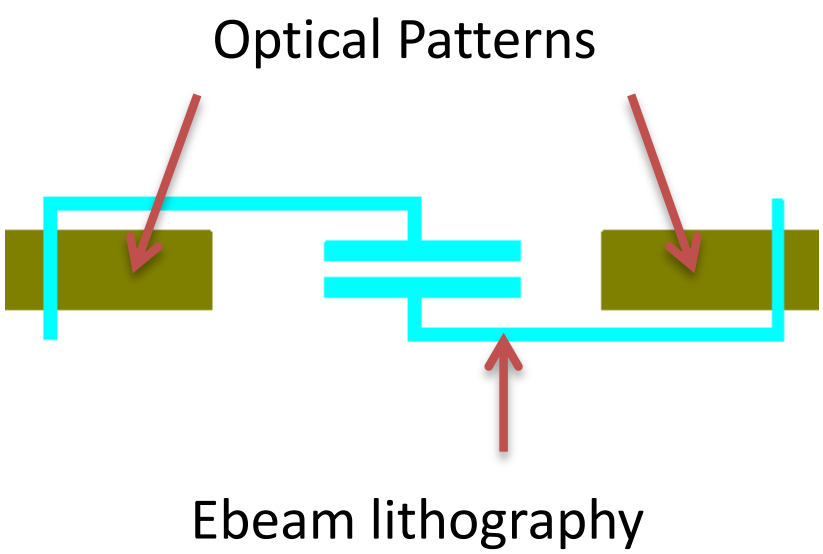

Figure 3-3 Design of electrodes made by electron beam lithography on optical patterns

3.3 Alignment Of Carbon Nanotubes By Dielectrophoresis (DEP)

To align the carbon nanotubes I chose the DEP method because it is easy to process yields high throughput and easily scalable method. Being a solution process method, this is also very very cheap method. For DEP one need the Carbon nanotubes well dispersed in solution form. We obtained solution of carbon nanotubes (99% single walled) from Brewer Science Inc. These CNTs were dispersed in water which make them suitable candidate DEP method. Another important factor is the size selection of nanotube. In order to have longer channel devices we need to have CNT solution which have much longer nanotubes. The solution I have used in this study from Brewer Science Inc. had average length of SWNT ~ 1.5 um and the average diameter ~ 1.7 nm. The mother solution was diluted 10 times, 50 times and tuned by changing the concentration of the solution.

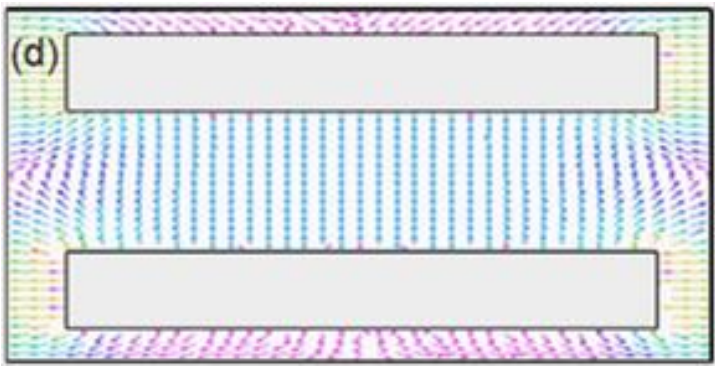

Figure 3-4 simulation of the electric field lines in between the two electrodes separated by 5 um gap.

Figure 3-4 show the simulation of the electric field lines produced during the DEP in between two electrodes. Simulation shows the uniform electric field lines in between the electrode except at the corners of the electrodes. In addition to Concentration of the solution there are other parameters which influence the density of nanotubes eg:

1) Driving frequency
2) Amount of solution drop casted
3) Voltage applied
4) Duration of time
5) Shape of electrode (not significant in this study)
6) Nature of electrode material

3.4 Experimental Setup For DEP

The experimental set up for Dielectrophoresis (DEP) is shown in figure 3.6. It consists of a osscilloscope, function generator, Optical mictoscope and probe station. The actual setup of

dielectophoresis is shown in figure 3.7. In order to trap carbon nanotubes in between the electrodes, I drop casted 3 µl of solution on to the prefabricated electrodes and applied 1MHz AC frequency for 30 seconds. This give rise to DEP force (F_{DEP}) between the two electrodes give by ε_p-εm

$$F_{DEP}\ \alpha\ \mathrm{Re}\left[\frac{\varepsilon p-\varepsilon m}{\varepsilon p+\varepsilon m}\right]\nabla|E|^2 \qquad (1)$$

Where F_{DEP} is the force due to dielectrophoresis, E is the electric field generated, εm is the permeability of the medium, ε_p is the permeability of the particle (in present case, it is CNT). By applying the electric, carbon nanotubes feels dielectrophoresis force and these CNT dispersed in non-polar solvent gets polarized and align themselves in the electric field line direction.

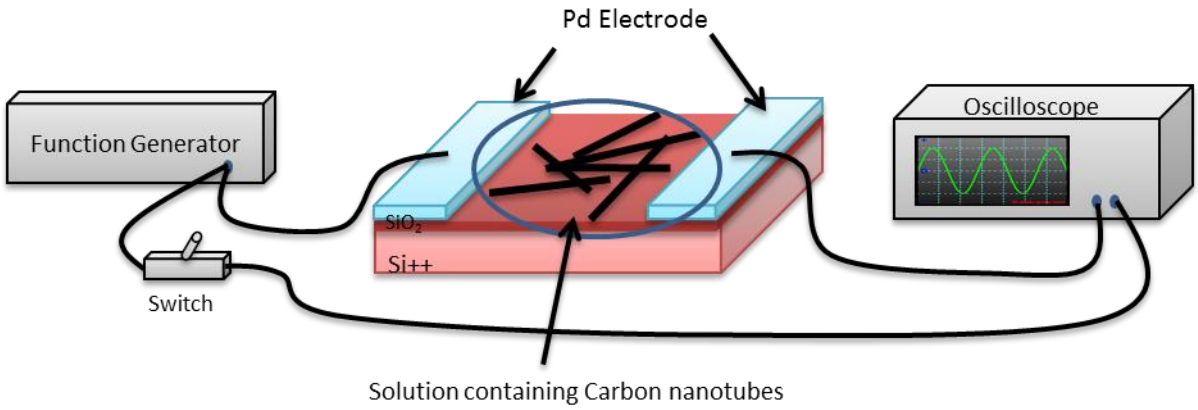

Figure 3-5 Systematic of the experimental setup for DEP (not to the scale)

A systematic cartoon for DEP circuit setup is shown in figure 3.5. It consists of an oscilloscope, function generator, a switch and a probe station. AC frequency signal sent to device was measured simultaneous with the oscilloscope at same time output signal was measured. The

actual experimental setup is shown in figure 3.6. Figure 3.7 show the AFM image of aligned array of carbon nanotube if low density as well as with high density and a zoomed in image of high density aligned array.

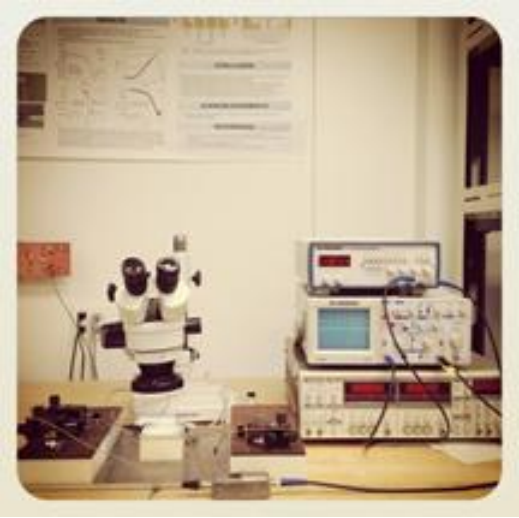

Figure 3-6 Actual setup for DEP to trap carbon nanotubes in between the electrodes.

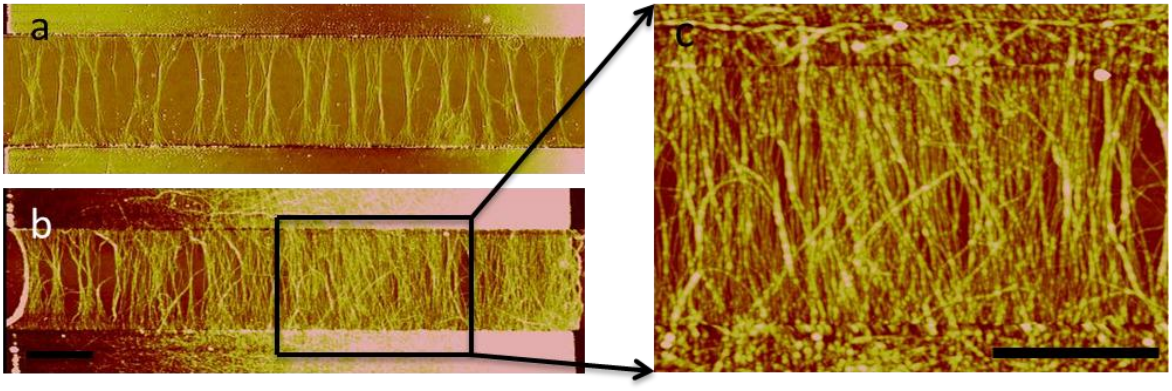

Figure 3-7 AFM image of aligned array of carbon nanotube with low density. (b) AFM image of an aligned array of high density (c) zoomed in image of (b). Scale shown in this image is 1 µm.

3.5 Experimental Setup For Electrical Breakdown Of An Aligned Array

The electrical breakdown setup is shown in figure 3.8. It consists of probe station, Keithley 2400 source meter, Keithley 6517A electrometer/high resistor meter and splitter. Output from Keithley 2400 source meter is fed into splitter which splits it into two and then these two outputs are fed in to source and drain of device. Keithley 6517A electrometer was used to apply the back gate voltage (not for all the cases). The whole setup was grounded (not shown in the diagram)

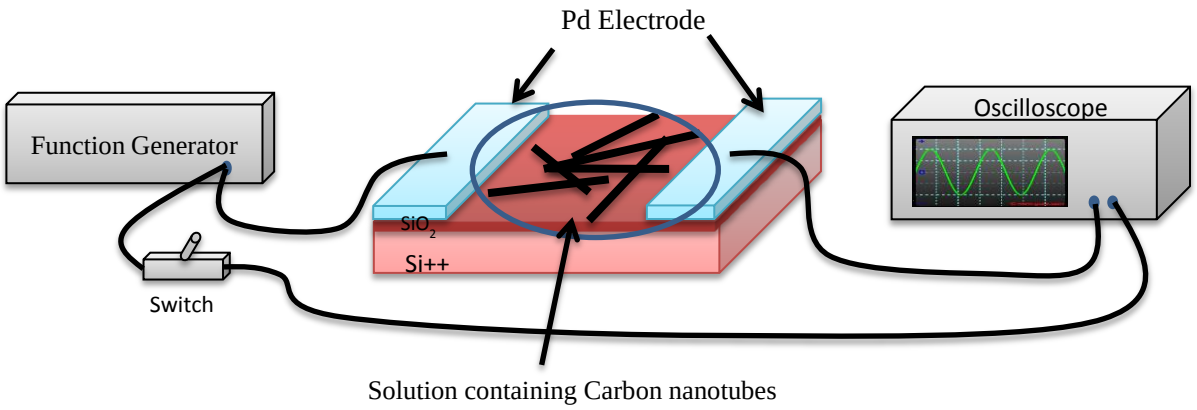

Figure 3-8 A systematic diagram of electrical breakdown setup.

CHAPTER 4: JOULE HEATING DURING ELECTRICAL BREAKDOWN IN ALIGNED ARRAY OF CARBON NANOTUBES

4.1 Introduction

In this chapter I shall discuss electrical breakdown of carbon nanotubes in an aligned array. I have divided this study broadly into two sections. First I shall discuss the breaking mechanism in low density (< 2 CNT/um) aligned array and then I shall move on the high density (> 10 CNT/um) aligned array. In addition to this I shall discuss the power required to break nanotubes in low density and high density aligned array. In the end of this chapter I shall show CNT density dependent electrical mechanism and explain the reason for particular kind of breaking behavior.

Carbon nanotubes due to their exceptional electronic properties, near ballistic conduction and other optoelectronic properties have been extensively used in the electronic industry. As explained in the previous 'Introduction and motivation' chapter, they are seen as a potential candidate for the future nanoelectronic devices. The electrical breakdown is caused by the internal heat produced inside the nanotubes due to Joule heating. The heat produce is given by

$$P = I^2 (R - R_c) \qquad (2)$$

Where I is the current flowing inside the aligned nanotube array, R is the electrical resistance of aligned array and R_c is the contact resistance at the metal (Pd) contacts. Here Pd metal has been chosen for metal electrodes particularly because Pd is known to have better contact with the carbon nanotubes and reduces the Schottky barrier [25]. Rc remain constant during the successive breakdown. Only resistance which is going to change with the successive breakdown is the resistance of aligned array.

4.2 Successive Electrical Breakdown In A Low Density Aligned Array Of Carbon Nanotubes

The IV curves of successive electrical breakdown for a low density aligned array (SEM image shown in figure 4.2) of carbon nanotube device are shown in figure 4.1. In order to get more insight into the breakdown mechanism, these breakdowns were performed in a more controlled way. A voltage was swept from 0 V and current flowing in the device was monitored. Current increases with the voltage and as soon as current starts to fall at certain breakdown voltage (V_{bd}), I stopped the bias voltage. Current corresponds to this V_{bd} is called breakdown current (I_{bd}). After the first breakdown, the voltage was swept again from zero until the second breakdown point and so on for the third and fourth breakdown point.

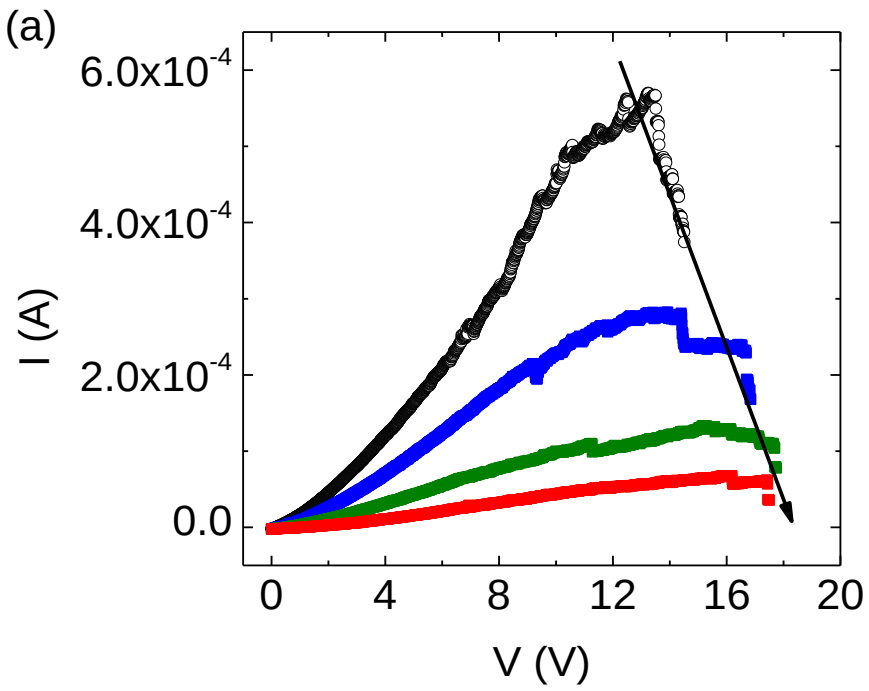

Figure 4-1 IV curve of successive electrical breakdown of aligned array of low density of carbon nanotubes in a device with geometry L= 25um, W =2um.

After the fourth breakdown current dropped completely to zero (curve not shown in this figure) indicates that there was no carbon nanotubes left intact in between source and drain. SEM image of actual device after each successive breakdown is shown in fig 4.2. The channel length of representative device was L = 2 um and the channel width W = 25 micron and the CNT density of aligned array is equal to 1.6 CNT/um. It is evident form the figure 4.2 that more and more nanotubes are getting broken after each breakdown. This is in well agreement with the IV curves shown in figure 4.2 that the current passing through the devices decreases after each breakdown.

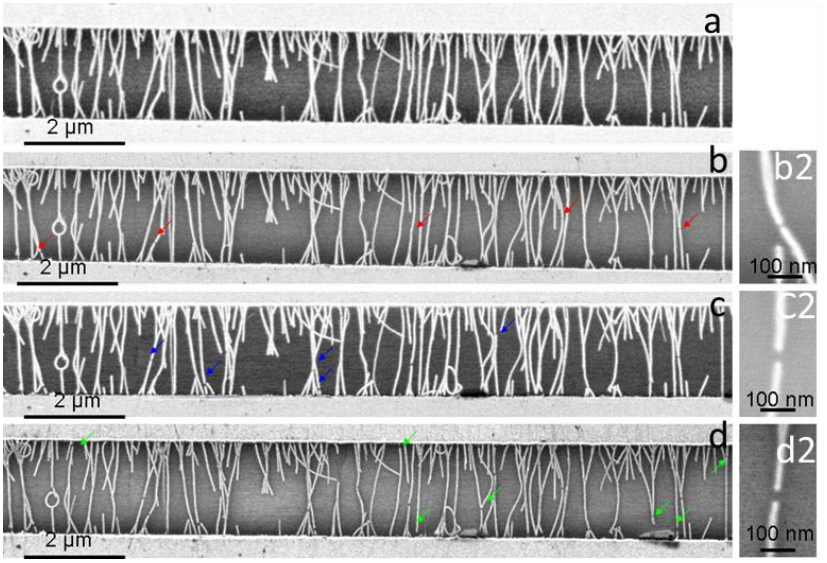

Figure 4-2 Successive electrical breakdown in low D aligned array of carbon nanotube. (a),(b),(c) & (d) shows the SEM image before breakdown after 1st , 2nd and 3rd breakdown respectively. (b2), (c2) & (d2) are zoomed in view of broken nanotubes after 1st , 2nd & 3rd breakdowns.

In order to get insight into the breakdown mechanism, it is important to carefully study the breakdown points in all successive breakdowns. The breakdown voltages V_{bd}, breakdown currents I_{bd} for all four breakdowns were extracted form IV curves of successive breakdowns. Based on these points, we calculated the total power at those points. Figure 4.3(a)&(b) show the

breakdown voltages and breakdown power at each successive breakdown point. It is evident from the figure that the breakdown voltage V_{bd} for each successive breakdown for a device with low D value (D < 2 CNT/μm) increases after each breakdown. On the other hand, the breakdown current (I_{bd}) decreases successively. From here, we calculated the total power required at each of these successive breakdown points and is shown in figure 4.3c. It is clear from this figure that P_{bd} also follow the similar trend as that of V_{bd}. A total of 5 devices were measured and their mean values are shown in the figures.

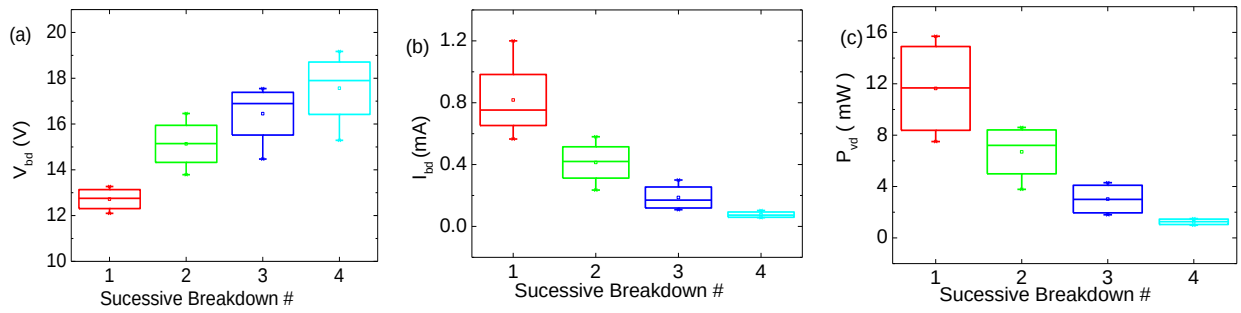

Figure 4-3 For low D aligned array, (a), (b) Breakdown voltage and breakdown current required at each successive breakdown for 5 devices. (c) Power required at each successive breakdown point for those 5 devices

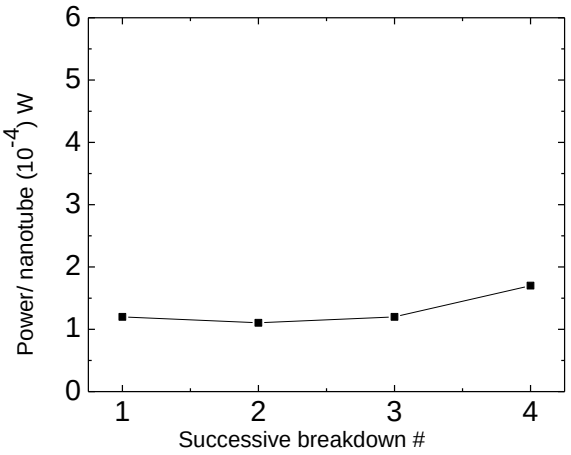

Figure 4-4 Breakdown power required per nanotube vs. the successive breakdown # in an aligned array with CNT density 1.6 nanotubes/ um

Going one step further, we calculated the power required to break one single nanotube in an aligned array. We have calculated this power/nanotube by dividing the total power required by the total number of nanotubes. Figure 4.4 shows the power required per nanotube at each successive breakdown. It has been found that the power per nanotube remains almost same approximately 0.1 ~ 0.2 mW for these devices with low D after each successive electrical breakdown. In order to test the variability in the result, total of 5 devices were used for this study. Results obtained from all of these devices were consistent and matched well with each other.

4.3 Analogy With Parallel Resistor Circuit

The above result can be explained by considering each carbon nanotube as a resistor in parallel resistor circuit shown in figure 4.5a, whose resistance values change slightly from each other. Such an assumption is justifiable because all the carbon nanotubes used in this study were synthesized by same method so their resistance values are very similar to each other with slight variation due to local distribution of defect inside them. By saying an aligned array of carbon nanotubes shown in figure 4.2 analogous to parallel resistor circuit shown in figure 4.5, we mean that current flow in one carbon nanotube does not affect the current density distribution in nearby nanotube the same way as the current flow in one resistor in parallel resistor network does not influence the flow of current in nearby resistor. Breaking mechanism in such an independent aligned array of nanotubes would be very similar that of breaking mechanism of resistor in parallel resistance circuit.

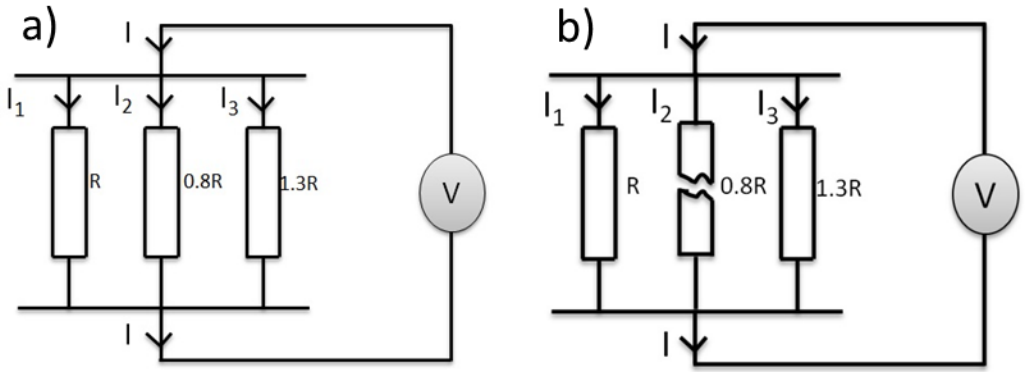

Figure 4-5 Parallel resistor circuit analogous to carbon nanotube aligned array device. a) Shows that all the resistors are intact and current gets distributed in them according to Kirchoff's law. b) Shows that that the resistor with lowest value will break first

In order to explain breaking mechanism in more simplistic and quantitative way we have assumed a resistor circuit with only three resistance connected parallel to each other. The total resistance of this network is given by

$$R_{tot} = \frac{1}{\frac{1}{R}+\frac{1}{0.8R}+\frac{1}{1.2R}} = 0.32\text{R } \Omega \qquad (3)$$

Here I have assumed the R is the average resistance value of resistance and other two resistors (shown in figure 4.5a) vary slightly from this average value. Now as the voltage is swept, current start to flow in the parallel resistor and it gets distributed among the different branches according to the Kirchoff's Law; smaller the resistor is, more the current flowing through it. Hence the resistor with resistance 0.8R will get the maximum share of total. Now since the Joule Heating, ($J \alpha I^2 R$) is proportional to square of current flowing in it, the resistor with least resistance will heat up more as compared to other resistors. As we keep on increasing the voltage, the more and more current will flow through the smallest resistor and eventually it gets burned out. The total

resistance of the circuit shoots up (from 0.32R Ω to 0.55R Ω) and the total current will redistribute itself again according to Krichoff's Law. Since the resistance of circuit increases after the first resistor in the circuit got burnt out, the current in the circuit decreases. In order to bur out second resistor, a larger current should pass through the circuit, which can only be achieved by applying higher voltage. In this way starting from the smallest resistor, all other resistors will get burns out one by one as the value of current flowing in them reaches the critical value at higher and higher voltages.

This situation is very similar to our device (with low D) where we have aligned array of carbon nanotubes each of which slightly vary in their resistance from each other. In the actual device, when a voltage is swept, the CNT with smallest resistance will get broken first the same way as resistor did. The breakdown of second carbon nanotube will happen at higher voltage as explained in resistor case. In the same manner CNT with second lowest value and third lowest will burn out at higher and higher voltages. This explanation satisfies our results shown in figure 4.3a where we have shown that V_{bd} increases after each successive breakdown.

The position of CNT in an aligned array does not affect the breaking mechanism. In other words the electrical breakdown in an aligned array with low D (< 7 nanotube/um) [10] gets initiated from CNT with low resistance. Also within a nanotube, breakdown occurs due to joule heating at randomly distributed defect sites in them. Due to this reason, we see a randonm breakdown in an aligned array of CNT with low D. Random breakdown have also been reported by other researchers [11,12].

In order to check whether this breaking mechanism is geometry dependent or not, we have also performed same experiment on devices with different geometry (W= 25um and L = 5 um, 10 um). We have observed the same results with these geometries as well.

4.4 Successive Electrical Breakdown In A High Density Aligned Array Of Carbon Nanotubes

In this section I shall explain the electrical breakdown mechanism in devices with high D (>10 CNT/μm). The IV curves of successive electrical breakdown of such a device with a high D is shown in figure 4.6. Experimental details have already been discussed in section 4.2. Again these experiments were performed on devices with different geometries to check if the breaking mechanism is geometry dependent or not.

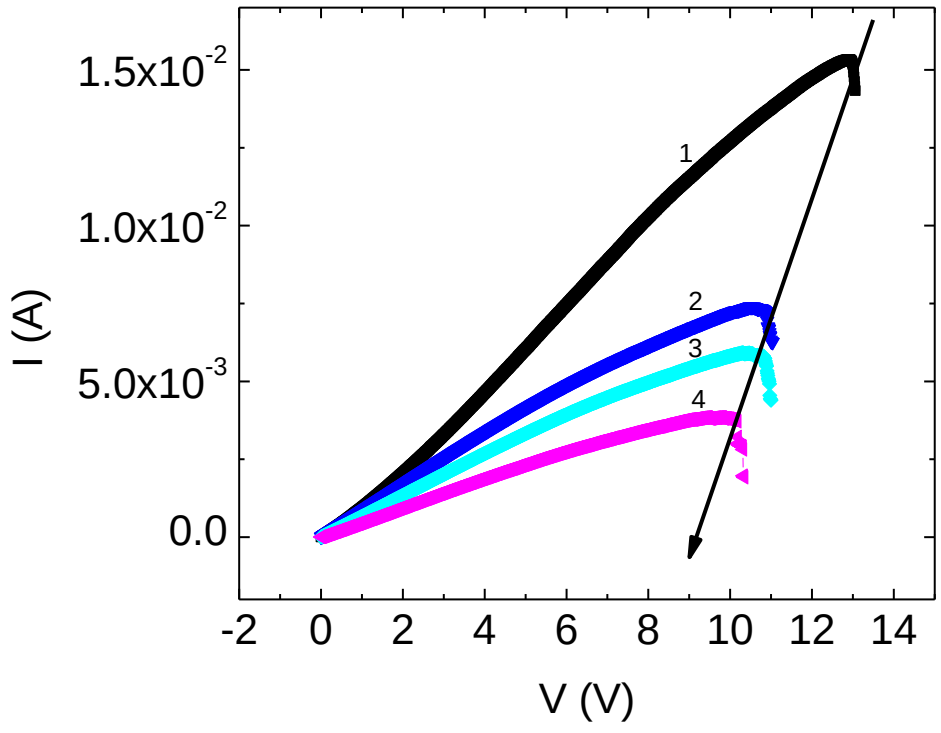

Figure 4-6 IV curve of successive electrical breakdown of high density (> 11 CNT/um) aligned array of carbon nanotubes in a device with geometry L= 25um, W = 2um.

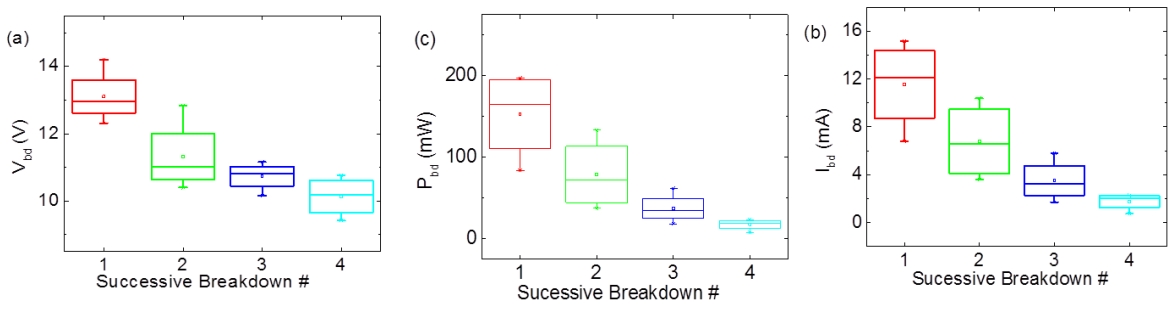

Figure 4-7 For high D aligned array, (a), (b) Breakdown voltage and breakdown current required at each successive breakdown. (c) Power required at each successive breakdown point

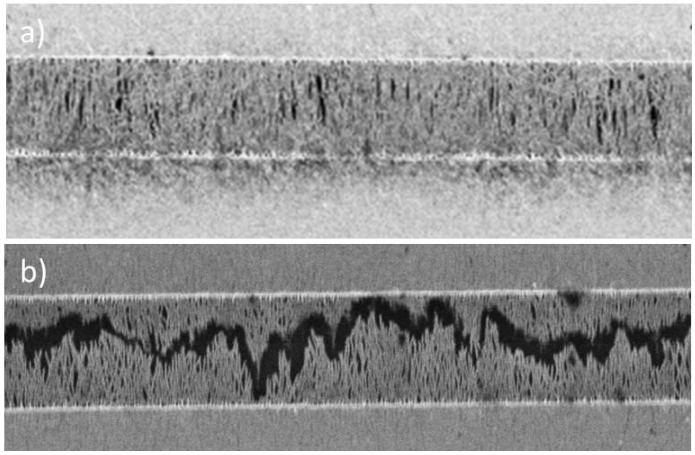

Figure 4-8 SEM image of a high density aligned array device with geometry L=2um & W=25um. a) shows image before electrical breakdown. b) shows the after complete breakdown. Scale bar shown in the figure is 2 um.

The representative result show in figure 4.6 are from a device with L = 2um and W =25um. In all of these experiments we have noticed that the Vbd decrease with successive electrical breakdown and in this particular representative device, Vbd decreases from 13V for the first breakdown to 10.3V for the 4th breakdown. This decrease in Vbd in each successive electrical breakdown in high D devices are in contrast with the previous result for low D aligned array. The V_{bd}, I_{bd} and P_{bd} values for all breakdown points have been shown in figure 4.7. A total of 5

devices were measure and analyzed. All of them showed the decrease in V_{bd} which is in contrast with the case of low D aligned array.

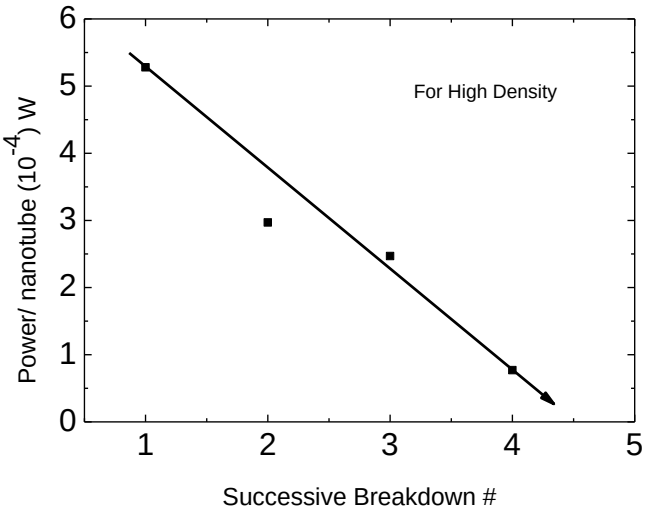

Figure 4-9 Breakdown power required per nanotube at successive breakdown in a high density aligned array

Figure 4.8 shows the SEM image of a high D (>10 CNT/um) aligned array carbon nanotube device before and after electrical breakdown. It is evident from the figure that breakdown in high D aligned array, breaking does not happen at random sites rather there is a correlation among the breaking sites [10]. In order to calculate the power required to break single nanotube in an aligned array, we extracted the values from IV curve shown in figure 4.6 and divide it by number of nanotubes in an aligned array. All of the 5 devices showed decrease in power/nanotube required for breaking. A plot of power required/nanotube vs. successive breakdown of a representative device is shown in figure 4.8. From the figure, it is evident that the power required per nanotube at first breakdown is 5.28×10^{-4} W whereas power/nanotube in breakdown #4 is 7.7×10^{-5} W which is an order of magnitude less than initial power requirement in the first breakdown. This decrease in power can be attributed to correlated breakdown which is an

intrinsic feature of sufficiently dense aligned array of carbon nanotubes. These correlations are caused by the dipole field produced by the broken nanotube at its end [10].

This dipole field is proportional to $1/r^3$, where r is inter tubes distance. In high density aligned array, this dipole field is very strong whereas in low density aligned array, as the inter tube distance is much larger, so this dipole field dies much faster and hence we didn't observe any correlation. Hence the reduction of power/nanotube required decreases.

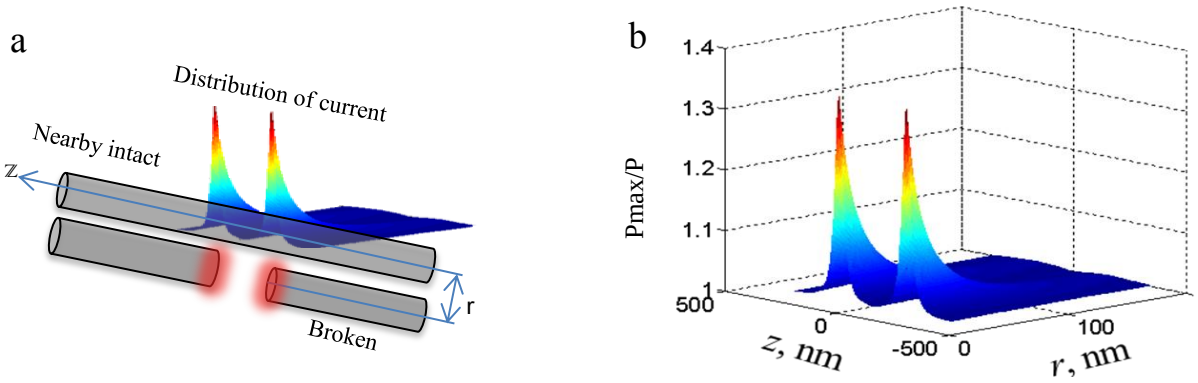

Figure 4-10 Ratio of maximum power of Joule heating due to current redistribution caused by broken nanotube to the power of Joule heating in absence of nearby broken nanotube. b) shows the schematic of current density distribution inside a nanotube sufficiently close to broken nanotube. [10].

CHAPTER 5: CONCLUSION AND FUTURE WORK SUGGESTIONS

5.1 Summary

In summary, I have investigated the electrical breakdown in aligned array of carbon nanotube with different D and different device geometries. These CNTs were assembled by the dielectrophorsis (DEP) method at room temperature and atmospheric pressure on pre-fabricated electrodes with the help of optical lithography followed by the electron beam lithography. Pd was chosen for the electrode material because CNTs are known to have good contact resistance with it hence it minimizes the contact resistance. In order to obtain the different CNT density per micron, I have changed the concentration of mother solution (from Brewer Science Inc.) and kept all other parameters (frequency applied, time of trapping, voltage applied) fixed. Throughout this study, I have varied the CNT density per micron along the channel length from low (~ 2 CNT/um) to high (> 10 CNT/um) and calculated the power required to break single nanotube in an aligned array in these two cases. I have found that power required breaking single nanotube in low density aligned array stays constant whereas in contrast to this, power required to break a single nanotube in and high density aligned array decreases with each successive breakdown. This reduction of breakdown power can be attributed to correlated breakdown in high density aligned array which is an intrinsic property of high density aligned array breakdown. This correlation happens due to change in the current density inside a intact carbon nanotube sufficiently close to a broken nanotube.

5.2 Future Suggestions

The work presented in this thesis can provide a platform in further understanding the electrical breakdown of carbon nanotubes in an aligned array. I have explored the intrinsic property of high D aligned array; a correlation among them in this thesis and calculated the power required per nanotube for electrical breakdown. The fundamental understanding about correlation is very important in order to utilize and exploit the aligned array properties in FET devices.

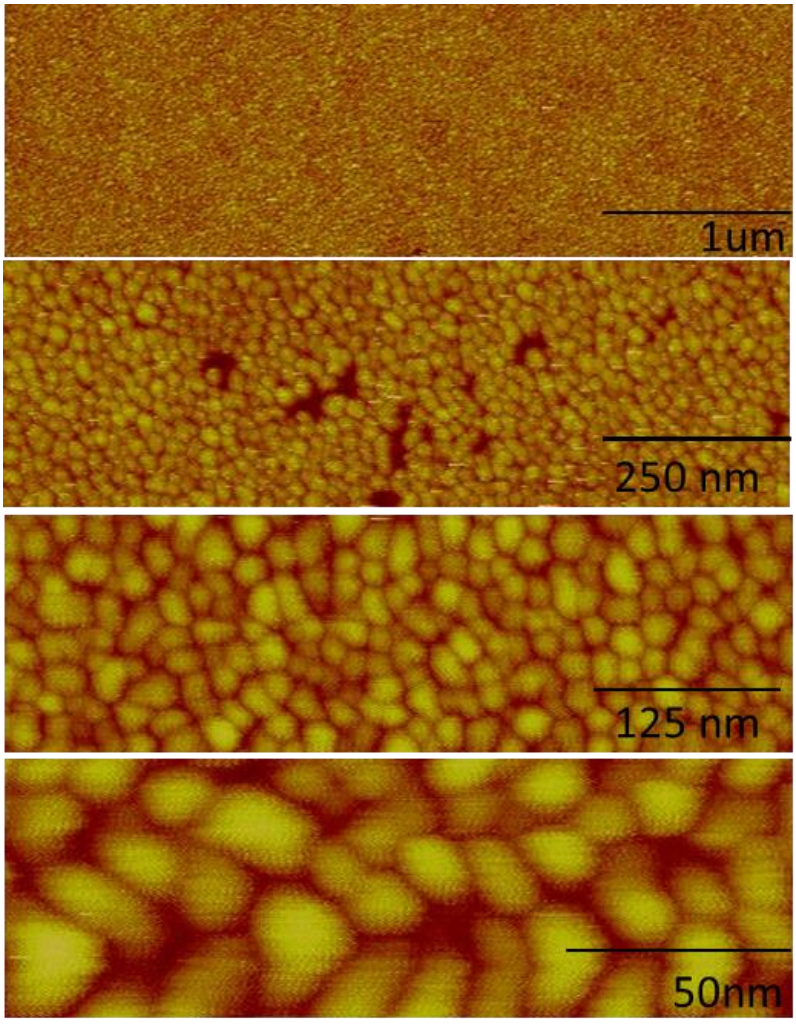

Figure 5-1 Deposition of Au nanoparticle on SiO2 substrate by thermal deposition.

One of the methods to study this correlation could be deposition the Au nanoparticle on it and do the electrical breakdown. Au nanoparticles are supposed to eliminate the dipole field and hence we expect to see no correlation. A preliminary work has been started in this direction where I have deposited 20 nm Au nanoparticle on the SiO_2 (as shown in figure 5.1), but this need to be further investigate in more details.

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