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High Current Density Low Voltage Isolated Dc-dc Converterswith Fast Transient Response

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HIGH CURRENT DENSITY LOW VOLTAGE ISOLATED DC-DC CONVERTERS WITH FAST TRANSIENT RESPONSE

by

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Major Professor: Issa Batarseh

ABSTRACT

With the rapid development of microprocessor and semiconductor technology, industry continues to update the requirements for power supplies. For telecommunication and computing system applications, power supplies require increasing current level while the supply voltage keeps decreasing. For example, the Intel's CPU core voltage decreased from 2 volt in 1999 to 1 volt in 2005 while the supply current increased from 20A in 1999 to up to 100A in 2005. As a result, low-voltage high-current high efficiency dc-dc converters with high power-density are demanded for state-of-the-art applications and also the future applications.

Half-bridge dc-dc converter with current-doubler rectification is regarded as a good topology that is suitable for high-current low-voltage applications. There are three control schemes for half-bridge dc-dc converters and in order to provide a valid unified analog model for optimal compensator design, the analog state-space modeling and small signal modeling are studied in the dissertation and unified state-space and analog small signal model are derived. In addition, the digital control gains a lot of attentions due to its flexibility and re-programmability. In this dissertation, a unified digital small signal model for half-bridge dc-dc converter with current doubler rectifier is also developed and the digital compensator based on the derived model is implemented and verified by the experiments with the TI DSP chip.

In addition, although current doubler rectifier is widely used in industry, the key issue is the current sharing between two inductors. The current imbalance is well studied and solved in non-isolated multi-phase buck converters, yet few discusse this issue in the current doubler rectification topology within academia and industry. This dissertation analyze the current

sharing issue in comparison with multi-phase buck and one modified current doubler rectifier topology is proposed to achieve passive current sharing. The performance is evaluated with half bridge dc-dc converter; good current sharing is achieved without additional circuitry.

Due to increasing demands for high-efficiency high-power-density low-voltage high current topologies for future applications, the thermal management is challenging. Since the secondary-side conduction loss dominates the overall power loss in low-voltage high-current isolated dc-dc converters, a novel current tripler rectification topology is proposed. Theoretical analysis, comparison and experimental results verify that the proposed rectification technique has good thermal management and well-distributed power dissipation, simplified magnetic design and low copper loss for inductors and transformer. That is due to the fact that the load current is better distributed in three inductors and the rms current in transformer windings is reduced.

Another challenge in telecommunication and computing applications is fast transient response of the converter to the increasing slew-rate of load current change. For instance, from Intel's roadmap, it can be observed that the current slew rate of the age regulator has dramatically increased from 25A/uS in 1999 to 400A/us in 2005. One of the solutions to achieve fast transient response is secondary-side control technique to eliminate the delay of optocoupler to increase the system bandwidth. Active-clamp half bridge dc-dc converter with secondary-side control is presented and one industry standard 16^{th} prototype is built and tested; good efficiency and transient response are shown in the experimental section. However, one key issue for implementation of secondary-side control is start-up. A new zero-voltage-switching buck-flyback isolated dc-dc converter with synchronous rectification is

proposed, and it is only suitable for start-up circuit for secondary-side controlled converter, but also for house-keeping power supplies and standalone power supplies requiring multi-outputs.

To my parents: Wengang Yao

Hongfu Li

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CHAPTER ONE: INTRODUCTION

1.1 DC-DC Switching Power Converter

Dc-dc converters are used in power electronics systems that convert system voltages from one dc level to another dc level.

Today dc-dc switching power converters are very popular and prevail in the power supply systems market. Prior to the 1970s, a majority of commercially available power supplies were the linear regulator type. Figure 1.1 shows a typical block diagram of a linear regulator power supply [1]. The front end of the linear regulator is a 60 Hz transformer, T_1, used to provide input electrical isolation and to step up or step down the line voltage, and this is followed by a full-wave bridge rectifier to convert the ac input to a dc input

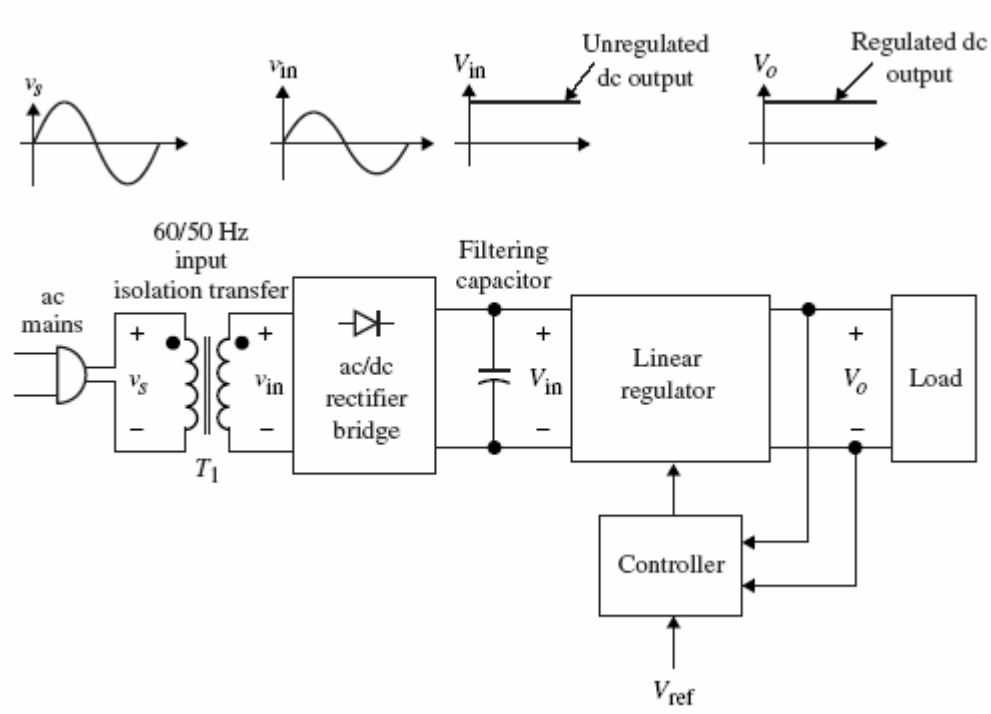


Figure 1.1 Typical block diagram of a linear regulator power supply [1]

by adding a large filtering capacitor at the input of the linear regulator. The input to the linear regulator, V_{in}, is unregulated dc and cannot be used to drive the load directly. Using a linear circuit that provides a stable dc output regulates the dc voltage at the output, V_o. The linear regulator is simple to use and provide tight control, good output voltage ripples and a low components count, but its main disadvantage for practical use is high power loss, hence, low power efficiency.

In the early 1970s, dc-dc switch mode converters entered the market. Because of high power efficiencies compared with linear regulators, traditional linear regulator power supplies gradually replaced for medium and high power applications. Unlike linear regulators, switching converters use power semiconductor devices to operate in either the on-state (saturation or conduction) or the off-state (cutoff or no conduction). Since either state will lead to low switching voltage or low switching current, it is possible to convert dc to dc with higher efficiency using a switching regulator. Figure 1.2 shows a simplified block diagram for a switched mode ac-to- dc power converter with multi-output application. Compared with the block diagram of Figure. 1.1, a switching network and high frequency output electrical isolation transformer T_2 are added.

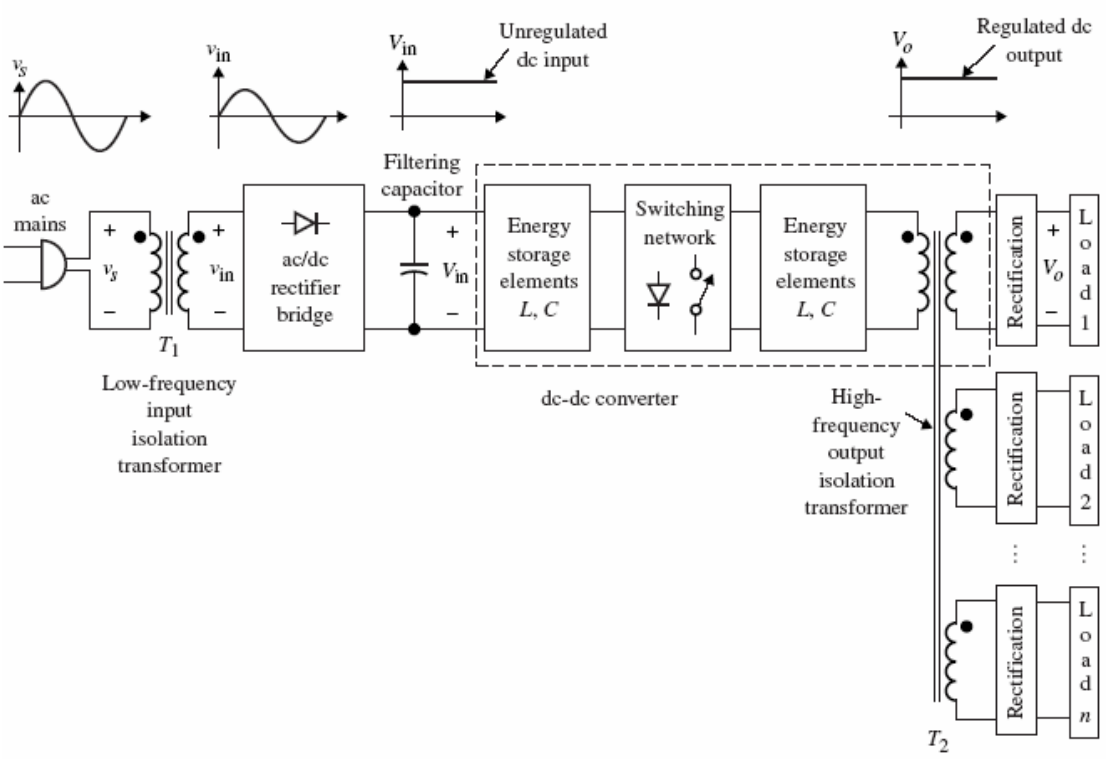


Figure 1.2 Block diagram of a switch mode power supply with multiple outputs [1]

The dc-dc switching converters can be classified as either non-isolated or isolated converter, depending on whether high frequency transformers are added between the power stage and output. The non-isolated converters have three basic topologies: buck, boost and buck-boost. There are also some other high order non-isolated topologies: CUK, SEPIC and ZETA.

The output voltage of non-isolated fixed frequency dc-dc converters is determined by the duty ratio D. For the application with high input voltage level and low output level, the converters must operate with very small duty cycles and asymmetrical transient responses. As a result, transformers are added in dc-dc switching converters and therefore becoming isolated dc-dc topologies.

The conventional isolated PWM dc-dc converter structure is shown in Figure 1.3, which consists of three parts: PWM converter, isolated transformer and rectifier. The PWM converter behaves as an inverter to generate ac voltage or current which is applied to the transformer primary winding. The transformer delivers ac voltage or current from the primary side to the secondary side and provides electrical isolation. With a transformer turns ratio, the converter may work at a desirable duty cycle and achieve good efficiency. ac voltages or currents are delivered to the transformer's secondary side, and through the rectifier, a dc voltage can be obtained from the output. Hence, the procedure in energy processing in a dc - dc converter is: dc→ac→transformer→ac→dc.

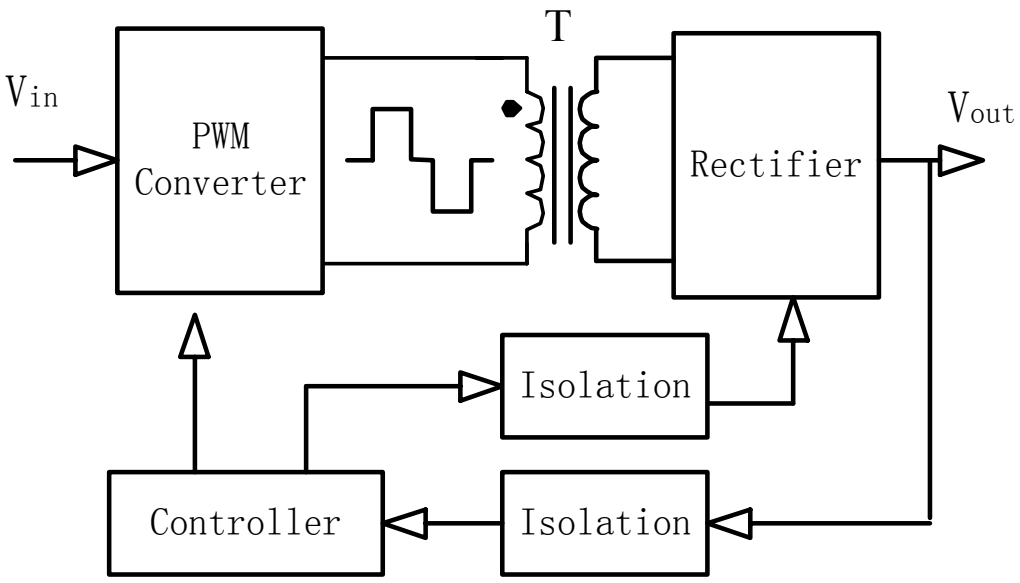
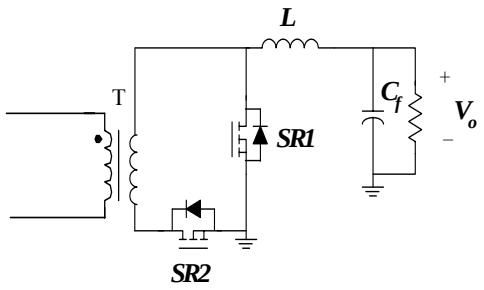


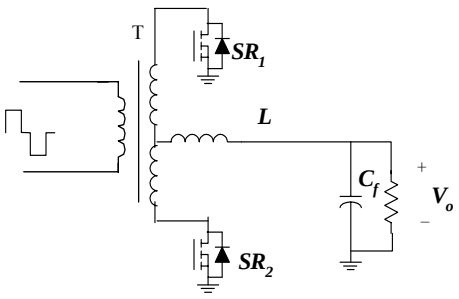
Figure 1.3 Block diagram of conventional PWM isolated dc-dc converters

PWM converters, like the one shown in Figure 1.3, can be realized in a variety of state-of-the-art topologies, such as forward, flyback, two-switch forward, push pull, half bridge,

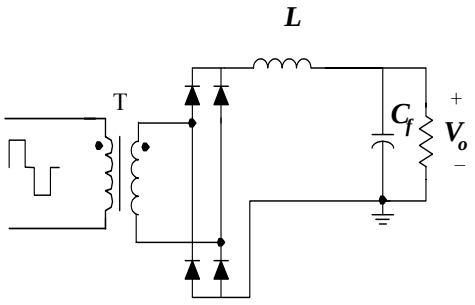
and full bridge. The rectifier topologies can be forward rectifier, center tapped, full bridge and current doubler rectifier as shown in Figure 1.4. Figure 1.5 shows the isolated dc-dc topologies.



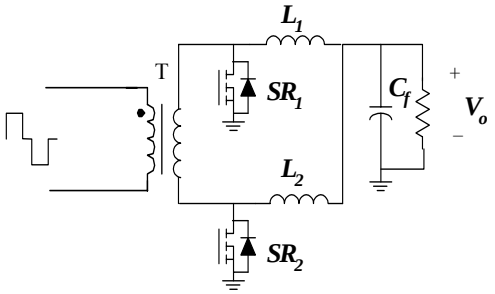
(a) Forward rectifier



(b) Center-tapped rectifier

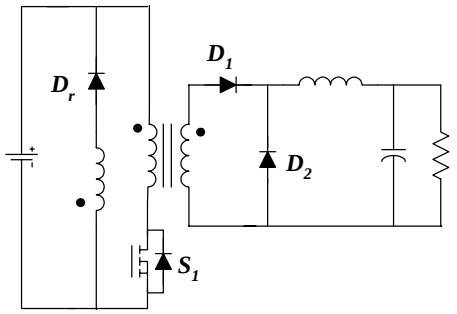


(c) Full-bridge rectifier

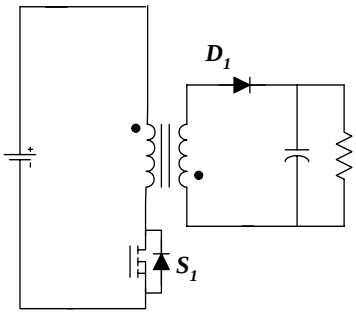


(d) Current-doubler rectifier

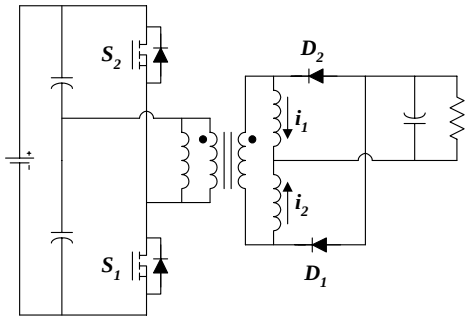
Figure 1.4 Various types of rectifier topologies



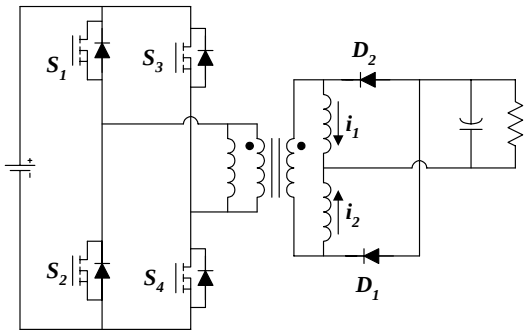
(a) Forward converter



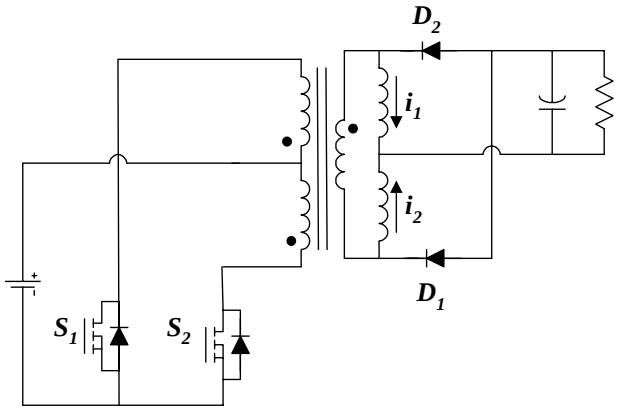
(b) Flyback converter



(c) Half bridge converter



(d) Full bridge converter



(e) Push pull converter

Figure 1.5 Examples of isolated dc-dc topologies

1.2 Low Voltage High Current DC-DC Converter

As the top largest consuming industries of dc-dc converters, telecom/datacom and computing systems have similar requirements for the power supplies: low voltage high current dc-dc conversion. Ever-higher level of integration offered by unprecedented advancement of semiconductor technology is enabling telecom and computing systems to incorporate more and more functions in increasingly smaller dimensions, which implies larger number of transistors on the silicon. As a result, the power level and current powering these ICs keep increasing. Since smaller-geometry processes drives the ICs' operating voltage to decrease and thus less power consumption due to the fact that the IC power consumption is proportional to the operating voltage, the output voltage of the power supplies in these applications continue to be lower. Another trend for the power requirements in these applications is fast transient response since the IC operation frequency is higher and higher. For example, based on the historical data of INTEL CPUs, Intel's CPU core voltage decreased from 2 volts in 1999 to 1 volt in 2005, while the supply current increased from 20A in 1999 to up to 100A in 2005, and the CPU power almost doubles around every 36 months till more than 100W today; the load current transient slew rate increased to 400A/us in 2005 from less than 50A/us in 1999.

The distributed power systems (DPS) is a popular and widely-used power solution in industry for telecom/datacom applications because it can generate high quality output voltage, and has improved reliability as well as easy thermal management[86-90]. The DPS basic architecture is shown in Figure 1.6 and the power conversion is achieved in multi-stage. The ac voltage from power grid is first converted and processed to high dc voltage through an offline ac-dc power supply and power factor correction circuit. Then an intermediate voltage bus is

generated from the high dc voltage by a bus dc-dc converter and the nominal bus voltage is typically 48V or 12V depending on different applications [58]. This DC bus supplies power to the load through different DC-DC converters, located on the same board where the supplied circuits are connected. These DC-DC converters are normally referred as on-board converters. The close proximity of the DC-DC regulator to the high slew-rate load reduces distribution impedances permitting more precise and easier to control regulation and faster transient response.

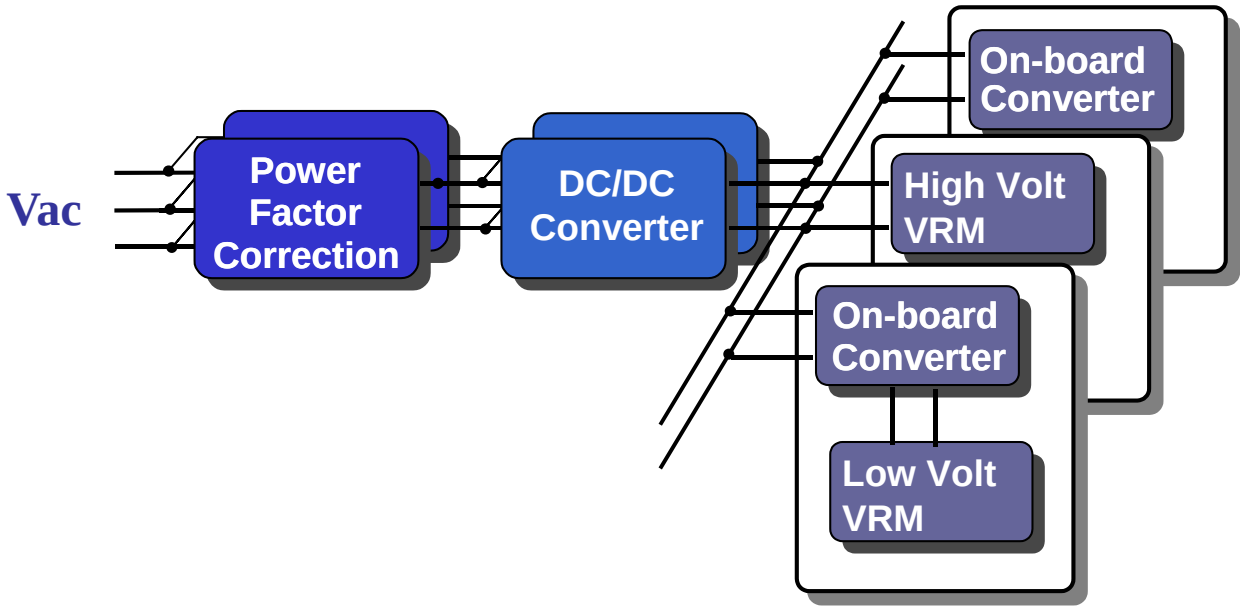


Figure 1.6 Basic architecture of a distributed power system [86]

High power-density is a continual demand for power supplies in telecom and computing systems since reduced parasitic elements in the control loop, lower voltage drop across the PCB power planes and a cost savings for distribution cables and connectors are obtained. Therefore, power converter size is a major challenge since the power level is ever-increasing as discussed above. One solution is high switching frequency operation since

the passive components' size is smaller as the switching frequency. However, power dissipation of the power converter may be higher in high frequency operation, so high efficiency topology and control techniques are always demanded for high frequency operation. However the size reduction and power density improvement of the power converter also depend on the thermal management which implies high frequency due to narrow pinch between the pc boards, otherwise bulky heat sink have to be added to the system and lower the converter power density correspondingly.

For the on-board converters, it can be non-isolated or isolated dc-dc converter depending on the applications. The dissertation focuses mainly on the high efficiency low-voltage high-current isolated dc-dc converter with fast transient response for telecom and computing systems. As shown in Figure 1.3, isolated dc-dc converter typically consists of three part, primary-side topology, secondary-side rectification topology and power transformer. Among the primary-side topologies, push-pull, half-bridge and full bridge are suited for low-voltage high-current applications. Considering lower component count and overall simplicity as well as an additional half step-down ratio due to the input capacitors, half-bridge is a preferred primary-side topology candidate for on board modules. In the traditional secondary-side rectifiers as shown in Figure 1.4, synchronous rectifiers are always used to replace the diode in the rectifier topologies for low voltage applications. The center-tapped rectifier and current doubler rectifier are commonly used in industry for low-voltage high-current application since in full-bridge rectifier, there are double voltage drop across the synchronous rectifiers (SRs) and SR driving is floating as well as the transformer utilization is bad; the half-wave rectifier has bad transformer utilization and current ripple frequency of output capacitor is switching frequency.

Compared to full-bridge and half-wave rectifier, both center-tapped and current doubler rectfiers have better transformer utilization and the twice current ripple frequency on the output capacitors which has potential for cost reduction and power-density improvement. However, center-tapped is better than current doubler in terms of single inductor structure while current doubler is better in lower conduction loss, simple inductor and transformer design.

1.3 Compensation for DC-DC Converter

The objective of dc-dc converters is to deliver a stable and regulated dc output voltage from an unregulated dc input voltage. The pulse width modulation (PWM) regulation method is used in switching converters, which controls the on time of the power switch devices to regulate the dc output voltage.

Based on the implementation of the PWM control method and compensator, the controller can be classified as either an analog controller or a digital controller.

Power control schemes have been revolutionized over the past few decades. Compared with analog controllers, the digital controller is gaining more attention because of its stable performance, flexibility, and ability to handle more complicated control techniques.

The advent of programmable digital signal processors (DSP) is creating thriving opportunities in the field of power electronics. The special architecture and high performance of DSP make it possible to implement a wide variety of control and measurement algorithms at a high sampling rate and reasonable cost. Power electronics systems are typically a complex combination of linear, nonlinear and switching elements. High-frequency converters add another dimension of complexity because of their fast dynamics.

Modern power electronics systems, therefore, demand the use of high-speed data-acquisition and real-time control. High performance DSP could meet these processing requirements imposed by such systems.

1.3.1 Analog Controller for DC-DC Converter

A typical switching power converter is shown above in Figure. 1.7 [2]. An analog control system provides output voltage regulation by comparing a scaled representation of the output voltage to a reference voltage and amplifying the difference. The "error voltage", applied to an analog Pulse Width Modulator, results in a variable width driving pulse that has an average value equal to the desired output voltage. After power amplification by the power stage, driving pulses are averaged by the filter to yield a dc output voltage.

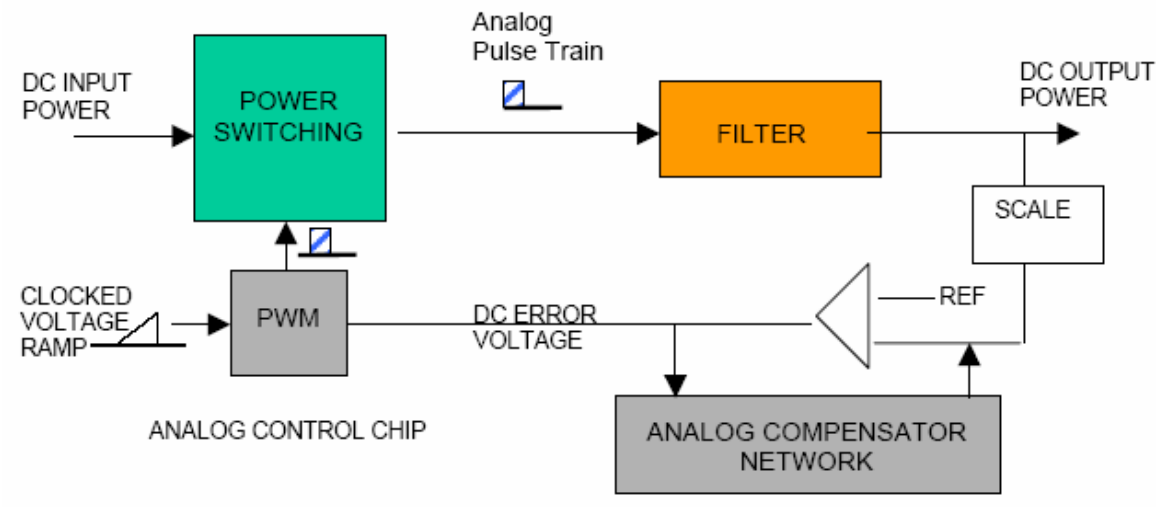


Figure 1.7 Typical switching power converter architecture with analog controller [2]

As a closed loop system, this circuit requires a control mechanism to ensure that the

gain around the loop (from output sensing back to the filter) does not exceed unity at any frequency where phase shift around the loop reaches 360 degrees. In addition to the built-in 180 degrees phase shift necessary for regulation, the phase shift around the control loop is also caused by delays introduced by reactive elements (capacitors or inductors) and to a smaller degree by operational delays in amplifiers, modulators and switching devices.

Adjustments, or compensations, for gain variation and phase shift over a range of frequencies is usually incorporated into error amplifier circuitry to assure that the circuit will be stable when operating under anticipated conditions.

Isolation between input and output may be included in the design, but even with isolation, conceptually. Most power converters operate as shown in Figure 1.7.

It is possible to incorporate digital devices, such as “micro-controllers”, into an analog control system like that of Figure. 1.7. A microprocessor control unit (MCU) can be set up to adjust and manage operation of an analog PWM (change switching frequency, for example) but that sort of control is still classified as an analog controlled dc-dc switching converter. Digital controlled switching converters are classified as a control system in which the feedback process is managed entirely by digital techniques. Specifically, the PWM functions, error signals, and compensator functions are performed in digital mode.

1.3.2 Digital Controller for DC-DC Converter

A digital control system, equivalent to that shown in Figure. 1.7, is depicted in Figure. 1.8 [2]. Notice that voltage sensing, compensator and pulse width modulator functions are still present but appear under different names. Power switching, scaling, and filtering functions are

exactly the same as in the analog design shown in Figure. 1.7.

Working back from the power switching stage, the Digital Pulse Width Modulator (DPWM) performs the same drive signal generation function as its analog counterpart. However, it does so by "calculating" and then "timing" the desired duration of ON and OFF periods of its output signal. In contrast, the analog PWM usually operates by triggering ON at a clock transition and triggering OFF when a fixed voltage "ramp" reaches a pre-set trip voltage. The distinction is important because it leads to many of the advantages and challenges associated with digital control.

Located before the DPWM, is a "control law" processor. Typically a PI or PID style subsystem is used to perform the task of translating a digital representation of output voltage into pulse duration (duty-cycle) information used by the DPWM. It is the job of the PID control element to center the output voltage on a pre-set value and adjust the pulse width, in real-time, to provide voltage regulation. It must do so by compensating for gain and phase-shift factors around the control loop, as seen in the analog version. In digital systems, there are additional phase shift factors arising from time delays in processing the control data stream. The major gain and phase-shift factors present in an analog system (mostly from the output filter), are also present in digital mode, with calculation and A/D conversion delay factors added.

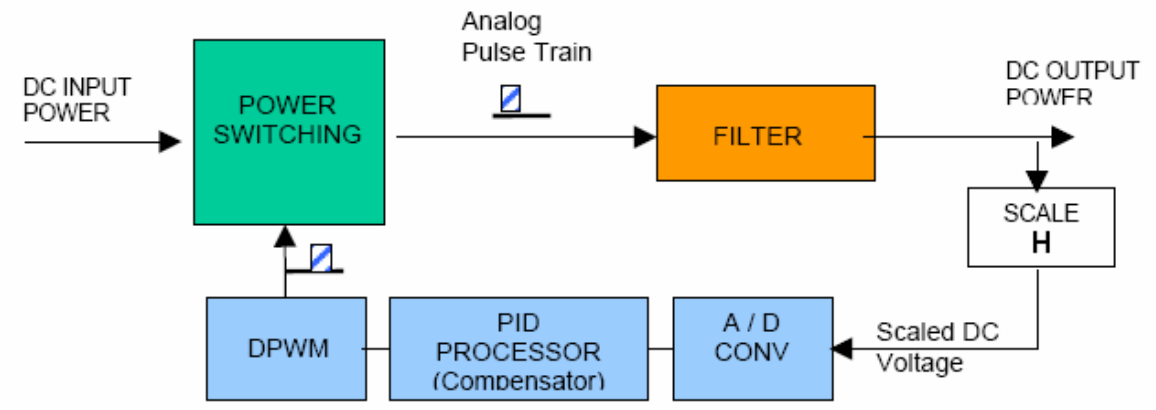


Figure 1.8 Typical switching power converter architecture with digital controller [2]

Moving farther upstream, an Analog-to-Digital (A/D) converter produces digital data that represents output voltage. Each binary "word" containing upwards of 8 bits of data, is sent at a high clock rate to the PID control law processor. Word length and A/D reference voltages set the precision at which the output voltage can be maintained. In digital systems, analog quantities such as voltage must be represented as a range of discrete values. Spacing between values, or the size of each "bucket" is set by the number of data bits divided into the total range of voltage over which the A/D conversion stage operates.

The digitally controlled switching power converters have the following advantages over traditional analog controlled converters [2-11]:

- Generate flexible power switch drive waveforms with programmable relationships to one another
- Implement sophisticated control laws
- Potential space saving and less component counts
- Offer precision that can counter the effects of component tolerance, parametric drift, aging, etc.

- Adapt to changing environmental conditions
- Store data for operational purposes and/or record keeping
- Communicate with the external digital world.

However, the digital controllers have their own disadvantages: high resolution is a must to satisfy the converters' tight regulation requirements and high speed is also a must in order to satisfy the converter dynamic requirements [7-8] [11]. These two requirements result in cost increase.

Generally, there are several implementation approaches for digital controllers today, which include Microprocessor/DSP's (Digital Signal Processors), FPGA (Field Programmed Gates Array) and Custom IC. The features of these approaches are compared as follows:

DSP:

• DSP chips can be reprogrammed;

• The speed is generally slower than ICs;

• Implementation is exceedingly complex for the intended application;

• DSP is costly over custom IC design;

• High frequency power converters have to use high performance DSP.

FPGA:

• FPGA can be programmed on site;

• The processing is faster than a general purpose DSP;

• For FPGA design there is no physical manufacturing step, which results in a very short design time;

• FPGA's typical price is higher than DSP.

Custom IC Design:

• Due to physical design consideration, custom IC's typically have better performance than FPGA;

• However it results in much longer design time than FPGA since there is a layout step;

• Custom IC design has lower price than FPGA and DSP.

1.4 Dissertation Outline

The dissertation consists of seven chapters.

Chapter One briefly discusses the research background and motivation of this work. After introduction of the history of switch-mode dc-dc converters, the dc-dc switching converters are categorized as non-isolated and isolated converters. In telecom and computing systems, low voltage high current dc-dc converters are needed. Major trend and challenges are discussed for low-voltage high current dc-dc conversion and typical architecture distributed power systems is shown. In this chapter, traditional analog control and digital control are also discussed and compared, and different implementations of digital control are presented as well.

Chapter Two focuses on the modeling and digital control of half-bridge dc-dc converters with current doubler rectification. Since half-bridge current-doubler dc-dc converter is widely used in industry and is a good topology suitable for high-current low-voltage applications, There're three control schemes for half-bridge dc-dc converters and in order to provide a valid unified analog model for optimal compensator design, unified analog and

digital state-space and analog small signal model are derived respectively. A digital compensator is designed for half bridge dc-dc converter with current doubler rectifier and implemented by TI DSP chip.

In Chapter Three, the current sharing in current doubler rectifier is discussed and compared with multi-phase non-isolated buck converter. Although duty cycle adjustment is widely used in current balancing for multi-phase buck converter, the analytic and experimental results show that this method can not effectively adjust the current distribution in the current doubler rectifier. Then a modified current doubler rectification topology is proposed to achieve passive current sharing without additional circuitry as duty cycle adjustment method.

Current tripler and current N-tupler rectification topologies are proposed in Chapter Four for future high current applications in telecom and computing systems. The proposed rectification technique features good thermal management and well-distributed power dissipation, simplified magnetic design and low copper loss for inductors and transformer due to the fact that the load current is better distributed in three inductors and the rms current in transformer windings is reduced. The operation principle and dc analysis are presented and the proposed rectification topology is compared with state-of-the-art rectification topologies.

Chapter Five discusses another major challenge in telecommunication and computing applications, which is the fast transient response of the converter to the increasing slew-rate of load current change. In isolated dc-dc converters, primary-side control is widely used in industry and low-speed optocoupler is commonly used for feedback signal. But typically optocoupler only has 10 to 30 KHz bandwidth and therefore limits the low close-loop bandwidth for the system resulting in slow transient response. Secondary-side control

technique can eliminate the delay of optocoupler to increase the system bandwidth and achieve fast transient response. Active-clamp half bridge dc-dc converter with secondary-side control is presented and one industry standard 16^{th} prototype is built and tested; good efficiency and transient response are achieved.

In Chapter Six, a novel hybrid zero-voltage-switching buck-flyback isolated dc-dc converter with synchronous rectification is proposed for multi-output applications. It can be used not only as house-keeping power supplies and standalone power supplies requiring multi-outputs, but also provide solution for start-up issue for secondary-side controlled converter. The operation modes are analyzed quantitatively and dc analysis is discussed, and the design guideline is also provided.

Chapter Seven summaries the work and presents some future work.

CHAPTER TWO: HALF BRIDGE DC-DC CONVERTER WITH CURRENT DOUBLER RECTIFIER

To further increase the processing speed and decrease the power consumption in VLSI (Very Large Scale Integration) circuits, the operating voltages of ICs keep decreasing with operation current increasing. Therefore the study of an isolated dc-dc topology suitable for low voltage high current applications is a must.

Among the four conventional rectification topologies shown in Figure 1.5, current doubler rectifier (CDR) can minimize transformer secondary-side winding *rms* current and has good transformer utilization. Since only half of the load current flows through each output inductor, the thermal management and inductor magnetic design for the current doubler rectifier is easier than the other three counterparts. Moreover, the current doubler rectifier can step down more voltage than full-bridge and center-tapped rectifiers. In addition, CDR minimizes the number of high current interconnections that simplify secondary side layout and further reduce layout-related losses. Therefore, current doubler rectification is very suitable for low voltage high current applications [12-13].

For the half bridge (HB) topology, the voltage rating of switching devices is half of that required by push-pull and forward converters. Besides, HB has good transformer utilization, and the leakage inductance energy can be recycled to the input capacitors. Due to the input bridge capacitors, HB has an additional 1/2 voltage step-down ratio as compared with forward, flyback, push-pull and full bridge topologies, from the line voltage to the transformer primary-side. For the primary-side topology of isolated dc- dc converters, half-bridge is a good candidate for low-voltage applications. Since current doubler rectifier can be used with half

bridge topology, the half bridge dc-dc converter with current doubler rectifier is a suitable isolated dc-dc switching converter topology for high current low voltage applications [14].

So far there are three control methods for half bridge dc-dc converter with current doubler rectifier: symmetrical control, asymmetrical (complementary) control and duty cycle shifted (DCS) control schemes [16], [33-35]. They all have their own advantages and disadvantages. When the conventional symmetric control is used for the half-bridge converter, its two switches operate at hard-switching with symmetric components stresses. When the asymmetric (complimentary) control is used, the two half-bridge switches operate at soft-switching, but unfortunately causing asymmetric stresses on the converter components which is not desirable especially for wide input voltage range. Moreover, the dc gain is not linear which degrades the converter performance. A recently proposed half-bridge control scheme, the DCS control, results in achieving soft-switching for one of the two half-bridge switches while maintaining symmetric duty cycle and hence symmetric components stresses.

To analyze and design a regulated current doubler rectified half bridge (CDRHB) dc-dc converter, modeling is a must. For optimal analog compensator design, small signal modeling is always necessary. However, few literatures discussed the unified modeling of half-bridge dc-dc converter with current doubler rectifier, which is applicable for all three control methods aforementioned. In addition, recently digital control becomes a hot topic in the power electronics area due to the ease of re-programmability and integration and implementation of nonlinear control laws. Similar to the analog control, a valid digital small signal model is needed for optimal design of digital compensator. However, no literature has derived and discussed the digital small signal model for digitally regulated CDRHB.

In this chapter, the operation and control schemes of half bridge topology with current doubler rectifier is discussed. Then unified state-space model of CDRHB is derived valid for symmetric, asymmetric and DCS control. Based on state-space model, both unified analog and digital small signal models for HB dc-dc converter with CDR are developed respectively.

2.1 Topology and Operation

Figure 2.1 shows the half bridge dc-dc converter topology with current doubler rectifier.

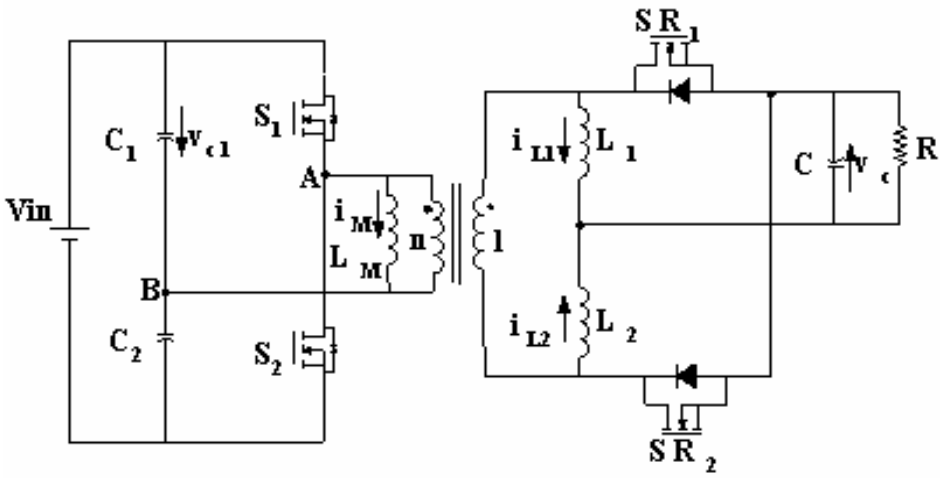
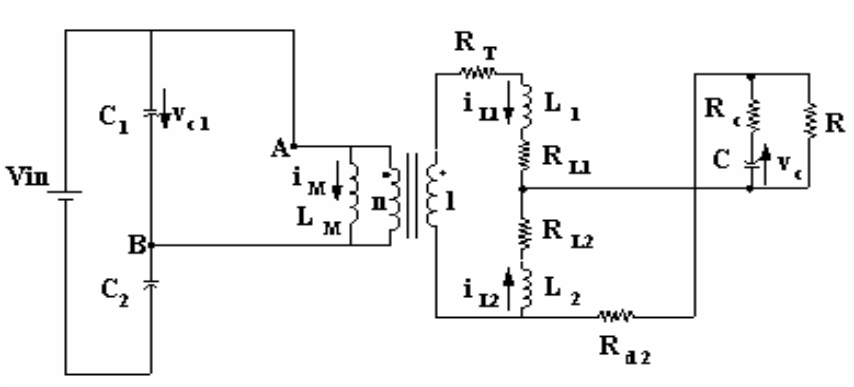


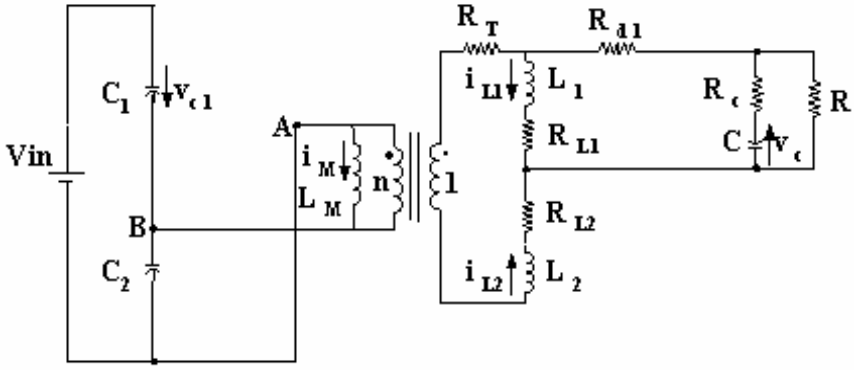
Figure 2.1 Half bridge dc-dc converters with current doubler rectifier

No matter which control scheme is applied, there are three typical operation modes shown in Figure 2.2, supposing the converter operates in continuous conduction mode (CCM)

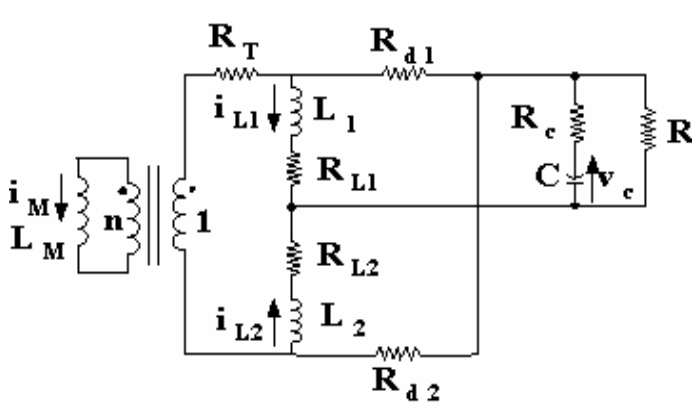
and neglecting transformer leakage energy and transient commutation [15]. In Figure 2.2, R_T is the equivalent resistance of the reflected switches on-resistance and DCR of the transformer windings, R_{L_1} and R_{L_2} are equivalent DCR's of inductor L_1 and L_2, respectively, and R_c is the ESR (Equivalent Series Resistance) of the output capacitor



(a) Mode 1: S_1 is on, S_2 is off



(b) Mode 2: S_2 is on, S_1 is off



(c) Mode 3: Both S_1 and S_2 are off

Figure 2.2 Operation modes

2.2 Unified State Space Model for HB Converter with Current Doubler Rectifier

State space equations can be derived according to three different operation modes shown in Figure 2.2 in terms of $\dot{x} = A_m \cdot x + B_m \cdot u$ and $y = C_m \cdot x$, where m denotes the corresponding operation mode. The state variable x is chosen as $x = \begin{bmatrix} v_{c_1} & i_1 & i_2 & v_c & i_M \end{bmatrix}^T$, input $u = V_{in}$, $\dot{x} = \begin{bmatrix} \frac{dv_{c_1}}{dt} & \frac{di_1}{dt} & \frac{di_2}{dt} & \frac{dv_c}{dt} & \frac{di_M}{dt} \end{bmatrix}^T$ and output is the voltage across the load R.

During the on time of switch S_1, A_1 and B_1 are as shown in (2-1):

$$A_1=\begin{bmatrix} 0 & -\frac{1}{n\cdot(C_1+C_2)} & 0 & 0 & -\frac{1}{C_1+C_2} \\ \frac{1}{n\cdot L_1} & -\frac{R_T+R_{L_1}+R_{d_2}+\frac{R\cdot R_c}{R+R_c}}{L_1} & -\frac{R_{d_2}+\frac{R\cdot R_c}{R+R_c}}{L_1} & -\frac{R}{L_1\cdot(R+R_c)} & 0 \\ 0 & -\frac{R_{d_2}+\frac{R\cdot R_c}{R+R_c}}{L_2} & -\frac{R_{L_2}+R_{d_2}+\frac{R\cdot R_c}{R+R_c}}{L_2} & -\frac{R}{L_2\cdot(R+R_c)} & 0 \\ 0 & \frac{R}{C\cdot(R+R_c)} & \frac{R}{C\cdot(R+R_c)} & -\frac{1}{C\cdot(R+R_c)} & 0 \\ \frac{1}{L_M} & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$B_1=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix},\quad C_1=\begin{bmatrix} 0 & \frac{R_c\cdot R}{R+R_c} & \frac{R_c\cdot R}{R+R_c} & \frac{R}{R+R_c} & 0 \end{bmatrix} \tag{2-1}$$

During the on time of switch S_2, A_2 and B_2 are as shown in (2-2):

$$A_2=\begin{bmatrix} 0 & 0 & \frac{1}{n\cdot(C_1+C_2)} & 0 & -\frac{1}{C_1+C_2} \\ 0 & -\frac{R_{L_1}+R_{d_1}+\frac{R\cdot R_c}{R+R_c}}{L_1} & -\frac{R_{d_1}+\frac{R\cdot R_c}{R+R_c}}{L_1} & -\frac{R}{L_1\cdot(R+R_c)} & 0 \\ -\frac{1}{n\cdot L_2} & -\frac{R_{d_1}+\frac{R\cdot R_c}{R+R_c}}{L_2} & -\frac{R_T+R_{L_2}+R_{d_1}+\frac{R\cdot R_c}{R+R_c}}{L_2} & -\frac{R}{L_2\cdot(R+R_c)} & 0 \\ 0 & \frac{R}{C\cdot(R+R_c)} & \frac{R}{C\cdot(R+R_c)} & -\frac{1}{C\cdot(R+R_c)} & 0 \\ \frac{1}{L_M} & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$B_2=\begin{bmatrix} 0 \\ 0 \\ \frac{1}{n\cdot L_2} \\ 0 \\ -\frac{1}{L_M} \end{bmatrix},\qquad C_2=\begin{bmatrix} 0 & \frac{R_c\cdot R}{R+R_c} & \frac{R_c\cdot R}{R+R_c} & \frac{R}{R+R_c} & 0 \end{bmatrix} \tag{2-2}$$

During the off time of both S_1 and S_2, (2-3) shows the corresponding A_3 and B_3 :

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\dfrac{R_{L_1} + R_{d_1} + \dfrac{R \cdot R_c}{R + R_c}}{L_1} & -\dfrac{R \cdot R_c}{L_1 \cdot (R + R_c)} & -\dfrac{R}{L_1 \cdot (R + R_c)} & -\dfrac{n \cdot R_{d_1}}{L_1} \\ 0 & -\dfrac{R \cdot R_c}{L_2 \cdot (R + R_c)} & -\dfrac{R_{L_2} + R_{d_2} + \dfrac{R \cdot R_c}{R + R_c}}{L_2} & -\dfrac{R}{L_2 \cdot (R + R_c)} & -\dfrac{n \cdot R_{d_2}}{L_2} \\ 0 & \dfrac{R}{C \cdot (R + R_c)} & \dfrac{R}{C \cdot (R + R_c)} & -\dfrac{1}{C \cdot (R + R_c)} & 0 \\ 0 & -\dfrac{n \cdot R_{d_1}}{L_M} & \dfrac{n \cdot R_{d_2}}{L_M} & 0 & -\dfrac{n^2 \cdot (R_T + R_{d_2} + R_{d_1})}{L_M} \end{bmatrix}$$

$$B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C_3 = \begin{bmatrix} 0 & \dfrac{R_c \cdot R}{R + R_c} & \dfrac{R_c \cdot R}{R + R_c} & \dfrac{R}{R + R_c} & 0 \end{bmatrix} \tag{2-3}$$

In order to obtain a unified state space averaged model [33], let the switching cycle be T , the on time of switch S_1 and S_2 are $d_1 \cdot T$ and $d_2 \cdot T$, respectively. Then the unified state space averaged model for half bridge current doubler converter can be derived as follows:

$$\dot{x} = A \cdot x + B \cdot u = f(x,\ u,\ d_1,\ d_2)$$

$$y = C \cdot x \tag{2-4}$$

where, $A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3$ (2-5)

$$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3 \tag{2-6}$$

and $C = \begin{bmatrix} 0 & \dfrac{R_c \cdot R}{R + R_c} & \dfrac{R_c \cdot R}{R + R_c} & \dfrac{R}{R + R_c} & 0 \end{bmatrix}$ (2-7)

2.3 Unified Analog Small Signal Model for HB Current Doubler Converter

Based on the unified state space averaged model derived in section 2.2, the analog small signal model is further developed in this section. In general, let $x = X_{ss} + \hat{x}$, $y = Y_{ss} + \hat{y}$, $u = V_{in} + \hat{v}_{in}$, $d_1 = D_1 + \hat{d}_1$, and $d_2 = D_2 + \hat{d}_2$, where X_{ss}, Y_{ss}, V_{in}, D_1 and D_2 are the steady state values of x, y, v_{in}, d_1 *and* d_2 respectively, and $\hat{x}$, $\hat{y}$, $\hat{v}_{in}$, $\hat{d}_1$ *and* $\hat{d}_2$ represent the small signal disturbances. In the steady state, $\dot{x} = A \cdot X_{ss} + B \cdot V_{in} = 0$, then the following can be determined:

$$X_{ss} = -A_{ss}^{-1} \cdot B_{ss} \cdot V_{in} \tag{2-8}$$

From (2-4), (2-9) can be derived as follows:

$$\frac{\partial \hat{x}}{\partial t} \approx \frac{\partial f}{\partial x} \cdot \hat{x} + \frac{\partial f}{\partial v_{in}} \cdot \hat{v}_{in} + \frac{\partial f}{\partial d_1} \cdot \hat{d}_1 + \frac{\partial f}{\partial d_2} \cdot \hat{d}_2 \tag{2-9}$$

Based on (2-4) and (2-8) ~ (2-9), we can conduct unified small signal analysis for CDRHB converters.

Table 2-1
Transfer functions for analog controlled half bridge current doubler converters with different control schemes

Control Scheme	**Duty Cycle**	$G_{vg}(s) = \frac{\hat{v}_o}{\hat{v}_{in}}$	$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}}$
Symmetric	$D_1 = D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (s \cdot I - A_{ss})^{-1}[(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}]$
Asymmetric	$D_1 = 1 - D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (s \cdot I - A_{ss})^{-1}[(A_1 - A_2) \cdot X_{ss} + (B_1 - B_2) \cdot V_{in}]$
Duty Cycle Shift	$D_1 = D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (s \cdot I - A_{ss})^{-1}[(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}]$

2.4 Unified Digital Small Signal Model for HB Current Doubler Converter

For developing the linear time invariant (LTI) digital model of the half bridge dc-dc converter with current doubler rectification in Figure 2.1, the following assumptions should be made:

- The converter operates in CCM;
- V_{in} is constant within each switching cycle;
- There is no ripple in the inductors currents and output capacitor voltage.

For simplicity, the digital model of the symmetric half bridge converter with current doubler rectifier will be derived first.

Assuming that the derivation starts from the k^{th} switching cycle, using the Forward

Euler approximation method as follows:

$$x(t_0 + \varepsilon) \approx x(t) + \varepsilon \frac{dx(t_0)}{dt} \tag{2-10}$$

When $kT < t \le kT + d_1 T$, converter operates in mode 1 (switch S_1 is on), according to Forward Euler approximation, we can get

$$x(kT + d_1 T) \approx x(kT) + d_1 T \cdot (A_1 \cdot x(kT) + B_1 \cdot V_{in}[k]) \tag{2-11}$$

After reformatting (2-11),

$$x(kT + d_1 T) \approx [I + d_1 T \cdot A_1] x(kT) + d_1 T \cdot B_1 \cdot V_{in}[k] \tag{2-12}$$

When $kT + d_1 T < t \le kT + d_1 T + \frac{1 - d_1 - d_2}{2} T$, the converter operates in mode 3 (both S_1 and S_2 is off), so after Forward Euler approximation:

$$\begin{aligned} x(kT + d_1 T + \frac{1 - d_1 - d_2}{2} T) \approx x(kT + d_1 T) + \frac{1 - d_1 - d_2}{2} T \cdot (A_3 \cdot x(kT + d_1 T) \\ + B_3 \cdot V_{in}[k]) \end{aligned} \tag{2-13}$$

After reformatting (2-13), the following is obtained:

$$\begin{aligned} x(kT + d_1 T + \frac{1 - d_1 - d_2}{2} T) \approx [I + \frac{1 - d_1 - d_2}{2} T \cdot A_3] x(kT + d_1 T) \\ + \frac{1 - d_1 - d_2}{2} T \cdot B_3 \cdot V_{in}[k] \end{aligned} \tag{2-14}$$

When $kT + d_1 T + \frac{1 - d_1 - d_2}{2} T < t \le kT + d_1 T + \frac{1 - d_1 - d_2}{2} T + d_2 T$, converter operates in mode 2 (S_2 is on),

$$x(kT+(d_1+d_2)T+\frac{1-d_1-d_2}{2}T)\approx x(kT+d_1T+\frac{1-d_1-d_2}{2}T)+d_2T\cdot (A_2\cdot x(kT+d_1T+\frac{1-d_1-d_2}{2}T)+B_2\cdot V_{in}[k]) \quad (2\text{-}15)$$

After reformatting (2-15),

$$x(kT+(d_1+d_2)T+\frac{1-d_1-d_2}{2}T)\approx [I+d_2T\cdot A_2]x(kT+d_1T+\frac{1-d_1-d_2}{2}T)+d_2T\cdot B_2\cdot V_{in}[k] \quad (2\text{-}16)$$

When $kT+d_1T+\frac{1-d_1-d_2}{2}T+d_2T<t\le kT+T$, converter operates in mode 3 (both S_1 and S_2 is off), so:

$$x(kT+T)\approx x(kT+(d_1+d_2)T+\frac{1-d_1-d_2}{2}T)+\frac{1-d_1-d_2}{2}T\cdot (A_3\cdot x(kT+(d_1+d_2)T+\frac{1-d_1-d_2}{2}T)+B_3\cdot V_{in}[k]) \quad (2\text{-}17)$$

After reformatting, (2-18) can be written as follows:

$$x(kT+T)\approx [I+\frac{1-d_1-d_2}{2}T\cdot A_3]x(kT+(d_1+d_2)T+\frac{1-d_1-d_2}{2}T)+\frac{1-d_1-d_2}{2}T\cdot B_3\cdot V_{in}[k] \quad (2\text{-}18)$$

Then substitute (2-12), (2-14) and (2-16) to (2-18) and neglect the terms including $T^N(N\ge 2)$, a state space digital model is developed as follows:

$$x[k+1]=[I+A\cdot T]x[k]+B\cdot T\cdot V_{in}[k]=\phi(x[k],v_{in}[k],d_1,d_2) \quad (2\text{-}19)$$

In order to derive the LTI digital model, linearization of the digital model (2-19) at the steady state operation point is taken to obtain:

$$\hat{x}[k+1] \approx \frac{\partial \phi}{\partial x}\hat{x}[k] + \frac{\partial \phi}{\partial v_{in}}\hat{v}_{in}[k] + \frac{\partial \phi}{\partial d_1}\hat{d}_1 + \frac{\partial \phi}{\partial d_2}\hat{d}_2$$

$$\hat{y}[k] = C \cdot \hat{x}[k] \tag{2-20}$$

And in steady state, $x[k+1] = x[k] = X_{ss}$, from (2-19), it can be derived as follows:

$$X_{ss} = -A_{ss}^{-1} \cdot B_{ss} \cdot V_{in} \tag{2-21}$$

The deviations in (2-22) can also be derived from (2-19) to obtain the LTI digital model:

$$\begin{aligned}\hat{x}[k+1] \approx{}& (I + A_{ss} \cdot T)\hat{x}[k] + B_{ss} \cdot T \cdot \hat{v}_{in}[k] \\ &+ [(A_1 - A_3)X_{ss} + (B_1 - B_3)V_{in}] \cdot T \cdot \hat{d}_1 \\ &+ [(A_2 - A_3)X_{ss} + (B_2 - B_3)V_{in}] \cdot T \cdot \hat{d}_2\end{aligned}$$

$$\hat{y}[k] = C \cdot \hat{x}[k] \tag{2-22}$$

Although the above derivations are based on the symmetric controlled half bridge current doubler dc-dc converter, the linearized digital model (2-20) is unified, and only different in derivatives in (2-20) according to the different control schemes.

Different transfer functions can also be derived based on different control schemes from the LTI digital model in (2-22), and they are listed in table 2-2.

Table 2-2
Transfer functions for digital controlled half bridge current doubler converters with different control schemes

Control Scheme	**Duty Cycle**	$G_{vg}(z) = \frac{\hat{v}_o}{\hat{v}_{in}}$	$G_{vd}(z) = \frac{\hat{v}_o}{\hat{d}}$
Symmetric	$D_1 = D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}]$
Asymmetric	$D_1 = 1 - D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 - A_2) \cdot X_{ss} + (B_1 - B_2) \cdot V_{in}]$
Duty Cycle Shift	$D_1 = D_2 = D$	$C \cdot (s \cdot I - A_{ss})^{-1} \cdot B_{ss}$	$C \cdot (z \cdot I - A_{ss} \cdot T)^{-1} \cdot T \cdot [(A_1 + A_2 - 2 \cdot A_3) \cdot X_{ss} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}]$

For comparison, bode plot of the derived digital small signal model is depicted in Figure 2.3 together with bode plots of analog small signal model and discretized analog model. The converter's specifications are Vin =48V, n=6, Vo=1V, Io= 50A, Co=1000 uF, Lo= 90 nH, and switching frequency of 400 KHz. It can be found that differences exist among these three models at high frequencies. Because digital systems will have additional phase shift compared to analog systems, a difference between the analog model and the digital model can be noticed at the high frequencies. Furthermore, it can be noticed that the discretized analog model starts to alias as it approaches half of the sampling frequency. Therefore, it can be concluded that the derived digital model is more valid than the other two models for digital compensator design

of the digitally controlled half bridge dc-dc converter.

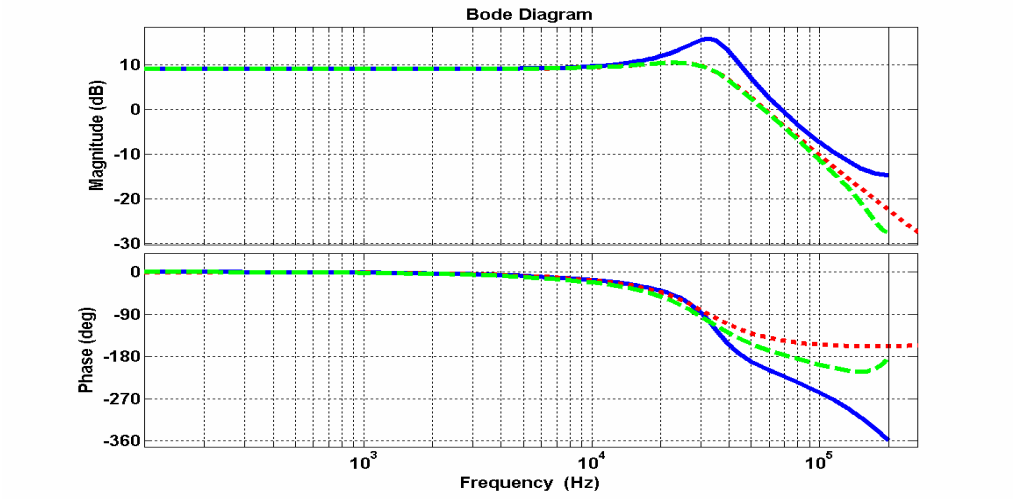


Figure 2.3 Bode diagrams of three converter models

(Dot trace: analog model, dash trace: discretized analog model,

solid trace: digital model)

A digital compensator based on the digital model of the converter is designed and the bode plot of its loop gain is shown in Figure 2.4. A prototype with the same design specification is built and the close loop bode plot is shown in Figure 2.5. The experimental results match theoretical design and therefore verify the derived digital model.

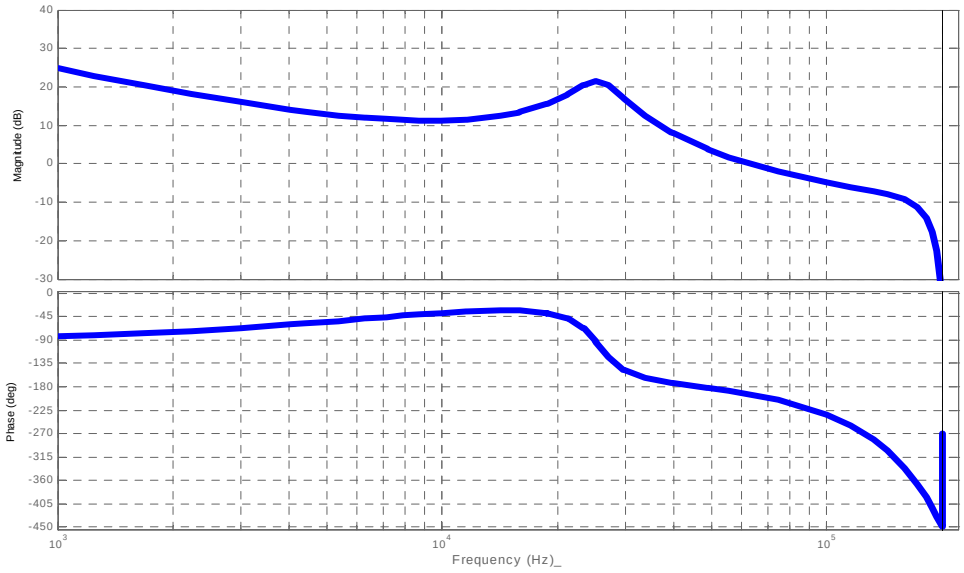


Figure 2.4 Close loop gain of theoretical design

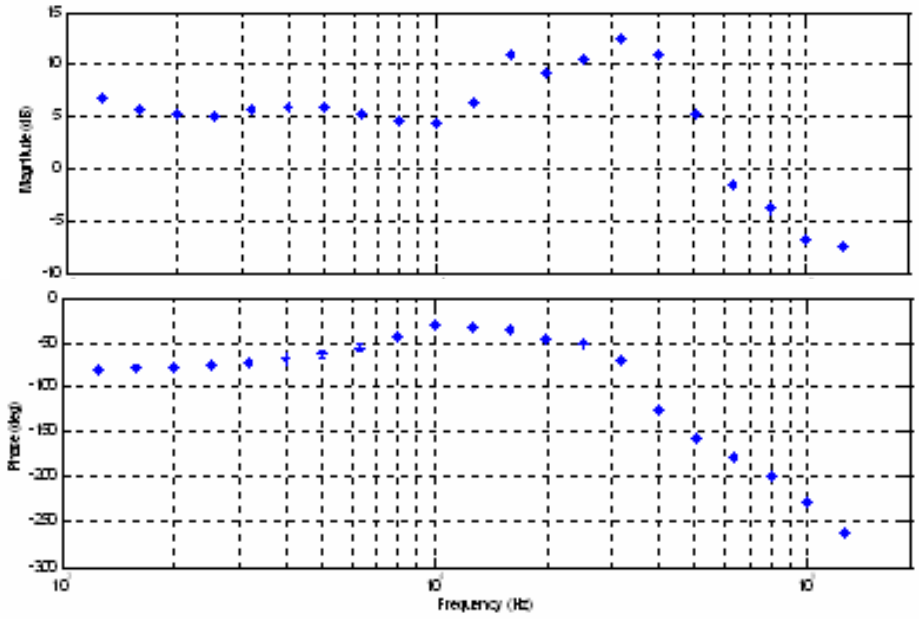


Figure 2.5 Close loop gain of experimental result

2.5. Digital Control of HB DC-DC Converter with Current Doubler Rectifier

The specifications of the half-bridge dc-dc converter prototype with current doubler rectification are listed as follows:

Vin =48V, n=6, Vo=1V, Io= 50A, fsw= 400kHz, Co=500 uF, Lo= 270 nH

Based on the small signal model of HB dc-dc converter and digital controller design theory, the digital controller is designed as follows:

$$Hc(z) = \frac{0.6113z^3 - 0.2847z^2 - 0.5968z + 0.2992}{z^3 - 1.418z^2 + 0.4619z - 0.04364} \tag{2-23}$$

The corresponding difference equation representation of the designed compensator is

D [n] =1.418 D [n-1] - 0.4619 D [n-2] +0.0436 D [n-3]

+0.6113 e[n] -0.2847e [n-1]-0.5968 e [n-2] +0.2992e [n-3] (2-24)

The digital compensator is implemented by TMS320F2812 DSP chip with DSP program with C language. A 12 bit ADC with 80 ns conversion time is set up for the digital controller in TMS320F2812 DSP chip. The DPWM can support 16 bit maximum resolution [24-27].

The DPWM generators in the DSP chip can generate symmetrical, asymmetrical and DCS PWM control signals for the half-bridge power stage.

Figure 2.6 shows the primary and secondary gate driving signals with 100ns dead time for HB with symmetrical control, which is generated by the DSP chip TMS320F2812. The two primary-side driving signals have the same duty cyle with a 180-degree phase shift, and the secondary-side driving signals are the complementary signals of the primary-side signals with a programmable dead time. In Figure 2.7, the asymmetrical primary-side gate driving signals

are shown with 100ns dead-time. Actually, the dead-times mentioned above are adjustable and programmable with DSP compensation program.

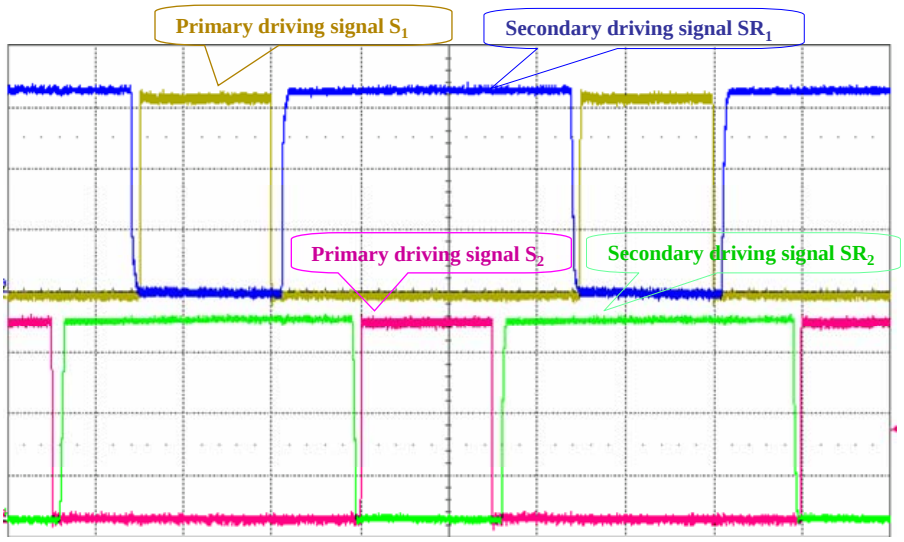


Figure 2.6: The primary-side and secondary-side gate driving signals with 100ns dead-time in symmetrical control case

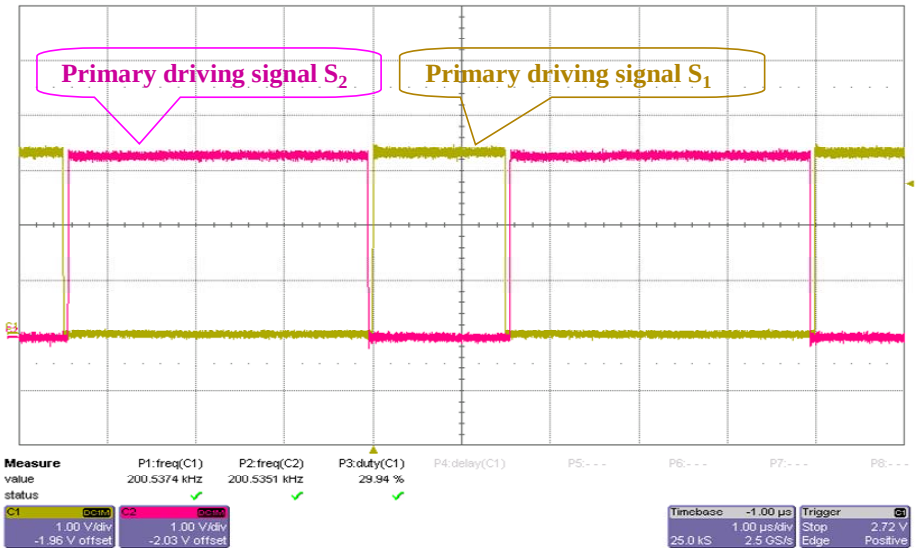


Figure 2.7: The gate signals with 100ns dead-time in asymmetrical control case.

Figure 2.8 shows the primary-side driving signals with 100ns dead-time in DCS control case. DCS control is used to reduce primary-side ringing of the signals. In DCS case, the two primary-side driving signals have the same duty cycle and shifted next to each other but with a fixed dead-time as compared with the traditional symmetrical control scheme. This dead-time is independent of the duty cycle and SR dead-time. Figure 2.9 shows the output voltage with significant noise and in this case the output is hard to regulate.

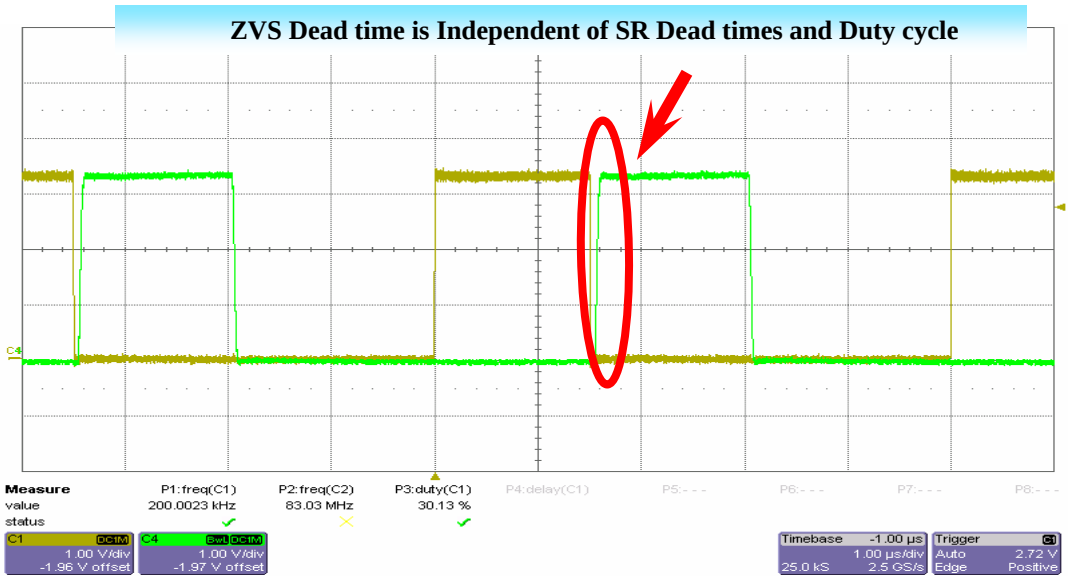


Figure 2.8: The primary signals with 100ns dead time in a DCS case

In the actual experiments, the close loop system was set up with the DSP-controlled HB power train as shown in Figure 2.10. The low-pass filter was used between the output of power stage and ADC input of the DSP board to filter out the switching noise. This filter also behaves as an anti-liaising filter for the sampling of the ADC. The protection circuit is used to give a voltage limit from 0 volts to 3 volts for the input signal of the DSP since that is the

range the DSP can accept.

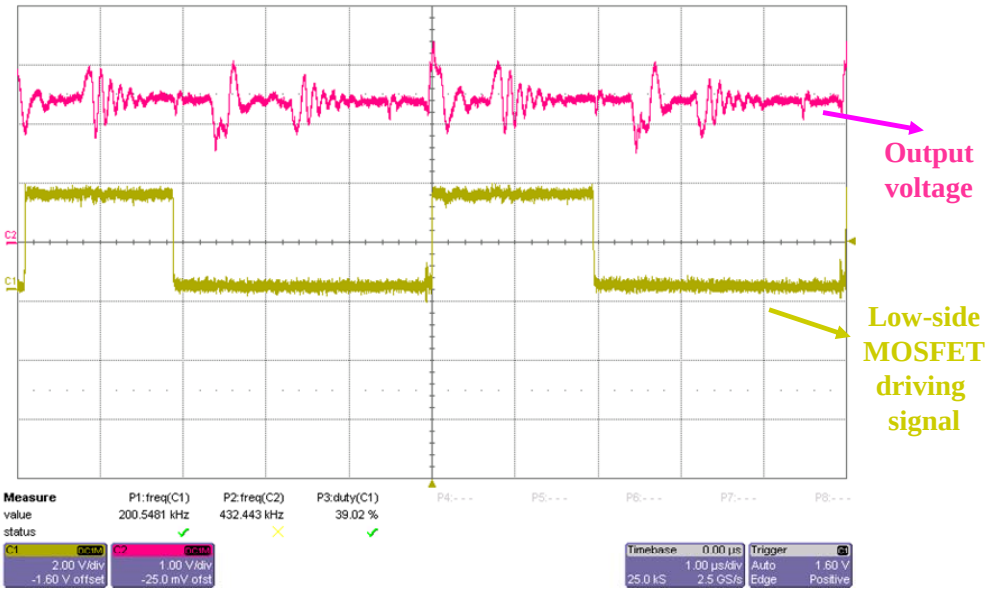


Figure 2.9: The output voltage with significant noise

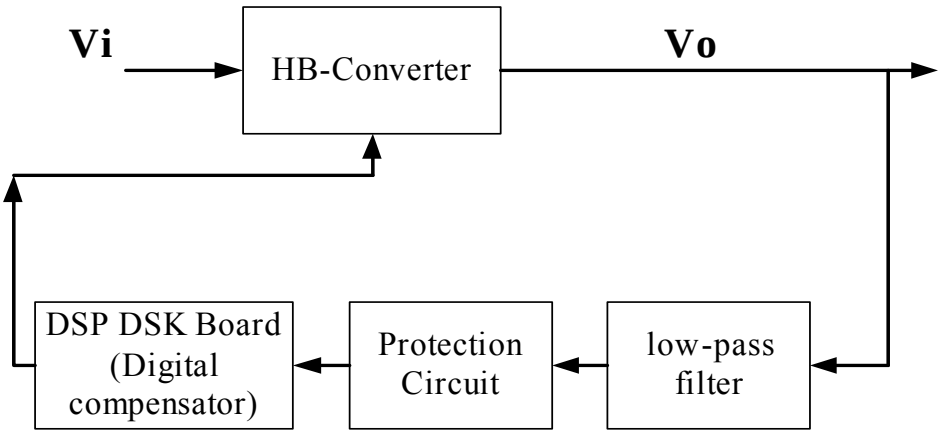


Figure 2.10: Close loop diagram with power stage and DSP controller

Figure 2.11 shows the output voltage and the gate signal for the closed-loop DSP

controller. In this case, the input voltage is 48 volts. It can be seen that the output voltage is regulated to the reference voltage of 1.5 volts, which is actually set up by the DSP program. The duty cycle is regulated at D=0.26, which is the calculation result of a digital PI compensator based on the error difference compared to the reference voltage. Figure 2.12 and 2.13 show the transformer primary-side current at steady state.

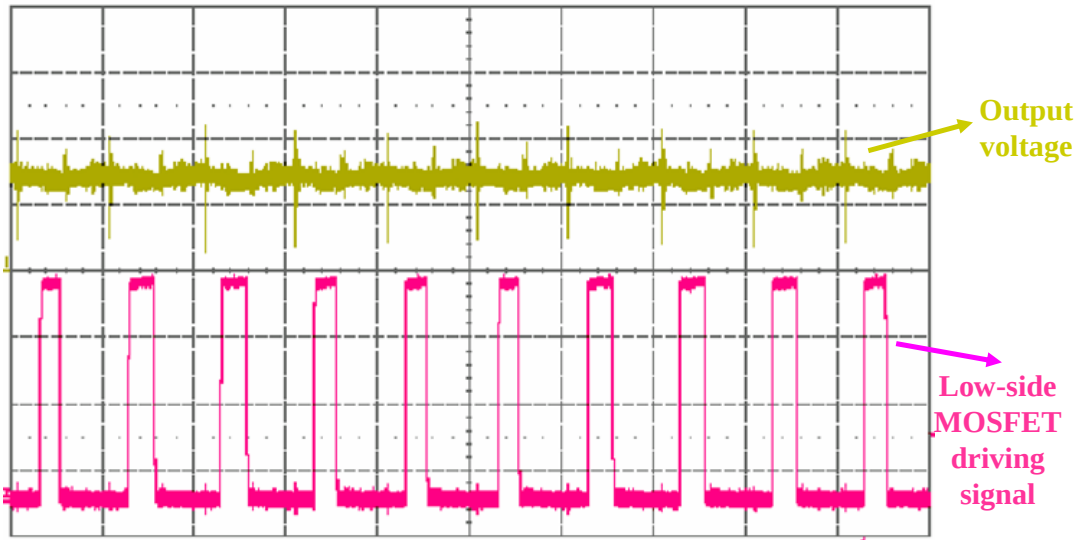


Figure 2.11: The output voltage 1.5 volt and gate signal with 0.26 duty cycle at steady state with a DSP controller (digital PI compensator) in symmetrical control case

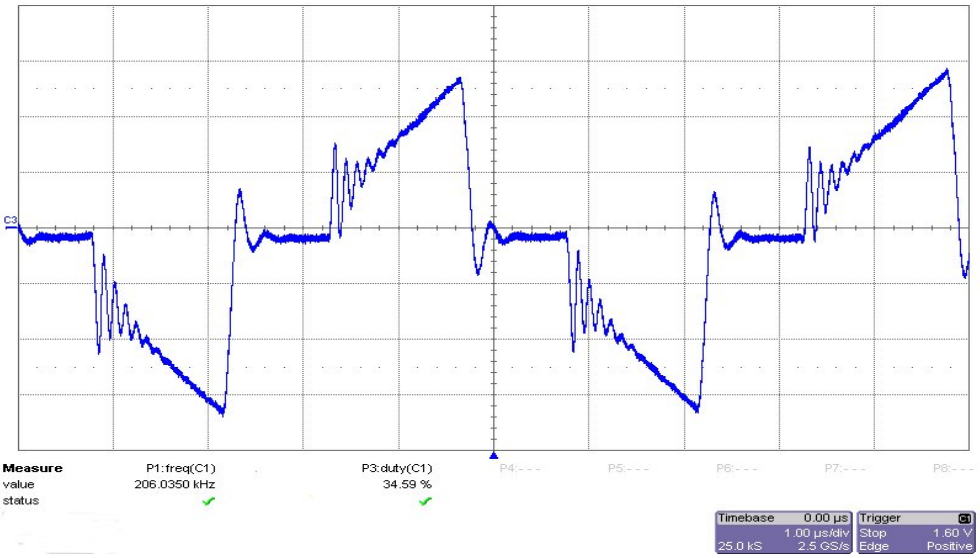


Figure 2.12: The transformer primary current waveform for symmetrical control case

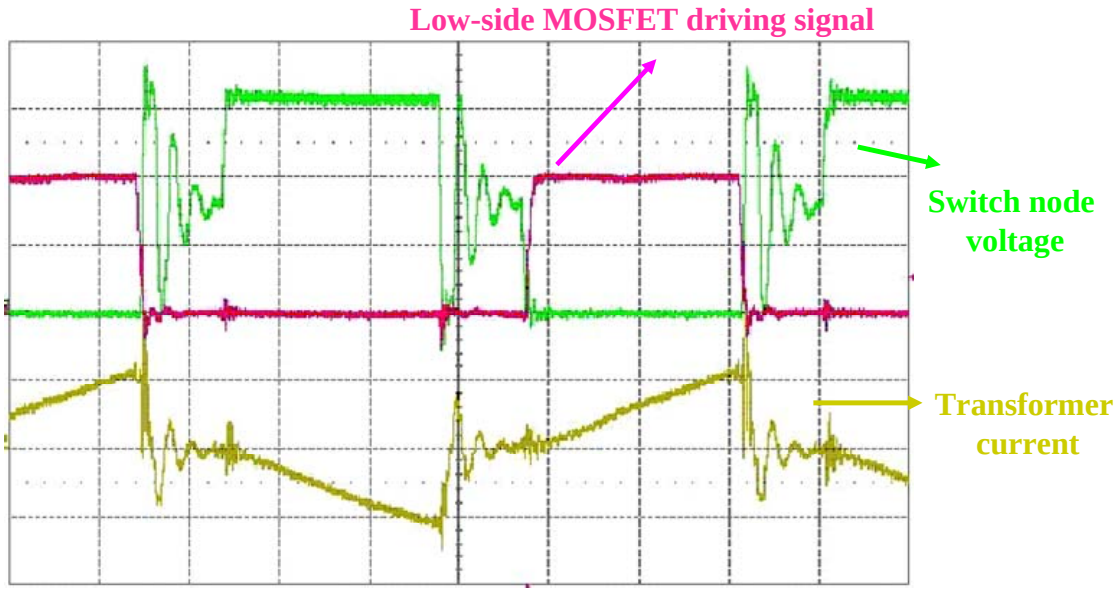


Figure 2.13: The transformer primary-side current and switch-node voltage

CHAPTER THREE: CURRENT SHARING ANALYSIS OF CURRENT DOUBLER RECTIFIER

With the increased output currents in both isolated and non-isolated Point-of-Load (POL) converters, the number of phases in a converter and the number of paralleled converters have been increasing. For high output current and low output voltage, the current sharing among paralleled channels is highly demanded, because uneven current distribution causes inductor saturation, thermal stresses and degraded converter performance [45-50]. Current sharing control with paralleled converters is generally implemented with external load sharing circuitry [45]. In voltage regulators (VRs) for microprocessors, multi-phase interleaved synchronous-rectifier (SR) buck converters are controlled by dedicated ICs with built-in current-sharing circuitry [45-47]. Various current sharing methods and circuitry have been documented and utilized in industry [45-50]. However, the original numerical analysis of the current sharing in multi-phase interleaved buck converters is not investigated in depth and open-loop current sharing steady-state models are not established in term of various parameters in the converters.

For isolated dc-dc converters, the interleaving concept enables converter topologies to operate at increased power levels. Other benefits include: reduced input and output voltage/current ripples, better thermal management and improved transient response [51]. Current Doubler Rectifier (CDR) is a good topology for low output voltage high output current applications. Actually, CDR is similar to an interleaved two-phase buck converter in term of rectification architecture. The current sharing issue between two inductors in CDR is brought up and the generalized current-sharing dc model is established in [52-53].

In this chapter, the current sharing characteristic in an interleaved buck converter is analyzed and compared with the current sharing model of the CDR in isolated dc-dc converters. Design guidelines are provided based on numerical analyses. Furthermore, a new CDR topology is proposed to achieve passive current sharing without additional current sharing control circuitry, which is verified by mathematical model and experimental results.

3.1 DC Current Sharing Analysis in the Interleaved Two-phase Buck Converters

A two-phase buck converter is shown in Figure. 3.1. Assuming driving signals of the two channels are interleaved with 180^0 phase difference, and under ideal conditions, two phases' parameters are absolutely symmetric. This means filter inductance, FET on-resistance and inductor DCR values in channel 1 and 2 are identical. Besides, actual duty cycles for each channel are identical.

In practice, the two channels of the converter are asymmetric, and even the actual duty cycle values of each channel may not be equal due to different driver propagation and FETs turn-on and turn-off delays. In this case, it is unlikely the two inductors carry equal average currents because of possible asymmetry parameters. dc modeling under asymmetric conditions will be provided thorough analytic equations below.

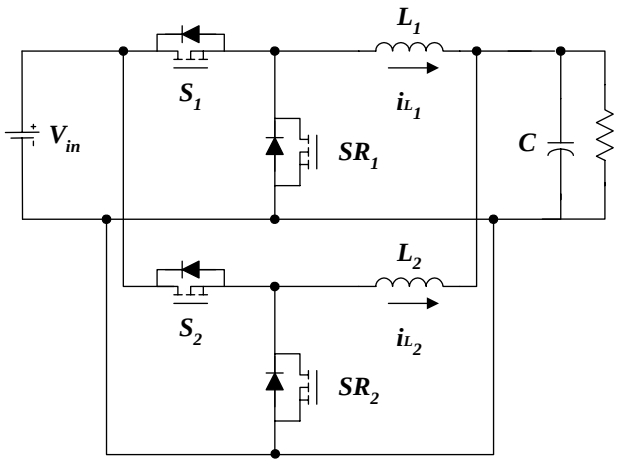


Figure 3.1. Two-phase buck converter

Average modeling method in [52-55] can be applied to the analysis. Assuming steady-state duty cycles $D_1<0.5$, $D_2<0.5$, and the converter modes of operation can be concluded in three modes as shown in Figure. 3.2 (a), (b) and (c).

For each mode during the period, the converter can be denoted using a set of linear state-space equations. Corresponding to three modes of operation, three sets of state-space equations are expressed as (3-1), where x is the vector of state variables, u is the vector of independent sources; A_1, B_1, A_2, B_2, A_3 and B_3 are respective system matrices for each of the three switched networks.

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{3-1}$$

The state-space variables are defined as follows:

$$\dot{x} = \left[\frac{di_{L1}}{dt} \quad \frac{di_{L2}}{dt} \quad \frac{dv_C}{dt} \right]^T \tag{3-2}$$

$$x = \begin{bmatrix} i_{L1} & i_{L2} & v_C \end{bmatrix}^T;$$

$$u = \begin{bmatrix} V_{in} & I_o \end{bmatrix}^T \tag{3-3}$$

A_1, B_1, A_2, B_2, A_3 and B_3 can be derived from modes of operation in Figure. 3.2(a), (b) and (c), respectively. Assuming the duty cycle of the switch S_1 and S_2 are d_1 and d_2, respectively. The key concept in state-space averaging is the replacement of the above three sets of state-space equations by a single equivalent set [54]

$$\dot{x} = Ax + Bu \tag{3-4}$$

where the equivalent matrices are defined by

$$A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3$$

$$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3 \tag{3-5}$$

where, A_1, B_1 are state-space matrices of Mode 1; A_2 and B_2 are state-space matrices of Mode 2; A_3 and B_3 are state-space matrices of Mode 3. All these matrices can be derived from Figure. 3.2 as follows:

$$A_1 = \begin{bmatrix} -\dfrac{R_C + R_{L1} + R_{onS1}}{L_1} & -\dfrac{R_C}{L_1} & -\dfrac{1}{L_1} \\ -\dfrac{R_C}{L_2} & -\dfrac{R_{L2} + R_C + R_{SR2}}{L_2} & -\dfrac{1}{L_2} \\ \dfrac{1}{C} & \dfrac{1}{C} & 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\dfrac{R_C + R_{L1} + R_{SR1}}{L_1} & -\dfrac{R_C}{L_1} & -\dfrac{1}{L_1} \\ -\dfrac{R_C}{L_2} & -\dfrac{R_{L2} + R_C + R_{onS2}}{L_2} & -\dfrac{1}{L_2} \\ \dfrac{1}{C} & \dfrac{1}{C} & 0 \end{bmatrix}$$

$$A_3 = \begin{bmatrix} -\dfrac{R_C + R_{L1} + R_{SR1}}{L_1} & -\dfrac{R_C}{L_1} & -\dfrac{1}{L_1} \\ -\dfrac{R_C}{L_2} & -\dfrac{R_{L2} + R_C + R_{SR2}}{L_2} & -\dfrac{1}{L_2} \\ \dfrac{1}{C} & \dfrac{1}{C} & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \dfrac{1}{L_1} & \dfrac{R_C}{L_1} \\ 0 & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \end{bmatrix}; \quad B_2 = \begin{bmatrix} 0 & \dfrac{R_C}{L_1} \\ \dfrac{1}{L_2} & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \end{bmatrix}; \quad B_3 = \begin{bmatrix} 0 & \dfrac{R_C}{L_1} \\ 0 & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \end{bmatrix}$$

The steady-state solution, with dc values indicated by capital letters, is obtained by setting $\dot{x} = 0$

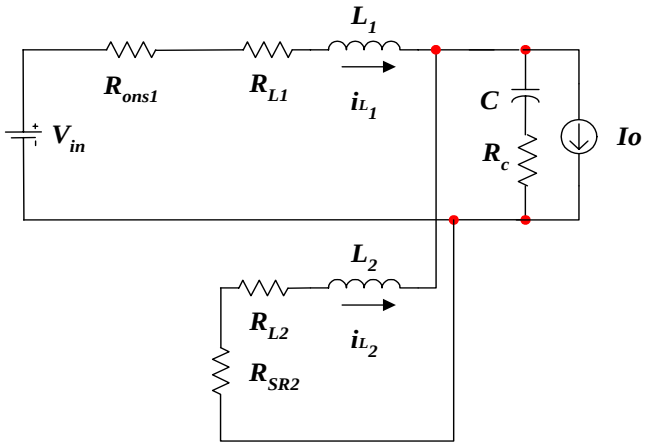
$$X = -A^{-1} B U \tag{3-6}$$

Through (3-1) ~ (3-6), the steady-state dc quiescent points can be derived and the

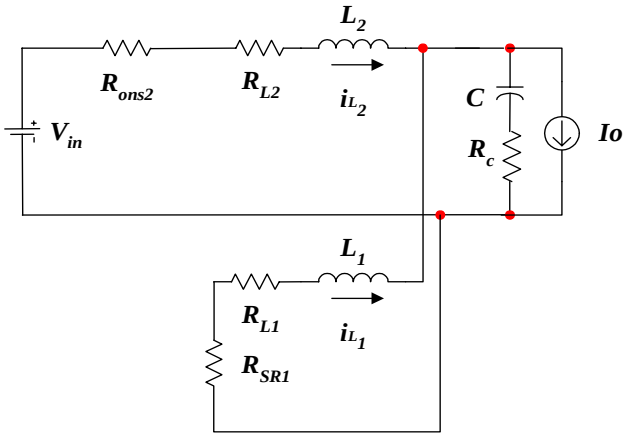
inductor dc currents are:

$$I_{L1} = \frac{(D_1 - D_2)V_{in} + [(1-D_2)R_{SR2} + D_2 R_{onS2} + R_{L2}]I_o}{D_1 R_{onS1} + D_2 R_{onS2} + (1-D_1)R_{SR1} + (1-D_2)R_{SR2} + R_{L1} + R_{L2}} \tag{3-7}$$

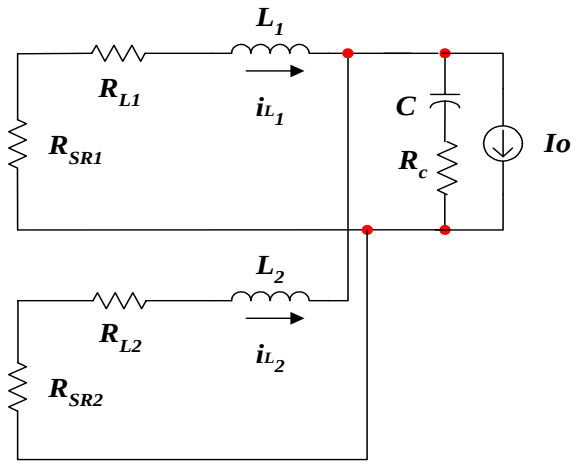
$$I_{L2} = \frac{(D_2 - D_1)V_{in} + [(1-D_1)R_{SR1} + D_1 R_{onS1} + R_{L1}]I_o}{D_1 R_{onS1} + D_2 R_{onS2} + (1-D_1)R_{SR1} + (1-D_2)R_{SR2} + R_{L1} + R_{L2}} \tag{3-8}$$



(a) Mode 1: S_1, SR_2 on; S_2, SR_1 off



(b) Mode 2: S_2, SR_1 on; S_1, SR_2 off



Mode 3: SR_1, SR_2 on; S_1, S_2 off

Figure 3.2. Modes of operation

To simplify the above equations, we define the equivalent resistance of phase 1 and phase 2, respectively:

$$R_{eq\_ch1} = (1 - D_1)R_{SR1} + D_1 R_{onS1} + R_{L1} \tag{3-9}$$

$$R_{eq\_ch2} = (1 - D_2)R_{SR2} + D_2 R_{onS2} + R_{L2} \tag{3-10}$$

Equation (3-7) and (3-8) are reformed as:

$$I_{L1} = \frac{(D_1 - D_2)V_{in}}{R_{eq\_ch1} + R_{eq\_ch2}} + \frac{R_{eq\_ch2}}{R_{eq\_ch1} + R_{eq\_ch2}} I_o \tag{3-11}$$

$$I_{L2} = \frac{(D_2 - D_1)V_{in}}{R_{eq\_ch1} + R_{eq\_ch2}} + \frac{R_{eq\_ch1}}{R_{eq\_ch1} + R_{eq\_ch2}} I_o \tag{3-12}$$

From (3-11) and (3-12), we may conclude:

(a) Inductance and capacitance values have no effect on current sharing between two

filter inductors.

(b) Current sharing can be achieved if the two channels operate under both equal duty cycle and balanced resistance.

(c) Under asymmetric dc resistances ($R_{eq\_ch1} \neq R_{eq\_ch2}$), current sharing can be achieved by adjusting duty cycle values. Increasing duty cycle value in one channel leads to an increase in average current of this channel. This current sharing technique has been widely utilized in current sharing of VR (M)s.

(d) To achieve balanced current sharing, duty cycles has to be adjusted to satisfy:

$$D_1 - D_2 = \frac{R_{eq\_ch1} - R_{eq\_ch2}}{V_{in}} \frac{I_o}{2} \tag{3-13}$$

3.2 Current Sharing of Current Doubler Rectifier in Isolated DC-DC Converters

As shown above, the analytic results show that all dc parameters in an interleaved buck converter have effect on current sharing, and, fortunately, imbalance of average phase currents can be calibrated by adjusting phase duty cycles.

Current doubler rectifier shows good performance in low-voltage double-ended isolated dc-dc converters, such as full bridge and push pull. In such isolated topologies, peak current mode control can be implemented to achieve balanced dc currents. However, for half bridge topology with a current doubler rectifier, peak current mode control cannot be implemented due to collapse of an input capacitor voltage [56]. Therefore, current sharing in the topology is worth investigating. Figure 3.3 shows a half bridge dc-dc converter with a current doubler rectifier. Compared with interleaved two-phase buck converters, the primary

switches are corresponding to upper switches in the buck converter. Assuming the converter operates under asymmetric dc parameters and duty cycles. Transformer primary winding resistance is R_{Tp} and secondary winding resistance is R_{Ts}; R_{L1} and R_{L2} are inductor DCR values. Like in an interleaved buck converter, S_1 gate signal and SR_1 gate signal are complementary as in a channel; and S_2 and SR_2 gate signals are complementary in the other channel.

Applying the same analytic method for the buck converter as described above to the half bridge dc-dc converter in Figure. 3.3, average currents in the three magnetic components can be derived:

$$I_{L1} = \frac{R_{L2} + \frac{D_2 R_{Ts}}{D_1 + D_2}}{R_{Ts} + R_{L1} + R_{L2}} I_o \tag{3-14}$$

$$I_{L2} = \frac{R_{L1} + \frac{D_1 R_{Ts}}{D_1 + D_2}}{R_{Ts} + R_{L1} + R_{L2}} I_o \tag{3-15}$$

$$I_M = \frac{\frac{D_2}{D_1 + D_2} R_{L1} - \frac{D_1}{D_1 + D_2} R_{L2}}{R_{Ts} + R_{L1} + R_{L2}} \frac{I_o}{n} \tag{3-16}$$

where I_o is the converter output current; D_1 and D_2 are steady-state duty cycle values for S_1 and S_2, respectively.

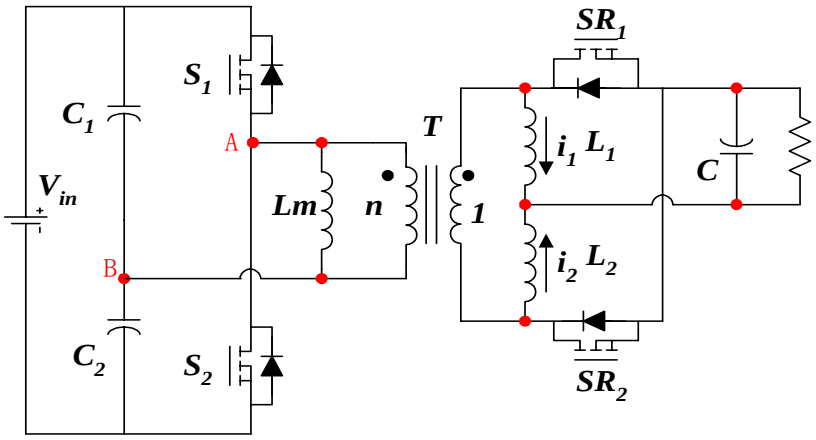


Figure 3.3 Half-bridge dc-dc converter with current doubler rectifier

From (3-14) ~ (3-16), we may conclude:

a) Current sharing is only determined by dc resistance values and steady-state duty cycles, while inductor inductance, transformer magnetizing inductance and filter capacitance have no effect on the current sharing.

b) Only inductor DCRs, transformer secondary winding DCR and steady-state duty cycles determine current sharing of two channels. It is clear that transformer primary winding DCR, primary-side FETs' on-resistance and secondary-side SRs' on-resistance values have no effect on the current sharing.

c) Current sharing can be achieved if two inductor DCR values are equal under symmetric duty cycles. If the two channels are driven symmetrically, inductor DCRs tolerance and layout in planner inductor design determine the current sharing.

d) Under asymmetric driving or unequal inductor DCR values, dc current bias of

magnetizing inductance exists. In order to achieve zero dc magnetizing current bias, the following equation should be satisfied:

$$D_2 R_{L1} - D_1 R_{L2} = 0 \tag{3-17}$$

e) Under asymmetric inductor DCR values, even current distribution can be achieved by adjusting the steady-stage duty cycle values to satisfy:

$$\frac{D_2 - D_1}{D_1 + D_2} = \frac{R_{L1} - R_{L2}}{R_{Ts}} \tag{3-18}$$

f) Both (3-17) and (3-18) cannot be satisfied with certain duty cycles unless $R_{L1} = R_{L2}$, which means zero dc magnetizing current and equal current sharing cannot be achieved by adjusting duty cycles.

3.3 Comparison of Two-phase Buck Converters with a Current Doubler Rectifier in Half-bridge DC-DC Converters

In both two-phase buck converter and current doubler rectifiers, current sharing depends on dc parameters and steady-state duty cycles. In buck converter, all the dc resistance values including switch and SR on-resistance and inductor DCRs, have effect on the current sharing. Besides, input voltage Vin has effect on current sharing when the two phases are asymmetrically driven ($D_1 \neq D_2$). While in the current doubler rectifier, the current sharing equations become more straightforward since only the inductor DCR values determine the current distribution. Transformer secondary winding DCR has effect on the current sharing only when the converter is asymmetrically driven ($D_1 \neq D_2$). Therefore, two-phase buck

converter is more likely to operate with asymmetric current distribution than the current doubler rectifier because of FETs' on-resistance tolerance and the high temperature sensitivity. Current sharing techniques have to be applied to multi-phase buck converters to achieve balanced inductor current.

Fortunately, as shown in (3-11) and (3-12), phase average currents are a function of duty cycle D_1 and D_2, and thus asymmetric current distribution can be adjusted to be symmetric by changing duty cycles. It can be noted that the first terms in (3-11) and (3-12) are very sensitive to duty cycle change. Thus the current distribution can be easily balanced by adjusting the asymmetry of steady-state duty cycles to balance the two-phase current sharing. In VR (M) applications, a closed-loop circuitry is implemented in a dedicated controller IC to balance two-phase currents.

In the current doubler rectifier, likewise, the current sharing can be achieved under asymmetric DCRs. However, the adjustment effect depends on transformer secondary DCR values. The adjusting effect can be expressed as:

$$\frac{\Delta I_{L1}}{I_o} = -\frac{R_{Ts}}{R_{Ts}+R_{L1}+R_{L2}} \cdot \frac{D_2}{(D_1+D_2)^2} \Delta D_1 \tag{3-19}$$

$$\frac{\Delta I_{L2}}{I_o} = -\frac{R_{Ts}}{R_{Ts}+R_{L1}+R_{L2}} \cdot \frac{D_1}{(D_1+D_2)^2} \Delta D_2 \tag{3-20}$$

It can be observed clearly from (3-19) and (3-20) that a duty cycle increase in a channel leads to the inductor current decrease in the corresponding channel. Therefore, the duty cycle adjustment direction in the half-bridge dc-dc converter with a current doubler rectifier is opposite to that in the two-phase buck converter. For example, if Channel 1 carries higher

current for some reasons, to balance the two-phase currents, in the two-phase buck converter, we should lower the duty cycle in Channel 1, while in the current doubler rectifier, an increment should be added to the duty cycle of Channel 1, and vice versa.

Compared with the two-phase buck converter, the current change in the current doubler rectifier is less sensitive to duty cycle change as shown in Figure. 3.4, where asymmetric DCR resistance values can be assumed as: $R_{L_2} = R_L$, $R_{L_1} = R_L + \Delta R_{L_1}\% \cdot R_L$, $\Delta R_{L_1}\%$ is defined as:

$$\Delta R_{L1}\% = \frac{\Delta R_{L1}}{R_L} = \frac{R_{L1} - R_L}{R_L} \tag{3-21}$$

Unequal current sharing resulting from asymmetric DCR resistance values can be adjusted by changing duty cycle value of Channel 1 assuming Channel 2 has a fixed duty cycle value ($D_2 = D$). $\Delta D_1\%$ is defined as:

$$\Delta D_1\% = \frac{\Delta D_1}{D} = \frac{D_1 - D}{D} \tag{3-22}$$

According to (3-14) and (3-15), the adjustment sensitivity is determined by the ratio: $R_n = R_{Ts}/R_L$. The higher ratio R_n, the higher regulation sensitivity can be achieved. However, since the sensitivity is determined by power train design and layout, limited options can be made there.

Figure 3.4 shows three curves for Rn=0.5, 1, and 2, respectively. For a typical dc-dc converter design, the Rn should fall in the range of 0.2-2.0. Using the best situation for the highest sensitivity to regulate unbalanced currents in the figure, for example Rn=2, for +40% inductor DCR tolerance from a nominal value, around -33% duty cycle offset is needed to be set to balance the current. For a symmetric half-bridge dc-dc converter, this offset is far beyond

what is acceptable; because asymmetric duty cycles result in uneven voltage stress across SRs and transformer dc magnetizing current bias.

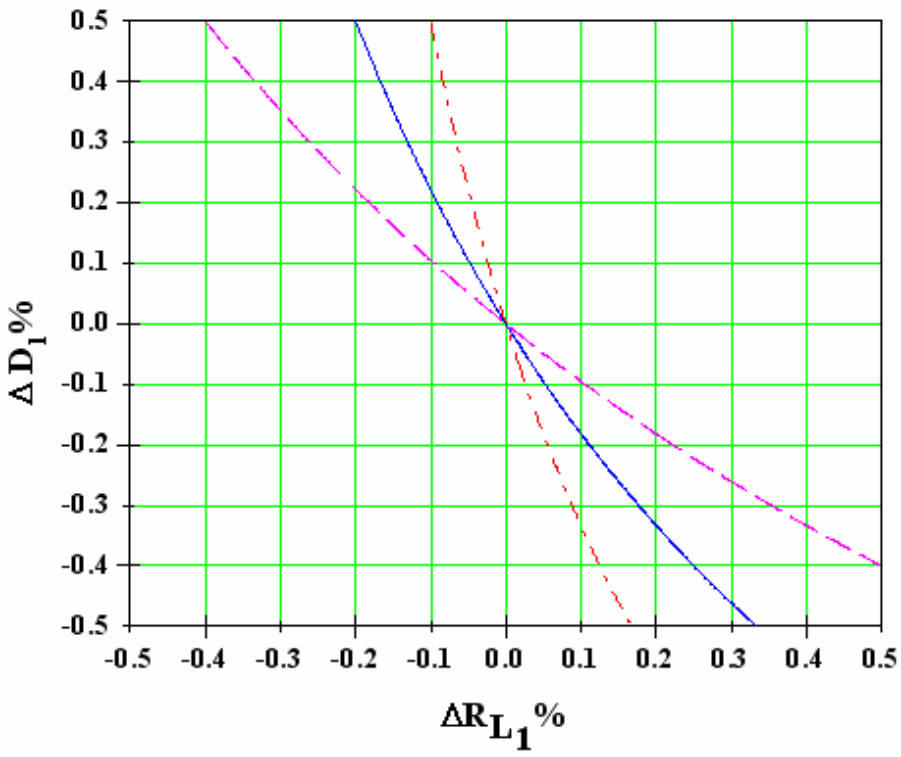


Figure 3.4 Duty cycle offset under asymmetric inductor DCR values (curve with highest slope: Rn = 0.5; curve with medium slope: Rn = 1; curve with lowest slope: Rn = 2)

From Figure 3.4, it is obvious that the duty cycle adjustment in CDR is less effective to achieve equal current sharing than the two-phase buck converter since the duty cycle adjustment range is limited by maximum duty cycle value 0.5 for symmetric half bridge dc-dc converter. In addition, when the duty cycles are adjusted to be highly asymmetric, the converter voltage gain is affected and the converter operating point will shift to a worse

condition that is not allowed for symmetric controlled half-bridge dc-dc converters. The general dc voltage gain is:

$$\frac{V_o}{V_{in}} = \frac{D_1 D_2}{n(D_1 + D_2)} \tag{3-23}$$

Moreover, as mentioned in Section 3.2, dc current bias is unavoidable when current sharing is achieved under asymmetric inductor DCR values Therefore, it may not be a good approach to achieve current sharing by adjusting duty cycles for a symmetrically controlled half-bridge dc-dc converter.

3.4 Proposed Half-bridge Current-doubler-rectifier DC-DC Topology with Passive Current Sharing

As mentioned above, due to asymmetric dc resistive parameters in the two channels of current doubler, unbalanced dc inductor currents degrade the converter performance. A careful design and layout have to be done to reduce the asymmetry of current distribution.

A half-bridge CDR dc-dc converter with passive current sharing is shown in Figure. 3.5, wherein, simply, an additional capacitor with low voltage rating is added in series with transformer secondary winding. The converter operates in the exactly same way as a conventional symmetric half-bridge dc-dc converter with three typical modes as shown in Figure. 3.6 (a), (b) and (c) respectively.

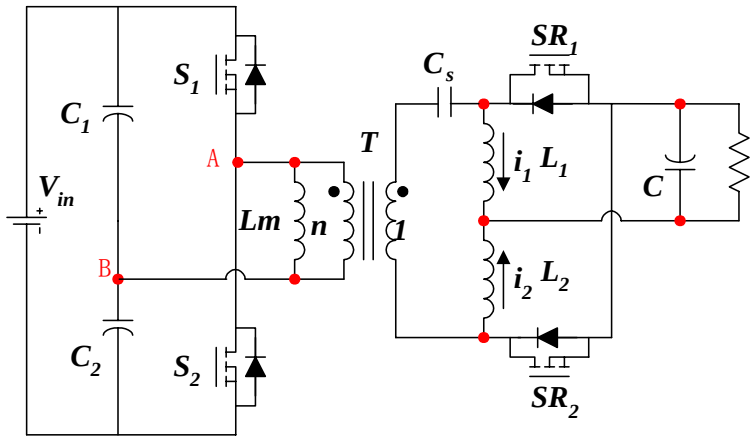


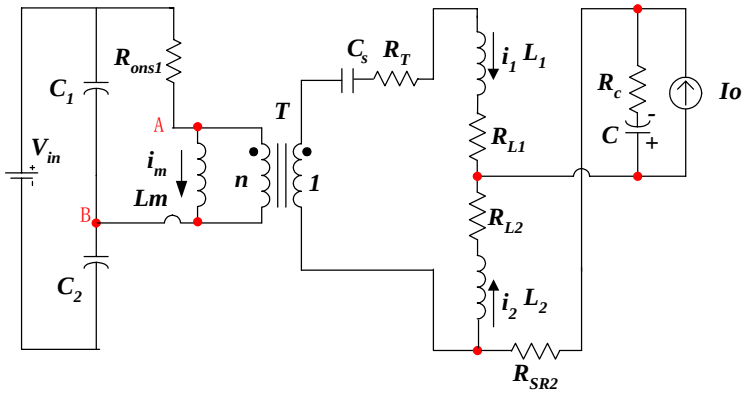
Figure 3.5 Half-bridge dc-dc converter with the modified current doubler rectifier

The converter state-space variables are defined as:

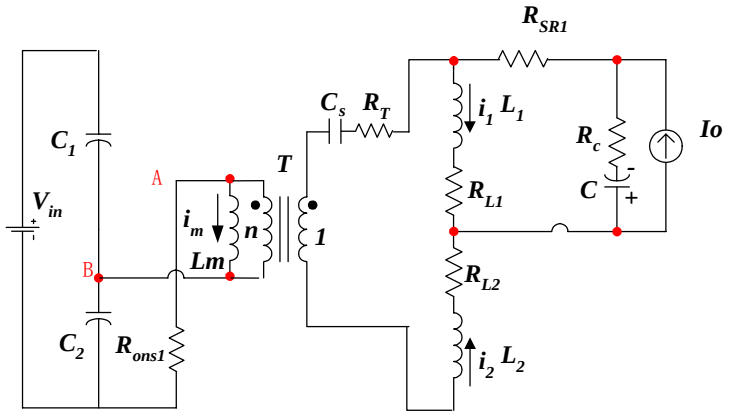
$$\dot{x} = \left[\frac{dv_{C1}}{dt} \quad \frac{di_{L1}}{dt} \quad \frac{di_{L2}}{dt} \quad \frac{dv_C}{dt} \quad \frac{di_m}{dt} \quad \frac{dv_{CS}}{dt} \right]^T$$

$$x = \left[v_{C1} \quad i_{L1} \quad i_{L2} \quad v_C \quad i_m \quad v_{CS} \right]^T;$$

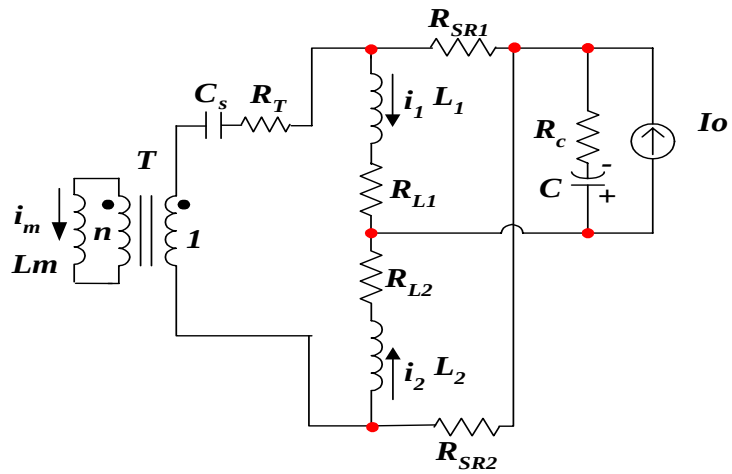
$$u = \left[V_{in} \quad I_o \right]^T \tag{3-24}$$



(a) Mode 1: S_1 on



(b) Mode 2: S_2 on



(c) Mode 3: Both S_1 and S_2 off

Figure 3.6. Modes of operation for the proposed half-bridge dc-dc converter with passive current sharing

Employing the average modeling method aforementioned, where matrices A_1-A_3 and B_1-B_3 are:

$$A_1=\begin{bmatrix} 0 & -\frac{1}{n(C_1+C_2)} & 0 & 0 & -\frac{1}{C_1+C_2} & 0 \\ \frac{1}{nL_1} & -\frac{\frac{R_{ons1}}{n^2}+R_T+R_{L1}+R_C+R_{SR2}}{L_1} & -\frac{R_C+R_{SR2}}{L_1} & -\frac{1}{L_1} & -\frac{R_{ons1}}{nL_1} & -\frac{1}{L_1} \\ 0 & -\frac{R_C+R_{SR2}}{L_2} & -\frac{R_{L2}+R_C+R_{SR2}}{L_2} & -\frac{1}{L_2} & 0 & 0 \\ 0 & \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 \\ \frac{1}{L_m} & -\frac{R_{ons1}}{nL_m} & 0 & 0 & -\frac{R_{ons1}}{L_m} & 0 \\ 0 & \frac{1}{C_s} & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$A_2=\begin{bmatrix} 0 & 0 & \frac{1}{n(C_1+C_2)} & 0 & -\frac{1}{C_1+C_2} & 0 \\ 0 & -\frac{R_{L1}+R_C+R_{SR1}}{L_1} & -\frac{R_C+R_{SR1}}{L_1} & -\frac{1}{L_1} & 0 & 0 \\ -\frac{1}{nL_2} & -\frac{R_C+R_{SR1}}{L_2} & -\frac{\frac{R_{ons2}}{n^2}+R_T+R_{L2}+R_C+R_{SR1}}{L_2} & -\frac{1}{L_2} & \frac{R_{ons2}}{nL_2} & \frac{1}{L_2} \\ 0 & \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 \\ \frac{1}{L_m} & 0 & \frac{R_{ons2}}{nL_m} & 0 & -\frac{R_{ons2}}{L_m} & 0 \\ 0 & 0 & -\frac{1}{C_s} & 0 & 0 & 0 \end{bmatrix}$$

$$A_3=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\dfrac{R_{L1}+R_C+R_{SR1}}{L_1} & -\dfrac{R_C}{L_1} & -\dfrac{1}{L_1} & -\dfrac{nR_{SR1}}{L_1} & 0 \\ 0 & -\dfrac{R_C}{L_2} & -\dfrac{R_{L2}+R_C+R_{SR2}}{L_2} & -\dfrac{1}{L_2} & \dfrac{nR_{SR2}}{L_2} & 0 \\ 0 & \dfrac{1}{C} & \dfrac{1}{C} & 0 & 0 & 0 \\ 0 & -\dfrac{nR_{SR1}}{L_m} & \dfrac{nR_{SR2}}{L_m} & 0 & -\dfrac{n^2(R_T+R_{SR1}+R_{SR2})}{L_m} & \dfrac{n}{L_m} \\ 0 & 0 & 0 & 0 & -\dfrac{n}{C_s} & 0 \end{bmatrix}$$

$$B_1=\begin{bmatrix} 0 & 0 \\ 0 & \dfrac{R_C}{L_1} \\ 0 & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad B_2=\begin{bmatrix} 0 & 0 \\ 0 & \dfrac{R_C}{L_1} \\ \dfrac{1}{nL_2} & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \\ -\dfrac{1}{L_m} & 0 \\ 0 & 0 \end{bmatrix} \quad B_3=\begin{bmatrix} 0 & 0 \\ 0 & \dfrac{R_C}{L_1} \\ 0 & \dfrac{R_C}{L_2} \\ 0 & -\dfrac{1}{C} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

DC current solutions for the proposed topology shown in Figure.3.5 can be derived according to (3-4) ~ (3-6):

$$I_{L1}=\frac{D_2}{D_1+D_2}I_o \tag{3-25}$$

$$I_{L2}=\frac{D_1}{D_1+D_2}I_o \tag{3-26}$$

$$I_M = 0 \tag{3-27}$$

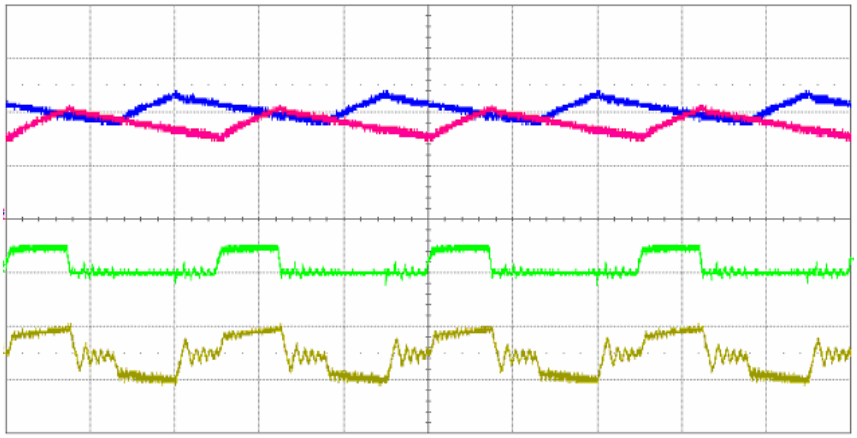
where Io is the converter output current, and D_1 and D_2 are steady-state duty cycle values for S_1 and S_2, respectively. Compared to the conventional symmetric half-bridge dc-dc converter, it is obvious that in the modified topology, current sharing is only determined by steady-state duty cycles, and inductor DCRs no longer have an effect on the dc current sharing any more. In other words, balanced current sharing can be achieved simply by keeping the steady-stage duty cycle values identical. It is always the case that nearly equal duty cycles can be assured with dedicated half-bridge controller and FET driver. Moreover, no dc bias magnetizing current exists in the transformer, resulting in simple design and high-efficiency of transformer.

3.5 Experimental Results

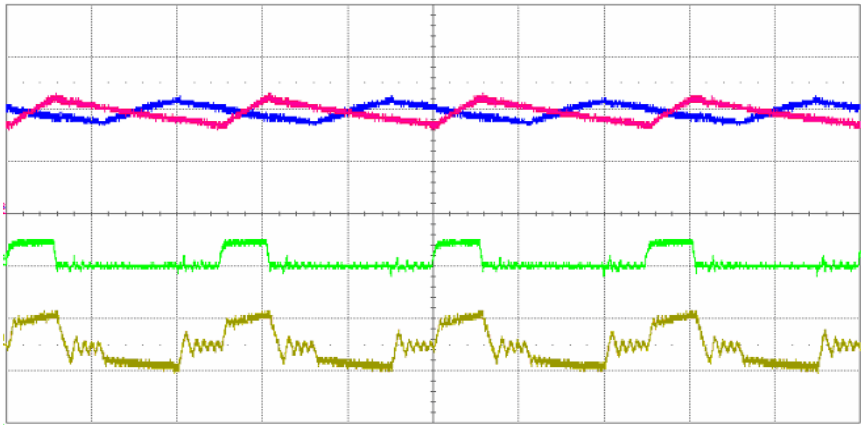
A prototype of HB dc-dc CDR converter is built with current sharing control loop. The converter operates at 36V-75V input voltage and 3.3V/20A output with switching frequency of 200 kHz. Due to the design asymmetry, the inductor DCR values originally are not identical. Experimental waveforms are shown in Figure. 3.7. Without current sharing control, it can be observed that two inductors share unequal currents under symmetric duty cycles as shown in Figure. 3.7 (a). By applying current sharing control, duty cycles are adjusted to achieve equal current sharing as shown in Figure. 3.7(b). The asymmetric duty cycles is observed from transformer primary current in the figure.

To verify the proposed topology shown in Figure 3.5, intentionally, an external resistor of 7.5m Ohm is added in series with inductor L_1 to make DCRs more unbalanced. Under this

condition, for comparison, the capacitor Cs is shorted, and the converter is driven symmetrically with equal duty cycles. The corresponding experimental waveforms are shown in Figure. 3.8, where current imbalance is observed due to unequal inductor CDR values, which agrees with the derived equations from the steady-state model in (3-14) and (3-15).



(a) Asymmetric inductor DCR values without current sharing control, $D_1 = D_2 = 30\%$, Io=20A



(b) Asymmetric inductor DCR values with current sharing control

$D_1 = 37\%$, $D_2 = 23\%$, Io=20 A

Figure.3.7 Conventional HB dc-dc Converter (Top two traces: two inductor currents (5A/div); middle trace: switch Vgs1 (20V/div); bottom trace: transformer primary current I_p (5A/div))

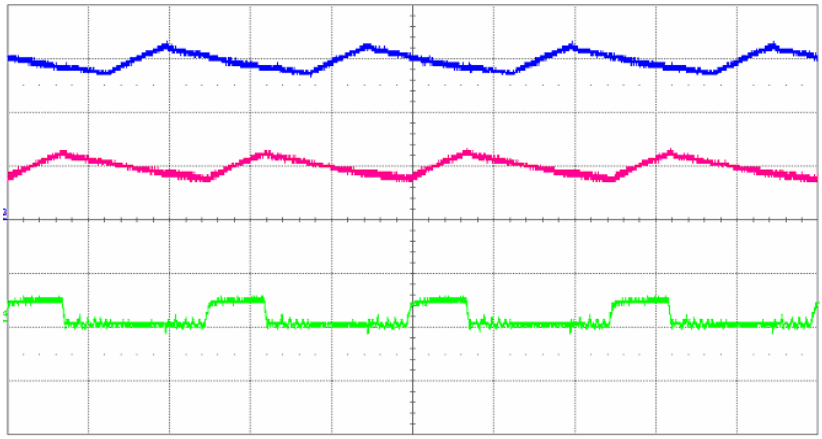


Figure 3.8 Symmetric HB dc-dc converter with asymmetric inductor DCR values without passive current sharing (top two traces: two inductor currents (5A/div); bottom trace: switch Vgs1 (20V/div)) (C_s shorted, asymmetric inductor DCRs with external 7.5m ohm resistor in series, $D_1 = D_2$ =30%, Io=20 A)

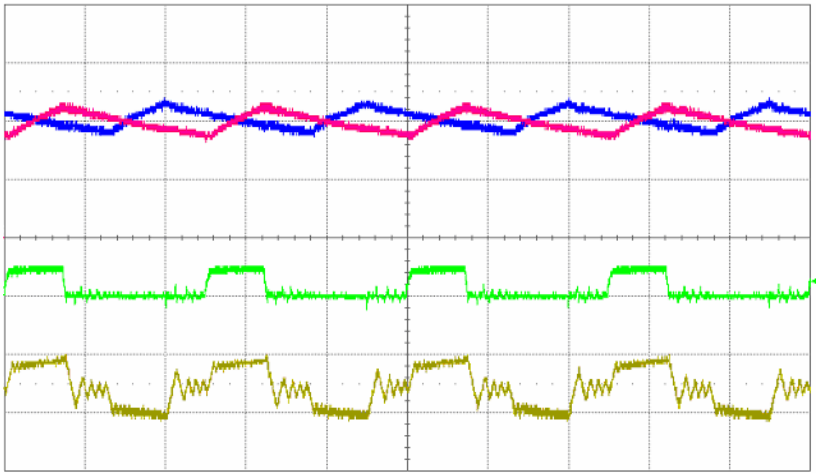
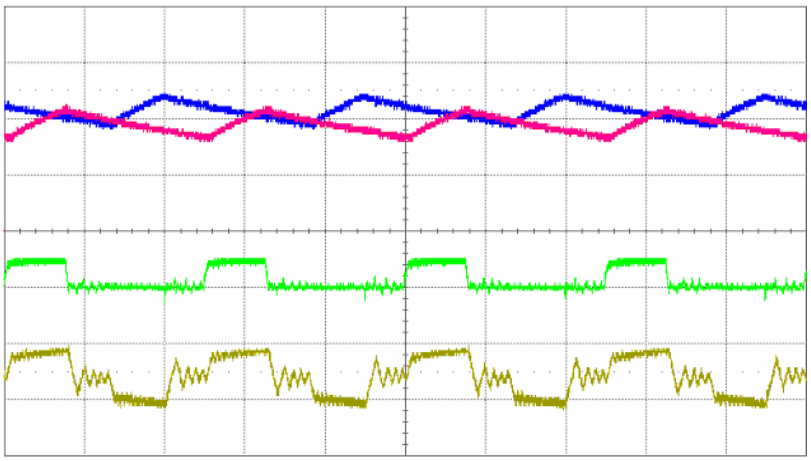
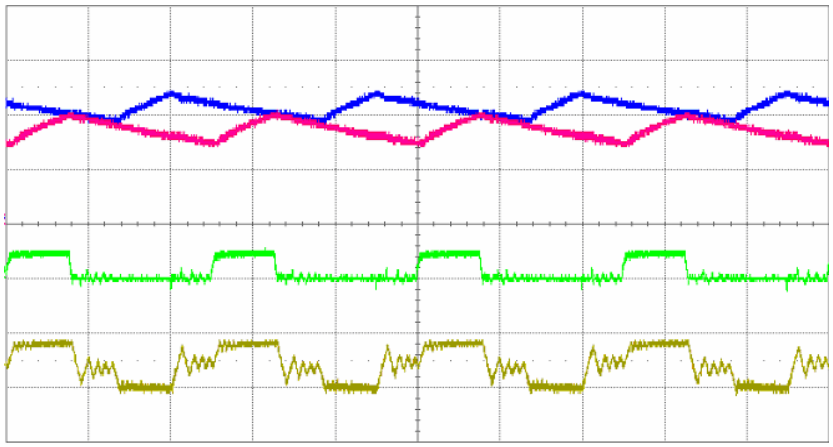


Figure 3.9 Proposed HB CDR dc-dc Converter (top traces: two inductor currents (5A/div); middle trace: switch Vds1 (20V/div); bottom trace: transformer primary current I_p (5A/div)); (C_s=8uF, asymmetric inductor DCRs with external 7.5m ohm resistor in series, $D_1 = D_2$ =30%, Io=20 A)



(a) With originally asymmetric inductor DCRs



(b) With intentionally asymmetric inductor DCRs

Figure 3.10. Proposed HB CDR dc-dc converter under asymmetric duty cycles (top traces: two inductor currents (5A/div); middle trace: switch Vgs1 (20V/div); bottom trace: transformer primary current I_p (5A/div)) (D_1 =28%, D_2 =32%, Io=20A)

An external capacitor of 8μF/10V is added in series with secondary side winding of transformer to verify the proposed HB CDR converter. Under symmetric duty cycle with external resistor of 7.5m ohm in series with L_1, the experimental waveforms are shown in Figure 3.9. It is seen that two inductor average currents are evenly balanced even with asymmetric inductor DCR values. Intentionally, asymmetric duty cycle signals are applied to the converter, and the experimental waveforms are shown in Figure.3.10. In Figure. 3.10(a), the inductor DCR values keep originally asymmetric; the two-phase currents are unequal due to asymmetric duty cycles. Keeping the same condition of asymmetric duty cycles, a 7.5 m Ohm resistor is placed in series with Inductor L_1, and the waveforms are shown in Figure. 3.10(b). It can be observed that the current sharing is not affected by the inductor DCR values, which agrees with (3-25) and (3-26). It should be noted that the voltage stress across Capacitor Cs is extremely low, which reduces capacitor ESR value and cost and allows practical applications of the modified converter in low voltage high current power conversion.

CHAPTER FOUR:
THE CURRENT TRIPLER RECTIFICATION TOPOLOGY

In high-performance microprocessor and telecommunication applications, the system operation speed and integration density continue to increase, resulting in a decrease in the required converter supply voltage while the supply current continuously increases due to the increasing power level requirement. Due to the limited real estate, high-current high-power-density power conversion is demanded for microprocessor and telecommunication applications. In general, conversion efficiency and thermal management are two restrictions against high power density. High switching frequency operation is an effective way to improve power density, and topologies featuring high efficiency at high switching frequency are desirable. In addition, topologies with even current and thermal stresses are demanded, especially for low voltage and high current applications.

Because secondary-side conduction loss dominates the overall power loss in isolated low-voltage high-current dc-dc converters [57-65], secondary-side topologies are desirable to have low conduction loss and well-distributed power dissipation to improve overall conversion efficiency and satisfy thermal management requirement. There are three conventional rectifier topologies for low voltage applications. In the forward rectifier (half wave rectifier), the rectifier has unidirectional utilization that causes the topology to have limited output current. For the center-tapped rectifier, the transformer utilization is bi-directional; however, a single output filter inductor is utilized to carry the whole load current. Therefore, the filter inductor suffers high current and thermal stresses for high current applications, resulting in bulky inductor size and inflexibility for footprint budget and PCB layout design. Moreover, the

transformer secondary windings are not efficiently utilized due to the fact that one of two tapped secondary windings conducts the full load current for half of the switching period [59-63]. Consequently, center-tapped rectifier is not well suited for high current applications.

In the current doubler rectification topology, there are two output filter inductors, and each carries only half of the load current. Compared with center-tapped rectifier, the copper loss in inductors is reduced and inductor magnetic design is simplified since each inductor carries half of the load current, which results in better thermal management and design flexibility. In addition, the transformer utilization is improved since the transformer secondary winding is utilized for bi-directional currents over the whole switching cycle and the transformer winding carries half of the load current [59-62], [65-66].

In this dissertation, a novel current tripler rectification topology is proposed for high current applications. An additional inductor is added in the current doubler rectifier to help share the load current, and each inductor carries only one-third of the load current. As a result, it has better power dissipation than the conventional center-tapped and current doubler topologies, leading to better thermal management and potentially improved power density. In addition, compared to the center-tapped rectifier, transformer secondary winding utilization is also improved and the transformer winding conduction loss is reduced.

The next section presents steady-state operation and dc analysis for the proposed topology. In section 4.2, major features are discussed and design considerations are presented in comparison with state-of-the-art rectification topologies. The concept of the proposed current tripler rectifier is extended to the current N-tupler rectifier in section 4.3. Section 4.4 shows experimental results and a conclusion is given in Section 4.5.

4.1 Proposed Rectification Topology

4.1.1. Current Tripler Rectification Topology

The proposed current tripler rectification (CTR) topology and the key steady-state operation waveforms are shown in Figure 4.1 and Figure 4.2, respectively. There are three output filter inductors and the transformer secondary side is center-tapped. Ignoring the leakage inductance and applying ac voltage pulse to the primary side of the transformer as shown in Figure 4.1. The primary ac voltage pulse can be generated by state-of-the-art topologies such as push-pull, half bridge and full bridge primary-side topologies.

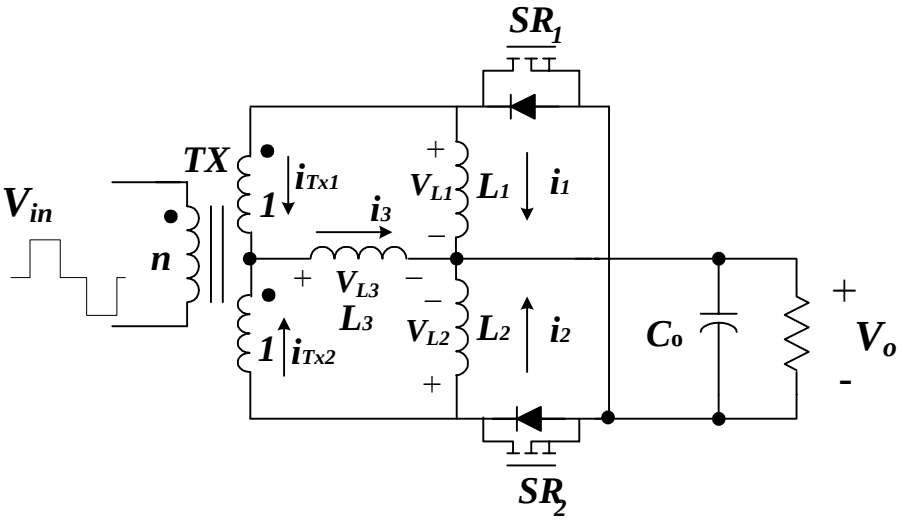


Figure 4.1. Proposed current tripler rectification topology

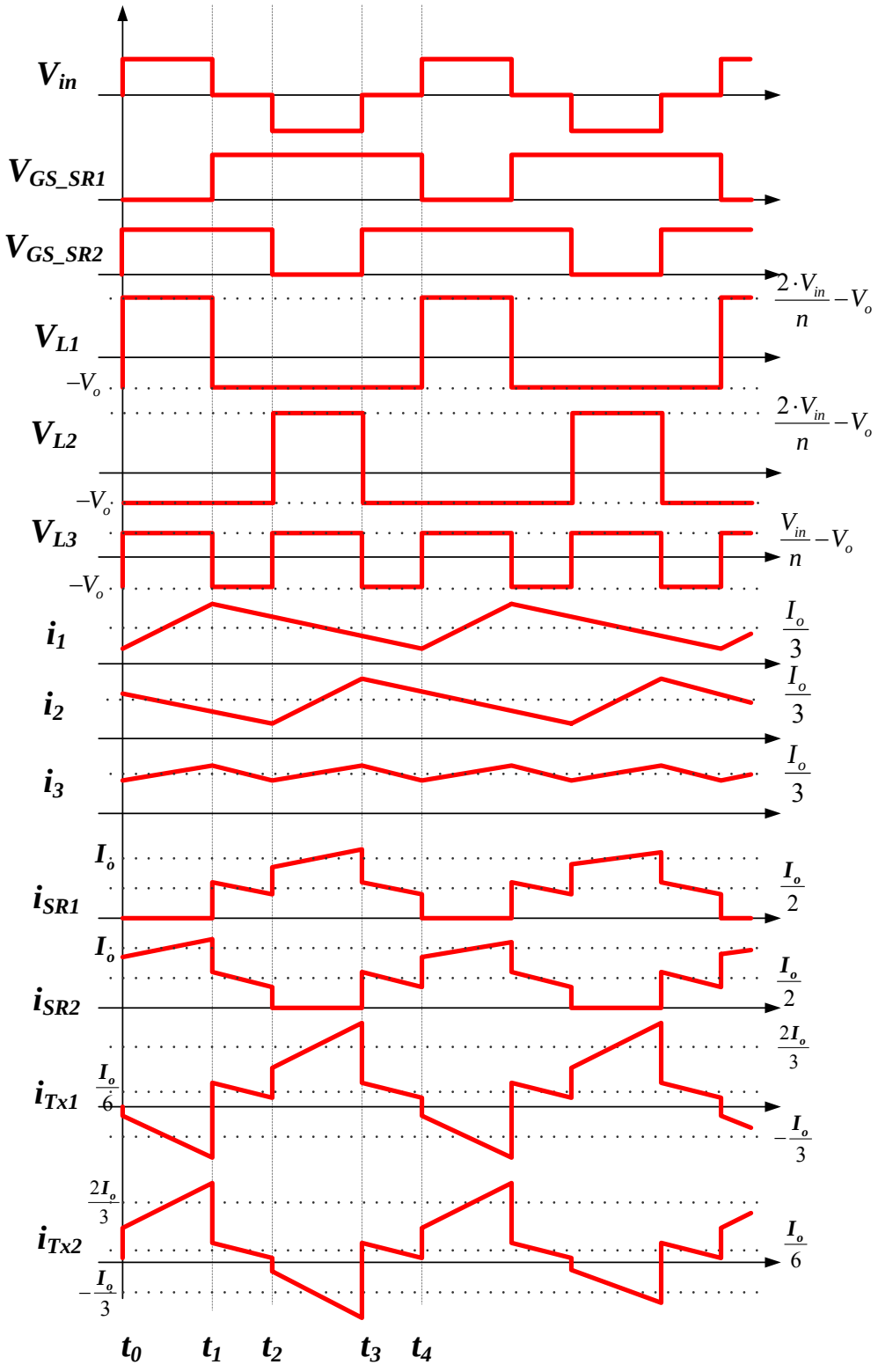


Figure 4.2. Key waveforms of steady-state operation

The transformer turns ratio is n: 1:1 as labeled, and according to volt-second balance across the inductors, the output voltage is obtained in terms of duty cycle and input voltage:

$$V_o = \frac{2 \cdot D \cdot V_{in}}{n} \qquad (0 \le D \le 0.5) \qquad (4\text{-}1)$$

where V_{in} is the input voltage, and D is the steady-state duty cycle value. The dc voltage gain of the above current tripler rectifier is the same for both the center-tapped and the current doubler rectification topologies. It can be seen, that removing either the inductor L_3, or removing both the inductors L_1 and L_2 from the proposed topology, these respective conventional topologies can be obtained.

Neglecting the inductor current ripple, each inductor's dc current is one-third of the load current:

$$I_1 = I_2 = I_3 = \frac{1}{3} I_o \qquad (4\text{-}2)$$

where I_o is the load current. This will be proven in Section 4.2. If the applied ac pulse is absolutely symmetrical, the dc bias of the transformer's magnetizing current is zero:

$$I_M = 0 \qquad (4\text{-}3)$$

4.1.2. Principle of Operation

The operation principle of the proposed current tripler rectifier can be described by four operation modes as shown in Figure 4.3, given that symmetrical ac pulse signal is applied to the primary side of the transformer. For this description of circuit operation, the following assumptions are made:

- The converter operates in steady state;
- Components are considered ideal except otherwise indicated;
- Leakage inductance L_k is neglected.

Mode 1 ($t_0 < t < t_1$): At t_0, the positive voltage V_{in} is applied to the primary side of the transformer. Switch SR_1 is turned off and SR_2 is on. The inductor L_1 is linearly charged by voltage ($\frac{2 \cdot V_{in}}{n} - V_o$), and in the inductor L_1 current i_1 linearly increases at the slope:

$$\frac{di_1}{dt} = \frac{\frac{2 \cdot V_{in}}{n} - V_o}{L_1} \tag{4-4}$$

where V_o is the output voltage and n is the transformer's turns ratio. The inductor L_3 is linearly charged by voltage difference between the reflected input voltage in the secondary side and the output voltage, and inductor current i_3 is increasing with the slope:

$$\frac{di_3}{dt} = \frac{\frac{V_{in}}{n} - V_o}{L_3} \tag{4-5}$$

During this interval, inductor L_2 is discharged by the output voltage V_o. The inductor current i_2 freewheels through output capacitor and SR_2, and decreases linearly at the following slope:

$$\frac{di_2}{dt} = -\frac{V_o}{L_2} \tag{4-6}$$

Mode 2 ($t_1 < t < t_2$): The transformer primary is shorted or opened according to the operation and control of the primary-side topology at t_1. Switches SR_1 and SR_2 are both on to provide freewheeling path for the three filter inductor currents. Three output inductors L_1, L_2 and L_3 are all linearly discharged by the output voltage V_o, and the three inductor currents

decrease at the same slope as follows:

$$\frac{di_1}{dt} = -\frac{V_o}{L_1} \tag{4-7}$$

$$\frac{di_2}{dt} = -\frac{V_o}{L_2} \tag{4-8}$$

$$\frac{di_3}{dt} = -\frac{V_o}{L_3} \tag{4-9}$$

Mode 3 ($t_2 < t < t_3$): At t_2, the negative voltage $-V_{in}$ is applied to the primary-side of the transformer. Switch SR_1 is on and SR_2 is turned off. The inductor L_1 is linearly discharged by the output voltage V_o, and the inductor L_1 current i_1 freewheels and decreases at the following slope:

$$\frac{di_1}{dt} = -\frac{V_o}{L_1} \tag{4-10}$$

The inductor L_2 is charged by the difference voltage ($\frac{2 \cdot V_{in}}{n} - V_o$), and the inductor current i_2 linearly increases at the slope:

$$\frac{di_2}{dt} = \frac{\frac{2 \cdot V_{in}}{n} - V_o}{L_2} \tag{4-11}$$

The inductor L_3 is linearly charged by the difference voltage ($\frac{V_{in}}{n} - V_o$), and i_3 increases with the slope:

$$\frac{di_3}{dt} = \frac{\frac{V_{in}}{n} - V_o}{L_3} \tag{4-12}$$

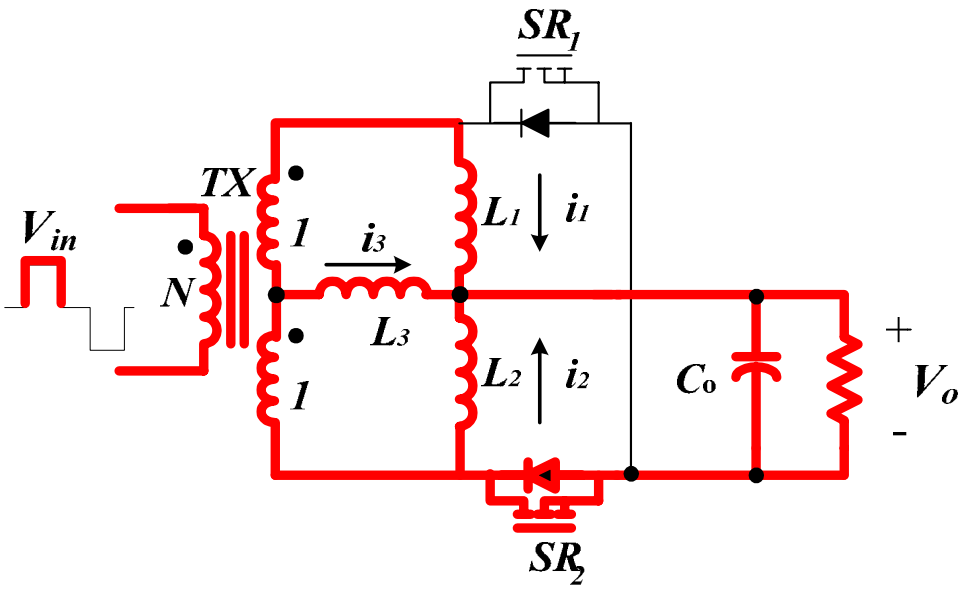
Mode 4 ($t_3 < t < t_4$): At t_3, the transformer primary side voltage becomes zero, and it repeats the same freewheeling mode as described in Mode 2 until the time instant t_4. The three inductor currents decrease with the same slope as:

$$\frac{di_1}{dt} = -\frac{V_o}{L_1} \tag{4-13}$$

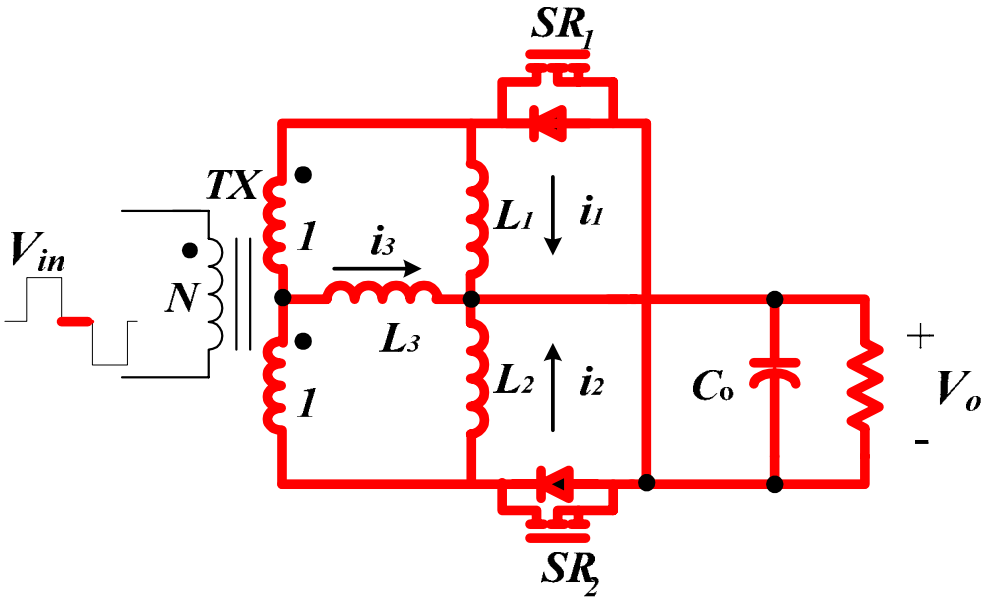
$$\frac{di_2}{dt} = -\frac{V_o}{L_2} \tag{4-14}$$

$$\frac{di_3}{dt} = -\frac{V_o}{L_3} \tag{4-15}$$

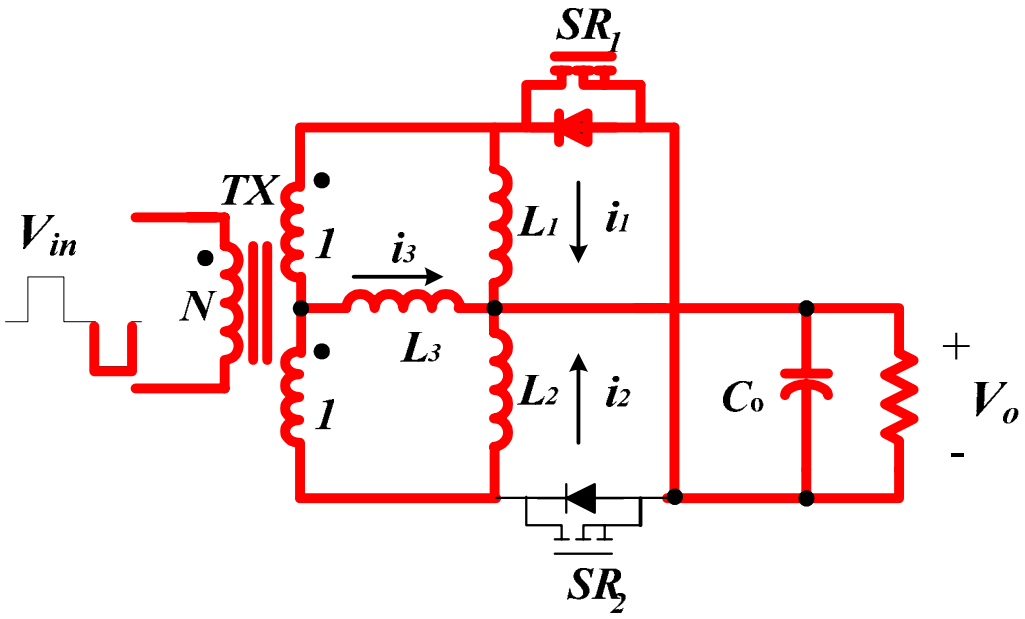
The operation mode goes back to Mode 1 after this mode, and a new switch cycle starts.


SR1
TX
Vin
N
1
i3
L3
L1
i1
L2
i2
Co
Vo
+
-
1
SR2

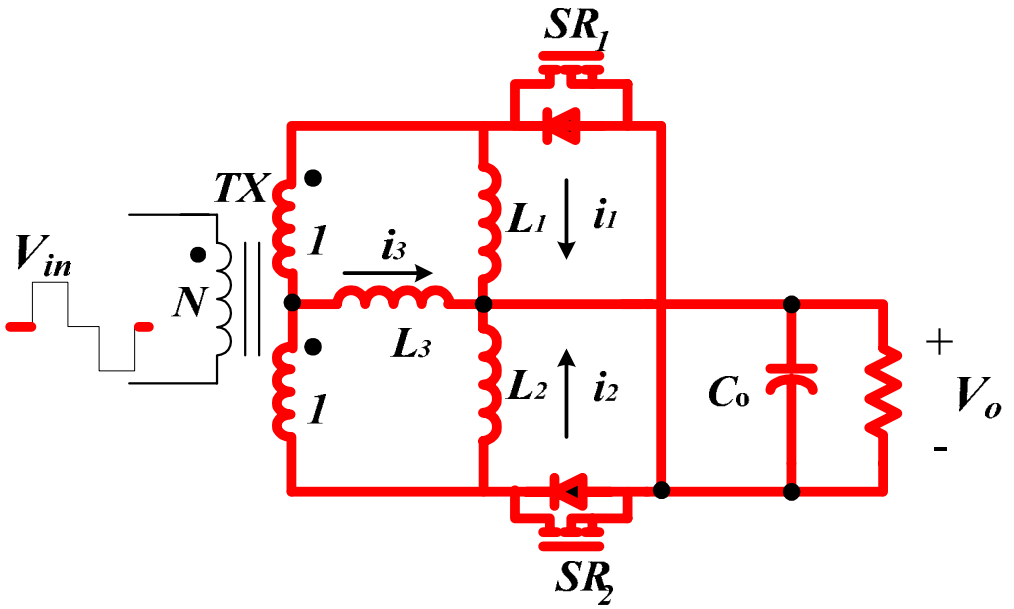
<Mode 1>


SR1
TX
Vin
N
1
i3
L3
L1
i1
L2
i2
Co
Vo
+
-
1
SR2

<Mode 2>



<Mode 3>



< Mode 4>

Figure 4.3. Equivalent circuits of operational modes

4.1.3. DC Analysis of the Proposed Topology

By applying the averaged state-space modeling method [67-69], the state-state dc analysis is presented for the design guidelines of the topology.

Before deriving the averaged state-space model, the following assumptions are made: the transformer leakage inductance is neglected, the transformer magnetizing inductance is referred to the primary-side, and the converter operates in CCM mode due to synchronous rectification. R_{SR1}, R_{SR2} are the on-resistance of the switches SR_1 and SR_2 respectively; R_{L1}, R_{L2} and R_{L3} are the DCR values of inductors L_1, L_2 and L_3 respectively; R_T is the dc resistance of the transformer windings, R_C is the ESR (Equivalent Series Resistance) of the output capacitor.

For each operation mode as described above and shown in Figure 4.3, there is a set of corresponding linear state space equations to represent it. Considering Mode 2 and Mode 4 to have the same state space representation, there are three sets of state space equations as expressed in (4-16), where x is the vector of state variables, u is the vector of independent sources that include input voltage and output current sources; A_1, B_1, A_2, B_2, A_3 and B_3 are respective system matrices for each of the three switched networks.

$$\dot{x} = A_m x + B_m u \quad (m = 1,2,3) \tag{4-16}$$

The state-space variables are defined as follows:

$$\boldsymbol{x} = \begin{bmatrix} \boldsymbol{i_M} & \boldsymbol{i}_1 & \boldsymbol{i}_2 & \boldsymbol{i}_3 & \boldsymbol{v_c} \end{bmatrix}^T;$$

$$\dot{x} = \begin{bmatrix} \frac{di_M}{dt} & \frac{di_1}{dt} & \frac{di_2}{dt} & \frac{di_3}{dt} & \frac{dv_C}{dt} \end{bmatrix}^T;$$

$$u = \begin{bmatrix} V_{in} & I_o \end{bmatrix}^T \tag{4-17}$$

The key concept in averaging the state-space model is the replacement of the above three sets of state-space equations by a single equivalent set [D11- D13]:

$$\dot{x} = Ax + Bu \tag{4-18}$$

where the equivalent matrices are defined by

$$A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3,$$

$$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3 \tag{4-19}$$

where, A_1, B_1 are state-space matrices of Mode 1; A_2 *and* B_2 are state-space matrices of Mode 3; A_3 *and* B_3 are state-space matrices of Mode 2 and Mode 4.; d_1 and d_2 are the duty cycle values of the primary positive and negative input pulse signal, respectively.

The steady-state solution, with dc values indicated by capital letters, is obtained by setting $\dot{x} = 0,$

$$X = -A^{-1}BU \tag{4-20}$$

Through (4-16) ~ (4-20), the steady-state dc quiescent points can be derived and the dc currents of magnetic components are:

$$I_M = \left(\frac{D_2 - D_1}{D_1 + D_2} \cdot \frac{R_{L1}R_{L2}}{R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3}} + \frac{D_2 R_{L1} - D_1 R_{L2}}{D_1 + D_2} \cdot \frac{2R_{L3}}{R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3}} \right) \cdot \frac{I_o}{n} \tag{4-21}$$

$$I_1 = \frac{R_{L2}R_{L3}}{R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3}} \cdot I_o \tag{4-22}$$

$$I_2 = \frac{R_{L1}R_{L3}}{R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3}} \cdot I_o \tag{4-23}$$

$$I_3 = \frac{R_{L1}R_{L2}}{R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3}} \cdot I_o \tag{4-24}$$

where I_o is the converter output current; D_1 and D_2 are the steady-state duty cycle values of d_1 and d_2, corresponding to the primary positive and negative pulses, respectively. It is noted that the current sharing depends on the inductor DCR values. If three inductors are designed to have identical inductance and DCR values, i.e., $R_{L1} = R_{L2} = R_{L3}$, (4-21) ~ (4-24) can be rewritten as follows:

$$I_M = \frac{D_2 - D_1}{D_1 + D_2} \cdot \frac{I_o}{n} \tag{4-25}$$

$$I_1 = \frac{1}{3} \cdot I_o \tag{4-26}$$

$$I_2 = \frac{1}{3} \cdot I_o \tag{4-27}$$

$$I_3 = \frac{1}{3} \cdot I_o \tag{4-28}$$

From (4-21) ~ (4-24), we may conclude:

[a] Transformer primary winding DCR, and the on-resistance of both primary-side and secondary-side switches have no effect on the dc current bias.

[b] Capacitance and inductance of the converter have no impact on the dc steady-state solutions. Actually, capacitance and inductance values only affect voltage and current ripples.

[c] When the three inductors have identical DCR values, each inductor carries one third of the load current, and even current distribution can be achieved.

4.2 Features and Design Considerations

4.2.1. Major Features and Comparison with Conventional Rectification Topologies

The proposed current tripler rectification topology can be used with double-ended primary-side topologies such as push-pull, half bridge and full bridge. There is no difference between the current tripler rectifier and the conventional center-tapped and current doubler rectifiers in terms of the control and operation of the primary-side topologies. In addition, the driving signals for the secondary-side synchronous rectifiers (SRs) are identical to those for the conventional center-tapped and current doubler rectifiers.

In the proposed topology, there are three output inductors evenly sharing the load current and thus the current stress is relieved in high current applications. As a result, the inductors design is simplified and better thermal management can be achieved.

A detailed comparison between the proposed topology and the conventional center-tapped and current-doubler rectifiers is shown in Table 4.1. For fair comparison, assume that three rectifiers operate with the same switching frequency and have the identical input and output voltages, as well as equal load currents and output ripple currents. Current values in Table 1 are not reflecting the effect of the ac components in the inductor currents for the purpose of simplicity.

From Table 4.1, it is noticed that the proposed current tripler rectifier has the same dc voltage gain as the center-tapped and current doubler rectifiers, and as a result, the steady-state duty cycle values are also identical. In addition, the rms current and voltage stress of synchronous rectifiers are identical. As mentioned above, the driving signals for the

synchronous rectifiers are also the same. Therefore, the design of the primary-side circuits, transformer and synchronous rectifiers are the same for the three compared rectification topologies.

The inductor currents in the proposed current tripler rectifier are only one-third of that in the center-tapped rectifier, while the individual inductor currents in the current doubler rectifier are half that of in the center-tapped rectifier. However, to achieve the same output ripple current, the filter inductance in the current doubler rectifier need to be doubled, and the filter inductance in the current tripler rectifier need to be tripled as shown in Table 4.1. One of the distinct features of the proposed current tripler rectifier is its better current distribution and possible lower power dissipation across the power train, which alleviates difficulties in thermal management and packaging for high current applications. This also leads to potentially increased power density.

Since the load current is evenly shared by three independent output inductors as shown in Table 1, the proposed topology has the lowest total inductor copper loss as compared with the center-tapped and the current doubler rectifier given identical dc resistance for each inductor. Another advantage of the proposed rectification technique is the simpler magnetic design for inductors because of the reduction in the inductor current.

Besides, the current tripler rectifier has better transformer utilization and lower transformer winding conduction loss than the center-tapped rectification in that the secondary winding in the proposed rectifier is used all over the switch cycle and only carries partial load current when conducting. As shown in Table 4.1, transformer secondary winding rms current in the current tripler rectifier is also lower than that in the center-tapped rectifier.

Also, the addition of the third inductor is a benefit to PCB layout design and power density improvement. Since the physical size of the magnetic core is proportional to the energy stored in it ($\frac{1}{2}I^2L$), the total volume of three inductors should be the same as that of the current doubler rectifier and the center-tapped rectifier. For discrete magnetics approach, the individual inductor size is reduced, which makes PCB layout design more flexible. Further converter size reduction can benefit from integrated magnetics and correspondingly increase the power density.

Therefore, compared to the center-tapped rectifier and the current doubler rectifier, the proposed current tripler topology has high current capability, well-distributed power dissipation and good thermal management for high current applications.

4.2.2. Design Considerations

As shown in (4-22) ~ (4-24), the analytic results show that the three inductor DCR values in the proposed rectification topology have effect on the current sharing. Inductor L_1 and L_2 should be designed to be identical in term of inductance and DCR values as in the current doubler rectifier. Although the optimal design is to keep three inductor DCR and inductance values identical, the inductor L_3 is allowed to have different inductance and DCR values from the inductor L_1 and L_2. In this case, the inductor current distribution can be analyzed. Figure 4.4 shows the current sharing under different R_{L3} value, where three inductor DCR values are assumed as $R_{L1} = R_{L2} = R_L$, $R_{L3} = (1 + \Delta R_{L3}\%) \cdot R_L$. Inductor current distribution can be

described as: $I_1\% = \frac{I_1}{I_o}$, $I_2\% = \frac{I_2}{I_o}$ and $I_3\% = \frac{I_3}{I_o}$. It is clear that the inductor L_1 and L_2 share identical current, and the inductor L_3 current depends on the DCR values. As shown in the Figure 4.4, when the inductor L_3 is designed identical to L_1 and L_2, three output inductors evenly share the load current. In practical design, the current distribution in three inductors is also affected if the secondary-side winding resistance of transformer is close to DCR values of output inductors.

According to the steady-state analysis results aforementioned, the inductance value of the three output inductors has no effect on the current sharing, and it only affects the current ripple as shown in (4-29) ~ (4-31). From Figure 4.2, it is shown that inductor currents of L_1 and L_2 are interleaved with 180^o phase difference with the current ripples at the switching frequency; while the third inductor L_3 operates at twice the switching frequency. As a result, the inductance values of three output inductors don not have to be identical. However, for optimal design and good circuit symmetry, the inductance value of L_1 and L_2 are suggested to be equal, and a different inductance value can be selected for L_3 to meet the total output current ripple requirement while current sharing can still be achieved. Individual inductor current ripples are shown as follows:

$$\Delta I_{1_{P-P}} = \frac{V_o}{L_1} \cdot (1-D) \cdot T \tag{4-29}$$

$$\Delta I_{2_{P-P}} = \frac{V_o}{L_2} \cdot (1-D) \cdot T \tag{4-30}$$

$$\Delta I_{3_{P-P}} = \frac{V_o}{2 \cdot L_3} \cdot (1-2 \cdot D) \cdot T \tag{4-31}$$

where $\Delta I_{1_{P-P}}$, $\Delta I_{2_{P-P}}$, $\Delta I_{3_{P-P}}$ are the peak-to-peak current ripple values of inductor L_1, L_2 and

L_3 respectively, T is the switching period, and D is the steady-state duty cycle value. The total output current ripple ΔI_{p-p} in terms of three inductance values is:

$$\Delta I_{p-p} = \frac{V_o \cdot T \cdot (1-2 \cdot D)}{2} \cdot (\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}) \tag{4-32}$$

To achieve the same output current ripple as those in the center-tapped and the current doubler rectifiers, the three output inductors can be selected in many ways. One option is to design each inductor to have an identical inductance value, i.e., $L_1 = L_2 = L_3 = 3L$ (L is the output inductance value of the center-tapped rectifier). The total output current ripples for the three rectification topologies are shown in Table 4.1.

The inductor peak current, which is the addition of the inductor dc current and half of the peak-to-peak current ripple, is used to design the inductor. In the optimally designed current tripler rectifier, the three inductors peak currents are presented in (4-33) ~ (4-35).

$$I_{1_{peak}} = \frac{1}{3} \cdot I_o + \frac{V_o}{2 \cdot L_1} \cdot (1-D) \cdot T \tag{4-33}$$

$$I_{2_{peak}} = \frac{1}{3} \cdot I_o + \frac{V_o}{2 \cdot L_2} \cdot (1-D) \cdot T \tag{4-34}$$

$$I_{3_{peak}} = \frac{1}{3} \cdot I_o + \frac{V_o}{4 \cdot L_3} \cdot (1-2 \cdot D) \cdot T \tag{4-35}$$

where $I_{1_{peak}}$, $I_{2_{peak}}$, $I_{3_{peak}}$ are peak current values of inductor L_1, L_2 and L_3 respectively.

Equation (4-25) shows that if the transformer primary side ac signal is symmetrical (i.e., D_1=D_2) and the circuitry is optimized to be symmetrical ($R_{L1} = R_{L2}$), there's no dc bias in the transformer magnetizing current. Otherwise, dc bias of magnetizing current exists and should

be estimated based on (4-21) when designing the transformer.

Considering the proposed topology is more desirable for low voltage and higher current application where the synchronous rectifiers (SRs) are utilized, only continuous conduction mode (CCM) exists due to bi-directional conduction of SRs in this case. All the above analysis and design are based on this assumption.

In some applications where synchronous rectification technique is not applied, the three output inductor currents can become discontinuous and the converter operates in discontinuous mode (DCM). In the boundary between CCM and DCM where inductor currents become zero at the end of switching cycle, the inductor peak to peak current ripple is two times that of inductor dc current:

$$\Delta I_{L_{P-P}} = 2 \cdot I_L \tag{4-36}$$

Based on the dc analysis result of section II as shown in (4-22) ~ (4-24) and individual current ripple values in (4-29) ~ (4-31), the critical inductance value can be derived in (4-37) ~ (4-39) in order to maintain CCM which is assumed throughout the analysis.

$$L_{1crit} = \frac{V_{in} \cdot D \cdot (1-D) \cdot (R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3})}{n \cdot R_{L2} \cdot R_{L3} \cdot f \cdot I_o} \tag{4-37}$$

$$L_{2crit} = \frac{V_{in} \cdot D \cdot (1-D) \cdot (R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3})}{n \cdot R_{L1} \cdot R_{L3} \cdot f \cdot I_o} \tag{4-38}$$

$$L_{3crit} = \frac{V_{in} \cdot D \cdot (\frac{1}{2} - D) \cdot (R_{L1}R_{L2} + R_{L1}R_{L3} + R_{L2}R_{L3})}{n \cdot R_{L1} \cdot R_{L2} \cdot f \cdot I_o} \tag{4-39}$$

where f is the converter switching frequency; D is the steady-state duty cycle value of d_1 and d_2 corresponding to the primary positive and negative pulses, respectively.

If output inductor design is optimized to have identical inductance and DCR values, i.e., $R_{L1} = R_{L2} = R_{L3}$, (4-37) ~ (4-39) can be further simplified as follows:

$$L_{1crit} = \frac{3 \cdot V_{in} \cdot D \cdot (1-D)}{n \cdot f \cdot I_o} \tag{4-40}$$

$$L_{2crit} = \frac{3 \cdot V_{in} \cdot D \cdot (1-D)}{n \cdot f \cdot I_o} \tag{4-41}$$

$$L_{3crit} = \frac{3 \cdot V_{in} \cdot D \cdot (\frac{1}{2}-D)}{n \cdot f \cdot I_o} \tag{4-42}$$

4.3 Derivative Topologies

The proposed current tripler rectification concept can be extended to the current quadrupler rectifier topology as shown in Figure 4.5. Figure 4.6 shows the current quadrupler rectifier's key waveforms for steady-state operation. The operation modes can be analyzed under the same assumptions aforementioned. At t_0, the positive voltage V_{in} is applied to the primary side of transformer. Switch SR_1 is turned off and SR_2 is on. The inductor L_1, L_3 and L_4 are linearly charged; inductor L_2 is discharged by the output voltage V_o. The transformer primary is shorted or opened according to the operation and control of the primary-side topology at t_1. Switches SR_1 and SR_2 are both on to provide freewheeling path for the four filter inductor currents. Three output inductors L_1, L_2, L_3 and L_4 are all linearly discharged by the output voltage V_o. At t_2, the negative voltage $-V_{in}$ is applied to the primary-side of the transformer. Switch SR_1 is on and SR_2 is turned off. The inductor L_2, L_3 and L_4 are linearly charged while inductor L_1 is discharged by the output voltage V_o. At t_3, the transformer primary

side voltage becomes zero, and it repeats the same freewheeling mode as described in Mode 2 until the time instant t_4. The operation mode goes back to Mode 1 after this mode, and a new switch cycle starts.

Like the current tripler rectifer, it is observed that the four individual inductors evenly share the load current and the transformer secondary side winding carries partial load current in the current quadrupler rectifier. So it has even higher current capability and better thermal management than the current tripler topology. Since each inductor current is only one-fourth of load current, the inductor magnetic design is further simplified than that in the current tripler rectifier. However, the transformer design is more complex since there are three secondary windings. As a result, there is always a trade-off in selection of rectifier topologies.

In general, the proposed current tripler rectification concept can be extended to the current N-tupler rectifier as shown in Figure 4.7. There are (N-1) transformer secondary-side windings and N inductors in the current N-tupler rectification topology. Each inductor evenly shares $\frac{1}{N}$ load current, leading to more evenly distributed power dissipation over the power train and therefore easier power management. As a matter of fact, current doubler and current tripler rectifiers are particular examples of the current N-tupler topologies where N is two and three, respectively.

Similar to the current tripler rectifier, the inductor magnetic design is simplified due to the reduction of the dc bias current. Besides, it still has the same control and operation of primary side topology as conventional current doubler rectifier without any complexity increase in driving circuitry for SRs. However, the current N-tupler rectifier becomes impractical for higher current output when N is larger than four because there are too many

filter inductors and secondary-side windings for the transformer resulting in complicated transformer structure as shown in Figure 4.7.

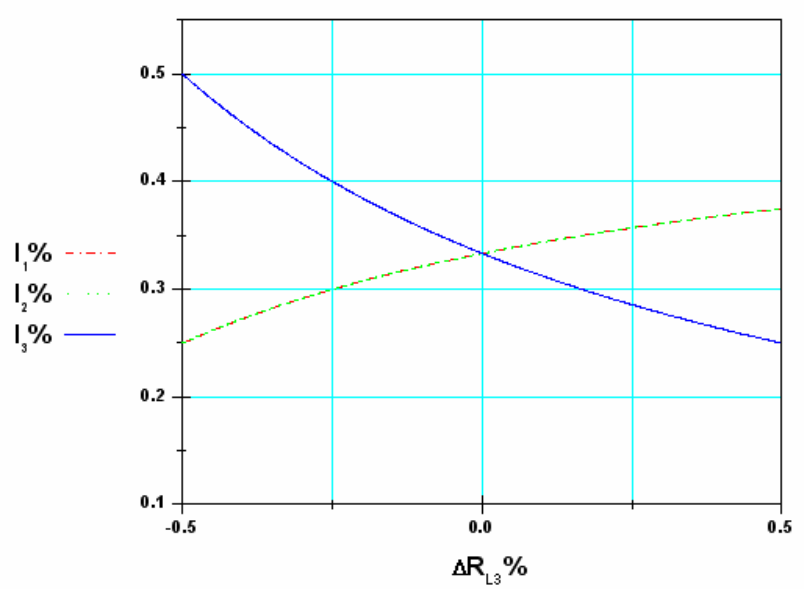


Figure 4.4. Inductor current sharing under different inductor DCR values

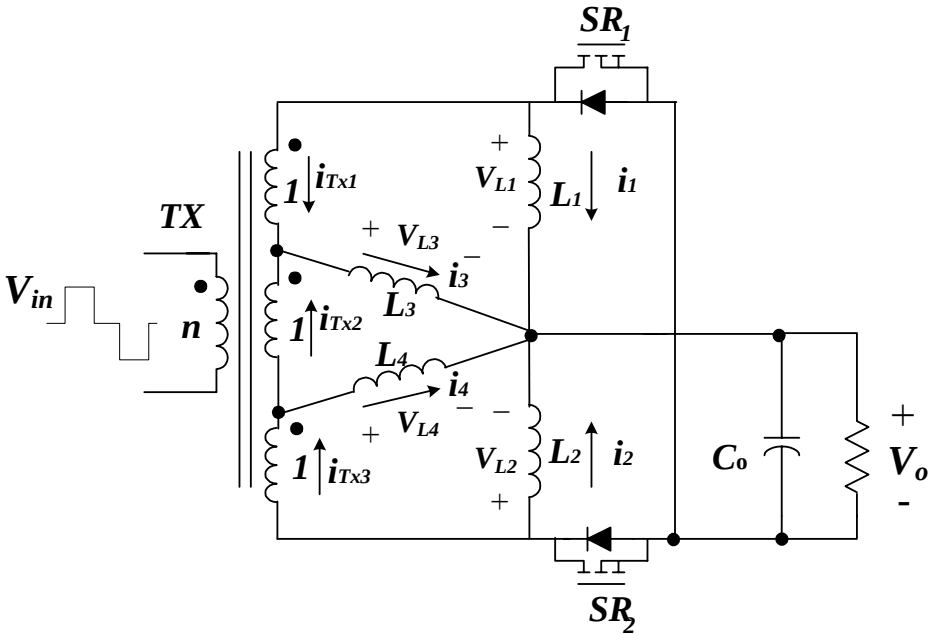


Figure 4.5. Current quadrupler topology

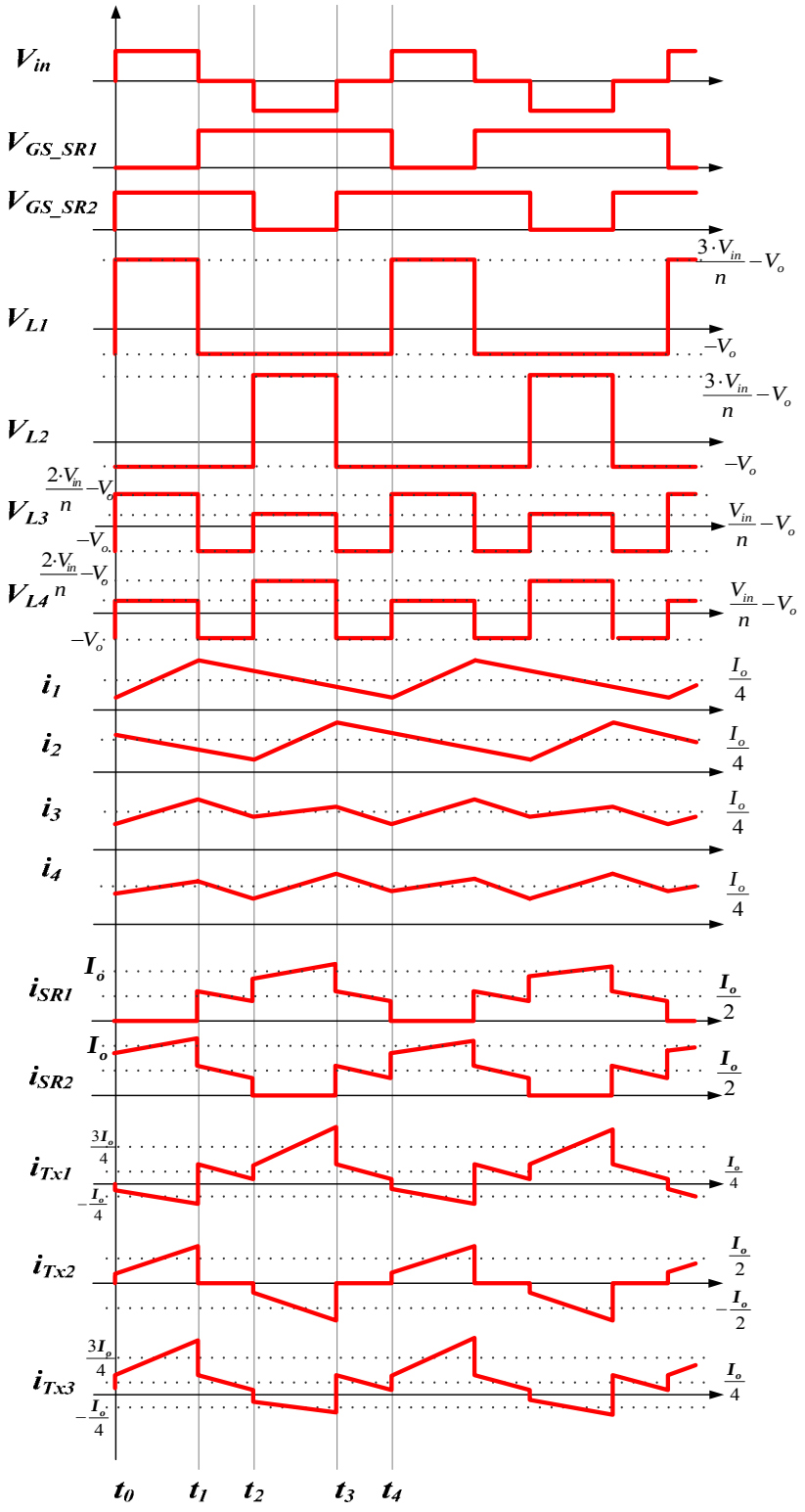


Figure 4.6. Key operation waveforms of current quadrupler topology

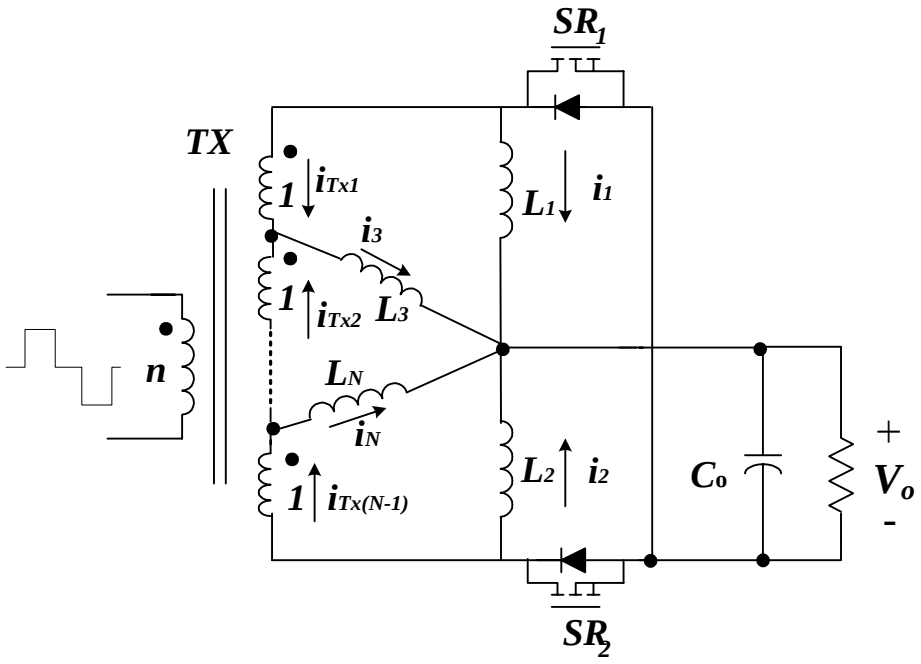


Figure 4.7. Current N-tupler topology

4.4 Experimental Results

An experimental prototype of the symmetrical half bridge dc-dc converter with the proposed current tripler rectifier is built as shown in Figure 4.8 with the nominal input voltage 48V, output voltage 1.2V, and maximum load current of 45A. In the prototype, Si7456 is used for two main switches S_1 and S_2 of the primary-side half bridge converter, and Si7868 is used for the secondary-side synchronous rectifier SR_1 and SR_2, two in parallel each side. Core ER14.5/3F3 is selected as the planar transformer with turns ratio of 12:1:1. The converter runs at the switching frequency of 211 kHz. Each output inductor has an inductance value of 0.8 μH and DCR value of 0.588 mΩ.

The experimental waveforms of the proposed topology are shown in Figure 4.9, and it is observed that the load current is evenly distributed in the three inductors. Removing the inductor L_3 from the proposed topology, the converter becomes the conventional half bridge dc-dc converter with the current doubler synchronous rectifier. Figure 4.10 compares the efficiency curves between the proposed CTR rectifier and the conventional current doubler rectifier at V_{in}= 48V, which are measured with the same primary-side half bridge dc-dc converter respectively. It can be noticed that the current triper rectifier achieves up to 1.5% efficiency improvement over the current doubler rectifier at 45A load, which verifies that the proposed topology is advantageous over the conventional current doubler rectifier. Noting that the efficiency improvement increases with the load current in Figure 4.10, it verifies that the proposed current tripler rectifier is more suitable for high current applications than the current doubler rectifier and significant efficiency improvement is expected for higher output current.

4.5 Conclusions

In this chapter a novel current tripler rectification topology is proposed for high current applications. Theoretical analysis, comparison and experimental results verify that the proposed rectification technique has good thermal management and well-distributed power dissipation, simplified magnetic design and low copper loss for inductors and transformer due to the fact that the load current is better distributed in three inductors and the rms current in transformer windings is reduced. Therefore, the proposed current tripler rectifier is a good candidate topology for secondary-side rectification for high current isolated dc-dc converters.

Figure 4.8. Experimental prototype

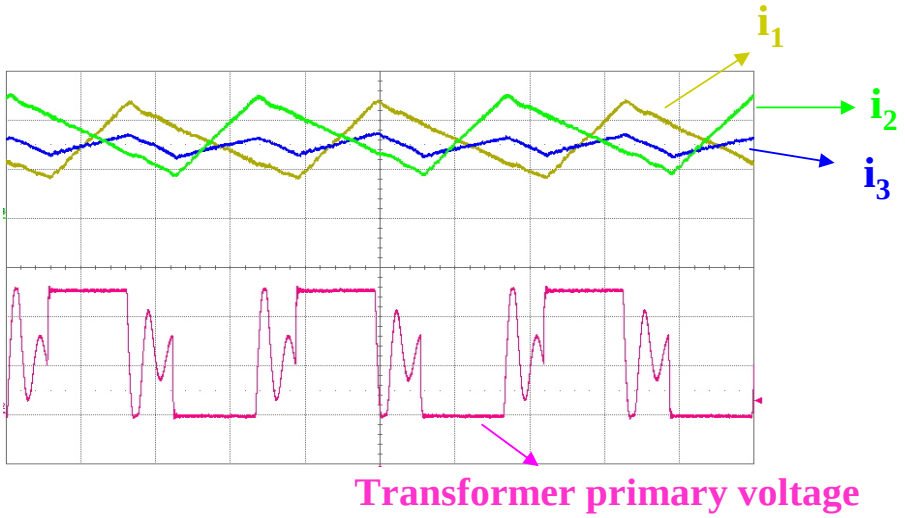


Figure 4.9. Experimental waveforms for Vin =48V, Io=10A (Top three traces: inductor currents (2A/div); bottom trace: transformer primary voltage (20V/div))

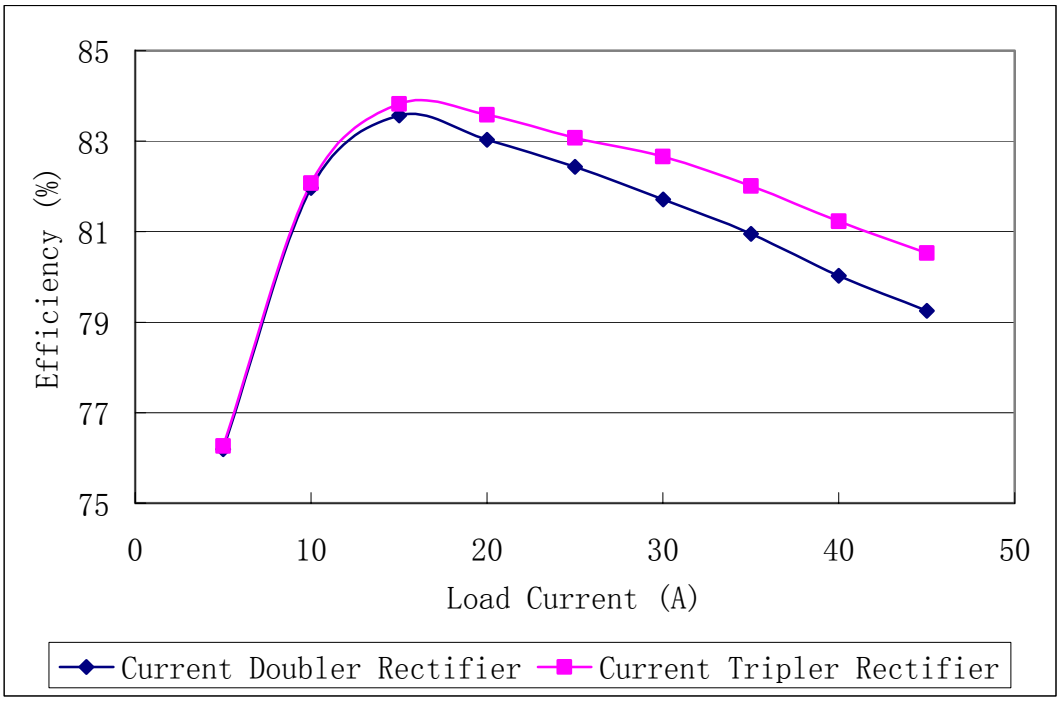


Figure 4.10. Efficiency comparison for Vin =48V.

Table 4-1. Current tripler rectifier comparison with center-tapped and current doubler rectifiers

Rectifier Topology	**Center-tapped Rectifier**	**Current Doubler Rectifier**		**Current Tripler Rectifier**		
DC Voltage Gain	$\frac{2}{N}\cdot D$	$\frac{2}{N}\cdot D$		$\frac{2}{N}\cdot D$		
Transformer Secondary Winding RMS Current	$\sqrt{\frac{1}{4}+\frac{D}{2}}\cdot I_o$	$\sqrt{\frac{D}{2}}\cdot I_o$		$\sqrt{\frac{1}{36}+\frac{D}{2}}\cdot I_o$		
SR Voltage Stress	$\frac{V_{in}}{N}\cdot 2$	$\frac{V_{in}}{N}\cdot 2$		$\frac{V_{in}}{N}\cdot 2$		
SR RMS Current	$\sqrt{\frac{1}{4}+\frac{D}{2}}\cdot I_o$	$\sqrt{\frac{1}{4}+\frac{D}{2}}\cdot I_o$		$\sqrt{\frac{1}{4}+\frac{D}{2}}\cdot I_o$		
Inductor DC Current	L	L_1	L_2	L_1	L_2	L_3
	I_o	$\frac{I_o}{2}$	$\frac{I_o}{2}$	$\frac{I_o}{3}$	$\frac{I_o}{3}$	$\frac{I_o}{3}$
Inductance Values For Identical output current ripples	$L_{Cent-tapped}=L$	$L_{CDR}=2L$	$L_{CDR}=2L$	$L_{CTR}=3L^{**}$	$L_{CTR}=3L^{**}$	$L_{CTR}=3L^{**}$
Total Inductor Copper Loss*	$I_o^2\cdot R_L$	$\frac{1}{2}\cdot I_o^2\cdot R_L$		$\frac{1}{3}\cdot I_o^2\cdot R_L$		
Total Output Current Ripple	$\frac{V_o\cdot T\cdot(1-2\cdot D)}{2}\cdot\frac{1}{L}$	$\frac{V_o\cdot T\cdot(1-2\cdot D)}{2}\cdot(\frac{1}{L_1}+\frac{1}{L_2})$ $(\frac{V_o\cdot T\cdot(1-2\cdot D)}{2}\cdot\frac{1}{L},\ for\ L_1=L_2=2L)$		$\frac{V_o\cdot T\cdot(1-2\cdot D)}{2}\cdot(\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3})$ $(\frac{V_o\cdot T\cdot(1-2\cdot D)}{2}\cdot\frac{1}{L},\ for\ L_1=L_2=L_3=3L)$		
Individual Inductor Current Ripple	L	L_1	L_2	L_1	L_2	L_3
	$\frac{V_o}{2\cdot L}\cdot(1-2\cdot D)\cdot T$	$\frac{V_o}{L_1}\cdot(1-D)\cdot T$	$\frac{V_o}{L_2}\cdot(1-D)\cdot T$	$\frac{V_o}{L_1}\cdot(1-D)\cdot T$	$\frac{V_o}{L_2}\cdot(1-D)\cdot T$	$\frac{V_o}{2\cdot L_3}\cdot(1-2\cdot D)\cdot T$

* *Given the DCR value of each inductor is R_L.*

** *Various sets of inductance values can be selected for identical output current ripples.*

CHAPTER FIVE: HIGH-EFFICIENCY ISOLATED DC-DC CONVERTERS WITH FAST TRANSIENT RESPONSE

There are many classifications for dc-dc converters, for example, it can be classified as non-isolated and isolated converters depending on whether there's dielectric isolation between the input power and output power, where a high-frequency transformer is used for such isolation. Based on the location of the PWM controller, the isolated dc-dc converters can be divided into two categories: primary-side controlled power converters and secondary-side controlled power converters. If the controller is in the primary side of converter, this converter is called primary-side controlled converter; if the PWM converter have the common ground with secondary-side circuitry, the converter is defined as secondary-side controlled power converter.

The primary-side control is a popular approach in industry due to its simplicity and low cost as well as long-time design experience. But as technologies advances, especially in microcomputer and computing system applications, fast transient response is demanded with high efficiency power conversion. In such applications requiring fast transient response, secondary-side controlled power converters are gaining popularity over their primary-side controlled counterparts, since no opto-coupler is introduced into the feedback control loop for secondary-side control, and thus higher system bandwidth and fast transient response can be achieved[70-71]. However, start-up is a key issue for applying secondary-side control and extra circuitry is needed to provide a bias voltage for secondary-side PWM controller during the start-up process. This chapter will discuss a high-efficiency dc-dc converter with secondary-side control for fast transient response requirement and a novel topology which can be a solution for the start-up issue is presented in the Chapter 6.

5.1 Demo Y Topology and Operation

Figure. 5.1 shows the active-clamp half-bridge dc-dc converter with current doubler rectification and its key steady-state operation waveforms is shown in Figure. 5.2 [72]. Capacitor C_{j1}, C_{j2}, C_{j3} and C_{j4} are the junction capacitors of MOSFET S_1, S_2, S_3 and S_4 respectively; L_k is the leakage inductance of the transformer. All components are ideal unless otherwise indicated.

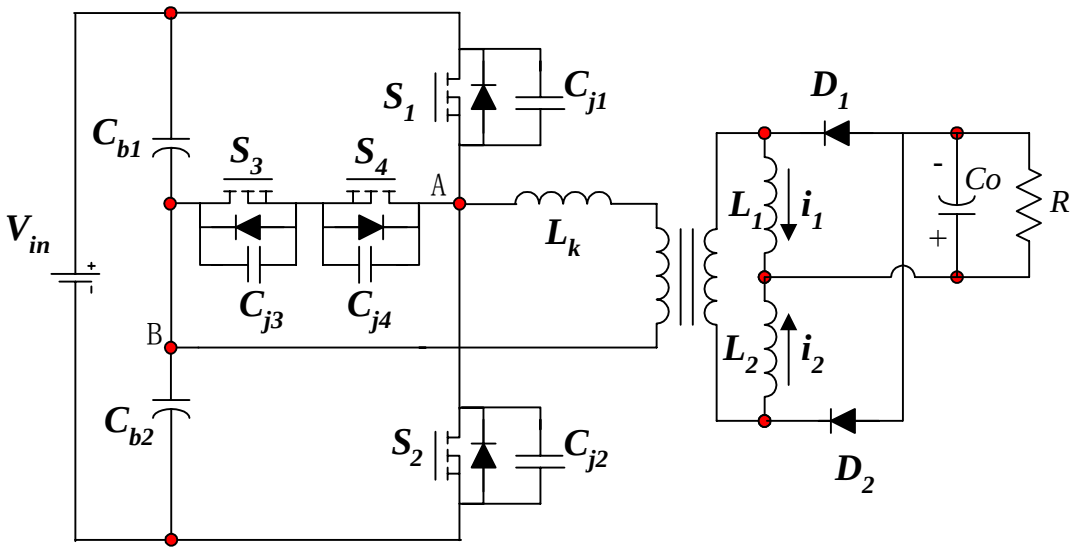


Figure 5.1 The active-clamp half-bridge dc-dc converter with current doubler rectifier.

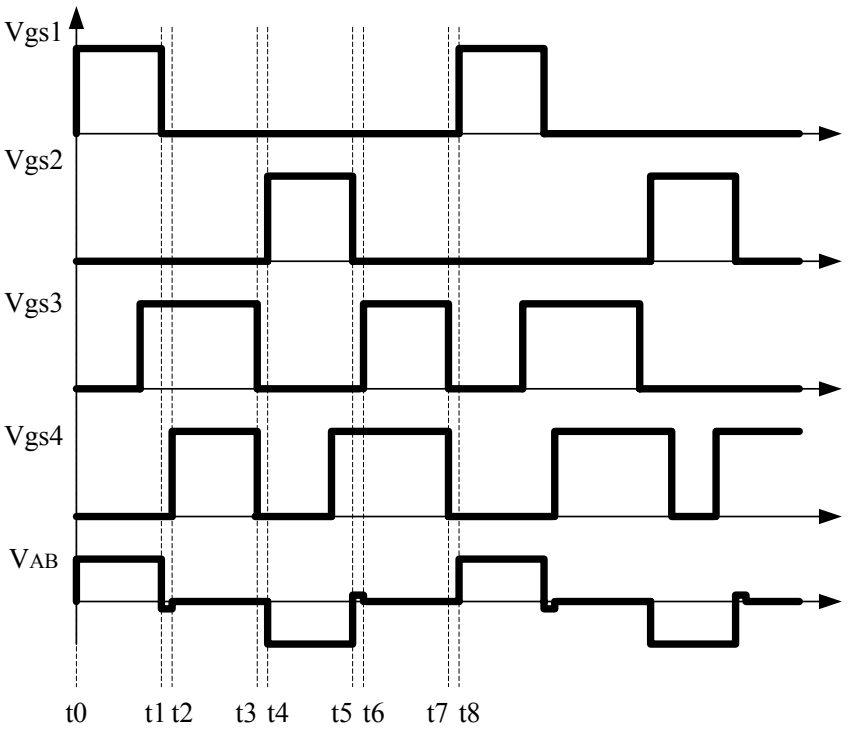


Figure 5.2 Key operation waveforms for the proposed active-clamp half-bridge with current doubler rectifier.

The operation modes analysis can be descried by eight modes as follows and the main equivalent operation modes are shown in Figure. 5.3:

Mode 1 *($t_1 < t < t_2$):* Initially, it is assumed that S_1 was conducting and S_3 was turned on with Zero-Current-Switching (ZCS). At $t = t_1$, S_1 is turned off, causing the primary current i_p to charge the junction capacitance C_{j1} and discharge C_{j2}. When the voltage across C_{j1} is charged to half of input voltage V_{in}, the leakage inductance current will flow through S_3 and the body diode of S_4 creating the ZVS condition for S4 to be turned on. Since leakage current does not flow through junction capacitor Cj1 and Cj2 after they are charged/discharge to 1/2Vin, the ringings, which is normally found in conventional half-bridge topology, are not presented in the proposed circuit due to the clamping of S3

and S4 branch. Considering the fact that the transformer is shorted, the leakage current continues to freewheel.

Mode 2 *(t2<t<t3):* At t2, S4 is turned on with ZVS. Since the transformer is shorted and the voltage across S3 and S4 is negligible, the leakage current keeps freewheeling through S3, S4 and the transformer primary winding.

Mode 3 *(t3<t<t4):* At t3, both MOSFETs are off, the current through leakage inductor begins to charge Cj1, Cj3 and Cj4 and discharge Cj2. When Vds of S2 drops to zero, the body diode of S2 conduct carrying all the leakage current and charging for Cj1, Cj3 and Cj4 is finished. The current though leakage inductor should be big enough so that voltage across S2 is able to drop to zero to obtain ZVS condition for S2 to be turned on.

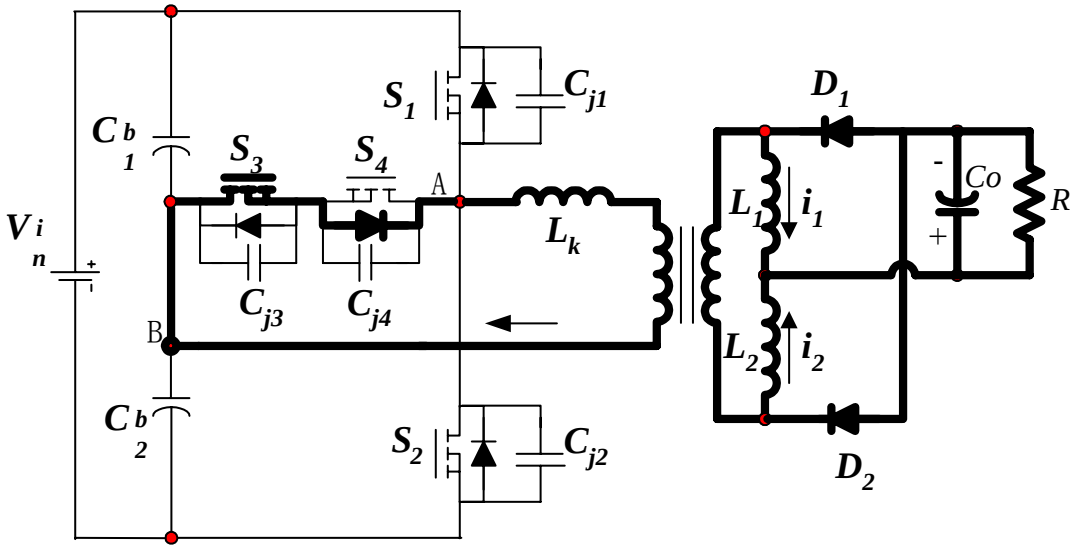
Mode 4 *(t4<t<t5):* At t4, S2 is turned on with ZVS. Power is delivered from primary side to secondary side.

Mode 5 *(t5<t<t6):* Prior to t5, S4 is turned on with ZCS. At t5, S2 is turned off. Similarly, Cj1 and Cj2 is discharged and charged respectively so that Vds of S2 rise to 1/2Vin. Then the leakage current flows through S4, body diode of S3 and transformer. As a result, the ringings are eliminated since no current flows through junction capacitor of the power MOSFET S1 and S2

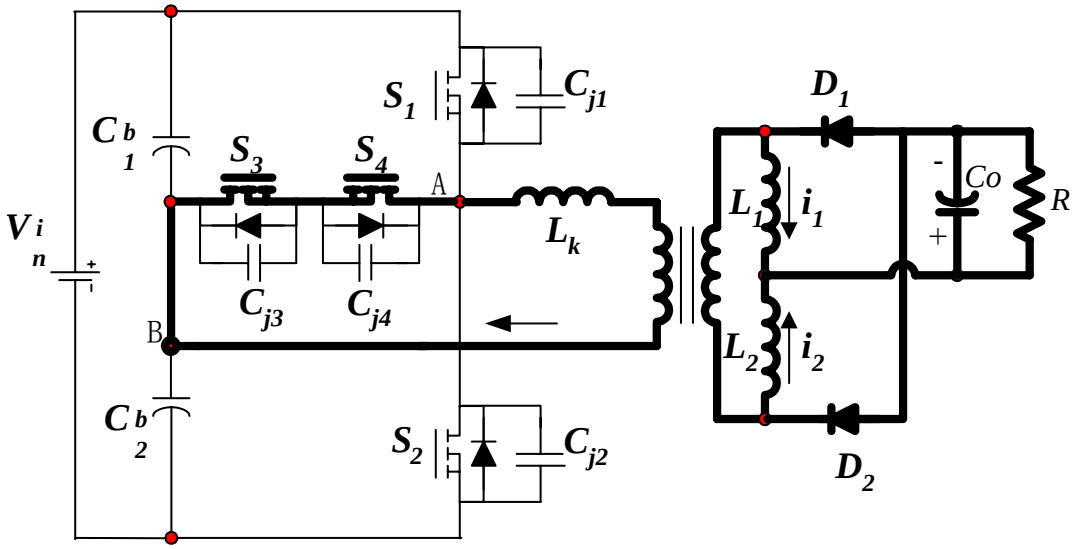
Mode 6 *(t6<t<t7):* This mode is similar with Mode 2. The leakage current keeps freewheeling through S3, S4 and transformer primary winding.

Mode 7 *(t7<t<t8):* At t7, both S3 and S4 are turned off, the leakage current charge/discharge S2 and S1.

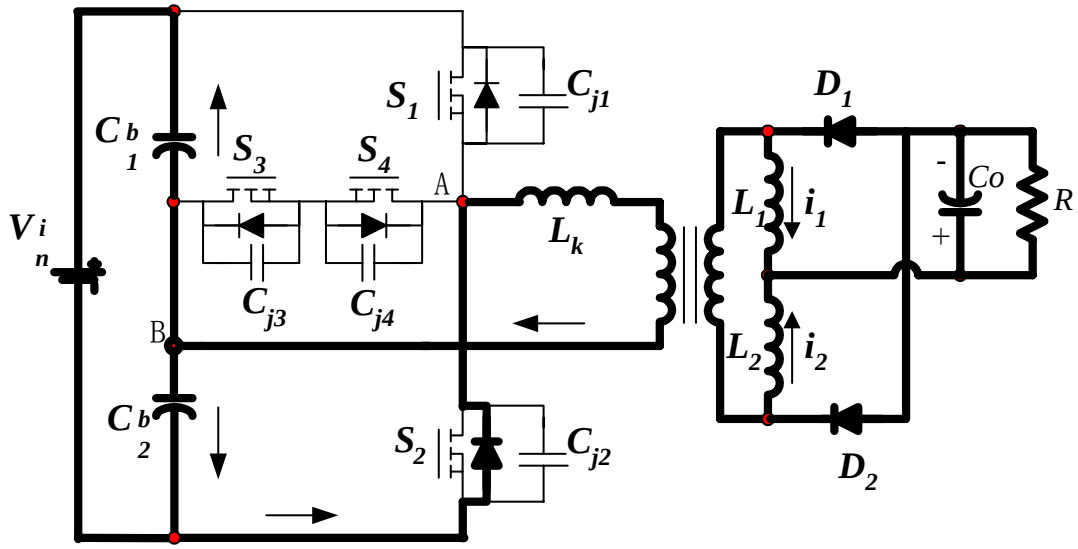
Mode 8 *(t8<t<t1):* At t8, S1 is turned on with ZVS. The converter delivers power from the primary side to the secondary side. One whole switching period is finished.


Vin
Cb1
Cb2
S1
S2
S3
S4
Cj1
Cj2
Cj3
Cj4
A
B
Lk
D1
D2
L1
L2
i1
i2
Co
R

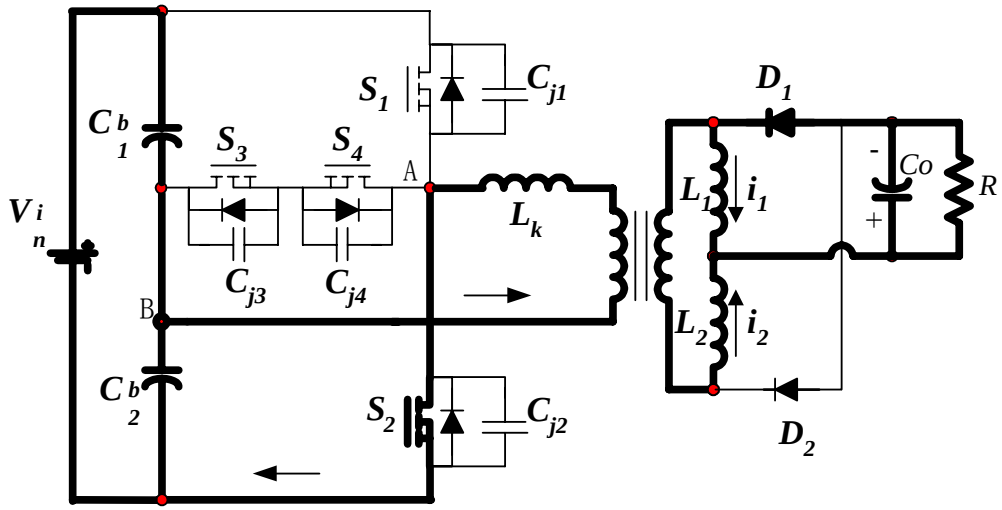
<Mode 1>


Vin
Cb1
Cb2
S1
S2
S3
S4
Cj1
Cj2
Cj3
Cj4
A
B
Lk
D1
D2
L1
L2
i1
i2
Co
R

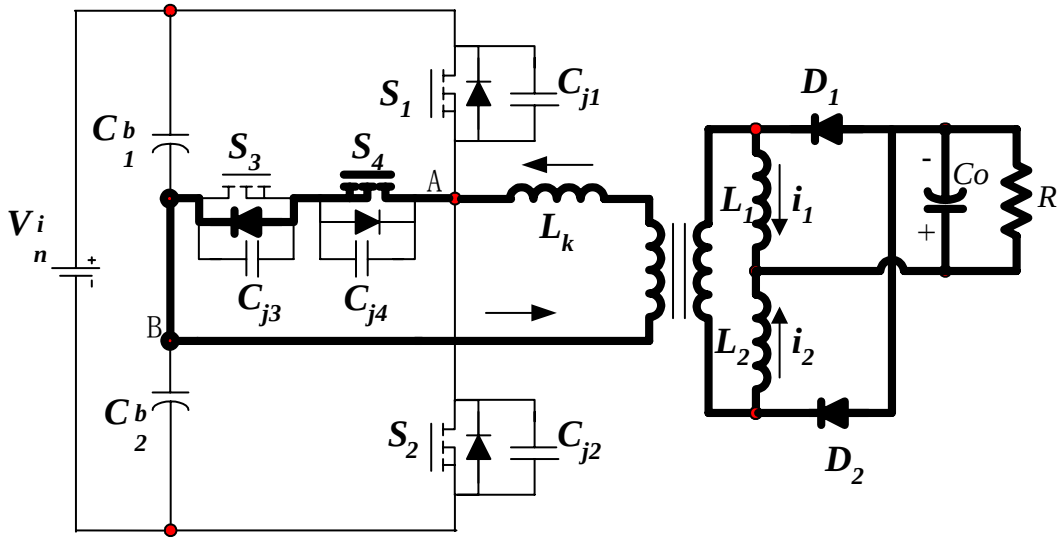
<Mode 2>


Vin
Cb1
Cb2
S1
S2
S3
S4
Cj1
Cj2
Cj3
Cj4
A
B
Lk
D1
D2
L1
L2
i1
i2
Co
R

<Mode 3>


Vin
Cb1
Cb2
S1
S2
S3
S4
Cj1
Cj2
Cj3
Cj4
A
B
Lk
D1
D2
L1
L2
i1
i2
Co
R

<Mode 4>


Cb1
S1
Cj1
D1
S3
S4
A
Lk
L1
i1
Co
R
Vin
Cj3
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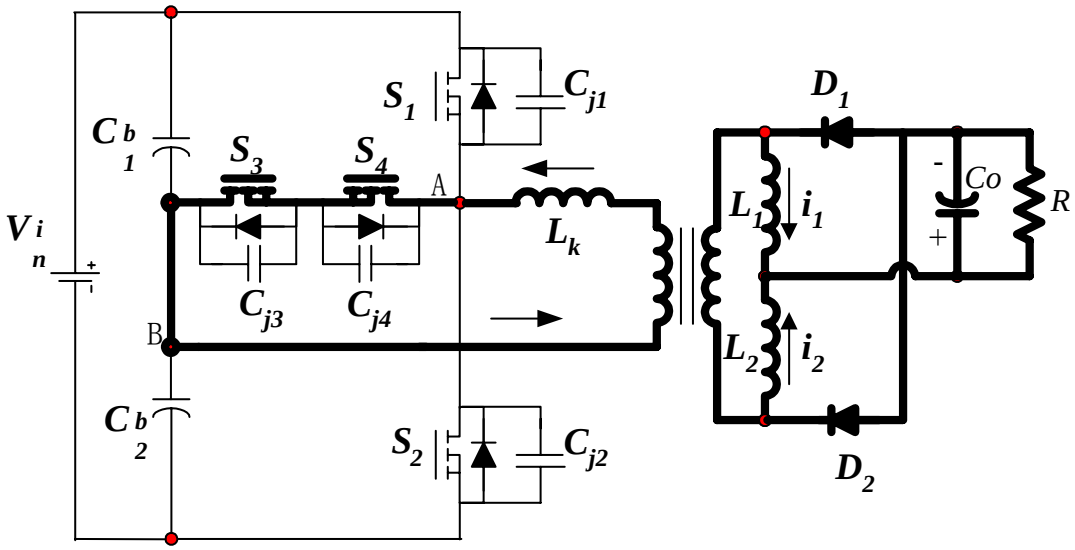
B
L2
i2
Cb2
S2
Cj2
D2

<Mode 5>


Cb1
S1
Cj1
D1
S3
S4
A
Lk
L1
i1
Co
R
Vin
Cj3
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B
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i2
Cb2
S2
Cj2
D2

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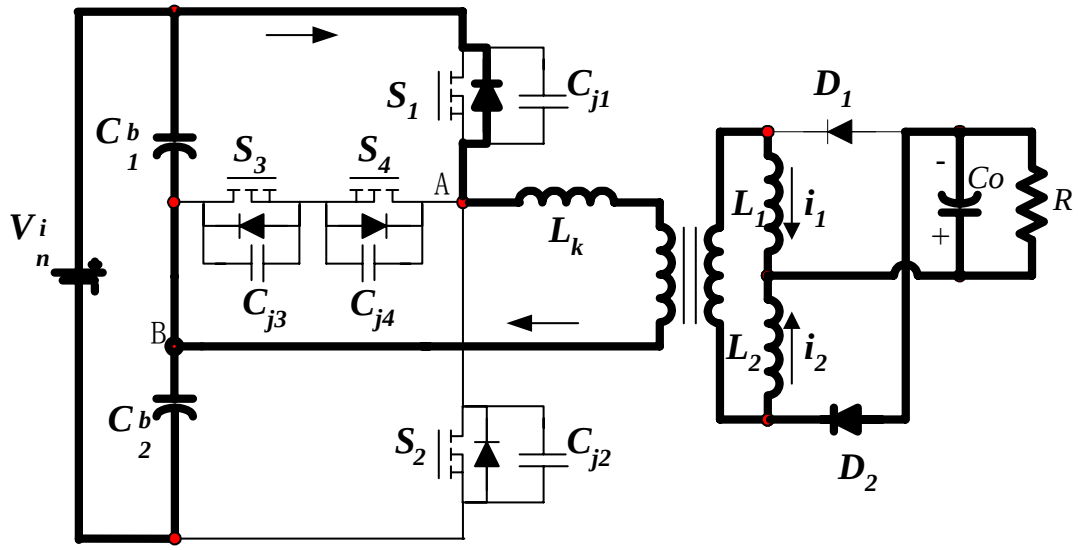

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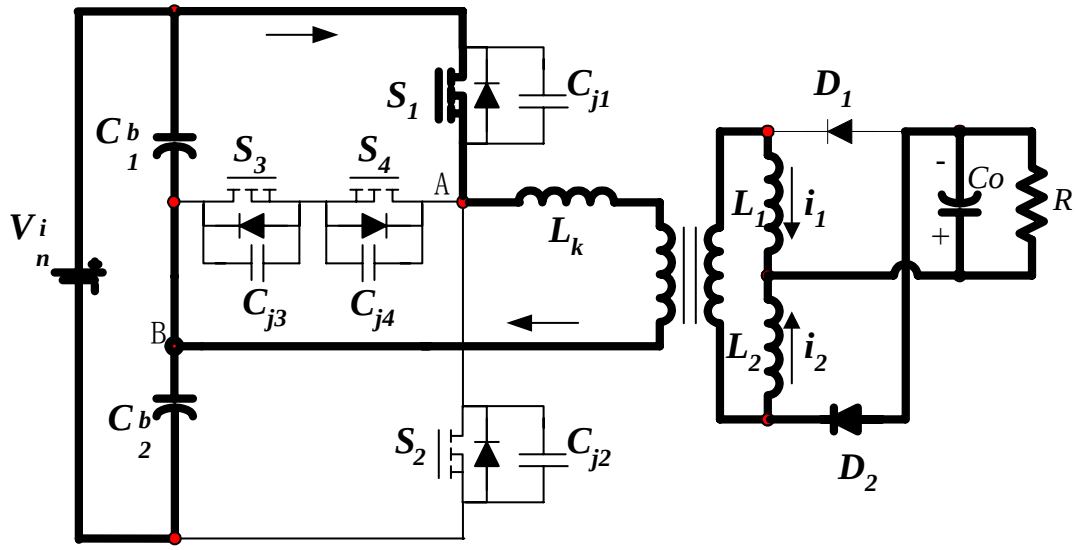


<Mode 8>

Figure 5.3 Operation mode for the active-clamp half-bridge CDR topology

5.2 Experimental Results

In order to meet fast transient response requirement, secondary-side control is applied to the proposed active-clamp half-bridge dc-dc converter with current doubler rectifier. A prototype is built as shown in Figure. 5.4 and the prototype schematics is presented in Figure. 5.5. The prototype is fabricated as standard 16^{th} brick by DOSA, and its specification is as follows: the input voltage 36~75 V with nominal voltage 48V, output voltage 1V, and maximum load current of 30A. In the prototype, Si7810 is used for two main switches S_1 and S_2 of the primary-side half bridge converter, Si7220DN is used for two auxiliary switches S_3 and S_4 and Si7868 is used for the secondary-side synchronous rectifier SR_1 and SR_2, two in parallel each side. Core ER14.5/3F35 is selected as the planar transformer with turns ratio of 6:1. The converter runs at the switching frequency of 450 kHz. Core ER9.5/3F35 is selected as the planar inductors with an inductance value of 0.26 μH. LM5033 is selected as secondary-side PWM controller, LM5101 is the driver for primary switches S_1 and S_2 and LTC 4440 is the driver for two auxiliary switches S_3 and S_4,

Figure 5.4 Experimental prototype

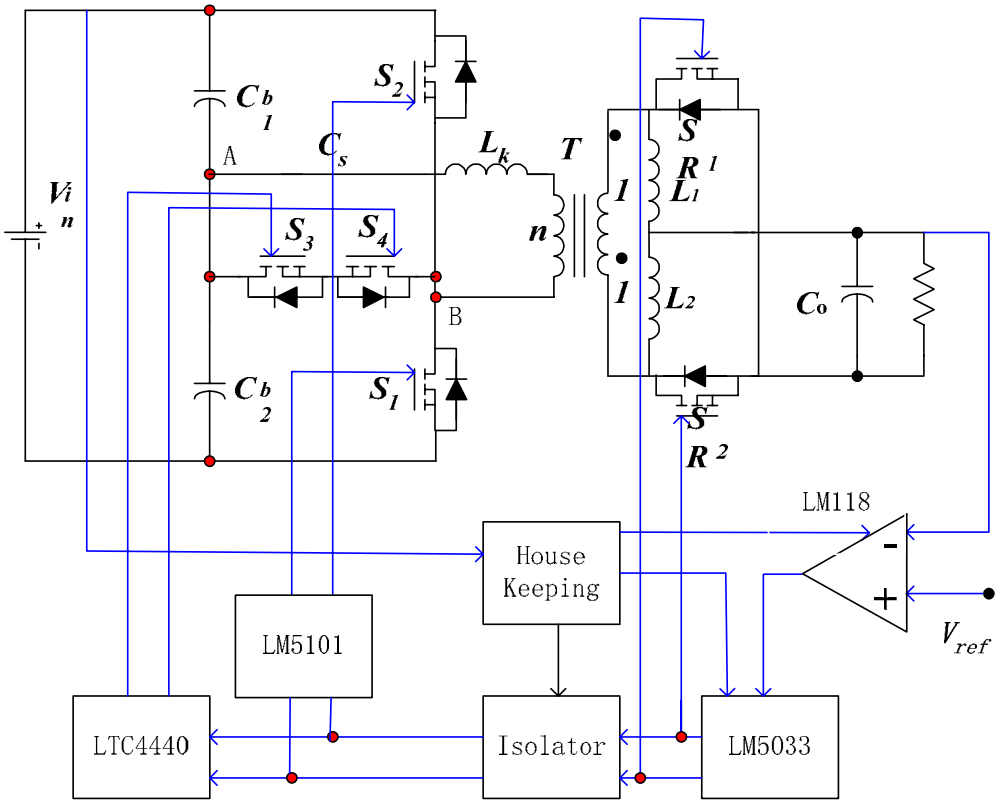


Figure 5.5 Prototype schematics

Figure. 5.6 shows the experimental waveforms for V_B and I_p, and it can be seen that the waveform is very clean and aggress well with theoretical analysis. The driving waveforms are shown in Figures. 5.7 and 5.8, where it can be found that the driving is very simple for the proposed active-clamp half-bridge dc-dc converter with current doubler rectification.

Efficiency is measured for different input line voltage of 36V and 48V respectively and good efficiency is achieved and shown in Figure 5.9. The infrared thermal picture is taken for the prototype operating at 450 kHz with fan and without fan under 48 V input voltage and 30 full load conditions as shown in Figure 5.10 (a) and (b). Good thermal performance is observed.

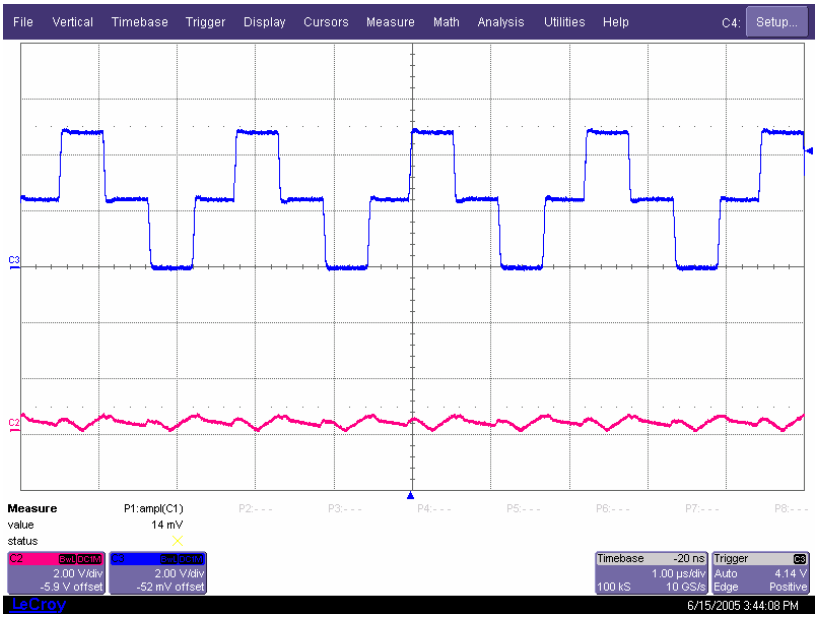


Figure 5.6 Experimental waveforms for V_{in}=48V and I_o=0A

(Top trace: V_B (20V/div), Bottom trace: I_p (2A/div))

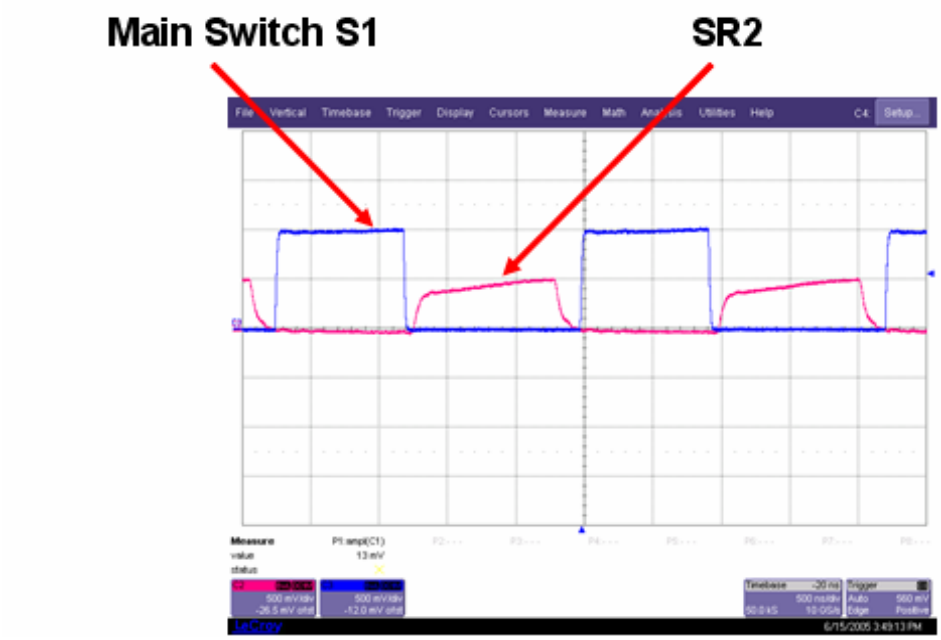


Figure 5.7 Driving waveforms for S_1 and SR_2 (5V/div)

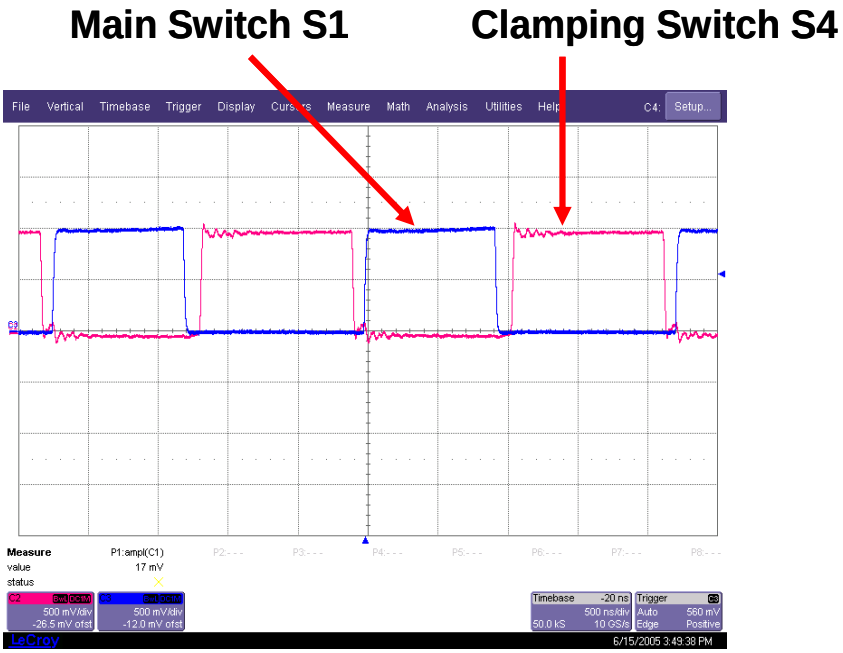


Figure 5.8 Driving waveforms for S_1 and S_4 (5V/div)

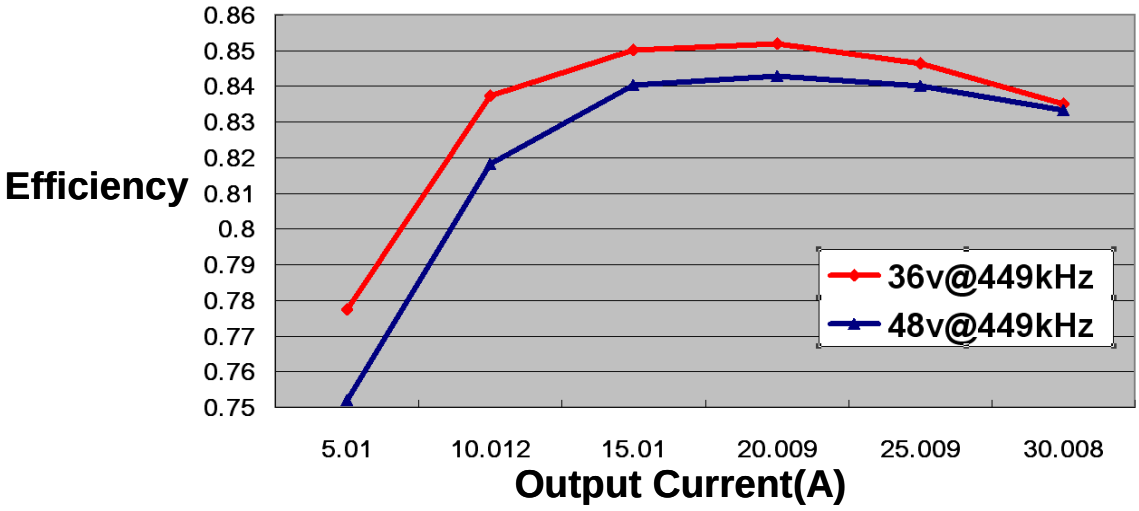
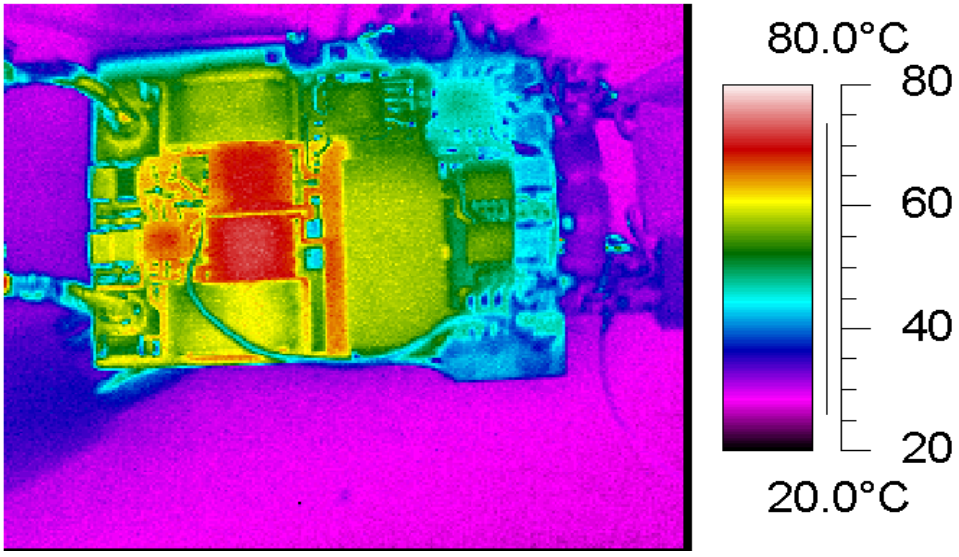
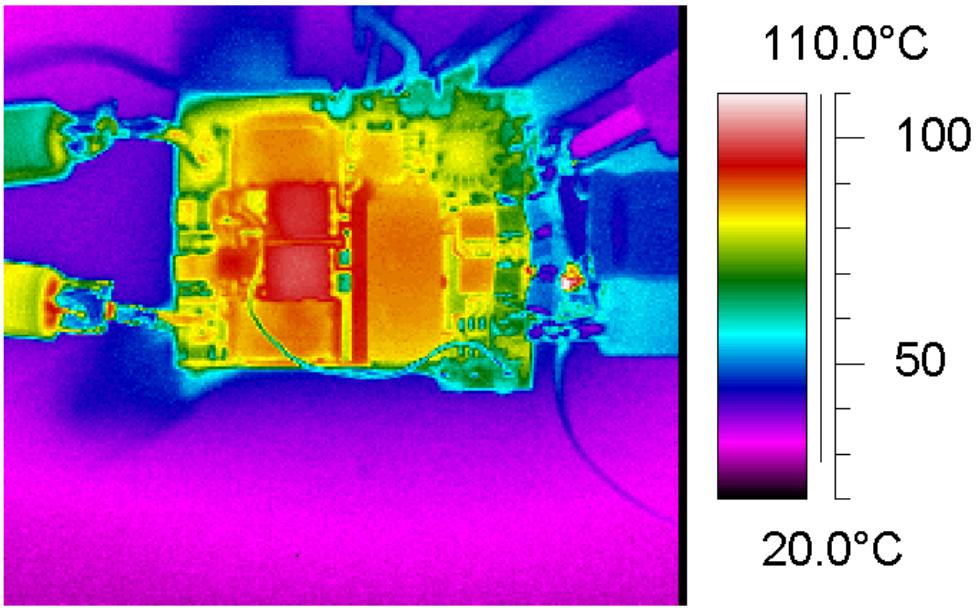


Figure. 5.9 Efficiency curves for different line input voltage.

(Top curve: V_{in} =36V, Bottom curve: V_{in} =48V)



(a) with fan



(b) without fan

Figure 5.10 Infrared thermal picture under condition:

Vin= 48V, Vo=1V, I_o= 30A, f_s=450 kHz

In order to evaluate the transient response, close-loop frequency response of the prototype is measured by Model 200 Analog Network Analyzer from AP instruments. As shown in Figure. 5.11, the bandwidth is 58 kHz and phase margin is 25 degree, which is a little bit low. Transient response is recorded in Figure. 12: for the step-up load change from 5 A to 25 A with a slew rate of 170 A / us, and the undershoot is 240 mV with 25 us settling time; for the step-down load change from 25 A to 5 A with a slew rate of 400 A/us, the overshoot is 260mV with 25 us settling time. Good transient response is observed with good efficiency under secondary-side control.

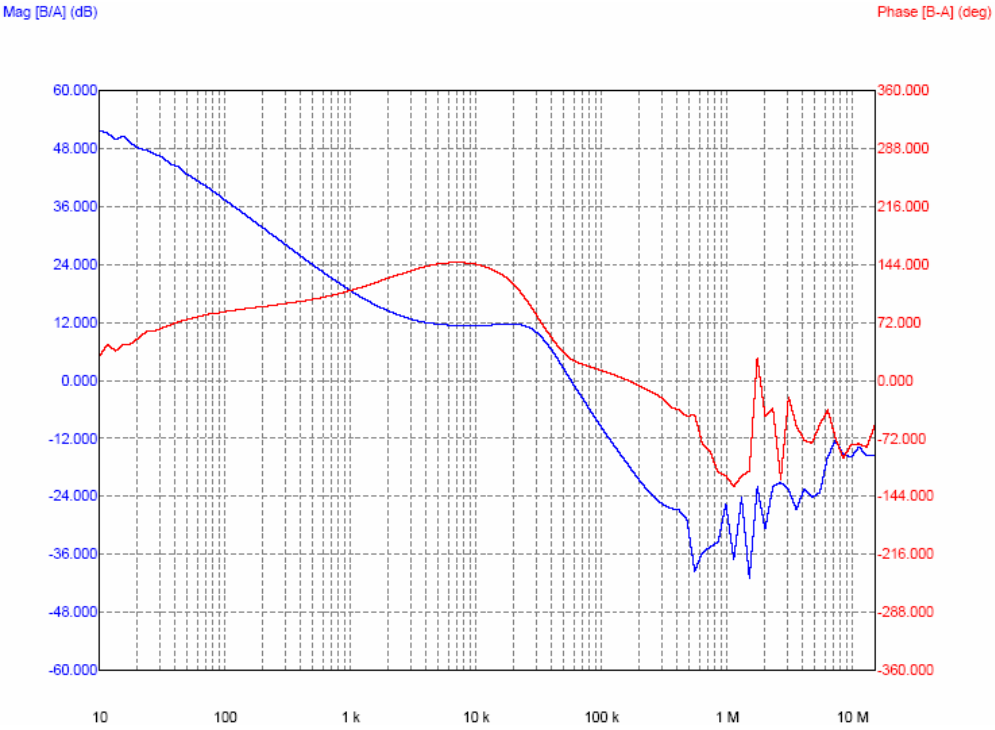


Figure 5.11 Close-loop bode plot before optimization

under the condition: Vin=36 V and Io=5A

To further improve the transient response, further compensation optimization is undertaken. The optimized system's close-loop frequency response is tested and shown in Figure. 5.13. The bandwidth is very high, increased to 80 kHz and phase margin is very good, which is 70 degree. Based on the frequency response parameters, better transient response is expected.

Figure 5.14 shows the transient response test results after the prototype is optimized: for the step-up load change from 5 A to 25 A with a slew rate of 170 A / us, the undershoot now is reduced to 170 mV with 20 us settling time, which is also shorter; for the step-down load change from 25 A to 5 A with a slew rate of 400 A/us, the overshoot is 180mV with 20 us settling time. Better transient response is achieved after optimization as expected.

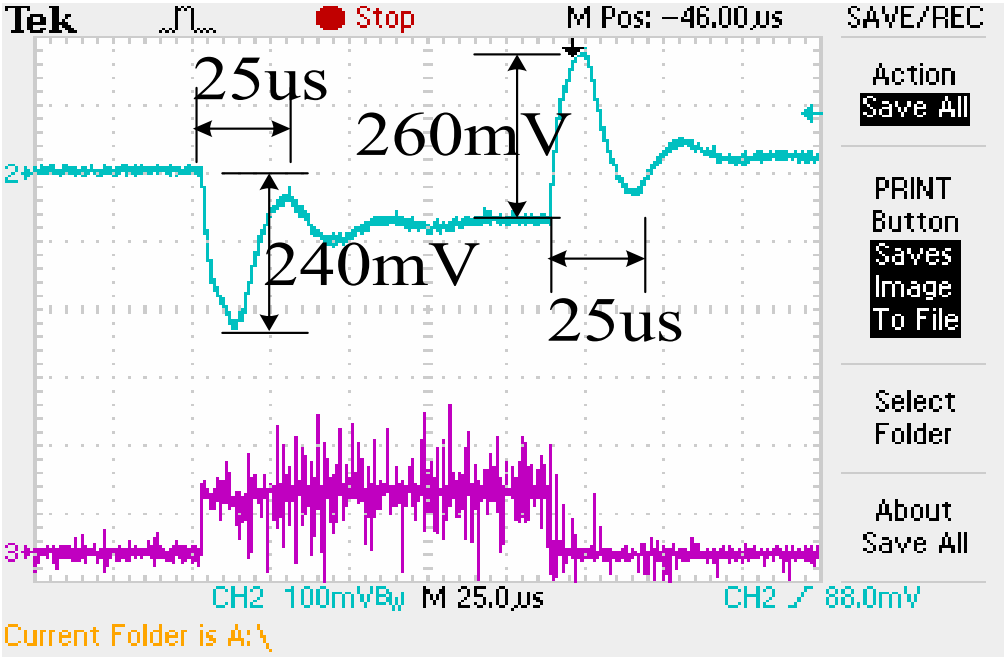


Figure 5.12 Initial transient response test for Vin=36 V

(Step-up load change from 5A to 25 A and step-down load change from 25A to 5 A)

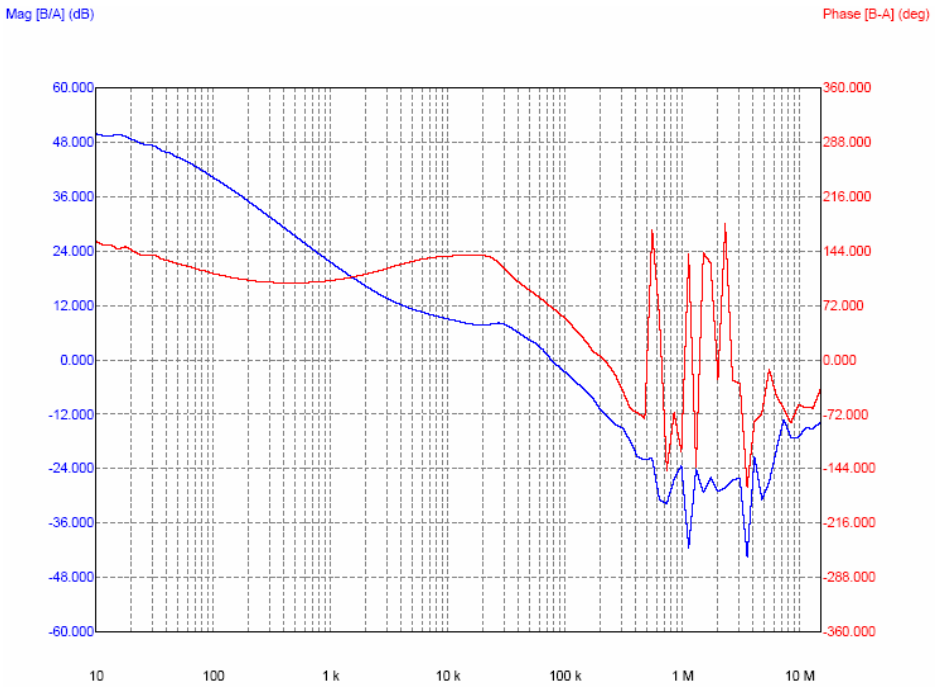


Figure 5.13 Close-loop bode plot after optimization

under the condition: Vin=36 V and Io=5A:

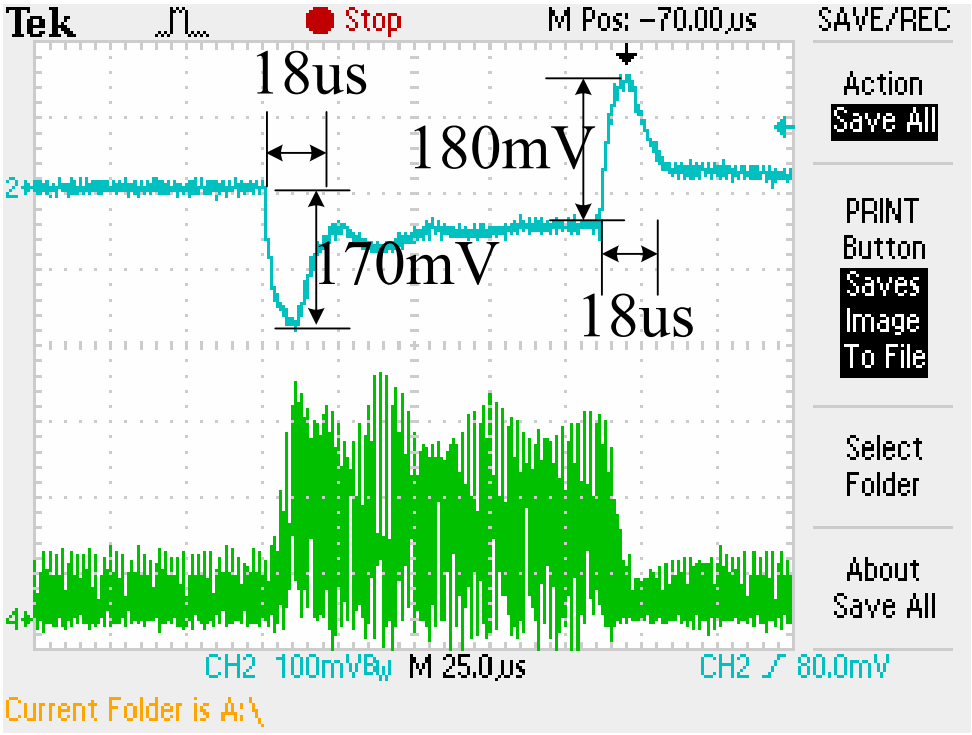


Figure 5.14 Transient response test after optimization for Vin=36 V

(Step-up load change from 5A to 25 A and step-down load change from 25A to 5 A)

CHAPTER SIX: ZERO-VOLTAGE-SWITCHING BUCK- FLYBACK ISOLATED DC-DC CONVERTER WITH SYNCHORNOUS RECTIFICATION

The conventional flyback converter has long been attractive due to its multi-output capability with cross regulation and relative simplicity as well as low cost, compared to other topologies used in low power applications [73-82]. However, the hard switching operation and leakage-inductance-related ringing result in high switching, ringing losses and EMI noise. In addition, it needs additional windings and rectifiers for multi-output applications as shown in Figure 6. 1.

Many flyback derived topologies have been developed to improve the performance of the traditional flyback converters [73-81]. Among them, resonant flyback converters were proposed to reduce switching losses and EMI noise at the expense of the voltage and/or current stress increase and high conduction loss [73-74]. Moreover, similar to traditional flyback converters, extra windings and rectifiers are needed for multi-output applications.

An active-clamp flyback converter can achieve zero-voltage-switching (ZVS) for switches and therefore reduce EMI noise, but it still has high voltage stress across the primary switches and secondary rectifier [75-77]. It has the same problem as traditional flyback converters when applied to multi-output cases, where more windings and rectifiers have to be added for additional outputs. Figure 6.2 shows the active-clamp flyback converter with multiple outputs.

Asymmetrical half bridge (AHB) flyback converter [78-81] gained popularity recently, since it can lower the switch voltage stress and achieve ZVS with low EMI noise. However, for the applications requiring two isolated outputs, for example, a standalone housekeeping power supply, two transformer windings are required to supply two channels of output as

shown in Figure 6.3. In addition, control isolation is regularly required to close the feedback loop when precisely regulating one of the two outputs and to provide isolation between the primary side and secondary side.

In this chapter, a new zero-voltage-switching buck-flyback isolated dc-dc converter with synchronous rectification is proposed. This topology can provide two isolated outputs without additional transformer windings and secondary rectifiers, leading to improvement of transformer copper window utilization and conversion efficiency. Moreover, primary-side control of this topology can eliminate control isolation, resulting in further reduction in cost and complexity. In addition, ZVS can be achieved for both switches with low switch voltage stress and EMI noise.

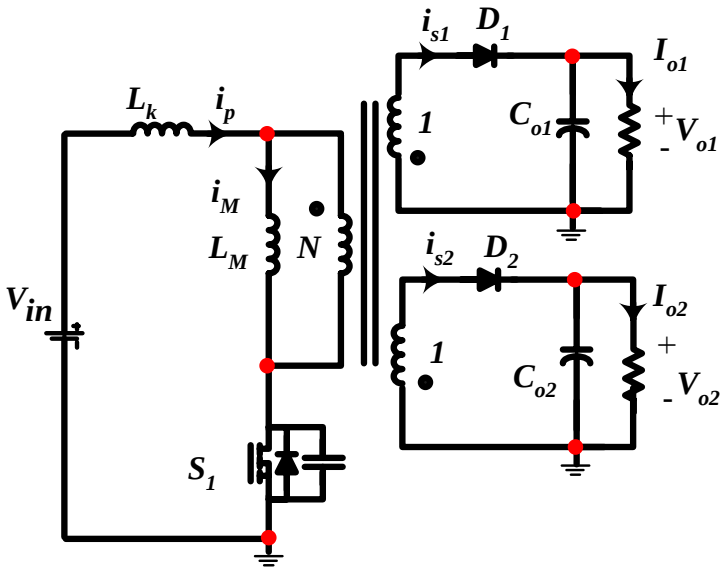


Figure 6.1 Conventional flyback converter with multi-outputs

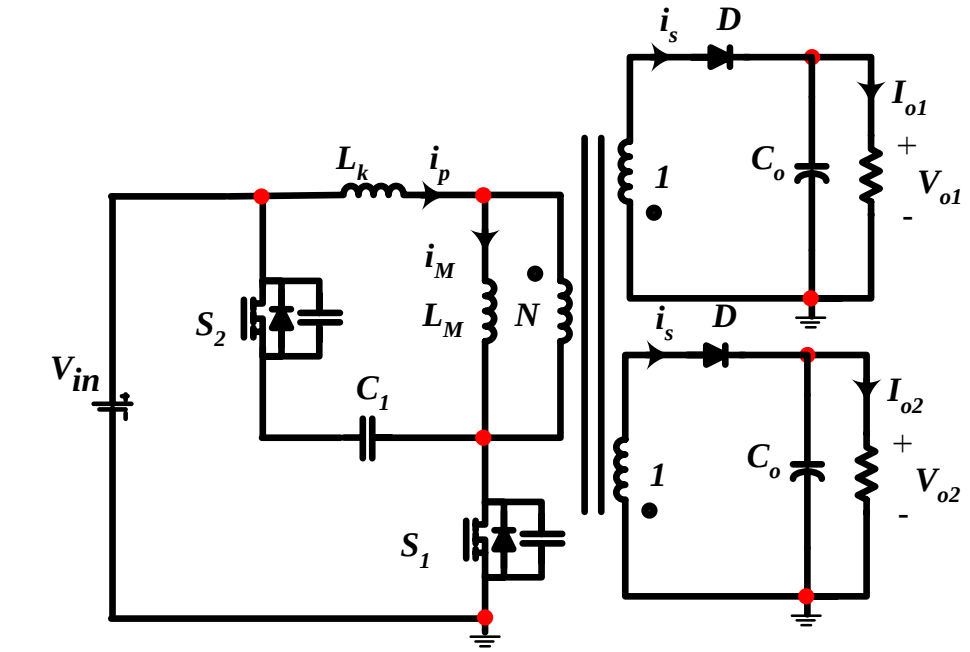


Figure 6.2 Active-clamp flyback converter with multi-outputs

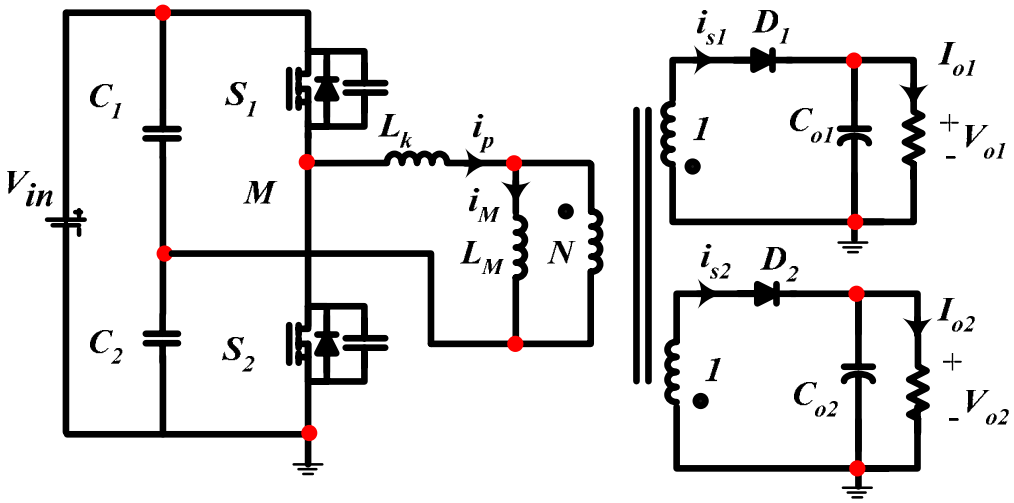
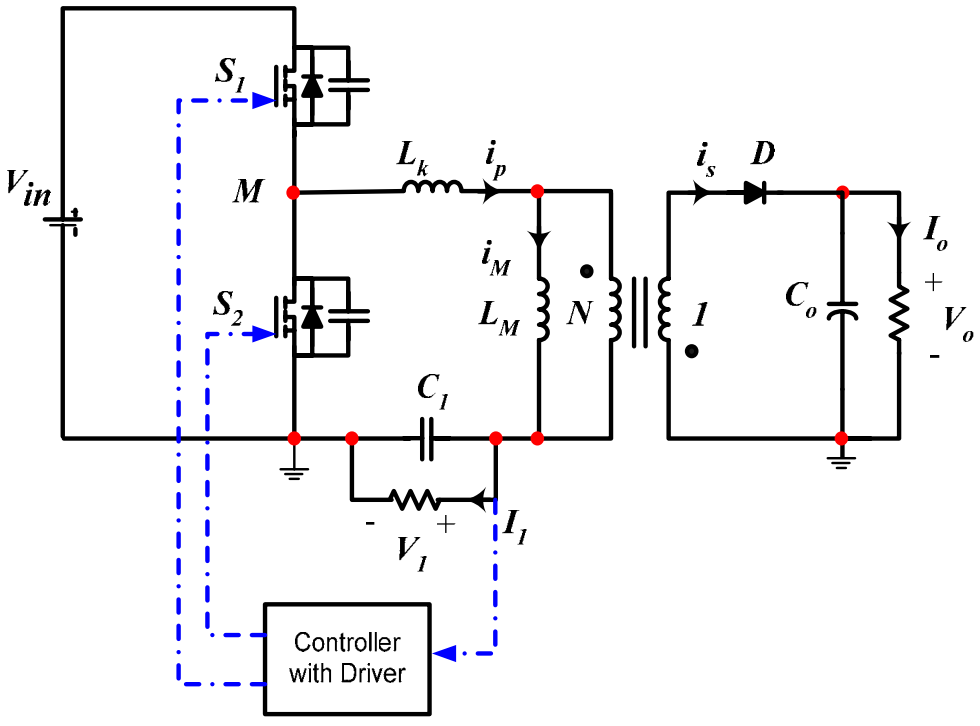


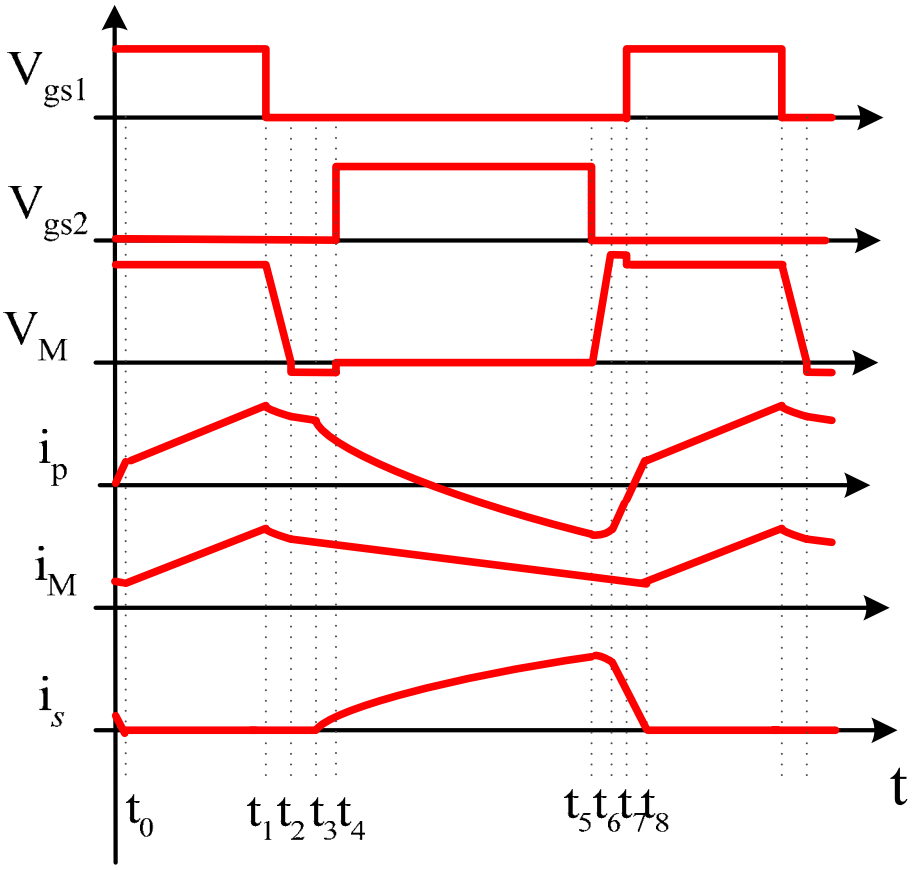
Figure 6.3 Asymmetrical half-bridge flyback converter with multi-outputs

6.1 Steady-state and DC Analysis

The proposed ZVS buck-flyback topology and its key waveforms of steady state operation are shown in Figure. 6.4. There are two isolated outputs: one is from primary capacitor C_1 and the other is from the secondary capacitor C_o. L_M is transformer magnetizing inductance and L_k is the leakage inductance of the transformer. S_1 and S_2 are driven complementarily. When there is no load on the secondary-side output (I_o=0), the converter is operating as a conventional buck converter; when no load is added at the primary side output (I_1=0), the converter acts as an AHB flyback converter. That is why the converter is named as a hybrid buck-flyback converter.



(a) Proposed ZVS buck-flyback topology



(b) Key waveforms of steady state operation

Figure 6.4. ZVS buck-flyback converter and key operation waveforms

6.1.1. DC Analysis

The following assumptions are made for the steady-state dc analysis: the dead time between the conduction modes of two main switches S_1 and S_2 is neglected, the leakage inductance is negligible as compared with the magnetizing inductance of transformer and magnetizing inductor current ripple is negligible.

1) *Voltage gain:*

The voltage gains of two outputs are proportional to the duty cycle *D*. The

secondary-side output voltage gain is also affected by transformer turns ratio N. They can be derived from the volt-second balance of the transformer.

For the primary side output V_1:

$$\frac{V_1}{V_{in}} = D \tag{6-1}$$

For the secondary side output V_o:

$$\frac{V_o}{V_{in}} = \frac{D}{N} \tag{6-2}$$

2) *Averaged magnetizing current I_M:*

The averaged magnetizing current is determined by two output load currents as well as transformer turns ratio N. It can be derived from the charge balance of two output capacitors.

$$I_M = I_1 + \frac{I_o}{N} \tag{6-3}$$

6.1.2. Steady-state Operation Mode Analysis

The operation principle of the ZVS buck-flyback converter can be described by eight operation modes as shown in Figure 6.2. For this description of circuit operation, the following assumptions are made: the converter operates in steady state, leakage inductance L_k is much less than magnetizing inductance L_M, sufficient energy is stored in L_k to completely discharge the junction capacitance voltage to zero and thereafter the body diode will carry current and the time constant of L_k and C_1 is much longer than the off time of S_1.

Mode 1 [t_0, t_1] At t_0, switch S_1 is on, and S_2 is off. The secondary side diode D is reverse biased. The converter operates in buck mode. The leakage inductance L_k and

magnetizing inductance L_M are linearly charged by the difference voltage $(V_{in} - V_1)$ as shown in (6-4).

$$(L_M + L_k) \cdot \frac{di_p(t)}{dt} = V_{in} - V_1 \tag{6-4}$$

where i_p is the primary-side current of the transformer, V_{in} is the input voltage and V_1 is the primary-side output voltage.

If considering v_1 is not constant, the state equations are:

$$(L_M + L_k) \cdot \frac{di_p(t)}{dt} = V_{in} - v_1(t) \tag{6-5}$$

$$C_1 \cdot \frac{dv_1(t)}{dt} + I_1 = i_p(t) = i_M(t) \tag{6-6}$$

Solving (6-5) and (6-6) yields:

$$i_p(t) = \frac{V_{in} - v_1(t_0)}{Z_0} \cdot \sin \omega_0 (t - t_0) + \left(i_p(t_0) - I_1 \right) \cdot \cos \omega_0 (t - t_0) + I_1$$

$$\approx \frac{V_{in} \cdot (1 - D)}{Z_0} \cdot \sin \omega_0 (t - t_0) + \left(i_p(t_0) - I_1 \right) \cdot \cos \omega_0 (t - t_0) + I_1 \tag{6-7}$$

$$i_M(t) \approx \frac{V_{in} \cdot (1 - D)}{Z_0} \cdot \sin \omega_0 (t - t_0) + \left(i_p(t_0) - I_1 \right) \cdot \cos \omega_0 (t - t_0) + I_1 \tag{6-8}$$

$$v_1(t) = V_{in} - \left(V_{in} - v_1(t_0) \right) \cdot \cos \omega_0 (t - t_0) + \left(i_p(t_0) - I_1 \right) \cdot Z_0 \cdot \sin \omega_0 (t - t_0)$$

$$\approx V_{in} - V_{in} \cdot (1 - D) \cdot \cos \omega_0 (t - t_0) + \left(i_p(t_0) - I_1 \right) \cdot Z_0 \cdot \sin \omega_0 (t - t_0) \tag{6-9}$$

where $\omega_0 = \sqrt{\frac{1}{(L_M + L_k) \cdot C_1}}$ and $Z_0 = \sqrt{\frac{L_M + L_k}{C_1}}$.

Mode 2 [t_1, t_2] Switch S_1 is turned off at t_1. L_k and L_M start to resonate with C_{ds1}, C_{ds2} and C_1. C_{ds1} is charged, and C_{ds2} discharged. Since this sub-interval is much shorter than the resonant period, it results in approximately linear charging and discharging characteristics.

The equations that define this operation mode are given in:

$$(L_M + L_k)\cdot\frac{di_p(t)}{dt} = V_{in} - v_{ds1}(t) - v_1(t) \tag{6-10}$$

$$C_1\cdot\frac{dv_1(t)}{dt} + I_1 = i_p(t) = i_M(t) \tag{6-11}$$

$$C_{ds1}\cdot\frac{dv_{ds1}(t)}{dt} - C_{ds2}\cdot\frac{dv_{ds2}(t)}{dt} = i_p(t) = i_M(t) \tag{6-12}$$

$$v_{ds1}(t) + v_{ds2}(t) = V_{in} \tag{6-13}$$

where C_{ds1} and C_{ds2} are the junction capacitance of switches S_1 and S_2 respectively; $v_{ds1}(t)$ and $v_{ds2}(t)$ are the drain-to-source voltage of switches S_1 and S_2 respectively.

Solving (6-10) ~ (6-13) yields:

$$\begin{aligned} i_p(t) &= \frac{V_{in} - v_1(t_1)}{Z_1}\sin\omega_1(t-t_1) + \left(i_p(t_1) - \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1\right)\cdot\cos\omega_1(t-t_1) \\ &+ \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1 \\ &\approx \frac{V_{in}(1-D)}{Z_1}\sin\omega_1(t-t_1) + \left(i_p(t_1) - \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1\right)\cdot\cos\omega_1(t-t_1) \\ &+ \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1 \end{aligned} \tag{6-14}$$

$$\begin{aligned} i_M(t) &\approx \frac{V_{in}(1-D)}{Z_1}\sin\omega_1(t-t_1) + \left(i_p(t_1) - \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1\right)\cdot\cos\omega_1(t-t_1) \\ &+ \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1 \end{aligned} \tag{6-15}$$

$$\begin{aligned} v_{ds1}(t) &= \frac{C_1\cdot(V_{in} - v_1(t_1))}{C_1+C_{ds1}+C_{ds2}}\left(1-\cos\omega_1(t-t_1)\right) + \frac{i_p(t_1) - \frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1}{(C_{ds1}+C_{ds2})\cdot\omega_1}\cdot\sin\omega_1(t-t_1) \\ &+ \frac{I_1}{C_1+C_{ds1}+C_{ds2}}\cdot(t-t_1) \end{aligned}$$

$$\approx \frac{C_1 \cdot V_{in} \cdot (1-D)}{C_1 + C_{ds1} + C_{ds2}} \left(1 - \cos \omega_1 (t - t_1)\right) + \frac{i_p(t_1) - \frac{C_{ds1} + C_{ds2}}{C_1 + C_{ds1} + C_{ds2}} \cdot I_1}{(C_{ds1} + C_{ds2}) \cdot \omega_1} \cdot \sin \omega_1 (t - t_1) \tag{6-16}$$
$$+ \frac{I_1}{C_1 + C_{ds1} + C_{ds2}} \cdot (t - t_1)$$

$$v_{ds2}(t) = V_{in} - \frac{C_1 \cdot V_{in} \cdot (1-D)}{C_1 + C_{ds1} + C_{ds2}} \left(1 - \cos \omega_1 (t - t_1)\right) - \frac{i_p(t_1) - \frac{C_{ds1} + C_{ds2}}{C_1 + C_{ds1} + C_{ds2}} \cdot I_1}{(C_{ds1} + C_{ds2}) \cdot \omega_1} \cdot \sin \omega_1 (t - t_1) \tag{6-17}$$
$$- \frac{I_1}{C_1 + C_{ds1} + C_{ds2}} \cdot (t - t_1)$$

$$v_1(t) = \frac{\left(C_{ds1} + C_{ds2}\right) \cdot (V_{in} - v_1(t_1))}{C_1 + C_{ds1} + C_{ds2}} \left(1 - \cos \omega_1 (t - t_1)\right) + \frac{i_p(t_1) - \frac{C_{ds1} + C_{ds2}}{C_1 + C_{ds1} + C_{ds2}} \cdot I_1}{C_1 \cdot \omega_1} \cdot \sin \omega_1 (t - t_1)$$
$$+ \frac{I_1}{C_1 + C_{ds1} + C_{ds2}} \cdot (t - t_1) + v_1(t_1) \tag{6-18}$$

where $\omega_1 = \sqrt{\frac{1}{(L_M + L_k) \cdot \left(C_1 // (C_{ds1} + C_{ds2})\right)}}$ and $Z_1 = \sqrt{\frac{L_M + L_k}{C_1 // (C_{ds1} + C_{ds2})}}$.

Mode 3 [t_2, t_3] The voltage of C_{ds2} is discharged to zero at t_2 , and the body diode of S_2 conducts. C_1 starts to resonate with L_k and L_M. S_2 can be turned on under ZVS after time instant t_2. The state equations can be written as follows:

$$(L_M + L_k) \cdot \frac{di_p(t)}{dt} = -v_1(t) \tag{6-19}$$

$$C_1 \cdot \frac{dv_1(t)}{dt} + I_1 = i_p(t) = i_M(t) \tag{6-20}$$

The transformer primary-side current i_p can be obtained by solving (6-19) and (6-20):

$$i_p(t) = -\frac{v_1(t_2)}{Z_2} \cdot \sin \omega_2 (t - t_2) + \left(i_p(t_2) - I_1\right) \cdot \cos \omega_2 (t - t_2) + I_1$$

$$\approx -\frac{D \cdot V_{in}}{Z_2} \cdot \sin \omega_2 (t - t_2) + \left(i_p(t_2) - I_1\right) \cdot \cos \omega_2 (t - t_2) + I_1 \tag{6-21}$$

$$i_M(t) = -\frac{D \cdot V_{in}}{Z_2} \cdot \sin \omega_2 (t - t_2) + \left(i_p(t_2) - I_1 \right) \cdot \cos \omega_2 (t - t_2) + I_1 \tag{6-22}$$

$$v_1(t) = v_1(t_2) \cdot \cos \omega_2 (t - t_2) + \left(i_p(t_2) - I_1 \right) \cdot Z_2 \cdot \sin \omega_2 (t - t_2) \tag{6-23}$$

where $\omega_2 = \sqrt{\frac{1}{(L_M + L_k) \cdot C_1}}$ and $Z_2 = \sqrt{\frac{L_M + L_k}{C_1}}$.

Mode 4 [t_3, t_4] At t_3, the voltage across the transformer secondary side is sufficient to forward bias secondary rectifier diode D. Diode D is turned on and the transformer primary voltage is then clamped by the secondary output capacitance to approximately NV_o. L_k begins to resonate with C_1 and C_o. The converter operates in flyback mode. The equations describing this mode can be written as:

$$L_k \cdot \frac{di_p(t)}{dt} = nV_o - v_1(t) \tag{6-24}$$

$$L_M \cdot \frac{di_M(t)}{dt} = -nV_o \tag{6-25}$$

$$C_1 \cdot \frac{dv_1(t)}{dt} + I_1 = i_p(t) \tag{6-26}$$

The solutions to (6-24) ~ (6-26) are given in:

$$i_p(t) = \frac{nV_o - v_1(t_3)}{Z_3} \cdot \sin \omega_3 (t - t_3) + \left(i_p(t_3) - I_1 \right) \cdot \cos \omega_3 (t - t_3) + I_1$$

$$\approx \left(i_p(t_3) - I_1 \right) \cdot \cos \omega_3 (t - t_3) + I_1 \tag{6-27}$$

$$i_M(t) = i_M(t_3) - \frac{n \cdot V_o}{L_M} \cdot (t - t_3) \tag{6-28}$$

$$v_1(t) = \left(nV_o - v_1(t_3) \right) \cdot \left(1 - \cos \omega_3 (t - t_3) \right) + Z_3 \cdot \left(i_p(t_3) - I_1 \right) \cdot \sin \omega_3 (t - t_3) + v_1(t_3) \tag{6-29}$$

where $\omega_3 = \sqrt{\frac{1}{L_k \cdot C_1}}$ and $Z_3 = \sqrt{\frac{L_k}{C_1}}$.

Mode 5 [t_4, t_5] At t_4, S_2 is turned on under ZVS. The transformer primary voltage is still clamped by the secondary output capacitance to approximately NV_o. L_k, C_1 and C_o continue to resonate. The dynamic equations are the same as (6-24) ~ (6-26), and the currents and voltage can be given:

$$i_p(t) = \frac{nV_o - v_1(t_4)}{Z_3} \cdot \sin\omega_3(t-t_4) + \left(i_p(t_4) - I_1\right) \cdot \cos\omega_3(t-t_4) + I_1$$

$$\approx \left(i_p(t_4) - I_1\right) \cdot \cos\omega_3(t-t_4) + I_1 \tag{6-30}$$

$$i_M(t) = i_M(t_4) - \frac{n \cdot V_o}{L_M} \cdot (t-t_4) \tag{6-31}$$

$$v_1(t) = \left(nV_o - v_1(t_4)\right) \cdot \left(1 - \cos\omega_3(t-t_4)\right) + Z_3 \cdot \left(i_p(t_4) - I_1\right) \cdot \sin\omega_3(t-t_4) + v_1(t_4) \tag{6-32}$$

Mode 6 [t_5, t_6] Switch S_2 is turned off at t_5. C_{ds1} is charged and C_{ds2} discharged by L_k in resonant manner. Since this sub-interval is much shorter than the resonant period, it results in approximately linear charging and discharging characteristics. The transformer primary voltage remains clamped at NV_o. The equations that define this mode are:

$$L_k \cdot \frac{di_p(t)}{dt} = V_{in} + n \cdot V_o - v_{ds1}(t) - v_1(t) \tag{6-33}$$

$$L_M \cdot \frac{di_M(t)}{dt} = -nV_o \tag{6-34}$$

$$C_1 \cdot \frac{dv_1(t)}{dt} + I_1 = i_p(t) \tag{6-35}$$

$$C_{ds1} \cdot \frac{dv_{ds1}(t)}{dt} - C_{ds2} \cdot \frac{dv_{ds2}(t)}{dt} = i_p(t) = i_M(t) \tag{6-36}$$

$$v_{ds1}(t) + v_{ds2}(t) = V_{in} \tag{6-37}$$

Solving the above equations yields:

$$i_p(t)=\frac{n\cdot V_o-v_1(t_5)}{Z_5}\sin\omega_5(t-t_5)+\left(i_p(t_5)-\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1\right)\cdot\cos\omega_5(t-t_5)+\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1$$

$$\approx\left(i_p(t_5)-\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1\right)\cdot\cos\omega_5(t-t_5)+\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1 \tag{6-38}$$

$$i_M(t)=i_M(t_5)-\frac{n\cdot V_o}{L_M}\cdot(t-t_5) \tag{6-39}$$

$$\begin{aligned}v_{ds1}(t)&=\frac{C_1\cdot(n\cdot V_o-v_1(t_5))}{C_1+C_{ds1}+C_{ds2}}\left(1-\cos\omega_5(t-t_5)\right)+\frac{i_p(t_5)-\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1}{(C_{ds1}+C_{ds2})\cdot\omega_5}\cdot\sin\omega_5(t-t_5)\\&\quad+\frac{I_1}{C_1+C_{ds1}+C_{ds2}}\cdot(t-t_5)+V_{in}\\&\approx\frac{i_p(t_5)-\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1}{(C_{ds1}+C_{ds2})\cdot\omega_5}\cdot\sin\omega_5(t-t_5)+\frac{I_1}{C_1+C_{ds1}+C_{ds2}}\cdot(t-t_5)+V_{in}\end{aligned} \tag{6-40}$$

$$v_{ds2}(t)\approx\frac{\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1-i_p(t_5)}{(C_{ds1}+C_{ds2})\cdot\omega_5}\cdot\sin\omega_5(t-t_5)-\frac{I_1}{C_1+C_{ds1}+C_{ds2}}\cdot(t-t_5) \tag{6-41}$$

$$\begin{aligned}v_{c1}(t)&=\frac{(C_{ds1}+C_{ds2})\cdot(n\cdot V_o-v_1(t_5))}{C_1+C_{ds1}+C_{ds2}}\left(1-\cos\omega_5(t-t_5)\right)\\&\quad+\frac{i_p(t_5)-\frac{C_{ds1}+C_{ds2}}{C_1+C_{ds1}+C_{ds2}}\cdot I_1}{C_1\cdot\omega_5}\cdot\sin\omega_5(t-t_5)+\frac{I_1}{C_1+C_{ds1}+C_{ds2}}\cdot(t-t_5)+v_1(t_5)\end{aligned} \tag{6-42}$$

where $\omega_5=\sqrt{\frac{1}{L_k\cdot\left(C_1//(C_{ds1}+C_{ds2})\right)}}$ and $Z_5=\sqrt{\frac{L_k}{C_1//(C_{ds1}+C_{ds2})}}$.

Mode 7 [t_6, t_7] The voltage of C_{ds1} is discharged to zero at t_6 , and S_1's body diode begins to conduct. C_1 starts to resonate with L_k. S_1 can be turned on under ZVS after time instant t_6. The voltage across L_k is clamped to approximately (V_{in} +NV_o-V_1), while the transformer primary voltage is still clamped at NV_o. The state equations can be written as:

$$L_k \cdot \frac{di_p(t)}{dt} = V_{in} + nV_o - v_1(t) \tag{6-43}$$

$$L_M \cdot \frac{di_M(t)}{dt} = -nV_o \tag{6-44}$$

$$C_1 \cdot \frac{dv_1(t)}{dt} + I_1 = i_p(t) \tag{6-45}$$

Solving (6-43) ~ (6-45) yields:

$$\begin{aligned} i_p(t) &= \frac{V_{in} + nV_o - v_1(t_6)}{Z_3} \cdot \sin\omega_3(t-t_6) + \left(i_p(t_6) - I_1\right) \cdot \cos\omega_3(t-t_6) + I_1 \\ &\approx \frac{V_{in}}{Z_3} \cdot \sin\omega_3(t-t_6) + \left(i_p(t_6) - I_1\right) \cdot \cos\omega_3(t-t_6) + I_1 \end{aligned} \tag{6-46}$$

$$i_M(t) = i_M(t_6) - \frac{n \cdot V_o}{L_M} \cdot (t-t_6) \tag{6-47}$$

$$\begin{aligned} v_1(t) = &\left(V_{in} + nV_o - v_1(t_6)\right)\left(1 - \cos\omega_3(t-t_6)\right) \\ &+ Z_3 \cdot \left(i_p(t_6) - I_1\right) \cdot \sin\omega_3(t-t_6) + v_1(t_6) \end{aligned} \tag{6-48}$$

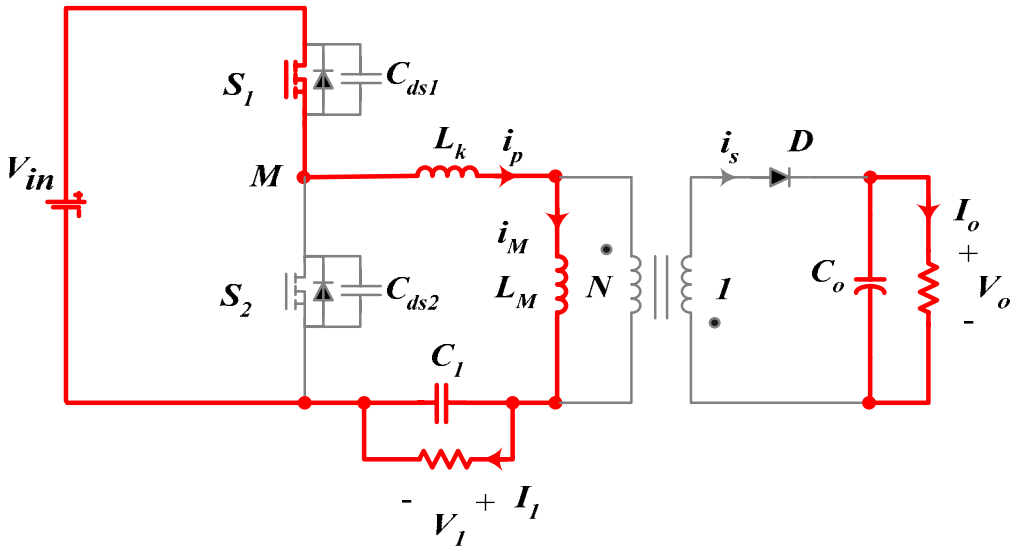
Mode 8 [t_7, t_8] Under the assumptions made above, S_1 is turned on under ZVS at t_7. At t_8, the magnetizing current i_M is equal to the primary side current i_p and diode D is reverse biased. L_k and L_M are linearly charged again by input voltage V_{in}, and a new switching cycle starts.

This mode has the same state equations as Mode 7, and the currents and voltage can be solved:

$$\begin{aligned} i_p(t) &= \frac{V_{in} + nV_o - v_1(t_7)}{Z_3} \cdot \sin\omega_3(t-t_7) + \left(i_p(t_7) - I_1\right) \cdot \cos\omega_3(t-t_7) + I_1 \\ &\approx \frac{V_{in}}{Z_3} \cdot \sin\omega_3(t-t_7) + \left(i_p(t_7) - I_1\right) \cdot \cos\omega_3(t-t_7) + I_1 \end{aligned} \tag{6-49}$$

$$i_M(t) = i_M(t_7) - \frac{n \cdot V_o}{L_M} \cdot (t-t_7) \tag{6-50}$$

$$v_1(t) = \left(V_{in} + nV_o - v_1(t_7)\right)\left(1 - \cos\omega_3(t-t_7)\right) + Z_3 \cdot \left(i_p(t_7) - I_1\right) \cdot \sin\omega_3(t-t_7) + v_1(t_7) \tag{6-51}$$



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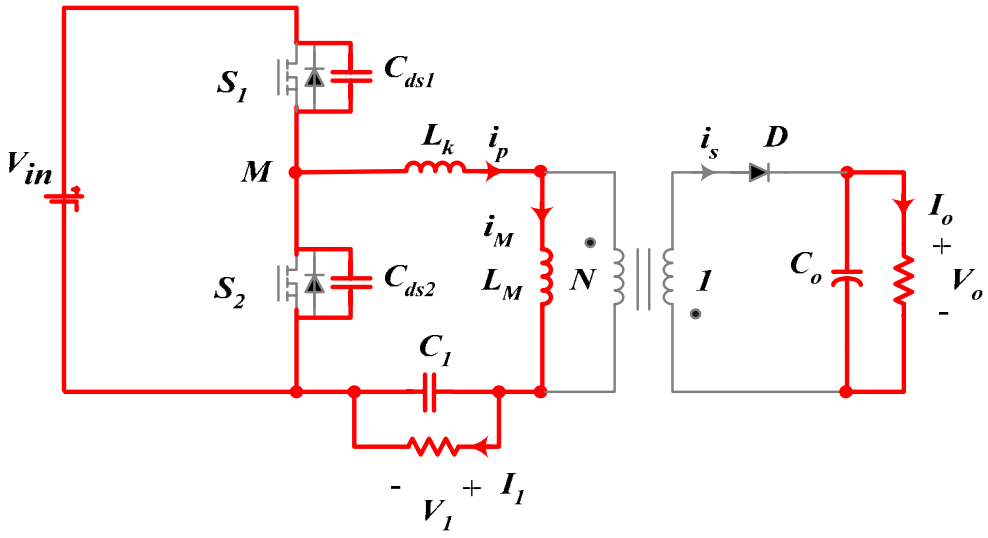

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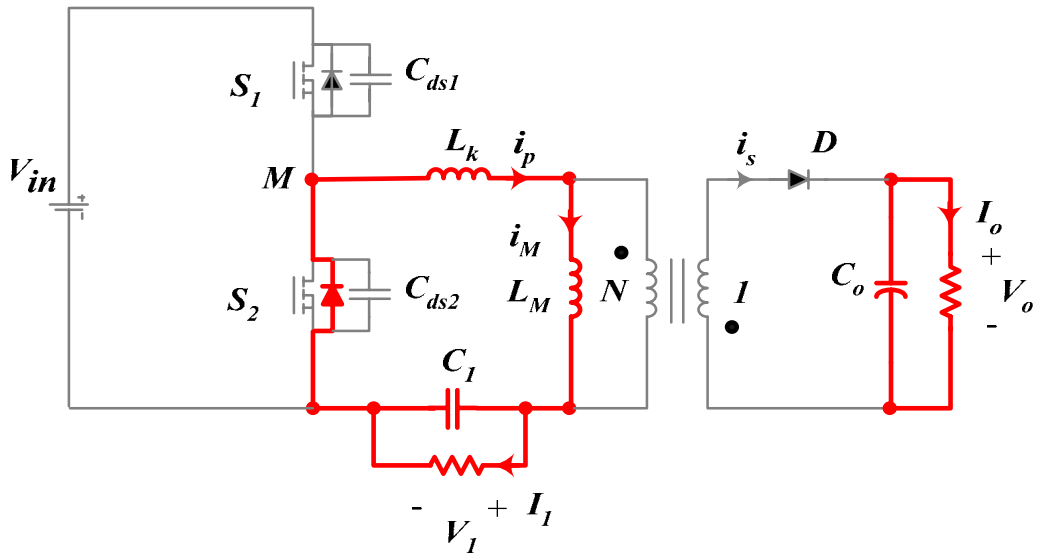
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C_{ds1}
M
L_k
i_p
i_M
S_2
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i_s
D
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C_o
I_o
+
V_o
-
-
V_1
+
I_1

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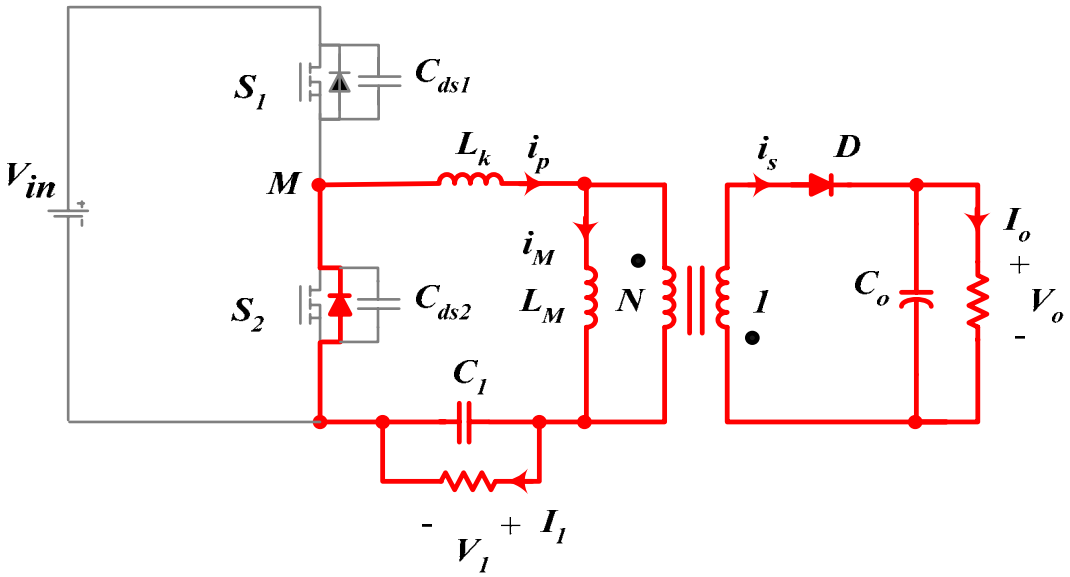
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C_{ds1}
M
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i_p
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S_2
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C_o
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+
V_o
-
-
V_1
+
I_1

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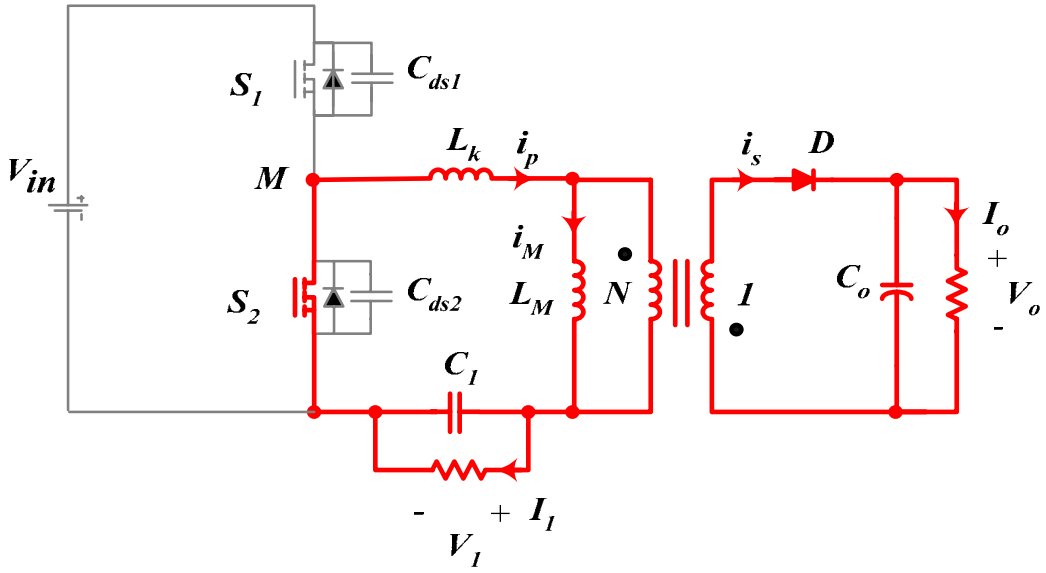
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I_o
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-
C_1
-
+
I_1
V_1

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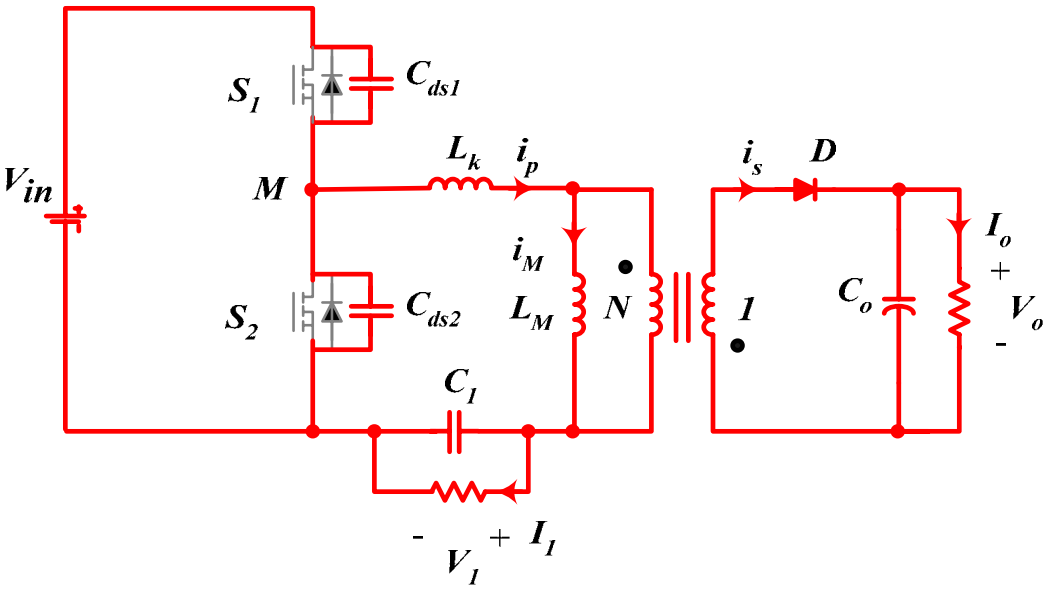
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i_p
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i_M
I_o
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-
C_1
-
+
I_1
V_1

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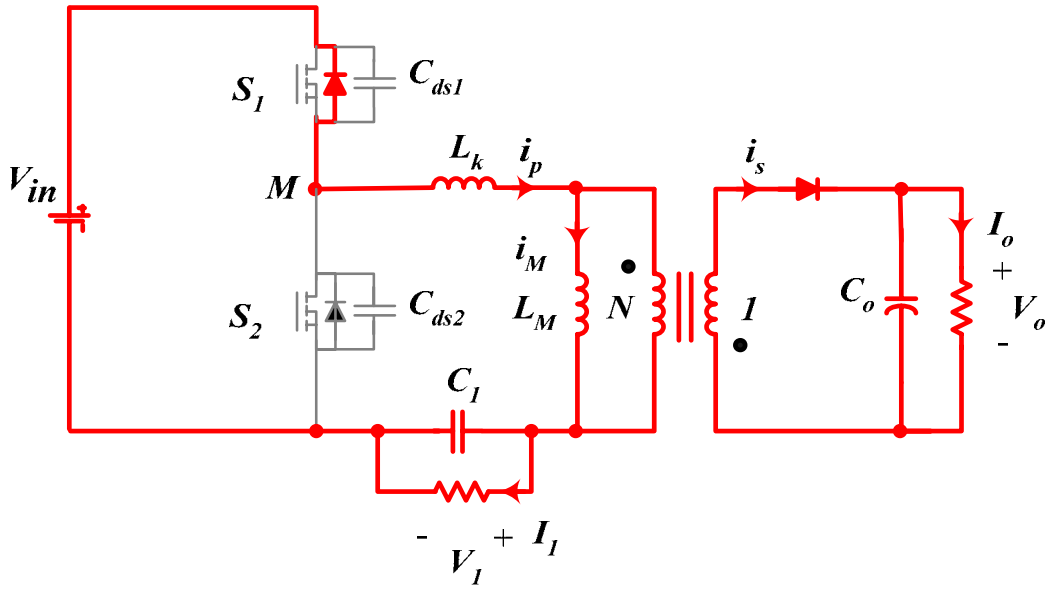

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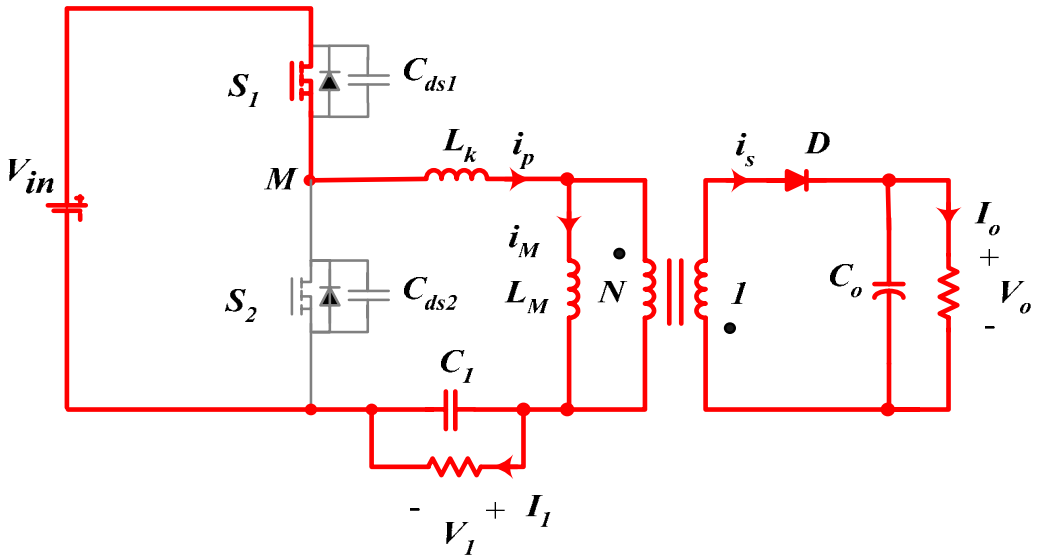


<Mode 8>

Figure 6.5. Operation modes

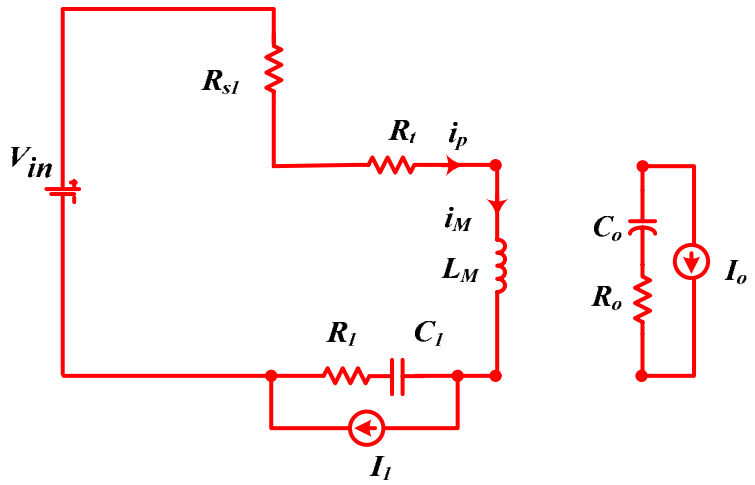
6.2 Average State-space Model of the Proposed Topology

By applying the averaged state-space modeling method [83-85], the state-state dc solutions are presented for the design guidelines of the topology.

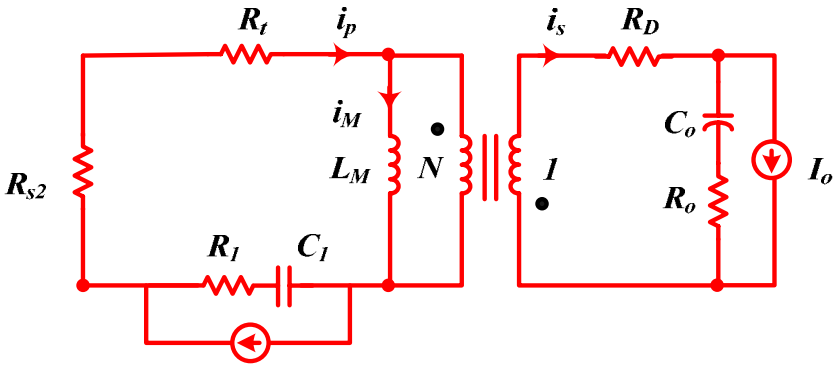
Before deriving the averaged state-space model, the following assumptions are made: both loads are assumed as constant current sources; the transformer leakage inductance is neglected, the transformer magnetizing inductance L_M is referred to the primary-side, and the converter operates in CCM mode due to synchronous rectification. R_{S1}, R_{S2} are the on-resistance of the switches S_1 and S_2 respectively; R_D is the total dc resistance of transformer secondary-side windings and secondary rectifier D; R_t is the dc resistance of the transformer primary-side windings, R_1 and R_o are the ESR (Equivalent Series Resistance) of the output capacitors C_1 and C_o respectively.

There are two typical operation modes: buck mode and flyback mode. For each operation mode shown in Figure 6.6, there is a set of corresponding linear state space equations to represent it. There are two sets of state space equations as expressed in (6-52), where x is the vector of state variables, u is the vector of independent sources that include input voltage and output current sources; A_1, B_1, A_2 and B_2 are respective system matrices for each of the two switched networks in Figure 6.6.

$$\dot{x} = A_m x + B_m u \quad (m = 1, 2) \tag{6-52}$$



i) Buck mode, [t_o, t_o + DT]



ii) Flyback mode, [t_o + DT, t_o + T]

Figure 6.6 Equivalent circuits of typical operation modes

The state-space variables are defined as follows:

$$\boldsymbol{x} = \begin{bmatrix} \boldsymbol{i_M} & \boldsymbol{v_{c1}} & \boldsymbol{v_{co}} \end{bmatrix}^T ;$$

$$\dot{x} = \begin{bmatrix} \frac{di_M}{dt} & \frac{dv_{c1}}{dt} & \frac{dv_{co}}{dt} \end{bmatrix}^T ;$$

$$u = \begin{bmatrix} V_{in} & I_1 & I_o \end{bmatrix}^T \tag{6-53}$$

The key concept in averaging the state-space model is the replacement of the above three sets of state-space equations by a single equivalent set [83-85]:

$$\dot{x} = Ax + Bu \tag{6-54}$$

where the equivalent matrices are defined by

$$A = dA_1 + (1-d)A_2,$$

$$B = dB_1 + (1-d)B_2 \tag{6-55}$$

where, A_1, B_1 are state-space matrices of buck mode ; A_2 *and* B_2 are state-space matrices of flyback mode; d is the duty cycle value of the switch S_1. All these matrices can be derived from Figure 6.6 as follows:

$$A_1 = \begin{bmatrix} -\dfrac{R_{s1} + R_T + R_{c1}}{L_m} & -\dfrac{1}{L_m} & 0 \\ \dfrac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \dfrac{1}{L_M} & \dfrac{R_1}{L_M} & 0 \\ 0 & -\dfrac{1}{C_1} & 0 \\ 0 & 0 & -\dfrac{1}{C_o} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\dfrac{n^2 \cdot (R_D + R_{co}) \cdot (R_{s2} + R_T + R_{c1})}{L_m \cdot \Delta} & -\dfrac{n^2 \cdot (R_D + R_{co})}{L_m \cdot \Delta} & -\dfrac{n \cdot (R_{s2} + R_T + R_{c1})}{L_m \cdot \Delta} \\ \dfrac{n^2 \cdot (R_D + R_{co})}{C_1 \cdot \Delta} & -\dfrac{1}{C_1 \cdot \Delta} & \dfrac{n}{C_1 \cdot \Delta} \\ \dfrac{n \cdot (R_{s2} + R_T + R_{c1})}{C_o \cdot \Delta} & \dfrac{n}{C_o \cdot \Delta} & -\dfrac{n^2}{C_o \cdot \Delta} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 & \dfrac{n^2 \cdot R_{c1} \cdot (R_D + R_{co})}{L_m \cdot \Delta} & -\dfrac{n \cdot R_{co} \cdot (R_{s2} + R_T + R_{c1})}{L_m \cdot \Delta} \\ 0 & -\dfrac{\Delta - R_{c1}}{C_1 \cdot \Delta} & -\dfrac{n \cdot R_{co}}{C_1 \cdot \Delta} \\ 0 \dfrac{n \cdot (R_{s2} + R_T + R_{c1})}{C_o \cdot \Delta} & -\dfrac{n \cdot R_{c1}}{C_o \cdot \Delta} & -\dfrac{\Delta - n^2 \cdot R_{co}}{C_o \cdot \Delta} \end{bmatrix}$$

where $\Delta = n^2 \cdot (R_D + R_{co}) + R_{s2} + R_T + R_{c1}$

The steady-state solution, with dc values indicated by capital letters, is obtained by setting $\dot{x} = 0$,

$$X = -A^{-1}BU \tag{6-56}$$

Through (6-52) ~ (6-56), the steady-state dc quiescent points can be derived and the dc solutions are:

$$I_M = I_1 + \frac{I_o}{N} \tag{6-57}$$

$$V_1 = DV_{in} - \left(DR_{s1} + (1-D)R_{s2} + R_t\right) \cdot I_1 - \frac{D(R_{s1} - R_{s2})}{N} \cdot I_o \tag{6-58}$$

$$V_o = \frac{DV_{in}}{N} - \frac{D(R_{s1} - R_{s2})}{N} \cdot I_1 - \frac{N^2 R_D + D(N^2 R_o + R_1 + R_{s2} + R_t)}{N^2 (1-D)} \cdot I_o \tag{6-59}$$

where I_o and I_1 are the two converter output loads; D is the steady-state duty cycle values of d.

It is noted in (6-58) and (6-59) that two load currents both have effect on output voltage regulation, and it will be discussed in detail in the design consideration part. In the ideal converter where non-ideality is not considered, (6-58) ~ (6-59) agree well with dc analysis results shown in (6-1) ~ (6-3).

6.3 Features and Design Considerations

6.3.1. Main Features

The proposed ZVS buck-flyback dc-dc converter can provide two isolated outputs without additional winding and secondary rectifiers as traditional multi-output flyback converters and other newly proposed flyback derived topologies with the multi-outputs aforementioned. It's suitable for applications where tight regulation is not required for the secondary-side output voltage. From the perspective of energy process path, the primary output power consists of two parts. One is directly delivered from the input (buck mode); the other is coming from the magnetizing energy (flyback mode). Compared with multi-output flyback converter where all the output power is processed through magnetizing energy, this scheme is more efficient. Therefore, the efficiency of this converter will be higher than that of the AHB flyback converter with multi-outputs.

Moreover, the second output can be provided without extra winding and diode rectifier compared to conventional multi-output flyback converter. Elimination of diode rectifier before output voltage will increase efficiency dramatically for low voltage applications. As a result, system cost and complexity are also reduced. In addition, primary-side control of this topology can eliminate control isolation, resulting in further reduction in cost and complexity.

Lastly, ZVS can be achieved for both switches, leading to low EMI noise and ringing loss, which allows this topology to work in high switching frequency operation. The voltage stress of two main switches is equal to input voltage, lower than that of conventional flyback, resonant flyback and active-clamped flyback converters.

The proposed ZVS buck-flyback dc-dc converter is a good candidate topology for

standalone power supply requiring multiple outputs.

6.3.2. Design Considerations

1) ***Transformer magnetizing inductance:***

The introduction of an additional output at the primary side only increases the dc bias of the transformer magnetizing inductor current as shown in (6-3), so the magnetizing inductance can be designed using the same method as that for traditional CCM flyback converters.

2) ***Power switches:***

The voltage stress of two main switches S_1 and S_2 is the same, and is equal to the input voltage after neglecting the forward voltage of a MOSFET's body diode:

$$\boldsymbol{V}_{s_1}^{MAX} = \boldsymbol{V}_{s_2}^{MAX} = \boldsymbol{V}_{in} \tag{6-60}$$

Assuming Mode 7 is so short to be neglected, the peak current value of switch S_1 is:

$$\boldsymbol{I}_{s_1,peak} = \boldsymbol{I}_{p,peak} \approx \boldsymbol{I}_1 + \frac{\boldsymbol{I}_0}{\boldsymbol{N}} + \frac{\boldsymbol{D}\cdot(1-\boldsymbol{D})\cdot\boldsymbol{V}_{in}}{2\cdot\boldsymbol{f}_s\cdot\boldsymbol{L}_M} \tag{6-61}$$

The approximate value of switch S_1 rms current can be evaluated as follows:

$$\boldsymbol{I}_{s_1,RMS} \approx \sqrt{\boldsymbol{D}}\cdot\sqrt{\left(\boldsymbol{I}_1 + \frac{\boldsymbol{I}_0}{\boldsymbol{N}}\right)^2 + \frac{1}{3}\left(\frac{\boldsymbol{D}\cdot(1-\boldsymbol{D})\cdot\boldsymbol{V}_{in}}{2\cdot\boldsymbol{f}_s\cdot\boldsymbol{L}_M}\right)^2} \tag{6-62}$$

In order to estimate the current rating for switch S_2, the assumption has to be made as above, where the L_k - C_1 - C_o resonant period is much longer than the off time of S_1. Under this assumption, and neglecting the short commutation modes such as Modes 2 and 3, the S_2 current waveform approximates to sawtooth waveform with a start-point equal to switch S_1 peak current.

The peak current value of switch S_2 is:

$$\boldsymbol{I}_{s_2,peak} \approx \boldsymbol{I}_1 + \frac{\boldsymbol{I}_0}{\boldsymbol{N}} + \frac{\boldsymbol{D}\cdot(1-\boldsymbol{D})\cdot\boldsymbol{V}_{in}}{2\cdot\boldsymbol{f}_s\cdot\boldsymbol{L}_M} \tag{6-63}$$

3) *Secondary rectifier:*

The voltage stress of secondary rectifier D is:

$$\boldsymbol{V}_D^{MAX} = \frac{\boldsymbol{V}_{in}}{\boldsymbol{N}} \tag{6-64}$$

According to the charge balance of C_o, the averaged current through secondary rectifier is:

$$\boldsymbol{I}_{D,AVE} = \frac{\boldsymbol{I}_0}{1-\boldsymbol{D}} \tag{6-65}$$

Under the assumptions and approximations aforementioned, the diode current waveform approximates triangular, so the peak current of the secondary rectifier D is:

$$\boldsymbol{I}_{D,peak} \approx \frac{2\cdot\boldsymbol{I}_0}{1-\boldsymbol{D}} \tag{6-66}$$

4) *ZVS conditions:*

According to the operation mode analysis in the above section, in order to achieve ZVS for S_2, two conditions have to be satisfied:

(i) Energy requirement: the primary current can discharge C_{ds2} completely:

$$\frac{1}{2}\cdot(\boldsymbol{L}_k+\boldsymbol{L}_M)\cdot\boldsymbol{I}_{p,peak}^2 \geq \frac{1}{2}\cdot\boldsymbol{C}_{ds2}\cdot\boldsymbol{V}_{in}^2 \tag{6-67}$$

where $\boldsymbol{I}_{p,peak} \approx \boldsymbol{I}_1 + \frac{\boldsymbol{I}_o}{\boldsymbol{N}} + \frac{\boldsymbol{D}\cdot(1-\boldsymbol{D})\cdot\boldsymbol{V}_{in}}{2\cdot\boldsymbol{L}_M\cdot\boldsymbol{f}_s}$

(ii) Timing requirement: the deadtime (t_2-t_1) is long enough:

Based on (16),

$$V_{ds1}(t) \approx \frac{C_1 \cdot V_{in} \cdot (1-D)}{C_1 + C_{ds1} + C_{ds2}}\left(1-\cos \omega_1 (t-t_1)\right) + \frac{I_{p,peak} - \frac{C_{ds1}+C_{ds2}}{C_1 + C_{ds1} + C_{ds2}} \cdot I_1}{(C_{ds1}+C_{ds2}) \cdot \omega_1} \cdot \sin \omega_1 (t-t_1) + \frac{I_1}{C_1 + C_{ds1} + C_{ds2}} \cdot (t-t_1) \geq V_{in} \quad (6\text{-}68)$$

Considering $\omega_1(t-t_1)$ is small so that $\sin \omega_1(t-t_1) = \omega_1(t-t_1)$ and $\cos \omega_1(t-t_1) \approx 1$, the approximate solution to (6-68) is as follows:

$$(t_2 - t_1) \geq \frac{(C_{ds1}+C_{ds2}) \cdot V_{in}}{I_{p,peak}} \quad (6\text{-}69)$$

Since (6-67) can always be met, the ZVS for switch S_2 can always be achieved as long as deadtime between two main switches meets (6-69).

To achieve ZVS for the switch S_1, the primary current i_p should at least reverse its direction during Mode 6, so:

$$\boldsymbol{I_{p,valley} \approx I_1 - \frac{I_o}{N} \cdot \frac{1+D}{1-D} - \frac{D \cdot (1-D) \cdot V_{in}}{2 \cdot L_M \cdot f_s} < 0} \quad (6\text{-}70)$$

The ZVS condition of S_1 can be obtained by:

$$\frac{1}{2} \cdot \boldsymbol{L_k \cdot I_{p,valley}^2} \geq \frac{1}{2} \cdot \boldsymbol{C_{ds1} \cdot V_{in}^2} \quad (6\text{-}71)$$

It should be noted that ZVS operation of S_1 depends not only on circuit parameters but also on the load conditions of two outputs. Given enough energy is stored in leakage inductance as (6-71), it is easier to achieve ZVS for S_1 when primary-side output is in light load than in heavy load.

5) *Output voltage regulation:*

As shown in (6-58) and (6-59), two load currents both have effect on two output voltage regulations. As discussed, if primary-side control is applied to the proposed

topology, tight regulation can be achieved for primary-side output while the secondary-side output voltage is roughly regulated. Based on the analytic results in (6-58) and (6-59), the secondary-side output voltage variation range can be derived as follows with primary-side control:

$$\Delta V = V_o - \frac{V_1}{N}$$

$$= \frac{R_{s2} + R_t}{N} \cdot I_1 - \frac{N^2 R_D + D(N^2 R_o + R_1 + R_{s2} + R_t)}{N^2 (1-D)} \cdot I_o \tag{6-72}$$

Secondary-side output can be tightly regulated with primary-side control when $\Delta V=0$:

$$\frac{I_1}{I_o} = \frac{N^2 R_D + D(N^2 R_o + R_1 + R_{s2} + R_t)}{N(1-D)(R_{s2} + R_t)} \tag{6-73}$$

The closer two load current ratio $\frac{I_1}{I_o}$ is to the result in (6-73), the better voltage regulation on secondary-side output can be achieved.

6.4 Experimental Results

An experimental prototype with 12V/2A for the primary-side output and 6V/2A for the secondary-side output was built to evaluate the proposed ZVS buck-flyback topology. For the prototype, MOSFET Si7456 is selected for the two main switches S_1 and S_2, and Schottky diode 30BQ040 is used for the secondary-side rectifier. A planar transformer is fabricated with turns ratio at 2:1, and the switching frequency is 500 KHz. The prototype is shown in Figure. 6.7.

From Figure 6.8, it can be found that the secondary side output voltage is very stable as the primary load changes while the primary side output is tightly regulated by

primary-side closed-loop control. Therefore, it verifies that both two isolated outputs can be regulated by the primary-side control. Figure 6.9 shows the efficiency curve with the primary-side load change when the secondary-side load is constant at I_o=2A. In Figure 6.10 it is shown that the efficiency curve with the secondary side load change under different primary side load conditions. It can be observed that high efficiency is achieved with the proposed topology.

In Figure 6.11, it can be observed that both switches S_1 and S_2 are turned on under ZVS. Figure 6.12 shows ZVS can still be realized for both switches under different load currents. ZVS waveform of switch S_1 and transformer primary side current i_p are shown in Figure. 6.13. They agree well with theoretical waveforms of steady-state analysis in Figure. 6.4. Figures 6.11-13 validate that ZVS can be achieved for both switches under different load conditions.

6.5 Conclusions

In this chapter a novel ZVS buck-flyback topology with two isolated outputs is proposed. Its operation principle and steady-state analysis are discussed along with design considerations. The theoretical analyses and experimental results have verified that good regulation is achieved for two isolated outputs by primary-side control. This topology does not need feedback isolation and extra windings for multi-output as in the conventional flyback converter with multiple windings. Moreover, ZVS is achieved for both switches with low switch voltage stress and EMI noise. As a result, the proposed converter minimizes the cost and improves efficiency compared to the conventional multi-output flyback converter. Therefore, this topology can be a suitable candidate for many isolated multi-output applications.

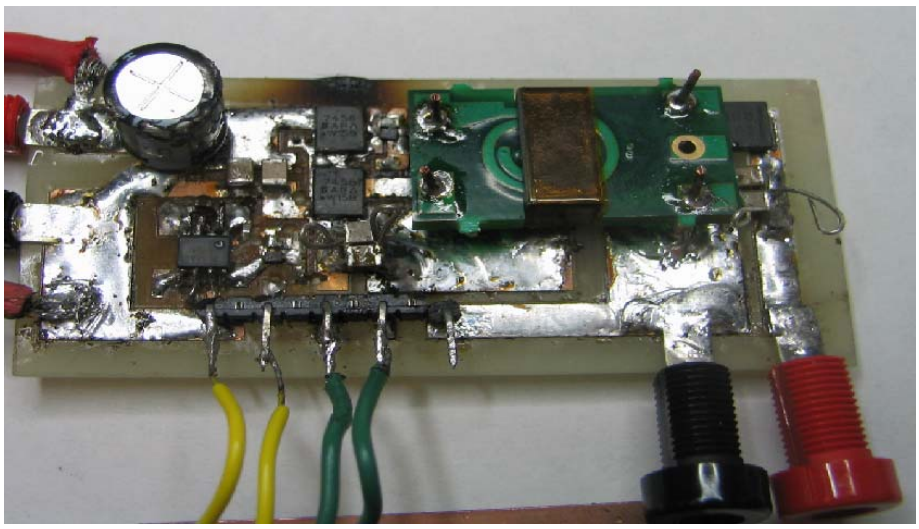


Figure 6.7. Experimental prototype

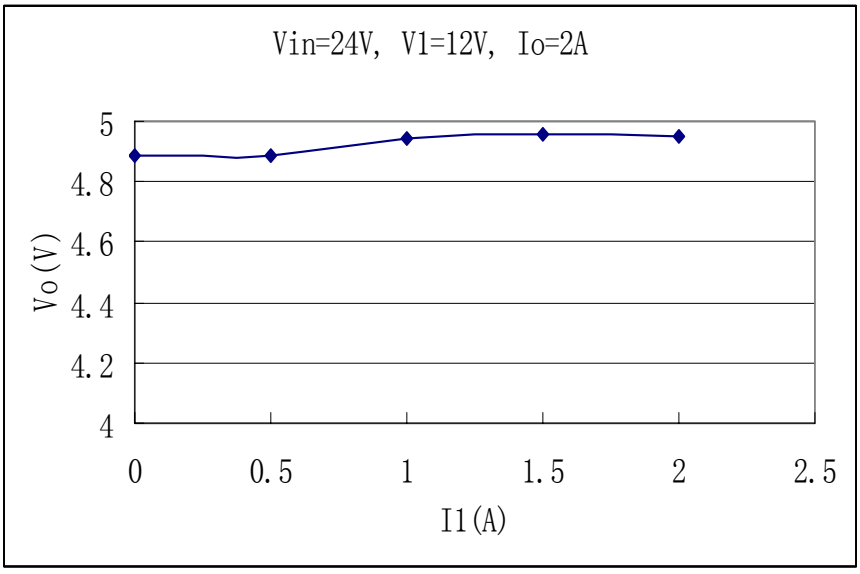


Figure 6.8. Secondary-side output voltage vs. primary-side load change

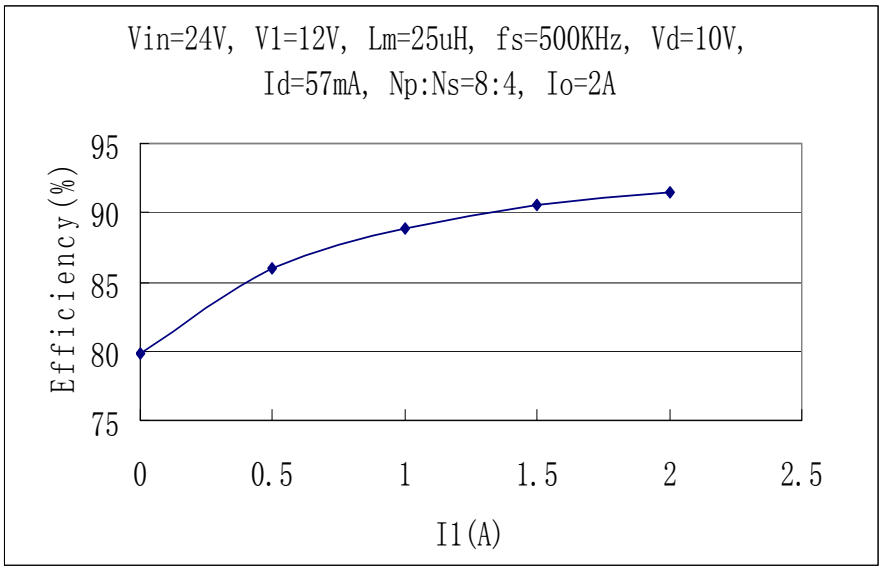


Figure 6.9. Efficiency curve with constant secondary-side load

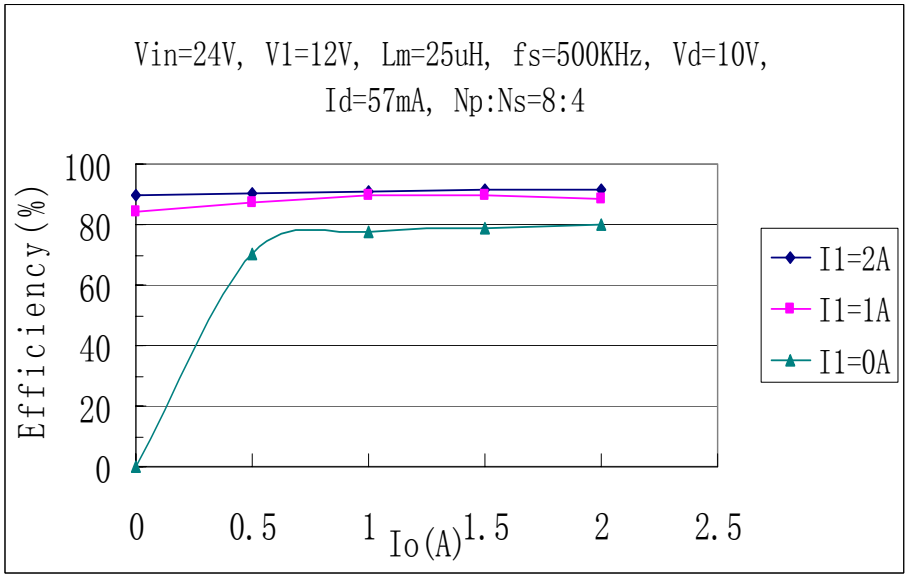


Figure 6.10. Efficiency curve with constant primary-side load

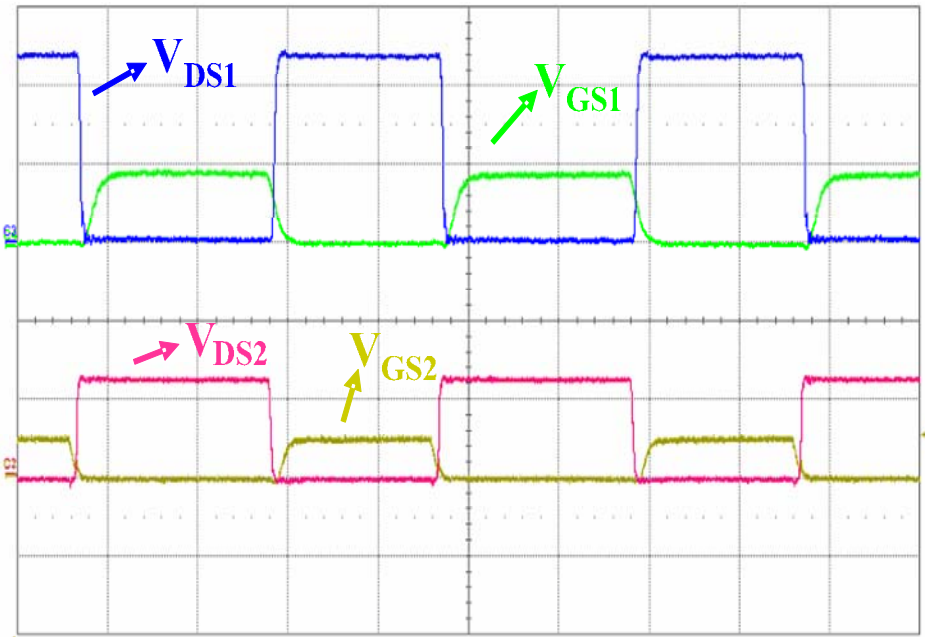


Figure 6.11. ZVS waveforms at I_1=0A and Io=2A

(Top two traces: S_1 (*10V/div*), and bottom two traces: S_2 (*20V/div*))

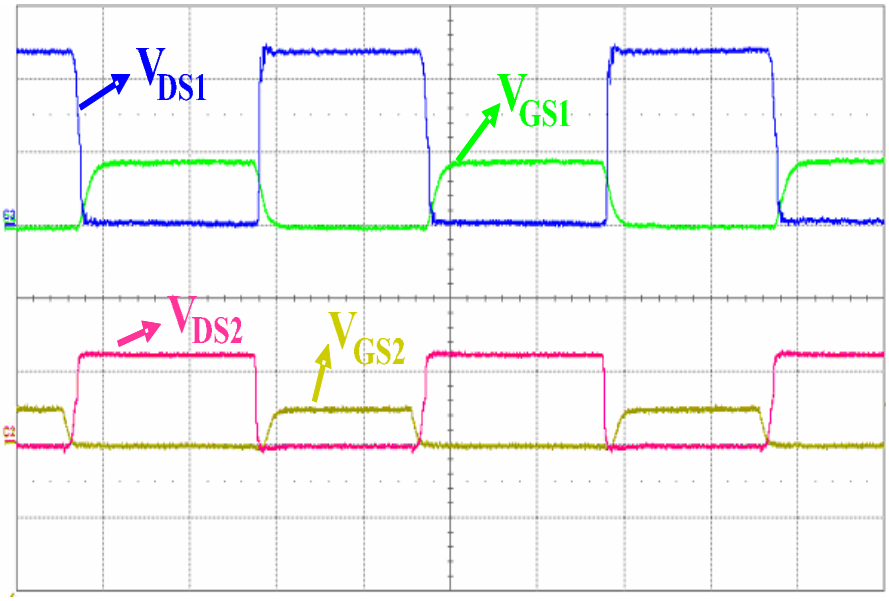


Figure 6.12. ZVS waveforms at I_1=2A and Io=2A

(Top two traces: S_1 (*10V/div*), and bottom two traces: S_2 (*20V/div*))

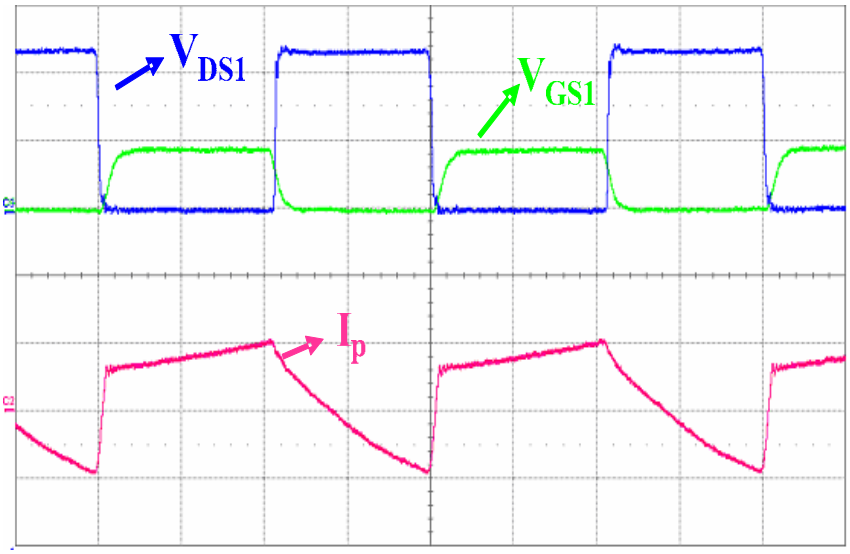


Figure 6.13. S_1 ZVS waveform and i_p waveform at I_1=1A and Io=2A

(Top two traces: S_1 (*10V/div*), and bottom trace: i_p (*2A/div*))

CHAPTER SEVEN: CONCLUSION

7.1 Summary

This dissertation primarily focuses on high-efficiency high-current-density dc-dc converter not only for state-of-the-art industry applications but also for future applications. For telecommunication and computer system applications, low-voltage high-current high efficiency isolated dc-dc converters with high power-density are demanded. Half-bridge dc-dc converter with current-doubler rectification is regarded as a good topology that is suitable for high-current low-voltage applications. There are three control schemes for this topology, symmetrical, asymmetrical and DCS control. In Chapter Two, unified analog and digital state-space models are derived, which are suitable for all three control schemes; for optimization and design of analog and digital compensator, analog and digital small signal model of this topology are developed respectively. A prototype of half bridge dc-dc converter with current doubler rectification is built and tested for typical telecom applications, and digital compensation is designed and implemented on the prototype with the TI DSP chip.

Current doubler rectification technique is widely used in industry for high-current application and is similar to an isolated two-phase buck in term of rectification architecture. Therefore CDR has the same issue of current sharing as two-phase interleaved buck converter. Duty cycle adjustment is an effective and practical solution to current imbalance in non-isolated two-phase buck converter, but it has little effect on balancing the current distribution in the current doubler rectifier. In Chapter Three, one modified current doubler rectifier topology is proposed to achieve passive current sharing that is solely depending on duty cycle. The performance is evaluated with half bridge dc-dc converter; good current

sharing is achieved without additional circuitry.

The powering requirements for on-board module in future telecom/datacom and computing systems are lower voltage and higher current. In Chapter Four, current tripler and current N-tupler rectification topologies are proposed for future high current applications. The proposed rectification technique features good thermal management and well-distributed power dissipation, simplified magnetic design and low copper loss for inductors and transformer due to the fact that the load current is better distributed in three inductors and the rms current in transformer windings is reduced. The operation principle and dc analysis are presented. Theoretical analysis, comparison and experimental results verify that the proposed rectification techniques are candidate topologies for secondary-side rectification in high-current isolated dc-dc converters..

Chapter Five discusses another major challenge in telecommunication and computing applications, which is the fast transient response of the converter to the increasing slew-rate of load current change. In isolated dc-dc converters, primary-side control is widely used in industry and low-speed optocoupler is commonly used for feedback signal. But typically optocoupler only has 10 to 30 KHz bandwidth, and therefore it becomes the barrier of the system transient response. Secondary-side control technique can eliminate the delay of optocoupler to achieve around three to four times higher the system bandwidth and therefore has good dynamic performance to the fast transient of advanced silicon loads. Active-clamp half bridge dc-dc converter with secondary-side control is presented and one industry standard 16^{th} prototype is built and tested; good efficiency and transient response are achieved.

A novel zero-voltage-switching buck-flyback isolated dc-dc converter with synchronous rectification is proposed in Chapter Six for multi-output applications. It can be

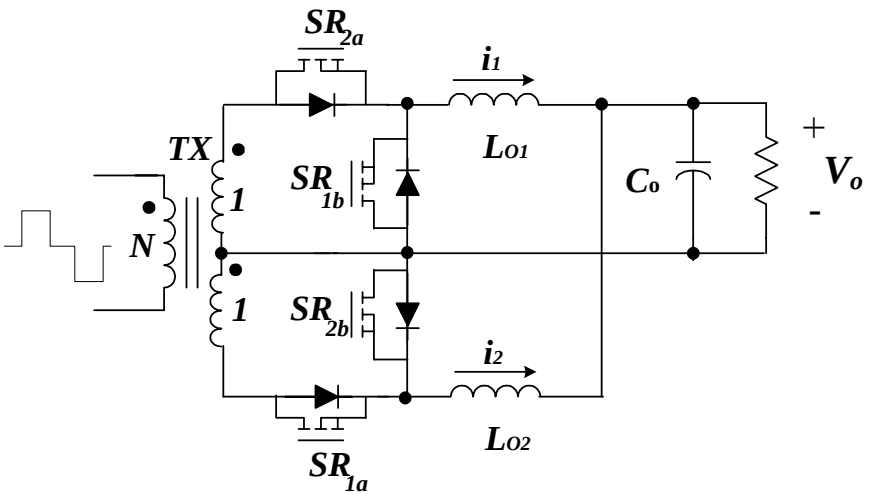
used not only as house-keeping power supplies and standalone power supplies requiring multi-outputs, but also provide solution for start-up issue for secondary-side controlled converter. The operation modes are analyzed quantitatively and dc analysis is discussed, and the design guideline is also provided. The theoretical analyses and experimental results have proved that the proposed converter is more cost-effective and has better efficiency compared to the conventional multi-output flyback converter, active-clamp flyabck and AHB flyback converters.

7.2 Future Work

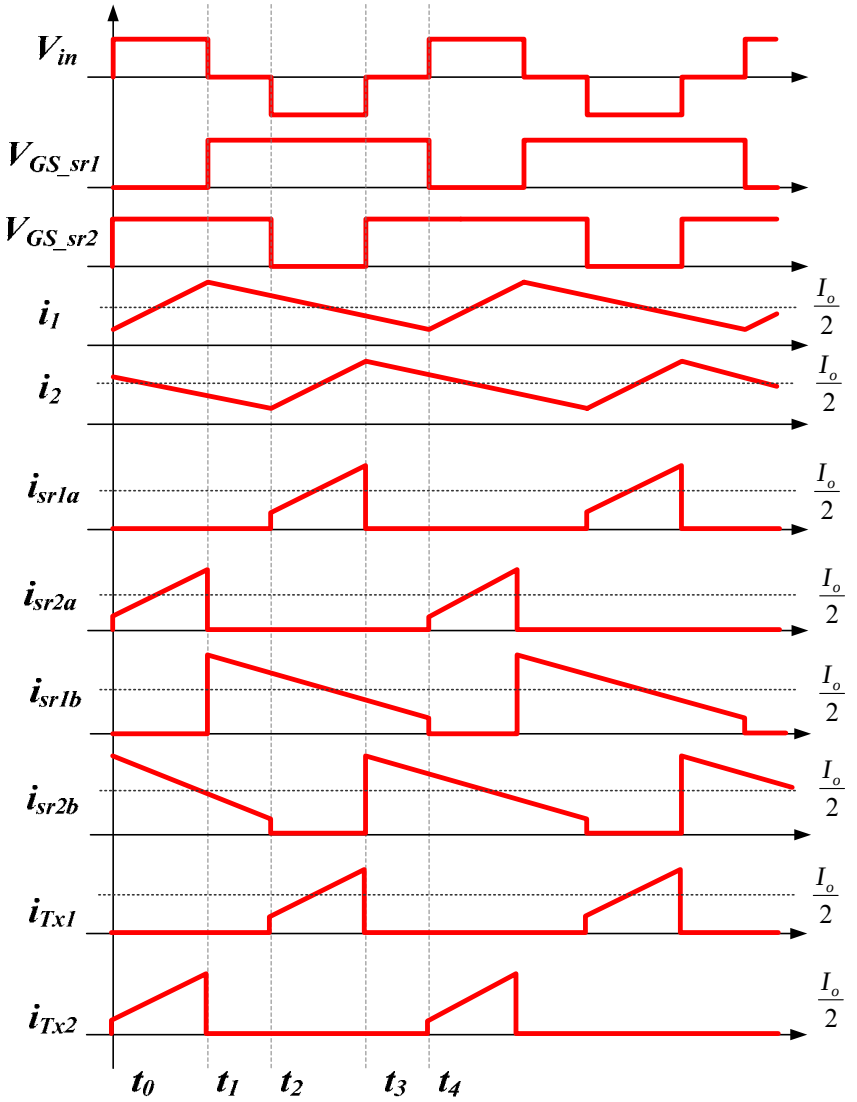
For the current sharing issue in the current doubler rectifier, it is worthwhile to analyze with other primary-side topologies, especially with full-bridge and active-clamp forward where the CDR works in asymmetrical case. Some preliminary result has been published by author in APEC 2006.

For the proposed current tripler rectification techniques, coupling of three output filer inductors has the potential to improve power density and the transient response of the rectifier. It will be a good contribution to find a way to fully integrated transformer and inductors to further improve the current-density and power-density for future high current applications. In addition, it will be interesting to analyze the current tripler operation in DCM and asymmetrical case respectively.

The following two-phase forward rectification topology can be an option for high-current application and it may beat current doubler rectifier when using with active-clamp or asymmetrical half bridge primary-side topologies. The topology and key waveforms is shown in Figure 7.1.



(a) Two phase forward rectifier



Key steady-state operation waveforms

Figure. 7.1. Two phase forward rectifier and its key waveforms for steady-state operation

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