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The Effect Of Carbon Nanotube/organic Semiconductor Interfacial Area On The Performance Of Organic Transistors

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THE EFFECT OF CARBON NANOTUBE/ORGANIC SEMICONDUCTOR INTERFACIAL AREA ON THE PERFORMANCE OF ORGANIC TRANSISTORS

by

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Major Professor: Saiful I. Khondaker

To my parents and my brother

ABSTRACT

Organic field-effect transistors (OFETs) have attracted tremendous attention due to their flexibility, transparency, easy processiblity and low cost of fabrication. High-performance OFETs are required for their potential applications in the organic electronic devices such as flexible display, integrated circuit, and radiofrequency identification tags. One of the major limiting factors in fabricating high-performance OFET is the large interfacial barrier between metal electrodes and OSC which results in low charge injection from the metal electrodes to OSC. In order to overcome the challenge of low charge injection, carbon nanotubes (CNTs) have been suggested as a promising electrode material for organic electronic devices.

In this dissertation, we study the effect of carbon nanotube (CNT) density in CNT electrodes on the performance of organic field effect transistor (OFETs). The devices were fabricated by thermal evaporation of pentacene on the Pd/single walled CNT (SWCNT) electrodes where SWCNTs of different density (0-30/um) were aligned on Pd using dielectrophoresis (DEP) and cut via oxygen plasma etching to keep the length of nanotube short compared to the channel length. From the electronic transport measurements of 40 devices, we show that the average saturation mobility of the devices increased from 0.02 for zero SWCNT to 0.06, 0.13 and 0.19 cm2/Vs for low (1-5 /μm), medium (10-15 /μm) and high (25-30 /μm) SWCNT density in the electrodes, respectively. The increase is three, six and nine times for low, medium and high density SWCNTs in the electrode compared to the devices that did not contain any SWCNT. In addition, the current on-off ratio and on-current of the devices are increased up

to 40 times and 20 times with increasing SWCNT density in the electrodes. Our study shows that although a few nanotubes in the electrode can improve the OFET device performance, significant improvement can be achieved by maximizing SWCNT/OSC interfacial area. The improved OFET performance can be explained due to a reduced barrier height of SWCNT/pentacene interface compared to metal/pentacene interface which provides more efficient charge injection pathways with increased SWCNT/pentacene interfacial area.

ACKNOWLEDGMENTS

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Secondly, I strongly would like to acknowledge Biddut Sarker and Daeha Joung for their help operating the equipment such as e-beam lithography (EBL), e-beam/thermal evaporation, scanning electron microscopy (SEM), atomic forced microscopy (AFM) to fabricate and characterize the nano-scaled devices. I wish them the best of luck continuing their research and beyond for their future career. I would also like to thank all the members in my group, Feras Alzubi, Muhammad Rakibul Islam, and Udai Bhanu. I also would like to thank the members of staffs and faculties at Nanoscience Technology Center (NSTC) and department of physics in University of Central Florida (UCF).

Last of all, my special thanks have to to my family for their endless love and support.

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LIST OF ABBREVIATIONS

a-Si:H – armorphous silicon hydrogenated

CNT – carbon nanotube

DEP – dielectrophoresis

DI water – di-ionized water

EBL – electron beam lithogrphy

HOMO – highest occupied molecular orbital

IPA - isopropyl alcohol

LUMO – lowest occupied molecular orbital

N_2 - nitrogen

OFET – organic field-effect transistor

OSC – organic semiconductor

P3HT – poly (3-hexylthiophene)

PMMA - Polymethylmethacrylate (Acrylic)

RFID – radio-frequency identification

SEM – scanning emission microscopy

Si – silicon

SiO_2 – silicon di-oxide

SWCNT – single-walled carbon nanotube

CHAPTER 1 : INTRODUCTION

1.1 Motivation

Organic field-effect transistors (OFETs) have attracted a great deal of research interests in the field of both academy and industry owing to their flexibility, transparency, low-cost and large-area.[1-4]

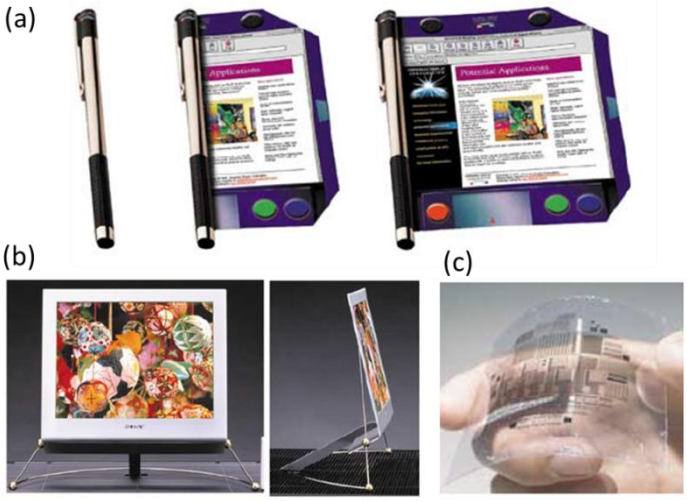

Figure 1 (a) A conceptual view of future organic flexible display which can be rolled into a pen-like device when not in use. Images courtesy of Universal Display Corp. (b) A full color, 13-inch OLED display with only 2mm thick. (c) A conceptual view of integrated circuits on flexible, and transparent plastic substrate. Photograph courtesy of T. Jackson, Penn state Univ. [ref. 2]

OFETs can be fabricated on glass or inexpensive flexible plastic substrates with lower temperature and considerably lower cost compared to amorphous silicon hydrogenated (a-Si:H) devices. These advantages are able to have substantial impacts on developing next generation

organic electronics such as flexible display, flexible solar cell, or radio-frequency identification (RFID) tags as shown in Figure 1.

The organic semiconducting materials have been used as active channel materials for OFETs including sublimed and solution-processed semiconductors. The most widely used organic materials for semiconducting layer of OFETs are pentacene and poly (3-hexylthiophene) (P3HT). Boundless choices of active materials and potentials can open up the further possibilities for practical applications of OFETs.

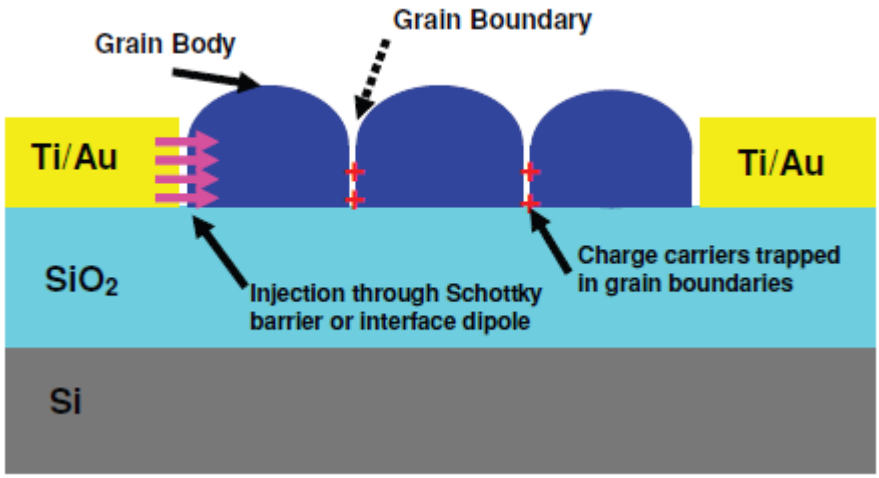

Figure 2 Schematic of bottom-gated organic field-effect transistors (OFETs) showing the factors that limits the performance of OFETs using the metal (Pd) electrodes.[ref. 25]

As the charge-injecting electrode for OFETs, conventional noble metals such as Au, Ti, Pt, and Pd have been used due to their chemical stability and work function, which can match the highest occupied molecular orbital (HOMO) of p-type organic semiconductors. However, the use of metal electrodes can form several interfacial barriers at metal electrode/organic semiconductor (OSC) such as the discontinuity in morphology, dipole barriers, and Schottky barriers, which

cause low charge injection at electrode/OSC interface and thus reduce the performance of OFETs.[5-9] Figure 2 shows two main factors that limits the performance of OFETs. One is low charge injection at metal electrodes and OSC interface. The other is large grain-boundary resistance by trapping charge carriers in grain boundaries from organic semiconductor molecules. In order to overcome these limitations, carbon nanotubes (CNTs) have been suggested as a promising electrode material for organic electronic devices.[10-15]

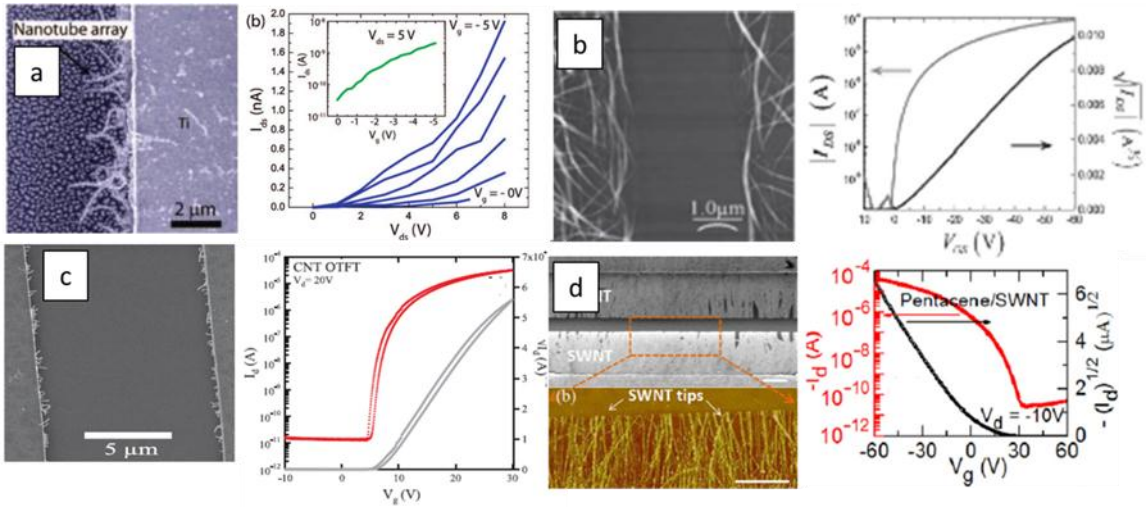

Figure 3 Different studies of OFETs using CNT electrodes show improved charge injection properties and different densities of CNT in the electrodes. (a) [ref. 11], (b) [ref. 12], (c) [ref. 26], and (d) [ref. 13]

Recently, several research groups have reported the device performance of OFETs using CNT electrodes as seen in Figure 1.3.[10-18] In these studies, CNT electrodes were fabricated with various techniques using either individual CNT,[10-11] random network CNTs,[15-17] CNT/polymer composite,[12] or aligned array CNTs.[13,14,18] The density of CNT in the electrodes is also various for each studies from 1 to 30 per μm. These studies also suggested that the device performance of OFETs using CNT electrode is enhanced compared to that of OFETs using metal electrodes.

However, one important question is still unanswered: whether the density of CNT in the electrode has any role in the performance of the fabricated OFETs and how much improvement can be possible using CNT electrode? The density of CNT in the electrodes can control the interfacial area between the CNTs and OSCs. A low density CNTs forms small CNT/pentacene interfacial area while high density CNTs creates large interfacial area with OSC. It has been suggested from the molecular dynamics simulation and NMR spectroscopy that a π-π interaction exists between CNT/OSC.[19-21] In addition, CNT has a field emission properties due their one-dimensional structure.[22] These theoretical and experimental studies suggest that charge injection should depend on the CNT/OSC interfacial area and that one can improve the performance of OFETs by maximizing CNT/OSC interfacial area. However, no such investigation has been reported yet. Such a study is of great importance for achieving the overreaching goal of the CNT electrodes in organic electronics.

Therefore, we systematically have investigated the effect of CNT/OSC interfacial area on the performance of the OFETs by varying the density of CNT in the electrode. The devices were fabricated by thermal evaporation of pentacene on the Pd/single-walled carbon nanotube (SWCNT) electrodes where SWCNTs of different density (0-30 /μm) were aligned on Pd using dielectrophoresis (DEP) and cut via oxygen plasma etching to keep the length of nanotube short compared to the channel length. From the electronic transport measurements of 40 devices, we show that the average saturation mobility of the devices increased from 0.02 for zero SWCNT to 0.06, 0.13 and 0.19 cm2/Vs for low (1-5 /μm), medium (10-15 /μm) and high (25-30 /μm) SWCNT density in the electrodes, respectively. The increase is three, six and nine times for low, medium and high density SWCNTs in the electrode compared to the devices that did not contain

any SWCNT. In addition, the current on-off ratio and on-current of the devices are increased up to 40 times and 20 times with increasing SWCNT density in the electrodes. Our study shows that although a few nanotubes in the electrode can improve the OFET device performance, significant improvement can be achieved by maximizing SWCNT/OSC interfacial area. The improvement can be explained due to a reduced barrier height of SWCNT/pentacene interface compared to metal/pentacene interface which provides more and more efficient charge injection pathways with increased SWCNT/pentacene interfacial area.

1.2 Organization of thesis

In Chapter 2, I will discuss the basic structure and working principle of OFETs. In addition, I will compare the device performance of OFETs using metal electrode and CNT electrode, showing several other groups' study related to transport properties of OFETs using CNT electrode compared to metal electrode.

Chapter 3 will introduce the device fabrication details of making different density CNT electrodes using dielectrophoresis (DEP) assembly. Then, the fabrication of OFETs using different density of CNT electrodes will be more discussed in detail.

Chapter 4 will show electron transport measurement of OFETs using different density of CNT electrodes compared to bare Pd electrode. The output/transfer characteristics of OFETs will be discussed depending on the different density of CNT electrodes compared to bare Pd electrode.

Finally, in Chapter 5, I will conclude the results and suggest future works.

CHAPTER 2 : BACKGROUND

2.1 Organic field-effect transistors (OFETs)

The schematic diagram of organic field-effect transistors (OFETs) is described in Figure 4 (a).

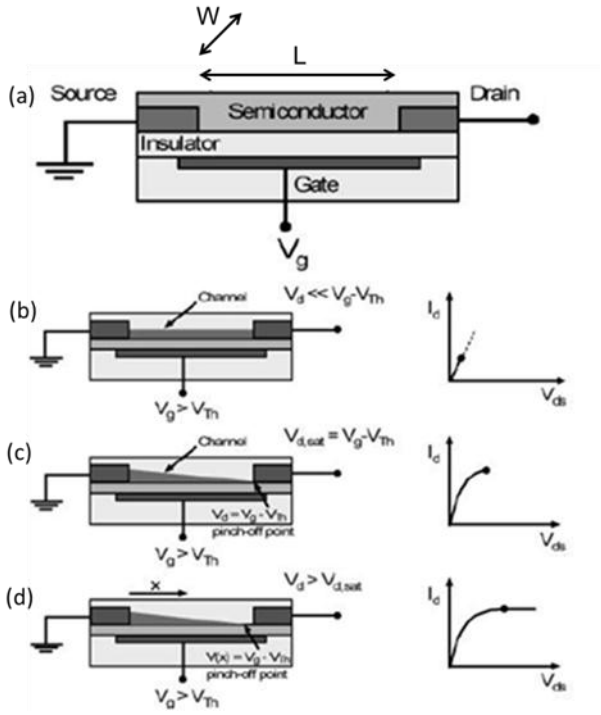

Figure 4. (a) The basic structure of bottom-gated OFETs. It has 5 components: source, drain electrode, insulating dielectric layer, gate electrode, and organic semiconductor. Channel length (L) and channel width (W) was described in the schematic diagram. The working principle of OFETs and current-voltage characteristics are illustrated in (b)-(d). (b) linear, (c) the beginning of saturation at pinch-off, and (d) saturation regime. [ref. 27]

Basically, OFETs have three terminals: source, drain and gate. Organic semiconducting materials can be placed between source and drain electrodes. The charge carrier density can be modulated by applying the gate voltage. The insulating dielectric layer is placed in the middle of the structure. We use the bottom-gated configuration for OFETs. Figure 4 (b)-(d) shows the basic operation of OFETs showing linear and saturation current-voltage characteristics. In the linear regime, the drain current (I_d) is directly proportional to gate voltage (V_g), and the field-effect mobility in linear regime (μ_{lin}) can be extracted from I_d-V_g curve at fixed bias voltage (V_d) with the equation of $\mu_{lin} = (dI_d/dV_g)(L/WC_iV_d)$. The field-effect mobility in the saturation regime (μ_{sat}) can be extracted using the equation of $\mu_{sat} = (2LI_{d,sat})(WC_i(V_g-V_T)^2)$ because the square root of the saturation current is proportional to the V_g.

2.2 Interfacial barrier at metal electrode/OSC interface

One of the major factors which limit the performance OFET is large interfacial barrier from the interface between metal electrodes and organic semiconductor (OSC). This causes low charge injection from the metal electrodes to OSC and finally reduces the performance of OFETs.[5-6] The interfacial barriers can be caused by several factors such as the discontinuity in morphology, dipole barriers, and Schottky barriers.[7-9]

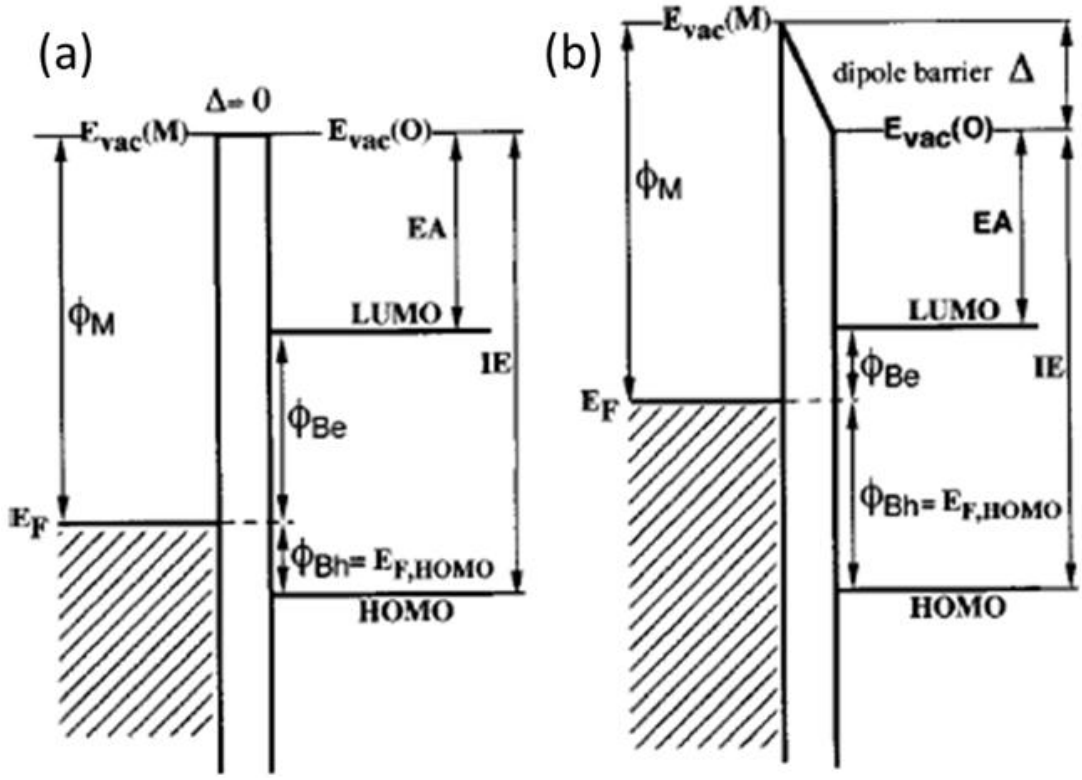

Figure 5. The schematic diagram of energy level difference between metal electrode and organic semiconductor (a) without and (b) with an interfacial dipole barrier. [ref. 8]

Figure 5 shows the schematic of metal electrode and OSC interface without and with dipole barrier, which is originated when the vacuum level of the material is shifted. The variety of mechanisms of interfacial dipole barrier between metal electrode/OSC is shown in Figure 6 (a)-(f). Schottky barrier is originated from a difference of energy level between work function of metal electrode and highest occupied molecular orbital (HOMO)/ Lowest occupied molecular orbital (LUMO) level at OSC. The presence of Schottky barrier at metal electrode/OSC interface makes non-ohmic behavior at low bias, which is meant to be large contact resistance and low charge injection efficiency.

In order to overcome those challenges of low charge injection and large interfacial barrier between metal electrode and OSC, carbon nanotubes (CNTs) have been suggested as a promising electrode material for organic electronic devices.[10-15]

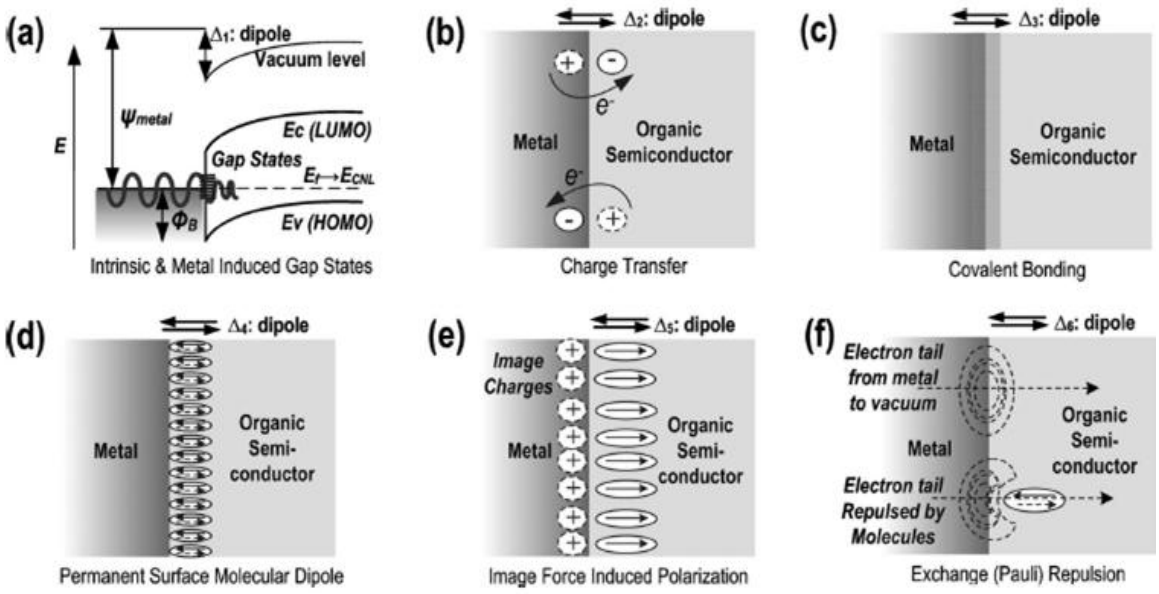

Figure 6. The different types of dipole barrier formation at metal electrode/organic semiconductor interface. [ref. 28]

2.3 Enhanced charge injection at CNT electrode/OSC interface

Carbon nanotubes (CNTs), formed by rolling up graphite sheet in three-dimension (Figure 7.), have been suggested as promising electrode materials for OFETs.

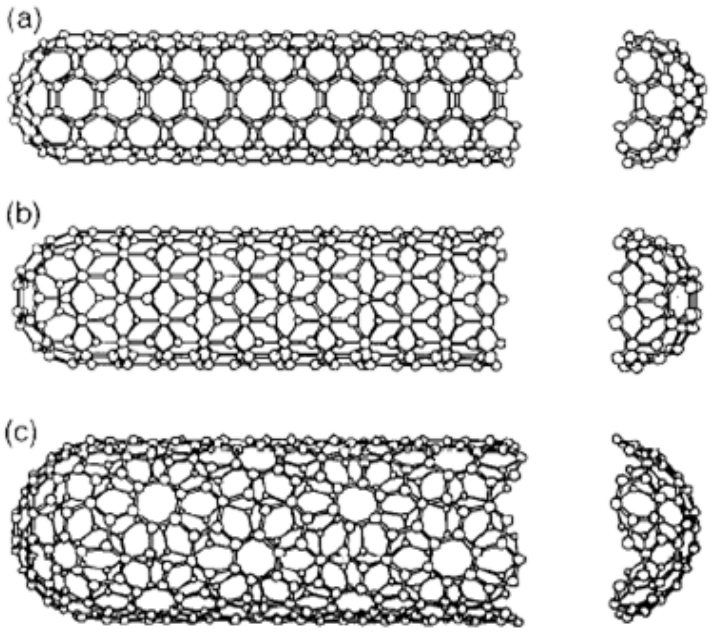

Figure 7. The schematic theoretical diagram of CNT structure. The properties of CNTs can be decided depending on its chirality. (a) armchair, (b) zigzag, and (c) chiral. The actual tubules shown in the figure correspond to (n,m) values of : (a) (5,5), (b) (9,0), and (c) (10, 5). [ref. 29]

The physical structure of CNT is decided depending on the specific angle of rolling a sp^2 bonded sheet into cylindrical shape. This angle is named 'Chiral angle', and the electronic properties of CNTs is provided based on types of nanotube chirality. As seen in Figure 7, 'armchair' nanotubes show metallic behavior, and 'zigzag' nanotubes show semiconducting behavior.

Due to their transparency, flexibility, low-cost, solution-processed and easy-processing, CNTs have been spotlighted as a material which can be integrated to future flexible display, flexible solar cell and many other flexible/transparent electronic applications.[1-4] Owing to its unique one-dimensional structure, CNTs have a field-emission properties and high electrical conductivity and chemical stability. Strong π-π interaction between the side walls of CNTs and

organic semiconductor and high work function of CNTs (~5.0eV) is the other benefits of using CNTs as an electrode material for OFETs.[10-17]

CHAPTER 3 : DEVICE FABRICATION

3.1 Fabrication of electrodes

The devices were fabricated on heavily doped silicon (Si) substrates coated with a thermally grown 250 nm thick silicon di-oxide (SiO2) layer. Palladium (Pd) electrodes of 5 μm x 25 μm were fabricated using standard electron beam lithography (EBL) process. The detail fabrication steps illustrate in Figure 8.

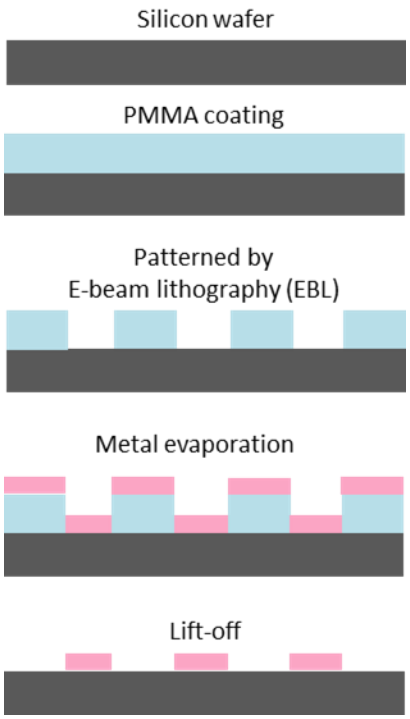

Figure 8. Schematic diagram of electrode pattern fabrication on the Si substrate. First, PMMA is spincoated on the Si substrate. Then, using EBL the pattern of electrode is defined. The desired metal is evaporated. Lift-off is done using action followed by IPA, DI water washing and drying with N_2 gun.

The single layer resist of PMMA (950K, C2, 2%, MicroChem) is spin-coated on the Si substrate at 4000 rpm for 1min, and then placed on hot plate to bake during 15 min at 180 ˚C. The thickness of PMMA is 100 to 150 nm. Then, the electrode patterns are defined using EBL (Zeiss Ultra 55 SEM) exposed with an area dose of ~ 350 μC/cm^2 and voltage of 28kV. As for the developing process, the devices are immersed into MIBK:IPA (1:3) for 75 sec and IPA for 15 sec followed by N_2 dry. The desired metals, such as Au, Pd, Pt, Al, Ni, Cu, Ti, Ag and other metals, depending upon their purpose, can be deposited by thermal/e-beam evaporation. For our device, Palladium (Pd) is deposited by e-beam evaporation. Finally, the device is place into Acetone for 3-4 hours to remove the rest of PMMA followed by IPA, DI water washing and N_2 dry.

3.2 Assembly of CNT using dielectrophoresis

Several methods to align carbon nanotubes (CNTs) have been introduced in recent years. The direct growth via chemical vapor deposition (CVD) is one of the examples; however, very high temperature (~ 900˚C) is required to transfer the aligned array of CNTs to substrate.

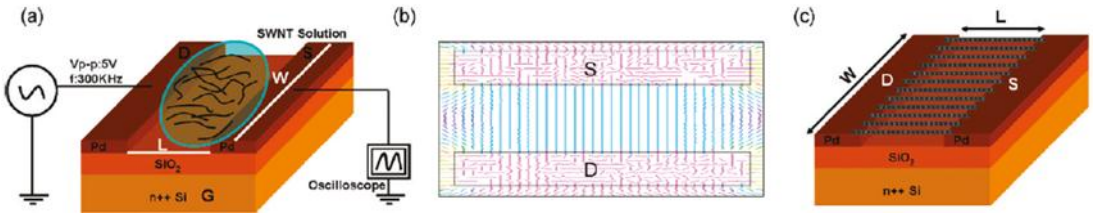

Figure 9. The schematic diagram of DEP assembly of CNTs. (a) The CNT solution is dropped between source and drain electrode. (b) The simulation pictures showing electric field formation when AC voltage is applied between source and drain electrode. (c) After applying AC voltage, CNTs are aligned along E-field between source and drain electrode. [ref. 23]

Since solution-processed assembly is easy-processing at room temperature, the post-growth techniques such as Langmuir-Blodgett assembly, bubble blown assembly, evaporation-driven self-assembly, spin coating assisted alignment and contact printing have been introduced. However, the number of aligned CNT arrays is from 1 to 10 per um. In order to align high dense CNT arrays, dielectrophoresis (DEP) assembly has been developed. 2D, 1D, and 0D nanomaterials can be aligned via DEP at desirable position of the devices. Figure 3.2 describes the schematic of DEP assembly. The basic working principle of DEP is very simple, low-cost, solution-processed and easy-processing. [24]

3.3 Fabrication of making different density CNTs in the electrodes

The single-walled carbon nanotubes (SWCNTs) of different linear densities of 0-30/um were assembled between the Pd electrodes via DEP using a high quality SWCNT aqueous solution obtained from Brewer Science. Figure 10. shows output/transfer characteristics of this SWCNT solution showing metallic behavior.

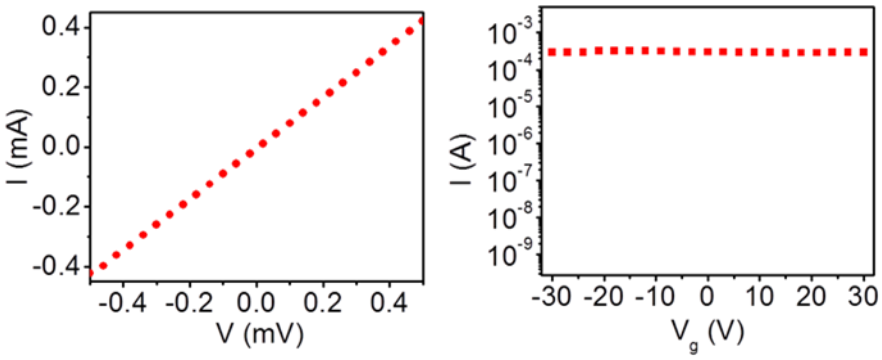

Figure 10. Electrical characterizations of SWCNT aligned arrays before cutting. (a) Current (I_d) –voltage (V_d) and (b) current (I_d) – gate voltage (V_g) characteristics at fixed V_{ds} = 0.5V.

Figure 11. illustrated the fabrication steps of making different density of SWNT electrodes. In short, a 3 µl SWCNT solution was dropped onto Pd pattern and an AC voltage of 5 V with a frequency of 2 MHz were applied for 30 sec. Due to the DEP force, the SWCNTs are aligned in arrays between the Pd patterns. The linear density was controlled by varying the concentration of SWCNT solution by diluting the original nanotube solution (~ 50 µg/mL) with deionized (DI) water. The SWCNT arrays were then cut by spin coating PMMA, defining a 4.4 µm (L) x 25 µm (W) window in the middle of the channel using standard EBL, and subsequent oxygen plasma etching. Finally, the chips are kept into chloroform and cleaned with isopropanol (IPA) and deionized (DI) water

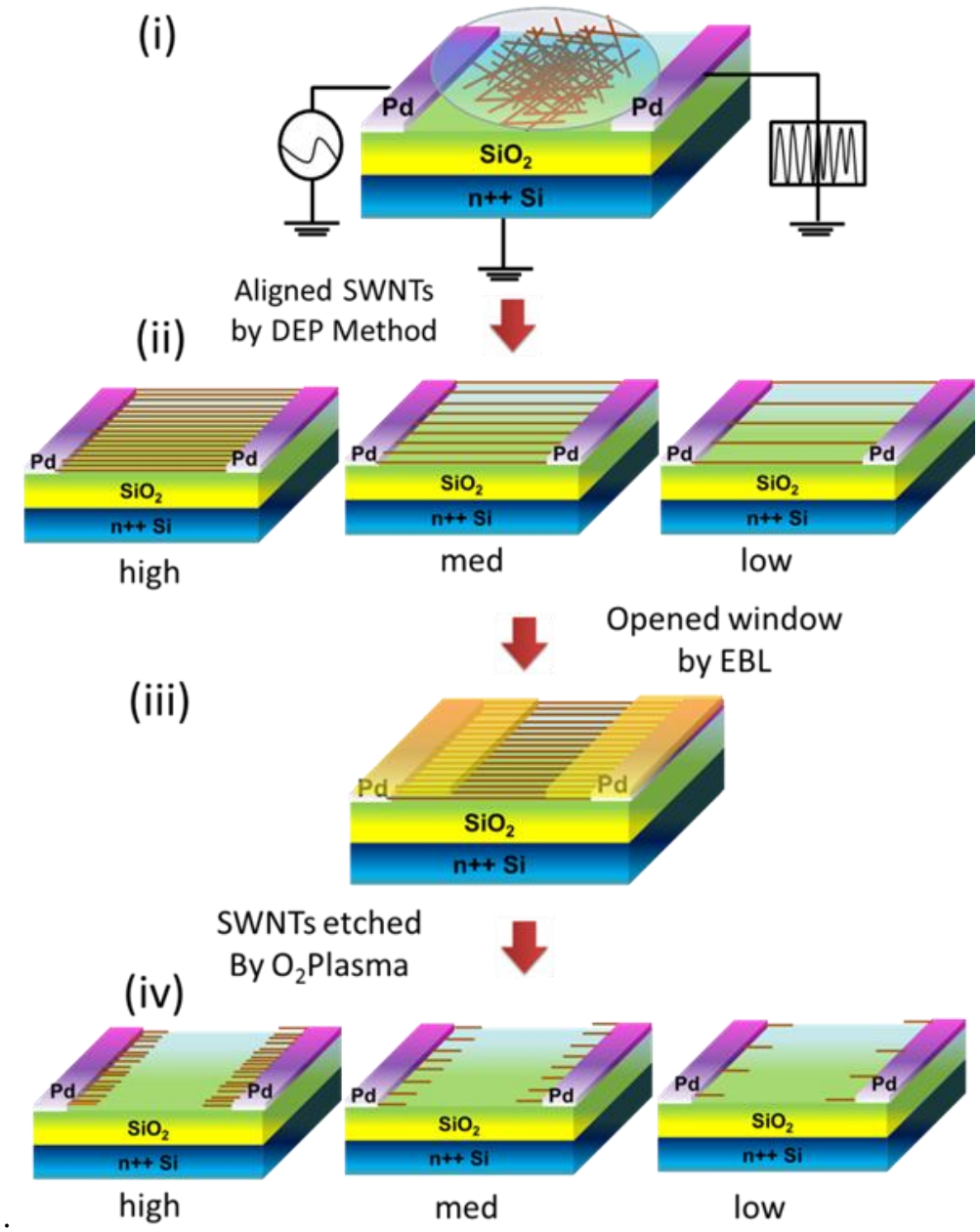

Figure 11. Schematic diagram of SWNT electrode fabrication with different density of SWNTs in the electrode. (i) Assembly of the aligned array SWCNTs by DEP assembly between Pd electrodes. Linear density of the SWCNT arrays was controlled by tuning the SWCNT solution concentration (iii) Opened a window on the SWCNTs array via electron beam lithography and (iv) etch the SWCNTs by oxygen plasma.

Figure 12. (a) shows representative scanning electron microscopy (SEM) images of the part of the electrodes containing an average of 30, 13 and 2 SWCNT/um as well as a bare Pd electrode.

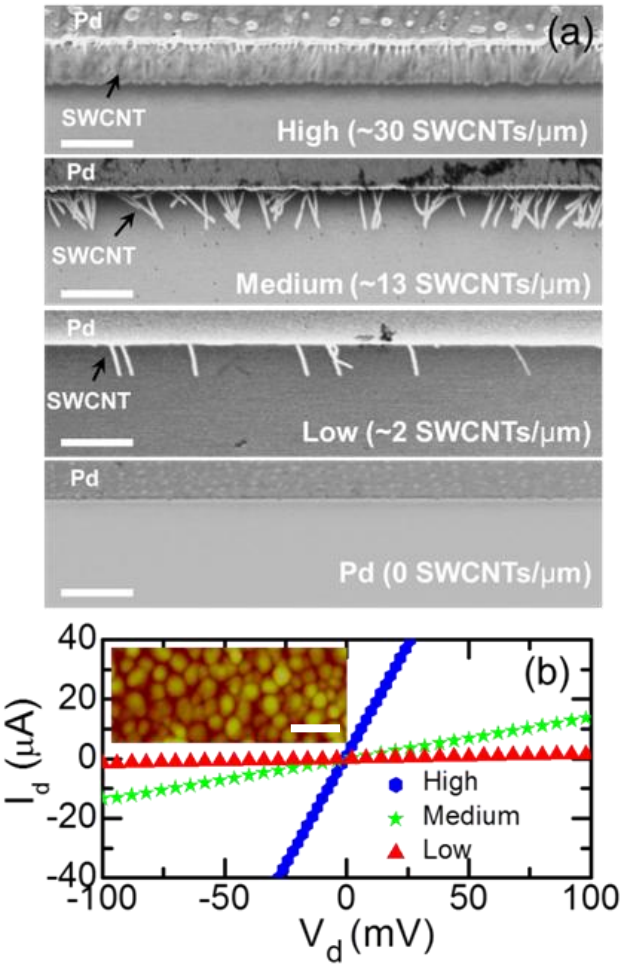

Figure 12. (a) SEM images of the edge of the electrodes with high, medium, low density SWCNTs and Pd electrode. (b) Current-voltage characteristics of the electrodes with high, medium and low density SWCNTs before cutting. Inset : AFM images of pentacene film. The scale bar indicates 500nm for each picture.

The average linear densities of the arrays were calculated by counting the total number of SWCNTs from the SEM images and then dividing it by the channel width. Figure 12. (b) shows

representative current-voltage (I-V) characteristics of the arrays before cutting. The typical resistances for the arrays with high, medium and low nanotube density are 0.68 kΩ, 7.19 kΩ, and 6.33 kΩ, respectively. This indicates the resistance of the arrays decreases with increasing the density of the nanotubes in the arrays.

3.4 Fabrication of OFETs using CNT electrodes

The pentacene film with thickness of 30 nm was thermally deposited in vacuum at a pressure of 2×10^{-6} mbar.

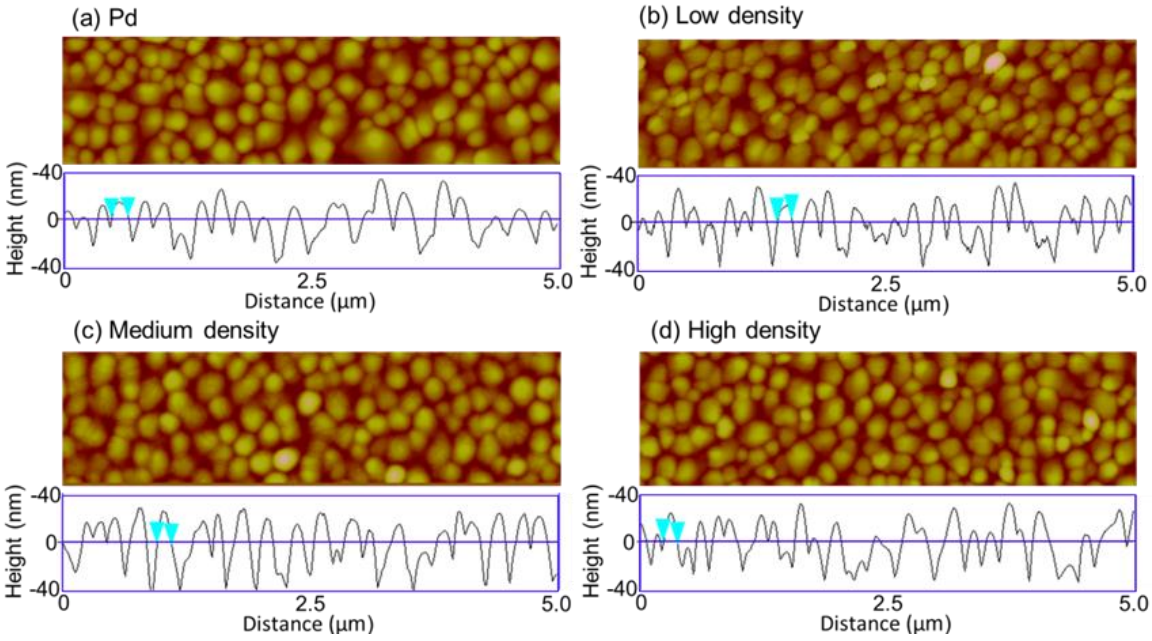

Figure 13. Morphology of pentacene film. Atomic force microscopy (AFM) images the deposited pentacene film on the electrodes. (a) bare Pd (no SWCNTs), (b) low, (c) medium and (d) high density SWCNTs in the electrodes. The height analysis of these films at the electrode/pentacene interfaces shows the morphology of the films are similar with typical pentacene grain size and rms surface roughness with ~150nm and ~3.5nm.

In order to minimize the device to device fluctuation from the active materials morphology, all of the pentacene films were deposited under identical conditions. The

morphological investigation using atomic force microscopy (Figure 12 (b), inset) showed that all the films have similar morphology with an average grain size of ~150 nm (Figure 13). For a fair comparison of the device performances in terms of nanotube density in the electrodes (different interfacial areas) and to obtain statistically meaningful results, we classified the devices into four categories with a narrow range of SWCNT densities: high (25-30 /μm), medium (10-15 /μm), low (1-5 /μm) and Pd (zero SWCNT) only.

CHAPTER 4 : ELECTRON TRANSPORT MEASUREMENT

4.1 Experimental Set-up

The electrical transport of CNT array is measured using DL instruments 1211 current preamplifier and Ketihly-2400 source meter interfaced with LabView program. The electronic properties and characterization of OFETs were performed using Hewlett-Packed (HP) 4145B semiconductor parametric analyzer interfaced with LabView program. This equipment is connected to a probe station inside an enclosed glove box system with N_2 gas flow as shown in Figure 14. For our measurements of OFETs, a total number of 40 devices were investigated with each different density.

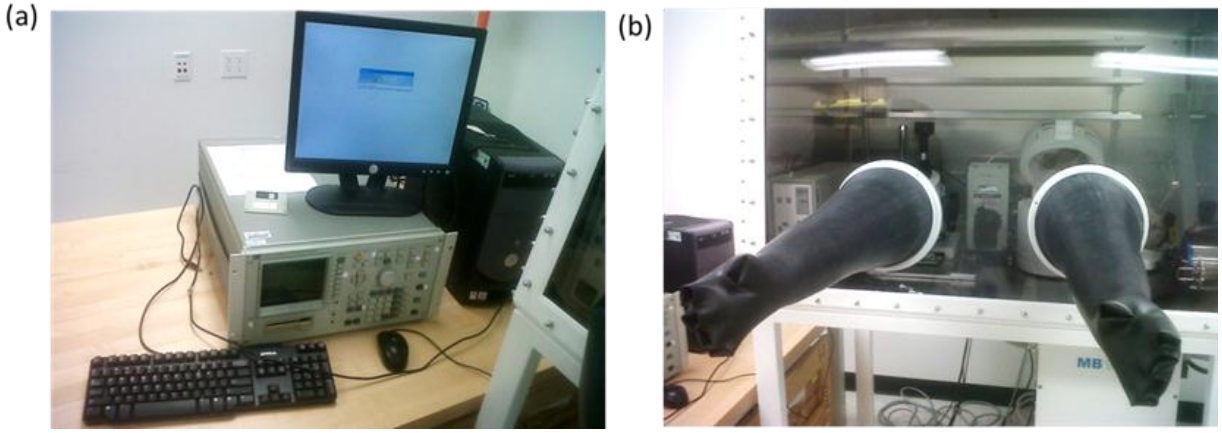

Figure 14. Experimental set-ups for electrical measurements of OFET devices. (a) The devices are measured using Hewlett Packed (HP) 4145B semiconductor parametric analyzer. This is connected to a probe station inside glove box system, which is filled with N2 gas flow as seen in (b).

4.2 Output/Transfer characteristics of OFETs

In order to investigate the effect of SWCNT density in the electrodes, electrical measurement is performed. Figures 15. (a)-(d) show the drain current (I_d) *vs* source-drain bias voltage (V_d) curves (output characteristics) at different gate- voltages (V_g) for our best devices with zero, low, medium and high SWCNTs in the electrodes.

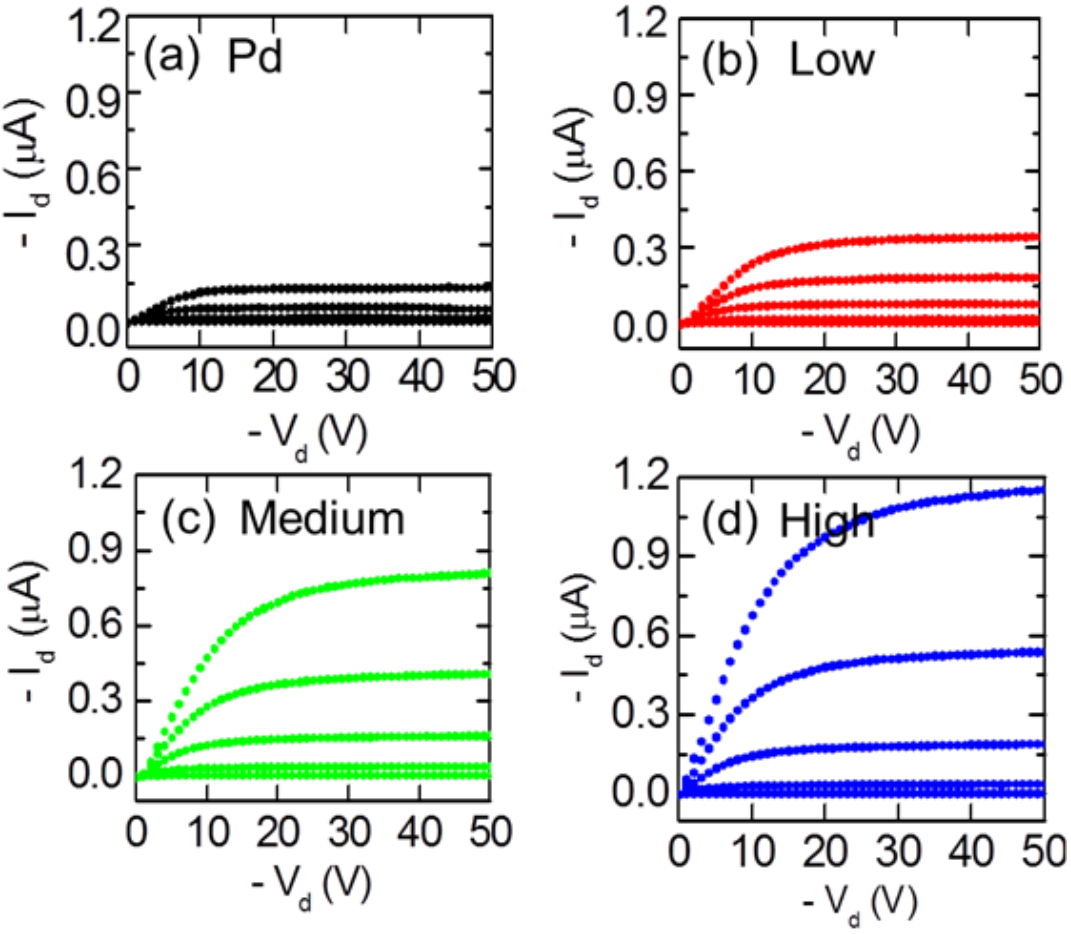

Figure 15. Output characteristics (I_d-$V_d$curve) of pentacene transistors at Vg = 0, -5, -10, -15 and -20V (bottom to top) for (a) zero, (b) low density, (c) medium density, and (d) high density SWCNTs in the electrodes.

All the devices show a good gate modulation with linear behavior at low V_d and saturation behavior at higher V_d, typical of p-channel OFETs. For comparison of device characteristics, we plotted all the curves in the same scale. From here, we see that the output current significantly increases with increasing the SWCNT density in the electrodes. The output current (at V_d = -50V and V_g = - 20V) of the devices with zero SWCNTs is 0.15 μA, whereas it is 0.34 μA, 0.81 μA and 1.15 μA for the devices with low, medium and high density SWCNTs in the electrodes. The output current is twice for low density and nine times for the high density SWCNTs compared to the device without any SWCNTs. Since the morphology of all the devices are similar, the increase of output current with increasing SWCNT density clearly show that the interfacial area at the SWCNTs/pentacene has significant impact on the output characteristics of the devices.

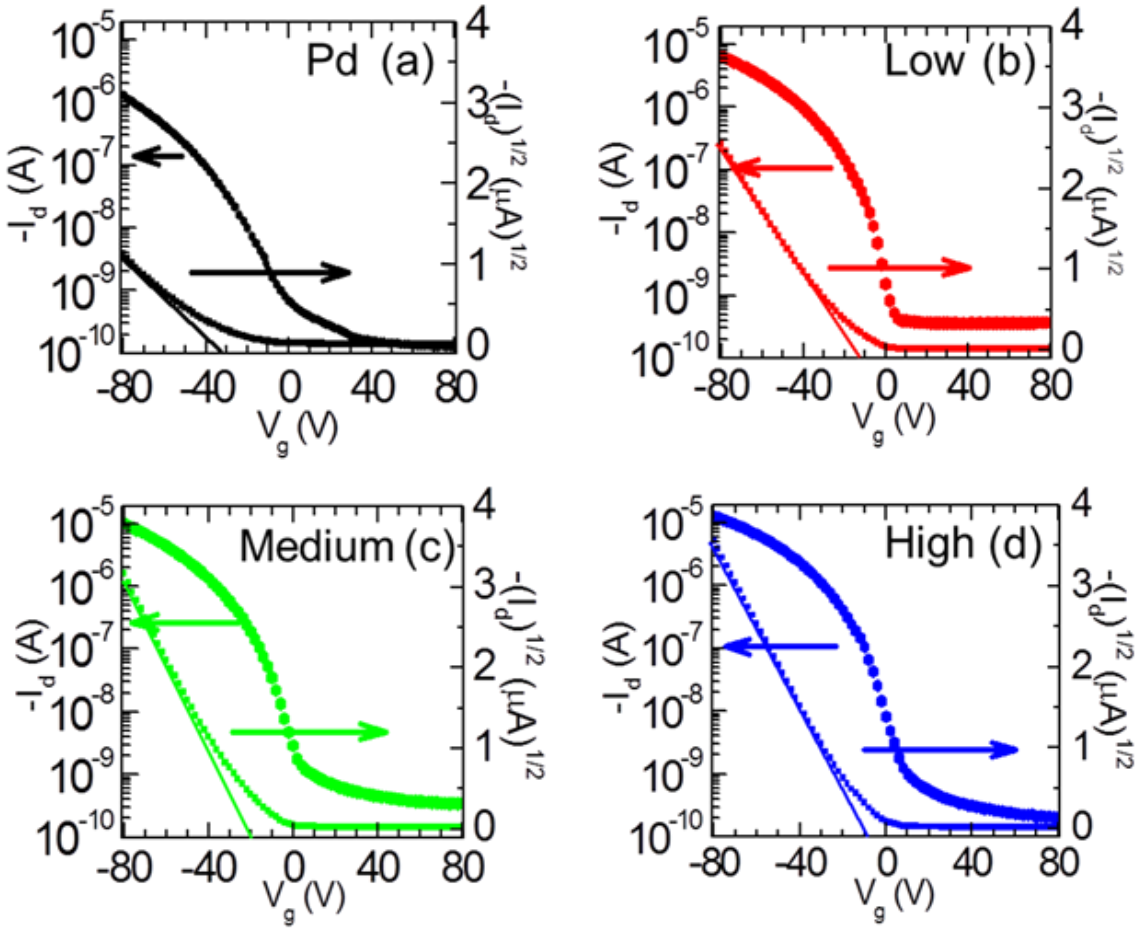

Figure 16. Transfer characteristics (I_d-V_g) of pentacene transistors at V_d = -50 V (left axis) and $(I_d)^{1/2}$ (right axis) of the devices with (a) zero, (b) low density, (c) medium density, and (d) high density SWCNTs in the electrodes.

To further investigate the effect of the interfacial area on the device performance, we also measured the corresponding transfer curves (I_d -V_g) of the same devices at V_d = -50 V (as seen in Figure 16. (a)-(d)) and at V_d = -10 V and calculated the field effect mobility (μ), on-off ratio (I_{on}/I_{off}) and on-current (I_{on}) of the devices. The linear mobility, μ_{lin} (at V_d = -10 V) and saturation mobility, μ_{sat} (at V_d = -50 V) are extracted using the standard formula,[18] $\mu_{lin} = (L/WC_iV_d)(dI_d/dV_g)$ and $\mu_{sat} = (2LI_{d,sat})/(WC_i(V_g-V_T)^2)$, respectively; where $I_{d,sat}$ is saturation

current, and C_i is the gate dielectric capacitance (13.8nF/cm^2). The maximum μ_{sat} (maximum μ_{lin}) of the devices for zero, low, medium and high densities SWCNTs in the electrodes are 0.05 (0.03), 0.10 (0.06), 0.19(0.13), 0.29 (0.19) cm2/Vs, respectively (see also Table 1).

Table 1. Summary of all measured devices. The saturation mobility (μ_{sat}), linear mobility (μ_{lin}), current on-off ratio (I_{on}/I_{off}) and on-current (I_{on}) for the devices with zero, low, medium, high density.

	Bare Pd (0 SWCNTs/μm)	Low (1-5 SWCNTs/μm)	Medium (10-15 SWCNTs/μm)	High (25-30 SWCNTs/μm)
μ_{sat} (max, average)	0.05 cm²/Vs (0.02 ± 0.02)	0.10 (0.06 ± 0.03)	0.19 (0.13 ± 0.06)	0.29 (0.19 ± 0.07)
μ_{lin} (max, average)	0.03 cm²/Vs (0.01 ± 0.01)	0.06 (0.03 ± 0.02)	0.13 (0.08 ± 0.03)	0.19 (0.11 ± 0.04)
Ion/Ioff (max, median)	$9.6x10^3$ ($1.5x10^3$)	$1.8x10^4$ ($4.5x10^3$)	$3.1x10^4$ ($2.0x10^4$)	$1.1x10^5$ ($5.5x10^4$)
Ion (max, median)	3.3 μA (0.6 μA)	10.8 (4.1)	12.8 (8.3)	14.2(11.8)

This demonstrates that the mobility of the devices also increases with increasing SWCNT/pentacene interfacial area. The maximum μ_{sat} is 100%, 280%, and 480% larger for low, medium and high density SWCNTs in the electrode compared to the devices that did not contain any SWCNT. Similar increment in the μ_{lin} with increasing the SWCNT density is also observed. In calculating the μ, we used L= 4.4 μm and L= 5 μm for devices with SWCNTs and no SWCNTs respectively. However, the SEM images of Figure 12. (a) for low and medium density SWCNTs in the electrode show that there may be an ambiguity in determining L for these densities as the charge injection comes from both Pd and SWCNT interface. In order to minimize this uncertainty, we kept lengths of anchored nanotubes to the Pd short (~ 300 nm). Nevertheless, if we were chosen L= 5 μm for these two densities then the μ_{sat} would be 0.11 and 0.22 cm^2/Vs, for low and medium SWCNT densities. These values are even higher, and indicate that our

experimental data exceeds the error that may arise from the choice of L in low and medium density electrodes. In addition to μ, other important parameters to evaluate the performance of the transistors are I_{on}/I_{off} and I_{on}. The transfer curves show that the on-current (I_d at V_g = - 80 V) and I_{on}/I_{off} increase with the nanotube density in the electrodes. The maximum I_{on}/I_{off} and I_{on} for high density SWCNT electrodes devices are 1.1×10^5 and 14.2 μA respectively, whereas they are 3.1×10^4 and 12.8 μA for medium density, 1.8×10^4 and 10.8 μA for low density, and 9.6×10^3 and 3.3 μA for zero density SWCNT in the electrodes. Therefore, both the Ion/Ioff and Ion are also increased significantly with increasing SWCNT density in the electrodes.

4.3 Device statistics

The device characteristics measured from 40 devices are summarized in Figure 4.4 where we plot the μ, I_{on}/I_{off} and I_{on} as a function of SWCNT density in the electrodes.

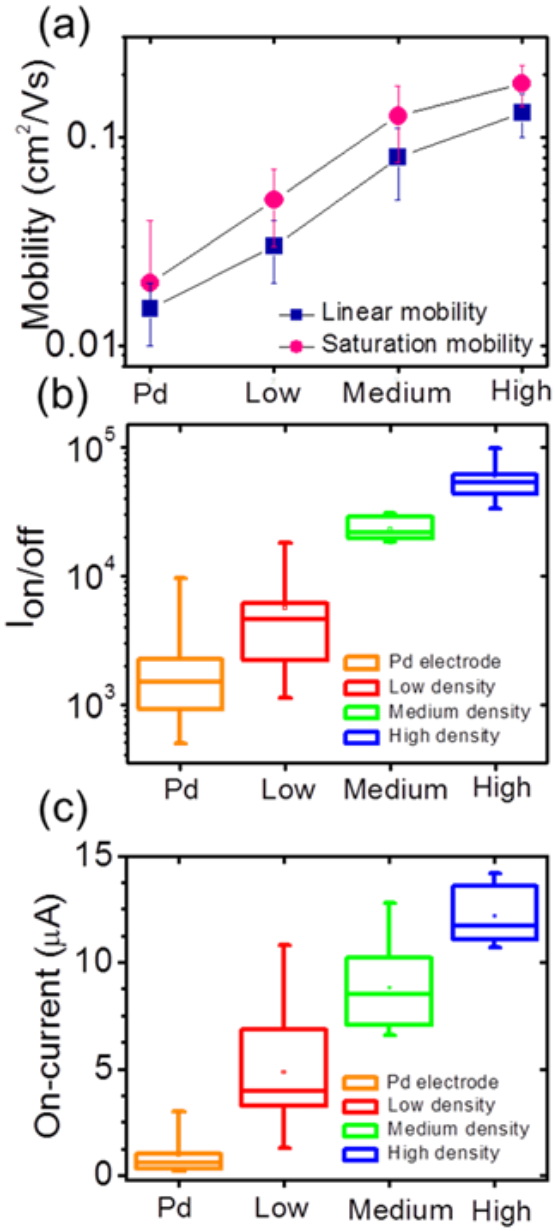

Figure 17. Device performance as a function of SWCNT density in the electrodes. (a) Linear and saturation mobility, (b) on/off ratio, and (c) on-current.

Figure 17. (a) show that, similar to our best devices, the average μ_{sat} are increased from 0.02 for zero SWCNT to 0.06, 0.13 and 0.19 cm^2/Vs (average μ_{lin} are increased from 0.01 to 0.03,

0.08 and 0.11 cm^2/Vs) for low, medium and high SWCNT density in the electrodes, respectively. The increase in average mobility for our OFET with high density SWCNT electrode is almost an order magnitude higher than that of OFETs with zero SWCNT. Similar significant increase can also be seen in the median value of the I_{on}/I_{off} and I_{on} with increasing SWCNT density (Figure 17. (b), and (c)). For the devices with zero SWCNT electrodes, the median value of I_{on}/I_{off} and I_{on} are 1.5×10^3 and 0.6 μA, respectively. These values increased to 5.5×10^4 (~40 times) and 11.82 μA (~20 times) for the devices with high SWCNT density electrodes. From this study, it is clear that the density of SWCNT in the electrode, which control the SWCNT/pentacene interfacial area, has significant impact on the performance of OFETs, Our study unequivocally show that, although a small number of SWCNTs in the electrodes can enhance the devices performance, the maximum performance were obtained using the most dense SWCNTs in the electrode.

The remarkable improvement in the OFET device performance with increasing the SWCNT density in the electrodes is due to increased interfacial area of SWCNT/pentacene interfaces. The current at an interface at a fixed bias voltage and temperature (T) can be approximated as $I \propto \exp(-\phi_b/KT)$, where ϕ_b is the Schottky barrier between the metal/semiconductor interface and K is the Boltzmann constant.[14] A decrease in ϕ_b will result in an increase of current at the interface. It has been recently shown that the value of ϕ_b at SWCNT/pentacene interface is ~ 0.16 eV, which is much lower than the ϕ_b at metal/pentacene interface (~0.35 to 0.85eV).[14]

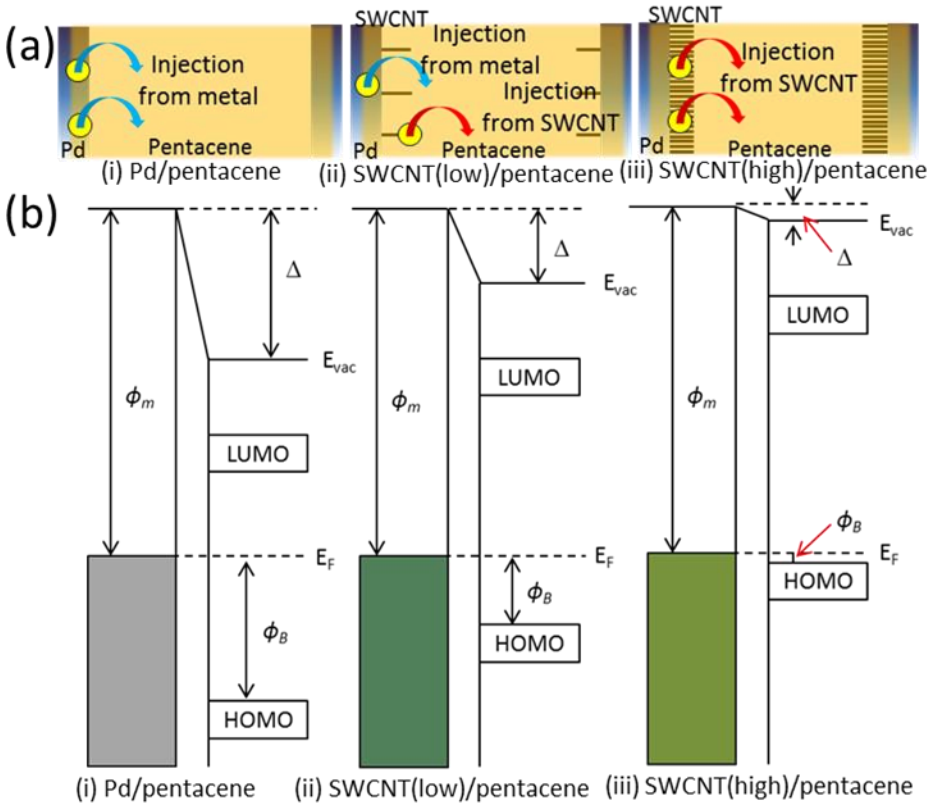

Figure 18. Schematic of diagram for (a) interfacial area and (b) the energy level diagram with (i) bare Pd, (ii) low, and (iii) high density SWCNT in the electrodes. (a) The arrows indicate the charge injection from the SWCNTs (red arrow) and Pd (blue arrow). (b) The schematic diagram shows the energy level digram showing the Fermi Level (E_F), HOMO and LUMO, the vacuum level (E_{VAC}), and the interfacial dipole (Δ) for each density electrodes.

Figure 18. shows schematic diagrams of interfacial area for bare Pd (0 SWCNT), low and high density SWCNT electrodes. In the devices without any SWCNT, all the charge carriers are injected from Pd and pass through only Pd/pentacene interface (Figure 18. (a) (i)). Since Pd has a larger barrier height compared to SWCNT, charge carriers need to overcome a larger injection barriers at the Pd/pentacene interface, which may reduce the number of injected charge carriers in the pentacene film and led to poor device performances (Figure 18. (b) (i)). In contrast, when a small number of SWCNTs are anchored with Pd (low density SWCNT electrode) charge carriers

are injected from both the SWCNT and Pd (Figure 18. (a) (ii)). In this case, the injected charge carriers pass through a smaller barrier at SWCNT/pentacene and a larger barrier at Pd/pentacene (Figure 18. (b) (ii)). Since the charge carriers now have limited access of injection paths through SWCNT, the injection efficiency and device properties are improved. With increasing SWCNT densities, the carriers have larger SWCNT/Pentacene interfacial areas for more efficient charge injection through the lower barrier pathways and the device properties continue to improve resulting in higher device performance (Figure 18. (a) (iii) and (b) (iii)). It is important to note that, in our highest density electrodes there are 30 SWCNT/μm leaving an inter-nanotube separation of 33 nm and we are unable to increase the density any further using DEP. If it will be possible to increase the density of SWCNT in the electrodes by any other technique, it can result in even more impressive device performance.

It is argued that although the work function of both the Pd (5.1 eV) and SWCNT (5.0 eV) are similar and matched with highest occupied molecular orbital (HOMO) level of the pentacene (4.9 eV), the reduction of barrier height is occurred to only SWCNT/pentacene interface due to a small dipole barrier forming at the SWNT/pentacene interface.[14] Instead, the charge transport is limited due to the formation of interfacial dipole barrier and Schottky barrier at Pd/pentacene interface.[7-9]

Figure 18. (b) shows schematic diagrams of interfacial area and energy band diagram for the (i) Pd/pentacene, (ii) SWCNT (low density)/pentacene, and (iii) SWCNT (high density)/pentacene interfaces. The band diagram of energy level illustrates how the Schottky barrier (φ_B) and dipole barrier (Δ) are changed with interfacial area at the SWCNT/pentacene interface. In the devices without any SWCNT, all the charge carriers are injected from the Pd and

pass through only Pd/pentacene interface. Since Pd has a larger barrier height compared to SWCNT (Figure 18. (b)), charge carriers need to overcome a larger injection barrier at the Pd/pentacene interface, which may reduce the number of injected charge carriers in the pentacene film and lead to poor device performances. In contrast, when a small number of SWCNTs are anchored with Pd (low density SWCNT electrode) charge carriers are injected from both the SWCNT and Pd (Figure 18. (b)). In this case, the injected charge carriers pass through a smaller barrier at SWCNT/pentacene and a larger barrier at Pd/pentacene. Since the charge carriers now have limited access of injection paths through SWCNT, the injection efficiency and device properties are improved. With increasing SWCNT densities, the carriers have larger SWCNT/Pentacene interfacial areas for more efficient charge injection through the lower barrier pathways and the device properties continue to improve resulting in higher device performance.

CHAPTER 5 : CONCLUSION

5.1 Summary

In this thesis, we show that the performance of pentacene transistors can be significantly improved by maximizing the interfacial area at single walled carbon nanotube (SWCNT)/pentacene. From the electronic transport measurements, we found that the average mobility is increased three, six and nine times for low, medium and high SWCNT densities, respectively, compared to the devices with zero SWCNT. In addition, the current on-off ratio and on-current are also increased up to 40 times and 20 times with increasing the SWCNT density.

Our study have demonstrated that (i) even a few nanotubes in the electrode can improve the OFET device performance, and (ii) significant improvement can be achieved by maximizing SWCNT/OSC interfacial area. Theses improved OFET performance can be explained by reduced barrier height from SWCNT/pentacene interface compared to metal/pentacene interface. The interface of high density SWCNT/pentacene provides more efficient charge injection pathways with increased SWCNT/pentacene interfacial area. We conclude that the performance of the pentacene transistors using aligned arrays SWCNT electrodes with various interfacial areas at the SWCNT/pentacene contact. From the electronic transport measurement, we showed that the OFET device performance such as mobility, current on-off ratio and on-current can be significantly improved with increasing interfacial area at the SWCNT/pentacene and best performance can be achieved by maximizing SWCNT/OSC interfacial area. We attributed the

improved device performance due to a lower barrier height at the SWCNT/pentacene interface compared to metal/pentacene interface.

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5.2 Future work suggestions

Our study showed that the density of SWCNT in the electrodes effects on the performance of devices. The conclusion of our study suggests the way to improve the organic field-effect transistor for future organic electronics. Also, this work will give us a better understanding of the effect of SWCNT in the electrode in terms of the device performance. More research can be done by low temperature transport measurement study to investigate the direct evidence of barrier height changes depending on the densities of SWCNT in the electrodes. This research will provide us a numerical value for the actual barrier height at different density of SWCNT and organic semiconducting thin film, which will be varied depending on the density of SWCNT in the electrodes.

Another potential future plan could be fabricating OFETs using graphene electrode. Due to its unique 2-dimensional hexagonal carbon atom structure, graphene has outstanding electrical, mechanical, and chemical properties. This study can give us an idea of improving the performance organic field-effect transistor.

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