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Electromechanical Lifting Actuation of a MEMS Cantilever and Nano-Scale Analysis of Diffusion in Semiconductor Device Dielectrics

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ELECTROMECHANICAL LIFTING ACTUATION OF A MEMS CANTILEVER AND NANO-SCALE ANALYSIS OF DIFFUSION IN SEMICONDUCTOR DEVICE DIELECTRICS

by

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ABSTRACT

This dissertation presents experimental and theoretical studies of physical phenomena in micro- and nano-electronic devices. Firstly, a novel and unproven means of electromechanical actuation in a micro-electro-mechanical system (MEMS) cantilever was investigated. In nearly all MEMS devices, electric forces cause suspended components to move toward the substrate. I demonstrated a design with the unusual and potentially very useful property of having a suspended MEMS cantilever lift away from the substrate. The effect was observed by optical micro-videography, by electrical sensing, and it was quantified by optical interferometry. The results agree with predictions of analytic and numerical calculations. One potential application is infrared sensing in which absorbed radiation changes the temperature of the cantilever, changing the duty cycle of an electrically-driven, repetitively closing micro-relay.

Secondly, ultra-thin high-k gate dielectric layers in two 22 nm technology node semiconductor devices were studied. The purpose of the investigation was to characterize the morphology and composition of these layers as a means to verify whether the transmission electron microscope (TEM) with energy dispersive spectroscopy (EDS) could sufficiently resolve the atomic diffusion at such small length scales. Results of analytic and Monte-Carlo numerical calculations were compared to empirical data to validate the ongoing viability of TEM EDS as a tool for nanoscale characterization of semiconductor devices in an era where transistor dimensions will soon be less than 10 nm.

To my wife and best friend, Javaneh, who is on my side all the time.

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At the end, I would like to give special thanks to my beloved wife, best friend and great colleague, Javaneh Boroumand. She had a major role especially in the first project presented in this dissertation which I am grateful for. I owe her a great deal of my success. Thanks god for her and all other blessings in my life.

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CHAPTER 1 INTRODUCTION

1.1 History of Semiconductors

Semiconductors are materials with electric conductivity between conductors and dielectrics. The first documented semiconductor was reported by Michael Faraday in 1833 when he observed reduction of silver sulfide resistance with temperature which was different than metals. [1] Another important property of semiconductors is that their conductivity can vary over several orders of magnitude by small changes in doping concentration. [2] The next big step for semiconductors happened in 1870s. In 1874, rectification was reported in the contacts between metals and some oxides and sulfides. Carl Ferdinand Braun made the first semiconductor rectifier, which became the foundation for the most basic and simple electronic device, the diode. [2, 3] Around the same time another important application was discovered for these materials with the invention of photovoltaic cells. Research until then showed promise of electricity production by shining light to selenium and in 1883 Charles Fritts made the first photovoltaic cell. [4]

Increasing use of radio and semiconductor rectifiers showed a bright future for these materials in 20th century. Silicon is currently the most known and used semiconductor material. Silicon made its entrance into the industry in 1906 when Greenleaf Whittier Pickard demonstrated and patented [5] that silicon crystals could be used as an electromagnetic wave detector. For about 50 years diodes were used in industry while efforts were made to better understand semiconductors. All these efforts paid off when the first point contact transistors were created in 1948. Bardeen and Brattain received the Nobel Prize for this discovery, together with Shockley, in 1956. [2]

Perhaps the final step for semiconductors to conquer electronics world was done in 1954 when Gordon Teal announced the first silicon transistor at a meeting of the Institute of Radio Engineers in Ohio. [2] This was the beginning of an era for semiconductor industry.

Today it is almost impossible to find people who are not using electronic devices in one way or another in their lives, and even harder to find an electronic device that does not have a semiconductor material inside. All industries are using these devices extensively, from cars and home appliances to optoelectronic devices that transfer huge amount of data every second all around the world. Semiconductors are playing a major role in our life. Since the beginning of this industry, the number of transistors in an integrated circuit (IC) has been increasing exponentially. [1] Gordon Moore predicted this trend in 1975, later known as Moore's Law [6]. Transistors had to be miniaturized in order to fit a larger number of them in same area. This trend in industry resulted in a downscaling of devices to move from a feature size of about 10 μm in the 1970 to a 10 nm feature size in 2015.

Among various types of semiconductor devices, microprocessors play an important role. Today virtually any electronic device that has to process information uses microprocessors. The first microprocessor was the 4 bit 4004 made by Intel in 1971. [7] Many current devices use system on chip (SoC) integration where all the components of a computer are contained on a single silicon chip. Regardless of their complexity or the application of an IC, the most fundamental component is the transistor. In 2009 there were about 1 billion transistors per person on earth. [8]

1.2 Microelectromechanical Systems and Infrared Sensing

Microelectromechanical systems (MEMS) are devices of smaller than 1 mm and larger than 1 μm that use electrical and mechanical components to perform a task in an electronic device. [9] MEMS are finding more applications in various industries every year and their market is about 15 billion dollars in 2015. These devices are often employed in electronics like sensors, actuators and energy harvesters over a wide variety of industrial systems. From complex systems like space and air vehicles to health care devices like wearable systems for remote monitoring of human health, they all use MEMS and NEMS (nanoelectromechanical systems) for various purposes. Most of these devices are based on energy conversion provided by suitable coupling effect. Among all different techniques, electromechanical conversion is predominant. It provides a transformation of mechanical energy introduced by forces, moments, stresses and strains in structural components into electromagnetic energy or vice versa. [10] One of MEMS applications is in infrared sensing which we are focusing on in this research.

Bolometers are devices that absorb electromagnetic radiation and as a result of that experience temperature change which is sensed by a temperature sensing principle like change in resistivity. Uncooled infrared bolometers have become dominant for the majority of commercial infrared imaging applications. Some of the most common infrared imaging applications are thermography, night vision, mine detection, surveillance, medical imaging and industrial process control. [11]

Many of MEMS infrared detectors work based on deflection of a movable part due to change in temperature and detection of such deflection by means of a sensing principle.

This can be a change in capacitance, resistance or other methods. Some of the most important parameters in the design of MEMS infrared sensors are low conductance between the bolometer and its surrounding, high absorption of the infrared radiation, low noise and a sufficiently low bolometer thermal time constant. At the same time it is important for commercial infrared imaging applications, that the bolometer pixels are as small as possible with reported pixel pitches being 17 μm x 17 μm [12-14]. This allows for high-resolution focal plane arrays at acceptable cost. [11]

1.3 Understanding of Semiconductor and MEMS Devices

With such importance of semiconductors and MEMS devices in our daily life, there is no doubt about the ongoing need for understanding their characteristics and functions. This can be done in two ways:

- Modeling and Simulation: Regardless of size, design, function and application, all of these devices follow the rules of physics. These rules are all expressed in forms of differential equations which can be solved analytically or numerically by different modeling techniques such as finite element modeling. This step is usually done before device fabrication and is used for better understanding of device design and behavior and its optimization. This will lower the chance of unpredicted device failure after fabrication.
- Characterization: As device complexity increases, the chances of missing some aspect of it in modeling increases. It is then necessary for each

fabricated device to be analyzed by suitable techniques to ensure its proper functionality and quality. In addition to quality control, other applications for device characterization are failure analysis, research and intellectual property protection, etc.

We can look into each device in two different ways. It can be analyzed as a whole, where many parts interact with each other to perform a single function. In this case it is more important to understand the device functionality and interaction of the parts. A simple example is current–voltage characterization of a transistor where drain current is measured Vs. drain to source voltage for different values of gate voltage. We can also characterize these devices according to the characteristics of their individual parts. Type of materials, dopant concentration, resistivity, etc. are all examples of such characteristics. The first category usually requires the device to stay functional while second category of characterization requires devices to be taken apart so that individual parts can undergo different necessary characterization processes.

1.4 Outline of This Dissertation

In this dissertation two research projects are presented. The first project is the design, modeling, fabrication and characterization of a novel MEMS infrared detector. This project was research done to test and optimize a proposed infrared detector detailed in US Patent 007977635B2 [15] for commercialization possibilities. This project will be presented in chapters 2 through 6. The second research project is selected out of a body of work that was done by the author in collaboration with NanoSpective, Inc.[16]

NanoSpective specializes in materials science with special emphasis on nanoscale materials characterization, particularly semiconductor devices. The company provides analytical services and consultation to a worldwide market in various industries specially semiconductors, offering complete solutions for intellectual property issues, failure analysis, quality control, and materials research. The selected project is analytical and numerical modeling of energy-dispersive x-ray spectroscopy (EDS) and transmission electron microscopy (TEM) for analyzing high-k dielectric layers of 22 nm node gates structures in a microprocessor. The modeling results are compared to experimental data for the observation of material diffusion in those layers. This project is presented in chapters 7 to 10. Chapter 11 provides an overall conclusion about both projects.

Outline of this thesis for next chapters is as follows:

- Chapter 2: This chapter will provide background information from US patent 007977635B2 [15] on proposed MEMS IR detector. After reviewing this patent and different aspects of such device, a short description of device design will be presented.
- Chapter 3: The main focus of the first presented project in this dissertation is on modeling and characterization of electrostatic behavior of the aforementioned MEMS IR detector. In this chapter, a semi-analytical approach is used to understand this electrostatic behavior.
- Chapter 4: Following the semi-analytical approach, this chapter presents the finite element modeling of the device. This provides a better understanding

of its electrostatic behavior. Modeling results also provide optimized design parameters for better functionality and limits of device operation.

- Chapter 5: Using the optimized design results of the finite element analysis, the device is fabricated. In this chapter all steps of fabrication are explained and the final devices are presented.
- Chapter 6: Post-fabrication characterization results are presented in this chapter. Here, different techniques for characterization of electrostatic behavior of this device are described and experimental results are presented. The expected behavior is compared with the results from the finite element modeling.
- Chapter 7: In this chapter additional available techniques for characterization of semiconductor devices are reviewed. This chapter provides an introduction to the second presented research project in this dissertation.
- Chapter 8: Analytical and theoretical background for EDS and TEM resolution limits are presented in the context of the characteristics of the device under investigation.
- Chapter 9: The fundamentals of Monte Carlo simulations are explained in this chapter. The results of using this simulation technique for TEM and EDS are used to optimize the data acquisition parameters to achieve highest possible lateral spatial resolution required for analyzing the interfaces of a complex stack of thin films.

- Chapter 10: In this chapter, the presence of diffusion in the high-k dielectric layers of two advanced generation semiconductor devices are investigated by experiments. The simulation results are compared with the empirical data to validate the experimental observations.
- Chapter 11: Conclusion is made in this chapter on both research projects and industrial applications are mentioned for them.

CHAPTER 2 PATENT REVIEW AND DEVICE DESIGN

2.1 Introduction

In this chapter different aspects of a MEMS IR detector design will be presented. Fabricated device in this project was based on a patent by Oliver Edwards [15]. We will first review his design and patent's claims. Then we will analyze some of the important aspects of this design and provide optimized factors to enhance the device functionality. Based on these analyses, the final design will be introduced in detail. It is worth mentioning that we are only reporting patent claims in first part of this chapter. These claims are tested though this research and modifications are done to provide optimum device behavior. Also, most of this research is focused on investigating the claimed electrostatic behavior of this device and optimizing its design to achieve the claimed behavior. Although the finalized design is suitable for infrared detection, it also has a wide range of other applications in MEMS industry that are not necessarily associated with infrared technology.

2.2 Review of Preliminary Work

Edwards [15] proposed a MEMS infrared (IR) detector comprised of a cantilever, a surface plate, and a buried plate. Lifting of the cantilever tip from a surface contact pad by electrostatic force is an essential principle of operation, in which the duty cycle of a repetitively opened and closed tip contact is a measure of the absorbed infrared energy. [17] Figure 2-1 demonstrate overall side view of suggested design.

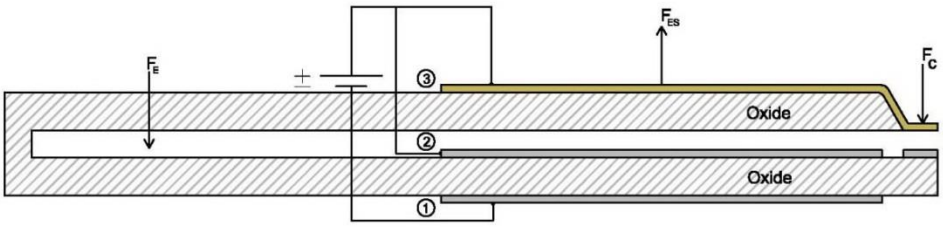

Figure 2-1 Simplified schematic of the device. [18]

The top and middle conductive plates are at the same bias while the bottom plate, buried under an insulating layer, is held at an opposite potential. The bottom and middle plates are fixed but the top plate is held above the surface by arms at one side and is free to move up and down on the other side which forms a cantilever. The device work principle is based on deflection due to three separate mechanisms. First, the claimed electrostatic repulsion that pushes top plate upward, second, the bending due to the difference in thermal expansion coefficient of the two different material layers in the cantilever and third, a restoring elastic force that tends to return the cantilever to its initial position after deflection.

In the absence of thermal deflection, by applying a saw tooth bias between the plates, regardless of its sign, cantilever will move up due to the total electrostatic repulsive force on it. But as the bias drops back to zero, the elastic force will restore cantilever to its initial position. The patent suggests a tip which will touch the surface once the cantilever is back to its original position. Such a tip enables an external circuit to count every time cantilever comes back to its initial position. In the absence of heat absorption, the touching frequency is the same as saw tooth bias frequency.

Figure 2-2 presents a schematic of the applied and measured voltage waveforms. In equilibrium the free end of the cantilever is in physical and electrical contact with the tip pad. When the cantilever is biased with a voltage V_B, an upward repulsive electrostatic force lifts the cantilever from the surface and breaks the tip contact. As V_B is ramped down during a time τ, the voltage at the tip contact V_T is monitored. If IR radiation is absorbed, thermal deformation of the bimorph arms causes the tip to return to the tip contact sooner than τ by a time $\Delta\tau$, as determined by the voltage V_T that appears on contact. The time $\Delta\tau$ gives a temporal measurement of the absorbed IR flux. [19]

Every time tip touches the surface, heat is drained through metallic tip and makes pixel ready for next sequence. One of the advantages of this design is the absence of a cooling system and the high frame rate which makes it more suitable for infrared scene detection.

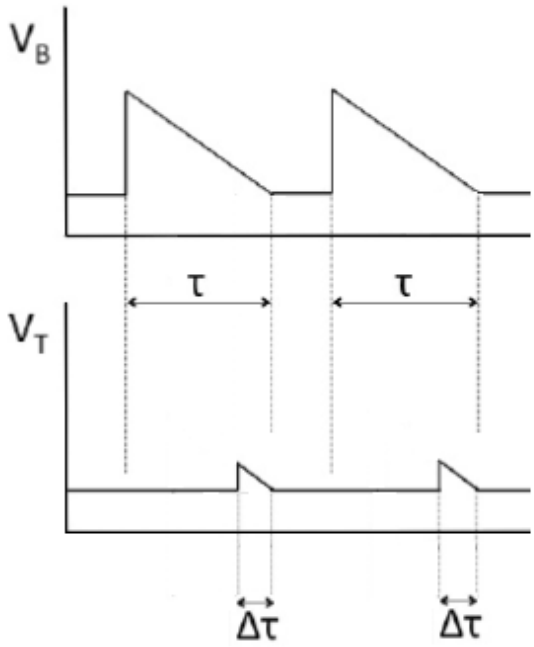

Figure 2-2 Timing diagram showing applied bias V_B and measured tip voltage V_T waveforms. [19]

Based on single pixel design, Edward proposes an array detector like the one in figure 2-3, where the pixels are closely packed together on a surface to form an infrared scene imager. This space-efficient three-layer design makes higher fill factor possible and suggests broader applications as a means of overcoming stiction in MEMS switches, actuators, and micromirrors. [20, 21]

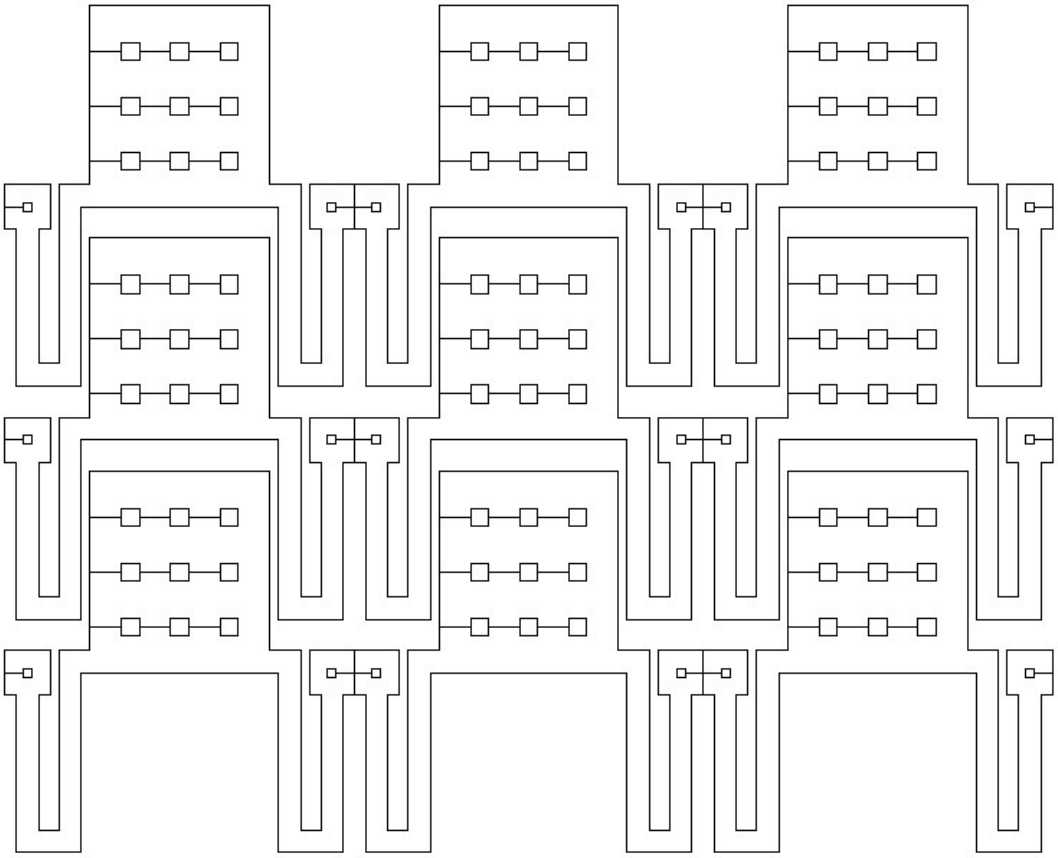

Figure 2-3 Focal plane array configuration of final devices.

2.3 Design Criteria

In this section we present a theoretical analysis of several design criteria for the proposed MEMS cantilever in Edward's design. The factors considered are:

1. The thermal bending of a bimorph arm that is anchored to the substrate.
2. The time constant for establishing thermal equilibrium for heated bimorph after its tip has contacted the substrate.
3. The electrostatic repulsion required to lift the cantilever from the surface.

In this section our approach is entirely analytical, seeking simple design formulas that give quick order of magnitude estimates, which can be tested and optimized in the hardware.

For the thermal bending problem, materials, geometries, and deposition temperatures are considered as parameters. For the thermal time constant problem, the substrate is assumed to be an infinite thermal reservoir at constant temperature while heat flow from a warm cantilever of small heat capacity through a cylindrical contact is considered. Finally, the electrostatic repulsion problem is solved using energy methods considering forces between conductors held at constant potential. The resulting formulas are useful for the final design of any MEMS-based thermal sensor and bolometer.

2.3.1 Thermal Bending

In a bilayer cantilever, due to the difference in thermal expansion coefficients of layers, thermally induced stress will bend the surface upward or downward. The stress is:

$$\sigma_{mismatch} = \frac{E}{1-\nu}(\alpha_f - \alpha_s)(T_d - T_r) \quad (1)$$

Figure 2-4 demonstrates the described bending for two different cases.

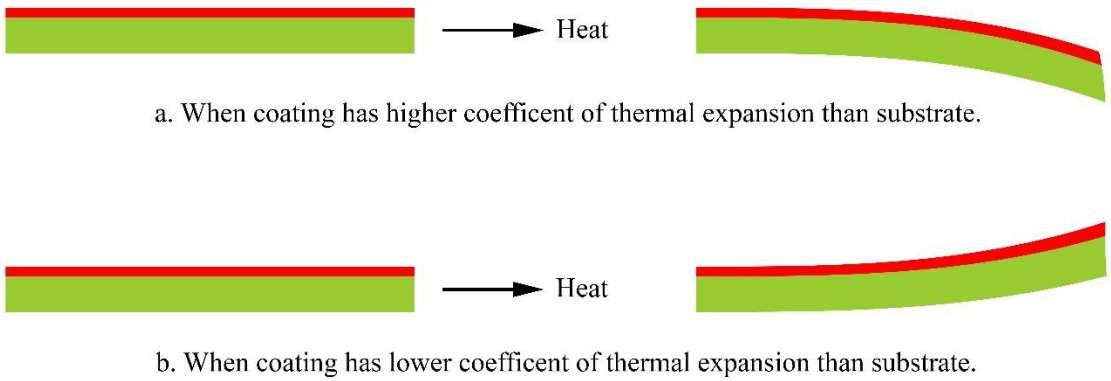

Figure 2-4 Demonstration of double layer system bending due to differences in thermal expansion coefficient of layers.

For a thin film on thick substrate this is [22]

$$\sigma_f = \frac{E_s t_s^2}{6Rt_f(1-v_s)}\kappa \quad (2)$$

The deflection is usually very small and hence having the two equations equal, will lead to

$$h(t) = \frac{3E_f t_f L^2}{E_s t_s^2}(\alpha_f - \alpha_s)(T - T_d) \quad (3)$$

Where L is cantilever's length, E is young module, α is thermal expansion coefficient, t_f is film thickness, t_s is substrate thickness and T_d is deposition temperature. Taking the first derivative of tip's deflection with respect to temperature we find:

$$\frac{dh}{dT} = \frac{3E_f t_f L^2}{E_s t_s^2}(\alpha_f - \alpha_s) \quad (4)$$

This value can be interpreted as cantilever sensitivity to temperature change and will have a great impact on proposed device functionality. Based on this value, better choices for materials can be made. Ideally higher values of thermal sensitivity are required. For example, a choice of Al as thin film on top of silicon oxide will lead to 0.095 μm/K while Zn over SiO_2 will have 0.192 μm/K sensitivity. Chosen materials in device fabrication are presented in chapter 5.

2.3.2 Thermal Time Constant

Infrared sensors have different mechanisms to drain absorbed heat. [23] In this design heat is drained through metallic tip once it touches the surface. In such mechanism tip design will have a great impact on how long it takes the device to get in thermal equilibrium with substrate. So it is important to have an estimation of this time constant.

Here we consider the substrate an infinite thermal source fixed at a constant temperature of 300 K. The heat flux is:

$$H = KA\frac{(T_2 - T_1)}{L} = c_1 m_1 \frac{dT_1}{dt} \quad (5)$$

With proper boundary conditions, the solution is:

$$T_1(t) = T_2 + e^{t/\tau}(T_{1i} - T_2) \quad (6)$$

Where thermal time constant is defined as:

$$\tau = \frac{c_1 m_1 L}{KA} \quad (7)$$

This time constant gives us a measure for how fast heat is leaving the cantilever once the connection between tip and substrate is established. For a gold tip, with its length L = 2 μm the thermal time constant is about 5.5×10^{-6} s.

This corresponds to 1.8 MHz frequency. Thus, in principle, thermal zeroing through periodic tip contact can allow high frame rates without chopping.

2.3.3 Thermomechanical Noise

Thermomechanical noise for a MEMs-based infrared detector using null switching [15] depends on vibrational amplitude, since IR radiation is transduced to a change in the duty cycle of a repetitively closing switch. Equipartition theorem determines the maximum rms vibrational amplitude for the fabricated cantilever switch at its natural frequency. This determines the worst case timing uncertainty. [19]

In this section we discuss thermomechanical noise. This detector is unusual in that absorbed IR radiation is transduced into a measurement of a time. High sensitivity to small differences in scene temperature requires high measurement bandwidth. Thermomechanical noise is determined by this bandwidth rather than by the frame rate, as in usual imaging detectors. Thus, the vibrational amplitude at the cantilever's natural oscillation frequency is important.

A simplified schematic of the MEMS cantilever device is presented in figure 2-1. The tip of the cantilever consists of a tip contact that is normally touching a surface tip pad ("null position"), allowing electrical sensing of contact. An upward electrostatic force F_{ES} appears when the device is biased as shown in [18, 24]. This is opposed by an elastic

restoring force F_E and a sticking force F_C (such as Casimir force).[25] The latter force will be ignored here. For simplicity we will consider the elastic force to apply mainly to the arms and we ignore any deformation of the metal-coated regions. Thermo-mechanical vibration of the cantilever results in uncertainty in the time of contact, and hence noise in the determination of IR flux. [17]

Key to the estimation of thermo-mechanical noise is an estimate of the elastic constants of the device, i.e. its spring constant when considered as a 1D simple harmonic oscillator. Figure 2-5 presents solved stress field and displacement of the cantilever. This calculation was done assuming Aluminum as the material, with Poisson ratio 0.35, Young's modulus 70 GPa, and density 2700 kg/m³. The cantilever is fixed to the substrate at its anchors. It is subjected to a stress of 154 N/m² as a result of uniformly distributed force on its 20 x 18 μm² area plates. Color indicates vertical displacement. Blue is the maximum displacement in the negative z direction, while white is the maximum displacement in positive z direction. The anchors are fixed at z = 0, which is color-coded light purple. For these calculations, the equilibrium position of the cantilever tip is at z = 0, in contrast to that actual device, where the cantilever is bent down with the tip touching the surface 2 μm below the anchor point for the isolation arms. But this should make only a little difference in the value of the spring constant determined.

Figure 2-5 shows that the elbows on the arms bend upward by ~ 10% of the amount that the tip bends down. From the top view color gradient, one sees that the bimorph arms (inner pair) have more curvature than the isolation arms (outer pair). Thus, the elastic restoring force is primarily due to the inner pair of arms.

A plot of force as a function of displacement is linear. We found for an Aluminum cantilever that the spring constant K has the value 0.73 N/m. (Aluminum is considered for comparison to some macroscopic machined models that we experimented with.) For SiO_2, as in the actual cantilever, K = 0.68 N/m.

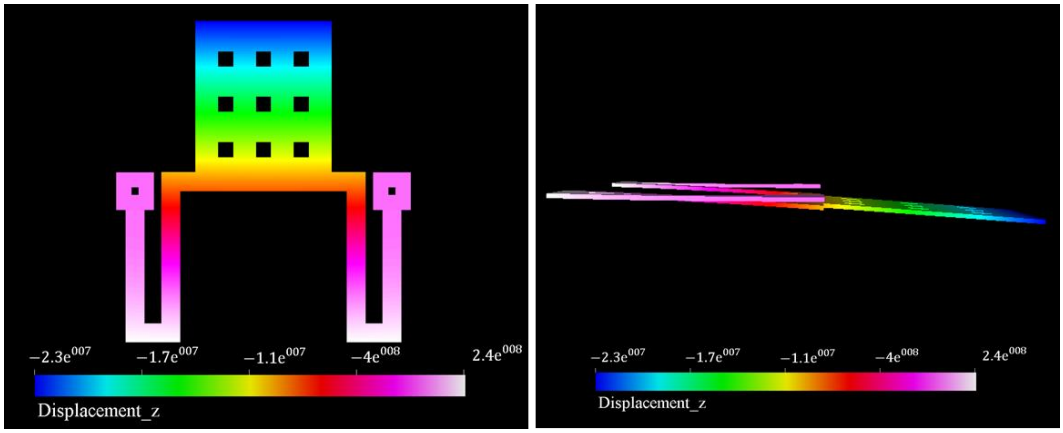

Figure 2-5 (Left) Top view of deflection map due to the stress caused by uniformly applied pressure of 154 N/m2 applied to the rigid 20 x 18 μm² cantilever plate. (Right) Side view of the cantilever displacement scaled up by a factor of 10. [19]

Suppose the cantilever is an un-damped one-dimensional oscillator with natural frequency ω_0. The equipartition theorem indicates that the mean square amplitude of the vibrations should not be less than

$$\left(\frac{1}{2}\right) K < z^2 > = \left(\frac{1}{2}\right) k_B T \qquad (8)$$

If we take the spring constant to have the value K = 0.68 N/m, we find the rms vibrational amplitude to be 79 pm. This value is 4000x larger than the value given in [17] from a published thermomechanical noise formula assuming 30 Hz bandwidth. The reason for the difference is that 30 Hz is far from the ~200 kHz natural frequency of the cantilever

(mass ~13 ng). The amplitude of oscillations at 30 Hz is small because this frequency is far out on the wing of the vibrational resonance line shape.

The detector mode of operation requires high electronic bandwidth to differentiate small timing differences that indicate small differences in scene temperature. Since timing measurements may be done with reference to quartz stable clocks operating easily at 20 MHz or more, the natural frequency of the cantilever will be within the measurement bandwidth. Thus, timing uncertainty (i.e. noise) is determined by the natural frequency where vibrational oscillations are maximum.

To illustrate, figure 2-6 presents the final 50 μs of the tip-height saw-tooth with superimposed thermal noise at the natural frequency. The tip touches early by 0.7 μs. We may demonstrate mathematically that the timing uncertainty depends primarily on noise amplitude as follows. For frame rate *f* and noise frequency ω, the tip height is

$$z(t) = z_0(1 - 2ft) + A\,Cos\,[\omega t + \phi] \qquad (9)$$

The time of contact is determined by setting the left side to zero and solving for *t*. When the noise amplitude A = 0, touch down occurs at time τ=1/2f (50% duty is assumed). The maximum timing error occurs when Cos = ±1, for which the maximum timing uncertainty is ± A/(2 f z_0). This timing uncertainty depends on A, but it does not depend on ω. Thus, thermomechanical noise is mainly defined by noise at the natural frequency of the cantilever, where amplitude is largest, which will be a function of device shape and materials. It is outside of the scope of this dissertation to investigate noise calculation aspect any further, but the author emphasizes that noise consideration has to be done in the design of commercialized products that are based on this design.

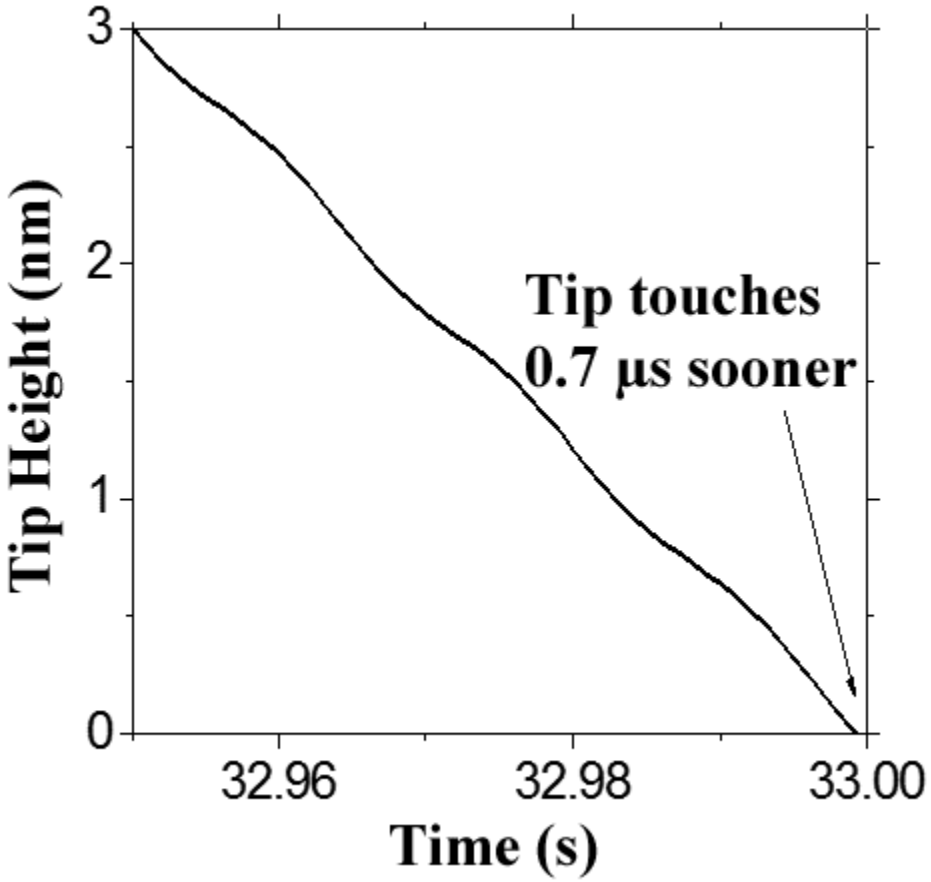

Figure 2-6 Tip height ramp vs time with superimposed vibrational noise. [19]

The most novel and important aspect of this device is in electrostatic repulsion on cantilever which we will study in detail in next chapters.

2.4 Device Design

Although we tried to keep design aspects similar to what Edward describes [15] it is important to know that patent design is only preliminary and all aforementioned factors as well as many other parameters such as fabrication feasibility, cost, available methods and time had to be considered in final design of the device. During three phases of this

project and over about 3 years we had to change details of the design to optimize its functionality and customize it for our purposes and capabilities. What is described in the following paragraphs is the finalized design considering all of these considerations.

Overall 3D demonstration of a single pixel can be seen in figure 2-7. As mentioned previously, each pixel consists of three plates. A bottom plate shown in red is buried under the substrate surface. A middle plate is fixed on the substrate surface. The distance between these two plates is 500 nm. The third plate is part of the actual cantilever which is held above the surface. The main parts of cantilever are as follow:

1. Anchors: anchors are the only parts of cantilever who are permanently in contact with surface. Each pixel has two anchors, one on each side. Anchors are made 10 μm × 10 μm. Each anchor has a hole that connects its top metallic surface to substrate. This hole ensures electrical connection between top plate and external circuitry that provides bias between plates.
2. Isolation arms: these are the arms that are connected to the anchor. These arms are made of 500 nm dielectric material with a thin layer of metal on top. This metal layer is continues all over the surface of cantilever and is in charge of making the connection between top plate and external bias source.
3. Bimorph arms: bimorph arms are double layers of dielectric material and thick layer of metal. These ensure thermal bending once cantilever changes temperature. Choice of length, thickness and material on these arms define thermal time constant as explained before.

4. Absorber layer: An absorber material is deposited on top of top plate which enhance thermal absorption and sensitivity of the device.
5. Release holes: Fabrication process requires release of cantilever from the sacrificial layer that device is built on. Such release is only possible by making holes on top plate that ensure uniform access to sacrificial layer for etching.
6. Tip: tip is only added for final devices when its functionality is tested by touching the sensing pad on the surface. It is hidden under top plate and is touching sensing pad in natural position. However by applying the bias it will disconnect from the surface.

Parts mentioned above are only main parts of this device. In chapter 6 we will explain details of fabrication including all materials, dimensions and techniques used to fabricate the actual device.

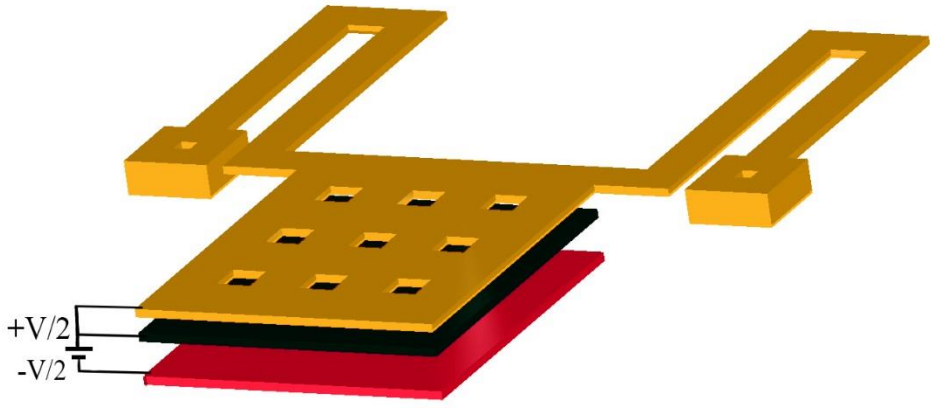

Figure 2-7 Overall structure of the device.

CHAPTER 3 SEMI-ANALYTICAL APPROACH

3.1 Introduction

As we mentioned earlier the focus of this dissertation is on understanding the electrostatic behavior of this device. We are specifically more interested in demonstrating presence of repulsive electrostatic field in a three plate configuration of this device. We will then further analyze different parameters of design to find an optimum configuration in which this force will be maximized. In this chapter, our approaches for analytical calculations of total electrostatic force applied on the top plate will be explained and a simple example of 2 plate system will be solved. Then we will explain three plate problem present in this device and solve that using similar technique. Using calculated solution for total electrostatic force we will show how plate movement will affect this force.

3.2 Electrostatic Field in a System of Conductors

We start our method by calculation of electrostatic force produced by conductors. It is a fundamental proven fact the electric field inside a conductor is always zero. That is because any electric field in a conductor will cause a current which then results in dissipation of energy. Hence it is impossible to have an electric field inside a conductor in the absence of external source of energy. This follows that all charges in a conductor have to be on the surface and cannot be inside conductive medium. This means that in system of conductors, electrostatic problems are reduced to calculating fields outside the conductors' volume. [26] Such system has to satisfy Laplace's equation in the vacuum:

$$\Delta\phi = 0 \quad \& \quad \boldsymbol{E} = -\boldsymbol{\nabla}\phi \qquad (10)$$

Where **E** is electric field vector and Φ is electric potential. Using these equations and having no electric field inside a conductor results in a conclusion that electric field on the surface of a conductor is perpendicular to the surface. [26] On the other hand, perpendicular component of electric field (in Gaussian units) is related to charge distribution on the surface by:

$$\mathbf{E_n} = \frac{\partial \phi}{\partial n} = 4\pi\sigma \qquad (11)$$

Where σ is the surface charge density.

Hence the total charge on the conductor is equal to:

$$q = \frac{-1}{4\pi} \oint \frac{\partial \phi}{\partial n}\, df \qquad (12)$$

3.3 Energy in Electrostatic Field of Conductors

Energy in electrostatic field of system of conductors can be written as:

$$U = \frac{1}{8\pi} \int E^2 dV \qquad (13)$$

Integral is taken over all spaces outside all conductors. We can take this further:

$$U = -\frac{1}{8\pi} \int \boldsymbol{E}.\boldsymbol{\nabla}\phi \; dV = -\frac{1}{8\pi} \int \boldsymbol{\nabla}.(\boldsymbol{\phi E})\, \boldsymbol{dV} + \frac{1}{8\pi} \int \boldsymbol{\phi}\, \boldsymbol{\nabla}.(\boldsymbol{E})\, \boldsymbol{dV} \qquad (14)$$

Second integral is zero since div **E** = 0. We can bound first integral to volume between surface of conductors and infinitely far away surface. Second boundary results in zero since electric field will be zero at infinite distances from the field source (in this case charges on conductor surface). Since potential is constant on surface of each conductor we can rewrite energy of the system in following form:

$$U = \frac{1}{8\pi} \sum_i \boldsymbol{\phi}_i \oint E_n \, df \qquad (15)$$

Where Φ_i is the constant potential on the i^{th} conductor's surface. Using equation 12 we can express energy as:

$$U = \frac{1}{2}\sum_i q_i \boldsymbol{\phi}_i \quad (16)$$

Where q_i is the total charge on i^{th} conductor. Since field equations are linear and homogeneous charges and potentials of conductors must have a linear relation which can be expressed in a general form of:

$$q_i = \sum_j C_{ij} \boldsymbol{\phi}_j \quad (17)$$

Where C_{ij} are called coefficients of electrostatic induction and C_{ii} are called coefficients of capacity. These numbers depend on shape and relative positions of conductors and are related to linear dimensions of conductors. We can express equation 17 in a matrix form of:

$$\begin{bmatrix} q_1 \\ \vdots \\ q_n \end{bmatrix} = \begin{bmatrix} C_{11} & \cdots & C_{1n} \\ \vdots & \ddots & \vdots \\ C_{n1} & \dots & C_{nn} \end{bmatrix} \begin{bmatrix} \boldsymbol{\phi}_1 \\ \vdots \\ \boldsymbol{\phi}_n \end{bmatrix} \quad (18)$$

It can be seen from symmetry or proven analytically [26] that

$$C_{ij} = C_{ji} \quad (19)$$

Using equation 12 we can rewrite equation 16 as:

$$U = \frac{1}{2}\sum_{i,j} C_{ij} \boldsymbol{\phi}_i \boldsymbol{\phi}_j = \frac{1}{2}\sum_{i,j} C_{ij}^{-1} q_i q_j \quad (20)$$

Since energy is always positive, it is easy to see that

$$C_{ii} > 0 \quad (21)$$

$$C_{ij} < 0 \quad (i \neq j) \tag{22}$$

3.4 System of Two Flat Conductors

Let us examine our calculation with a simple example first. Imaging a conventional capacitor. Where two infinitely large flat conductors are separated with distance d from each other. One plate has –q and the other has +q charge on themselves. So we can write equation 18 for this system as:

$$\begin{bmatrix} -q \\ +q \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{12} & C_{22} \end{bmatrix} \begin{bmatrix} \phi_1 \\ \phi_2 \end{bmatrix} \tag{23}$$

Similarly we can express energy of the system using equation 20 in following form:

$$U = \frac{1}{2}\sum_{i,j} C_{ij}^{-1} q_i q_j = \frac{1}{2}(C_{11}^{-1}(-q)(-q) + C_{12}^{-1}(-q)(+q) + C_{21}^{-1}(+q)(-q) + C_{22}^{-1}(+q)(+q) = \frac{1}{2}(C_{11}^{-1}q^2 - 2C_{12}^{-1}q^2 + C_{22}^{-1}q^2) \tag{24}$$

Where inverse matrix of C is:

$$C_{ij}^{-1} = \frac{1}{C_{11}C_{22} - C_{12}^2} \begin{bmatrix} C_{22} & -C_{12} \\ -C_{12} & C_{11} \end{bmatrix} \tag{25}$$

Hence:

$$U = \frac{1}{2}\frac{(C_{22} + 2C_{12} + C_{11})}{C_{11}C_{22} - C_{12}^2} q^2 \tag{26}$$

Comparing this results with conventional definition of energy for a parallel plate capacitor:

$$U = \frac{1}{2} q^2 / C \tag{27}$$

We can have the relation between conventional capacitance for a parallel plate capacitor and capacitance coefficient as follows:

$$C = \frac{\varepsilon_r A}{4\pi d} = \frac{C_{11}C_{22} - C_{12}^2}{C_{22} + 2C_{12} + C_{11}} \quad (28)$$

Assuming a symmetry between two plates it is reasonable to consider diagonal elements equal to each other and in the order of linear length of the plate.

$$C_{11} = C_{22} \sim L \quad (29)$$

We will use this later to provide a handwaving argument for repulsive electrostatic force in three plate system.

3.5 Three Parallel Plate Problem: Real Case

The net force on the cantilever is determined from the position dependence of the coefficients of capacitance and electrostatic induction. All of these coefficients depend on the conductor shapes, sizes, and relative positions. The model system consists of 3 parallel plates (figure 3-1), which are assumed square and each with area *A*. A buried plate (1) is at depth *d* below the surface and is held at a potential of –*V*/2. A fixed surface plate (2) is held at potential +*V*/2. The cantilever (3) is a variable height *z* above the surface plate, to which it is electrically connected so that its potential is also +*V*/2. The energy of a system of conductors at fixed potential is

$$U = \frac{V^2}{8}(-2C_{12} - 2C_{13} + 2C_{23} + C_{11} + C_{22} + C_{33}) \quad (30)$$

Differentiation of this energy with respect to the vertical position *z* of the cantilever gives the electrostatic force on it:

$$F = +\frac{\partial U}{\partial z} = \frac{V^2}{8}\left[-2\frac{\partial C_{12}}{\partial z} - 2\frac{\partial C_{13}}{\partial z} + 2\frac{\partial C_{23}}{\partial z} + \frac{\partial C_{11}}{\partial z} + \frac{\partial C_{22}}{\partial z} + \frac{\partial C_{33}}{\partial z}\right] \quad (31)$$

It is very important that the "+" appears before the derivative in Eq. 3, rather than the usual "-" from ordinary mechanics. The quantity *U* is the electric energy of the plates alone, and it does not include the energy of the large charge reservoirs, batteries, or power supplies that are necessary to maintain the plates at constant potential as the cantilever moves. The energy of these charge sources or sinks do work in moving charges to maintain the potentials, so their energy changes. When this is properly included, it turns out that it is the positive derivative of *U* that determines the force [26].

3.6 Repulsive Electrostatic Force

It is important to show that total electrostatic force applied on top plate is repulsive and find out what conditions are required for this to be valid. First we present a handwaving argument that proves the force to be repulsive in simplified conditions. We can simplify three plate system to three individual systems of two plates. Figure 3-1 has a simplified diagram of this problem.

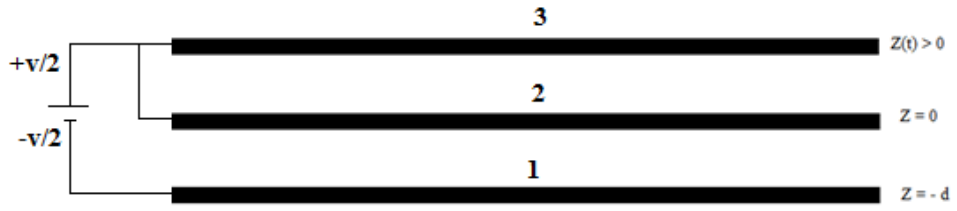

Figure 3-1 Schematics of simplified three plate system for this device.

In such case, using equation 29 and 28 to solve off-diagonal elements in terms of plates' distances and dimensions results in:

$$C_{12} = \frac{-L^2}{2\pi d} \qquad C_{13} = \frac{-L^2}{2\pi(d+z)} \qquad C_{23} = \frac{-L^2}{2\pi z} \tag{32}$$

Putting these definitions back into equation 31 and taking z derivative of each term we get the force in terms of our system configuration as follows:

$$F = \frac{V^2 L^2}{8\pi}\left(\frac{-1}{(d+z)^2} + \frac{1}{z^2}\right) > 0 \tag{33}$$

This force is always positive meaning it is upward and repulsive on top plate. It is important to notice that this is a handwaving argument and is not intended to give accurate values for total electrostatic force on the plate.

To drive a more accurate value for total electrostatic force on top plate we used a commercial software called FastCap [27] to calculate each coefficient and use equation 31 to drive total force. Figure 3-2 (upper) plots the six *z*-dependent coefficients calculated by FastCap for 10 µm x 10 µm plates. As z increases, the magnitude of C_{13} decreases due to fringe-field weakening, which lessens induced charges. Generally, however, the z-dependence of all the C_{1j} is very weak, because the surface plate screens the buried plate from the field of the cantilever, whose motion therefore has little effect on the buried plate's total charge. [18] This allows us to ignore the derivatives of those three coefficients in equation 31, giving:

$$F \cong \frac{V^2}{8}\left[2\frac{\partial C_{23}}{\partial z} + \frac{\partial C_{22}}{\partial z} + \frac{\partial C_{33}}{\partial z}\right] \tag{34}$$

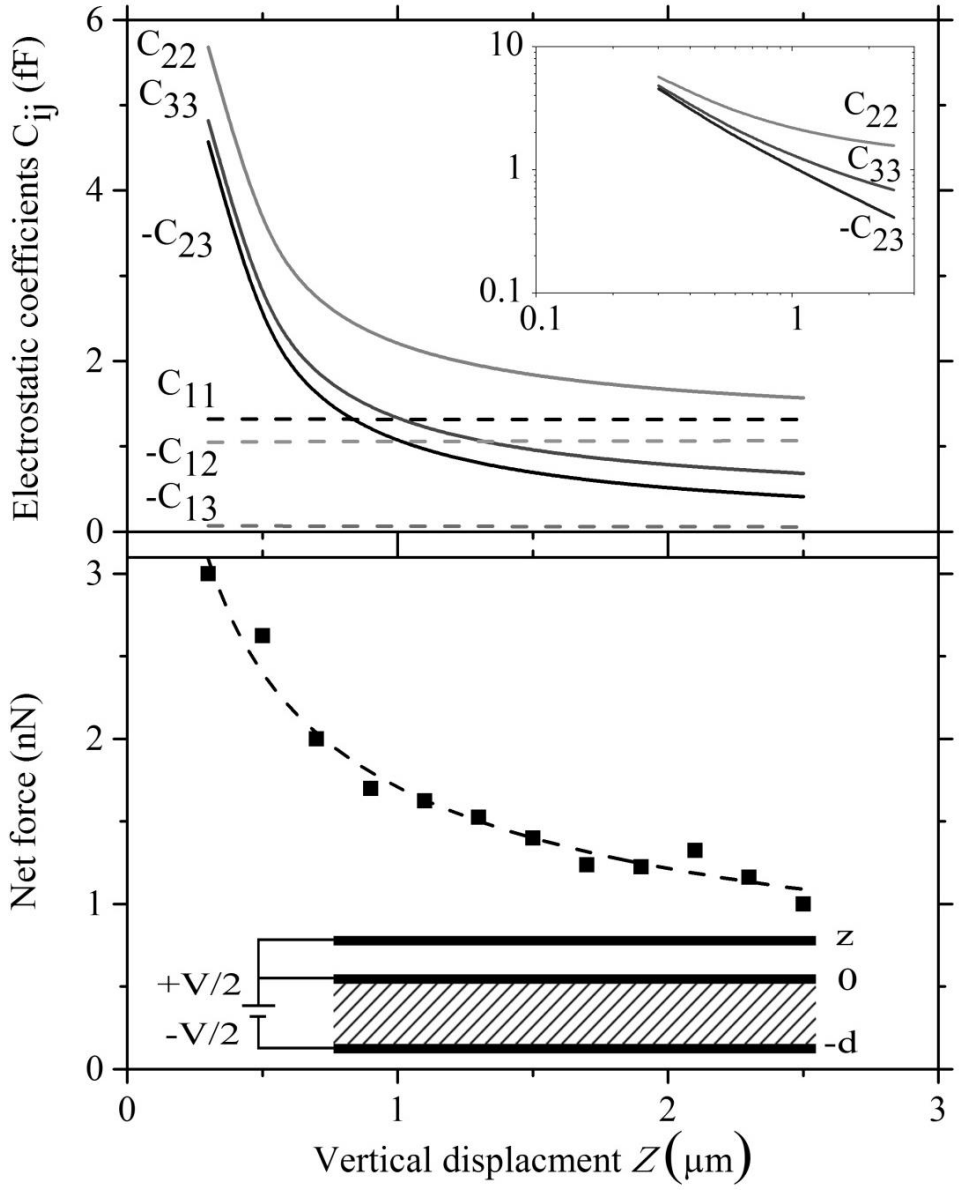

Figure 3-2 (upper) Coefficients C_{ij} for system of three parallel square plates as a function of the cantilever height z for plate area 10 μm x 10 μm. Inset: log-log plot for three of the curves. (lower) Net force on 10 μm x 10 μm cantilever vs. its height above the surface for 20 V bias. Symbols are calculation results. The line is a fit to $\frac{1}{\sqrt{z}}$. Inset: Model schematic. [18]

The induction coefficient C_{23} (which is negative) approaches zero with increasing separation of the two upper conductors, as expected, so that dC_{23}/dz is positive. The

positive coefficients of capacity C_{22} and C_{33} are expected to decrease to constant positive values as the separation between the top two conductors increases, and we expect $C_{22} > C_{33}$ because the surface plate is near to two plates while the cantilever is near to just one. These expectations are also confirmed in figure 3-2, upper. Thus the z derivatives of these coefficients of capacity are negative. The inset in figure 3-2 upper presents a log-log plot of the three coefficients in equation 34. The slope of $-C_{23}$ is more negative than the slopes of the other two, so that the first term in equation 34 exceeds the sum of the magnitudes of the other two terms. Hence, the total force is positive. In other words, the direction of the force is the same as if the cantilever is being *repelled from* the surface. (We eschew the convenience of phrases such as "repulsive force" and "repelled *by* the surface" to avoid conceptual controversies associated with the fiction of force at a distance. Each conductor feels only the negative pressure due to the fields at its own surface [26]. Integration of this pressure over the surface gives the net force [24] and confirms the sign found here.)

Figure 3-2 (lower) plots the calculated force (equation 34) using coefficient values from figure 3-2 (upper). The net force is positive in the considered range 0.25 μm < z < 2.5 μm, which are the motional limits in the experimental device. The force decreases as the separation increases. Over the range considered, the force is adequately described by a power law. The line shows a fit to the function $\frac{1}{\sqrt{z}}$. That line reveals a small oscillation with z in the force data, which is an artifact due to meshing, as determined using higher mesh density at the expense of longer calculation times. When the permittivity of the structural oxide in the actual device is included [24], the force magnitude increases nearly four-fold in comparison to that presented in figure 3-2 for the simple model system.

3.7 Conclusion

In this chapter we used energy formalism to derive total electrostatic force on top plate in a MEMS device. Using this formalism we calculated total force as function of capacitance matrix elements. Using two separate approaches of handwaving argument based on dimensional analysis and direct calculation of capacitance coefficients we showed this force will be toward positive z direction meaning an upward or repulsive (with respect to substrate) on top plate. We furthered analyzed behavior of each capacitance matrix element and explained its behavior with change in vertical position of top plate.

Without a surface plate, the force on the cantilever would be downward toward the oppositely biased buried plate. On the other hand, if the surface plate were much larger than the others, it would screen the buried plate so that there would be no fields from it at the cantilever, and hence no force on the cantilever. As found above, the force is upwards for plates of equal dimensions. Thus, were the surface plate to increase in size monotonically from zero, the force would change from downward to upwards before decreasing again to zero. There will be an optimum surface plate size that maximizes the upward force.

Further understanding of device electrostatic behavior requires more complicated model that consider other factors such as plates with different sizes and different dielectric constant in between. We will approach this problem in next chapter by finite element analysis to achieve more in-depth understanding of this device.

CHAPTER 4 FINITE ELEMENT MODELING

4.1 Introduction

In previous chapter we used theoretical analysis based on values of position-dependent coefficients of capacitance and electrostatic induction to demonstrate the sign of the force on the cantilever and determines its magnitude. In this chapter we use finite element simulations of local fields to confirm these results and give the distribution of the force across the cantilever. Size and motion effects have been studied. Finally an optimum design is suggested to achieve highest repulsive force and best performance.

First we will explain fundamentals of finite element analysis and software we used. Then we will explain our model and its elements. We will then go through our simulation results and their interpretation. Finally we conclude with optimum factors to achieve highest possible electrostatic response from our device.

4.2 Fundamentals of Finite Element Modeling

Solving a physical problem requires multiple steps usually starting with defining differential equations that describes physical system. Whether it's a heat flow problem or electrostatic or a simple point mass in a uniform gravitational field there will be one or more differential equations that their solutions describe the behavior of physical characteristics of the all elements in the system, like temperature, electric potential or position and velocity of particles in our system. Next step in solving these problems is to define boundary conditions. These are values that most of the time are determined by real cases of the problem. In given examples above these could be like temperatures, electric

charge or initial position and velocity. In a general problem however, you can keep these values as parameters and solve the model as a dependent to these parameters to obtain a general understanding of that physical system with different boundary conditions.

Most of the time it is nearly impossible to thoroughly solve these equations analytically and find a mathematical model that describes all aspects of the system. This is especially the case when system has many objects that interact with each other or more than one physical aspect of a system are under investigation with assumption of that these aspect are dependent to each other. An example of such systems can be more than three bodies with masses in gravitational fields of each other or heat flow through an electrostatically charged dielectric in liquid form. In reality only very simple systems with symmetries and simple boundary conditions are describable completely by analytically solving their governing differential equations.

Finite element method (FEM) [28] is a powerful tool in more complicated situations. In this method, a complex physical system is subdivided into non-overlapping finite elements with simple geometry. Behavior of each element is described in terms of finite number of values sets of nods. Overall behavior of the system is then obtained by connecting these nods and defining interaction between neighbor elements. In an example of heat flow in an object this can be done by considering it as a collection of many thin sheets stacking on top of each other where temperature is constant across each sheet but changes as we move from one to another.

FEM is still an approximation technique, but its accuracy can be improved at the cost of longer processing time like many other numerical methods. To solve a problem

using finite element method, following elements are typically required as input for the solver:

- Elements geometry: to describe the system it has to be divided into finite number of element with known shapes and sizes. This is usually done using meshing method, where user defines overall geometry of the system, then using a meshing algorithm, software will divide it into finite number of elements. On most software packages, this can be done either by the software itself or by another software when final mesh can be imported into the solver. More information about meshing methods can be found in [29].
- Nod positions: Nods are where numerical values of system characteristics are defined for each elements. These points are where mesh lines are intersecting with each other. Hence they are obtained as another output from meshing procedure.
- Body properties: Each object will be defined with certain physical properties other that it's geometry such as its mass density, charge density, viscosity etc. Depending on the physical problem we are trying to solve, certain number of these physical properties have to be defined.
- Boundary conditions and restrains: As mentioned earlier, to have known values for system parameters as solution of FEM, we need to define initial state of the system and any possible restrain that system has to follow. An example for a restrain is fixed volume of a gas container while a boundary condition can be a fixed temperature at the walls.

- Governing physical model: Although in reality a physical system will have all possible physical properties, we do not usually want to know them all. This is where physics is taking a part. It is our job to identify which parameters we are interested in and how they are interacting with each other in real system. This will be done by defining one or sets of differential equations. Most of modern FEM software packages come with predefined models and equations. But it is still user responsibility to define valid equations in the model and adjust them as suited for the problem.
- Solver parameters: Although fundamentals of all FEM are the same, there are many parameters in solver package that define how it will attempt to solve the problem and when it stops. These can be as simple as convergence error, which defines what percentage of tolerance in final answer is acceptable or factors like solution methods that requires more in-depth understanding of both physical model and how different methods work. Once again, most of modern FEM packages come with predefined methods and values suitable for different physical models. It is however the user's responsibility to ensure that those choices will suit the problem and their results are accurate and close to natural behavior of system. To do so, it is usually recommended to try a simpler problem with known solutions and compare the solution to figure out all required solver parameters, and then attack physical problem of interest.

A typical FEM process can be simplified as follow:

1. Design the object.
2. Discretization of the designed object into elements and connect them at nodes.
3. Define equation sets that describe system behavior.
4. Solve equations for elements considering their interactions.
5. Calculate system properties based on final values obtained for elements.

FEM obtains unknown parameters of physical system by defining an energy functional which includes all energies related to elements of our system of interest. Solver then tries to find a solution where this functional is minimized due to conservation of energy, by setting the derivatives of functional with respect to unknown grid points potentials to zero. [30] Result can be defined as condition where equilibrium is achieved.

4.3 FEM Software Packages

In this section we will provide a quick overview of FEM software packages used for modeling of our device behavior. Although many FEM software packages are available commercially, we have decided to use an open-source package. This decision was based on wider range of capabilities that we could achieve through them and higher educational value. Two main software were used for modeling of this device. A short description of each will come next.

4.3.1 Gmesh: Grid Generator

Meshing process was done by Gmesh [31]. Gmesh is a 3D open source finite element grid generator with built-in CAD engine and post-processor.[31] It has four main

modules: geometry, mesh, solver and post-processing. However, in this project we only used geometry and mesh modules of this software. In order to be fast and light software, Gmesh is written in C++.[32] Although it can be used as a stand-alone user-friendly software, it is also scriptable and can be integrated inside a larger computational package. Figure 4-1 is a screen shot of Gmesh with designed and meshed 3D cube.

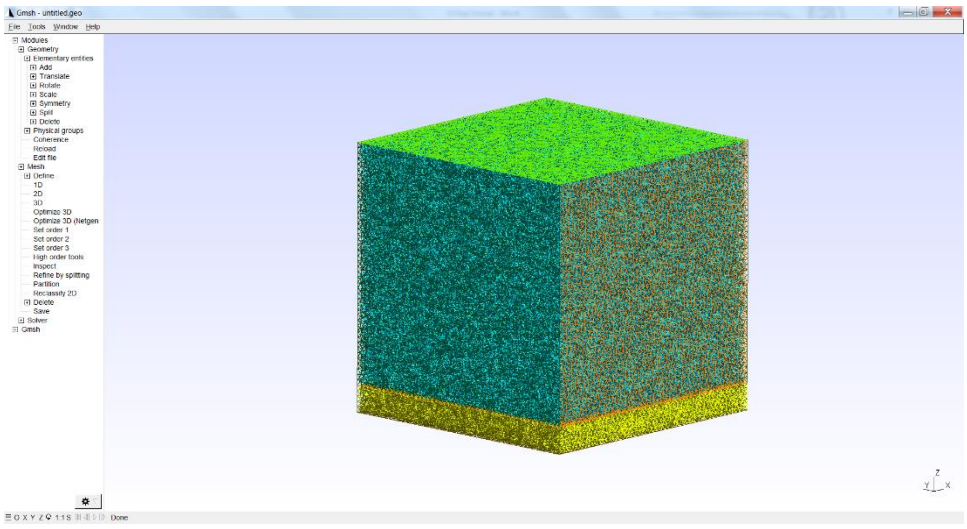

Figure 4-1 Screen shot of Gmesh with a designed and meshed 3D cube with different layers and physical properties on each surface.

Geometry module is where overall shape and geometry of physical system has to be defined. Design of the object is done through sequences of defining points, lines, surfaces and volumes. Tools like translation, rotation, scaling, symmetry producers and splits can be used to accelerate designing process. Many other design formats can also be imported into Gmesh. Geometry script file is easy to understand and manipulate in case user is more interested in scripting the geometry rather than using user-interface tools.

Mesh module is responsible for generating elements and nodes required for finite element modeling. User is responsible to define a mesh size which defines how large each element can be in final meshed object. Mesh size can be defined as a single value or as a function of location in the object. For example, in meshing an infinitely large parallel plate capacitor with no priority between locations, it is reasonable to have a uniform mesh size. However, if we are interested in understanding of fringe fields close to the edge of a finite parallel plate capacitor, it is now more logical to have smaller elements close to the edge than points far away from it. Figure 4-2 demonstrate the difference between the two cases in 2D plate.

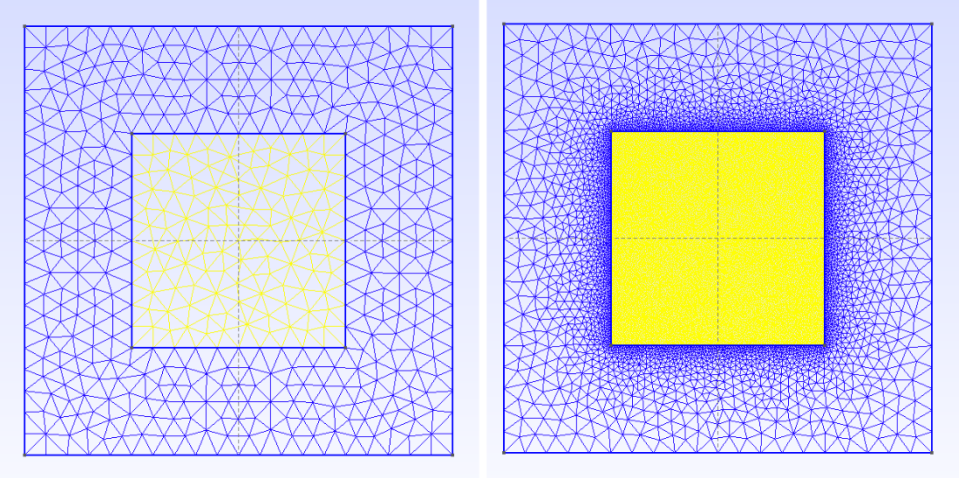

Figure 4-2 Comparison of single value mesh size (left) and location dependent mesh size (right).

4.3.2 Elmer: FEM Solver

Once mesh file is ready it is imported into a FEM solver. For this project we used an open-source FEM software package called Elmer. As an open source package, it allows users to modify pre-defined solution process to create a new solver suitable for their

models.[33] It covers wide range of physical models and numerical methods. One of disadvantages of Elmer is lack of its own proper mesh generator. However it lets users to import mesh files from various other software including Gmesh.

Elmer has different executables that some are explained briefly below:

- ElmerGUI: It is a user interface for Elmer package. Here mesh or geometry files can be imported. User will define material properties, boundary conditions, physical models and solution methods in this interface. It also includes a real-time convergence monitor that informs the user about the progress of simulation once it starts.
- ElmerSolver: This is where problem is solved. Once all parameters are set in ElmerGUI by user, it generates a code which will then be used by ElmerSolver to solve the problem.
- ElmerPost: This executables is in charge of post processing ElmerSolver results. It has user-friendly graphical interface.
- ElmerGrid: It can import mesh files of other software packages or generate and manipulate simple mesh files on its own. This part still needs development and hence we decided to use an external mesh developer for our modeling.

Figure 4-3 shows an interface of ElemrGUI where main part of modeling is done. It shows the 3D model of 3 parallel plate conductors surrounded by world walls. World walls are required to define boundary conditions at infinity.

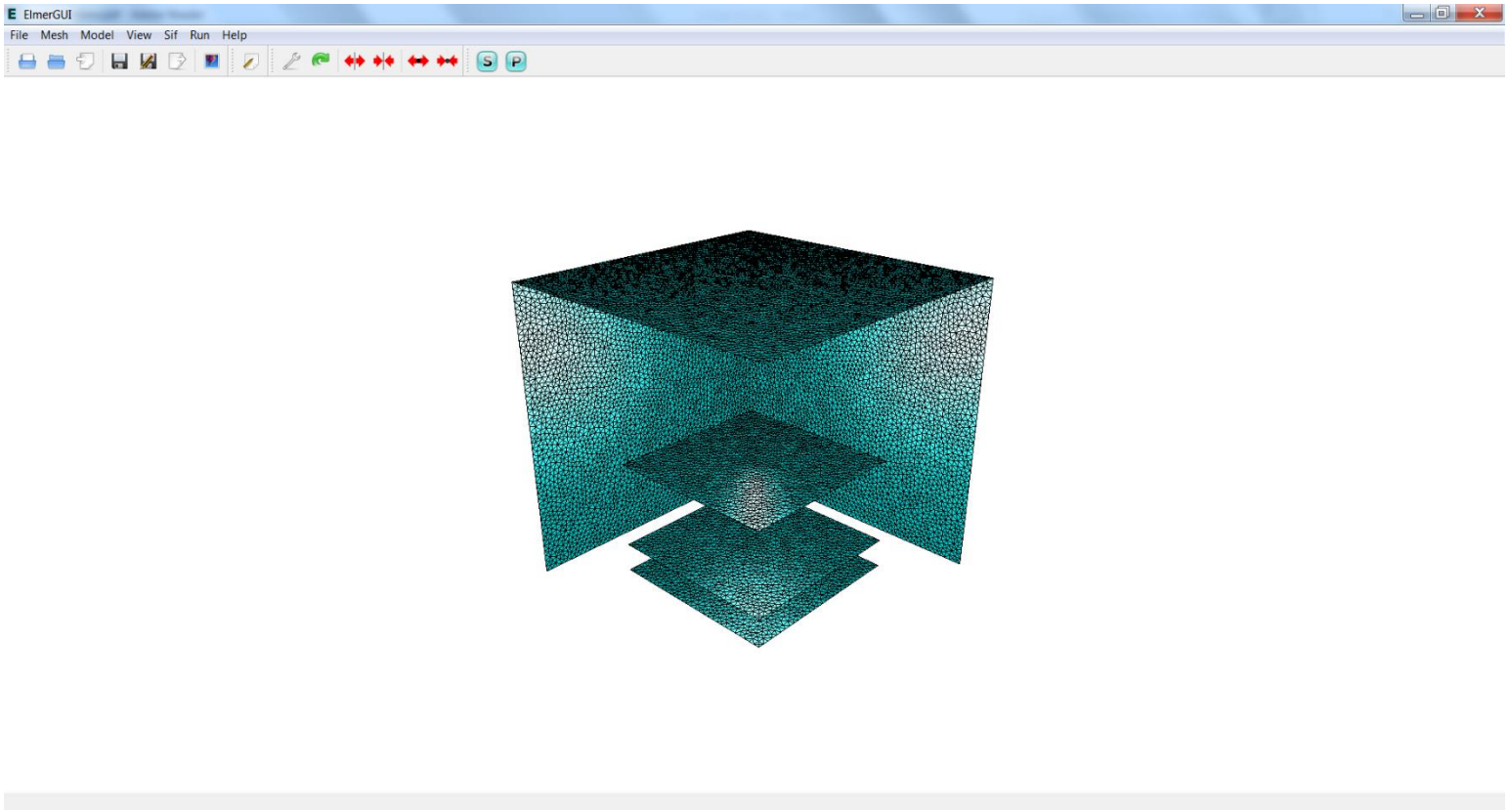

Figure 4-3 ElmerGUI Interface. Shown object is meshed 3D model of three plate capacitor. Some of surrounding world walls are hidden to show 3 plates. Volume mesh is also hidden.

4.4 Device Modeling and Results

In chapter 3 we studied simple case where plates are all square and have same size. We showed by means of analytical derivation of force as function of coefficients of capacitance and inductions which were calculated by FastCap, a commercial solver [27], that cantilever will experience repulsive electrostatic force. Here we will investigate design parameters to optimize and maximize electrostatic force and also understand the limits of cantilever. This will be done by finite element simulation of system to drive electric force applied on the cantilever. We will also compare electrostatic force for a more realistic design [15] with Casmir force as one of the major obstacles in lifting MEMS devices while they get close to the surface.

To calculate the electric field distribution, we used the finite element software Elmer [33, 34]. A 2D mesh was designed for the 3 plate configuration of figure 2-1 using Gmesh 2.7 [31]. The cantilever is given 100 nm thickness while surface plate and buried plate were considered as two dimensional sheets. The minimum mesh size is set to 100 nm to reveal any dependence on plate thickness. The volume surrounding the plates is given a permittivity of air. Elmer calculates the distribution of the potential and electric field E.

Figure 4-4 presents the resulting spatial distribution of the vertical component of the electric field vector when all three plates are squares of 10 μm dimension. Since electric field at metal surface is normal to the surface, there is no horizontal electric-field component at the boundaries. The buried plate potential is -20 V while surface plate and cantilever are at +20 V. The field between surface and buried plate is strong and negative (downward). A negative fringe field extends to the bottom outer edges of cantilever, but

the fields on top of cantilever are positive. The fields both above and below the cantilever approach zero near the center, but the positive field on top drops more slowly.

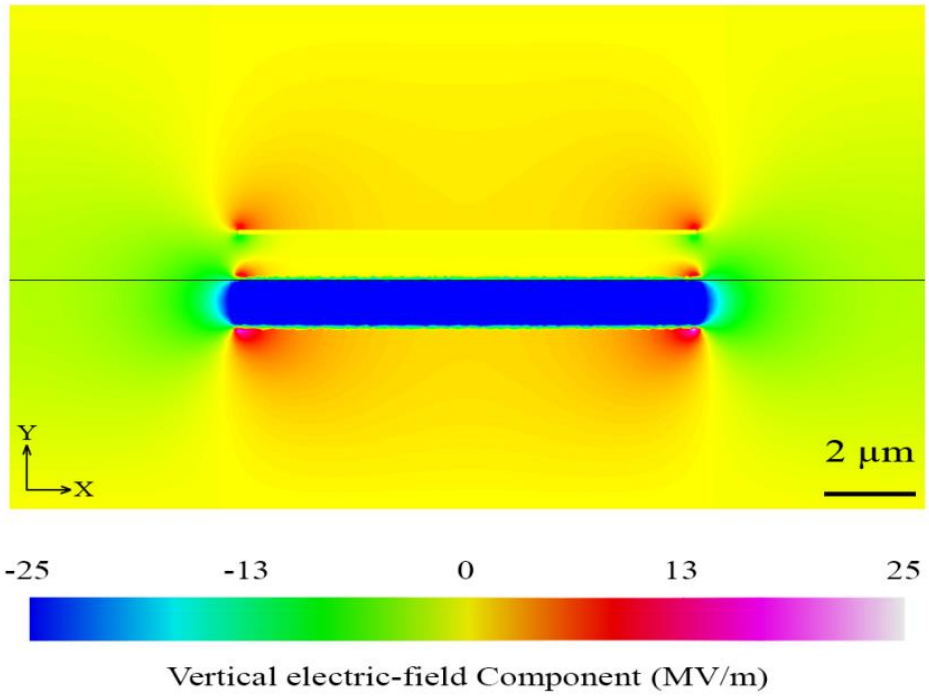

Figure 4-4. Electric field distribution of 10 µm long 3 parallel plate system. Top and middle plates are at +20 V while bottom plate is held at -20 V. Gaps between plates are 1 µm. [24]

Field values are imported into Mathematica [35] for integration over the surface. Since fields peak near the edges, it is critical that all integrals have exactly the same limits. To ensure this, we perform a first order interpolation before integration. We then integrate the value of the negative electrostatic pressure $(1/2)\ \varepsilon_0\ E^2$ over top and bottom cantilever surfaces to find the net electric force density in N/m. Figure 4-5 presents a plot of the total force acting on cantilever as a function of surface plate lengths, holding the dimensions of the buried plate and cantilever constant. Figure 4-5 (inset) shows the cross-over region,

where the force becomes repulsive. This appears when the surface plate length is 95% of cantilever length, and it peaks at 105%.

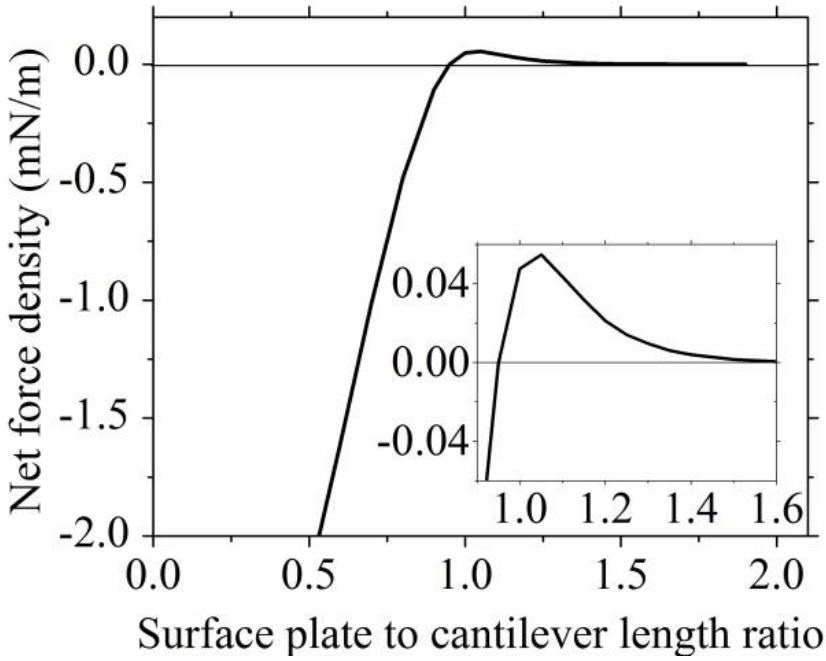

Figure 4-5 Net force density vs. size of the surface plate relative to that of the cantilever. [24]

Figure 4-6 presents a plot of the maximum net force density vs. the vertical position z of the cantilever. The surface plate length was taken to be 5% larger than the others to achieve maximum net force, according to figure 4-6. The force becomes negative when z exceeds ~ 2.3 μm.

The 2D calculations (figures 4-5 and 4-6) lack two of the edges and all of the corners compare to real 3D case. Since these are the locations of highest charge density and surface fields (figure 4-4), these calculations underestimate the magnitude of the

repulsive force. We may speculate that the cross-over for the force density in figure 4-6 to negative values at 2.3 μm is similarly an artifact of 2D calculation.

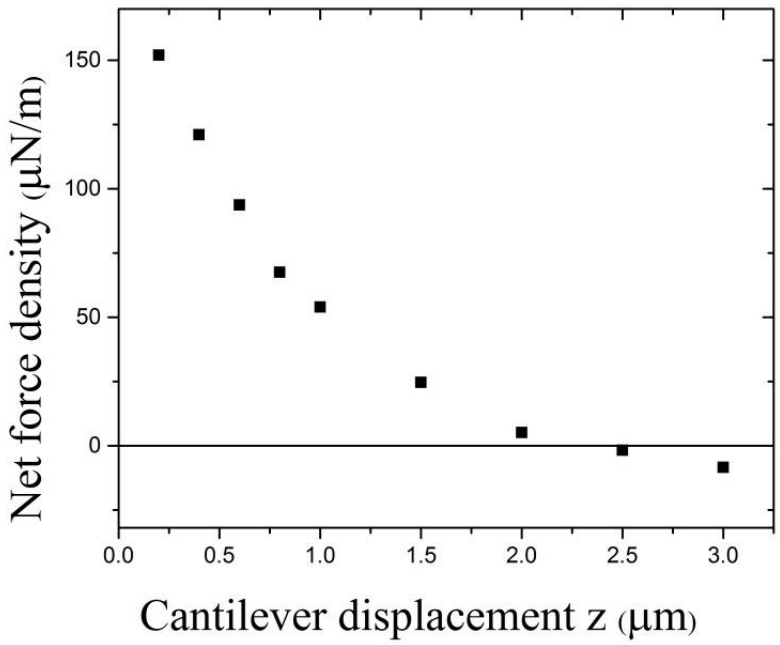

Figure 4-6 Net force density vs. cantilever displacement. [24]

Figure 4-7 presents the spatial distribution for the vertical component of the electric field at z = 1 and 3 μm. As the height increases the negative fringing fields penetrate more into the space under the cantilever, while the positive field on top gets weaker. The net force eventually changes sign. Figure 4-7 (top) represents a repulsive situation, while figure 4-7 (bottom) represents an attractive net force. Higher damping points where net force becomes negative require larger surface plate to insure screening of attractive fields.

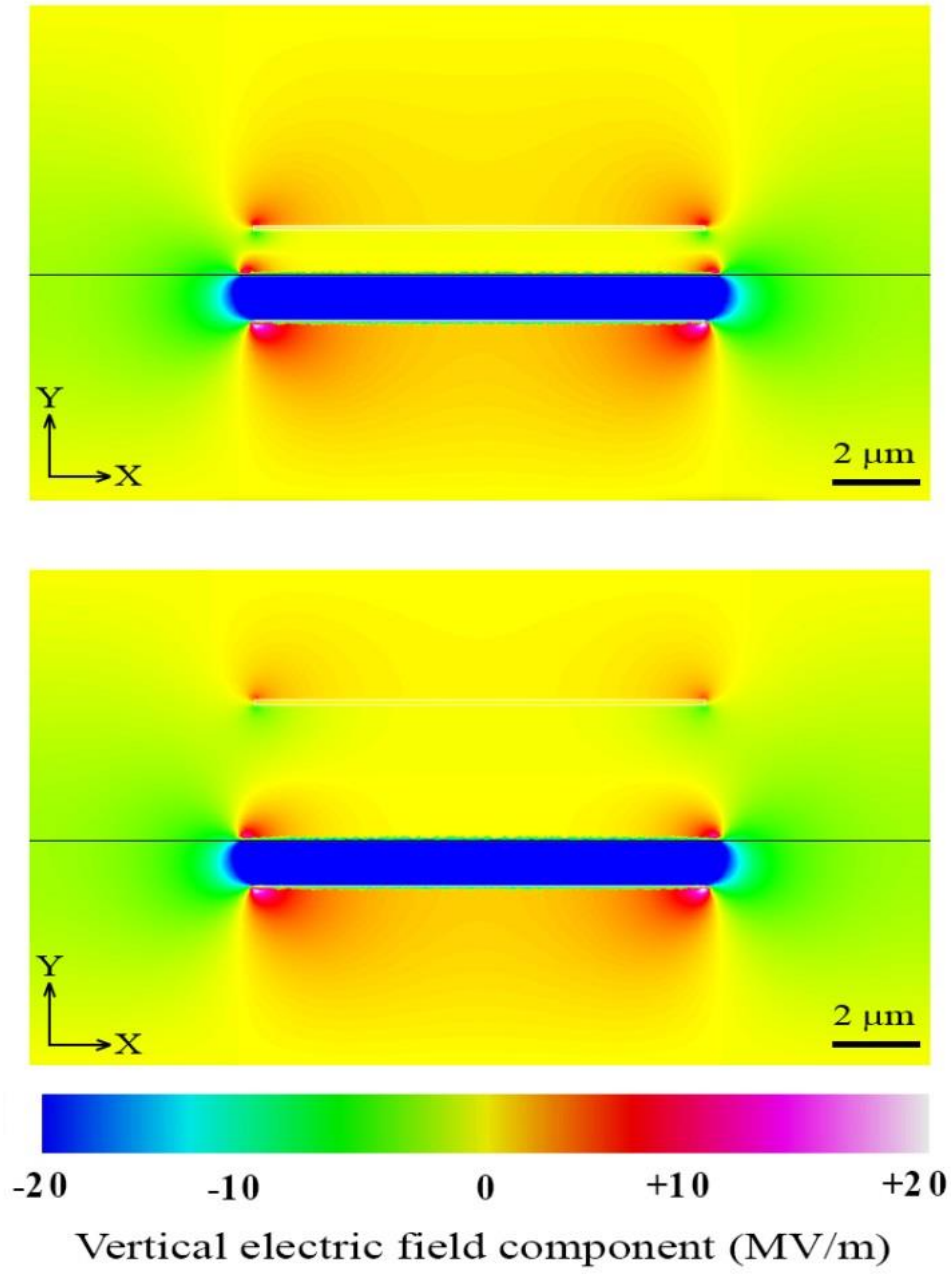

Figure 4-7 Distribution for the vertical component of the electric field vector (V/m) for z = 1 (top) with repulsive force on top plate and 3 µm (bottom) with attractive force on top plate. Dark line in the middle shows where surface is located.[24]

Figure 4-8 presents the net force as a function of surface plate to cantilever size ratio for the different cantilever heights indicated in microns next to each curve. For larger separations z, the optimum ratio increases. The maximum achievable net force is a decreasing function of z.

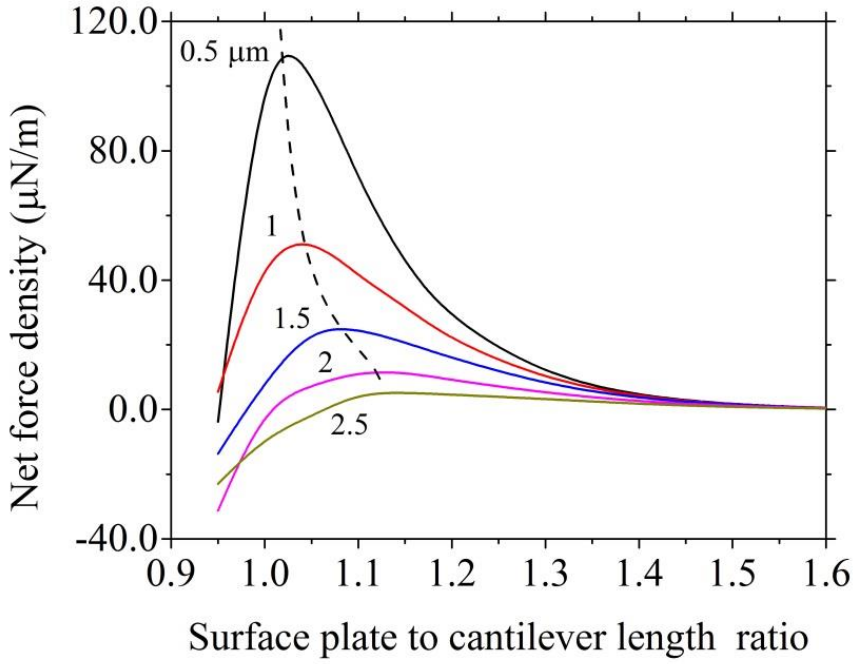

Figure 4-8 Force Density vs. surface plate to cantilever length ratio for cantilever heights z. The z values are indicated next to each curve in microns. [18]

4.5 Conclusion

In this chapter we briefly described finite element method of modeling and its fundamentals. Then we introduced two FEM tools we used in this project to solve our three parallel plate conductor problem. We described our modeling parameters and simulation results. After solving electric field surrounding the plates we calculated total electrostatic

force applied on top plate and showed that only for certain range of top plate to bottom plate length ratio this force will be repulsive. Further we found that this force is maximized for specific top plate to bottom plate length ratio which defines our optimum design dimensions to achieve highest possible electrostatic force. We also investigated change of this optimum point and maximum force by increasing the distance between top plate and bottom plate. Results demonstrated that as this distance decreases, this maximum force happens at shorter length ratio but always happens for the cases that top plate is larger than bottom plates. This maximum force magnitude also decreases as we increase two plates separation which is expectable by common logic too.

CHAPTER 5 FABRICATION

5.1 Introduction

So far we have demonstrated theoretical aspects of the device by means of analytical calculations and simulations. In this chapter we will review fabrication of this MEMS device.

We have fabricated three prototypes of optimized device, single pixel with 100 µm pitch, single pixel with 50 µm pitch and 3x3 arrays of pixels with 20 µm pitch. Different methods of deposition and fabrication have been tried to achieve best possible quality of structure for the device. Innovative methods are used in different parts which will be explained in details. [18, 19]

Processing steps can be summarized in the list below:

- Buried plate fabrication
- Surface plate fabrication
- Anchors and Tip fabrication
- Arms and Cantilever fabrication
- Release

Although one of the first steps in this device full fabrication is making electric pads were bias will be applied, we present it only at the end of this chapter for fabrication of 3 by 3 arrays, since they are easy to fabricate and their shape and positions are irrelevant to main structure of the device as long as they are made far enough from the pixels so that their electric fields are small and ignorable. In our experience this was satisfied for distances more than twice the device length. All fabrication processes have been done in UCF

physics department cleanroom facility and CREOL Nano-Fabrication facility. We will explain each of these steps in detail and provide schematics and images of fabricated device.

5.2 Buried Plate Fabrication

Lower most plate is buried plate which is hidden under substrate surface. Devices are fabricated on top of Silicon wafers. In first step silicon is spin coated with a layer of photoresist and then plate patterns are transferred to them by photolithography process. After resist development, 100 nm of Cr is deposited by e-beam evaporation and then lift of process is done to pattern silicon with Cr. Finally we coat all surface with 500 nm of TEOS based PECVD Silicon dioxide. These sequences of fabrication are demonstrated in figure 5-1. Reactive ion etching (RIE) opens a via in the oxide for buried plate biasing. This step however, is skipped in figure 5-1 since it is irrelevant to fabrication of main device structure and will be explained when electrical pads fabrication is demonstrated.

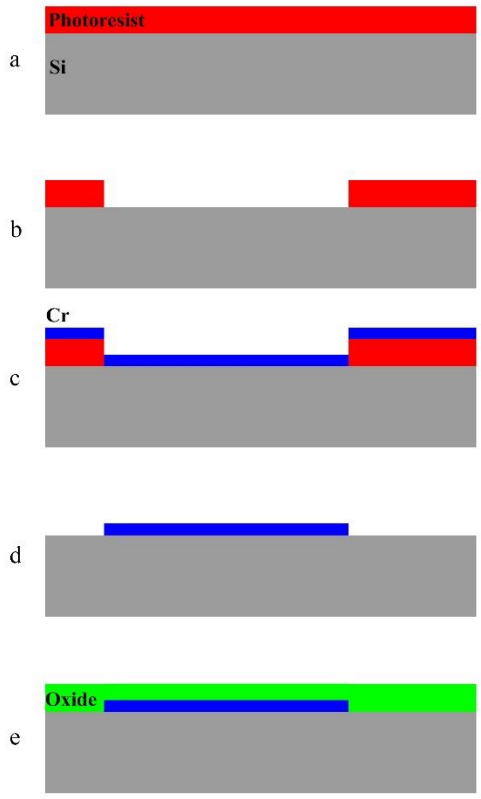

Figure 5-1 Steps in fabrication of buried plate. a) Spin coating Si with photoresist and baking. b) Photolithography and pattering resist with buried plate mask. c) 100 nm Cr deposition. d) Lift off. e) 500 nm silicon dioxide PECVD deposition.

5.3 Surface Plate and Tip Pad

This part is similar to buried plate fabrication. Device Electrodes are fabricated in the same step as surface plate and to keep them from oxidation over time and enhance electrical connectivity we fabricate them in Au. However, Au does not have a good adhesion to silicon dioxide. As a solution, we deposit 10 nm of Cr before Au deposition. These two depositions have to be done in same chamber without breaking the vacuum immediately after each other to avoid oxidation of Cr layer. We also made a small pad separate from surface plate which will be connected to an external circuit for sensing tip

connection to the surface and another pad under anchors which is used for providing top plate bias. In a more simplified device, anchors pad and surface plates can be connected since they are held at same bias. Figure 5-2 demonstrate these sequences.

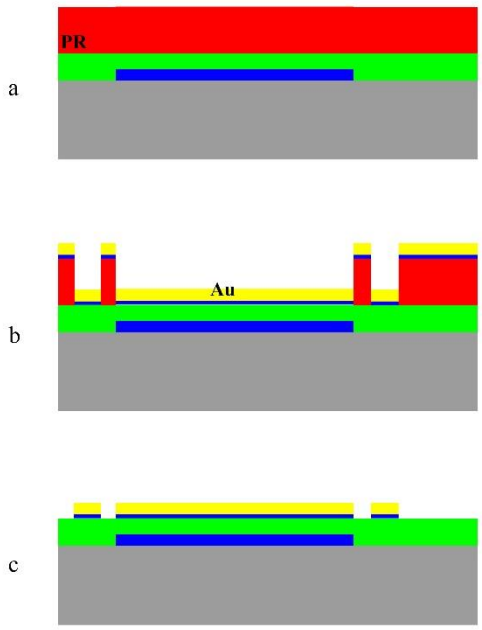

Figure 5-2 Processing steps for fabrication of surface plate. a) Photoresist spin coating. b) 10 nm Cr and 100 nm Au deposition. c) Lift off.

5.4 Anchors and Tip Fabrication

This is one of the more complicated steps. It started by spin coating the surface with 3 µm of sacrificial layer. In this project we used ProLift 100 from Brewer Science [36] which is a polyimide soluble in positive resist developers. However, we experimentally found that it can be paired with both positive and negative resists which have TMAH base developers, such as MF319, RD6, etc. It features good resistance to acids and organic solvents. Although ProLift is a good sacrificial layer, it cannot be patterned. To overcome

this problem, we spin coated ProLift surface with photoresist and then patterned our photoresist layer using photolithography process. Then we used a TMAH based developer to co-develop photoresist and ProLift at the same time. Partial co-development created a divot in the ProLift above the tip pad, and this divot was then filled with Cr to form the tip metal. Then spin coating and pattering was repeated again to produce anchor holes through the sacrificial layer to the surface plate, this was done with same co-development technique but with longer times. Once all of these steps are done, we coat sample with 500 nm of Silicon dioxide which will work as main structure material for our device. Figure 5-3 summarizes these fabrication steps.

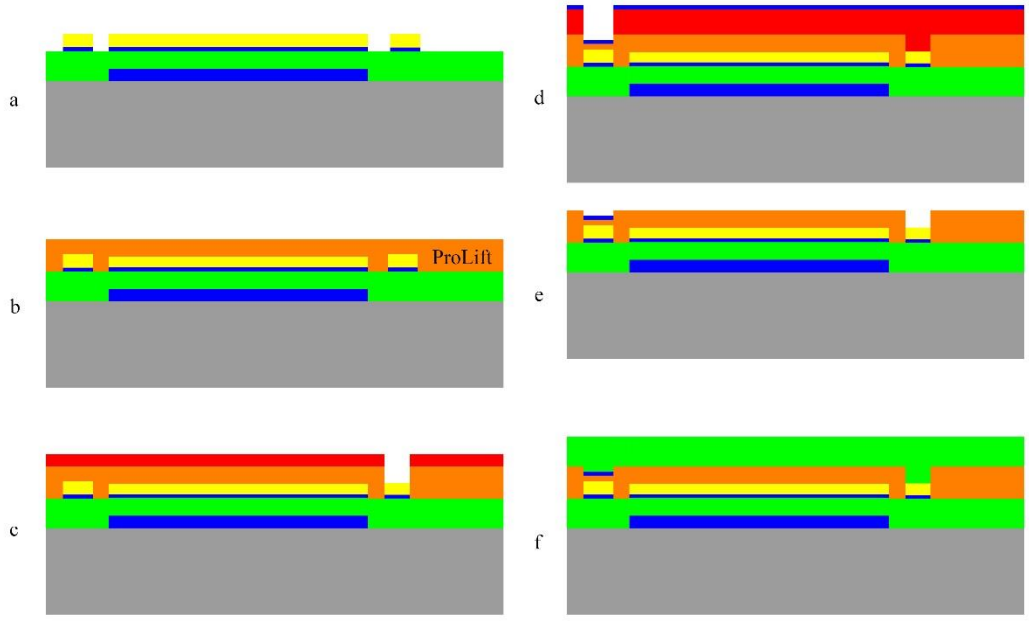

Figure 5-3 Summarized fabrication process for tip, anchors and structure oxide. a) Starting with pre-patterned surface plate, tip pad and anchor pad. b) Sacrificial layer (ProLift) spin coating. c) Photoresist spin coating and creating anchors pattern into ProLift. . d) Spin coating, patterning and Cr deposition for Tip metal. e) Lift off. f) PECVD SiO_2 deposition.

5.5 Arms and Cantilever

This step is where main structure is made. In our design two pairs of arms are present as explained earlier. One pair are connected to anchors and only have very thin layer of metal to provide electrical continuity between pads under anchors to top plate. These are located on outside and we call them isolation arms since they are thermally isolating the device from losing heat through anchors. Second pair of arms are located inside and have thicker layers of metals on top. These arms are called bimorph due to their designs. Bimorph arms are responsible for bending the cantilever up and down by heat due to the difference in thermal expansion coefficient between structure oxide and thick metal layers. Although metal thickness are different at these two pairs of arms, we are only demonstrating one of them in cross section illustrations for fabrication.

A very important objective in this step is to adjust device stress and initial position so that it touches the surface in the absence of external forces. This goal is achieved by low temperature deposition of bimorph metal layer. To do so, we made a cooled stage in e-beam evaporator chamber and did experiments to achieve the right temperature for inducing such internal stress and hence strain in our device.

At this step we also have to provide electrical continuity between tip metal, top metal plate and anchor pads which are connected to external bias source. Additionally, to enhance release process of cantilever at the end of fabrication, we added few holes on top plate to increase etcher access to sacrificial layer. All of these steps are done with following fabrication process.

We started by patterning our cantilever structure on structure oxide. After photoresist spinning and photolithography of pattern, we deposited a thin layer of Cr and Au and then did the lift off to transfer the pattern. We repeated this process with a different mask to add additional metal on bimorph arms. Next, we used reactive ion etcher (RIE) with metal mask to etch through oxide until we reach to metals or ProLift where etch stops automatically. To connect top metal plate to tip metal and metal pad under the anchor, we did another set of photolithography, metal deposition and lift of to fill the holes in anchor and tip with Au. Figure 5-4 illustrates different steps of this process.

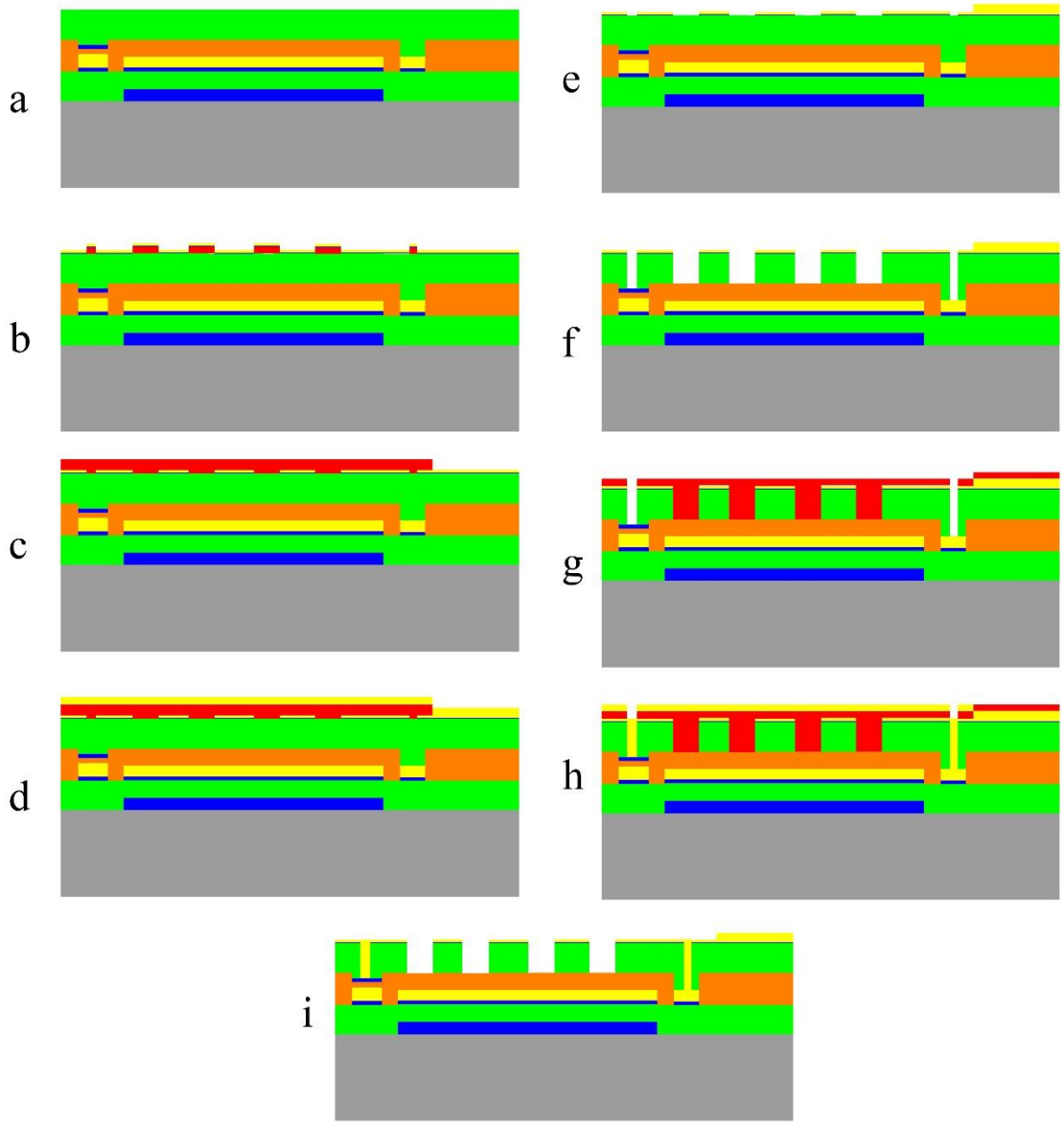

Figure 5-4 Fabrication process for top metal plate and providing electrical connection between plate, tip and metals under anchors. a) Starting point. b) Photoresist spin coating, patterning and metal deposition for release holes and access via to tip and anchor pad. c) Photoresist spin coating and patterning for additional metal on bimorph arms. d) Au deposition. e) Lift off. f) RIE with CF4 using metal masks to create access via to tip and anchors pad and release holes. g) Photoresist spin coating and patterning for anchors and tip access via. h) Angled Au deposition. i) Lift off.

5.6 Release

Last step in fabrication is the release process. Removal of polyimides used as sacrificial layer in fabricating MEMS devices can be challenging after hard-baking, which may easily result by the end of multiple-step processing. We considered the specific commercial co-developable polyimide ProLift 100 (Manufacturer: Brewer Science, Inc.).[36]

Polyimide is usually supplied commercially as polyamic acid precursors dissolved in an N-methyl-2-pyrrolidone (NMP) based solvent suitable for spin coating [37]. The polyimide studied here, ProLift100 [38, 39], contains 70-90% N-Methyl-2-pyrrolidone (NMP, C5H9NO), which suspends and dilutes the remaining 10-30% polymer solid. NMP has relative molecular mass 99.13, density 1.028 g/cm3, melting point -23 to -24.4 C, boiling point 202 C at 101.3 Pa, and vapor pressure 45 Pa at 25 C [40].

Excessive heat hardens this material, so that during wet release in TMAH based solvents, intact sheets break free from the substrate, move around in the solution, and break delicate structures. On the other hand, dry reactive-ion etching of hard-baked ProLift is so slow, that MEMS structures are damaged from undesirably-prolonged physical bombardment by plasma ions. We found that blanket exposure to ultraviolet light allows rapid dry etch of the ProLift surrounding the desired structures without damaging them. Subsequent removal of ProLift from under the devices can then be safely performed using wet or dry etch. We demonstrate the approach on PECVD-grown silicon-oxide cantilevers of 100 micron × 100 micron area supported 2 microns above the substrate by ~100-micron-long 8-micron-wide oxide arms. [41]

Although ProLift 100 is specified to withstand temperatures exceeding 300 C, we found that removal becomes more and more difficult the longer it is baked, even at temperatures within this limit. Such long baking is unavoidable in multi-step processes, including for example steps that involve PECVD growth of oxide.

Four types of ProLift 100 provide different spin-on thickness ranges. All experiments in this work have been done on ProLift 100-20 which gives thicknesses in the range ~1 to 4 micron.

Our MEMS device requires eight mask steps using both positive and negative photoresist. The most heating is caused by PECVD of silicon-oxide on top of the ProLift, 2 microns above the substrate, which bakes the ProLift at 300 C for ~30 min.

5.6.1 Hardened ProLift

Control of wet co-development is critical since ProLift dissolves in the resist developers faster than photoresist itself. Co-development time depends on the type of photoresist used and on pattern dimensions. Figure 5-5 presents our data for development vs. time in MF319 (2% TMAH) at room temperature using PMMA as wet etch mask for 100 micron pattern size in as-spun 1.5 micron thick ProLift without the usual hard-baking that results during our process (Solid triangles). This result shows that the ProLift is completely developed down to the substrate in about 50 seconds. Smaller patterns develop more slowly. Open triangles represent data for the same process on hard-baked ProLift, where it is obvious that the development rate has been reduced by more than a factor of 2.

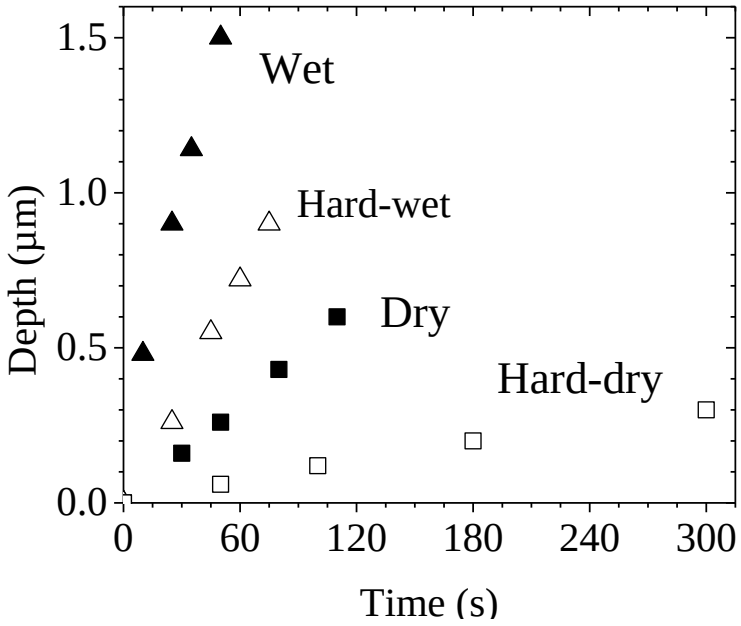

Figure 5-5 (Solid triangles) Wet development depth vs. time for bare 1.5 μm thick Prolift100-20 in MF319 developer at room temperature with PMMA mask and 100 micron pattern size. (Open triangles) Wet development for hard-baked ProLift (30 min at 300 C) with other conditions the same. (Solid squares) Dry plasma etch depth vs. time for 1.2 μm ProLift and 1 mm pattern size (Open squares) Dry etch data for hard-baked ProLift with other conditions the same.

Dry etch depth vs. time is plotted in figure 5-5 for 1.2 micron thick ProLift100-20 without long time hard baked, and 1.5 micron thick ProLift 100-20, which has been hard baked at 300 C for 30 minutes. Etching was done using Trion RIE with 150 W RF power, 750 mTorr pressure, 98 sccm O2, and 2 sccm CF_4 flow rate [42]. Brewer Science has reported different dry etch rates using different equipment and recipe [43].

After spinning ProLift, our process involves 11 minutes of photoresist baking at temperatures in the range 110 – 150 C and ~30 min at 300 C in the PECVD chamber during oxide growth. This excessive heat hardens ProLift so that release by either wet or dry method is more difficult and takes longer, as shown in figure 5-5. Development of 2 micron

thick un-baked ProLift takes a little over 1 minute in MF319 (2% TMAH), but after baking complete removal from under the cantilever paddle takes hours. We experimented with different solvents, including MF319 (containing 2% TMAH), 5% TMAH solvent, and ProLift remover (Brewer Science). In all cases, the hard-baked ProLift came off in slabs like "ice-floes". These move around on the surface, even without intentional agitation, and collide with the cantilevers, shearing them off. Optical microscope images of free floating ProLift slabs and a damaged cantilever are presented in figure 5-6. The floating sheets of ProLift are evident above and below the arms in the left image and on top of the contact pad on the right side of the right image.

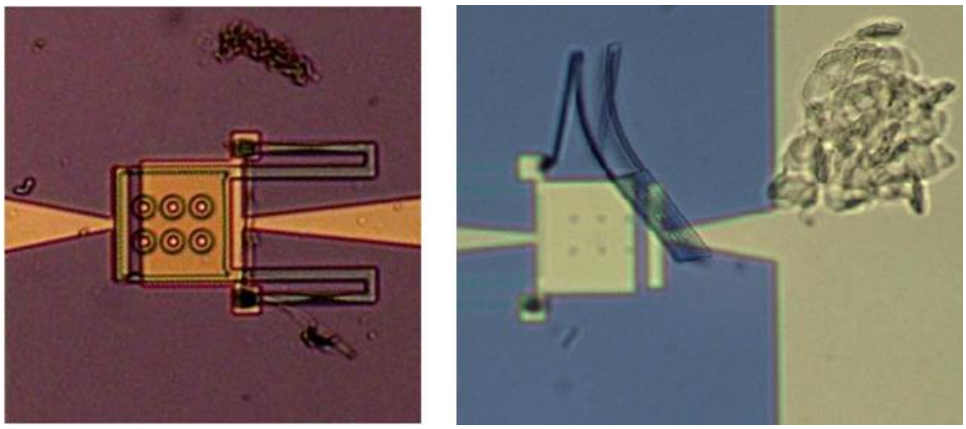

Figure 5-6 (Left) Optical microscope images of cantilevers during wet release process in MF319. ProLift sheets are coming off the structure. (Right) A cantilever broken by floating intact sheets of ProLift.

In the case of dry etch in oxygen plasma, long times are required to release cantilevers from hard-baked ProLift. During this process, physical bombardment by the plasma ions damages the cantilevers, as shown in figure 5-7. Here the cantilever arms

appear badly eroded while the paddle is still incompletely released. Additionally, black residue is left on the surface in form of grass caused by long RIE process.

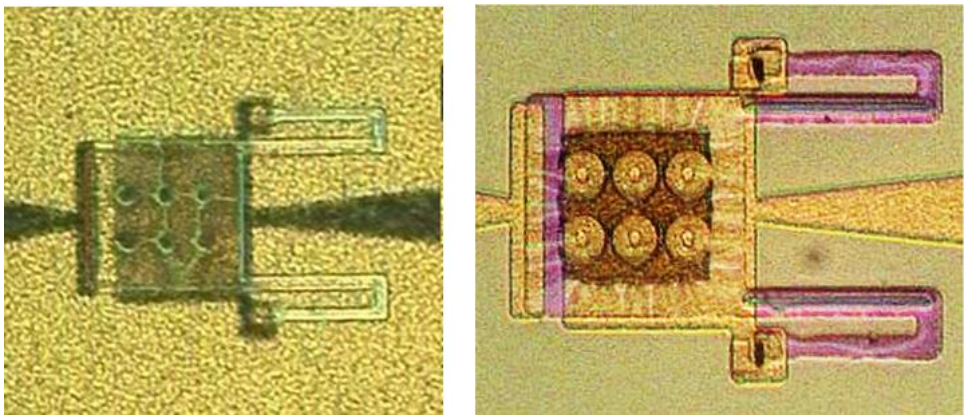

Figure 5-7 (Left) Black residue left by dry etching hard baked ProLift in oxygen plasma. (Right) A cantilever that has been partially released from hard-baked ProLift sacrificial layer by 55 minutes of oxygen plasma etch. The cantilever arms appear badly eroded by ion bombardment.

5.6.2 Solution to Hardened ProLift

Our solution is a multi-step release process. First, we blanket exposed the entire wafer with UV light at the range of 300-400 nm wavelength for six minutes using the source from our mask aligner. ProLift strongly absorbs this wavelength, according the spectrum in figure 5-8. This spectrum was measured in reflectivity R using a Perkin-Elmer UV-Vis spectrometer. The ProLift was deposited on a metal-coated substrate, so that there was no transmittance, and absorptance is given by 1-R.

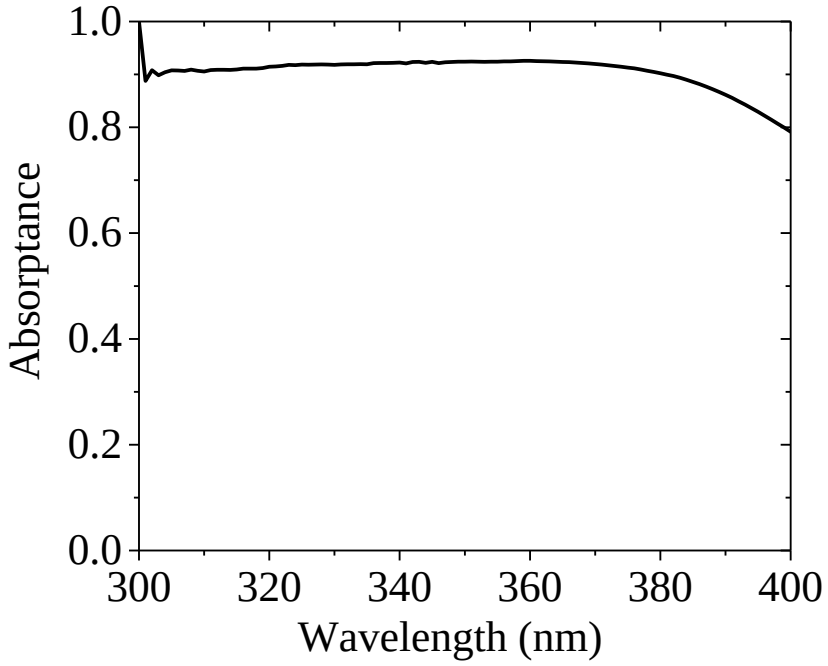

Figure 5-8 Absorption spectrum of ProLift in the range of 300-400 nm wavelengths.

Our hypothesis was that UV exposure would break the chemical bonds formed during heat treatment and at least partially reverse the hardening and resistance to etching. We did indeed find that the ProLift surrounding the cantilevers was released in MF319 developer after the UV exposure ~70-75% faster compared with wet release without exposure. With most of the surrounding ProLift gone, the potential for large slabs to break free and bulldoze the cantilevers was essentially eliminated. Still, to protect the delicate arms and anchors, these were covered by a photoresist mask, while the sample was soaked in MF319 developer for a time sufficient to remove the ProLift from under the paddles. Then we stripped the PR and placed our sample into a dish of fresh solvent to release the

arms. Optical microscope images of the intermediate steps of releasing the paddle, and finally the arms are presented in figure 5-9.

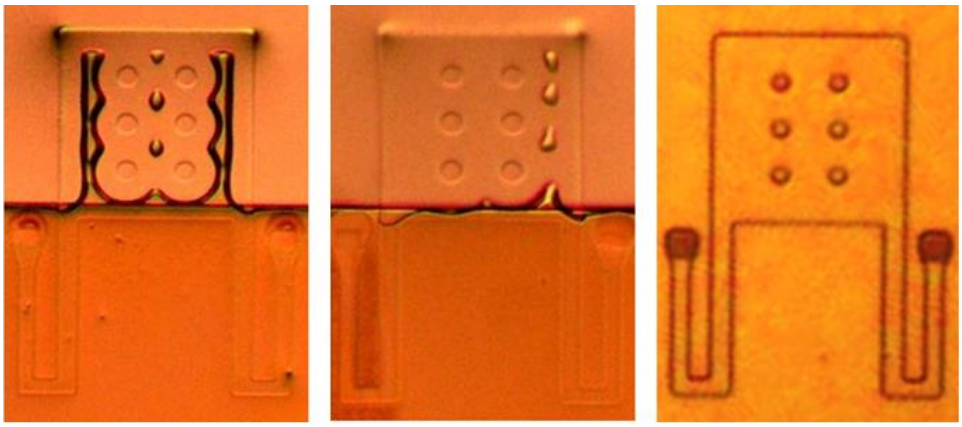

Figure 5-9 (Left) A partially released paddle after 12 minutes in MF319 developer, while arms and anchors are covered by PR. (Middle) Paddle is almost released after 22 minutes in MF319 with PR still present. (Right) PR is striped and the whole cantilever is soaked in fresh MF319 developer, fully releasing the cantilever after 13 minutes.

Instead of using wet developer to remove the ProLift under the paddle, dry oxygen plasma etch could also be used. Prolonged dry etch can cause physical damage to the cantilever (figure 5-7), but the UV exposure sped the process and spared the oxide cantilever from significant damage. Dry etching gave us cantilever yield exceeding 90%, and the surrounding substrate became smoother and cleaner than with wet release. Figure 5-10 presents the intermediate steps in the dry release. Etching was done using Trion RIE with 100 W power, 900 mTorr pressure, 98 sccm O2, and 2 sccm CF_4 flow rate.

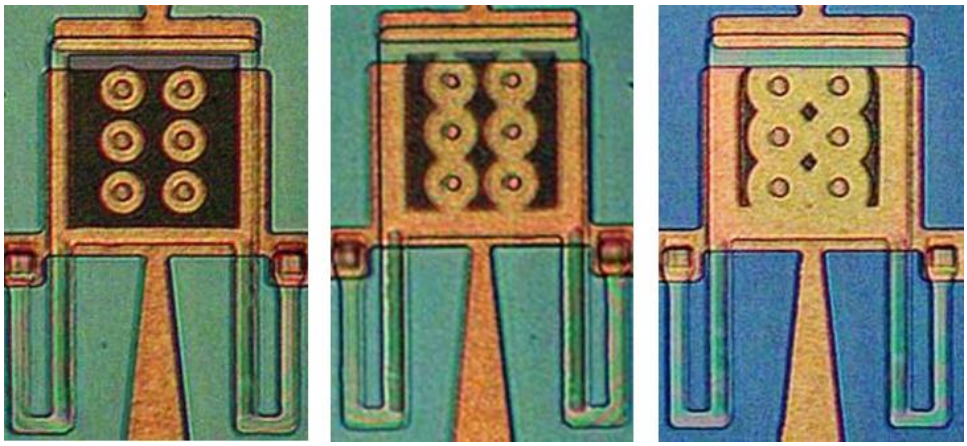

Figure 5-10 (Left to right) Optical microscope images of the stages of cantilever release after 60, 90, and 120 minutes O_2

5.7 Device Dimensions

In previous sections we showed fabrications steps of cantilever and illustrated them by cross section diagrams. In this project different dimensions of this device were fabricated in different phases. We fabricated single pixels of 100 µm x 100 µm plates using photolithography techniques for preliminary researches. Additionally we fabricated 50 µm × 50 µm single pixels and 3x3 arrays of pixels with 20 µm x 20 µm plates. The later was an effort to demonstrate device fabrication in a compact form ready for commercialization in form of array of imagers. Here we summarize these three designs and provide their respective dimension.

Single pixels were fabricated in two dimensions of 100 µm x 100 µm plates and 50 µm x 50 µm plates. However, these pixels have same shape and design and hence we are only presenting smaller pixels design here. Larger pixels are simply twice in all x and y dimensions and same in z dimensions. Figure 5-11 illustrate top view of these pixels.

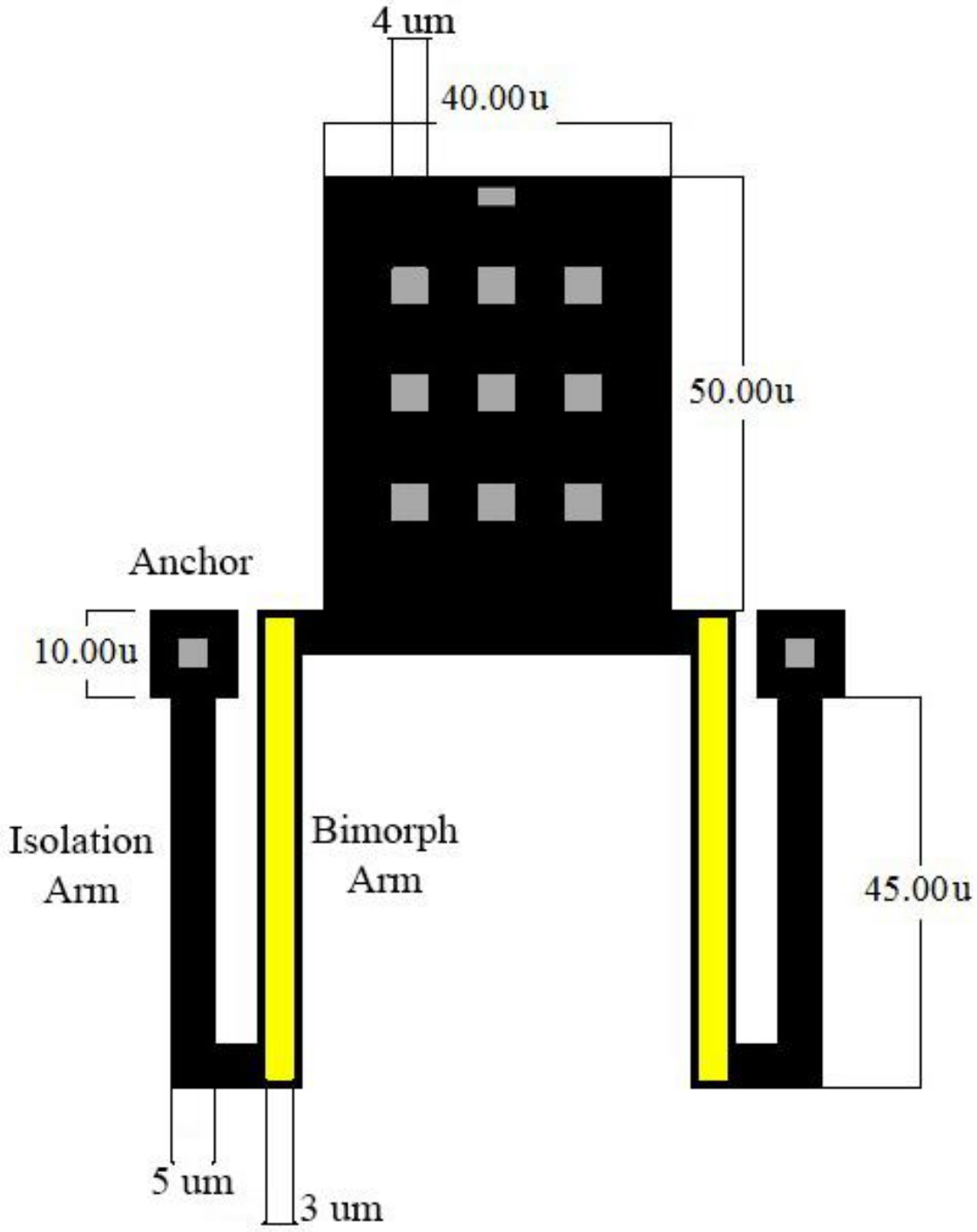

Figure 5-11 Top view design of single pixel in medium size.

Figure 5-12 shows optical microscope image of a single fabricate pixel and figure 5-13 shows SEM image of fabricated pixel.

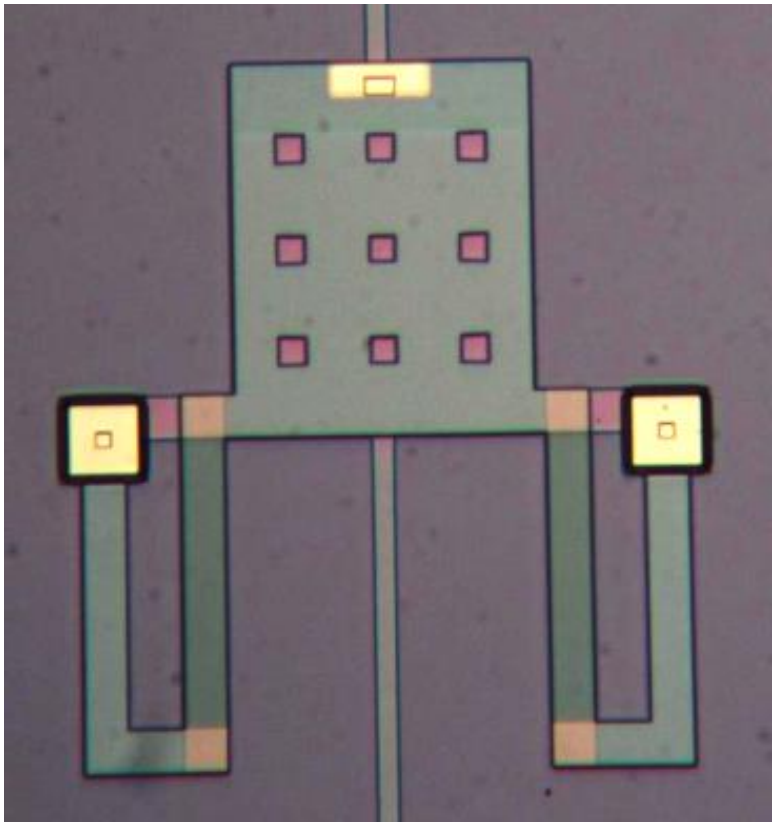

Figure 5-12 Optical microscope image of device after fabrication.

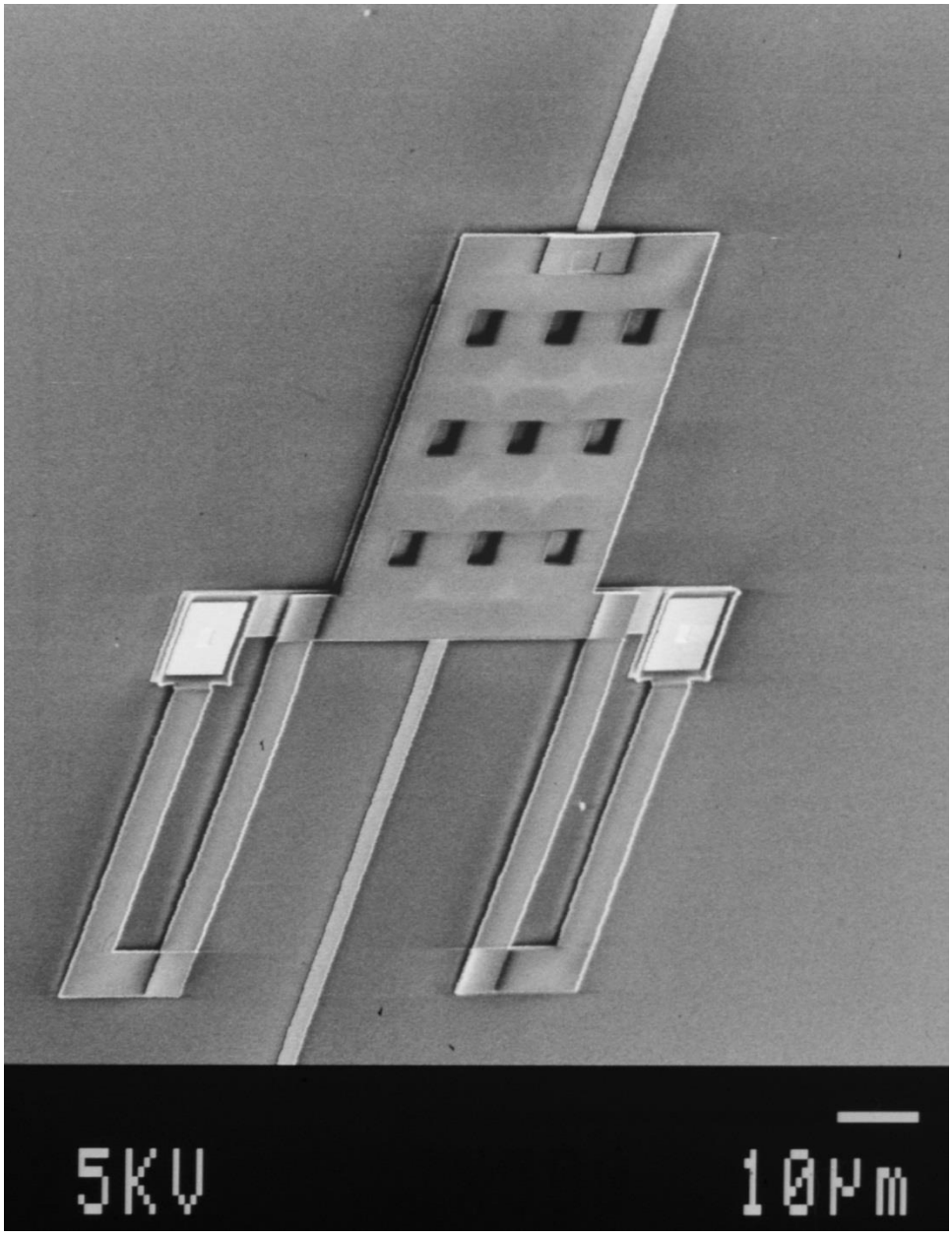

Figure 5-13 SEM image of a fabricated device.

5.8 Contact Pads and Final Device

One of the great advantages of this design is its high fill factor. As last part of fabrication in this project we designed and fabricated a 3×3 array of this device. Any larger array can be designed in a same way with no additional modification.

So far we have not explained connection pads that connect the device to external circuitry. For each pixel 3 signals are required; Input signal for top and bottom plates' biasing and an output signal that comes from tip pad for counting purposes. All devices can have same bias for buried plate. Hence we only need one connection pad for them. However, top plate biasing and sensing is separate. This means total of 2n+1 connection pads for n pixels in the array. Due to lack of resolution in photolithography we fabricated these arrays by e-beam lithography. We used Leica EBPG5000+ Electron Beam Lithography System capable of running at 20, 50 and 100 kV, with a minimum spot size of less than 10nm. However, in industrial fabrication these will be done by deep UV photolithography or other techniques which have better resolution than conventional photolithography and are much faster than e-beam writers. These systems are too costly for research studies and we did not have access to them. Figures 5-14 shows two levels of bond pads. Since contact pads are many orders of magnitude larger than pixels, these figures include two views, one dedicated to close up of center region were pixels are sitting and one showing overall view including all pads.

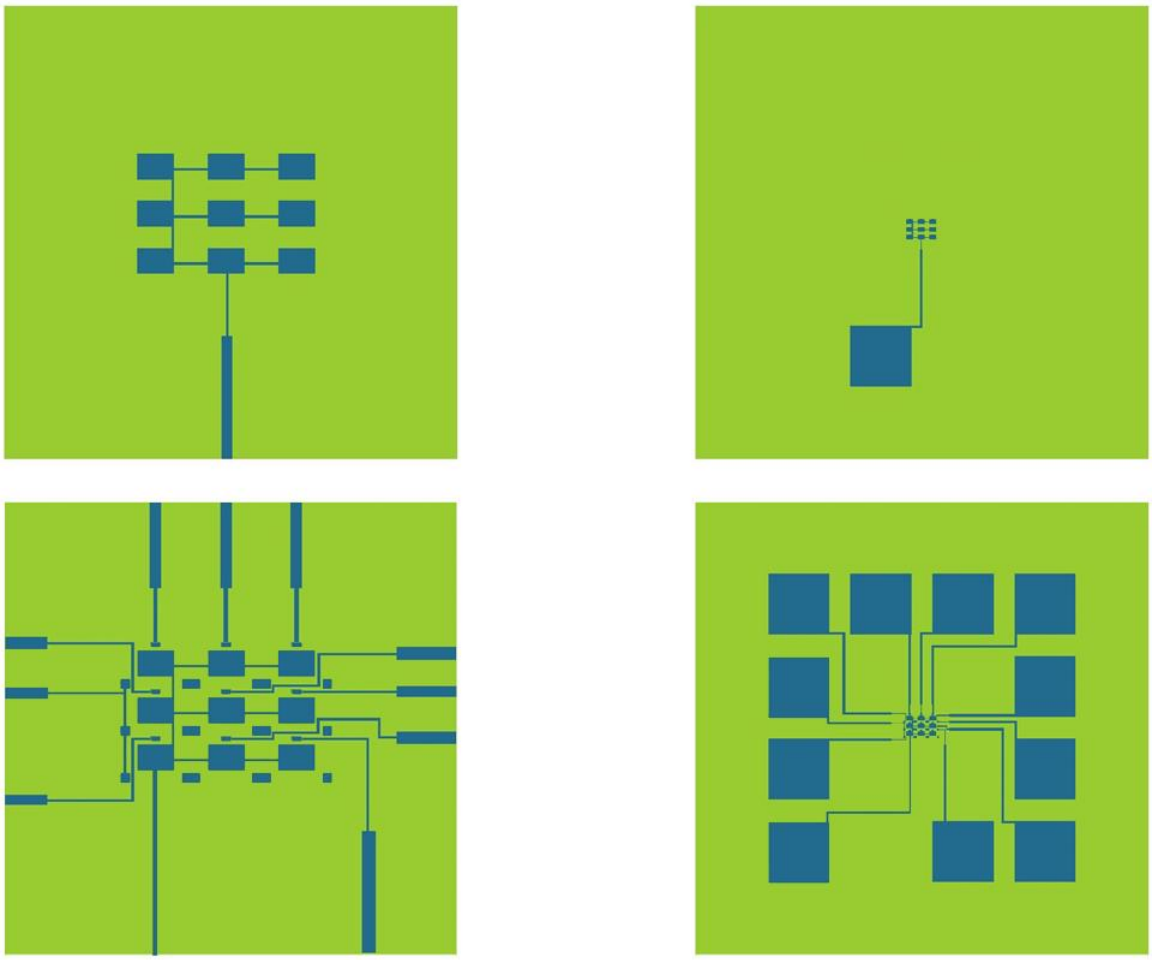

Figure 5-14 Close up and overall view buried plates and it's corresponding bond pad (top figures) and surface plates, tip contact pads, anchor pads and their corresponding electrods. (bottom figures) these two patterns are made at two different lavels and are seperated by a dielectric layer. and RIE etching creates access to buried plate bond pad the the end.

Figure 5-15 shows a light optical microscope image of fabricated surface plates and tip pads for 3 × 3 array.

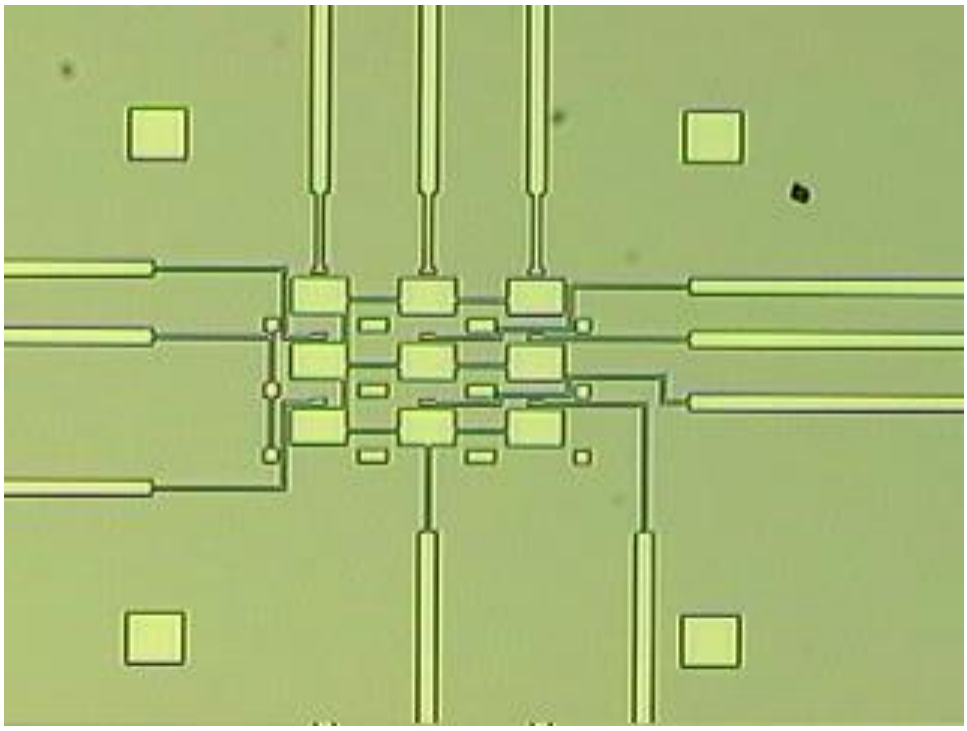

Figure 5-15 Optical microscope close up of 3 × 3 array pad and biasing line regions.

Figure 5-16 shows SEM image of final fabricated 3 × 3 array in full view and figure 5-17 shows close up of pixel region.

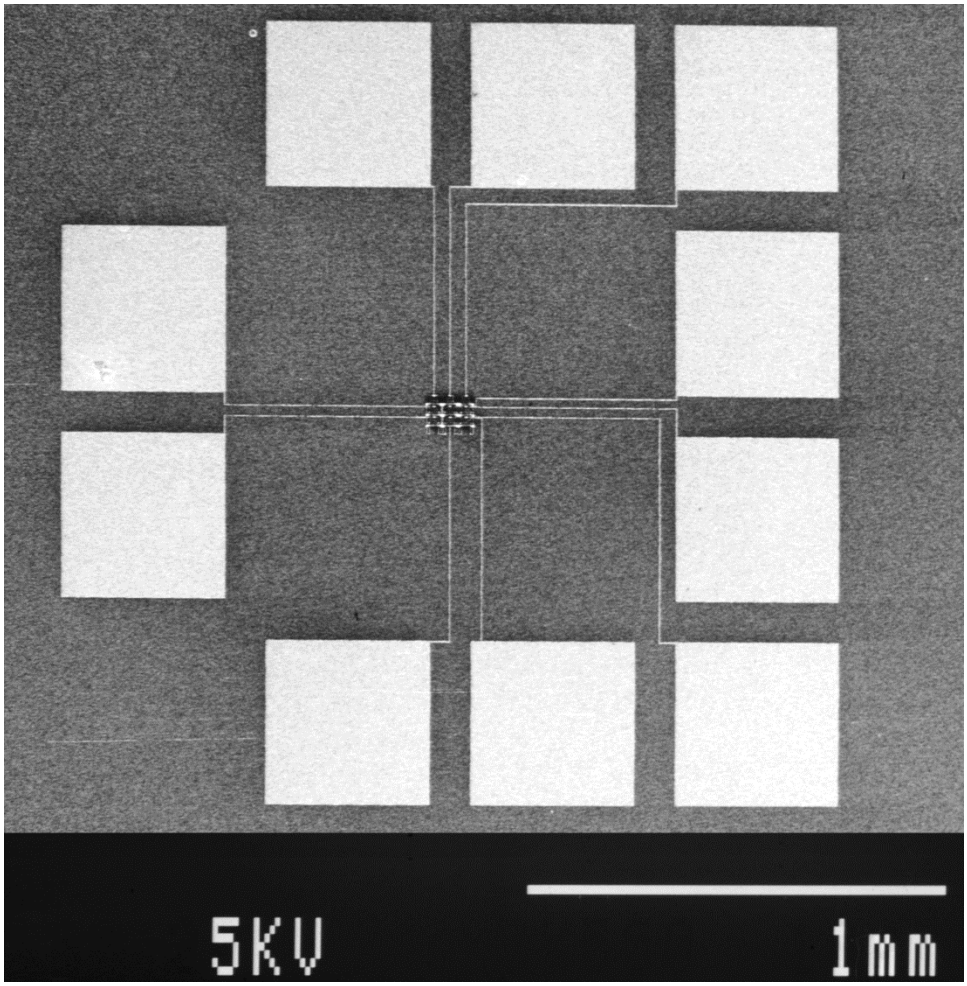

Figure 5-16 Low magnification SEM image of 3 × 3 fabricated array. Optional separate biasing of anchors (and concesuently top plate) and surface plates are removed in the final fabricated device without and change to its function.

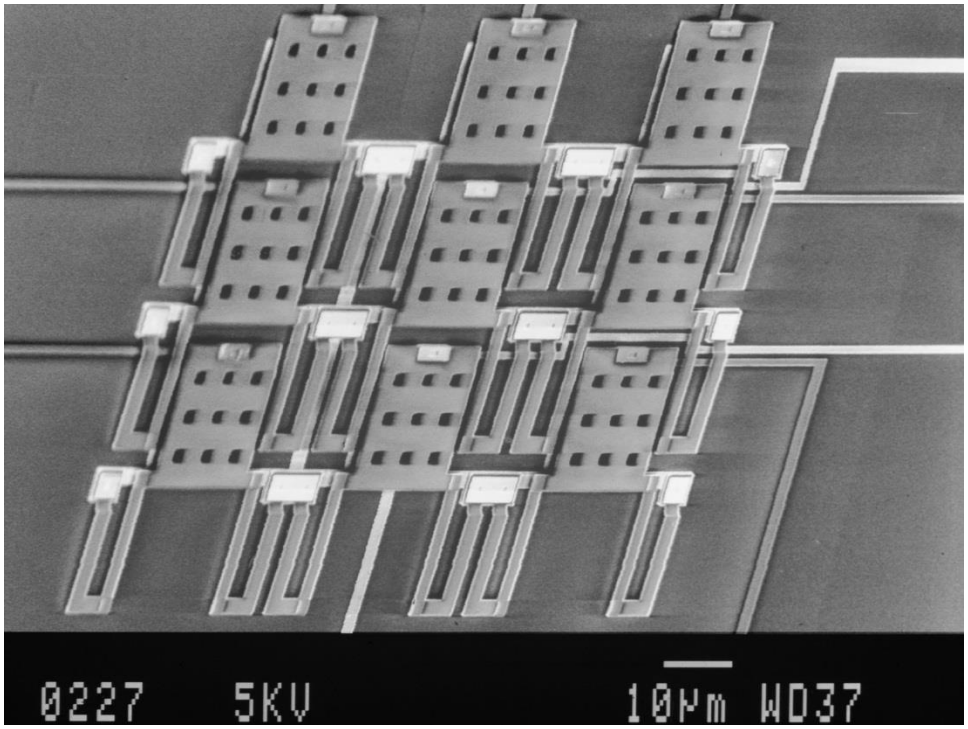

Figure 5-17 High magnification SEM image of 3 × 3 array of final pixels.

5.9 Conclusion

In this chapter we explained all fabrication steps of designed MEMS device in details. Other than various fabrication steps, hard baking of polyimide sacrificial layer is studied. A method for accelerating release process is developed by UV exposure of sacrificial layer and etch rates of exposed and non-exposed layers are compared. It is shown that in both wet and chemical etching this process significantly reduce etch time and increase fabrication yield by lowering mechanical and plasma damage to the device. At the end, light optical and SEM images of final fabricated devices are presented.

CHAPTER 6 DEVICE CHARACTERIZATION

6.1 Introduction

So far we have explained design and fabrication of a MEMS IR detector that works based on electrostatic repulsive force applied on a cantilever structure and heat absorption. In this chapter we present characterization methods and experimental results that proves presence and effectiveness of this electrostatic repulsive force in this design. First we will present our methods of characterization and experimental setups and then results will be presented.

6.2 Curvature and Stress Measurement

We report an optical interference method to measure stress in a silicon dioxide thin film. This method is based on observation of Fizeau fringes [44] that are caused by interference of reflected light between a curved semi-reflective silicon dioxide thin film and a flat reflective surface beneath it. Fizeau interferometry is widely used to compare the shape of an optical surface on a mirror or lens to a reference surface of known shape [45]. The two surfaces are separated by a narrow gap, and interference fringes in reflected monochromatic light indicate spatial variations of the gap. Among other applications are thickness measurement of thin films, strain measurement of fiber optics, residual wedge measurement for optical flats and characterization of organic light emitting devices [46-49].

Stress is important to free-standing thin films in MEMS due to the deformations it induces, intended or otherwise. Intrinsic stresses, which depend on deposition conditions,

are difficult to predict. Usual methods to measure stress in a thin film require measurement of the radius of curvature of a large substrate (e.g. a wafer) on which the film has been deposited and to which it is firmly attached [50]. This can be either done by a contact profiler, which can damage soft and suspended features, or by noncontact profilers, which can be expensive and slow.

We are interested in controlling the stress and deformation in free standing MEMS cantilevers, which consist of a 500 nm thick oxide topped with 30 nm of Cr/Au above a gold surface plate. Observed Fizeau fringes allow observation of height and curvature, as shown in figure 6-1. Cantilever motion and curling lead to a change in the fringe pattern. These cantilevers tend to curl upward after the metal deposition and release due to the different thermal expansion coefficients of metal and oxide. The curvature depends on the oxide deposition recipe, where different methods give different intrinsic stress, and on the temperature of the sample during deposition.

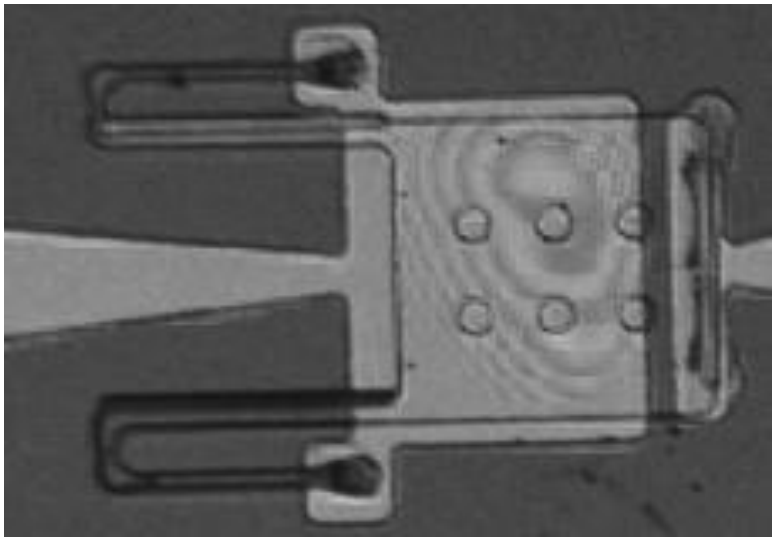

Figure 6-1 Optical microscope image in monochromatic light, showing Fizeau fringes.

Simplified cantilevers with a range of widths and lengths were fabricated. Figure 6-2 presents a schematic of the processing steps. We spin-coated a Si wafer with 1.2 um ProLift-100 as polyimide sacrificial layer, and then 600 nm PMMA (495 A) was spin-coated on top. The desired pattern was exposed by electron-beam to define 10 micron square anchors. The PMMA was developed by MIBK:IPA 1:3 solution and ProLift was etched 15 s with TMAH based developer MF319 following by 75 sec dry etch in plasma enhanced etcher with O_2 gas. Longer wet etch undercuts the ProLift. PMMA was stripped in acetone, and 500 nm TEOS-based silicon oxide was deposited on the ProLift using the Trion PECVD system. The recipe was optimized to achieve high step coverage to strengthen the anchor neck points. The cantilever etch mask was produced by another PMMA spin, e-beam exposure, and MIBK:IPA development, followed by 42 nm sputtered Au and lift off. The Au serves as the reactive ion etch (RIE) mask for etching the oxide in CF_4 gas. The last steps to release the cantilevers are 2 min anisotropic etch of ProLift in RIE system using O_2 gas mixed with 6% CF_4 (300 W, 100 mTorr) and 10 min isotropic etch (300 W, 300 mTorr) while the sample is tilted 45 deg [41]. Figure 6-3 presents an optical microscope image of the resulting cantilever array.

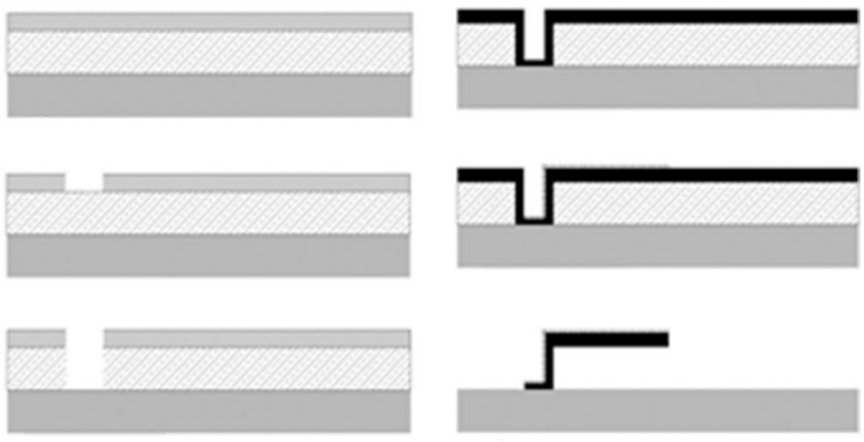

Figure 6-2 Fabrication steps of cantilevers: a. Spin ProLift 100-2 as sacrificial layer, then PMMA; b. Pattern PMMA using e-beam writer and development in MIBK:IPA solution; c. Transfer pattern to sacrificial layer using combination of wet and dry etch; d. PECVD SiO_2; e. Patterned Au lift-off to achieve oxide etch mask; f. Etch oxide in RIE, then release in O_2 plasma RIE.

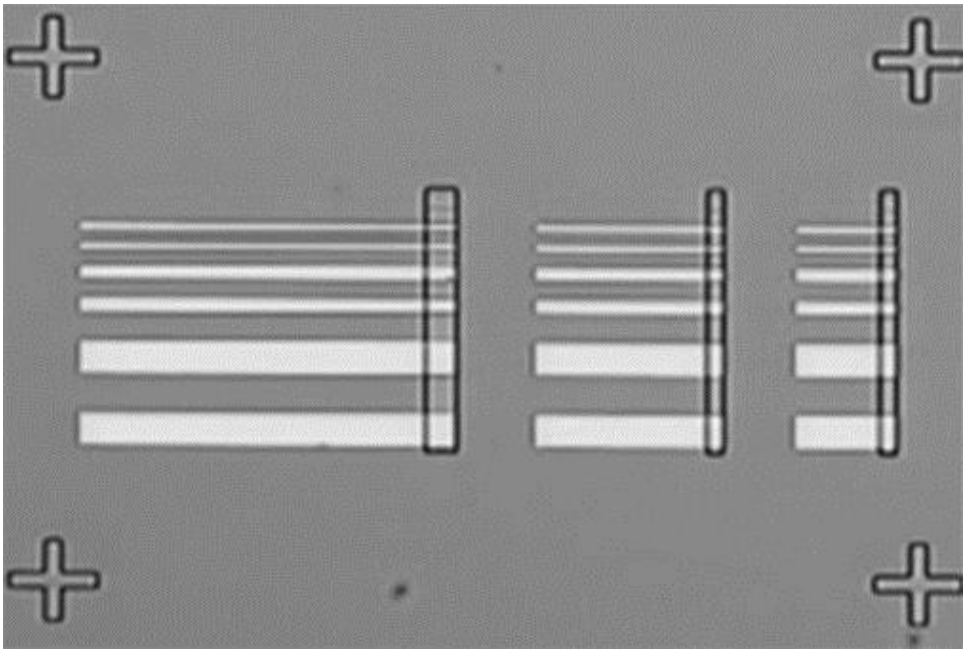

Figure 6-3 Optical microscope image of cantilever arms with length 55, 120, and 250 micron and with width 1, 5, 10, and 25 micron. The narrowest arms are invisible in this image. All arms are anchored at one end. The image was collected before etching the oxide and release from the sacrificial layer.

Fizeau fringes were recorded with a microscope equipped with a digital CCD camera. Images were analyzed in LabVIEW to obtain line intensity profiles. To enhance fringe visibility and allow quantitative analysis, either a monochromatic laser or narrow band-pass filtered white light were used for illumination. Figure 6-4 shows schematic of used setup and figure 6-5 has an example of final result in both graphical image and plotted intensity along specific line.

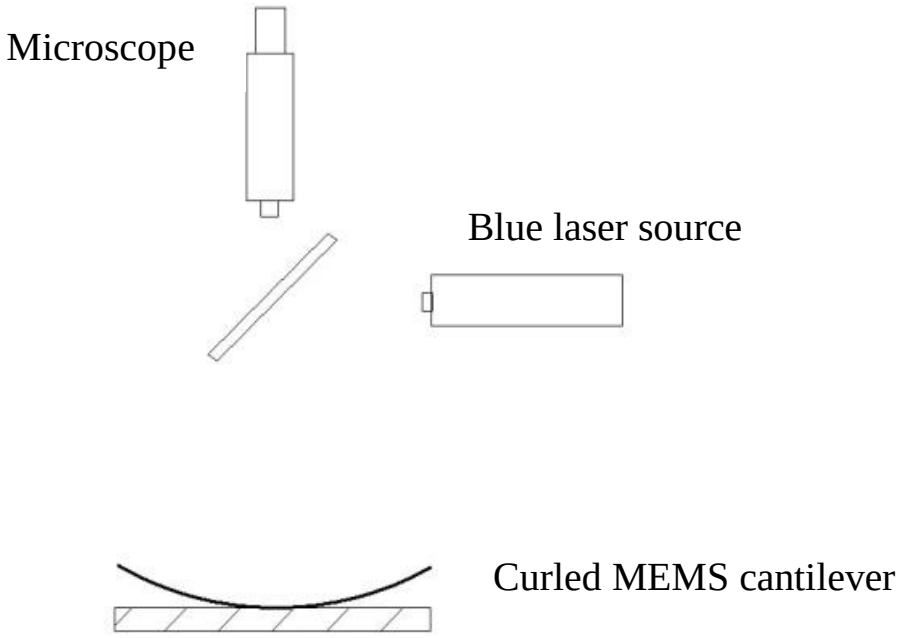

Figure 6-4 Schematic of set-up for observing Fizeau fringes.

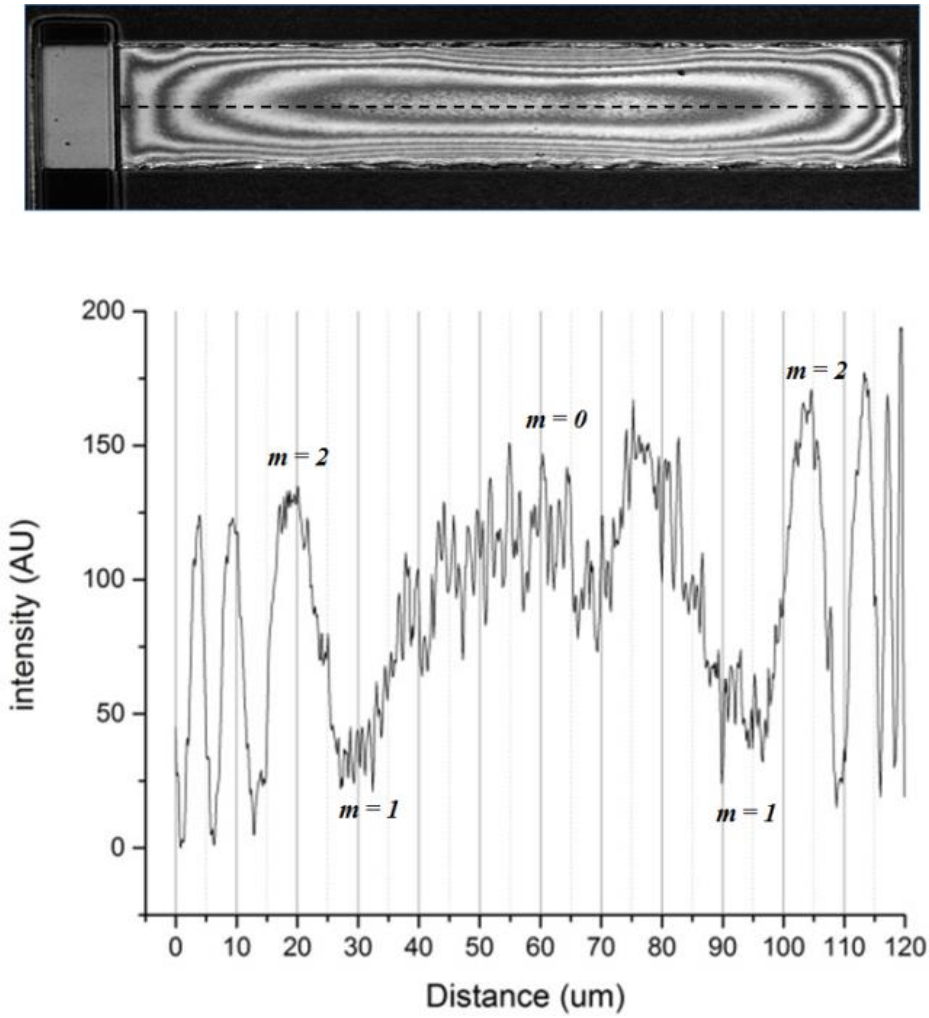

Figure 6-5 Microscope image of cantilever with results of indicated intensity line-scan.

6.2.1 Theoretical Considerations

The optical boundaries that reflect light in the figure 6-2 structures are the top Au surface, the Au/SiO_2 boundary, the SiO_2-air boundary underneath the cantilever, and the Si substrate surface. Interference between reflections from the top three parallel surfaces gives no fringes. Fringes due to interference come only between reflected light from Si substrate surface and light reflected from the cantilever as a whole. The latter reflection has some amplitude and phase whose exact values are unimportant. Amplitude affects

fringe visibility while a shift in phase is equivalent to a uniform height offset between cantilever and substrate. We are only interested in height differences from different parts of the structure, which for adjacent light and dark fringes is just half a wavelength λ/2.

The profile of small deformations may be considered as the arc of a circle of radius *R*, as shown in the figure 6-6 schematic. Stoney's formula [22] relates radius of curvature in a double layer structure to the stress in the film as

$$\sigma^{(f)} = \frac{E_{SiO2}}{6(1-\nu_{SiO2})} \times \frac{h_{SiO2}^2}{R h_{Au}} \qquad (35)$$

where *E* and ν are Young's modulus and Poisson's ratio respectively and *h* is the layer thickness. This formula is valid when $h_{Au} \ll h_{SiO2} \ll R$. The height differences d_m above the minimum at the position of the m^{th} ring is $m\lambda/2$, where *m* is an integer that is incremented with each new light or dark ring counting from the central spot (m = 0). See figure 6-5 for an example of how the rings are numbered. Across a cantilever d_m generally amounts to only several half wavelengths, i.e. no more than a few microns, while ring radii r_m are on the scale of 10s of microns, according to figure 6-5. In this limit of $d_m \ll r_m$, $R \approx \frac{r^2}{2d}$ according to figure 6-6 so that equation 1 becomes

$$\sigma^{(f)}(r) = \frac{E_{SiO2}}{6(1-\nu_{SiO2})} \times \frac{h_{SiO2}^2}{h_{Au}} \times \frac{m\lambda}{r_m{}^2} \qquad (36)$$

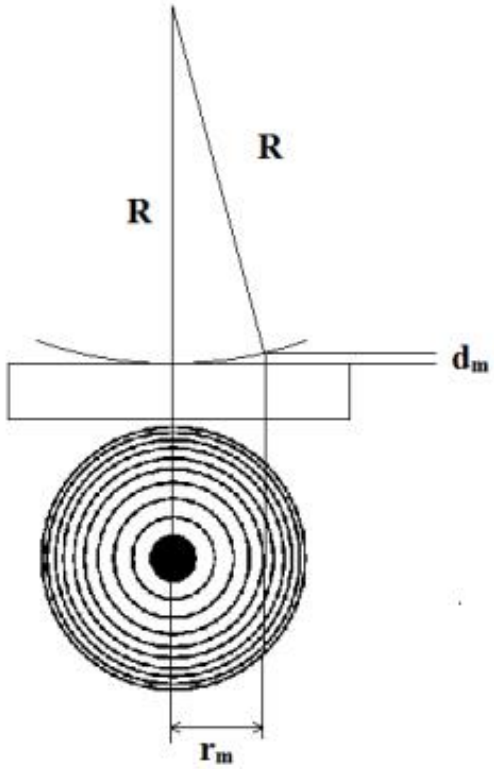

Figure 6-6 Schematic with air gap d_m, ring radius r_m, and radius of curvature R.

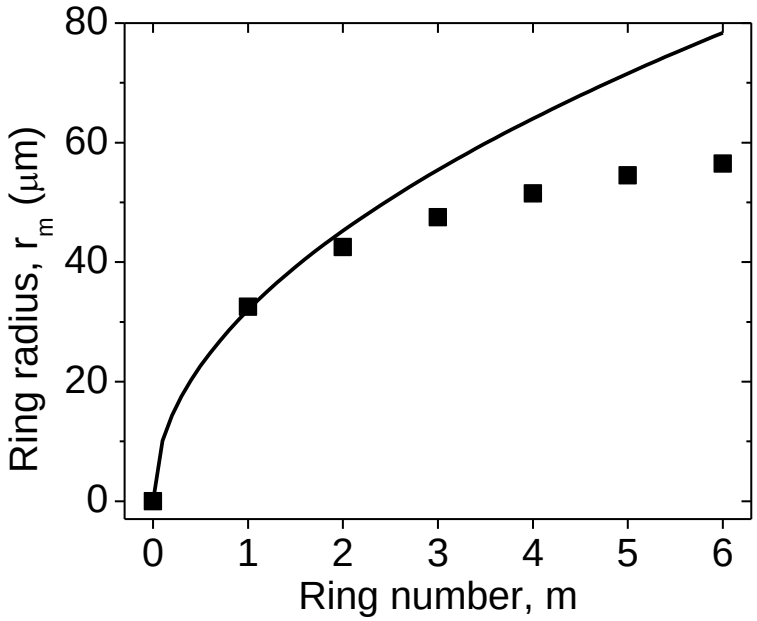

Figure 6-7 ring radius rm vs. ring number m for figure 66-5 profile (symbols) and function 32√m (line).

6.2.2 Results and Discussion

The assumption that the deformation along a particular direction is the arc of a circle means the stress has the same value at every point along that direction. In other words, uniform σ has no *m* dependence, which requires r_m to increase as the square root of *m* according to Eq. 2. For the example of figure 6-7, the experimental r_m values rise more slowly than $\sqrt{m}$, which implies that stress is higher near the edges. In other words, closer ring spacing means more curling and higher stress. For other directions the stress might be lower at the edges. That stress is not uniform is supported by figure 6-8, where the Fizeau rings even lack the same symmetry as the cantilever, one corner being strongly curled.

Figure 6-8a presents an SEM image of one of the fabricated arms. Curling of the lower right corner is obvious, but it is clearly impossible from this image to quantify the deformation. Figure 6-8b presents the Fizeau fringes for the same arm at 408 nm wavelength. To obtain a map of stress over the surface, a radial mesh was drawn from the center dark fringe to the boundaries and the position of each dark and bright fringe was determined along each line. Figure 6-8c is the resulting contour plot of the d_m in units of μm. Figure 6-8d gives the stress distribution over the surface calculated according to Eq. 2, where the darkest shade indicates 111 MPa and the lightest 753 MPa The stress is highest along the short direction and at the curled corner and lowest in the long direction. During release a tilted sample helps RIE removal of hard baked ProLift. This may explain the asymmetry of the deformation [51].

In summary, we have presented a method of measuring topography, stress (and motion) of free standing transparent films with high spatial resolution and without special instrumentation.

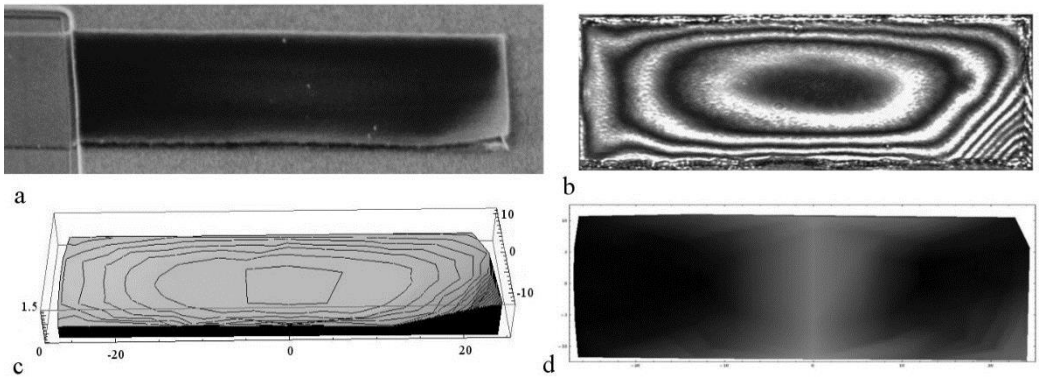

Figure 6-8 a. SEM image of an arm after release b. Image taken with 408 nm wavelength source revealing fringe pattern. c. Contour plot. d. Calculated stress map on the surface of cantilever, bright areas shows higher stress values.

6.3 Device Experimental Test Setup

Design and fabrication of this MEMS device had to be modified over the course of this project to meet all requirements and demonstrate most efficient functionality. For this purpose a testing setup was necessary. Full testing of this device requires a multifunction setup that can perform all following tasks:

- Sourcing electrical bias to pixels.
- Measuring tip pad current for sensing tip touching the surface.
- Live view of the device through fringe recording setups for curvature measurement.

To control all mentioned functions and record all measurements from a single interface we have used LabVIEW to create and application that send and receive all required signals to our setup instruments from one interface. Figure 6-9 shows Front view of this program with its various sections.

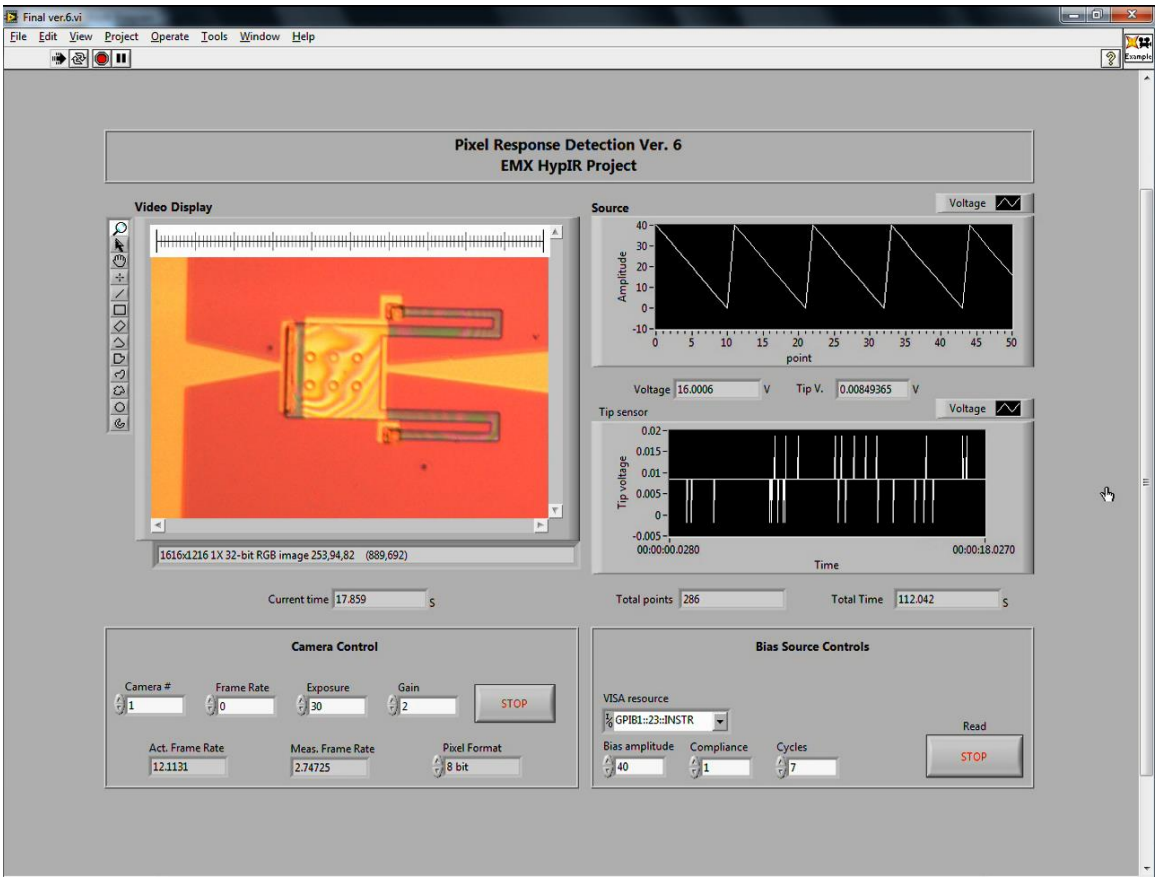

Figure 6-9 Front view of created LabVIEW interface used for testing devices.

For our setup we used two Keithley 4200 source/meter. One was used for sourcing our saw-tooth bias which was programed by our LabVIEW interface while measuring the current between surface plate and buried plates. According to our design this current has to be zero (or very small) due to presence of 500 nm oxide layer which will form a capacitor in between these two plates. However, this capacitor have a breakdown voltage. To keep our device functional we had to keep bias between plates lower than this voltage. Hence it was necessary to measure the current through this capacitor and make sure it doesn't break by another Keithley source/meter.

6.4 Device Characterization Results

Video microscopy dramatically reveals the upward displacement due to the electrostatic force. Figure 6-10 (upper) presents video frames before and after reaching 40 V applied bias, where the electrostatic force has ripped the cantilever from its anchors, displacing it. Some videos show the cantilever flying away when the anchors give way.

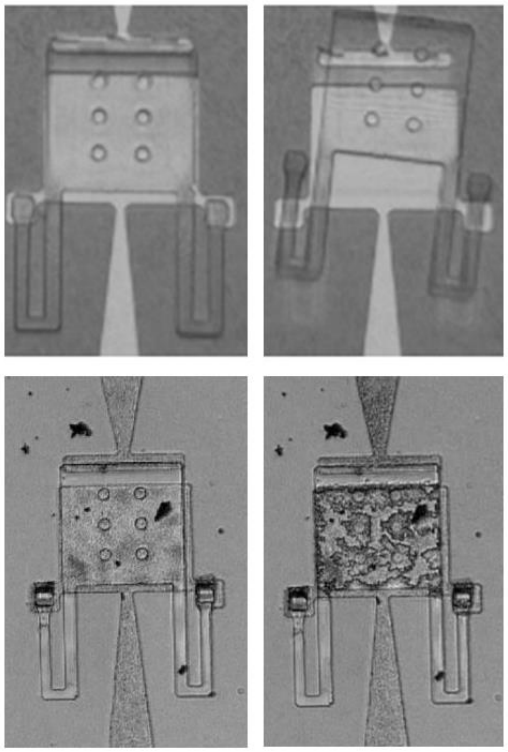

Figure 6-10 Video microscopy frames of well-released cantilever before (upper left) and after (upper right) reaching 40 V applied bias, where upward electrostatic force has ripped the cantilever off its anchors. Video frames for incompletely released cantilever before (lower left) and after (lower right) applying bias. Electrostatic force lifts the cantilever from polyimide residue, causing air bubbles to intrude under the semi-transparent cantilever from the edges and release holes.

Figure 6-10 (lower) presents images of incompletely released cantilevers stuck in polyimide residue. When biased, the cantilever slowly peeled up from the surface. Loss of contact between cantilever and residue is revealed by intrusion of air under the cantilever from the edges and release holes. When the bias is removed, the cantilevers sink back into the sticky film, and the air is squeezed back out.

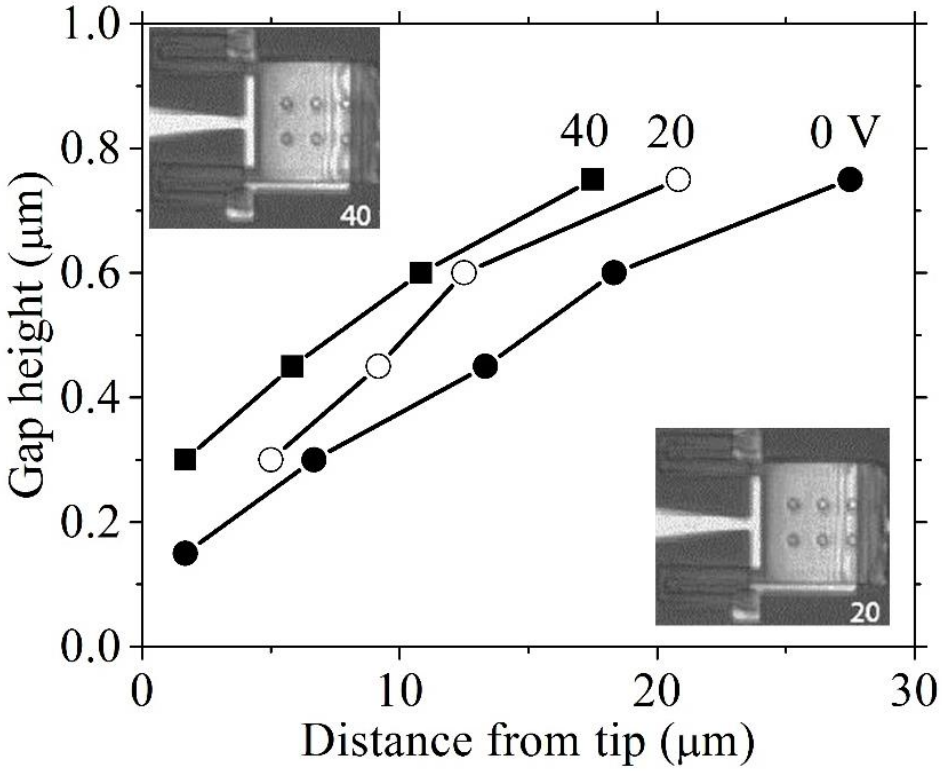

Figure 6-11 Height of gap between surface plate and cantilever as function of distance from tip for three values of applied bias. Insets show images with different interference patterns in red light at 20 V and 40 V.

Vertical displacement of the semitransparent cantilever was quantified by an optical interferometry method described before and in [52] on a large cantilever with 100 μm x 100 μm paddle using a 600-nm-wavelength long-pass filter to improve contrast. At zero bias, the highest density of fringes occurs near the middle of the paddle, where the curvature of the paddle is evidently maximum. An SEM image of one of these large cantilevers confirms this interpretation of the initial paddle deformation in null position [24]. When bias is applied, the fringes from the middle of the paddle are observed to shift toward the tip, increasing their spacing, while no change in the interference pattern is

observed near the base of the paddle or arms. This indicates a lifting of the tip and flattening of the paddle with bias. Figure 6-11 plots the height of the gap between cantilever and surface determined from the first several dark fringes nearest the tip where their visibility is highest. We assume that the dark fringe nearest the tip at 0 V has a quarter-wave gap of 150 nm. Insets are microscope images at 20 and 40 V, where the difference in interference pattern is most obvious over the rightmost release holes which change from bright to dark. The observed average change in height with bias is roughly 5 nm/V. An estimate of the spring constant for bending of the paddle due to a concentrated force near the tip [19] is 0.22 N/m. Thus, to obtain 100 nm of tip lift for 20 V bias requires a force of ~22 nN. We note that the portion of the large curved cantilever feeling most of the lifting and paddle-flattening force is evidently near the tip, a strip of say ~5 μm x 100 μm, which is five-fold larger than the 10 μm x 10 μm area of the model cantilever in figure 3-2. We also note that the structural oxide tends to increase the electrostatic force [24]. Hence, the observed displacement agrees with expectations in order of magnitude.

Setting the electrostatic force, which for the simple model goes as $\sim \frac{V^2}{\sqrt{z}}$ according to equation 34 and figure 3-2, equal to the elastic force, which goes as *z*, we expect the displacement to increase as $V^{4/3}$. In fact, figure 6-11 suggests that displacement depends sub-linearly on *V*. We also noted that some cantilevers are destroyed at 40 V bias by excessive leakage current between surface and buried plates. Any leakage reduces the expected electrostatic force on the plates. Leakage can be reduced by using materials with higher dielectric constants.

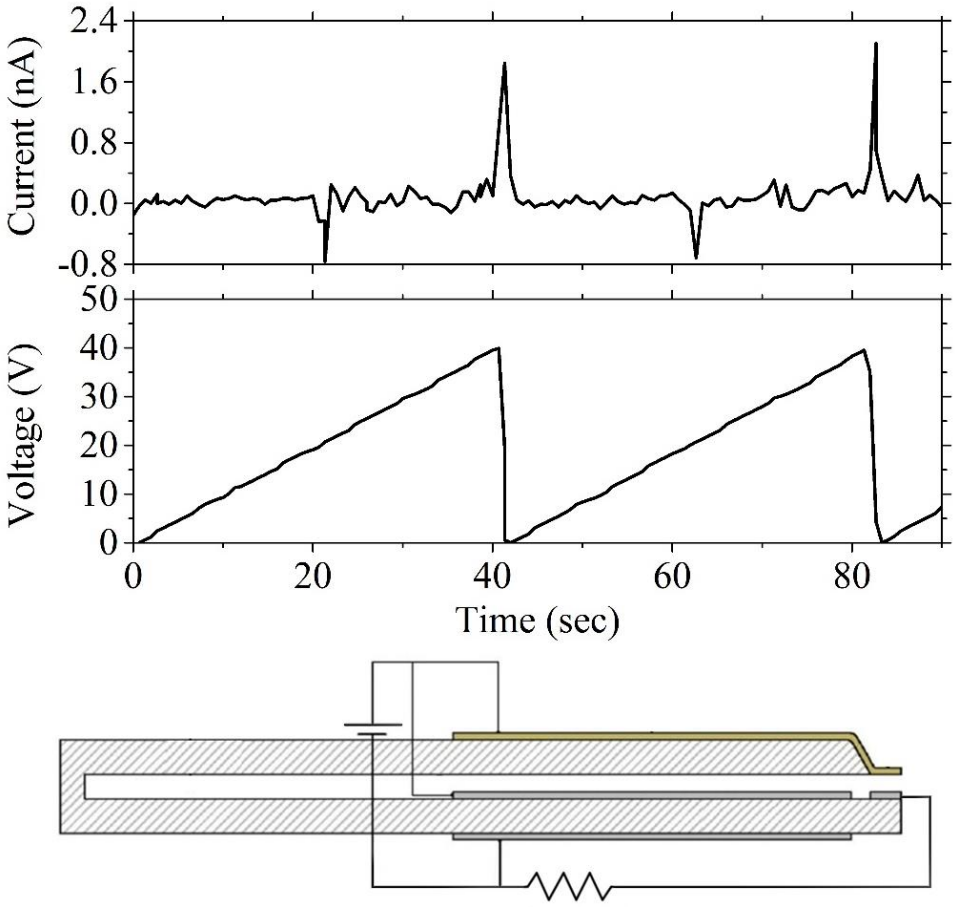

Figure 6-12 (top) Applied sawtooth ramp bias applied between cantilever and buried plate and measured current through load resistor. (bottom) Schematic of device with external circuitry.

The vertical displacement caused by the electrostatic force was also observed electrically. In null position, a bias applied to the cantilever should appear across the load resistor shown schematically in figure 6-12. When contact with the tip breaks due to the lifting of the cantilever, the voltage across the load returns to 0 V. A saw tooth ramp bias was applied as shown in figure 6-12. The actual tip contact resistance was very high (due to residue or curling), so that no direct current was observed in null position. Instead, as bias increased, breaking of physical contact at the tip caused a sudden redistribution of

charge, which was sensed as a small current in the load resistor. When the bias was switched off, there appeared an induced current in the load of the opposite sign, which we interpret as being due to the sudden return of the cantilever to null position. This effect is repeatable.

The sign and relative size of the current spikes in figure 6-12 are easily explained. When the positively-biased tip is in physical (but not electrical) contact with the tip pad, the latter is negatively charged by induction. When the cantilever pops up, some of this negative charge flows away through the load resistor, causing negative current. The cantilever continues to rise slowly during the ramp, allowing more negative charge to bleed off, but the rate of this charge flow is below the noise. When the bias is shut off, the cantilever returns suddenly to null position from its maximum height, inducing a large positive current as all of the original negative charge rushes back up through the load resistor to inductively recharge the tip pad.

The tip may be designed so that the electrostatic force overcomes the Casimir sticking force even for very close electrical contact between tip and tip pad [24]. Noise equivalent power and noise equivalent temperature difference for IR sensing mechanism are discussed in [19].

6.5 Conclusion

In summary, an electrostatic force that lifts a MEMS cantilever from the surface, for a design comprised of three parallel conducting plates, has been demonstrated experimentally. A method was developed to observe and measure cantilever curvature

using light interference pattern between reflected light from semi-transparent cantilever and substrate surface. Presented video microscopy results indicated upward motion of cantilever by application of bias between plates. This motion was quantitatively studied as function of applied bias. Device claimed repetitive touching once bias is dropped to zero is proven by measurements of current passing though tip pad.

CHAPTER 7 TRANSISTORS AND THEIR CHARACTERIZATION

7.1 Introduction

Previous chapters demonstrated characterization techniques that measure device functionality. Electrical probing and curvature study using interferometry techniques were used to understand a fabricated MEMS cantilever. As discussed earlier there are numerous other characterization techniques that provide in depth information about device composition, structure and even fabrication techniques. Many of these techniques require destructive specimen preparation steps to access specific regions of interest resulting in the loss of device functionality. In this chapter some of these techniques are reviewed to explain their requirements, limits, how they work and what kind of information can be obtained using them.

In later chapters we will explore advanced nanoscale materials characterization using a beam of energetic electrons. The capabilities and limitations of transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM) and analytical electron microscopy (AEM) using energy dispersive x-ray spectroscopy (EDS) will be discussed. Research results will be presented where TEM and STEM EDS are evaluated as tools to investigate multi-layered ultrathin high-k dielectric film stacks in the transistor structures of two advanced generation semiconductor devices. However, it is helpful if we review transistor structure briefly first to have better understanding of our research goals.

7.2 Field Effect Transistors

Transistors are electronic devices that are made of three or four terminals. These devices can be used as amplifiers or switches in electronic circuits. Transistors can be divided in two categories of bipolar junction transistors (BJT) and unipolar field effect transistors (FET). BJT are made of two PN junctions and hence can be in PNP or NPN form. One diode is biased forward and the other is biased in reverse. These transistors are current operated devices. FET on the other hand are voltage operated devices. The FET uses an electric field created by an applied bias to the gate terminal to control the flow of electrons from the source to the drain. BJTs were widely used in older technologies and remained popular in analog circuits like amplifiers. However, field effect transistors now own most of digital circuit markets. Our study was done on field effect transistors and hence we will describe them further in the following sections. [53, 54]

7.2.1 Structure and Function of FET

The first practical field effect transistors were invented in 1947 through the efforts of William Shockley [2]. The type of field effect transistor that is widely used in industry is metal–oxide–semiconductor field-effect transistor (MOSFET) which was first reported by Kahng [55]. The constant pressure for faster processing has driven the development of smaller and faster transistors and thus many aspects of the MOSFET have changed from the original form.

The basic structure of a MOSFET device is shown in figure 7.1. It includes two doped regions as a source and a drain within an oppositely doped substrate. There is a bias

between these two terminals (V_{DS}). There is another bias between the gate and the source (V_{GS}). The operational characteristics of the FET are dictated by the dopant types and the relative biasing conditions. Depending on type of dopants in the source and drain, the device can be NMOS or PMOS, where NMOS has n^+ doped source and drain and PMOS has p^+ doped source and drain.

In a simple MOSFET device, the source and drain are interchangeable and can only be differentiated by applying a bias to them. [56] However in current day applications and designs it is common to find physical distinctions between the two transistor types, for example dimensions, morphology, or materials.

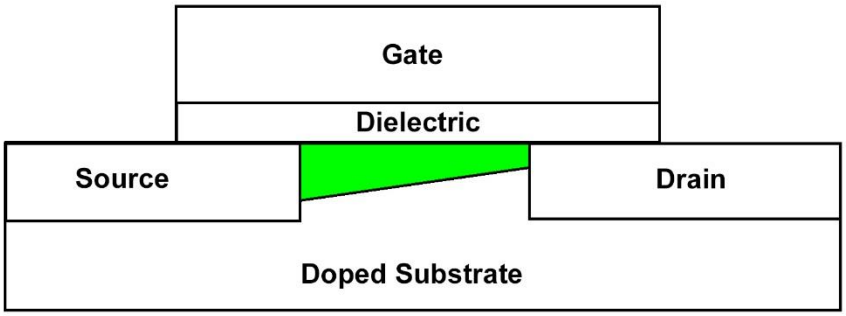

Figure 7-1 Simple MOSFET Structure, highlighted region is the current channel.

The gate electrode is usually composed of metal or heavily doped poly silicon. When a voltage is applied to the gate electrode, an electric field forms through dielectric layer in the underlying silicon region which is called the channel. The channel is located between the source and drain directly under the gate electrode. The gate voltage changes the conductivity of the channel and hence controls the current that flows between the source

and drain. For further explanation let's consider an NMOS device. Similar statements can be made about PMOS by considering its opposite type of dopant.

MOSFET behavior in three different regions [56]:

- Accumulation: In case of NMOS, when a negative voltage is applied to the gate, a vertical field from substrate toward the gate is created and holes in the substrate are attracted toward the gate dielectric/substrate interface region. This condition prevents current flow from source to drain when a bias is applied between them.
- Depletion: the flatband voltage (V_{FB}) is the point when the gate to source voltage is higher than the voltage required to flatten the energy bands of the gate electrode, oxide, and the substrate. At V_{FB} a vertical field directed toward the substrate is created. This depletes holes from dielectric/substrate interface. At threshold voltage (V_{TH}) this surface becomes completely depleted of mobile charge.
- Inversion: when gate voltage is higher than V_{TH} an electron layer will be created called inversion layer which creates a conductive channel between source and drain.

7.2.2 Advancements in MOSFET technology: High-k Dielectrics

PMOS and NMOS transistors were introduced early in the 1970s. Silicon was and still is the most common substrate used for semiconductor devices. The raw materials for

its manufacture are plentiful and the electrical and mechanical properties of silicon make it suitable for large scale fabrication of integrated circuits. By the 1990s, complimentary MOS (CMOS) dominated the microelectronic industry because of their low power consumption and the possibility of scaling them down to very small sizes. [57]

The semiconductor industry has passed from micro to nano scale integrated circuits. However, the miniaturization of transistors to smaller than 100 nm gate lengths has been accompanied by unique challenges. One such consideration arises because reduction of the gate dimension must be accompanied by a concurrent reduction in the gate dielectric thickness. For the traditional gate dielectric material, SiO_2, this equates to layers less than 2 nm in thickness. [56] Thin layers of SiO_2 are increasingly subject to reliability problems due to breakdown as well as being susceptible to current leakage. Leakage or subthreshold current causes increased power consumption of devices while nominally in the off-state and in the upper limit the leakage current can become as high as the on-state current rendering the transistor nonfunctional. To overcome this challenge, significant advances in the IC industry have been ongoing. For example, the introduction of high-k dielectrics to replace SiO_2 in the gate structure and the development of alternative transistor shapes like FinFET. [58]

The replacement of SiO_2 with high-k gate dielectrics has brought much attention to this field. As a result, several alternatives were introduced some of which are used in advanced semiconductor technologies. [59] For years, SiO_2 was a suitable choice as gate dielectric because of following reasons [56]:

- High quality interface between Si (substrate) and SiO_2.

- Chemical and thermal stability at high temperature.
- Good insulating characteristics.
- High breakdown field.

Among all the high-k dielectric candidates, the following materials have shown the highest promise for replacing SiO_2 in gate dielectric:

- HfO_2: It has k value (relative permittivity) of 25, compare to 3.9 for Silicon dioxide. It is thermally stable with Si at high temperatures and exhibits a lower leakage current and higher breakdown voltage than SiO_2. It is one of the commonly used materials in advanced generation CMOS transistors.
- Al_2O_3: It has lower permittivity (10) than HfO_2 but it is still larger than SiO_2. It also shows high mechanical robustness and thermal stability with Si at high temperatures.
- La_2O_3: It is a rare earth oxide but excellent results are reported for it including k value of 27. [60]
- Ta_2O_5: Its relative permittivity is about 26-28 and has a low leakage current. This is another widely used replacement for SiO_2 in current advanced generation devices. [61]
- TiO_2: With dielectric constant as high as 80 it could be considered as a good choice. However, it is reported that the field effective mobility is lower than SiO_2 based MOSFETs. [62]

Although each of these materials show promising results, researchers are still looking for alternative methods to overcome the leakage current challenge as gate dielectric

thicknesses continue to decreases. Some current ICs are using various combinations of these materials to overcome this challenge with better success. Nanoscale materials characterization is essential to the research and development of new engineering materials for many applications including electronic materials. The objective of this research effort is to define the operating parameters that are best suited to the analysis of complex interfaces in the lower limits of lateral spatial resolution. TEM and EDS are used to characterize the high-k gate dielectric layers two of 22 nm technology node IC's. The optimized parameters are ultimately applied to determine if interdiffusion has occurred between the ALD thin film layers that comprise the high-k dielectric stack in the aforementioned production devices.

7.3 Physical and Chemical Characterization of Nano-Transistors

Many techniques have to be used to fully characterize semiconductor devices. Each technique has its own set of strengths and limitations and will provide various pieces of the device characteristics. [63] Here we are interested in physical and chemical characterization techniques. Historically these have been done by microscopy and spectroscopy techniques. However, transistors incorporated in advanced ICs are typically less than 100 nm in size. The latest ICs in market by this day are in size range of 14 nm and 10 nm is right on the horizon. The resolving power of light optical techniques are limited by the wavelength of the light source (λ) and numerical aperture of the objective lens (NA): [63]

$$r = \frac{0.61\,\lambda}{NA} \qquad (37)$$

Using liquid immersion with high numerical aperture limits of 1.3-1.4 for oil-immersion, the resolution limit is about 250 nm for λ≈500 nm (green light). This is much larger than the gate dimensions characteristic of current ICs and hence makes visible light not effective for high-resolution characterization of the transistor or interconnect structures. Using X-ray microscopy the theoretical resolution can be as low as 30 nm. Although great advances have been made in X-ray microscopy and tomography, theoretical resolution limits have not yet been achieved. The technique still needs to overcome some disadvantages like problematic focusing, long acquisition times and X-ray source choice which keeps it from being a routine technique. [64]

Electrons on the other hand have much smaller wavelengths and higher energies:

$$\lambda = \frac{h}{\sqrt{2m_0 eE\left(1+\frac{eE}{2m_0 c^2}\right)}} \qquad (38)$$

Where h is Plank constant, m_0 is mass of electron, e is electron charge and E is electron energy. Hence for techniques like scanning electron microscopy (SEM) with typical electron energies of 10 KeV, the wavelength is about 12.2 pm and for techniques like transmission electron microscopy with electron energies of about 200 KeV, it is about 2.5 pm. [65] This makes electron microscopy and spectroscopy techniques ideal for the physical and chemical characterization of transistors found in advanced ICs.

Before getting into an in depth explanation of some of these techniques it is important to mention the trade-offs inherent to materials characterization at small dimensions: high sensitivity and small volume sampling are competing factors. A smaller beam diameter will provide improved lateral spatial resolution which is required for small volume analysis

but simultaneously equates to a reduced beam current. The reduced electron flux of a smaller beam will generate fewer core shell electron ejections, which will result in the production of fewer X-rays available to be detected by the EDS detector. For EDS this translates to reduced signal to noise complicating the detection of both light elements and those present in low concentrations. The importance of thoroughly understanding the objectives of the analysis and the material systems under analysis cannot be overemphasized. The subject of this investigation shows how such information must be used in order to optimize the operating parameters of the TEM for each specific experiment to produce the highest quality data with the fewest undesired artifacts. [63]

Characterization of a sample using an electron beam can be described based on a simple principle:

When a high-energy incident electron interacts with a sample it can be absorbed, deflected, or transmitted. Additionally the interaction of an electron with a sample can produce secondary electrons and electromagnetic radiation which can in turn excite secondary particles and radiation. The products that are generated as a result of the interaction of an energetic beam of electrons with a sample are summarized in figure 7.2.

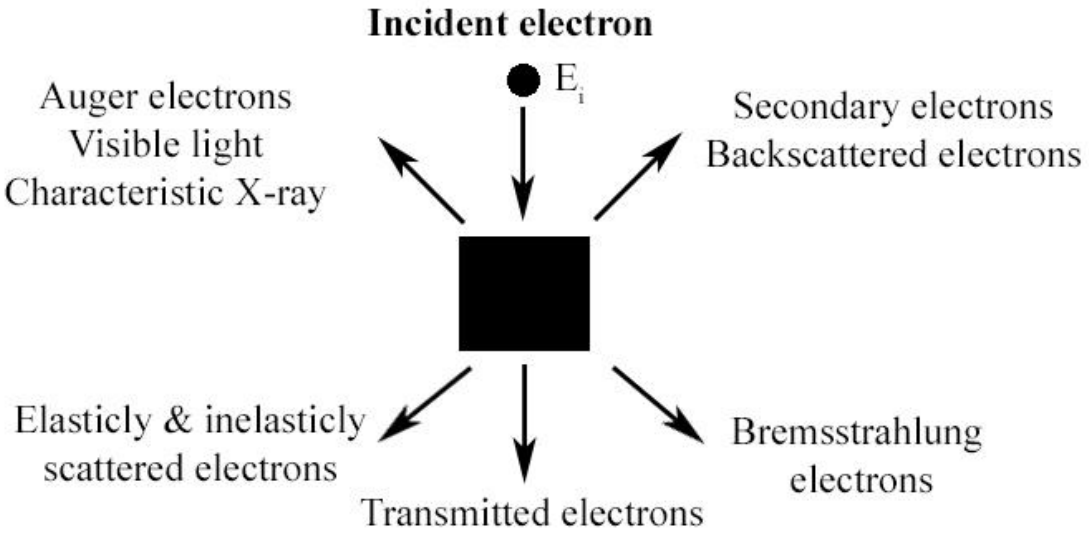

Figure 7-2 Some important signals generated by the interaction of high-energy electrons with a specimen.

The purpose of this investigation is the morphological and elemental analysis of small volumes with high resolution within a time frame acceptable for industrial applications. The technique of choice is analytical electron microscopy (AEM). In this work a transmission electron microscope (TEM) is operated in scanning mode (STEM) where the electron beam is focused to a fine probe and rastered over the specimen in a user defined pattern. Operating the TEM in STEM mode provides a precise registration between the probe coordinates and the signals generated. The signals of interest for this work are the image, characteristic X-rays and transmitted electrons that have lost energy through inelastic collisions with the atoms contained in the specimen. In STEM mode the diffracted signal intensity at each point is collected by an electron sensitive scintillator which generates visible light in response to electron impact. Some of the characteristic X-rays that are generated at each point are collected by the energy dispersive X-ray spectroscopy

(EDS) detector. The EDS spectrometer contains a silicon semiconductor crystal that is ionized by the incident X-ray of a particular energy resulting in an electric charge pulse of proportional size. The charge pulses are converted to a voltage, digitally sorted and displayed as an X-ray energy spectrum by the pulse processing electronics of the spectrometer. The transmitted electrons that have lost energy through inelastic interactions with the atoms contained in the specimen also contain characteristic information about the elements and chemistry of the specimen. An electron energy loss (EEL) spectrometer is used to collect and disperse the post specimen electrons according to energy. The spectrometer consists of a 90^{o} bending prism which disperses the electrons according to energy, a series of pre and post prism lenses and an electron sensitive camera. The scanned probe generates data points linked to the x and y position coordinates for each of the aforementioned signals resulting in a cube of data or spectrum image that can be subsequently extracted and plotted in a variety of dimensional combinations.

In following section we will explain these techniques in greater detail.

7.3.1 Transmission Electron Microscopy (TEM)

Knoll and Ruska [66] introduced first built electron microscope in 1932. Within 60 years, efforts in making better electron sources, electromagnetic lenses and sample preparation resulted in achieving 1 Å resolution. Detailed history of these efforts can be found in many references. [67-69]

The transmission electron microscope consists of multiple components which can be summarized as follows:

- Electron gun: generates the electron beam and accelerates it toward the sample. The gun consists of cathode, Wehnelt cylinder used in thermionic sources and the anode(s). Heat, a large electric field or a combination of the two is used to extract the beam of electrons from the filament or cathode. This is emission current. The anode then accelerates the electrons through a potential giving them a high kinetic energy, most commonly between 100-300 keV. The best resolution is achieved by field emission gun (FEG) sources where the electrons are extracted by a first anode and accelerated by a second anode.
- Condenser system: at least two sets of electromagnetic lenses and apertures. The condenser lens system transfers the accelerated electrons from the gun to form the illumination system for the TEM. The excitation of the condenser lenses electron beam determines whether the illumination is a parallel beam for conventional TEM (CTEM) or a focused probe for STEM. The apertures are inserted to block electrons that are far from the optical axis or adjust the convergence angle of the STEM probe.
- Objective lens: is the most important lens in the TEM. The specimen sits between the two pole pieces of the objective lens and it is the location where all of the beam/specimen interactions occur. The image is focused and magnified by the objective lens. The objective aperture is used in the back focal plane of the objective lens to select the electrons that will contribute to the final image. The objective aperture can be used to increase

diffraction contrast by blocking Bragg reflections, or to reduce aberrations by limiting the angular range of electrons that contribute to the image. By using different beam or sample tilt conditions combined with an objective aperture different types of images like dark field images can be formed.

- Imaging system: includes a series of intermediate and projector lenses and selected area aperture. The lenses magnify the image of the sample or diffraction pattern to the final magnification. The selected area aperture allows only electrons from limited area of the sample to reach detector. The selected area aperture is primarily used to collect selected area diffraction patterns (SADP).
- Viewing and camera system: Since electrons are not directly visible to the human eye, cathodoluminescence (CL) systems are required for viewing and capturing the images generated in the TEM. Most TEMs are equipped with a pair of directly observable viewing screens inside the chamber. These screens are coated with a fluorescent material like a doped ZnS that emits light in the mid-visible range. The most common type of image capture system uses a scintillator material like Ce-doped yttrium-aluminum garnet (YAG) fiber optically coupled to a CCD camera.
- Sample holder: A specialized TEM specimen holder is required to insert the electron transparent specimen in to the ultra-high vacuum chamber. The holder basically consists of sophisticated specimen tilt and translational motion systems and a long rod with a 3 mm hole or specimen cup at the

end. The specimen is clamped into place at the end of the rod. The holder is inserted into the TEM where it is positioned in the center of the optic axis held in between upper and lower pieces of objective lens by a goniometer.

- Vacuum system: For FEG systems vacuum as low as 10^{-9} Pa is required which can be achieved by ion getter pumps.
- Additional detectors: most modern TEMs are equipped with additional detectors like EDS, EELS and in some systems secondary electron detectors.

Figure 7-3 shows an overall configuration of a TEM. As electrons pass through the sample they suffer elastic and inelastic scattering. These scattered electrons form an image which is magnified using electron lenses and then captured by imaging system. TEM is one of the most powerful tools in science and industry for materials characterization. Aberration corrected TEMs can generate images with 0.5 Å resolution. [70] However, specimen condition and thus specimen preparation is critical to achieve such high resolution images.

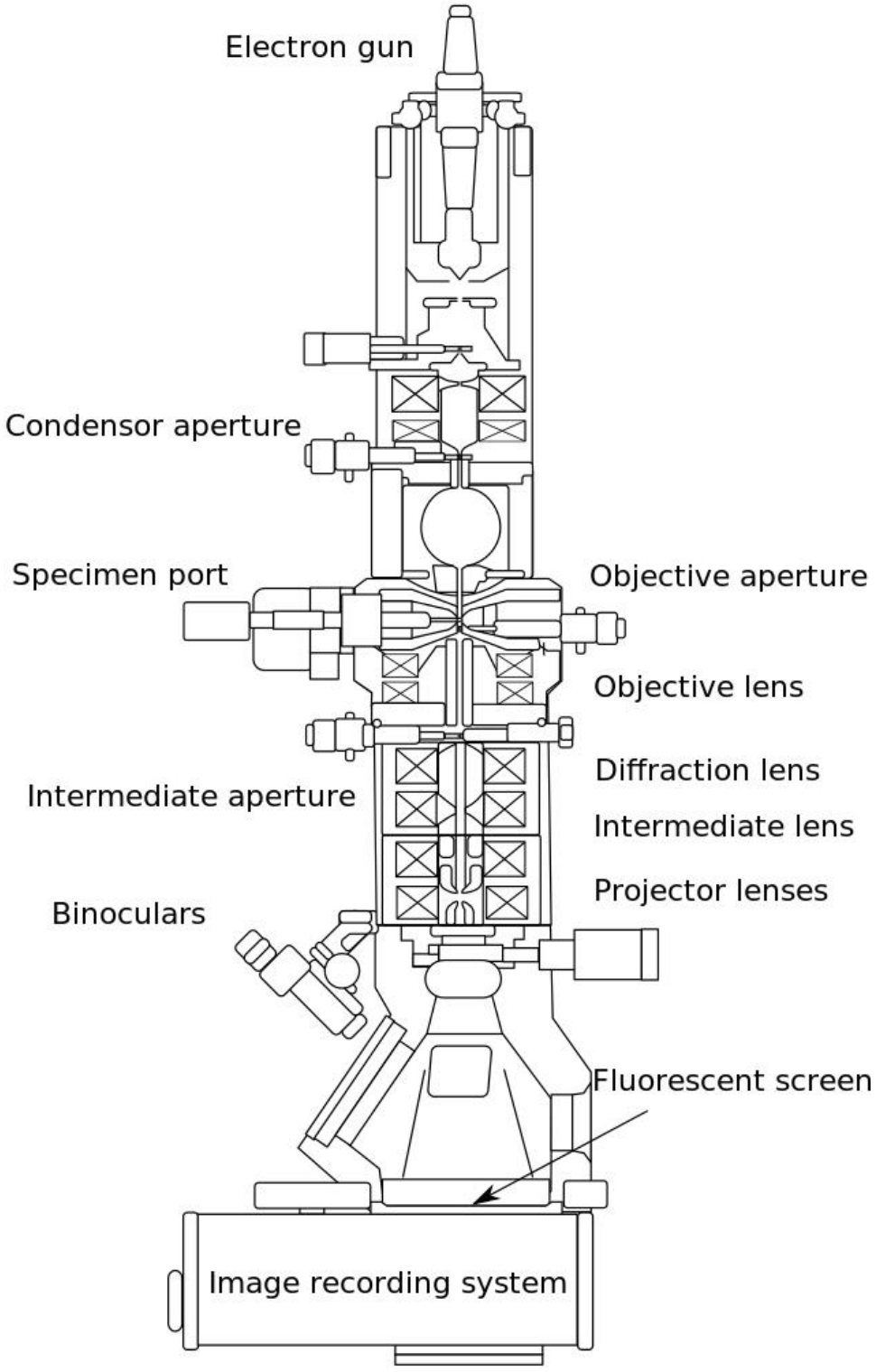

Figure 7-3 Schematic diagram of a Transmission electron microscope. [71]

7.3.2 Energy Dispersive X-ray Spectroscopy

When incident high-energy electrons pass close to an electron or the nucleus of an atom, they can deflect from their original path. These coulomb interactions cause electron scattering which is the basis of transmission electron microscopy. Electrons can interact with the specimen in different ways. The results of these interactions are what we described earlier as signals like characteristic X-ray generation or electron diffraction. Some of signals that are generated are detectable in TEM with current day detector and some remain illusive. Electrons that transit the thin specimen with minimal interaction and energy loss are referred to as being elastically scattered electrons. Elastically scattered electrons can also excite phonons with energy losses in the order of 10 eV which are very hard to observe in TEM. However recent efforts show promising results regarding Imaging of phonons in TEM. [72] Electrons can also generate plasmons and excitons with respective energy losses of 20 eV and 10 eV. Another type of electron-sample interaction product is the generation of X-rays. Plasmons are a regular feature in an EEL spectrum there are reports of observation of excitons with EELS. When a high energy electron hits an atom, it can eject a bound electron from a core shell leaving behind a vacancy. The atom will relax from the excited state by filling the core hole with an outer shell electron. The atom may then emit either a photon or an auger electron with energy equal to energy difference between the two energy levels. Since each atom has uniquely quantized energy levels, such transition result in the production of photons with energies that are characteristics of that atom. [65, 73] For most core shell transitions the characteristic energy corresponds to frequencies in the X-ray portion of the electromagnetic spectrum.

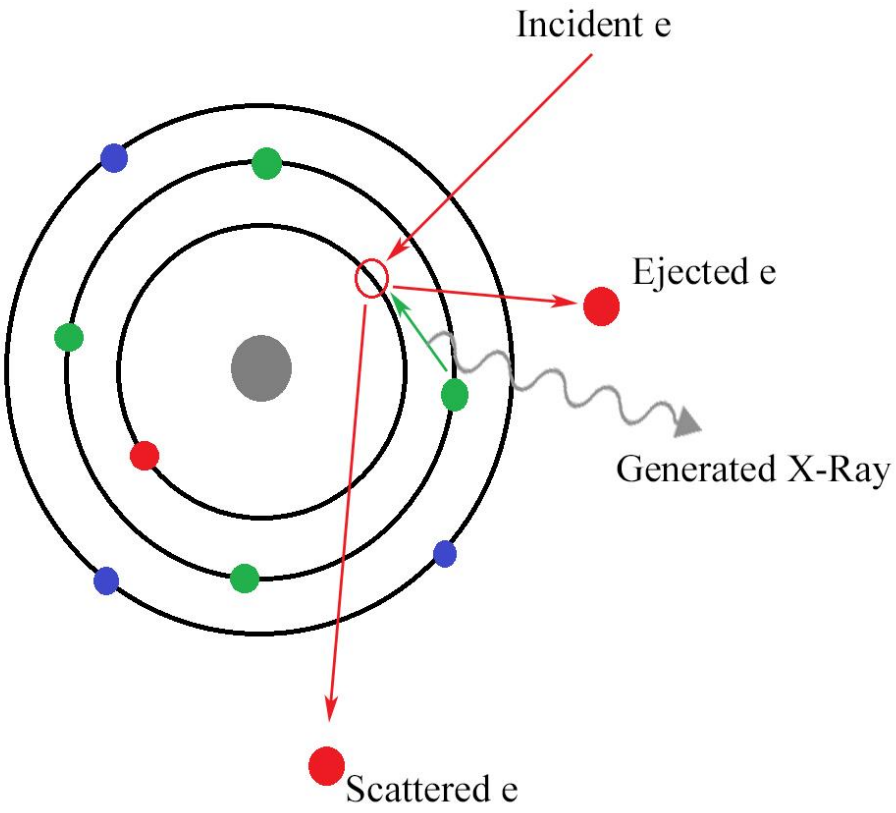

Figure 7-4 Characteristic X-ray generation caused by the interaction of a high energy electron with a core shell electron of an atom.

When the characteristic X-rays hit the active or charge producing Si semiconductor crystal of the EDS detector, electrons are transferred from valence band to conduction band which create electron-hole (e-h) pairs in the crystal. The energy for this process in a Li drifted Si detector Si(Li) is about 3.8 eV at liquid nitrogen temperature. A typical characteristic X-ray has an energy of well over 1 KeV. This means that each x-ray photon will create thousands of e-h pairs. The number of e-h pairs is directly proportional to the energy of incoming X-ray photon. The signal processing electronics of the EDS detector converts the charge pulses to a voltage which is then amplified through a field effect

transistor and then stored as a digital signal in the channel assigned to that energy in the computer display, thus creating an X-ray energy spectrum. [65] Figure 7-5 shows schematic diagram of a typical Si(Li) EDS detector. The Si(Li) detector has been the main detector used in AEM since about 1963 when they were first introduced into the TEM. [74] Some of the limitations of Si(Li) detectors are that they require uninterrupted liquid nitrogen cooling, they are ineffective for collecting X-rays of energies above 25keV and compared to the newer technology they are relatively slow and inefficient at collecting X-rays. Between 1963 and current day there have been several developments in the EDS detector technology that have never quite taken off, e.g X-ray calorimeters and intrinsic-Germanium detectors which could efficiently collect X-rays with energies up to 100keV, had a better signal to noise ratio and improved energy resolution as well. The most recent advance in EDS detectors is the Silicon-Drift detectors (SDD). They are basically a CCD consisting of concentric rings of p-doped Si implanted on a single crystal of n-Si. These detectors are rapidly and almost universally replacing the Si(Li) detectors. The SDD detector are Peltier cooled, have a large active area for significant improvement in collection efficiency (higher count rate), better energy resolution and better signal to noise ratio.

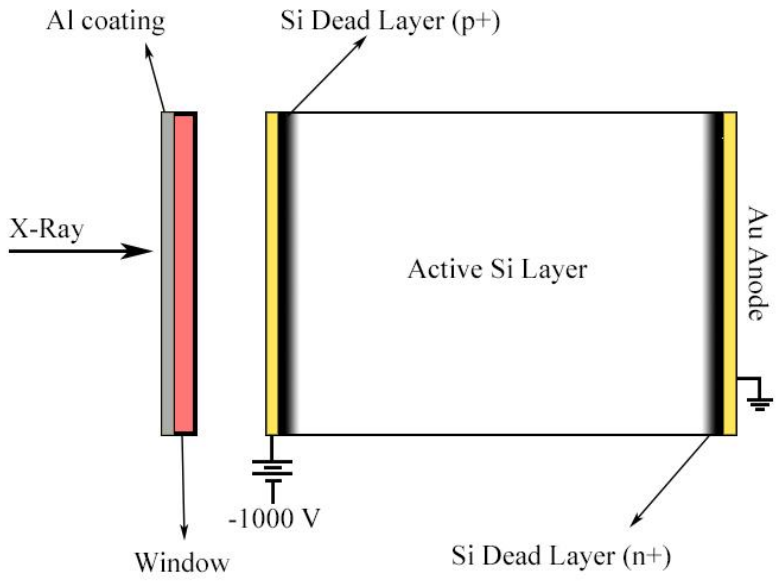

Figure 7-5 Schematic diagram of a Si(Li) X-ray detector.

7.3.3 Energy Electron Loss Spectroscopy

One of the biggest limitations of the EDS technique is the lack of sensitivity for elements lighter than oxygen. EELS provides a complementary technique for microanalysis in the TEM with a signal that can be simultaneously acquired with the EDS signal. EELS has very high sensitivity for the low atomic number elements. The two techniques together provide a powerful complementary analytical arsenal.

When an incident high energy electron passes through the specimen, it can inellastically interact with an atom causing an electron to be ejected from a core shell. Conservation of energy requires that the energy required to eject the core shell electron be equivalent to the energy lost by the beam electron. Because the energy levels of the atom are quantized and characteristic of that element, the energy loss of the beam electron is also characteristic of the electronic transition in that element. Thus, by using an electron

dispersive prism the electrons can be separated according to energy loss creating an energy loss spectrum. If an energy selecting slit is inserted into the spectrum, then the electrons can be filtered according to energy loss and an image can be formed with electrons that have lost a specified amount of energy. The latter is called energy filtered TEM (EFTEM).

The ability of the EELS spectrometer to disperse electrons according to energy is based on the following fundamental equations.

The force applied to electrons in a homogeneous magnetic field is equal to:

$$F = -e(\boldsymbol{V} \times \boldsymbol{B}) \quad (39)$$

Having this force equal to centrifugal force results in radius of trajectory equal to:

$$r = \frac{m|v|}{e|B|} \quad (40)$$

This means that electrons with different energies will have different trajectories and hence we can disperse them based on their energy. This is the basis of EELS. Post specimen electrons pass through a perpendicular magnetic field which cause them to follow different trajectories, this is the electron dispersing prism. The EELS detector consist of sets of pre and post prism lenses, the prism, the energy filtering slit and a scintillator CCD camera to capture an image of the spatially dispersed electrons, the energy loss spectrum or the energy filtered images. Whether the EELS spectrum or the EFTEM images is collected is dependent upon the microscope operating conditions and the spectrometer configuration. The energy loss spectrum is separated into regions which consist of the zero-loss peak formed by non-scattered and elastically scattered electrons. The zero-loss peak is several orders of magnitude larger than the rest of the spectrum. The region immediately following

the zero-loss peak is the low-loss region including plasmons excitation. Following the low-loss region is the core-loss region which results from interactions of the electron beam that have caused the ejection of core-shell specimen electrons. The core-loss region contains characteristic elemental energy loss edges as well as information about bonding and nearest neighbor atoms.

To characterize the elemental composition and morphology of a sample it is critical to understand the capabilities and the limitations of the techniques used. For this purpose we studied resolution limits of TEM and EDS and these studies are presented in next chapter.

CHAPTER 8 THEORY OF TEM and EDS RESOLUTION

8.1 Introduction

To obtain highest quality and most accurate results of a characterization technique it is important to understand its limits to avoid errors and erroneous conclusions. TEM data can suffer from various sources of artifacts. These can result from the TEM operating conditions, data interpretation or from the condition of the specimen. We will study specimen preparation in next chapter and it is ensured that all sample preparation requirements are met in this research. However, it is equally important to optimize TEM conditions for the most dependable final results.

The purpose of this research is to characterize the ultra-thin high-k gate dielectric layers in 22 nm technology node commercial ICs. This requires highest possible TEM and EDS resolution. Hence, in this chapter we will explore possible sources of TEM artifact and explain how to safeguard against them. We will then study TEM spatial resolution analytically and calculate its dependence on different beam and sample parameters. Later we extend our analysis to the EDS spectrum and the EDS line profile. These studies helped us to obtain best conditions for most accurate TEM and EDS results.

8.2 Potential Sources of TEM Artifacts

Imperfections in a TEM image or spectrum can be the result of errors, artifact or simply the limitation of the instrumentation. For example, a TEM designed with a thermionic electron source cannot be converted to a FEG source in a practical, easy nor cost efficient manner. As mentioned earlier there is significant difference between the

energy resolution as well as spatial resolution that the two types of electron sources can provide. However, some of limitations in modern TEMs can be corrected by means that are already manufactured in them. Most of such errors are related to TEM electromagnetic lenses.

Here we will compare various electron beam characteristics in TEM and compare these characteristics in different TEM sources. We will then explain TEM lens errors, how they impact electron beam and possible methods to correct for them.

8.3 Electron Source Types

Electron source can be categorized into Thermionic and field emission guns. Thermionic electron sources use heat to eject electrons from source material. According to Richardson's law [75, 76], current density is related to source temperature by:

$$J = AT^2 e^{\frac{-\Phi}{kT}} \quad (41)$$

Where k is Boltzmann's constant (8.6×10^{-5} eV/K), A is Richardson's constant and Φ is source work function which both are intrinsic characteristics of the source material/filament. Electron emission occurs in a thermionic source as the filament is heated temperatures high enough so that electron energy becomes higher than Φ so that they can escape the filament. To have a bright beam, good choices for source materials are those with either refractory materials or those with low work functions. Traditional choices have been tungsten with a melting point of 3660 K or more recently Lanthanum hexaboride (LaB_6) which has low Φ. High operating temperatures and relatively large filament diameter in tungsten sources create broad electron energy distribution and large probe

sizes, neither of which is suited for high resolution TEM or high energy resolution EELS. Although LaB_6 operates at lower temperature and has higher brightness, the lack of coherence, energy spread and large probe size is still not optimal for the most challenging applications facing modern AEM.

An alternative electron source is the field emission gun (FEG). The FEG has become mainstream within the past 15 years. FEG sources can be either cold extraction or Schottky where a combination of heat or strong applied field are used to extract electrons from the filament. Both types of FEG sources provide a highly coherent beam with very high brightness and a low energy spread. The fundamental equation governing field emission of electrons from the FEG source is as follows. When a bias is applied to a spherical point of radius r, electric field at the surface is:

$$E = \frac{V}{r} \qquad (42)$$

If a sharp tip is fabricated then, the electric field is very strong at that tip. The strength of the field at the tip is large enough to overcome the potential barrier and extract the electrons from tip of the filament to produce emission current for the electron beam. Such high fields can impose high levels of stress on tip and hence very mechanically stable materials are required for use in FEG sources. Tungsten is the current material choice due to its durability and because it can be fabricated as small as 100 nm in diameter. In addition to the requirements of the filament there are there are also stringent environmental requirements for the operation and longevity of a FEG source. FEG instruments require is ultra-high vacuum condition to keep them clean and prevent their oxidation. Table below summarize some of the most important parameters between common types of electron sources. [65]

Table 8-1 Comparison of different types of electron sources. [65]

Parameter	W Filament	LaB_6	Cold FEG
Work Function (eV)	4.5	2.4	4.5
Operating Temperature (K)	2700	1700	300
Brightness at 100 KeV (A/m^2sr)	10^{10}	5×10^{11}	10^{13}
Energy Spread at 100 KeV (eV)	3	1.5	0.3
Vacuum (Pa)	10^{-2}	10^{-4}	10^{-9}
Lifetime (hr)	100	1000	>5000

For this research we have used to type of TEMs and both of them are equipped with Schottky FEG electron sources which are by far best choices of electron source.

8.4 Electron Beam Characteristics

For most accurate final results, it is important to have best possible incident beam. In STEM mode the lateral spatial resolution of the imaging and microanalysis capabilities are directly linked to the probe size. As the beam passes through specimen it will be scattered by its atoms leading to beam spreading. Smaller incident beam diameter will result in a smaller exiting beam diameter which is an important factor in lateral spatial resolution as we will discuss later. Other factors like brightness, energy spread, coherency etc. each have theoretical value and are important in precise interpretation of final results. Here we will explain most important electron beam characteristics.

8.4.1 Beam Brightness

Beam brightness is defined as current density in unit of solid angle. The beam angular distribution is dependent on the type and performance of electron source. It becomes most important when we use small beam sizes. Brightness can be defined as:

$$\beta = \frac{4i_e}{(\pi d_0 \alpha_0)^2} \quad (43)$$

Where d_0 is beam diameter, i_e is emission current and α_0 is divergence angle. Brightness is an important factor when spectroscopy is performed in the TEM. Higher brightness in a small probe gives high spatial resolution and analytical sensitivity e.g. higher X-ray counts in EDS.

8.4.2 Energy Coherence and Spatial Coherence

. Electromagnetic lenses like physical lenses have different focal lengths for rays of different energy which results in chromatic aberration. It is then important to have a monochromatic beam with minimum energy spread. Table 8-1 shows beam energy spread for different types of electron sources. TEMs used in this research are equipped with field emission electron sources that have about 0.3 eV energy spread. Spatial coherency is another factor in determining the quality TEM images. Spatial coherence is most important in parallel beam images to give the highest quality phase contrast images and the best diffraction contrast in crystalline specimens. Spatial coherence is directly related to the size of the source. Perfect coherence would be achieved from a true point source, thus the extremely small size of the FEG tips provide a highly spatially coherent beam.

8.4.3 Beam Diameter

Beam diameter can be determined both theoretically and by measurement. A common definition of beam diameter is full width at half maximum of incident beam at beam cross over assuming it has a Gaussian distribution. This is however a very optimistic assumption since it requires fairly new source that is well centered along the optical axis with all beam aberrations such as astigmatism corrected.

The initial incident beam diameter is determined at the gun. However before it hits the sample it is broadened at two other points, once in condenser lenses due to spherical aberration and again at the final condenser aperture due to diffraction. The equation for the incident beam diameter will then be:

$$d = \sqrt{\left(\frac{2i^{0.5}}{\pi\beta^{0.5}\alpha}\right)^2 + \left(\frac{C_s\alpha^3}{2}\right)^2 + \left(\frac{1.22\,\lambda}{\alpha}\right)^2} \qquad (44)$$

Where α is the convergence angle, β is brightness, i is the beam current, C_s is the spherical-aberration coefficient and λ is the electron wavelength. [65] The first term in equation 44 is initial beam diameter, the second term is due to spherical aberration and can be neglected in in a C_s corrected TEM. The last term is due to diffraction. Finely focused, bright electron probes are essential for high resolution STEM imaging and spectroscopy. It must be noted that equation 44 incident probe diameter. What really defines the limits of lateral spatial resolution for imaging and microanalysis is the beam diameter at the exit surface of the TEM specimen.

There is also an experimental technique to measure beam diameter. This is done by taking an image of the probe. Beam diameter then can be identified by fitting a Gaussian function

to beam intensity profile and measuring its full width at half maximum. Two TEMs used in our experiments are FEI Titan 80-300 probe aberration TEM and FEI Tecnai F30 TEM. Calibrated measurements of beam diameter on these instrument showed 1 Å and 4 Å beam diameter respectively.

8.5 TEM and EDS Spatial Resolution

STEM EDS analysis of small features requires that we carefully consider the lateral spatial resolution of the instrument with respect to spatial dimensions of the features of interest. Unlike many techniques where no information can be obtained, lack of spatial resolution in STEM EDS will create artifacts that are hard to distinguish from actual features on sample. Hence we spend this section on analysis of our instruments to ensure that the capabilities of the instruments are sufficient to meet our requirements for analytical accuracy.

What defines X-ray spatial resolution in TEM is interaction volume of electron beam with sample. Smaller interaction volumes mean more localized X-ray signal and hence better spatial resolution. Unlike bulk samples where electron-sample interaction volume increases by incident beam energy, in TEM, higher beam energy causes less scattering of electron beam in sample and thus smaller interaction volume. Figure 8-1 shows electron scattering in 50 nm thick Silicon foil for two typical TEM electron beam energy. Figure 8-2 shows same comparison but with two typical voltages in SEM for a bulk sample.

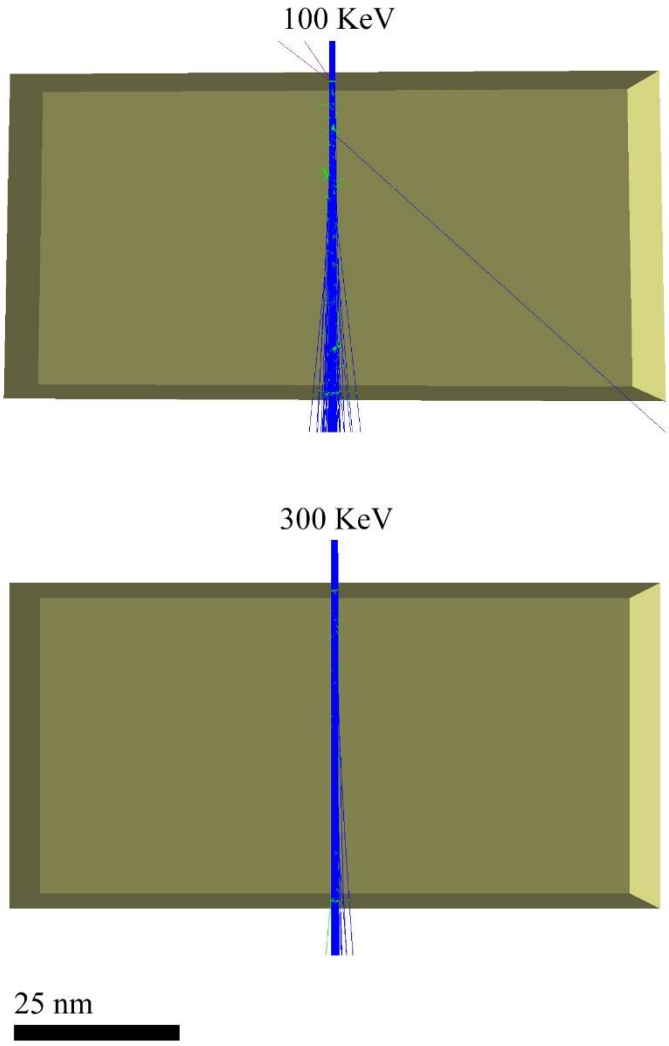

Figure 8-1 Monte Carlo simulation of TEM electron-sample interaction in 50 nm thick foil of Si with 100 KeV incident electron beam energy (top) and 300 KeV (bottom). As incident beam energy increases interaction volume decreases.

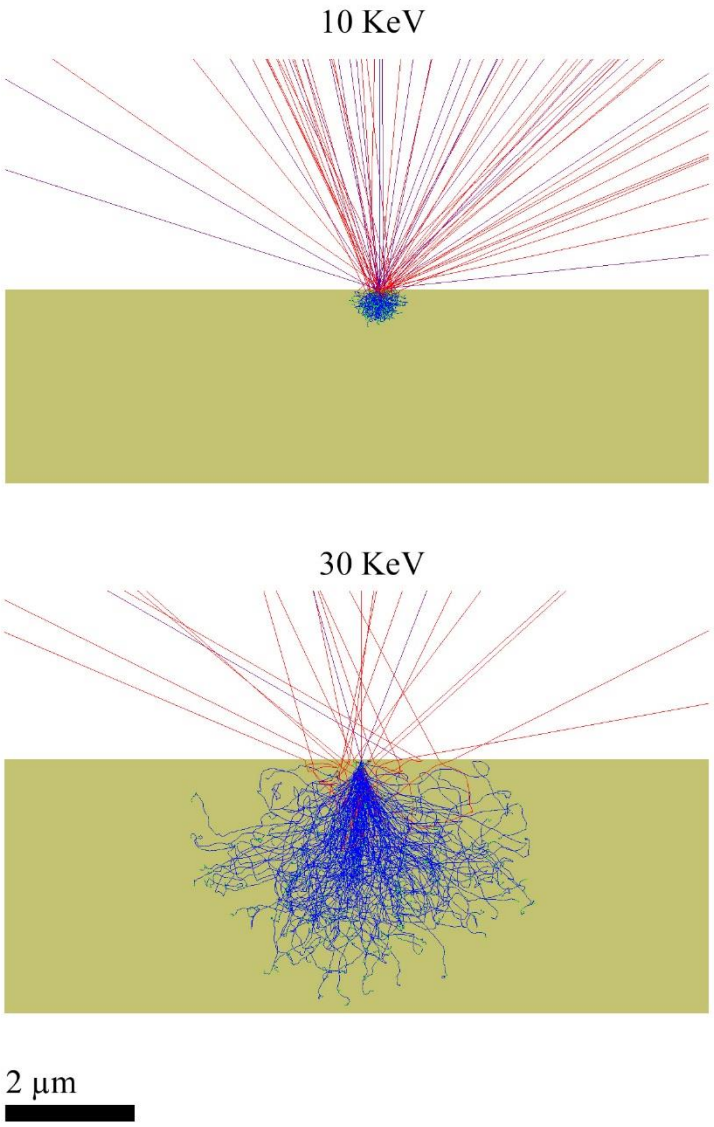

Figure 8-2 Monte Carlo simulation of SEM electron-sample interaction in 50 µm thick foil of Si (only portion of sample is shown) with 10 KeV incident electron beam energy (top) and 30 KeV (bottom). As incident beam energy increases interaction volume increases.

One of the electron-sample interaction products is X-ray. It can be generated anywhere within interaction volume and hence EDS spatial resolution is a function of this volume. Since thinner sample causes less scattering and hence less beam spreading, then

resolution will be effected by sample thickness and it is critical to prepare best possible sample to achieve good enough resolutions. However, this comes with the cost of less X-ray counts, longer acquisition time and lower signal to noise ratio. That is why there is no standard or ideal analysis parameters and we have to optimize all parameters in sample preparation and TEM to meet our analysis requirements.

Interaction volume depends on incident beam diameter, and beam spreading caused by electron scattering in the sample. We have already shown how to calculate and measure incident beam diameter. Beam spreading is defined by single scattering theory [77] as a function of beam energy, sample thickness and atomic number. In theory it is estimated [78] as:

$$b = 8 \times 10^{-12} \frac{Z}{E_0} (N_v)^{0.5} t^{1.5} \quad (45)$$

Where b is beam spreading, Z is sample atomic number, E_0 is incident beam energy, t is sample thickness and N_v is concentration of atoms or molecules per unit volume in the sample. N_v can be calculated based on number of atoms per unit cell and unit cell volume.

Next is to calculate spatial resolution. Assuming Gaussian distribution for both incident and exiting electron beam from sample, we can define spatial resolution (R) as [65]:

$$R_{max} = \sqrt{b^2 + d^2} \quad (46)$$

This is however worst possible resolution, a better approximation is achieved by convoluting Gaussian distributions of b and d in Gaussian model [79], which then defines R in the center of the sample as:

$$R = \frac{d+\sqrt{b^2+d^2}}{2} \quad (47)$$

Combining equations 45 and 47 we get:

$$R = \frac{d+\sqrt{d^2+\left(8\times10^{-12}\frac{Z}{E_0}(N_v)^{0.5}t^{1.5}\right)^2}}{2} = \frac{d+\sqrt{d^2+6.4\times10^{-23}\frac{Z^2}{E_0^2}N_v t^3}}{2} \quad (48)$$

For beam diameter (d) we will use measured values of 1 Å in Titan TEM and 4 Å in Tecnai TEM. All measurements were done by 200 KeV electron beam in Titan and 300 KeV in Tecnai.

Experiments were done on thin samples prepared by focused ion beam which will be covered in next chapters. These samples have about 20 nm thickness after final thinning. Table 8-2 and 8-3 show calculated beam spreading and resolution values for expected materials in high-k dielectric stack of analyzed samples for two different TEMs used in this project.

Results show sufficient resolution for all of these materials and their lattice constant are close to calculated spatial resolution. It is however important to mention that these calculations are estimates. In most of modern devices these materials are deposited with techniques that can lower their density compare to their crystal structure density and this will improve EDS resolution in TEMs. We will provide experimental results in chapter 10 with these materials distinguishable in TEM image as another proof of sufficient resolution.

Table 8-2 Parameters and final results for calculation of EDS spatial resolution in Titan TEM with 1 Å incident beam diameter and 200 KeV beam energy for 20 nm thick sample.

Compound	Z	Density ($Kg/m^{3)}$	Molar Mass (Kg/mol)	N_v ($1/m^3$)	Beam spreading (A)	Resolution (A)
SiO2	30	2650	0.06008	2.66×10^{28}	5.5	3.3
Al	13	2700	0.02698	6.03×10^{28}	3.6	2.4
Al2O3	50	3950	0.10196	2.33×10^{28}	8.6	4.8
Si	14	2329	0.02809	4.99×10^{28}	3.5	2.3
Ti	22	4506	0.04787	5.67×10^{28}	5.9	3.5
TiN	29	5400	0.06187	5.26×10^{28}	7.5	4.3
Hf	72	13310	0.17849	4.49×10^{28}	17	9.1
HfO2	88	9680	0.21049	2.77×10^{28}	17	8.8
Ta	73	16690	0.18095	5.55×10^{28}	19	10

Table 8-3 Parameters and final results for calculation of EDS spatial resolution in Tecnai TEM with 4 Å incident beam diameter and 300 KeV beam energy for 20 nm thick sample.

Compound	Z	Density ($Kg/m^{3)}$	Molar Mass (Kg/mol)	N_v ($1/m^3$)	Beam spreading (A)	Resolution (A)
SiO2	30	2650	0.06008	2.66×10^{28}	3.7	4.7
Al	13	2700	0.02698	6.03×10^{28}	2.4	4.3
Al2O3	50	3950	0.10196	2.33×10^{28}	5.8	5.5
Si	14	2329	0.02809	4.99×10^{28}	2.4	4.3
Ti	22	4506	0.04787	5.67×10^{28}	4.0	4.8
TiN	29	5400	0.06187	5.26×10^{28}	5.0	5.2
Hf	72	13310	0.17849	4.49×10^{28}	11.5	8.1
HfO2	88	9680	0.21049	2.77×10^{28}	11	7.9
Ta	73	16690	0.18095	5.55×10^{28}	13.0	8.8

CHAPTER 9 TEM PARAMETERS OPTIMIZATION

9.1 Introduction

Before any TEM and EDS measurements it is important to have a good understanding of TEM parameters and optimize them for the measurement. While some parameters are fixed and operator are encouraged to work with them, there are many others that have to be adjusted for best possible TEM performance.

In this chapter we will investigate the effect of some of these parameters on TEM resolution using Monte Carlo simulation of electron beam interaction with sample. Based on simulation results we conclude how to optimize TEM parameters in order to obtain required resolution. These results will be used in next chapters to get best possible signal for TEM and EDS. Here we will study the effect of sampling size, specimen geometry, instrumentation and accelerating voltage.

9.2 Monte Carlo Simulation of Electron interaction

In this section we will focus on Monte Carlo modeling applications in electron microscopy and microanalysis, for more in depth understanding of Monte Carlo method other references are suggested. [80-82]

Electron interaction with solid can be categorized in elastic and inelastic scattering. Former happens when electron keeps its energy but may change its direction due to the interaction and latter is when it losses some of its energy by generating some other type of particles like photons (X-ray), phonons etc. While many simpler theoretical models consider only one interaction between an incident electron and specimen, in reality

electrons may encounter many of these interactions. This will end only in one of these two ways, it can lose all of its energy and come to thermal equilibrium with sample or it can reach sample's edge and leave it. Considering that a TEM beam current of only 1 nA carries about 10^9 electrons per second toward the sample, it is impossible to have a theoretical model that can predict all electron trajectories with all possible interactions.

Monte Carlo method uses random sampling to fewer number of electrons to conclude about overall behavior of large number of electrons. This sampling however is made by considering probabilities of certain events such as scattering in specific angle. For example, if the probability of scattering an electron with angle θ can be determined by an experiment or a theoretical model as P(θ), then for each scattering event, Monte Carlo simulation will choose a random value (RND) and solve following equation to determine scattering angle α:

$$RND = \frac{\int_0^{\alpha} P(\theta) d\theta}{\int_0^{\pi} P(\theta) d\theta} \quad (49)$$

Repeating this process for each event will then determine trajectory of electron. Although this won't be necessarily an actual trajectory in experiment, simulating sufficiently large number of electron trajectories will provide a good estimation of expected experimental results. [83]

For simulation of X-ray generation by electron-specimen interaction we have to know cross section for X-ray production. A known formula for this cross section is [83]:

$$\sigma = 6.51 \times 10^{-20} . \frac{n_s b_s}{U E_c^2} \ln(c_s U) \quad (50)$$

Where n_s is number of electrons in atoms shell, E_c is ionization energy, U is defined as E/E_c, b_c and c_c are constants. This formula has number of ionization per incident electron with energy E per atom in unit of area in the sample. Based on equation 50 then number of x-rays produced per incident electron can be calculated as:

$$I_s = \sigma N_A \rho \omega . step/A \quad (51)$$

Where N_A is Avogadro number, ρ is density, A is atomic weight and ω is the yield. Equations 50 and 51 can be used to provide characteristics X-ray generation probability for a Monte Carlo simulation of electron beam interaction with thin samples.

9.3 Monte Carlo Simulation Tools

To calculate TEM and EDS spatial resolution and also optimize TEM parameters we used two software packages that use Monte Carlo simulation method in order to define electron trajectory. We will provide a brief description of these software in this section.

9.3.1 Casino v3.2

Casino, "monte CArlo SImulation of electroN trajectory in sOlids" [84, 85] is an open access Monte Carlo simulator of electron trajectories in solids and thin films. Casino v3.2 (2011) was used in this project. [86] Figure 9-1 shows main interface of this software. Performing a simulation in this software requires defining sample geometry, chemical composition, electron beam parameters, acquisition parameters, selection of physical model used for simulation and output options.

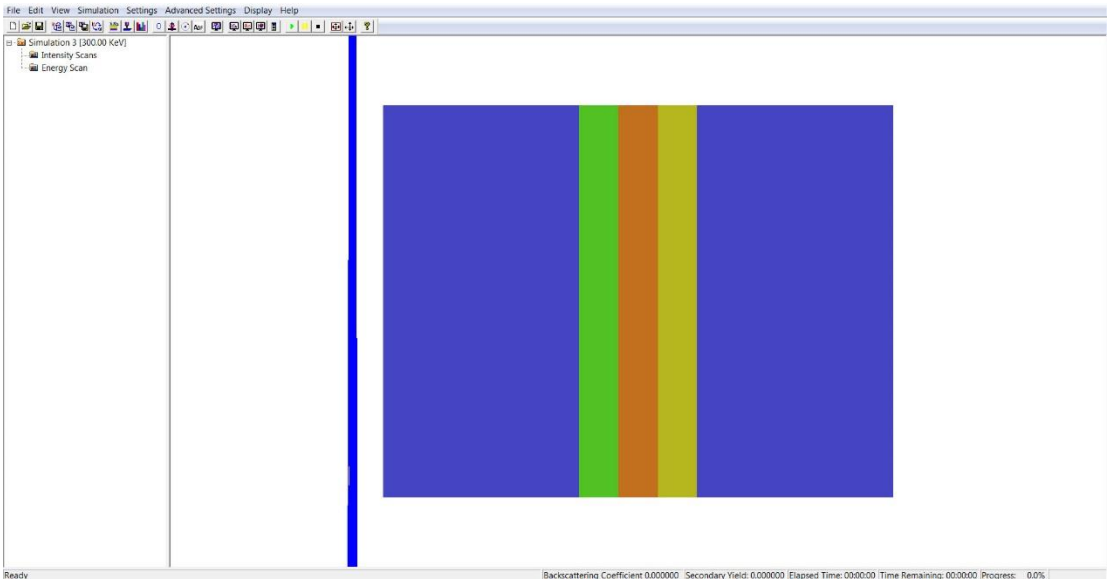

Figure 9-1 Main interface of Casino v3.2.

The process of simulation can be summarized as follow:

- Designing specimen geometry: any number of sample with various dimensions can be generated through setting>modify sample. To define how different parameters can affect our sample resolution, various layers with sharp interfaces are put side by side and electron beam scans across their interfaces. Materials are chosen based on expected compositions in analyzed samples.
- Microscope and simulation properties: accessed through setting>set up microscope, simulation parameters can be set up. For our studies 100000 electrons were simulated with 200 KeV and 300 KeV (depending on TEM used). Secondary electrons were considered and beam spacing and diameter

were varied for study their effects. In all cases incident beams were assumed with Gaussian distribution with 1.65 variance.

- Physical models: For cross section calculations Dirac partial-wave analysis for the electrostatic potential derived from Dirac-Fock atomic electron densities [87] were used. Random number generator used lagged Fibonacci [87] algorithm.

This software can produce number of results which we will explain in later sections.

9.3.2 MC X-Ray Lite v1.2

For EDS line scan simulations we used MC X-Ray Lite Version 1.2. [88] This program is an extension to Casino with additional capabilities of complete simulation of the X-ray spectrum and the charging effect for insulating specimen. Figure 9-2 shows this software main interface.

Although steps to prepare simulation are similar to Casino however MC X-Ray provide some additional capabilities in each section which makes it more suitable for our final simulation of EDS lines scans. In specimen tab, user can add as many number of regions and define their composition characteristics either manually or using available library in the software. For purpose of studying material diffusion effect on EDS line scans we designed mixed elements with variable concentration close to interfaces. In microscope tab many electron beam parameters can be defined as well as all characteristics of used detectors. Physical models were kept as close as possible to models used in Casino. In case on unavailability, default models were chosen.

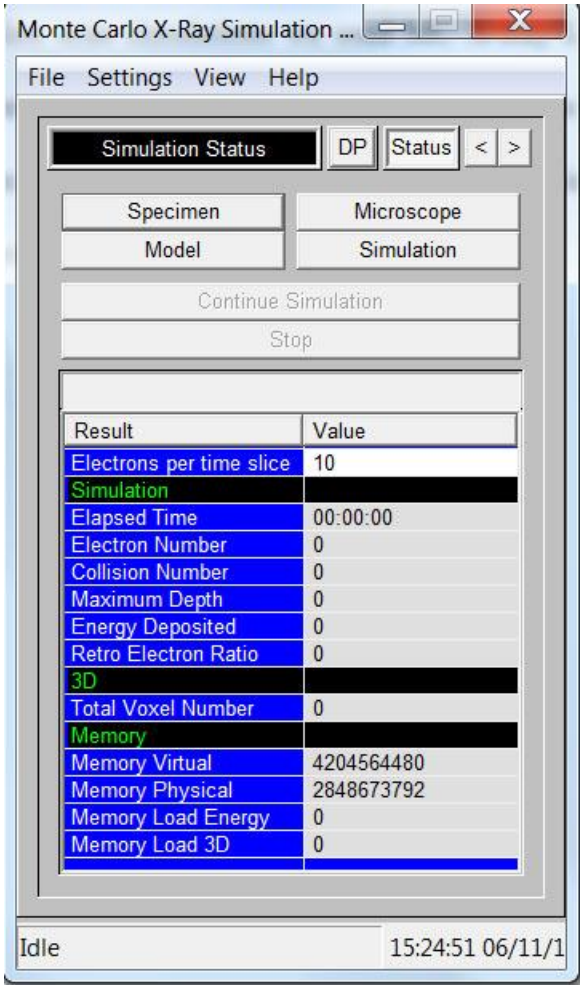

Figure 9-2 MC X-Ray Lite Version 1.2 main interface.

9.4 TEM Parameter Study and Their Optimization

Now that we explained tools and methods used here to simulate electron trajectories in sample, we will investigate effects of various parameters to obtain a better understanding of their role in TEM imaging and EDS mapping. Then we conclude what an optimum value for each parameter is in order to achieve most accurate results in our TEM and EDS analysis.

9.4.1 Beam Diameter

The ultimate goal of this project is achieve conditions for accurate detection of diffusion in the interfaces of thin layers of materials in high-k dielectric stack in a MOSFET gate. To achieve this goal we have to make sure how each TEM parameter will effect collected signal in EDS and TEM of interface region. First analyzed parameter is beam diameter. Typical TEM beam diameter in our measurements is between 1 to 4 Å. However, incident beam diameter depends on many parameters in TEM and hence it does not always poses its optimum value. So, here we will demonstrate effect various beam diameter in 1 to 4 Å range.

Figure 9-3 shows schematic of simulated specimen.

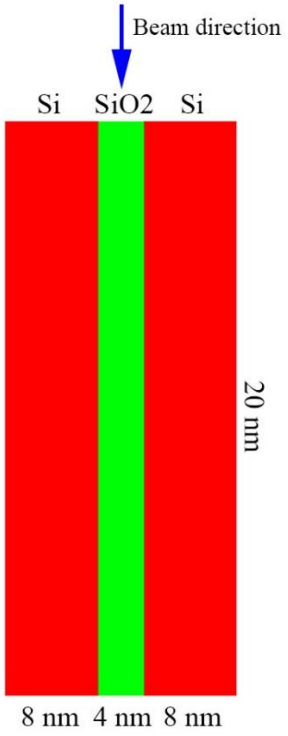

Figure 9-3 Schematic of simulated specimen.

Figure 9-4 shows transmitted electron intensity for a line scan across interfaces between three layers of Si, SiO_2, Si. For this result 100000 electron trajectories were simulated with 200 KeV incident beam energy. Beam diameter and beam step size where both set at 1 Å.

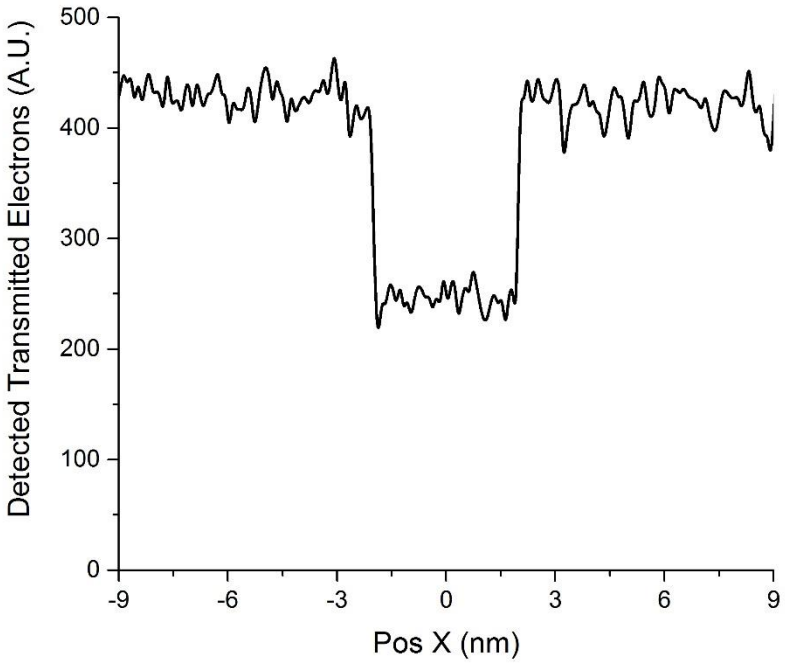

Figure 9-4 Simulated transmitted electrons counts through Si/SiO2/Si specimen shown in figure 9-3. A sharp interface is observed.

Figure 9-5 compare transmitted electron for three beam diameters. It is important to mention here that since beam spacing has an important effect which we will talk about it later, here we kept this value for these simulations 1 Å. This means that as we increase beam diameter, sampling points will have overlaps but number and positions of sampling points will be the same.

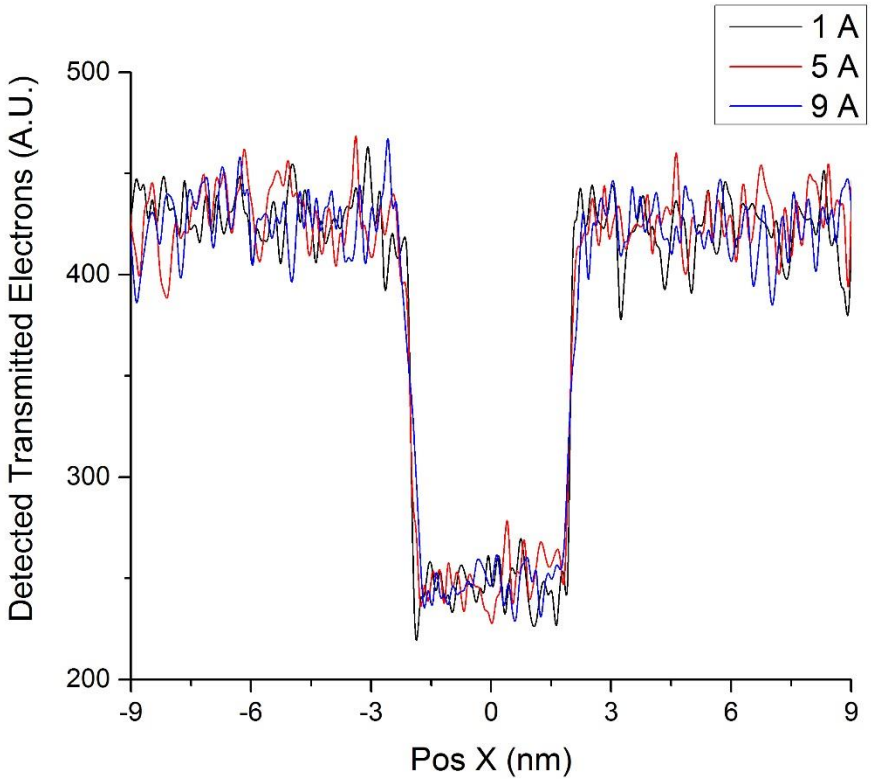

Figure 9-5 Comparison of transmitted electron signals for 1 A, 5 A and 9 a beam diameter with same beam step size of 1 A.

From figure 9-5 it may look like that incident beam diameter do not change interfaces appearance in TEM signal. However, if we look closer to interface region of these graphs the effect will be obvious. Figure 9-6 shows the right interface region for 5 different beam diameters with same parameters used before. From this graph it is clear that as beam diameter increase we lose resolution and detection of a sharp interface will be harder. For samples with atomically sharp interfaces, this lack of resolution will introduce an artifact which can be interpreted as diffused interface.

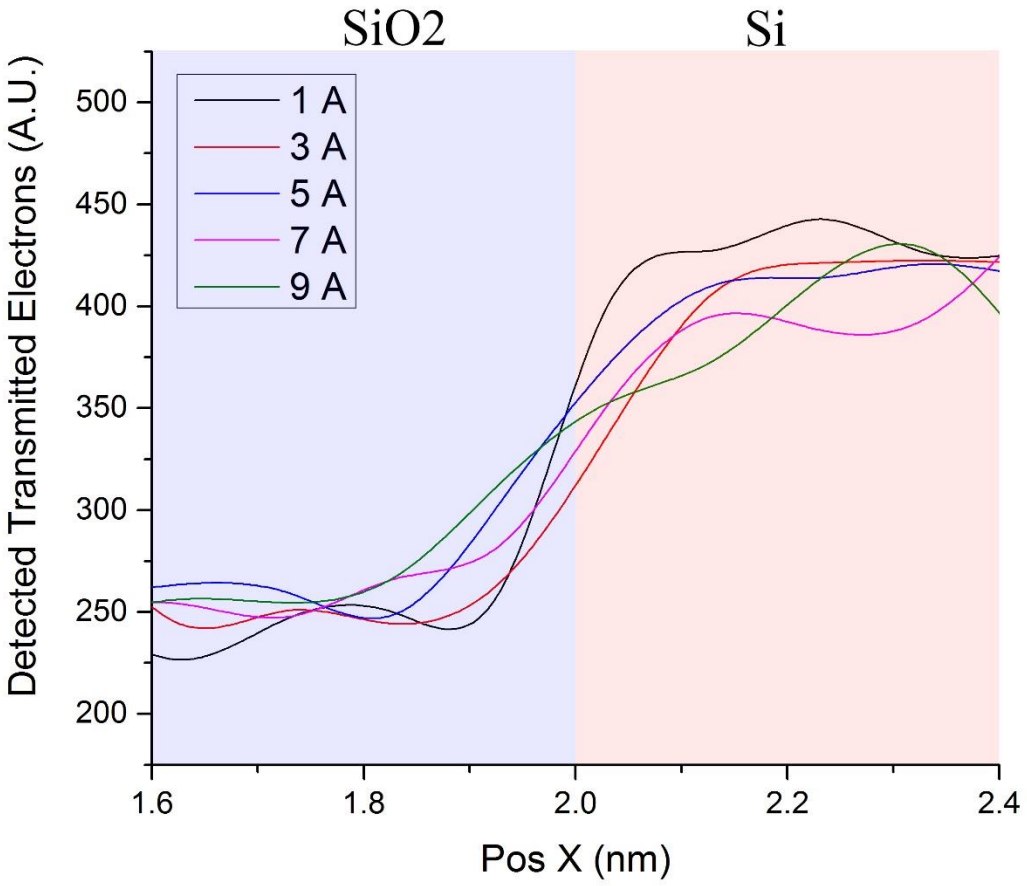

Figure 9-6 Transmitted electron counts for five different beam diameters with same beam spacing at the interface region of Si and SiO2.

9.4.2 Beam Spacing

To capture high resolution images or acquire EDS signals in TEM, electron beam is focused in a fine spot and spot scans the surface. In these cases incident beam diameter determines our probe size and smaller probe sizes provide better spatial resolutions. However, maximum probe current is proportional to the cube of probe diameter [65], hence higher probe current for better signal to noise ratio will require large probes.

Using a probe for scanning sample requires defining few other parameters. Assuming a line scan is intended, user has to define initial and final point of line scan, beam spacing and acquisition time. Among these beam spacing plays an important role in detection of fine features like an atomically sharp interface. Ideally, larger number of probing spots is preferred to increase sampling of region of interest. However, this will increase total acquisition time which can be costly and increase the chance of sample damage. Sample drift during the acquisition may reduce long acquisition's accuracy too. So it is important to understand beam spacing effect and its optimum value for each analysis.

Here we will use same type of sample geometry and composition for our simulation. This time beam diameter is kept at 1 Å but and beam spacing is varied from 0.5 Å to 5 Å. Figure 9-7 shows simulation of transmitted electrons signal along a line scan with three different spacing and figure 9-8 shows a closer view to right interface of Si and SiO2 for 6 different beam spacing. Smoothing artifact due to under-sampling across the interface is clear.

It is then up to analyst to decide how much beam spacing is required for detection of feature of interest in the specimen. This choice will also depend on how much damage beam can cause on the sample and on type of detectors used for EDS. Higher sensitivity will increase signal to noise ratio and hence increasing the number of sampling spots can be compensated by reducing acquisition time for each spot but keeping signal to noise ratio the same.

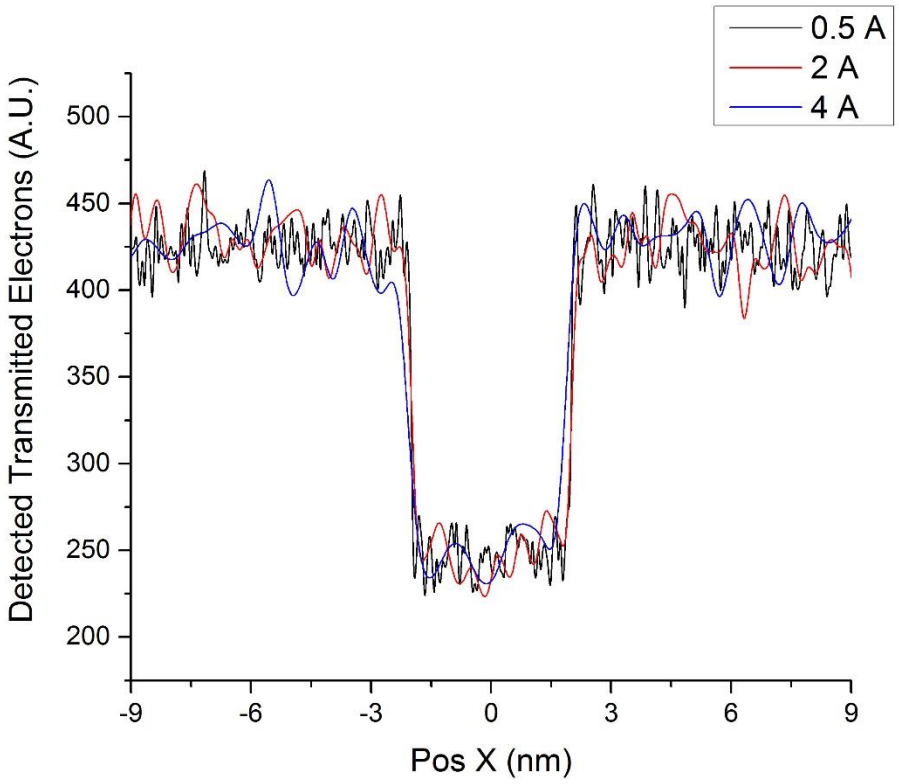

Figure 9-7 Transmitted electron signal for three different beam spacing.

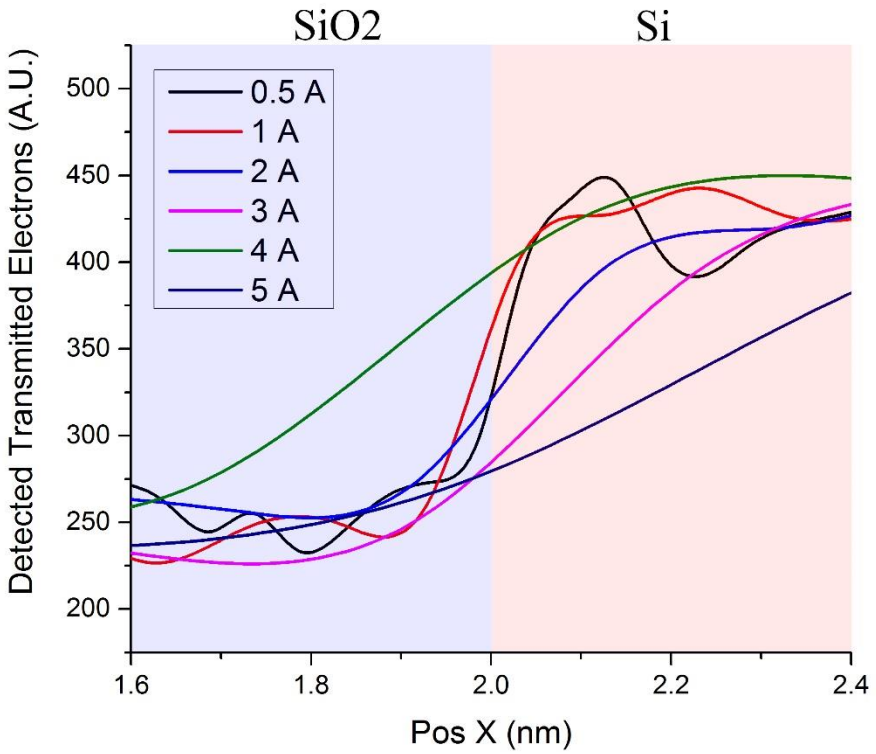

Figure 9-8 Transmitted electron counts for six different beam spacing with same beam diameter of 1 Å at the interface region of Si and SiO2.

9.5 Sample Thickness Effect

Other than beam parameters sample composition and thickness would also impact EDS signal resolutions. Thicker samples have higher chances of multiple scattering which increase beam spreading and worsen beam resolution. On the other hand, thinner samples have less inelastic scatterings and lower number of emitted x-rays, which decrease signal to noise ratio. Sample preparation technique used in this research will be explained in next chapter, here we study sample thickness effect and find out what thickness ranges are suitable for our study.

For these simulations sample thickness was varied from 5 nm to 40 nm while other parameters were kept the same. Beam focal point was set at the surface of the sample for all simulations. Beam diameter and beam spacing were set to 2 Å and beam energy is 200 KeV. Figure 9-9 shows normalized absorbed energy for beam positions around right interface of Si and SiO_2.

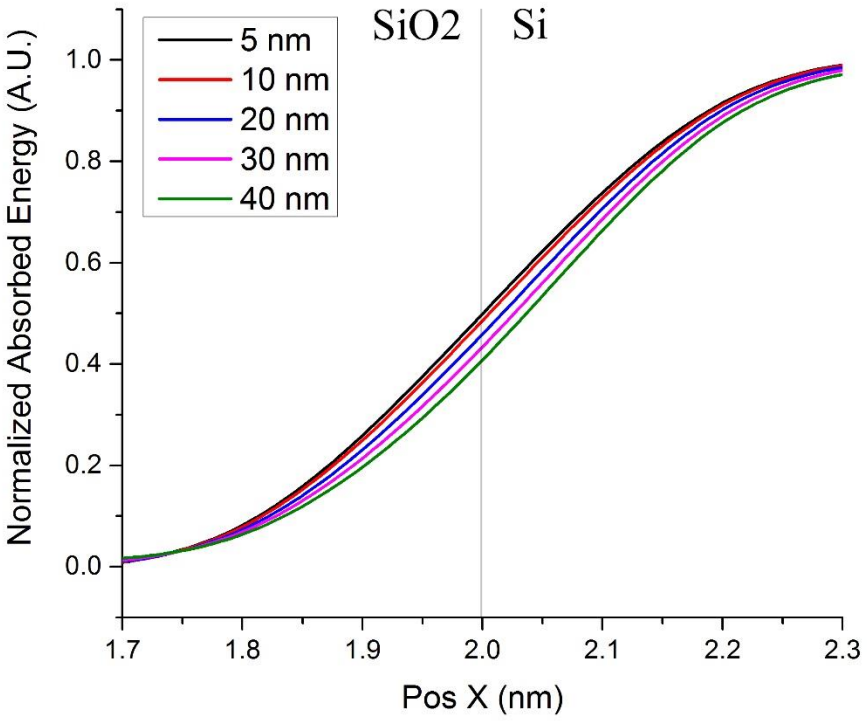

Figure 9-9 Normalized absorbed energy line scan across SiO_2 / Si interface.

Figure 9-10 shows a comparison between simulated electron beam trajectory through 10 nm and 40 nm thick vertical double layer of SiO2/Si. Beam is set parallel to the

interface surface and centered on it. Once again it shows how beam scattering will increase as sample thickness increases.

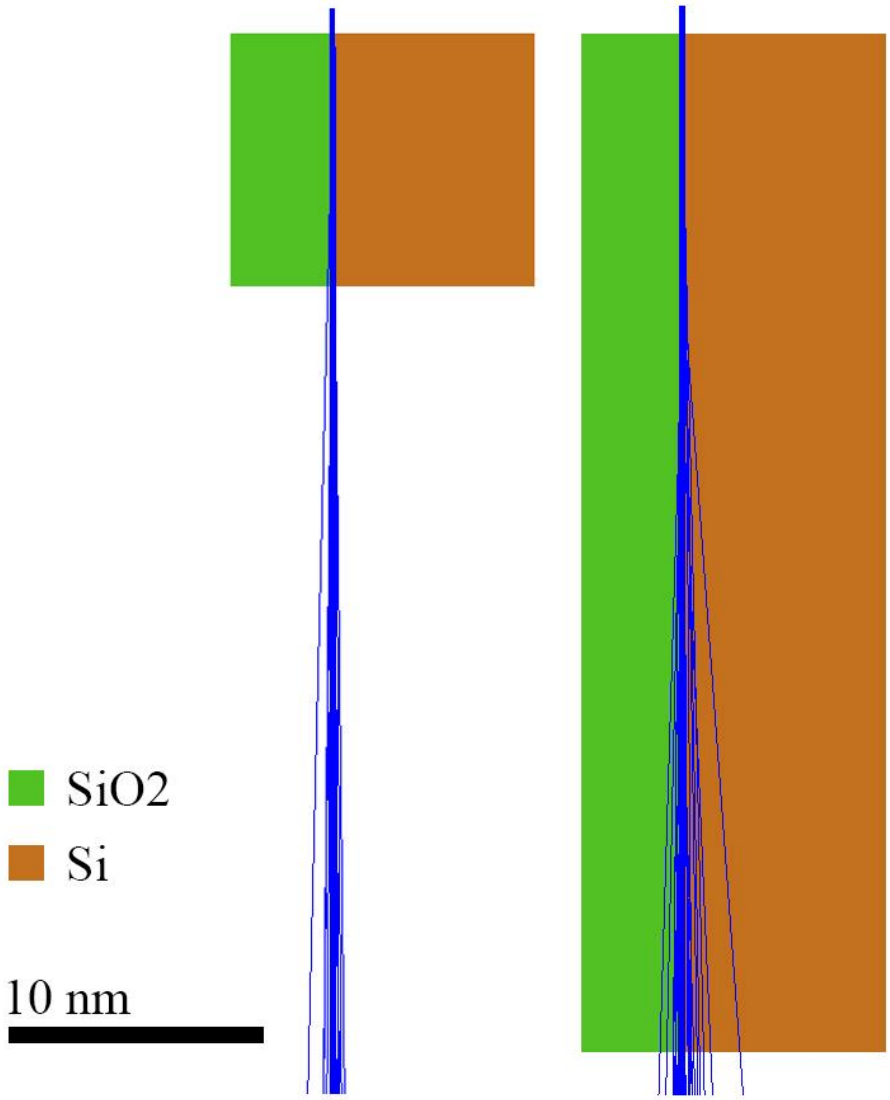

Figure 9-10 Comparison of electron beam scattering through 10 nm and 40 nm thick samples of SiO_2 / Si.

9.6 Conclusion

In this chapter we reviewed the fundamentals of Monte Carlo simulations and software packages we used for our study. Using these software, effects of various beam and sample parameters on beam spreading and detection of material interfaces are studied.

Although these studies provide good understanding of how the beam has to be optimized to avoid artifacts that resemble diffusion in the sample, analyzing a real sample with unknown characteristics and sample preparation imperfections makes some quantitative correlation between simulation results and experiments impossible. However, optimization of the beam using these results and standard samples creates an artifact free beam which can be used for analysis. Using such electron beam, experimental results are expected to reflect real nature of specimen. We will explain how we used this approach to obtain EDS line scans from two samples with various compositions at high-k dielectric layer and compared them to simulation results made with same beam parameters to reveal real diffusion of these dielectrics into each other.

CHAPTER 10 DIFFUSION DETECTION BY EDS LINE SCAN

10.1 Introduction

Last chapter beam parameters and sample thickness effects on beam spreading and spatial resolution of EDS and TEM signals were studied. Assuming an optimized beam and sample thickness, one may expect a sharp drop (or jump) in EDS line scan results. However, if the materials across the interface are diffused into each other, this will create a smooth transition from one composition to the other across the interface. Here we will study this effect using Monte Carlo simulations. We will then present simulation results from two different devices assuming sharp non-diffused interfaces at their high-k dielectric layers. After explaining sample preparation methods we will compare these simulations with experimental results and conclude about diffusion extent of these layers in our samples.

10.2 Diffusion Effect in Simulations

Fabrication of modern semiconductor devices may include thousands of steps that many require heat treatments. As heat is applied to the device, atoms gain kinetic energy and vibrate which depending on their treatment temperature may cause lattice distortions due to atoms migrations. Explaining diffusion mechanism and its theory is outside of this dissertation interests and further explanations are referred to references. [89] These heat treatments may also cause chemical reactions at the interfaces between two materials in a device. Many studies are done to demonstrate effect of reaction–diffusion in high-k dielectrics. [90-92]

Here we are interested in detection such possible diffusions in fully processed semiconductor devices. However, before presenting experimental and simulation results, we demonstrate appearance of this effect in a simple double layer of Si/SiO2 by Monte Carlo simulation of EDS line scan across their interface.

Three simulations are presented here, figure 10-1 shows simulated line scan across a sharp interface of SiO_2 and Si layers. In this simulation no diffusion is assumed which means oxygen mass fraction is uniformly 0.533 in SiO_2 layer and 0 in Si layer. Figure shows that even though the interface is 100% sharp, the line scan is steep but not vertical. Such slight deviation from vertical line is artifact created by beam spot size. For some collected data points in Si region close to interface beam is scattered into SiO_2 region too, hence x-rays are generated from both Si and Oxygen.

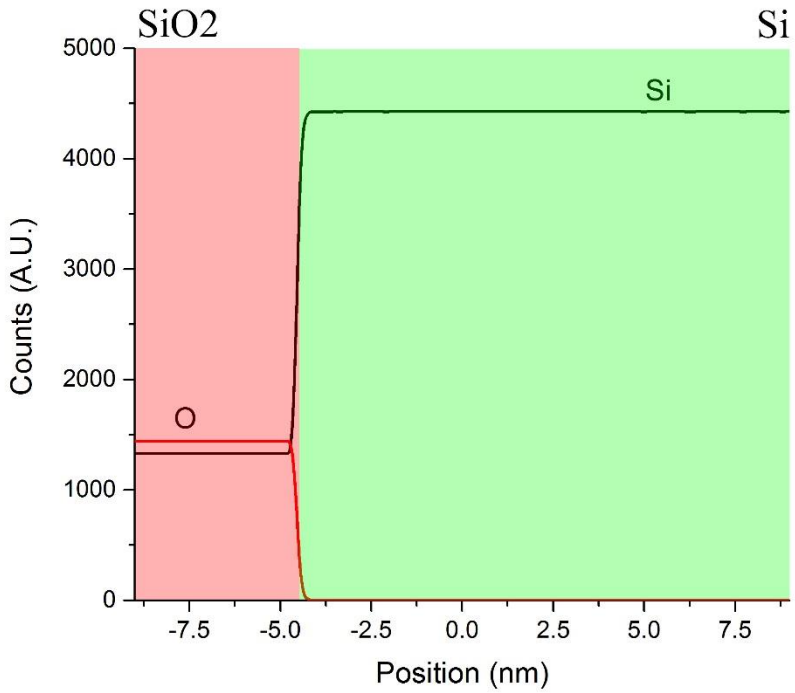

Figure 10-1 EDS line scan simulation across non-diffused SiO2 / Si interface.

Figure 10-2 shows simulated results when oxygen distribution is Gaussian with its standard deviation equal to 1 and figure 10-3 has similar results for case of standard deviation equal to 5.

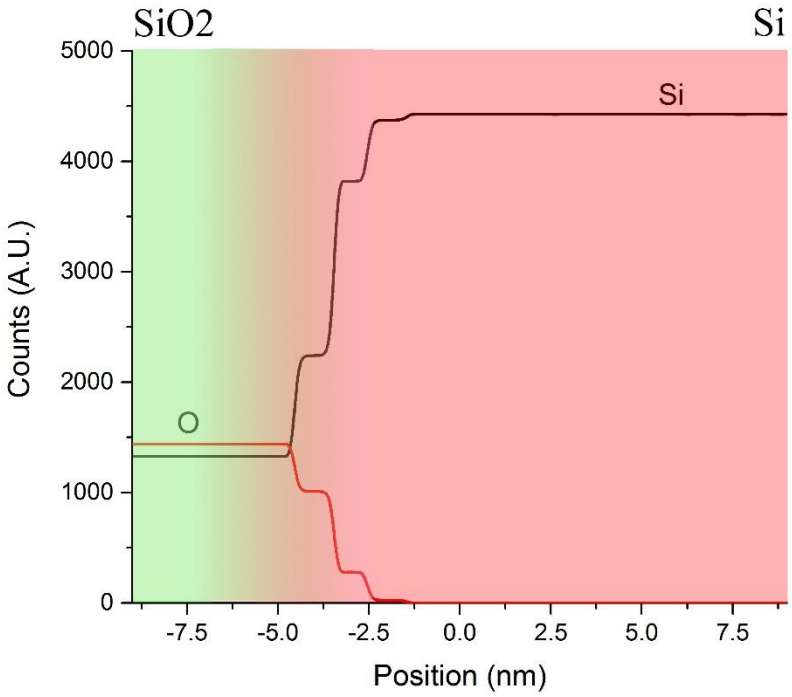

Figure 10-2 EDS line scan simulation across diffused SiO2 / Si interface with normal distribution of standard deviation equal to 1.

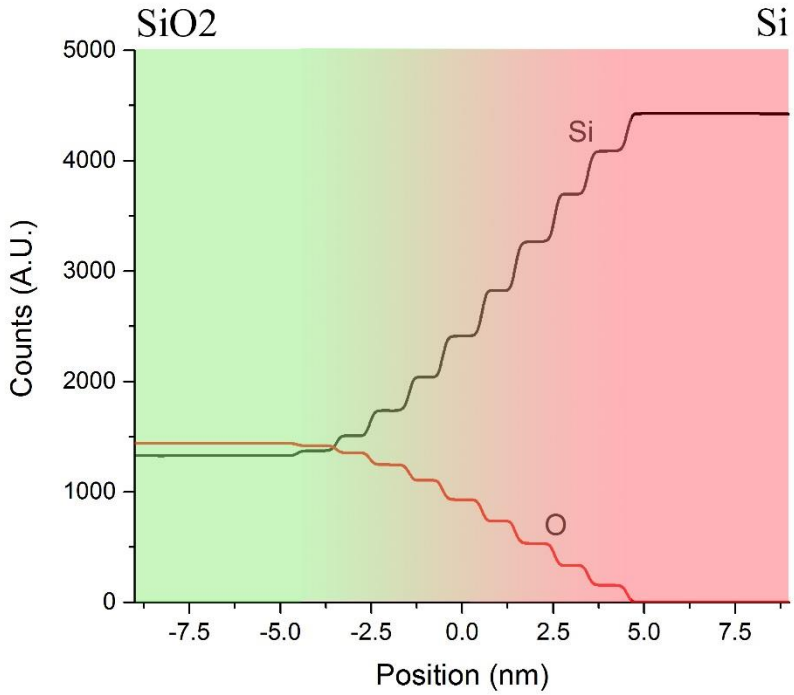

Figure 10-3 EDS line scan simulation across diffused SiO2 / Si interface with normal distribution of standard deviation equal to 5.

Steps in these line scans are artifacts of simulations. For each simulation interface was divided into several 1 nm intervals and Oxygen to Si weight ratio was set based on normal distribution. For a natural sample this transition will be much smooth with no such steps as we will see in later sections.

10.3 Sample Preparation

To obtain high resolution TEM images and EDS line scans from our samples they had to undergo series of sample preparation steps before being ready for TEM. These sample preparation steps were done at NanoSpective, Inc. teardown labs and Materials

Characterization Facility (MCF) of University of Central Florida. We will explain these steps briefly in this section.

10.3.1 Teardown

Sample preparation for characterization of a fully processed semiconductor IC usually starts with identification of an electronic device that has incorporated that IC in one of its printed circuit boards. Once identified, device will be carefully disassembled and documented for future references. Depending on selected device, tear down process may also include heating for adhesive loosening, mechanical sectioning or other techniques. An example of a teardown process is shown in image 10-4.

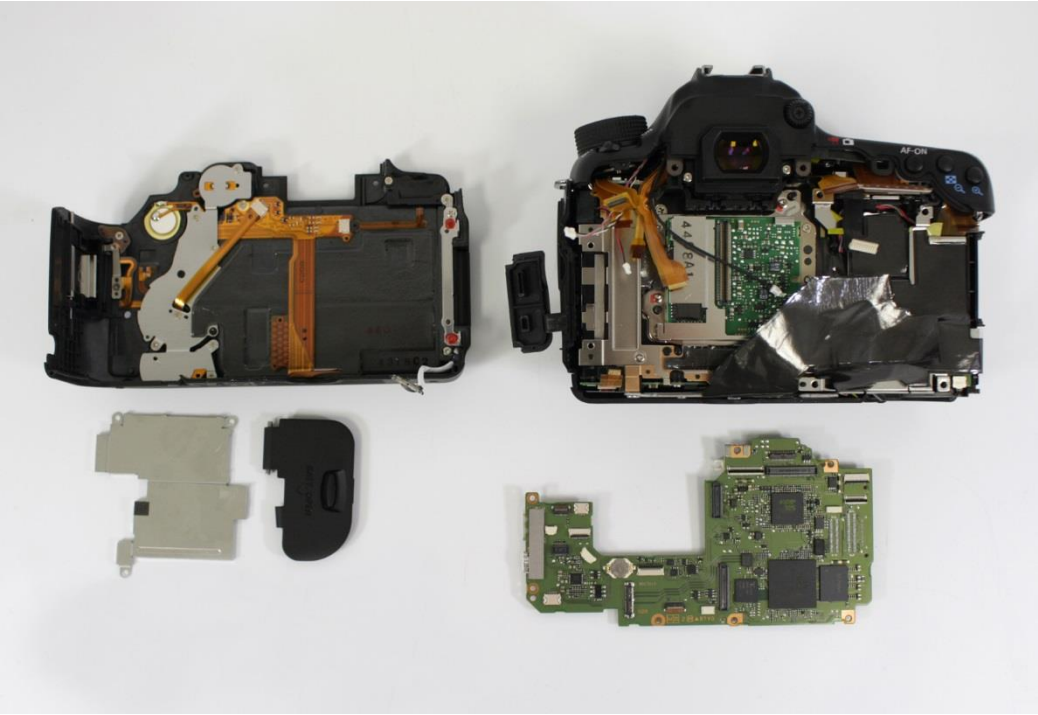

Figure 10-4 Example of torn down electronic device to access contained PCBs. Image used courtesy of NanoSpective, Inc.

10.3.2 Decapsulation

Once the device is torn down, the PCB that has IC package will be subjected to local heat to remove that package from PCB. Once the package is removed from PCB and documented, it will be dissolved into an acid solution chosen based on packaging material. In some specific cases like multi-chip packaging, an x-ray microscopic imaging helps in pre examination of package and better handling in decapsulation process. Figure 10-5 shows an x-ray image of a multi-chip package from different angles.

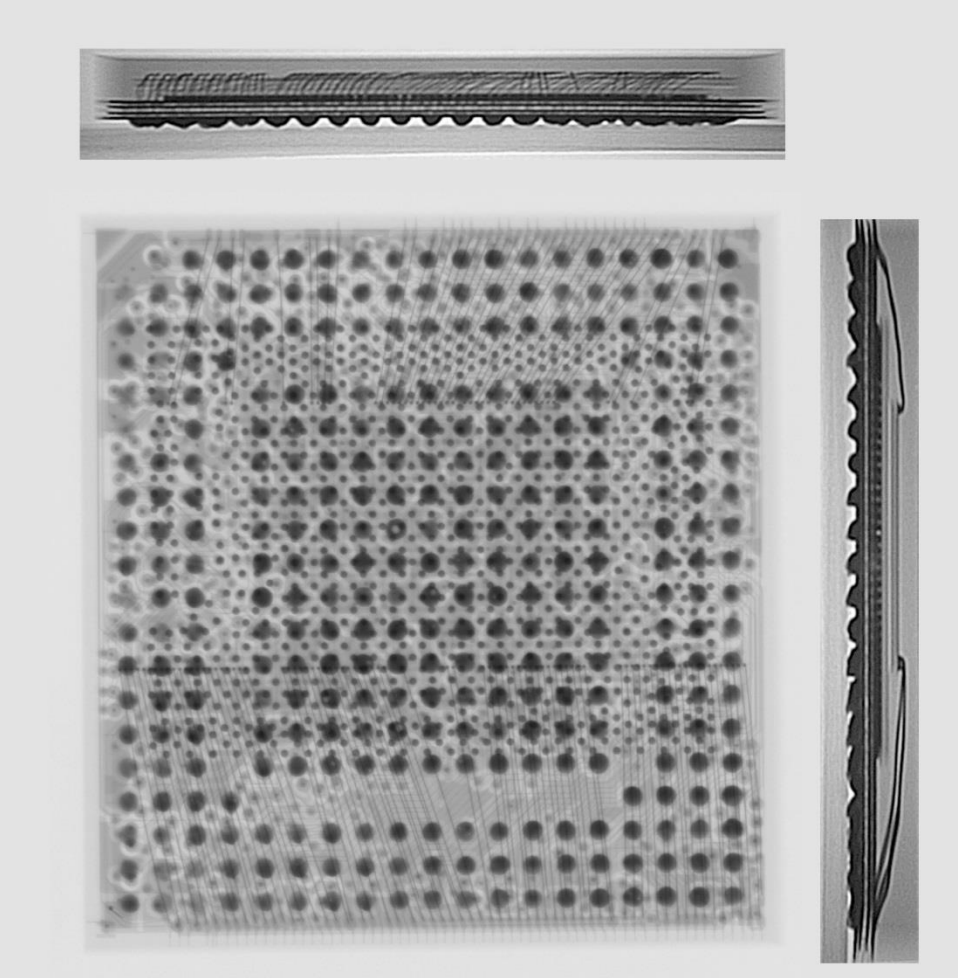

Figure 10-5 X-ray image of a multi-chip package from different angles. Image used courtesy of NanoSpective, Inc.

Figure 10-6 shows an IC package before decapsulation and removing of packaging material.

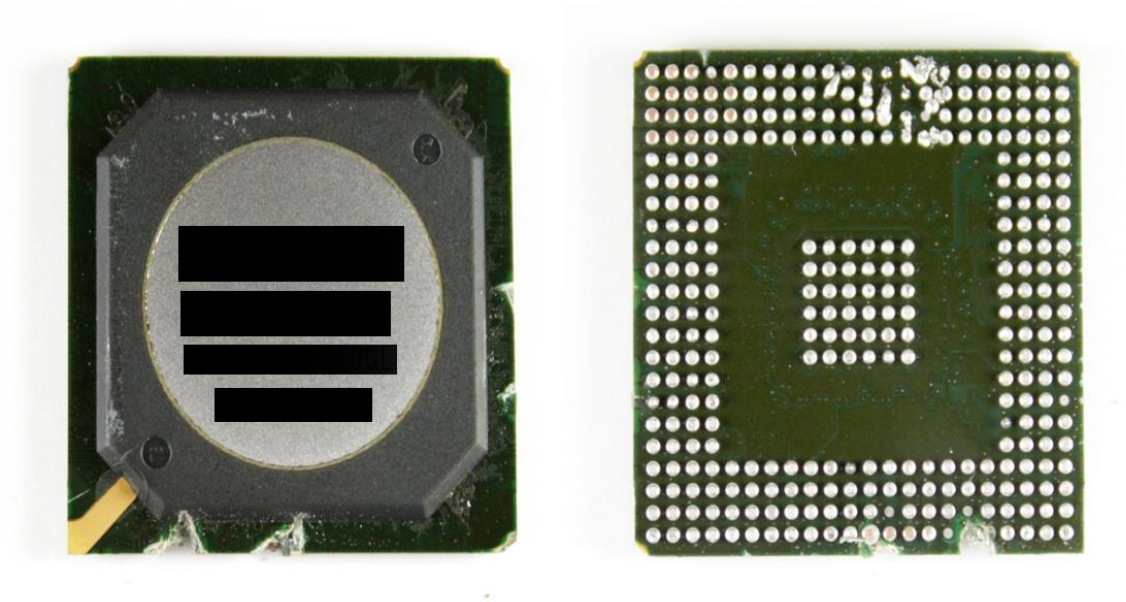

Figure 10-6 IC package front and back side before removal of packaging materials. Image used courtesy of NanoSpective, Inc.

10.3.3 Light Optical and IR Microscopy

With over millions of transistors in modern ICs, with various tasks and designs for example in system on chips (SoC), it is critical to investigate IC's designs by non-destructive methods first and pinpoint approximate region of interest on the die. This is done through series of light optical and infrared microscopy. In particular, front side light optical image and back side infrared images provide valuable information about die circuitry and enable the analyst to locate region that requires investigation. Figure 10-7 provide an example of front side light optical and back side infrared image of a die.

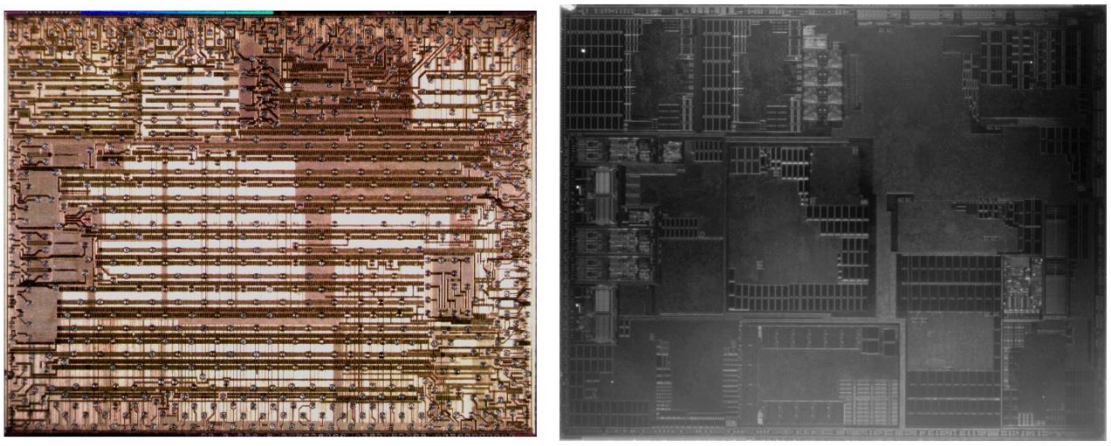

Figure 10-7 Front side light optical and back side infrared image of a die. Image used courtesy of NanoSpective, Inc.

10.3.4 Cross Section and Plan View Polishing

Modern ICs may have up to 13 layers of metallization, which makes it impossible to look at lower levels patterns from top side since they are obscured by upper levels of metallic patterns. Even though IR backside imaging helps in identifying regions, its low resolution compare to dimensions of gates in moderns ICs leaves no chance for identifying lowest levels of patterns and some of die characteristics like its technology node based on gate physical dimension. To achieve this goal, series of mechanical polishing are done parallel to the surface of the die and also on die's cross section. Polishing usually starts with providing the die with additional support to avoid fracturing. This is done by fixing the die on an aluminum block for plan view polish and between two pieces of silicon and glass slide for cross section polish. Then sample is polished by set of diamond lapping films and alumina slurries from 30 µm particle size down to 0.05 µm. Final polish is done

on polishing nap using only DI water filtered for particles smaller than 50 nm. Figure 10-8 shows light optical microscope image of plan view polished die.

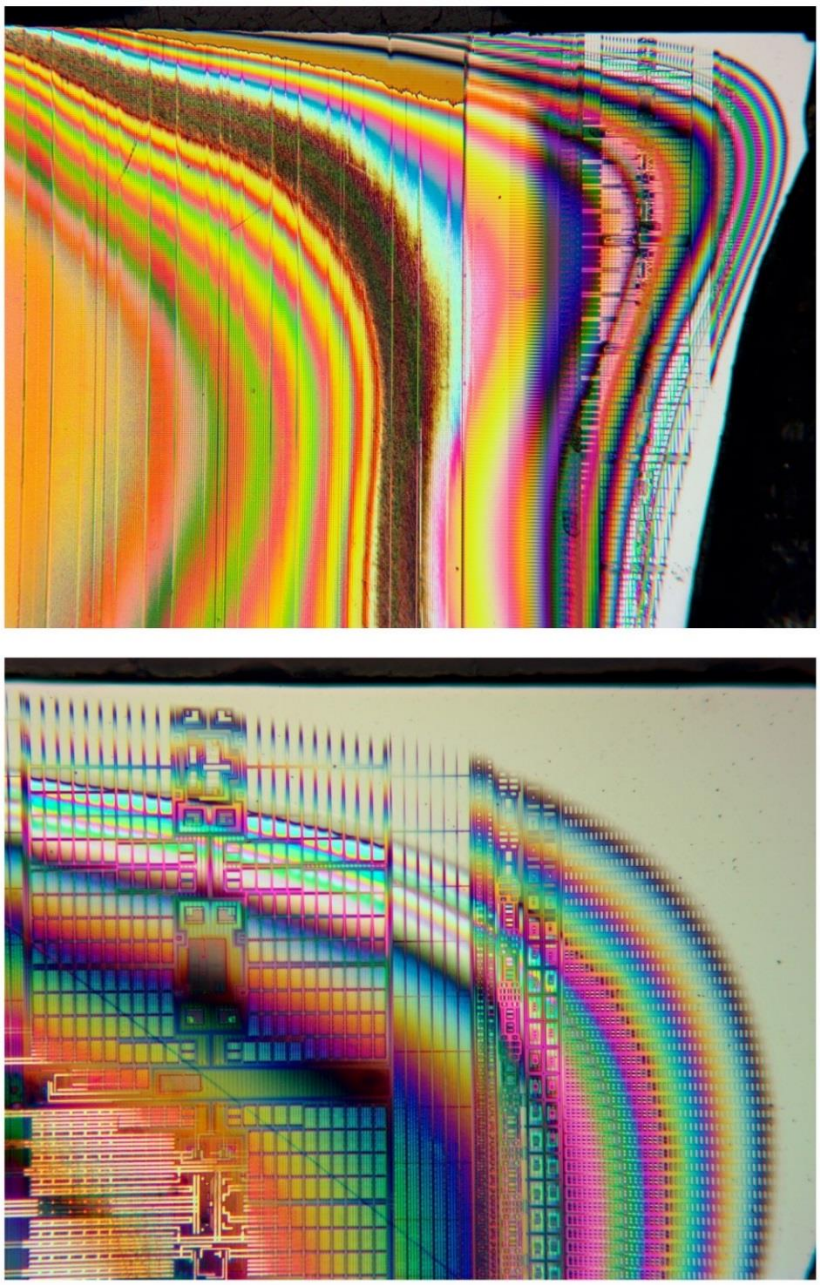

Figure 10-8 LOM images plan-view bevel polished die showing multiple levels of interconnect down to substrate. Images shown at two different magnifications reveal different levels of detail. Image used courtesy of NanoSpective, Inc.

Scanning electron microscopy is used to study cross-section and top plan view polished of these dies. For enhancement of image contrast and revealing various features of interest like dopant junction depth, metal routing, inter-dielectric layers, etch stop layers etc. various combinations of wet and dry chemical and plasma etching are used before electron imaging. Figure 10-9 shows tilted SEM image of skeleton etched sample showing top metal runners in different layers and locations on the die. This was done by optimization of reactive ion etching recopies for grass free anisotropic etching of dielectric layers. Performing this technique on a beveled plan view polished sample helps in finding exact area of interest on the die by following metal runners from one level to the next.

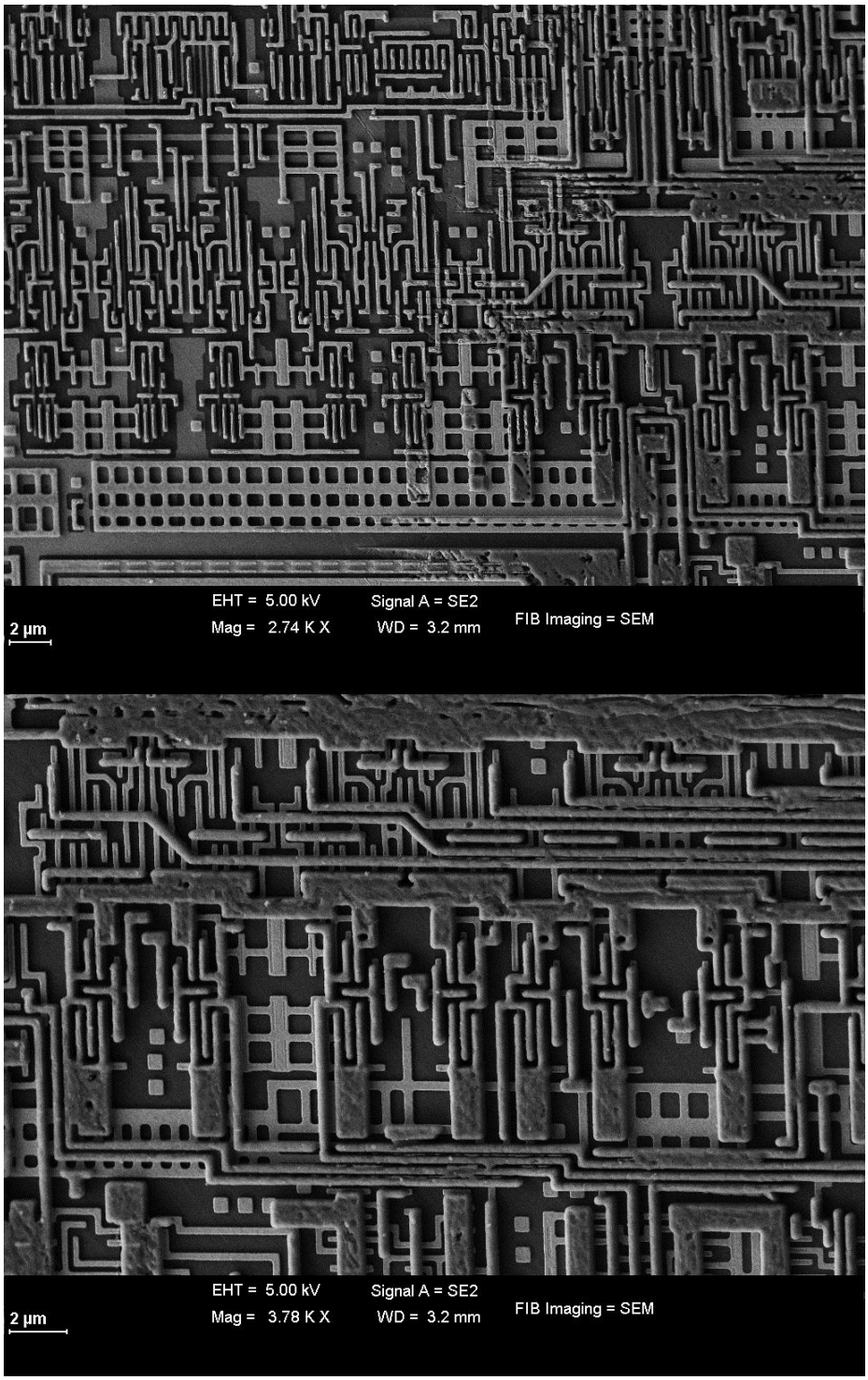

Figure 10-9 SEM images of sample that was skeleton etched after subsequent to a plan-view beveled polish. Image used courtesy of NanoSpective, Inc.

Figures 10-10 and 10-11 are SEM images of cross section polished sample at different magnifications. Wet chemical etchings together with SEM imaging techniques was used to identify junction depth and gate physical dimensions.

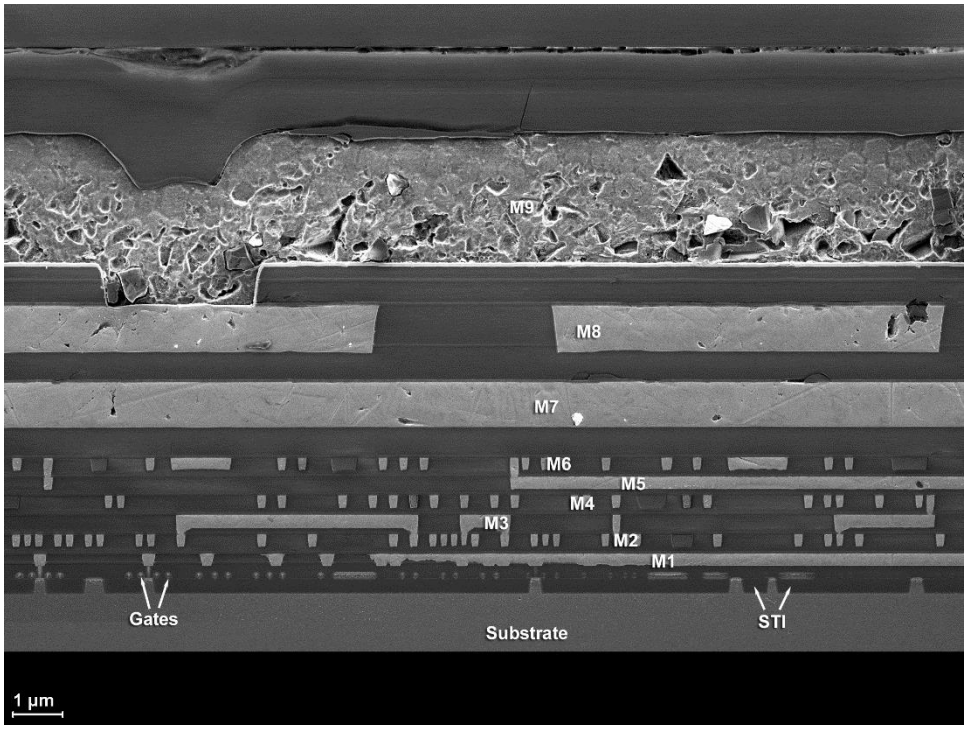

Figure 10-10 A die cross-section SEM image at low magnification showing all levels of metallization. Image used courtesy of NanoSpective, Inc.

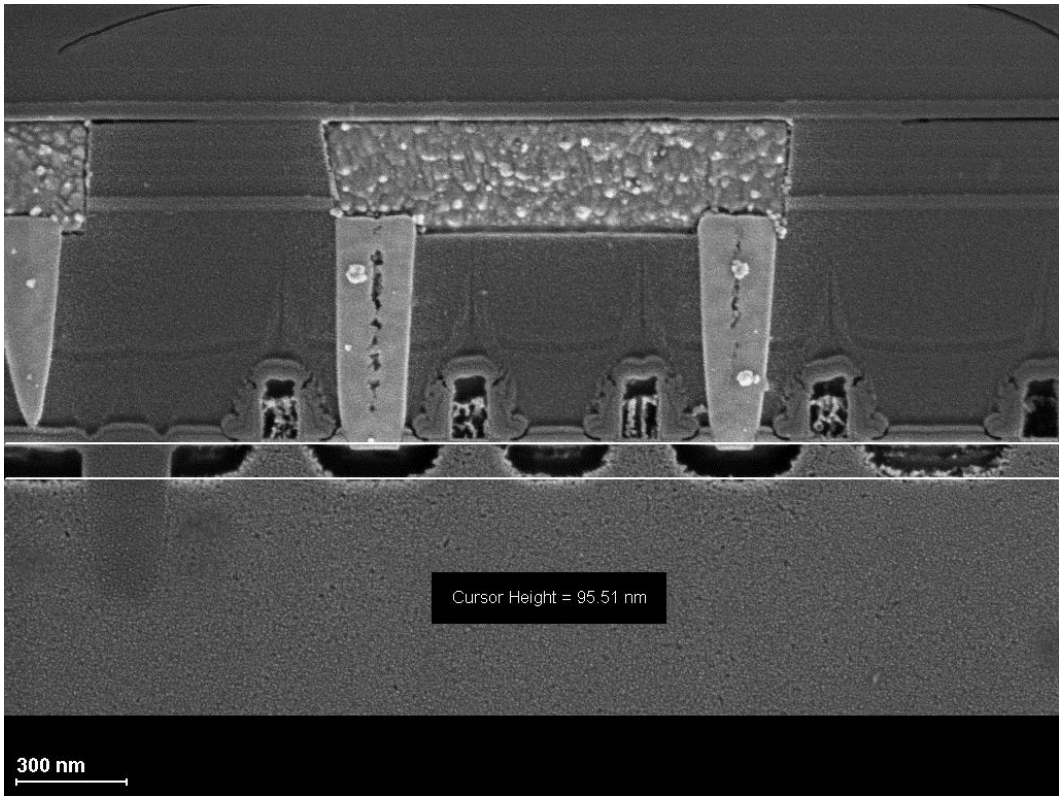

Figure 10-11 High magnification cross-section SEM image showing the dopant depth and transistor structure after wet chemical etching. Image used courtesy of NanoSpective, Inc.

10.3.5 Focused Ion Beam (FIB)

After thorough sample investigation using scanning electron microscope to identify device technology, some of its characterization and locating exact sample extraction location and direction, focused ion beam is used to extract and prepare TEM sample. This is done by following steps:

- Creating wedge shaped holes on two sides of region of interest so that final sample surface is perpendicular to gate directions. This step is shown in figure 10-12.

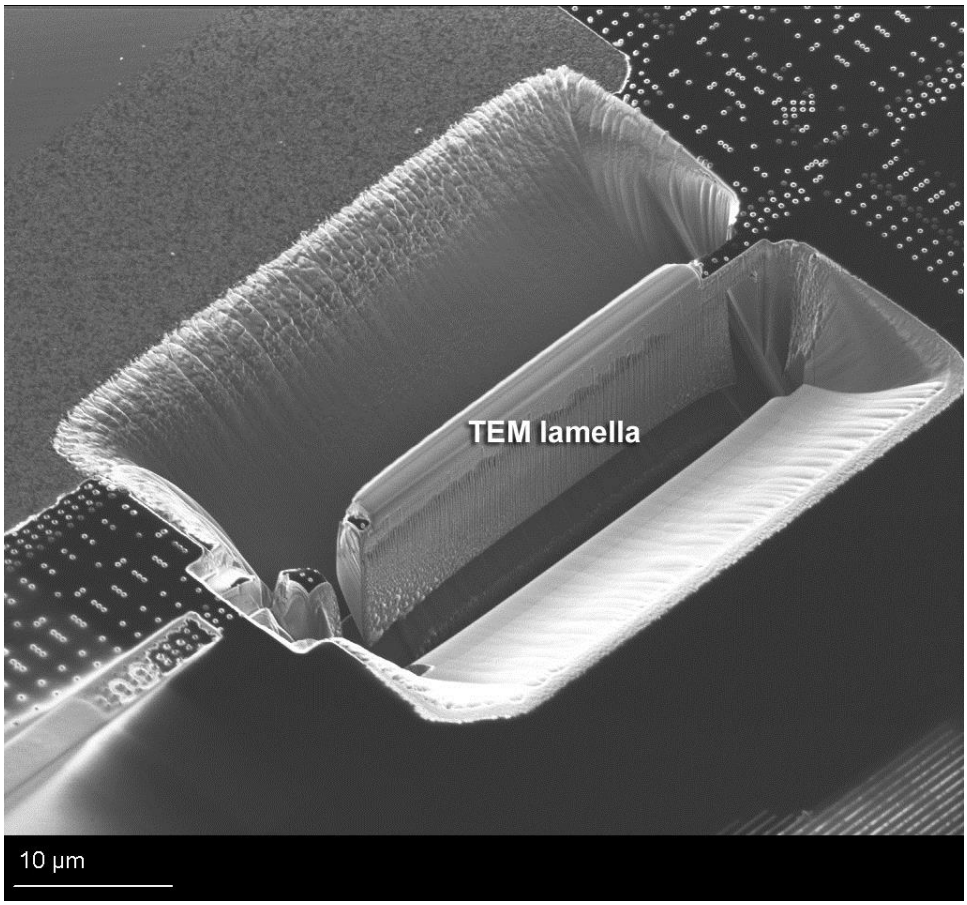

Figure 10-12 TEM lamella creating by cutting wedge shaped holes on two sides of region of interest.

- Welding the sample to an extraction probe and cutting its sides to release it from the die. Figure 10-13 shows this step.

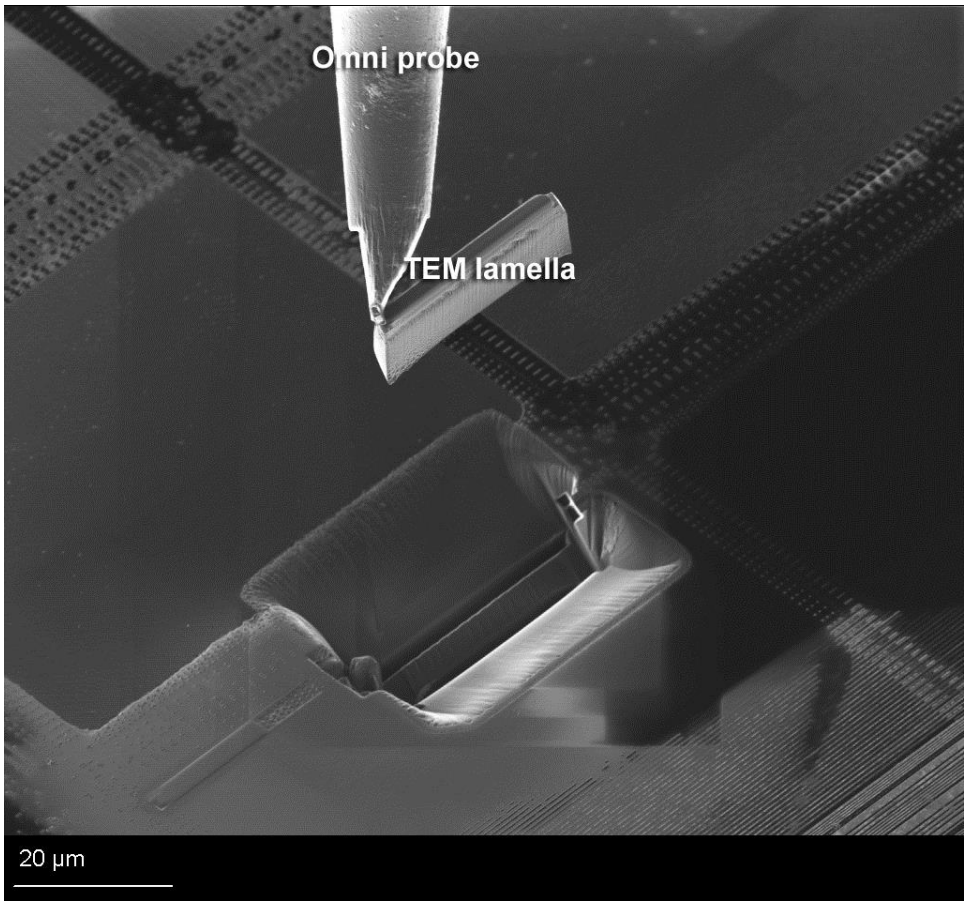

Figure 10-13 TEM sample attached to the probe and cut out of the surface.

- Moving the sample with probe to copper grid and inserting it in a prepared groove on the grid. Cutting probe from the sample and fixing the sample to the grid. Figure 10-14 shows sample fixed on a copper grid.

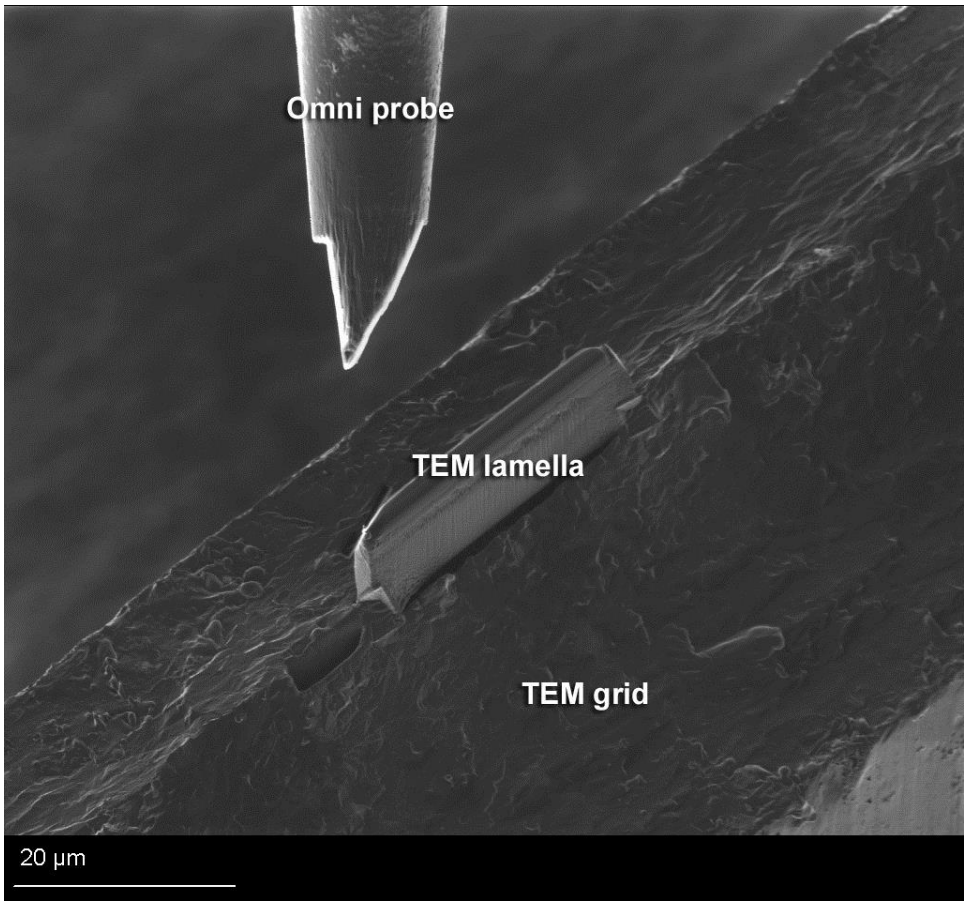

Figure 10-14 TEM sample is fitted into a groove on TEM grid and probe is cut from the sample.

- Thinning sample from front and back side using ion beam down to its final thickness proper for TEM analysis. At this point sample is approximately only between 20 to 40 nm thick.

Once sample is thin and fixed on the grid, it is ready for imaging and other analysis in TEM.

10.4 TEM Images and EDS Line Scans

We mentioned sample preparations were done on two different samples for studying their high-k dielectric layers composition and physical dimensions. For all of these studies, beam and TEM parameters were optimized to achieve highest possible resolution in imaging and EDS line scans. Analysis were done using two different types of TEMs mentioned before.

Figure 10-15 shows bright field scanning transmission electron microscopic (BF STEM) image of overall transistor structure and upper metal layers for the first sample and figure 10-16 shows higher magnification High-Angle Annular Dark-Field scanning transmission electron microscopic (HAADF STEM) image of PMOS gate indicating location of high-k dielectrics layer in this device.

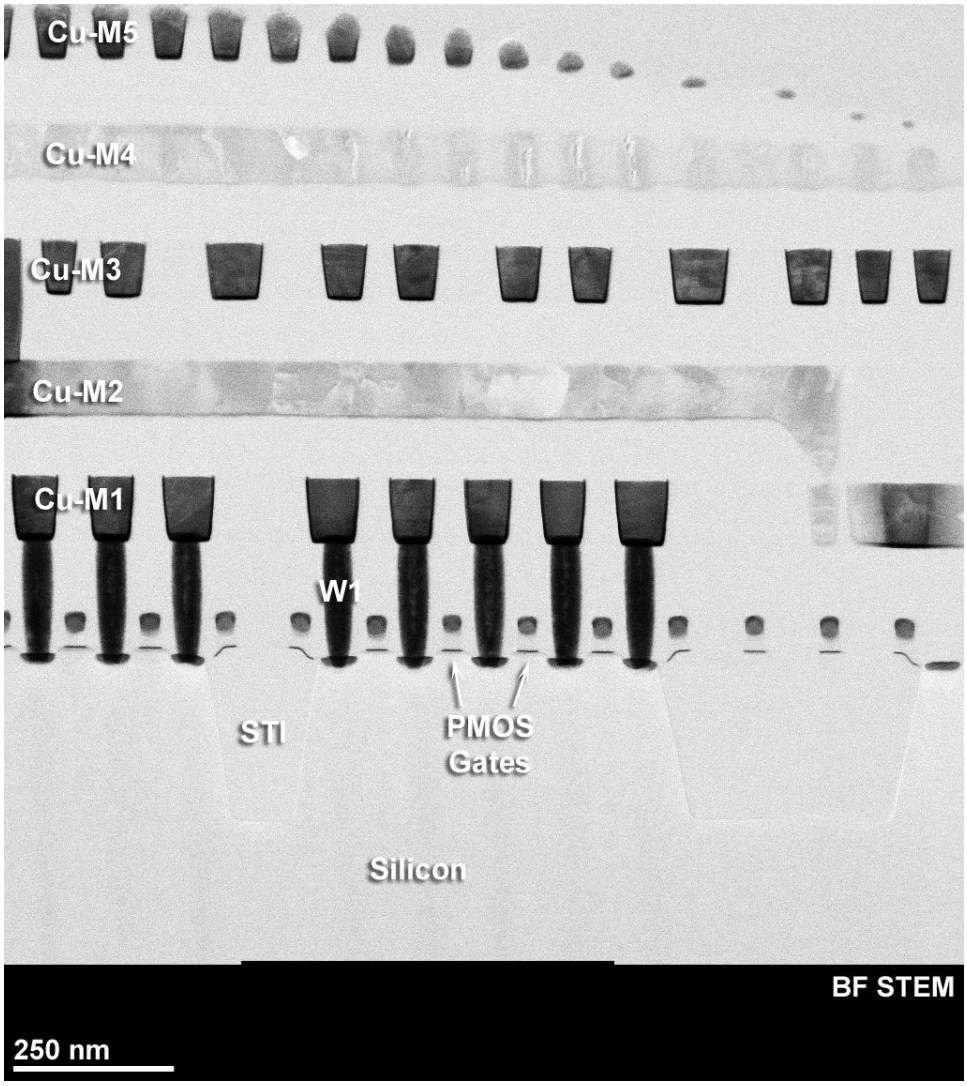

Figure 10-15 Bright field STEM image of PMOS gates and upper metal and dielectric layers.

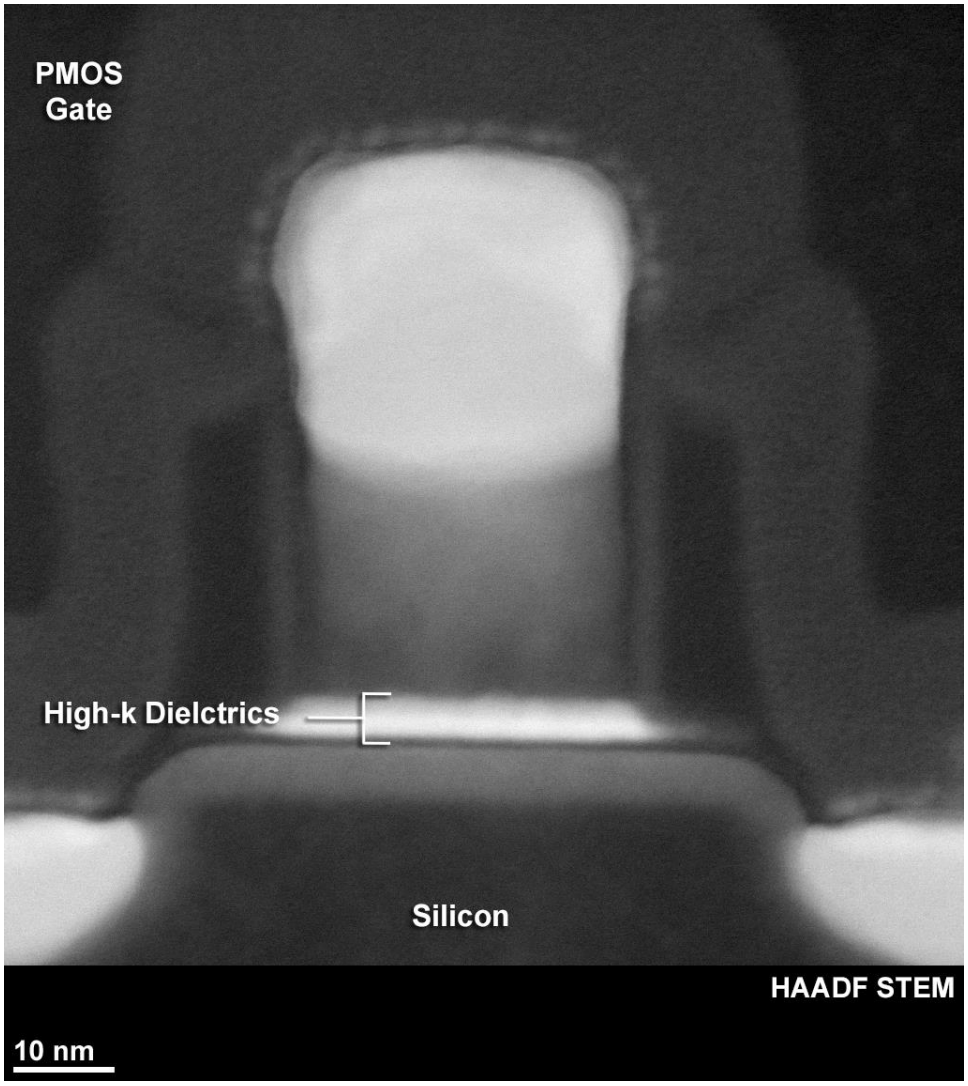

Figure 10-16 High magnification HAADF STEM image of PMOS gate in sample one. Image shows the location of high-k dielectrics layer.

Figure 10-17 shows ultra-high magnification of high-k dielectric region. At this magnification, lattice planes are visible in crystalline regions of the sample. Compositions noted on the image are results of EDS line scans. Rotation in the image is inevitable as it is due to phase change of electron beam induced by magnetic lenses as results their current change caused by zooming process.

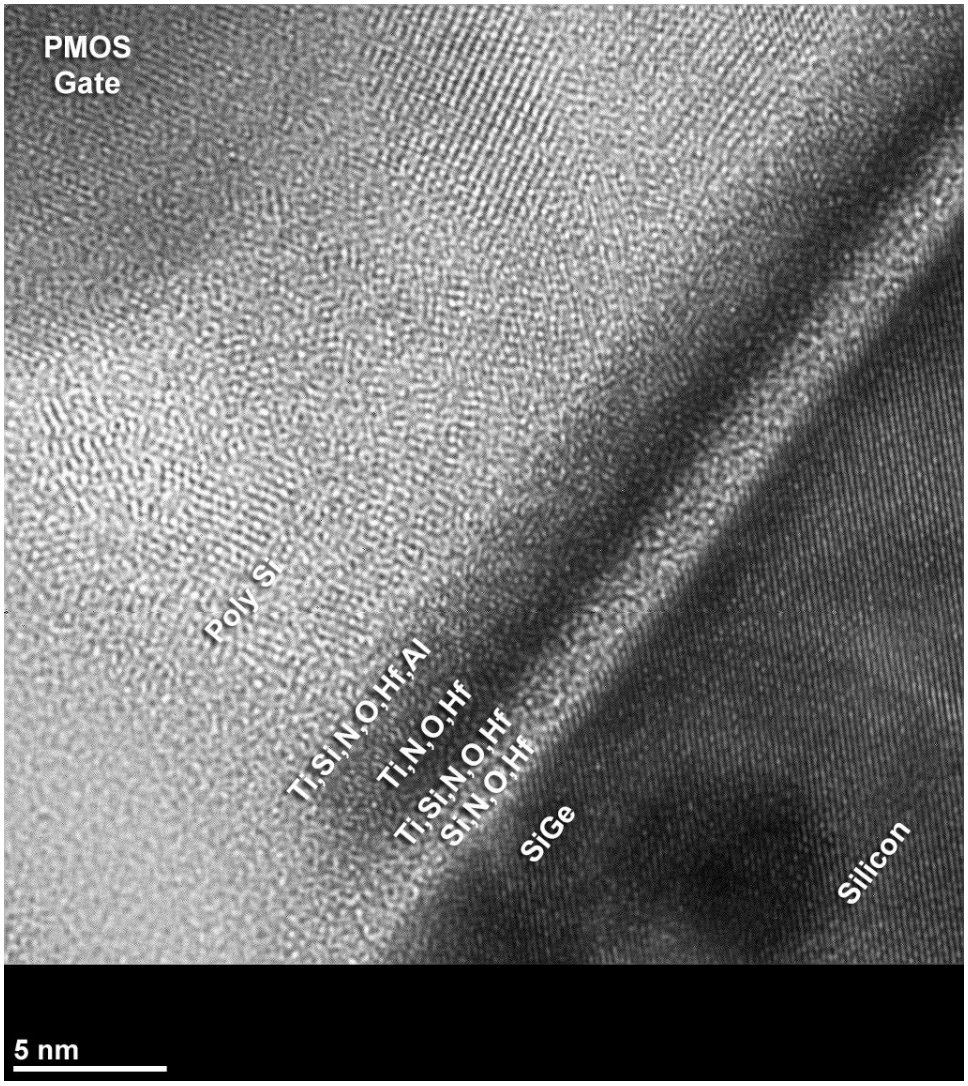

Figure 10-17 Ultra-high magnification of high-k dielectric region in a PMOS gate of sample 1. Compositions are obtained by EDS line scans.

Figure 10-18 shows lower magnification bright field scanning transmission electron microscopic image of NMOS transistor overall structure in second sample together with upper metal and dielectric layers and figure 10-19 shows HAADF STEM image of NMOS gate at higher magnification indicating location of high-k dielectric region.

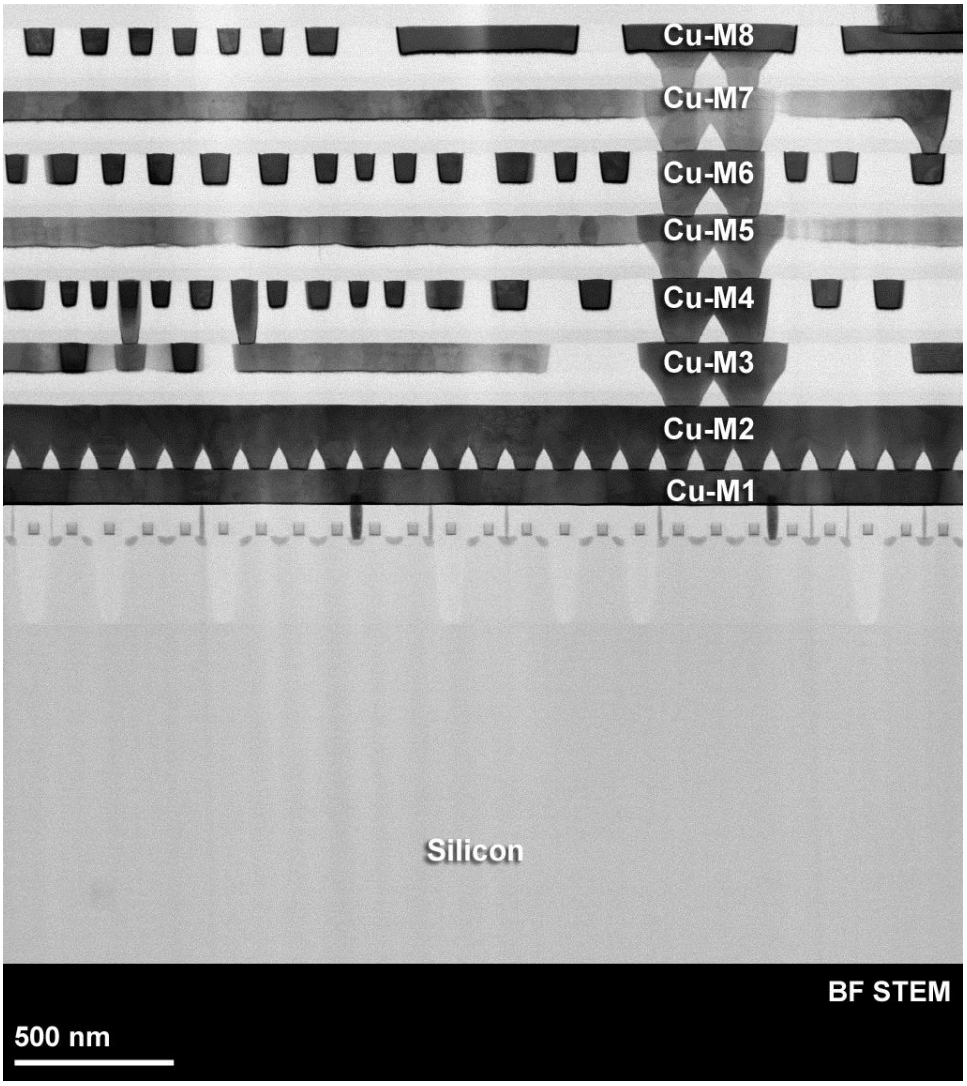

Figure 10-18 BF STEM image of NMOS gates and upper metal and dielectric layers.

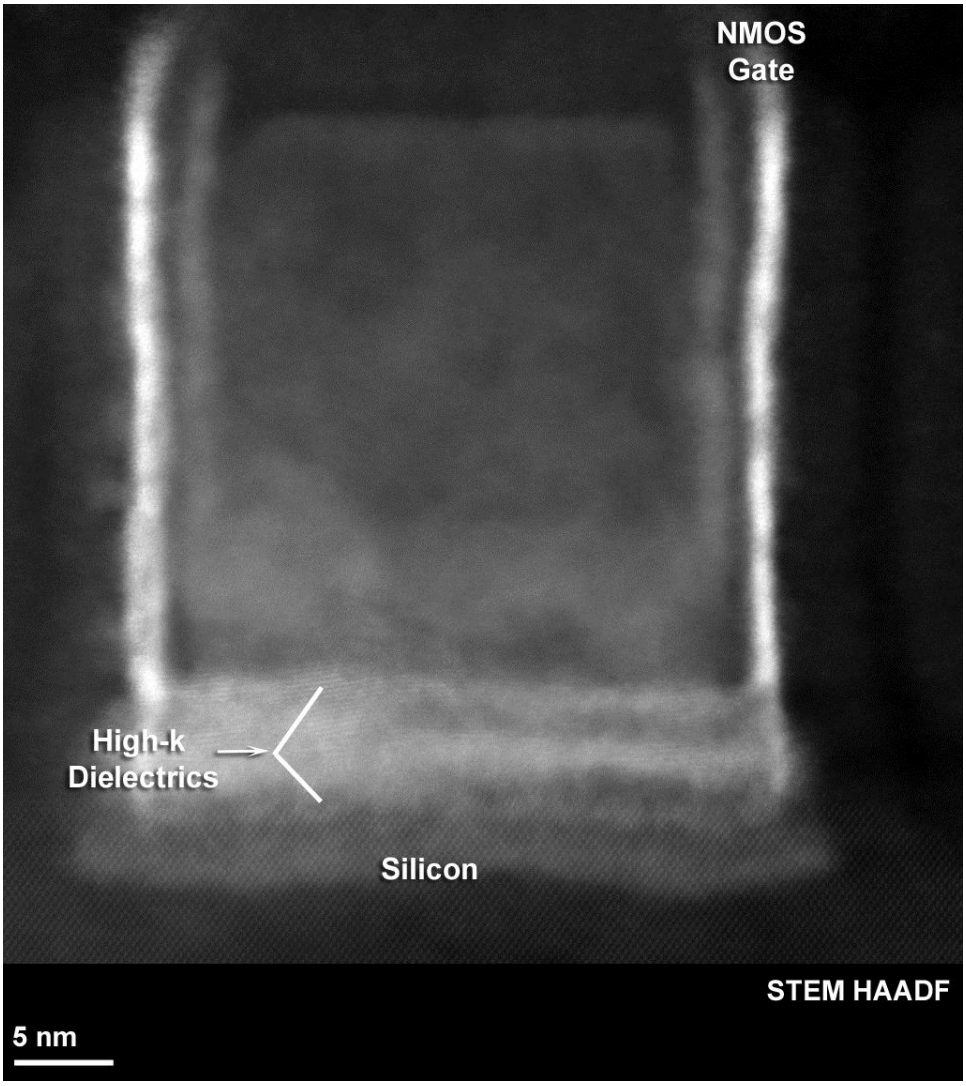

Figure 10-19 High magnification HAADF STEM image of NMOS gate in sample 2. Image shows the location of high-k dielectrics layer.

Figure 10-20 shows ultra-high magnification of high-k dielectric region for second sample in an NMOS gate. Compositions indicated on image are obtained from EDS line scans.

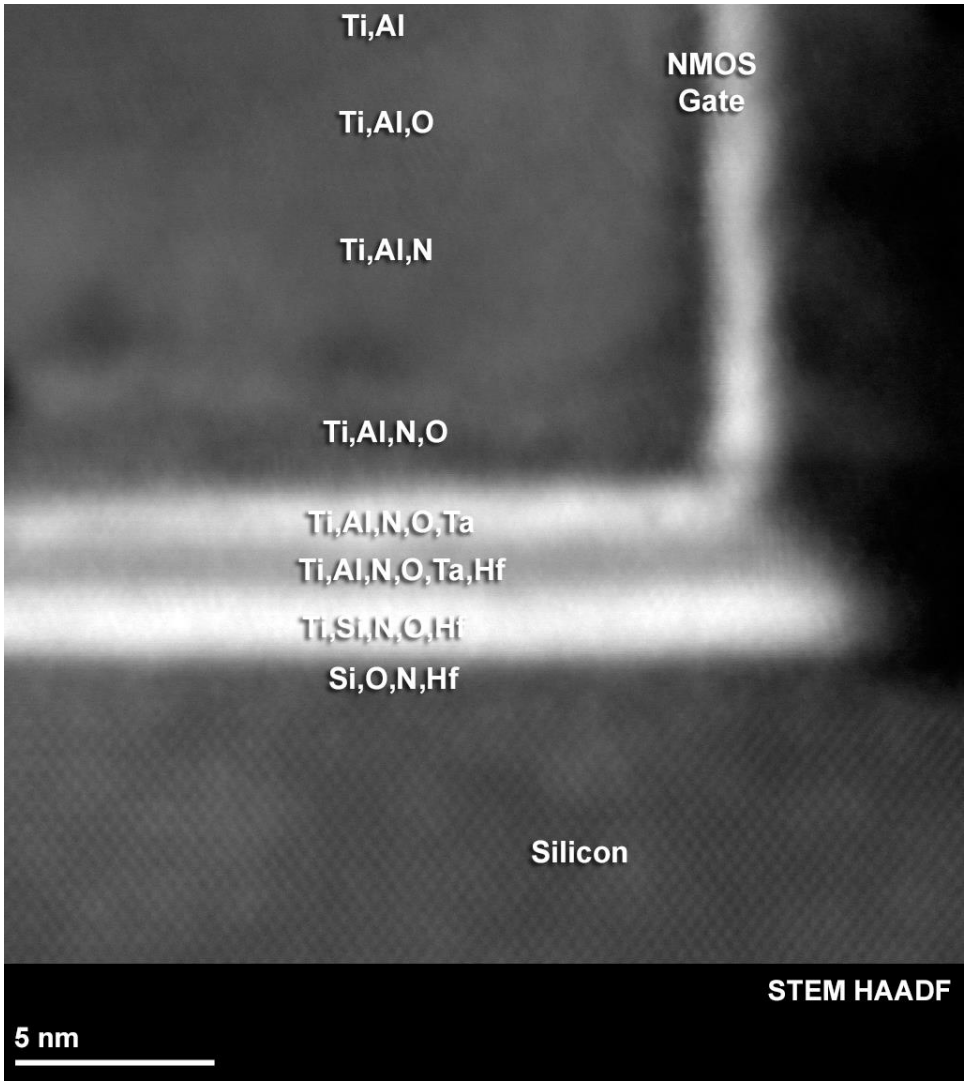

Figure 10-20 Ultra-high magnification of high-k dielectric region in a NMOS gate of sample 2. Compositions are obtained by EDS line scans.

For chemical composition analysis, EDS line scans were obtained across high-k dielectric region of gate structures in these two samples. Figures 10-21 and 10-22 show these line scans with corresponding scan regions marked in TEM image.

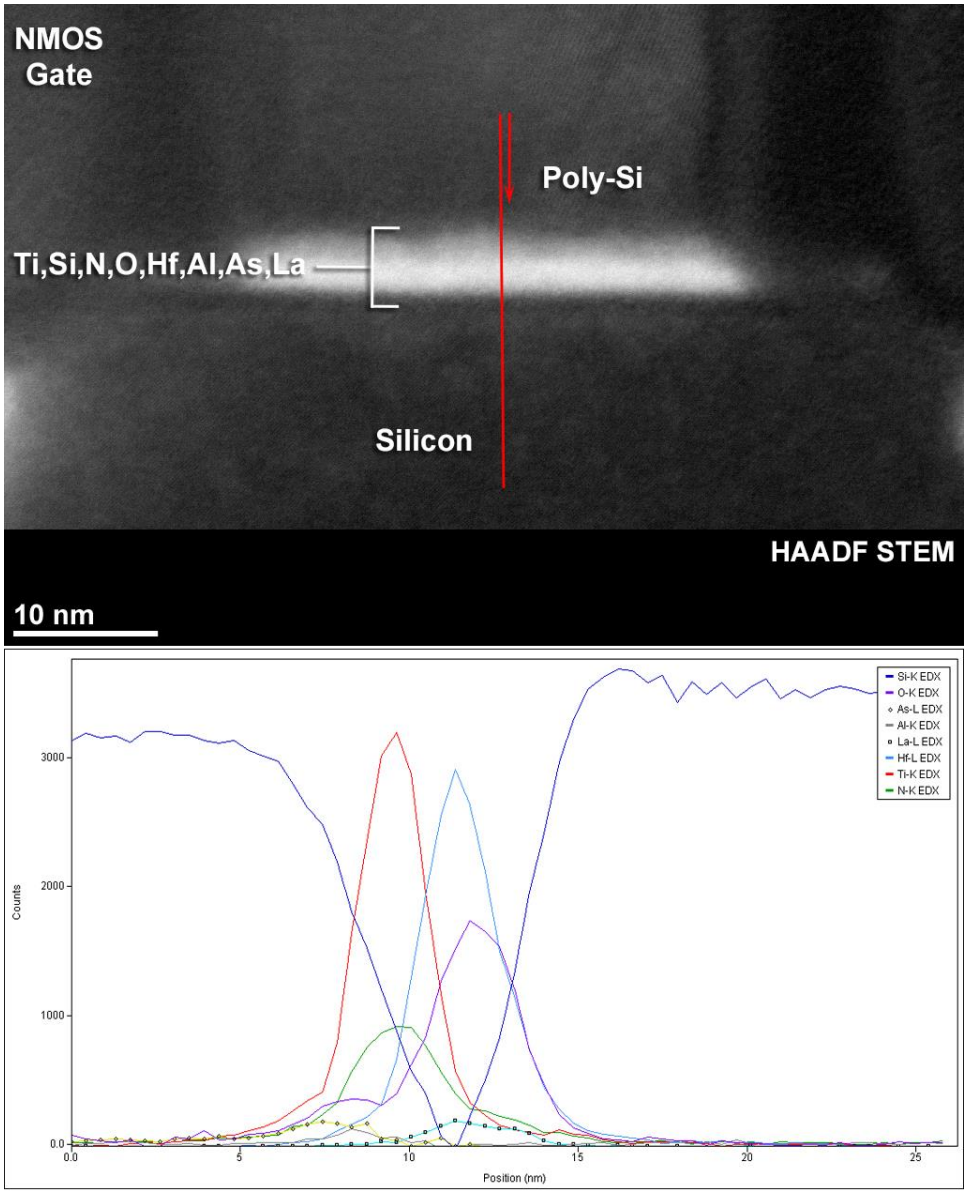

Figure 10-21 EDS line scan across high-k dielectric region on the NMOS gate in sample 1.

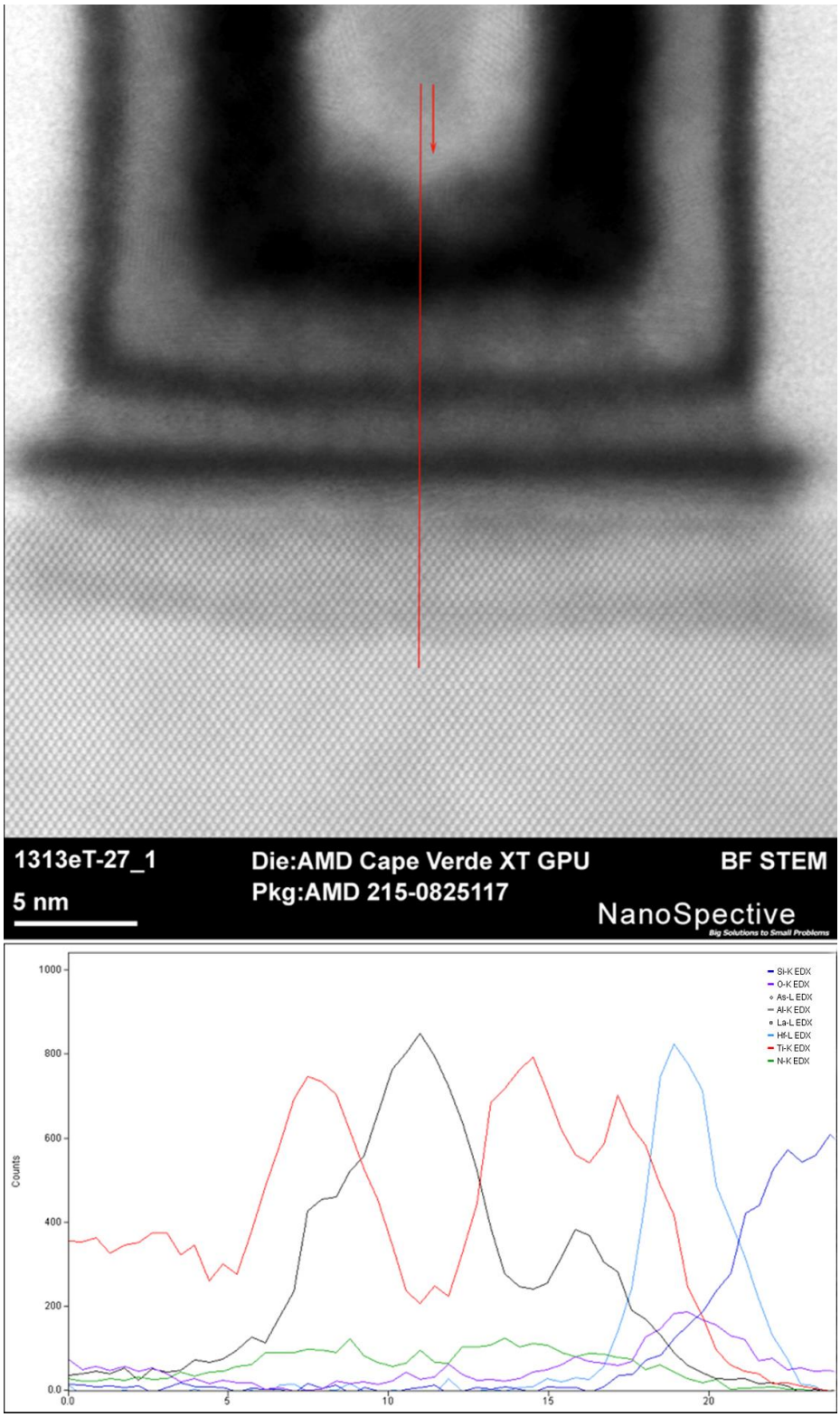

Figure 10-22 EDS line scan across high-k dielectric region in sample 2.

10.5 EDS Line Scans Simulation and Comparison with Experiment

Experimental line scans smooth transition from one layer to another suggest high probability of atomic diffusion in between these layers. However, to confirm this hypothesis we used Monte Carlo simulations to obtain EDS line scans of high-k dielectric layers with compositions seen in experiments. For these simulations we assumed sharp non-diffused interfaces between these layers and used exact same beam parameters used in experiments to simulate possible low-resolution artifacts too. Results are presented in figures 10-23 for first sample and 10-24 for second sample.

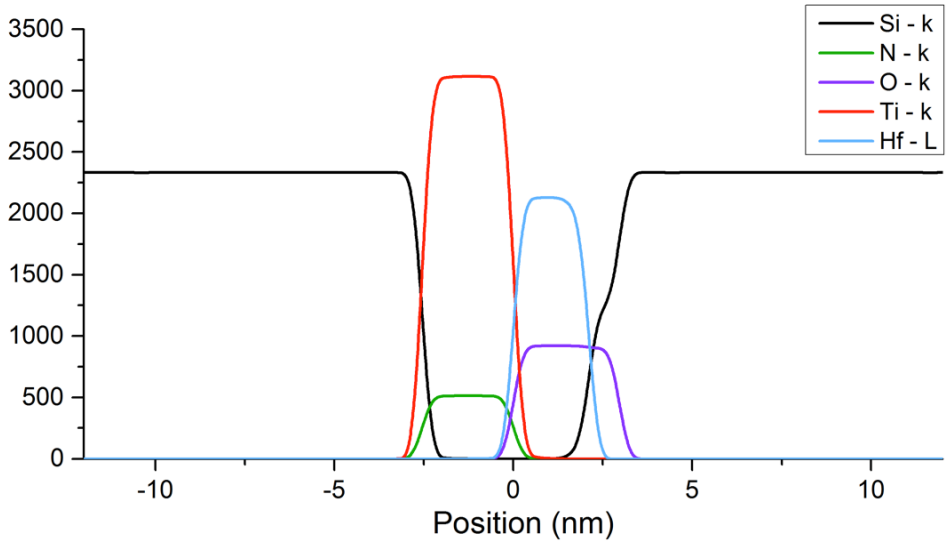

Figure 10-23 EDS line scan simulation for first sample. Beam and scan parameters were chosen same as experiments.

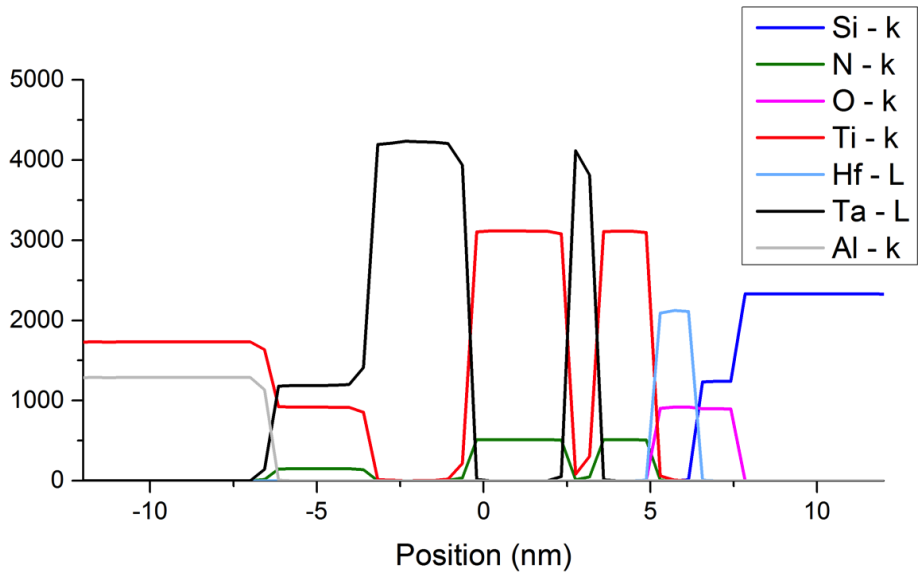

Figure 10-24 EDS line scan simulation for second sample. Beam and scan parameters were chosen same as experiments.

As can be seen in these images, lack of resolution creates artifacts that resemble diffusion in simulations even though simulated samples were designed with sharp interfaces. However, side by side comparison of simulation results with experimental line scans shown in figures 10-21 for first sample and 10-22 for second sample indicates much higher extent of diffusion-like effect in experimental line scans. Based on these results we can conclude that real diffusion is present in between high-k dielectric layers of these two samples which is a signature of possible heat treatments during fabrication of these two devices.

CHAPTER 11 CONCLUSION

A novel MEMS IR detector is presented based on optimization of patented design in [15]. Important factors in device functionality are explained and original design is described with three parallel plates. Lower most plate is buried under the surface of substrate held at negative bias, middle plate is fixed on the surface and is held at positive bias and top plate is a free to move cantilever above the surface and is held at same potential as middle plate. Cantilever vibrates by applications of saw-tooth bias between the plates that creates a repulsive electrostatic force on it, for each time cantilever's tip touches the surface a signal is detected by an external circuit. Device respond to heat absorption by changing touching time constant due to difference in thermal expansion coefficient of bilayer of materials used in arms holding the cantilever. Thermal bending, time constant and thermomechanical noise are studied theoretically.

Claimed electrostatic behavior is studied using semi analytical techniques. Total electrostatic force on cantilever is derived as function of coefficients of capacitance and inductance. A hand waving argument is presented based on dimensional analysis of these coefficients to confirm repulsive force on the cantilever. For more accurate study, their behavior as function of cantilever vertical position is studied. It is proven that electrostatic repulsive force can be applied on top plate using such design.

Device is simulated using finite element modeling technique. Fundamentals of finite element modeling are explained as well as software packages used for these simulations. Electrostatic field distribution is calculated around three plates and its behavior with change in vertical displacement of cantilever is demonstrated. Total

electrostatic force on cantilever is calculated using field values over the surface and it is shown when surface plate length is 95% or larger than cantilever total force is positive and it peaks when this ratio is about 105%. Calculations of total force vs. vertical displacement shows that after a certain height total force will be negative. Calculations are done to show the relation between max force and vertical height and it is concluded that force maximum is dropped and shifted toward higher length ratios of surface plate to cantilever as vertical height is increased. This shows the need for optimization of size ratio for each specific application with different vertical displacement requirements.

Device design is optimized based on modeling and it is fabricated using MEMS fabrication techniques in three different prototypes of single large 100 μm, single medium 50 μm and 3 × 3 array of small 20 μm pitch for pixels. Fabrications steps for device are explained. Experiments are done to enhance the release of cantilever from sacrificial layer. A method based on exposure of sacrificial layer to UV light to accelerate the release is developed and its effect on wet and dry chemical etching speed is shown. Device contact and sensing pads fabrications are described.

A technique based on observation of interference fringes between semitransparent cantilever and reflective substrate is developed to quantify cantilever curvature and relative height. Same technique is applied for stress measurements on semitransparent structures based on Stony formulism. A LabVIEW application is developed to automatically develop stress and curvature maps by receiving an input from microscope camera.

Experiments are done to prove presence of upward motion as result of electrostatic repulsion. A LabVIEW application is developed to simultaneously capture device motion,

sense tip contact signal and control applied bias. Pixels motion is captured by video microscopy while bias between plates is increased. In some, stress due to force is enough to break pixels from the anchor and in some unreleased pixels, lifting them off cause air bubble to penetrate into polyimide sacrificial layer underneath the plate. Thin and semi-transparent layers of cantilever let interference fringes be visible. The change in the fringe pattern as the cantilever lifts is a means for quantizing cantilever displacement. This techniques is used to describe plate upward motion as a function of applied bias between plates. Such repulsive force in MEMS device make high impact factor possible and has application in many MEMS devices such as IR detection, switches, and micromirrors.

In the second part of this work ultra-thin high-k gate dielectric layers in two 22 nm technology node semiconductor devices were studied for the possible presence of diffusion in between the layers. The efficacy of STEM, EDS and EELS as methods for this investigation is evaluated. The necessity for high resolution STEM imaging and EDS line profiles to observe interdiffusion in the layers is emphasized. Possible sources of experimental error are identified and safeguards are proposed.

Analytical calculations are done to predict the expected lateral spatial resolution for the tools and parameters used in the experiments and to understand the potential factors that might limit the ability to distinguish interdiffusion from artifact under the proposed conditions. The experiment was performed on two FEG TEMs. One instrument was an XFEG with Cs correction in the probe-forming lens and the other was a standard uncorrected TEM. Because beam spreading is highly material dependent, the lateral spatial

resolution for the various materials in high-k dielectric layer stack were calculated to range from 2.4 Å to 10 Å.

Monte Carlo simulations of incident electron trajectory and X-ray generation volume were done to more accurately predict the effect of and sample and instrument parameters the limits of lateral spatial resolution for STEM imaging and EDS microanalysis of a series of ultra-thin layers. The fundamentals of Monte Carlo simulations and the software packages used are explained briefly. The effect that the incident beam diameter has on lateral spatial resolution is studied by comparing transmitted electrons intensity as a focused electron probe is stepped across the atomically sharp simulated interfaces of Si and SiO_2 layers. It is shown that a beam diameter that is too large with respect to the feature of interest will cause an apparent broadening of the line profile across the interface. This effect is an artifact created by the selected STEM parameters that will mimic the appearance of a line profile across an interface where the two materials have interdiffused. The two conditions are not distinguishable from the TEM data. This underscores the necessity to carefully evaluate the features of interest and plan your experimental parameters prior to starting the analysis. A similar set of calculations was performed using the same set of modeled interfaces. This time the probe size was sufficiently small but a series of line profiles were modeled where the step size between sequential EDS spectrum acquisitions was varied. It was observed that too large of a step size meaning too few sampling points across the interface produced an apparent broadening across the interface similar to that which was observed for the excessively large probe size. It was determined that a probe size and step size should be selected to allow no fewer than

three discrete sampling points within a layer. Additionally, it was observed that the elemental profiles of a multilayered thin film stack could appear erroneously skewed if the position of the probe steps across the interfaces was asymmetric with respect to the interfaces. Because this falls more on the side of random error it is recommended that line profiles are acquired in multiplicity to ensure repeatability. The effect that specimen thickness exerts on lateral spatial resolution was also modeled. The expected result was observed that lateral spatial resolution is improved with decreased specimen thickness. However, a thinner specimen will produce far fewer X-ray counts because there are a lower number of interactions. This causes a deterioration of the signal to noise ratio in EDS line profiles, hence an optimum target specimen thickness has to be chosen to maximize the benefits from each of the competing factors.

The high-k gate dielectric layers are analyzed experimentally on two different 22 nm node semiconductor devices. The thin film stacks are the same as those modeled analytically. The samples are prepared using series of required steps including polishing, optical and IR microscopy, wet and dry chemical and plasma etching, scanning electron microscopy and focused ion beam. All sample preparation methods are described in detail in the text. Upper metal layers, gates and high-k dielectric layers are imaged by two TEMs using BF STEM and HAADF STEM modes with the optimized beam parameters. EDS line profiles are obtained for compositional analysis of these layers.

By comparing the simulation results with the empirical data, it was concluded that the broadened elemental line profiles observed in the actual results could be attributed to interdiffusion between the high-k gate dielectric layers and is not an artifact of improper

sampling. The simulations were performed on corresponding layer stacks with atomically sharp interfaces and the results are compared with the experiments. The results confirm that the interfaces appear much sharper in the simulations than experiments for the same parameters. This result suggests diffusion in the high-k gate dielectric layers of the studied samples. The results presented in this work are significant for any application where high-resolution, high-quality elemental profiles across multiple interfaces are required. These results are actively used when planning AEM experiments and evaluating experimental data for the nanoscale characterization of partially or fully processed commercialized semiconductor devices including ICs, photonic and MEMS. Reliable characterization methods are essential for the development of new technologies and this work is used to support the industries that design and manufacture semiconductor devices.

APPENDIX: PUBLICATIONS

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6. Patterning of oxide-hardened gold black by photolithography and metal lift-off, Deep Panjwani, Imen Rezadad et al., Infrared Physics & Technology 62, pp. 94-99 (2014).
7. Repulsive electrostatic force in MEMS Cantilever IR Sensors, Imen Rezadad et al., Proc. SPIE Vol. 9070-57 (2014).

8. Thermomechanical characterization in a radiant energy imager using null switching, Javaneh Boroumand, Imen Rezadad et al. Proc. SPIE Vol. 9070-125 (2014).
9. Stress Analysis of Free-standing Silicon Oxide Films Using Optical Interference, Imen Rezadad et al. Proc. MRS Vol. 1536, pp. 155-160 (2013).
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