Study of Reliability Evaluation Technology using DRAM Sensor with Planar MOS Capacitor for 3D Integrated System

氏　　名	たにかわ　せいや 谷　川　星　野
研究科，専攻の名称	東北大学大学院工学研究科（博士課程）バイオロボティクス専攻
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論 文 審 査 委 員	主査　東北大学教授　田中　徹　　東北大学教授　湯上　浩雄 東北大学教授　三浦　英生　東北大学教授　田中　秀治 東北大学准教授　福島　誉史

論文内容要約

Three-dimensional integrated circuits (3D-ICs) have several advantages such as small interconnect length, high-speed operation, and parallel processing. The 3D-IC stacks thinned IC chips to be electrically connected by a through silicon via (TSV) and metal bumps. A 2D-IC is formed on a plane in one chip. 3D-ICs have some significant advantages over conventional 2D-ICs. A 3D-IC realizes a connection of various chips at a small distance because the size of the TSV and the metal bump can be scaled down to less than 10 μm. However, various reliability issues occur since 3D-IC needs new processes for TSV formation.

First, IC chips are electrically and mechanically connected with metal bumps. An adhesive is injected between the stacked IC chips to improve the mechanical strength. Local bending stress is induced by organic adhesive shrinkage in stacked structure. The shrinkage of metal bumps is lower than that of organic adhesives such as the epoxy region. As the coefficient of thermal expansion (CTE) of an organic adhesive is generally larger than that of metal bumps, the volume of the organic adhesive decreases after the organic adhesive curing process induced by a curing reaction and cooling to room temperature. This volume shrinkage of the organic adhesive induces local bending strain in IC chips. In addition, as IC chips are generally thinned to less than 50 μm during the 3D stacking process and the flexural rigidity of the IC chips decreases depending on chip thickness, the thinned IC chips are largely bent due to the organic adhesive shrinkage. Local bending stress exhibits more severe effects on device reliability in 3D-ICs. Therefore, it is important to precisely understand the impact of local stress on device reliability for highly reliable 3D-ICs. However, analysis instruments for stress are not enough for these issues. For example, Raman spectroscopy can measure mechanical stress and crystal defect with a high resolution and in-plane distribution. The measurement takes long time depending on the exposure time and number of measuring points, and the measurement point is only the sample surface. In-plane distribution using a CMOS strain gauge also detects stress at high sensitivity. In addition, complicated stress in the Si substrate is divided into x, y, and z directions, but the cell size is very large because each cell includes some transistors.

Second, the 3D-IC consists of several vertically stacked IC chips thinned to 20–50 μm thickness with many TSVs. The silicon thinning process removes the intrinsic gettering (IG) regions for gettering the metal diffusion, and Cu atoms can rapidly diffuse into the dielectric layer and active region in the Si substrate. Moreover, the Si substrate is deeply etched using the Bosch process for a high-aspect-ratio via. Bosch process is repeated for anisotropic Si etching and passivation deposition. The cycle induces sidewall roughness called scallops. good coverage of the barrier layer on the scallop is difficult. Poor coverage induces the diffusion of Cu atoms during post-annealing. The scallops cause the Cu to easily diffuse from TSV in case of a poor coverage of via hole. These metals generate a deep energy level in the bandgap. These deep energy levels act as the generation and recombination of the carrier. This contamination causes the degradation of device performance and easy breakdown of the dielectric layer. Therefore, it is important to establish a 3D technology without metal contamination. An evaluation technology of the metal contamination is important to realize highly reliable 3D-ICs. However, analysis instrument for Cu contamination is also not enough for these issues. For example, secondary ion mass spectrometry (SIMS) or total reflection of X-ray fluorescence (TXRF) is conventionally used as an evaluation technology for Cu contamination. SIMS can perform mapping analysis and depth direction analysis. However, it is necessary to break a sample. A long time is required for mapping measurement, and quantitative analysis cannot be performed unless a standard sample. The Cu concentration is not measured to be less than 10^{16} atoms/cm^3 by SIMS. On the other hand, the Cu concentration on the back surface is also measured by TXRF. The Cu concentration reached 10^9 atoms/cm^2. TXRF can detect low Cu concentration in the Si substrate. However, the beam size was approximately 10 mm, and TXRF cannot be used for small size sample and concentration mapping.

Therefore, conventional evaluation technologies are not enough for deeply analysis and large area analysis. In this study, a new evaluation technology using DRAM sensor with planar MOS capacitors is proposed. The retention time of the DRAM sensor is affected by various phenomena such as stress or Cu contamination. The detection mechanism for Cu contamination and stress is

explained. In the experiments, it is proved that Cu contamination and stress can be detected using DRAM sensor with a planar MOS capacitor. The in-plane distribution in the Si substrate can be precisely evaluated. At first, the DRAM chip is fabricated. The DRAM is composed of the DRAM cell arrays, a sense amplifier, a controller, a row and column decoder, and an I/O circuit. There are DRAM cells at the intersections of bit line (BL) and word line (WL). 0-1 and 1-0 retention time is compared. 0-1 retention time shows a small variation among the DRAM cells and can be measured within a short time, while 0-1 retention time is suitable for in-plane distribution in a large area. Next, to clarify the mechanism for detecting Cu contamination and stress distribution, the retention between retention time and current paths in DRAM cell is shown.

It has been qualitatively explained that the retention time changes when mechanical stress are applied to DRAM. However, to use planar MOS capacitors as a stress sensor, it is necessary to quantitatively associate the stress with the retention time. To classify the stress detection mechanism, the planar MOS capacitors is bent by a four-point bending tool. The capacitance of the planar MOS capacitors dramatically increased due to applied compressive stress. At a strain of -0.04%, the maximum capacitance was found to be 122 pF. The maximum capacitance at -0.02% and -0.04% was up 10% and 30% compared to that at 0%. As the capacity increases, the time constant dramatically increases. Therefore, the planar MOS capacitors detects compressive stress. Next, the relation between the local stress and retention time shift is investigated. The test structures consisting of the DRAM flip-chip bonded on a Si interposer with dummy Cu/Sn bumps are successfully fabricated. The stress profiles are measured on the back Si surface after the organic adhesive curing, and the retention time shifts of the DRAM cell arrays before and after organic adhesive curing are measured. A comparison of the stress profile and in-plane distribution of retention time shift shows that the compressive stress increases the retention time, whereas the tensile stress decrease the retention time. As a result, the 2D mapping of the retention time clearly indicates the in-plane local stress distribution. It is also successfully clarified that the local stress affects the electrical characteristics of the device in thinned IC chips. In addition, in-plane distribution of retention time shift gradually changes depending on the shorting bump pitch. The large shift in the retention time is suppressed by fine-pitch bumps. Therefore, bump pitch shorting decreases stress in Si substrate.

On the other hand, the generation lifetime depends on the impurity in the Si substrates. It is well known that C-t measurement using planar MOS capacitors is an effective technology to determine the generation lifetime. The DRAM sensor can detect ionic metallic contaminations by shifts of the generation lifetime. Generation lifetime depends on the level of impurity in the Si substrate. Cu contamination in 3D-IC is evaluated by shifts of the generation lifetime. Next, fabricated test structure with Cu deposition on the back surfaces of thin Si chips, and observed that the retention time decreased by annealing and the retention time gradually decreased depending on the annealing temperatures. Thus, the DRAM sensor can detect Cu contamination even though Cu diffuses into Si substrates under low-temperature annealing at 200 °C. In addition, to induce Cu diffusion from TSV, the sample with many TSVs is measured under various annealing temperatures. The retention time shift clearly degraded at space distances of 3, 5, and 10 μm. Therefore, under 200 °C annealing, a 20-μm distance from the TSV is necessary to avoid Cu contamination, while a 40-μm distance from the Cu-TSV is necessary to avoid Cu contamination. Using my evaluation technology, the optimized guidelines for the 3D-IC can be developed, and various 3D-ICs can be realized with high performance and reliability.

At last, evaluation results from the DRAM sensor is used for 3D stacked retinal prosthesis. The 3D integration technology can stack multifunctional IC chips, and thus, enlarge the circuit size. The advantages of a retinal prosthesis chip are useful in realizing high-resolution, multifunction, and small-size ICs. However, residual stress in a multilayer photodetector causes large bending in 3D stacked process flow. The removal of the outer adhesive process and the press process are added to the 3D integration process. These new processes restrict the bending of the chip. In addition, the bump pitch of the photodetector chip and the annealing processes are adjusted by the evaluation results of Cu contamination and stress by the DRAM sensor. Moreover, the new fabrication process exchanges formic acid reflow with Ar etching, and the bonding condition was adjusted at 250 °C. These changes reduced Cu diffusion from TSV. Performance of 3D stacked retinal prosthesis is improved. It is confirmed that the output frequency varies with the incident light intensity. A circle image is focused on the front surface of the photodetector chip. The area of the circle image is consistent with dark color pixels, while that of bright light is consistent with bright color pixels. Moreover, the output image is changed to a dark color, but the edge of the circle image remains due to the edge enhancement function, reducing the power consumption by 18%. For this reason, 3D stacked retinal prosthesis is shown to be operating appropriately.