Research on Highly Efficient and Highly Integrated DC-DC Converters Using Vertical Body Channel MOS Field-Effect Transistor and its Power Management for Microprocessors

Doctoral Thesis

Thesis Title

Research on Highly Efficient and Highly Integrated DC-DC Converters Using Vertical Body Channel MOS Field-Effect Transistor and its Power Management for Microprocessors

(縦型ボディチャネル MOS Field-Effect Transistor を用いた
マイクロプロセッサ向け高効率・高集積 DC-DC コンバータと
そのパワーマネジメントに関する研究)

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ABSTRACT:

In recent years, our life style has been transformed by the utilization of computer platforms, and from now on by the emerging technologies such as Internet of Things (IoT) and cloud data centers. According to the spread of the use of computer platforms, the power consumption of the computers has become an emergent issue for environmental sustainability. For microprocessors, the operation voltage is lowering to suppress the power consumption while keeping its performance, and then the current consumption of microprocessors has been risen accordingly. In addition, power-saving techniques have been intensively developed for microprocessors such as dynamic power gating (PG) which cuts off the stand-by power by shutting down the supply voltage. These trends in microprocessors cast difficult issues on DC-DC converters, which are widely adopted as power supply of microprocessors. The first issue is regarded to the power management. In order to adapt to load current which frequently varies from heavy to light load and vice versa, conventional power management techniques are inadequate to supply voltage stably because of the inaccuracy of current sensing circuits and so on. The second issue is that highly efficient and highly integrated DC-DC converter is required for power saving. Conventional planar MOS Field Effect Transistor (FET) based CMOS DC-DC converters have large conduction loss mainly generated at the PMOS high-side power switches, consequently large transistor area is required.

In this thesis, novel power management circuits techniques of current sensing, current digitalization, and switching control are presented to meet the requirements of future microprocessor power supplies. Moreover, highly efficient and highly integrated CMOS DC-DC converters using vertical Body Channel (BC) MOSFET and its efficient transistor layouts are proposed and evaluated using experimentally extracted models of BSIM4 60 nm vertical BC MOSFETs.

In chapter 3, a novel current sensing method which achieves highly accurate and low-loss is proposed. In the proposed method, additional bypass switch is utilized to suppress the conduction loss in the sensing resistor. From a numerical analysis using typical parameters of current sensors, it is found that designing sampling duty cycle small has importance because it effects on the equivalent resistance and accuracy in the proposed method. The analytical result revealed that the proposed method with 0.10 sampling duty cycle is able to obtain 47% higher accuracy with an approximately equivalent conduction loss in compared with the conventional DCR sensing. Furthermore, the prototype of the current sensing circuit is built on the 12 V to 1.0 V, 20 A synchronous buck DC-DC converter which is digitally controlled by FPGA. By using the prototype, the proposed method is demonstrated that it can output the current sensing circuit with a good linearity within a load range throughout full load range 0 A to 20 A, and the measured LSB was 33.8 LSB/A which is +3.3% from the ideal value.

In chapter 4, it is found that the conduction loss in MOSFET at near the boundary current reaches

98% of loss at the maximum load from the result of the loss of MOSFET under adaptive driving control, hence the temperature increase causes a serious issue. In order to suppress the temperature increase, a novel switch toggling technique is presented and evaluated. It is verified that in case that three MOSFETs are connected in parallel, temperature increase of high-side and low-side MOSFETs are suppressed 64% and 59% when one module is driven, and 32% and 27% when two modules are driven respectively.

In chapter 5, a novel inductor current to digital converter (ICDC) is proposed to decrease the required number of components for power management. The proposed ICDC features a new operation principle which converts DC and ripple component of inductor current to digital data separately and simultaneously with small number of components, which was difficult for conventional ADCs. From the circuit simulation results with 12 V to 1 V DC-DC converter, it is successfully shown that the proposed converter can digitalize the 10 A DC component with 5 A ripple component. Input range of DC and ripple component are 0 A to 14.4 A and 4 A to 6 A, respectively, with 65 mA maximum quantization error.

Chapter 6 presents a highly efficient CMOS DC-DC converter circuit using constructed by vertical BC MOSFETs with a cascode power stage including a high-side (HS) NMOS cascode switch and its driver circuit. From the simulation results regarding to the on-state performance as a HS cascode power switch, it is clarified that the proposed n-channel vertical BC MOSFETs based HS cascode power switch has high current drivability, which is +85% superior to the conventional planar p-channel MOSFET based one. The proposed and conventional converters with the same operation conditions of 100 MHz switching frequency, 3.3 V input and 1.2 V output voltage, and load current up to 2.5 A are evaluated under identical transistor size. The peak efficiency of the proposed converter was +3% higher than the conventional one.

In chapter 7, in order to realize cascode CMOS DC-DC converters with improved efficiency and compactness, a novel transistor layout of multi-pillar type vertical BC MOSFET is presented. In the proposed layout, the metal and gate layer have a stacked and multi-fingered pattern. Instead of connecting via bottom contacts, the drain and the source are connected on the diffusion region of the multi-pillar type vertical BC MOSFETs. CMOS DC-DC converters with the proposed layout are evaluated for HS-PMOS and HS-NMOS topologies with experimentally extracted transistor models of 60 nm technology vertical BC MOSFETs. The results indicated that the peak efficiency became approximately 90% under the conditions of f_{SW} = 100 MHz, V_{IN} = 2.0 V, and V_{OUT} = 0.8 V. The efficiency improvements are 5.4% and 6.0% compared to the converters using the conventional layout for HS-PMOS and HS-NMOS configurations respectively, simultaneously suppressing the sum of power transistor area by 16%.

From the above all, it is concluded that the proposed power management circuits with improved performances are suitable for power supply of future microprocessors. Moreover, it is also verified that the proposed CMOS DC-DC converter using vertical BC MOSFETs are highly efficient and compact compared to the conventional one. Therefore, the proposed converter is a promising candidate for future microprocessor power conversion. Finding from results of this research will greatly contribute in the power electronics and semiconductor technologies for DC-DC converters.

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Chapter 1

Introduction

1.1. Increasing Importance of Green Power Electronics

In order to realize sustainable society for future development of the human race, more strategic energy utilization is indispensable. Greenhouse gas (e.g. carbon dioxide) generated by electricity generation gradually increases the average temperature of the earth and it will cause seriously harms ecosystem [1]. To tackle this problem, Japan decided to take the leadership and reduce the carbon dioxide emission of by 80% by 2050 in the Forth Basic Environmental Plan. Figure 1.1 shows the Japanese objective of the reduction of the carbon dioxide emission. To achieve the 80% reduction, the innovative energy efficiency will be important. In the energy utilization of modern society, the portion of computer platforms in the whole energy consumption is becoming large by the spreading use of computers, and it is discussed in Section 1.2 in detail.

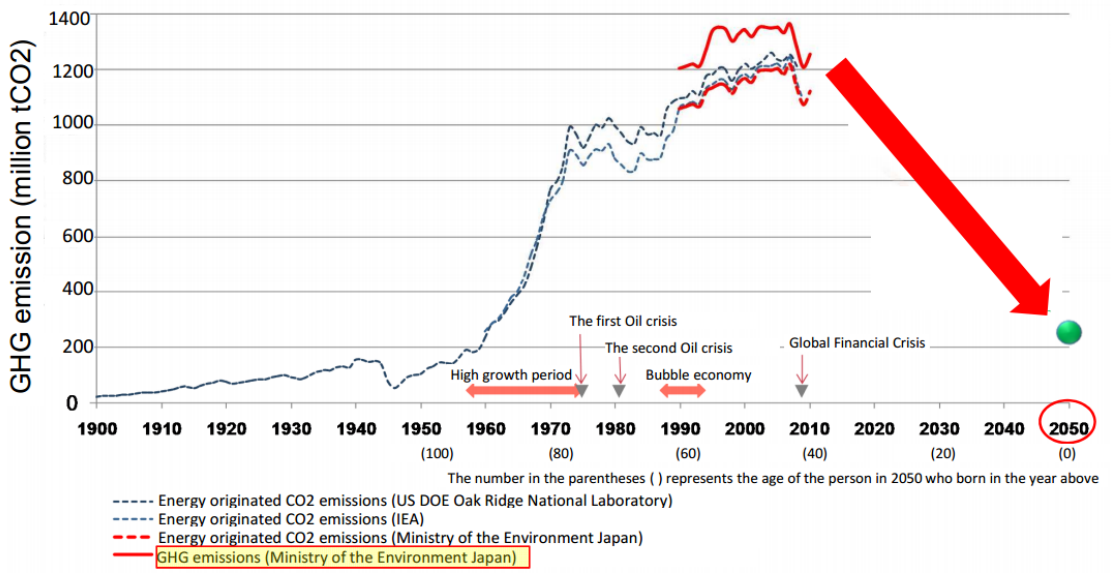


Figure 1.1. Japan's greenhouse gas emission trends and the long term goal [1].

To prevent this global warming, the energy utilization is rapidly shifting from primary energies such as fuel cell to the electric energies because the usage of electricity emits less greenhouse gas compared to fuel cells. For example, the energy utilization in vehicles are rapidly changing from gasoline to electricity. Britain has decided that they will ban the gasoline vehicles by 2040 [2]. Despite the increase of the amount of electricity generation is one of the possible ways, actually there is no shortcut. A nuclear power generation emits less greenhouse gas; however, it has proven that the nuclear power generation has a serious risk of radioactive contamination to ecosystems in Fukushima Daiichi nuclear disaster during the aftermath of the 2011 Tohoku earthy quake and tsunami. Natural energy such as solar photo-voltaic power generation and wind power generation is clean but the amount of the power is still small to replace the fuel cells and its supply is unstable because it is affected by atmospheric conditions. Therefore, smart electricity utilization is necessary in this age.

There are two principal technologies to achieve smart power utilization: power electronics and green electronics. Green electronics reduces the power consumption in Large Scale Integration (LSI) by applying vertical structured Complementary Metal Oxide Semiconductor (CMOS) devices and Spintronics devices such as Magnetic Transfer Junctions (MTJs). Developing the green electronics, we can keep prosperity keeping prospering brought by the information society. On the other hands, power electronics is engineering filed which deals power conversion by using semiconductor devices [3]. High to low voltage power conversion performed at the point of load suppress the loss in wiring in power delivery path from the power plant. The roles of green and power electronics for future society are shown in Fig. 1.2 [4]. In terms of the demand of the energy saving, both green electronics and power electronics will play important roles, and they will be harmonized in order to integrate power and green functions into next generation infrastructures.

In regard to power electronics, it is also expected as a promising market. Figure 1.3 shows the market prediction [5]. The power electronics market will rapidly grow by the needs of lower energy consumption in many markets such as automotive, industrial, consumer electronics. From the above, development of power electronics is not only necessary for future energy utilization but also will be highly impactful for economic growth. From the above, the importance of power electronics will be significant for our future delightful life.

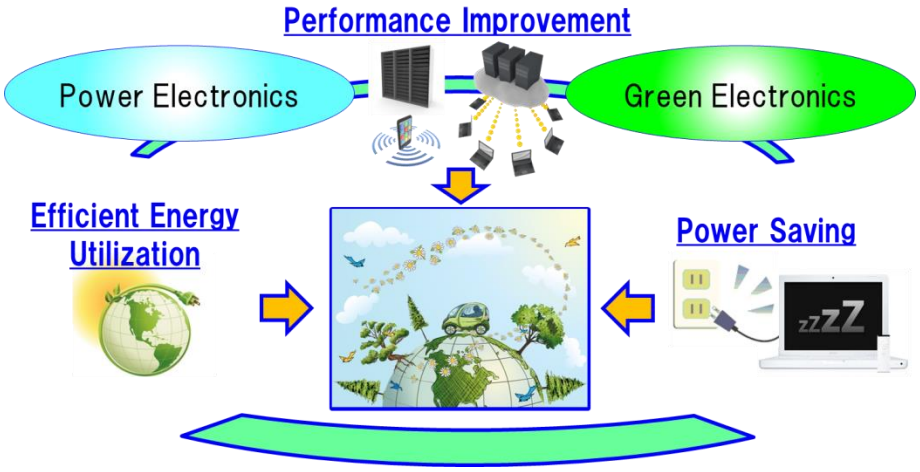


Figure 1.2. Role expected for green power electronics to realize future energy saving society [4].

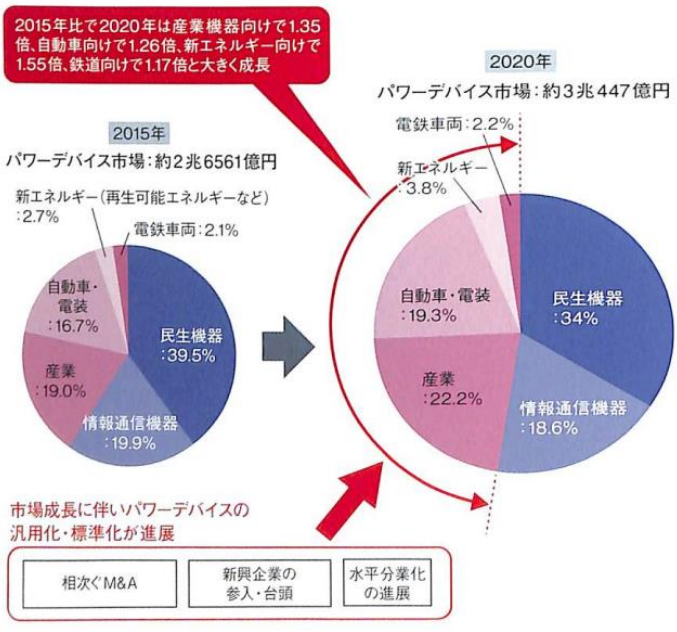


Figure 1.3. Growth forecast for the power device market [5].

1.2. Energy Consumption of IT Equipment

In 1946, IBM has developed Electronics Numerical Integrator And Calculator (ENIAC) for the first computer to calculate trajectories of missiles. Then, Jack Kilby invented the first integrated circuit (IC) in 1958. The number of transistor in one IC chip is exponentially increased exponentially according to Moore's law advocated in 1965. With the growth of performance of IC technology, the utilization of the information technology which is made up of plenty of semiconductor devices has spread to our life. Nowadays, computers are used as personal computers, servers, and smartphones and they play an important role for major communication tool in today's information society. With the spreading of the computers, the energy consumption has been increased.

This drastic change will not only continue but also be accelerated because there are some emerging technologies. Kevin Ashton presented a concept of Internet of Things (IoT) which is a system which connects not human to human but things to things [6]. Figure 1.4 illustrates expected future applications of IoT and AI technologies [7]. Trillions of sensors with tiny edge processing terminals will send huge amount of data to cloud data centers, hence the real world information will be more and more utilized in Internet. AI is expected to judge something or support people in many situations in many application areas such as autonomous driving, robot, finance, and so on. AI makes decision using big data integrated at a cloud data center. In near future, AI will be applied not only virtual world but also the real world by the using the big data from sensor networks. Therefore, the power consumption of cloud data centers, network infrastructures, and IoT edge device might increase significantly for next few decades.

From the perspective of the future computer utilization, Artificial Intelligence (AI), and big data based on cloud data centers, the power consumption in computers is an emergent issue for the sustainability. Figure 1.5 shows the prediction of energy consumption of data centers in Japan. Ministry of Economy, Trade and Industry in Japan predicts that the traffic on the Internet will be 190 times by 2025, and the power consumption will be 12 times by 2050 compared to that of 2006 in Japan [8]. Therefore, the Japanese government regards power saving of computers as a very important field, and Ministry of Economy, Trade and Industry vigorously promotes Green IT project to solve this problem.

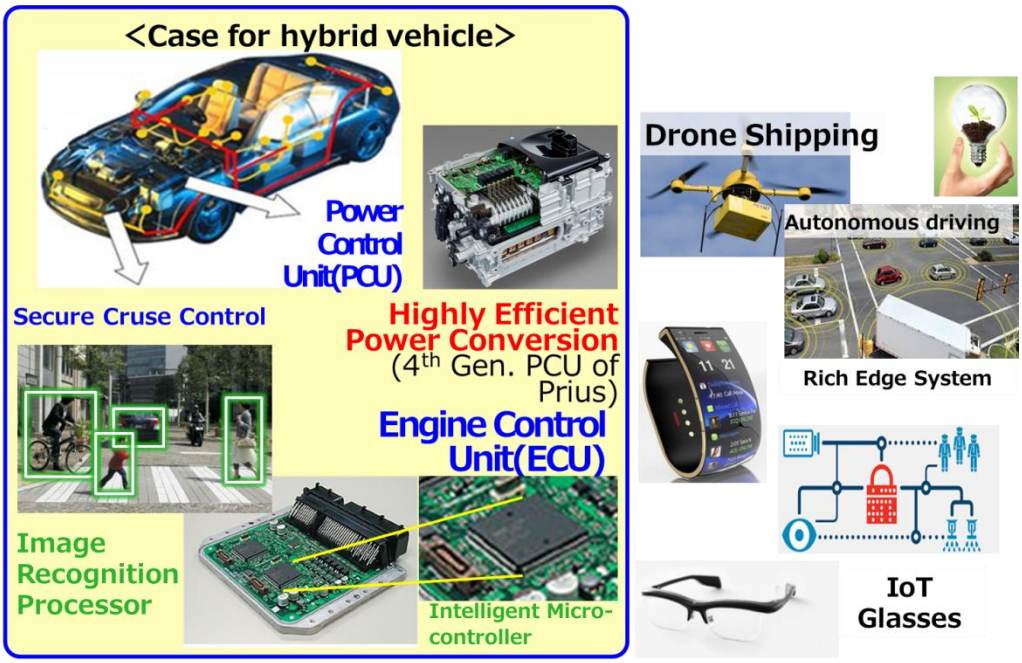


Figure 1.4. Expected future applications of IoT and AI technologies which are enabled by green power electronics [7].

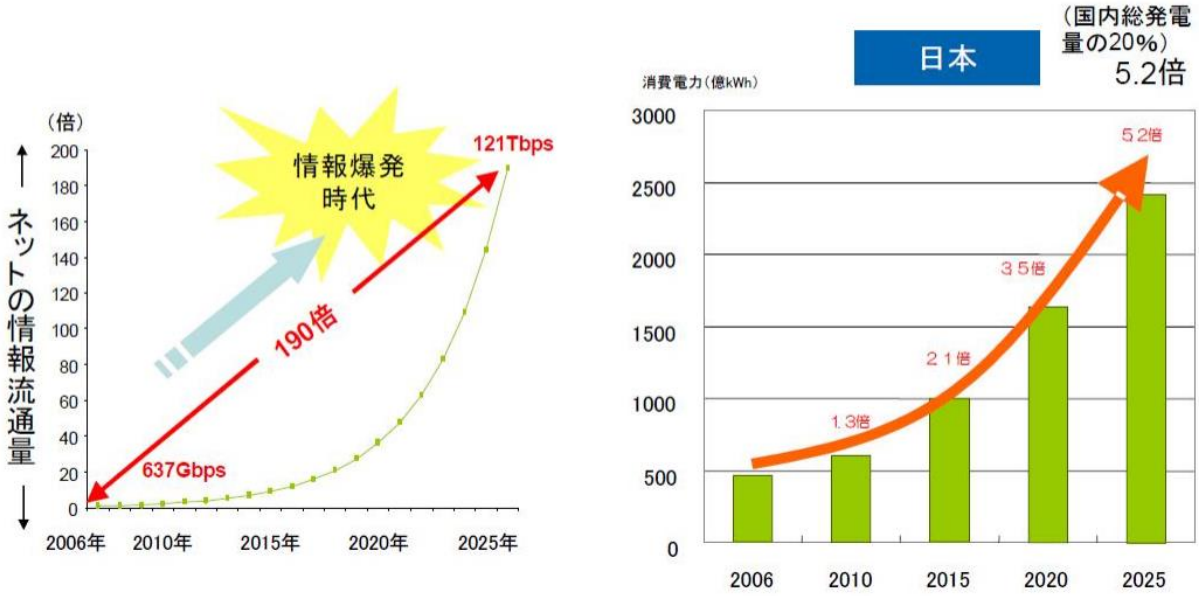


Figure 1.5. Predictions of national traffic of information and total amount of power consumption of IT equipment in Japan [8].

1.3. Power Conversion inside IT Equipment

In most case, the high-voltage AC power is input to the computer, and the energy is consumed as low voltage DC power in microprocessors, memories, chip sets, fans, and so on. From the AC supply to the loads, several power conversions such as AC-DC, DC-DC is needed. The block diagram of the power delivery system of data center servers is shown in Fig. 1.6 for example [9]. The power supply system is ordinary composed of two lines for redundancy. In first, commercial AC power is input to the Uninterpretable Power Supply (UPS). The output of UPS is distributed to each server rack via Power Distribution Units (PDUs). Then, 208 Vac or 120 Vac power is supplied to the servers. In the servers, AC-DC and DC-DC conversions are carried out in the Power Supply Unit (PSU) as shown in Fig. 1.7. PSU outputs medium bus voltage normally 12 V, and it is converted to smaller DC voltage such as 5 V, 3.3 V, 1.2V appropriate for each load component by DC-DC converters. Finally, microprocessors, memories, and other components consume energy supplied by the DC-DC converters.

Energy utilization in computers is classified into two types: power consumption consumed by ICs and losses in the process of power conversion and power distribution. The loss dissipated in the process of energy conversion occupies a large portion in the whole energy consumption of the computers. Figure 1.8 shows energy breakdown of a server [10]. The energy conversion dissipates approximately 35% of whole power in a computer system; consequently the ratio of the energy consumed for data processing becomes small. The heat due to the loss also increases the required volume of bulky heat sinks because the heat generated by the loss damages electric devices and shortens product life time. Hence, conversion efficiency must be improved by developing power electronic technologies for the future.

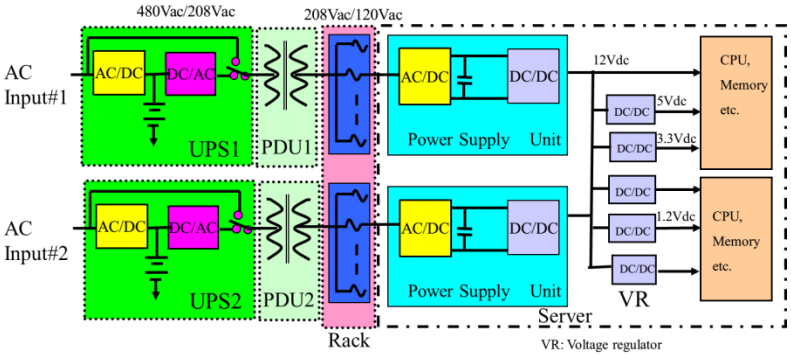
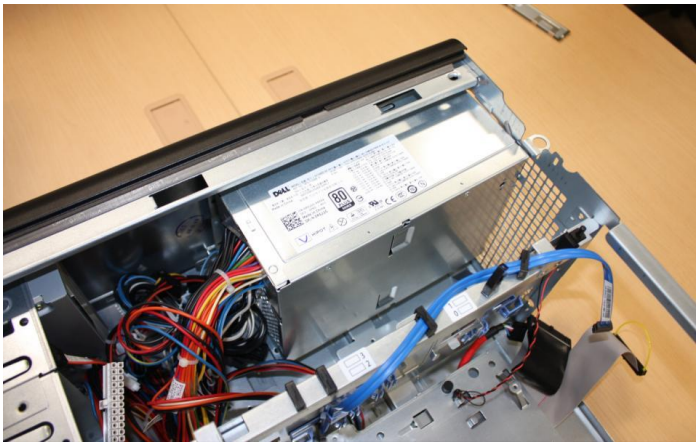
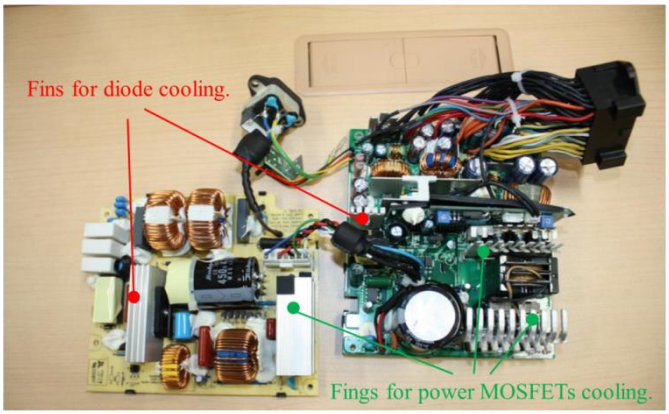


Figure 1.6. System block diagram of the power delivery network in a server [9].



(a) Case photo of a power supply unit.



(b) Power conversion circuit photo of a power supply unit.

Figure 1.7. Photos of a Power Supply Unit (PSU)

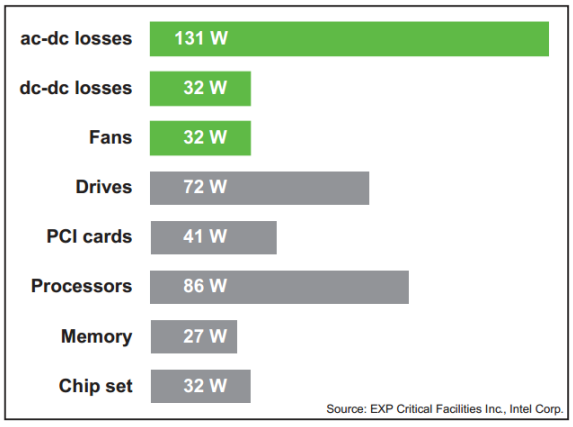


Figure 1.8. Energy breakdown including IC power consumption and loss in server [10].

1.4. Microprocessor Trends and Associated DC-DC Converter Requirements

Following Moore's law, microprocessors have increased its performance and number of transistor. Fig. 1.9 shows a die photo of state-of-the-art commercial microprocessor [11] and Fig. 1.10 shows 40 years of microprocessor trend data [12]. The number of transistors in a microprocessor reaches approximately 10^7. From 1970 to 2005, typical power dissipated in a microprocessor has grown exponentially. However, since 2010, the growth has slowed down. This is because current microprocessors suffer from performance limitations due to the heat generation exceeding package heat dissipation performance despite remaining room for realizing performance improvement by introducing more energy in the current silicon integrated circuit technology.

The most basic way of microprocessor power saving is lowering operating voltage since the transistor power is highly dependent on its operating voltage. Fig. 1.11 shows the required operating voltage V_{DD} for future microprocessors [13] (IRDS). The active power of transistors can be expressed as CV^2, and the static power can be expressed as VI_{leak}. Lowering operating voltage keeping its performance increases required supply current of microprocessors. The usual supply current of microprocessors for desktop PCs or servers are 100 A - 200 A, hence DC-DC converter with large output current is necessary.

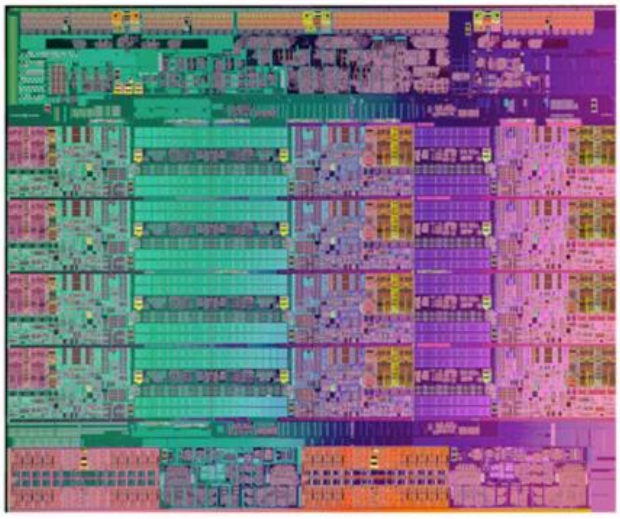


Figure 1.9. Die photo of state-of-the-art microprocessor [11].

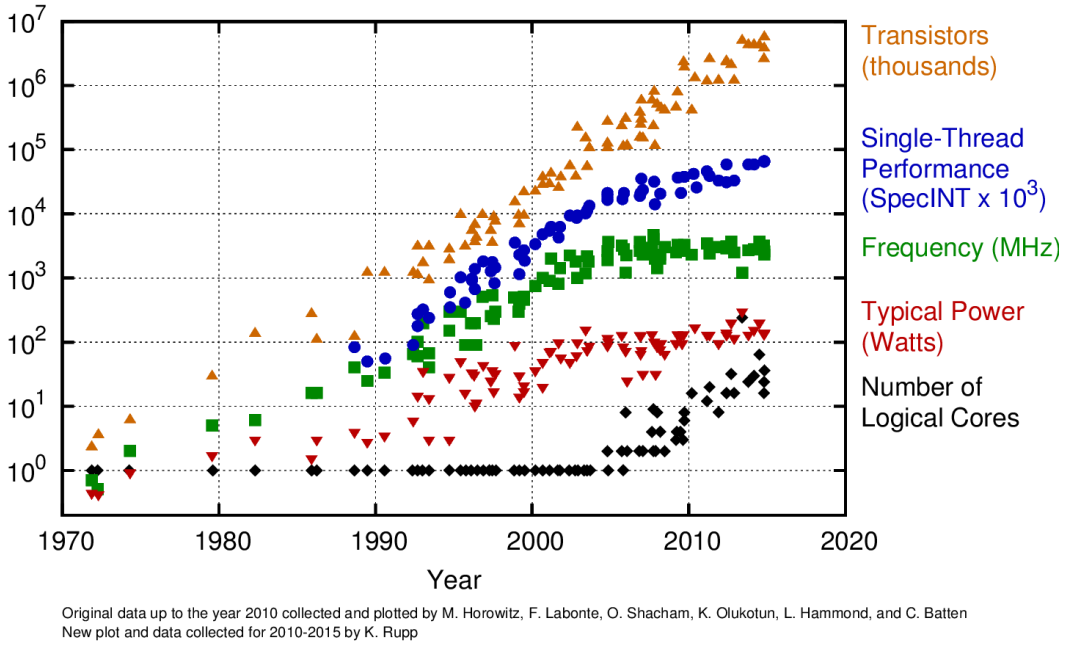


Figure 1.10. 40 years of microprocessor trend data [12].

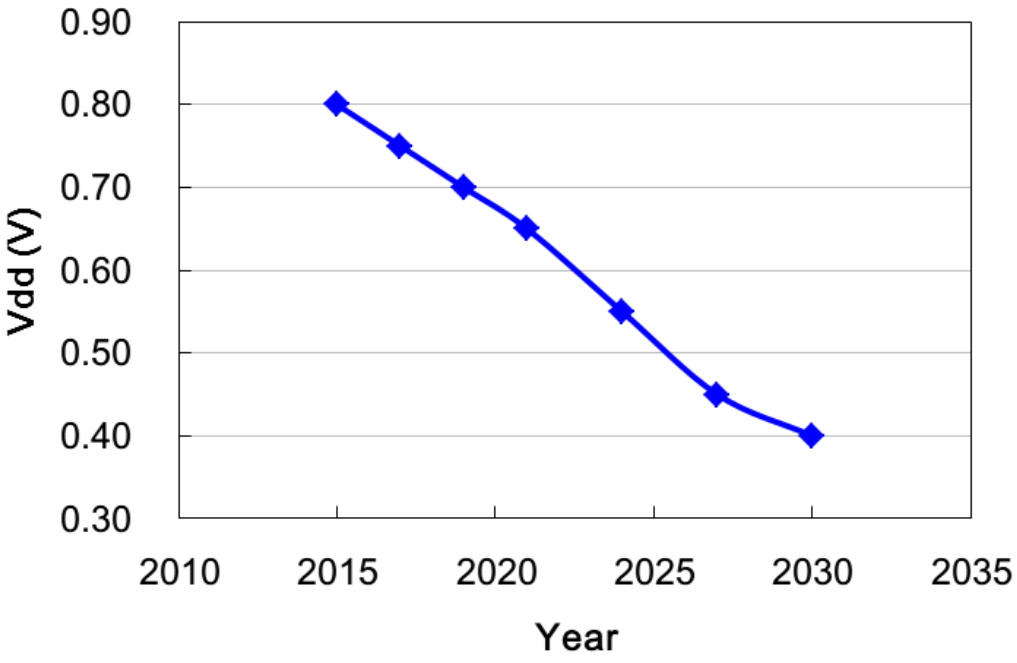


Figure 1.11. Roadmap of power supply voltage Vdd for logic circuits [13].

Another principal approach for power saving is the power gating which reduces static power by scaling voltage or scaling according to the computational load. The ultimate power gating technique is to absolutely shut down the supply voltage of microprocessors very frequently. In order to break through the limitation due to heat generation, a non-volatile logic circuit technology has been developed. Many world-renowned large companies such as TSMC, Global Foundries, UMC, Sam-sung, Intel, Qualcomm and others entry into development of NV logic circuit technology; therefore, this technology is the tide of the world. Thankfully for the pioneer's research and development, this technology is becoming a new platform for realizing an energy saving society. The non-volatile microprocessor unit (NV-MPU) which is shown in Fig. 1.12 uses conventional CMOS technology and Spintronics technology, and is expected as a promising candidate because they suppresses power consumption by shut down the supply voltage because NV elements such as Spin-Transfer-Torque Magnetic Random Access Memory are utilized as a cash memory [14]. Thus, the trade-off between heat dissipation and high-end computing, which is a bottleneck of existing silicon integrated circuit technology, is being solved. However, breakthrough due to a new framework associated with a nonvolatile microprocessor does not reduce power consumption as whole but accompanies a sudden change in power consumption. NV-MPU utilizes more current than conventional microprocessors, because a Magnetic Tunnel Junction (MTJ) which configures STT-MRAM writes data by current.

This technology trend in microprocessors causes serious issues in its power supply. The output current requirement of DC-DC converters will significantly increase, consequently the size of components will be bulky and the conduction loss expressed as RI^2 will be large. In addition, as its cost is strongly related to its footprint, high integrability is a very important point for practical applications. This is because the smaller the chip area, the larger the number of chips that can be manufactured from silicon wafers of the same size, and the higher the yield, thus manufacturing cost of the IC chip lowers according to the circuit density. Therefore, efficiency and compactness are very important criteria for DC-DC converters as a future microprocessor power supply. However, the conventional planar MOSFET based high-side PMOS type cascode DC-DC converter is inefficient and requires large transistor size due to the conduction loss.

Moreover, a power management technique will become all the more crucial because the power consumption of future microprocessors will changes more frequently

and massively from small to large or vice versa due to the power gating technologies. The issues for DC-DC converter power management for future microprocessors are illustrated in Fig. 1.13. Whether the power electronic circuit tuned to high power is high efficiency even at low power, it is not so. There is a sweet spot to the load in the power conversion efficiency of the power electronic circuit. In order to reduce the loss seen by users, future DC-DC converter must reduce power loss in a wide load range. Furthermore, it must have high responsiveness to the load. Even if we acknowledge the effect of innovation on low power consumption of IC based on non-volatilization, we cannot conduct social implementation because the technology value chain will not be established unless innovation of power supply circuit is also achieved. Therefore, DC-DC converters are required to control its output current and switching operation more precisely and flexibly adaptive to the wide range of output current.

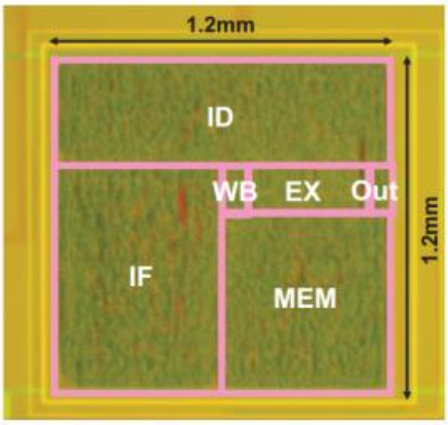


Figure 1.12. Die photo of Non-Volatile Micro-Processor Unit (NV-MPU) [14].

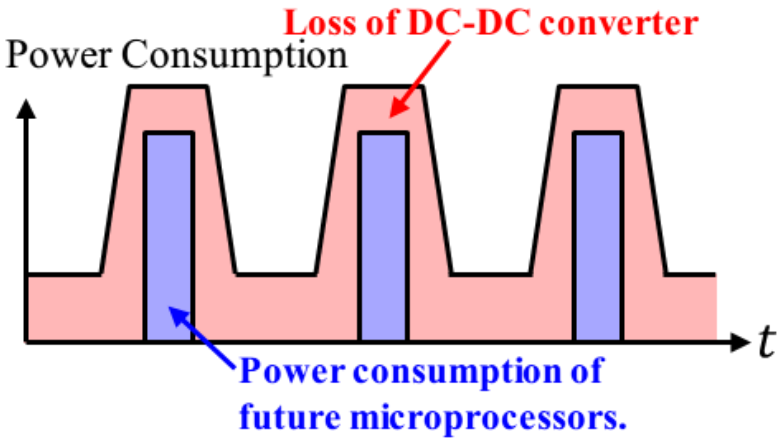


Figure 1.13. Issue regarding to loss of DC-DC converter for next generation microprocessor.

1.5. Objective of This Thesis

According to spread of the use of computer platforms, the power consumption of the computers has become an emergent issue for environmental sustainability. In the series of power supply to the microprocessors, this study addressed to the DC-DC converter for microprocessors as shown in Fig. 1.14. For microprocessors, the operation voltage is lowering to suppress the power consumption while keeping its performance, and then the current consumption of microprocessors has been risen accordingly. In addition, power-saving techniques have been intensively developed for microprocessors such as dynamic power gating which cuts off the stand-by power by shutting down the supply voltage. These trends in microprocessors cast difficult issues on DC-DC converters, which are widely adopted as power supply of microprocessors.

The motivation of this thesis is to provide a DC-DC converter that achieves high efficiency with both high power and low power that meets the needs of next generation microprocessors. Another motivation is to provide a power management circuit technology that copes with frequent load fluctuations of next generation microprocessors. Figure 1.15 shows the concept that this research aims. In order to supply power to future microprocessors including NV-MPU, power management circuit technology that senses the state of the motherboard DC - DC converter with high accuracy and feeds back to the microprocessor is required. Moreover, on the microprocessor die, it is required to realize DC-DC conversion from 2.0 V to 0.8 V with high efficiency and high integration using a vertical BC-MOSFET. This thesis aims to contribute to lower loss of DC power supply for microprocessor including future nonvolatile logic circuit by investigating the above technologies.

In this thesis, novel power management circuit techniques of current sensing, current digitalization, and switching control are presented to meet the requirements of future microprocessor power supplies. Moreover, highly efficient and highly integrated CMOS DC-DC converters using vertical Body Channel (BC) MOSFET and its efficient transistor layouts are proposed and evaluated using experimentally extracted models of BSIM4 60 nm vertical BC MOSFETs. It is described that these power management and efficiency enhancement techniques overcome the aforementioned issues of the DC-DC converters for microprocessors.

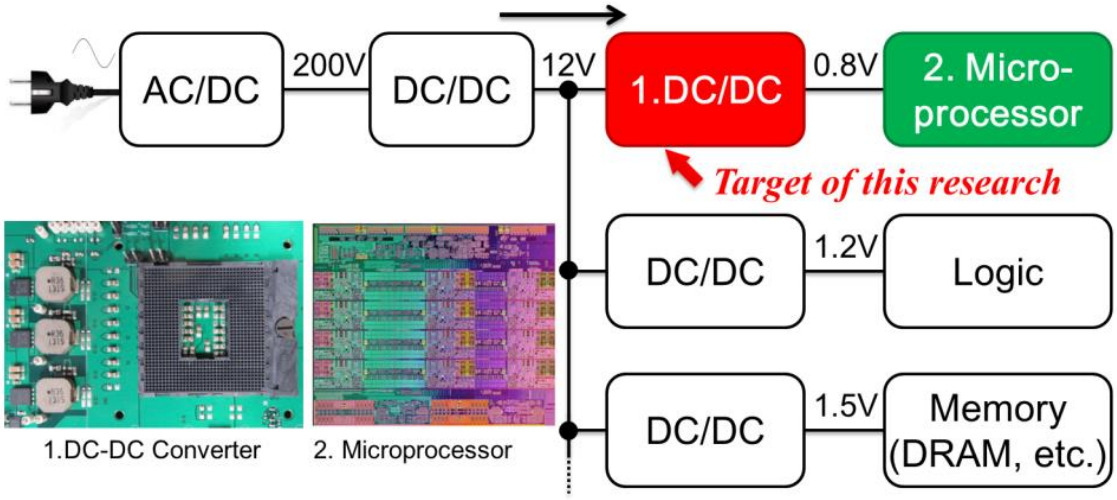


Figure 1.14. DC-DC converter for a microprocessor which is the target of this thesis.

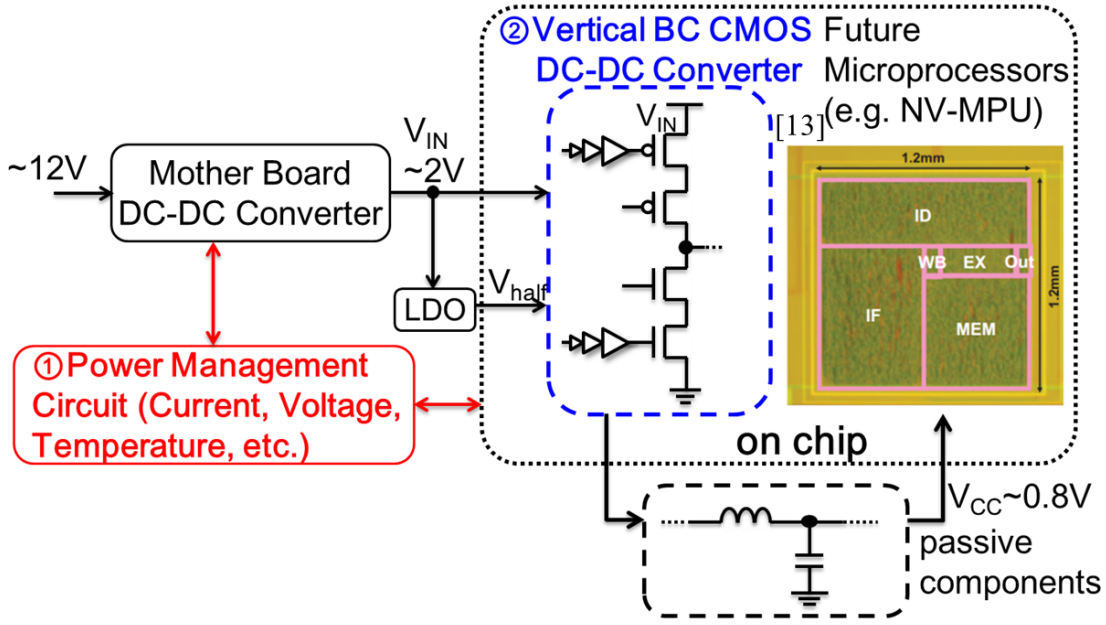


Figure 1.15. Block diagram of the concept of this research.

1.6. Thesis Overview

This thesis is organized as follows. Chapter 2 overviews power converters such as switching regulator, linear regulator, and switched capacitor. Conventional power management techniques for DC-DC converters and its issues are explained. The conventional CMOS DC-DC converter based on planar MOSFET is also described. In chapter 3, a novel current sensing method which achieves highly accurate and low-loss is proposed. In chapter 4, a novel switch toggling technique is presented and evaluated in order to suppress the temperature increase. In chapter 5, a novel Inductor Current to Digital Converter (ICDC) is proposed to decrease the required number of components for power management. In chapter 6, a highly efficient CMOS DC-DC converter circuit topology with a cascode bridge composed of an high-side (HS) NMOS power switch and a dedicated bootstrap driver using vertical BC MOSFETs is proposed. In chapter 7, in order to realize cascode CMOS DC-DC converters with improved efficiency and compactness, a novel transistor layout of multi-pillar type vertical BC MOSFET is presented. Finally, chapter 8 presents a summary, conclusion and future works of this study.

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Chapter 2

DC-DC Converter for Microprocessors in the Power Electronics Field

2.1. Classification of Power Conversion

Electric energy is used in various devices including microprocessors. AC and DC powers are one of the forms of electric energy required for these devices. As shown in Fig. 2.1, conversion to the power form required by each device is necessary [1]. AC power of 50 Hz or 60 Hz is supplied to the household outlet, whereas the integrated circuit inside the IT equipment operates with a low voltage DC power, so a circuit for converting AC to DC is necessary.

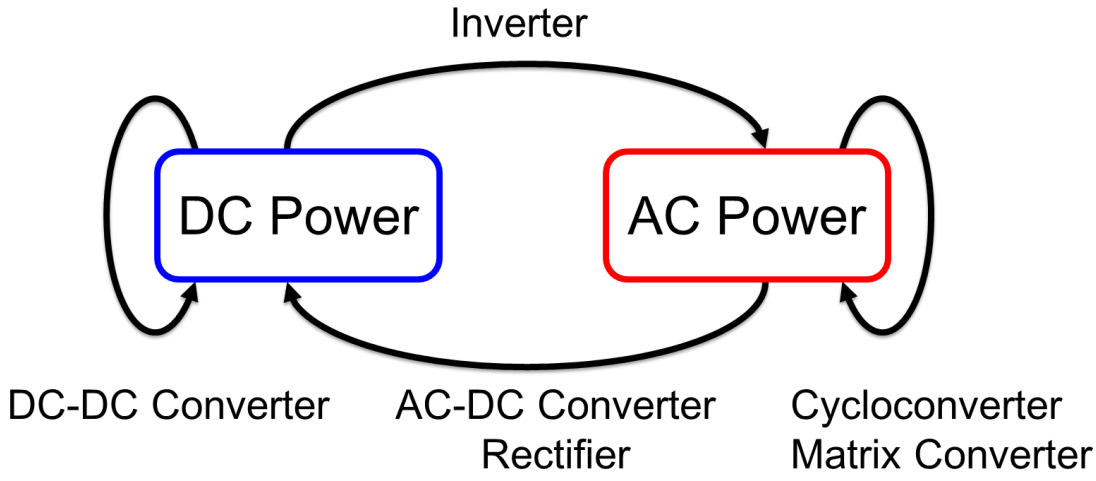
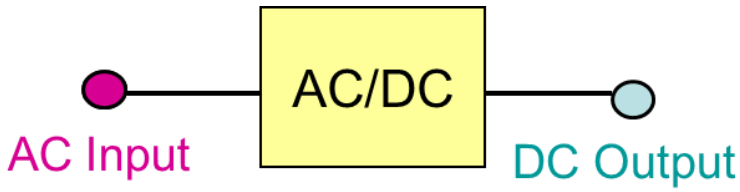


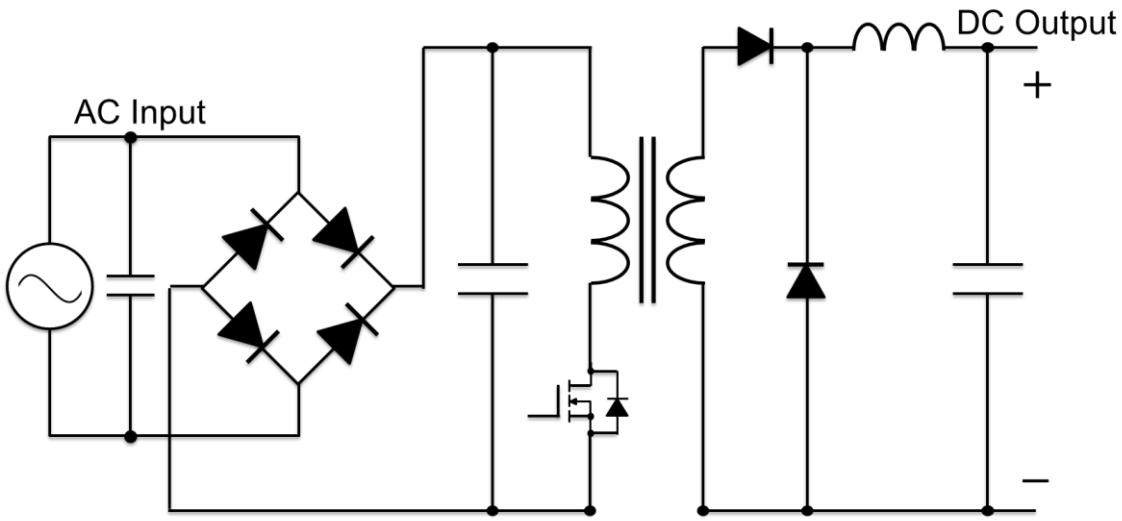
Figure 2.1. Classification diagram of power conversion [1].

2.2. AC-DC Conversion

AC-DC converters convert commercial AC power to DC power. AC-DC converters are mainly used as rack power supply in server systems. Typical output power is several tens of kilowatts to several hundreds of kilowatts. Typical output voltage is several volts to several tens of volts. Figure 2.2 shows the schematic of AC-DC converter used in computers [2]. Commercial AC power is converted to DC power by rectifier composed of a diode bridge and smoothing circuit. The output of PSU is converted to AC power by high frequency chopper circuit, and delivered to the DC output via the transformer and rectifying and smoothing circuit to isolate the output from commercial AC power supply.



(a)



(b)

Figure 2.2. (a) Block diagram and (b) schematic of AC-DC converter [2].

2.3. DC-AC Conversion

The DC-AC conversion is generally performed by an inverter. The inverter converts DC power into AC power of frequency and voltage that the load requires. Inverters are widely applied to trains, automobiles, air conditioners and the like, and are power conversion circuits at the core of energy-saving technology. The circuit configuration of a single-phase inverter is shown in Fig. 2.3 [1]. Practically, in addition to this, an input filter circuit, an output transformer, an output filter circuit, a control circuit and others are necessary. The single-phase inverter circuit is composed of four sets of switches using diodes reverse-parallel connected to the transistors as one set of switches. The voltage between U-V can output three levels of the voltages which are V_{DC}, 0, -V_{DC}. Figure 2.4 shows basic waveforms of a single-phase inverter. To control the frequency of the output voltage, the output voltage cycle T_O should be changed. The shorter T_O, the higher the output frequency, and the longer T_O the lower the output frequency.

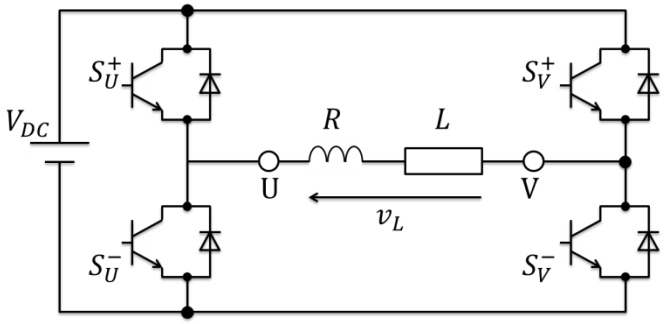
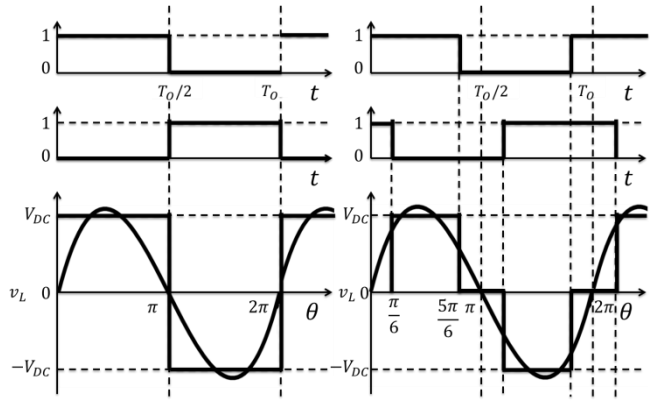


Figure 2.3. Schematic of the single-phase inverter [1].



(a) Maximum output voltage. (b) Adjusted output voltage

Figure 2.4. Basic waveforms of the single-phase inverter. [1].

2.4. AC-AC Conversion

In AC-AC conversion, AC power is converted into different voltage or frequency AC power which the load requires. A typical circuit system for AC-AC conversion includes a cycloconverter and a matrix converter. Fig. 2.5 shows a schematic diagram of a cycloconverter [3]. Cycloconverters are used to drive AC motors, constant frequency power supplies for aircraft, and electric propulsion of passenger ships for cruising. The cycloconverter is composed of twelve thyristors. Fig. 2.6 shows the basic waveform of the cycloconverter. The cycloconverter combines the input power supply voltage waveforms to create an alternating voltage with a frequency lower than the power supply frequency.

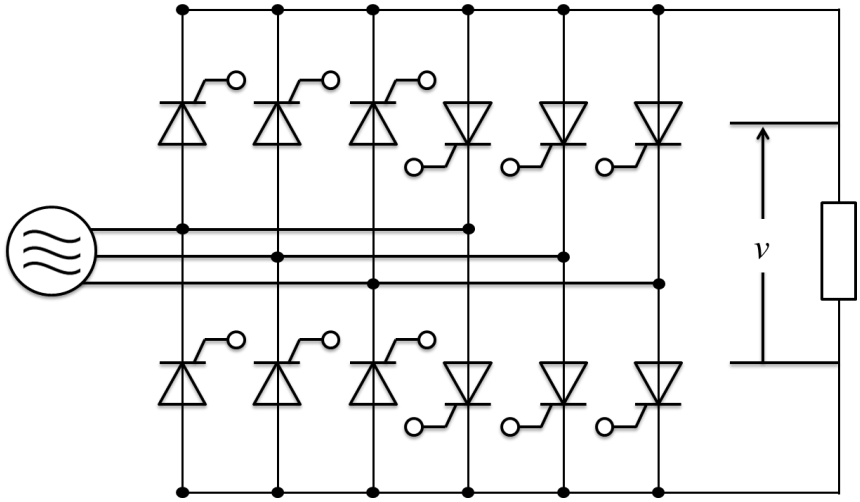


Figure 2.5. Schematic diagram of a cycloconverter. [3].

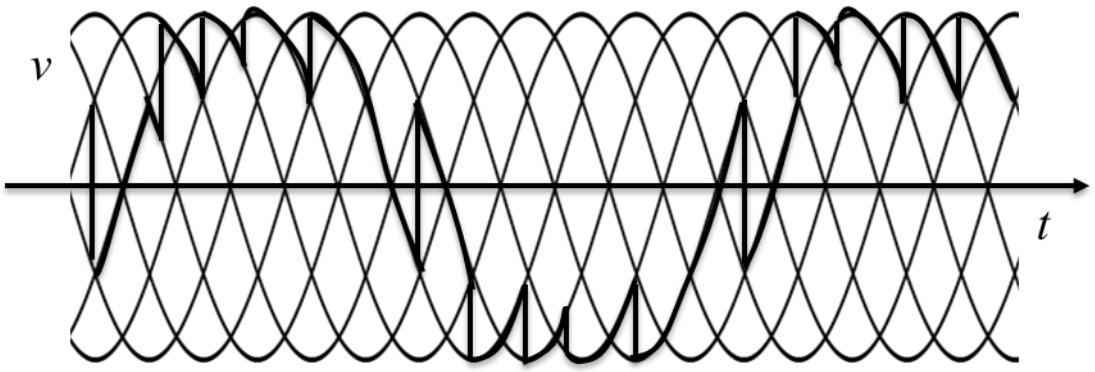


Figure 2.6. Basic waveforms of the cycloconverter. [3].

2.5. DC-DC conversion

DC-DC converter converts DC power to different level of high quality DC power. The typical output voltage is several watts to several hundreds of watts, and the typical output voltage is several watts to several tens of watts. Fig. 2.7 shows the block diagram of the DC-DC converters. Many types for DC-DC converters exist: switching regulator, linear regulator, switched capacitor, etc. Most of energy is converted by the switching regulators because they are substantially highly efficient and dense compared to other DC-DC converters. Each IC operates under different operation voltage; therefore many DC-DC converters must be located close to the ICs on a motherboard.

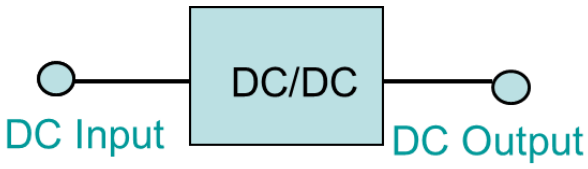


Figure 2.7. Block diagram of a DC-DC converter [2].

2.5.1. Switching Regulator

Switching regulator (in other words, Switched Mode Power Supply (SMPS), Switched-mode DC-DC converters, Point Of Load (POL) regulator, Voltage Regulator (VR), etc.) is popular for high-power applications including microprocessor power supplies for its high efficiency. For instance, Figure 2.8 shows the schematic of switching synchronous buck converter. Switching regulator needs an inductor and capacitors for energy storage. To obtain high-efficiency, it is important to select low on-resistance and low gate charge for suppressing conduction loss and switching loss. Operation under high switching frequency is important for reducing output voltage ripple noise and the size of passive components such as inductors and capacitors.

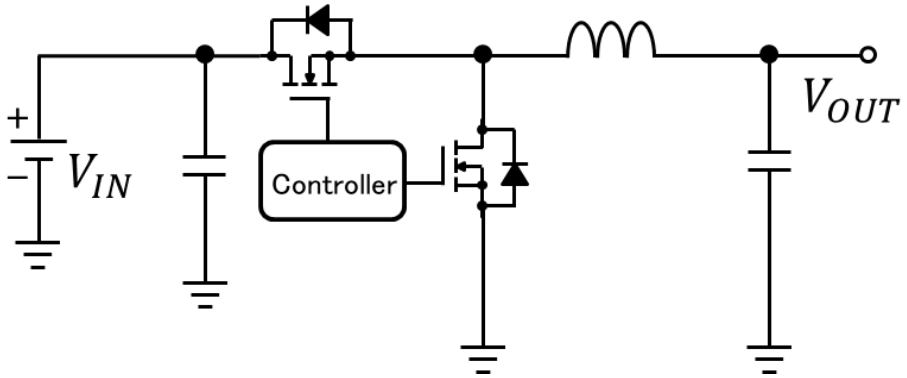


Figure 2.8. Schematic of the switching regulator.

2.5.2. Linear Regulator

Linear regulator (in other words, Low-Drop-Out (LDO) regulator) is a very simple, low Electric Magnetic Interference (EMI) noise, and low-cost power supply circuit, however, it generates a significant loss for high-to-low voltage conversion. Figure 2.9 shows a schematic of the linear regulator. Linear regulator includes power transistor (bipolar transistor or FE) and feedback circuit for monitoring output voltage. When a conversion ratio V_{OUT}/V_{IN} is small, it generates large amount of loss and heat, especially at heavy load region. Therefore, the linear regulator should be used for small energy applications with low dropout voltage.

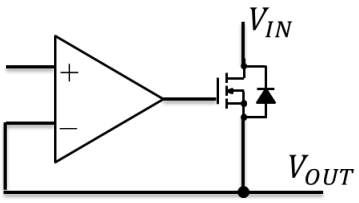


Figure 2.9. Schematic of the linear regulator.

2.5.3. Charge Pump

In charge pump circuits, a capacitor is used to storage energy which is necessary for highly efficient energy conversion. Figure 2.10 shows a schematic of the charge pump circuit. The output noise is relatively large since rush current is generated when switching occurs. Due to the energy capacity of the capacitor is smaller than inductors; a current capability is limited to a few tens of mA. As a future microprocessor power supply, the charge pump might be insufficient to supply large current.

Table 2.I shows the summary of DC-DC converter topologies. Even so the switching regulators require inductor, capacitor, switching components and controllers, switching regulators will keep popular in microprocessor power supply applications because it is inherently highly efficient and is able to supply high current. Therefore, this thesis focuses on power management technologies and efficiency enhancement technologies for switching regulators from here.

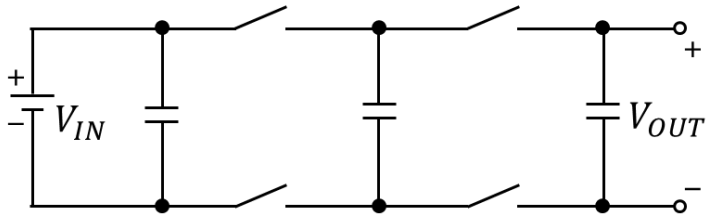


Figure 2.10. Schematic of the charge pump

2.6. DC-DC Converter Power Management

2.6.1. Conventional Current Sensing Methods for DC-DC Converters

Accurate current sensing in DC-DC converter is important because future microprocessor generates frequent and massive load fluctuations. There are many reasons why the switching regulators need current sensing circuit. Recent DC-DC converter for microprocessors is required to equip a function which adjusts output voltage according to the output current, called adaptive voltage positioning as shown in Fig. 2.11 [4]. Multi-phase DC-DC converter which is shown in Fig. 2.12 requires current sharing function, which equalizes the current in each module to dissipate current stress in components [5]. Modern microprocessors needs accurate current information to grasp its power consumption to calculate appropriate operation frequency considering power and heat budget. Over Current Protection (OCP) which shuts down the power supply when the amount current exceeds the limitation is an essential function for DC-DC converters to guarantee a fail-safe operation.

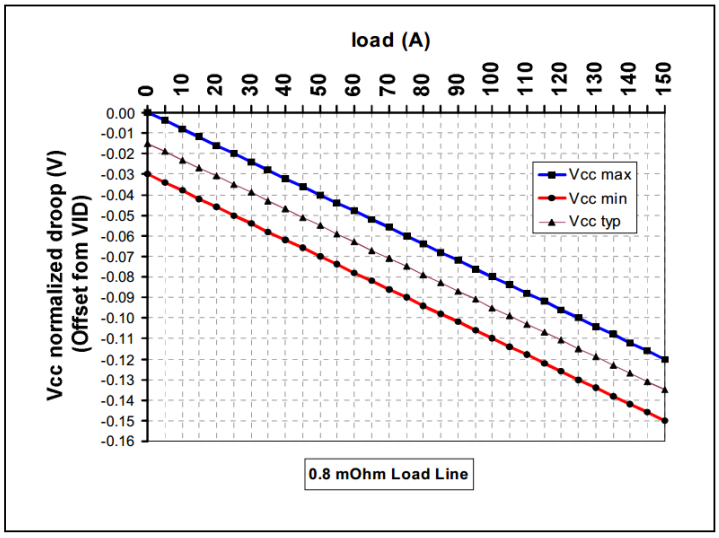


Figure 2.11. Adaptive Voltage Positioning (AVP) which droops output voltage according to the level of load current [1]. AVP is a standard equipment in modern microprocessors.

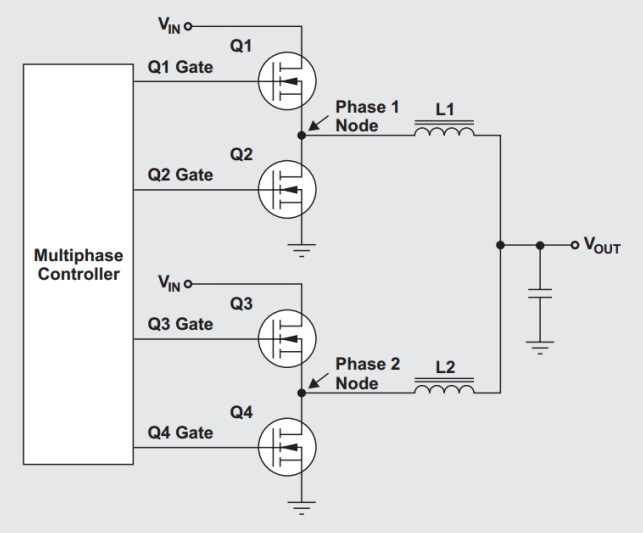


Figure 2.12. Schematic of two-phase DC-DC converter [5].

Conventional current sensing methods for microprocessor power supplies usually use voltage drop of some sort of resistive component. Resistor sensing which is shown in Fig. 2.13 uses a dedicated sensing resistor connected in series with a power inductor [6]. Resistor sensing is often accurate compared to other sensing methods because it can use a resistor based on a alloy which has low component tolerance and low temperature coefficient. However, it is not widely adopted in microprocessor power supplies because it dissipates large conduction loss.

On the other hand, inductor Direct Current Resistance (DCR) sensing which is shown in Fig. 2.14 is very popular for microprocessor power supplies for its low-loss feature. DCR sensing uses a parasitic winding resistance of the power inductor RL. Parallel RC network with matched time constant is additionally required to obtain the current sensing signal voltage which is proportional to the inductor current.

Rds sensing detects a voltage drop across the drain and gate of high or low-side power transistor when conducting as shown in Fig. 2.15. Rds sensing is low-loss sensing method among the resistive current sensing method because additional resistive component is required on the current path. However, it needs to neglect the off-state voltage and very inaccurate, and has large temperature dependence. Pros and Cons of the conventional current sensing methods are summarized in Table 2.I. These conventional methods have the disadvantage either of the loss or accuracy, therefore accurate and low-loss current sensing method is required.

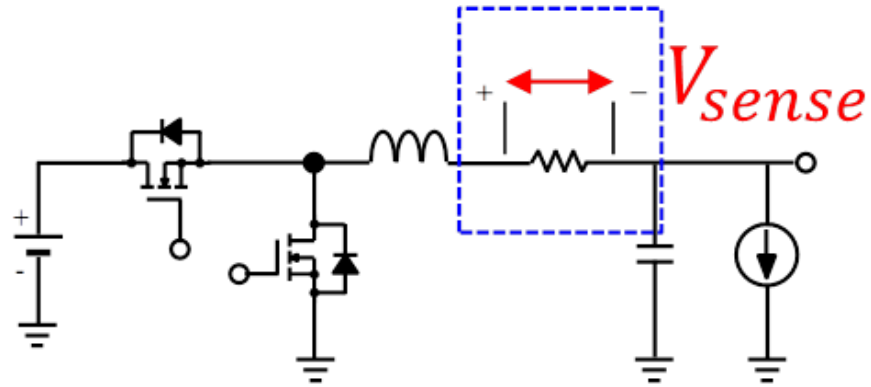


Figure 2.13. DC-DC converter with a sensing resistor method.

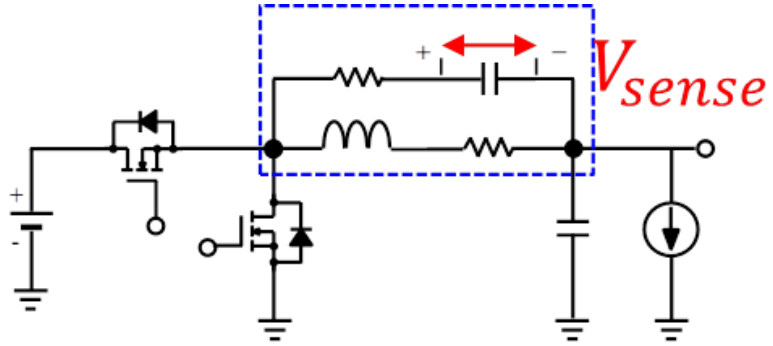


Figure 2.14. DC-DC converter with a inductor Direct Current Resistance (DCR) method.

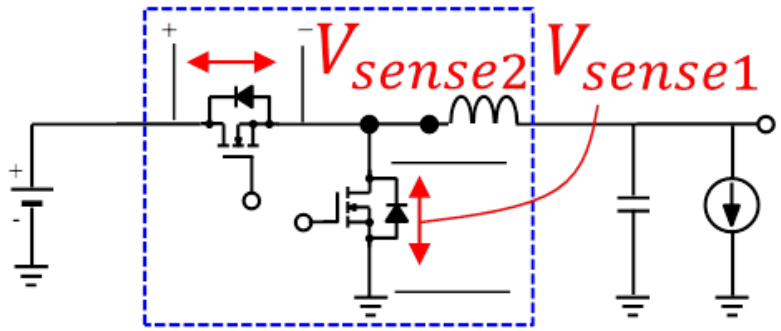


Figure 2.15. DC-DC converter with a R_{ds} method.

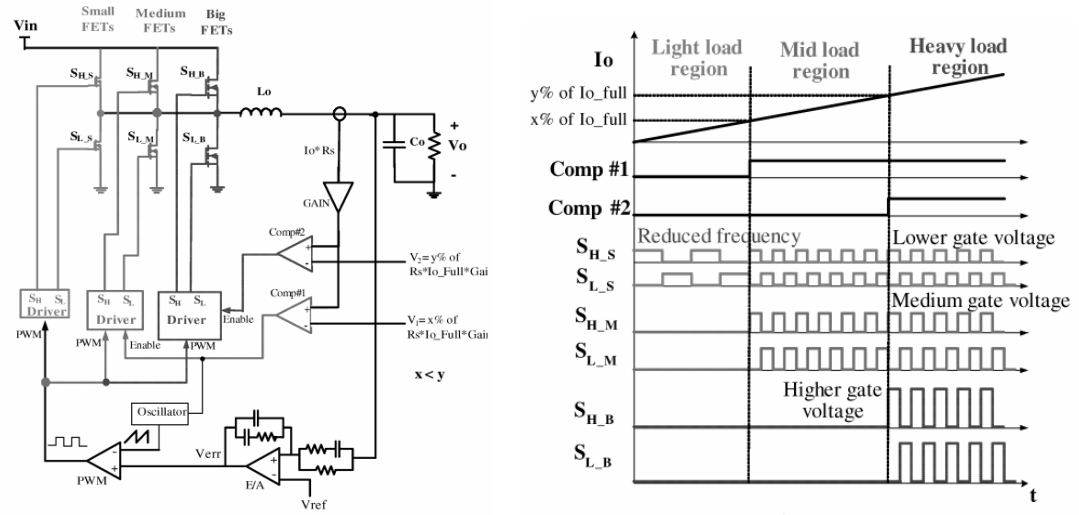
Table 2.I. Pros and cons of conventional current sensing methods for DC-DC converters.

Method	Pros	Cons
Sensing resistor	· High accuracy · Small TC	· High loss
Inductor DCR	· Low loss	· Low accuracy · Large TC
R_{ds}	· Low loss	· Low accuracy · Large TC

※TC: Temperature Coefficient

2.6.2. Adaptive Control for Efficiency Improvement for Wide Load Range

The adaptive control is a power management technique which is utilized to enhance efficiency within wide load range by modulating circuit operation according to the level of load current. Adaptive phase number control is one of the adaptive control techniques which adjust the number of active DC-DC converter module used in multi-phase DC-DC converter. Apart from this, adaptive FET modulation (AFM) is able to enhance light load efficiency without additional inductors or capacitors [7]. Figure 2.16 shows the schematic of the DC-DC converter using conventional AFM technique. The conventional AFM technique is composed of power MOSFETs connected in parallel, several drivers, control logic, and reference current comparators. However, the temperature increase on the power MOSFETs under the operation which is critical for the reliability is not clarified in the conventional AFM technique.



(a) Schematic. (b) Timing diagram

Figure 2.16. Conventional Adaptive FET Modulation (AFM) technique [7].

2.7. CMOS DC-DC Converters Using Cascode Power Switch

CMOS DC-DC converter is an on-chip power supply circuit which is utilized in some of commercial microprocessors. Fig. 2.17 shows the block diagram of a power distribution network using CMOS DC-DC converters [8]. CMOS DC-DC converter converts energy by using low-voltage CMOS devices as a power switch at very close to core circuits in order to archive very high switching frequency, low output impedance, and small implementation area, and high efficiency. The CMOS DC-DC converter utilizes very small power inductor such as 0.9 nH, therefore the implementation area becomes very small which enables to incorporate inductors on-chip or on-package. Intel uses on-chip Air Core Inductor (ACI) as a power inductor for the CMOS DC-DC converters as shown in Fig. 2.18 [9].

In the power stage in CMOS DC-DC converter for microprocessors, CMOS cascode bridge is frequently adopted. Figure 2.19 shows the circuit diagram of the cascode bridge utilized in 8-phase integrated voltage regulator applications. The cascode bridge uses cascode power switches which connect two or more MOSFET in series as high and low-side power switches. In the two MOSFETs cascode bridge, half-rail voltage which is a half of the input-voltage is needed to handle the input-voltage by low-voltage CMOS device. The one of the issues of the conventional CMOS DC-DC converter is a conduction loss generated at the high-side cascode power switch composed of p-type MOSFETs (PMOS). The on-resistance of PMOS is significantly larger than n-type MOSFET (NMOS) because the mobility of PMOS is often as small as a half of that of NMOS. In addition, conventional CMOS DC-DC converter based on planar MOSFET occupies large transistor area and generates large loss due to its small drivability.

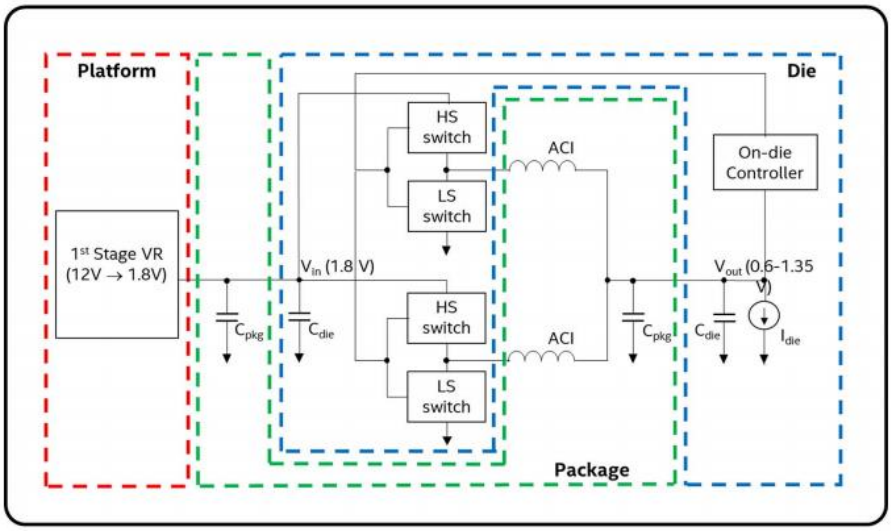
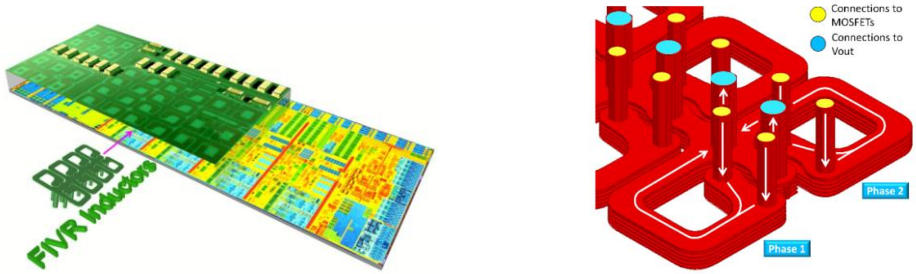


Figure 2.17. Diagram of power supply including on-board and on-chip converters [8].



(a) Diagram of the on-package implementation. (b) Connections to the terminals.

Figure 2.18. Air core inductor for embedded microprocessor power supply [9].

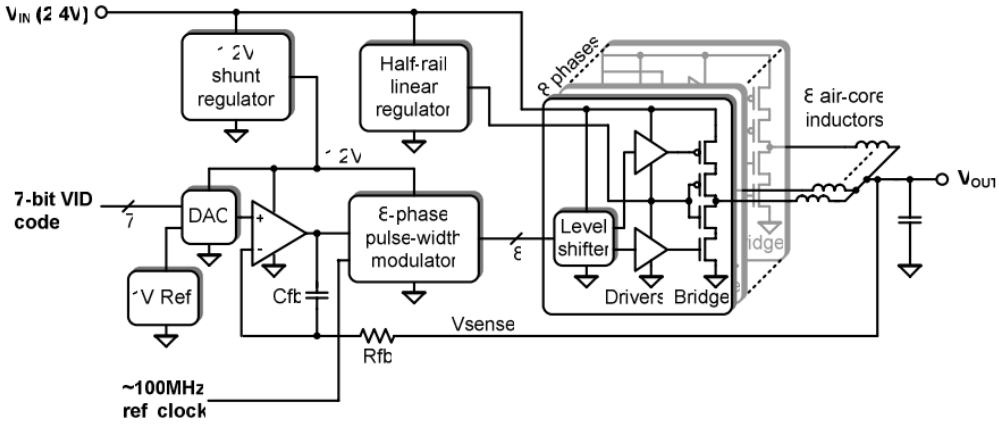


Figure 2.19. Schematic of 8-phase cascode bridge DC-DC converter [10].

2.8. Vertical Body Channel (BC) MOSFET

2.8.1. Electrical Characteristic

Three dimensional structured CMOS devices are massively studied for its excellent electric characteristics and scalability. Vertical Body Channel (BC) MOSFET arranges source, drain and channel vertically as shown in Fig. 2.20 [11]. Fig. 2.21 shows the measured current-voltage (IV) characteristic of both p-type and n-type vertical BC MOSFETs fabricated in 60 nm CMOS technology [12]. In the drain current (ID) - gate voltage (VGS) characteristics in Fig. 2.21(a), the drain voltage is applied to 0.05 V and 1.0 V. The vertical BC MOSFETs archives steep sub-threshold swings which are 69 mV/decade for n-type and 66 mV/decade for p-type. The on-current is 281 μA/μm for n-type and 149 μA/μm which indicates the high drivability of the vertical BC MOSFETs. ID-VGS characteristics with three different substrate bias voltage (VSUB) is shown in Fig. 2.22 [12]. The drain current is hardly affected by the back bias voltage in linear region. Therefore, vertical BC MOSFET is attractive for CMOS DC-DC converters because of its high current drivability and back bias free characteristic.

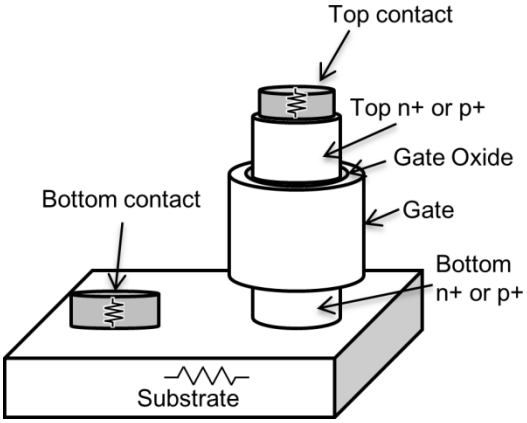
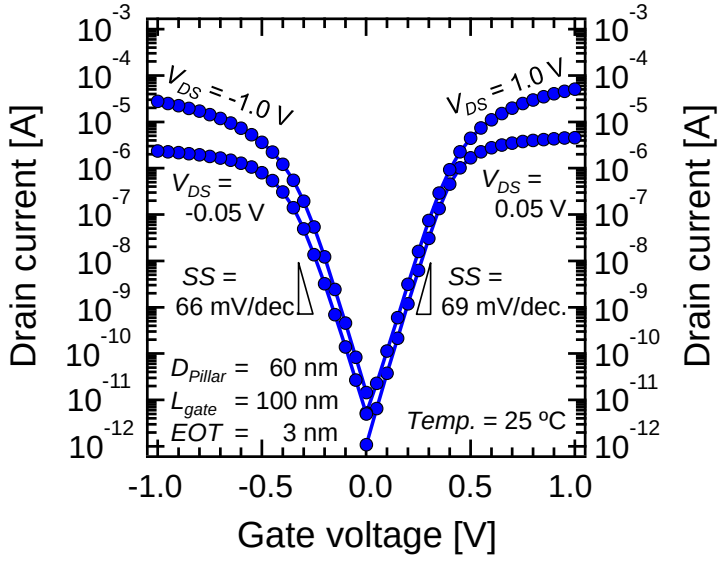
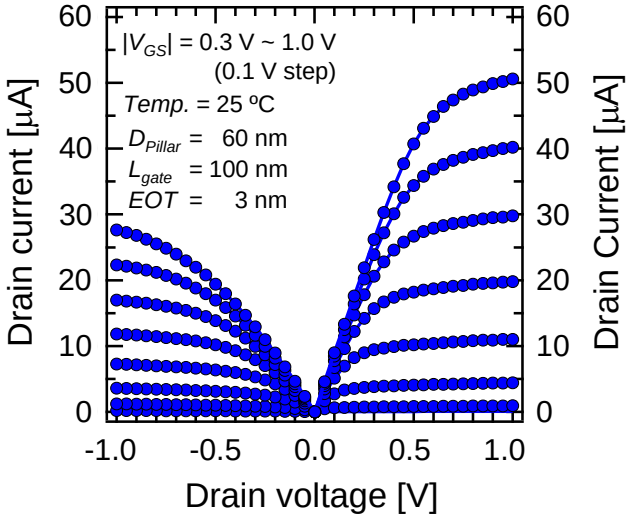


Figure 2.20. Bird’s eye view of the vertical Body Channel (BC) MOSFET [11].



(a) I_D-V_{GS} characteristics



(b) I_D-V_D characteristics

Figure 2.21. Current voltage (IV) characteristics of the p- and n-type vertical BC MOFETs [12].

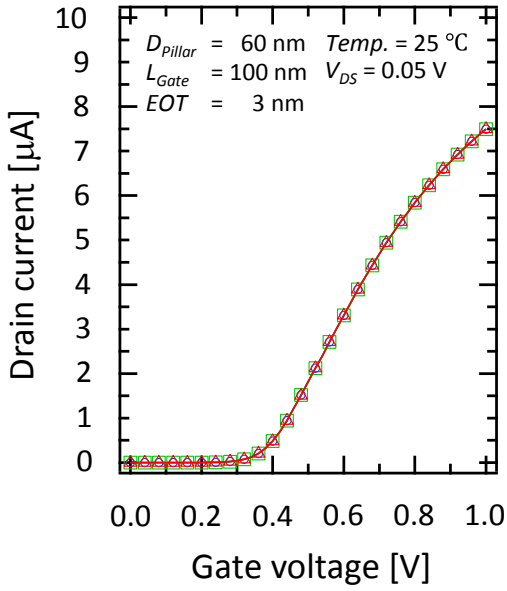
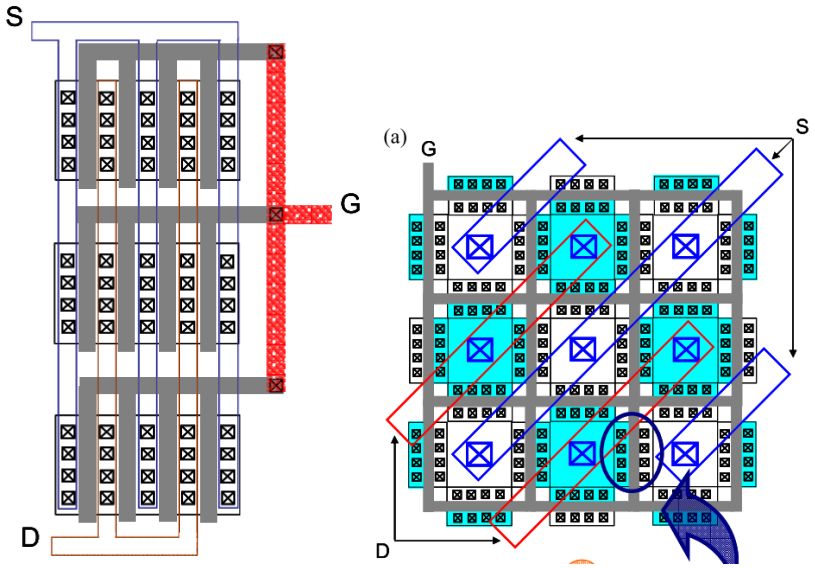


Figure 2.22. Current-voltage characteristic of the vertical BC MOSFET under various back bias voltage conditions [12].

2.8.2. Transistor Layout for Power Switch

In CMOS DC-DC converter applications, the transistor layout of power switches should be arranged carefully because its performance is dependent on the layout. Figure 2.23 shows an example of the conventional transistor layout of the power switch based on planar MOSFETs [13]. The multi-fingered structure is widely used because it can achieve low on-resistance. The hybrid waffle layout has lower loss than the multi-fingered layout, however it requires diagonal lines which needs additional process cost.

Meanwhile, these transistor layout cannot be applied to the vertical BC MOSFETs because the transistor layout of vertical MOSFETs should be designed taking care of top and bottom contacts as shown in Fig. 2.24. The conventional layouts and its effects on the drain current characteristics are investigated in Ref. 11. For the non-cascode use, it can obtain relatively large drain current by locating intermediate bottom contacts surrounded by silicon pillars in multi-pillar type vertical MOSFETs. However, the area and energy efficient layouts for the cascode power switches which are widely applied in CMOS DC-DC converters for microprocessors have not clarified yet.



(a) Conventional multi-finger layout. (b) Hybrid waffle layout.

Figure 2.23. Conventional transistor layouts with planar MOSFETs for power switches [13].

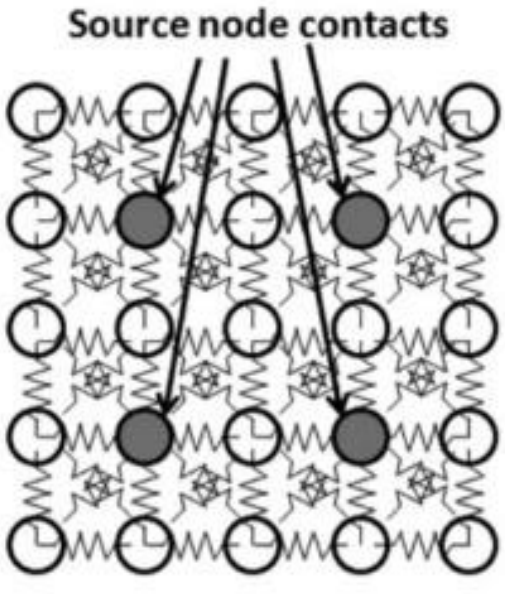


Figure 2.24. Top view of the conventional transistor layout with vertical BC MOSET for power switches [14]. The conventional layout has intermediate bottom contacts in order to obtain large drain current.

2.9. Conclusions

Among various power conversion circuits, the DC-DC converter plays a role of directly supplying stable DC power to various electronic circuits including microprocessors. From the viewpoint of power supply to the microprocessor, comparisons were made on the typical topologies of DC - DC converters. In these topologies, switching regulator is widely applied, and will keep its popularity for microprocessor power supply applications for its efficiency, area, high power output, and etc. Typical resistive current sensing methods and adaptive control techniques are described as an important power management technique for microprocessors. In addition, CMOS DC-DC converter which is commercially used for microprocessor power saving is described and explained. Since conventional CMOS DC-DC converters are based on planar MOSFETs, it has an issue regarding to the loss and the transistor area. A vertical MOSFET is described for an attractive device to overcome the issue in the conventional CMOS DC-DC converters for its high current drivability and back-bias free characteristics.

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Chapter 3

Highly Accurate and Low-Loss Current Sensing Method for Power Management of DC-DC Converters

3.1. Introduction

As a power supply circuit of a Very Large Scale Integration (VLSI) system typified by a microprocessor and a micro-controller, a DC-DC converter can be said to be an important circuit block in a modern computers. A dedicated DC-DC converter for microprocessors is generally referred to as Voltage Regulator Modules (VRMs). Since the power demand of microprocessors is increasing, high efficiency and high reliability are indispensable requirements in state-of-the-art VRM technology.

The application of the current information in the DC-DC converter, particularly VRM, is as follows: Adaptive Voltage Positioning (AVP) technology that lowers the output voltage in proportion to the amount of current is an indispensable specification in current microprocessors to improve transient response [1-3]. It is necessary to implement AVP technology on the controller of VRM. In multi-phase type VRM, the current amount in each module must be made uniform by using current feedback in order to alleviate thermal stress [4], [5]. In order to avoid excessive temperature rise of the processor die, it is necessary to determine the power state by referring to the current amount information flowing in the VRM [2], [6]. In the VRM adopting the current mode control, the current signal is used as the feedback signal of the second order loop. Over current protection is an indispensable requirement in commercial VRM to guarantee failsafe operation. For the above reasons, high precision current detection in VRM is an important requirement for high reliability and performance improvement of computer systems. In addition, since the digital controller is becoming a majority in VRM due to the merit that the number of elements is small, it is desirable that the current detection be obtained by digital value by using Analog-to-Digital Converter (ADC) [7]-[9].

Various current detection methods can be applied to VRM. For instance, a

current transformer, a hall sensor, and a Giant Magneto Resistive (GMR) sensor are one of the main methods in current detection [12]-[14]. However, the above technique requires a very large or expensive external element, therefore it is a minor in VRM applications. Since inductor DC Resistance (DCR) method is low cost and lossless, it is widely used in commercial VRM [13]-[16]. The main drawback of the DCR method is that the current voltage gain largely changes according to the temperature because the temperature coefficient of the copper wiring forming the inductor which is the detection element of the DCR method is as high as 3900 ppm/℃. In the Rds method, the on-resistance of the power MOSFET is used as a current sensor by detecting the voltage across the drain terminal and the source terminal of the power MOSFET [15]. Similar to the DCR method, the Rds method utilizes the parasitic resistance of the basic element of the DC-DC converter and is low cost and lossless. However, both the temperature coefficient and the resistance tolerance are worse than the DCR method, and rarely used in high-end computers. Although the DCR method and the Rds method are lossless, there are design restrictions that lead to a considerable increase in conduction loss: a component having a large resistance value must be selected to obtain noise immunity in an actual application.

Another approach which detects the current using a sense resistor while shunting by multiple MOSFETs for lower loss can be considered. However, in this method, the measured value is effected by other parasitic resistance values with low precision, such as MOSFET on-resistance, so the accuracy is low.

When importance is attached to the reliability of the system, dedicated sensing resistor should be used for current detection. When sensing resistance is used, the cost becomes moderate, and accuracy is very high compared with Rds and DCR method [14], [17]. The current detection system of the DC-DC converter using the sense resistor is described in the Fig. 3.1. The sensing resistor Rsen is connected in series with the load. Due to the conduction loss generated in the resistance which can be expressed as RsenI2, the conversion loss of the DC-DC converter is remarkably lowered. Various techniques have been proposed to solve this problem. In the on-line calibration technique, the merits of low-loss of Rds sensing and high accuracy of resistor sensing are combined [17]. In the discrete current sensing, the current bypasses the sensing resistor when current is not sampled [18], [19]. However, these conventional methods require a large number of additional switches, so that a large efficiency improvement can not be obtained due to the switching loss generated.

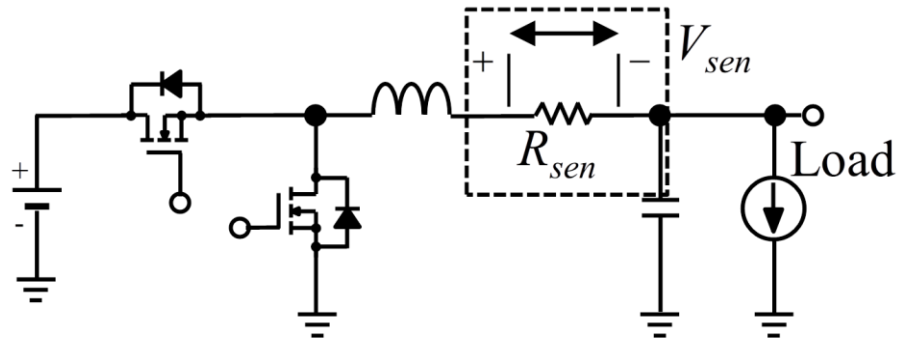


Figure 3.1. Schematic of DC-DC buck converter with a resistor connected in series with load.

A novel Current Path Narrowing (CPN) method is presented to achieve low-loss and accurate current detection in this chapter. Sensing resistor is connected between low-side switch and the ground in the proposed method. Only an additional switch is required in the DC-DC converter. By sampling the current during the low-side switch is on and the auxiliary switch is off, and then distributing the current by turning the auxiliary switch on, the proposed method lowers the loss in the sensing resistor. In order to quantify the effect of the proposed method, the equivalent resistance analysis, which is a widely used method for predicting the conduction loss of the DC - DC converter, was used [20]-[22]. From the results of the equivalent resistance analysis, we analyzed the optimum design methodology under the same Figure Of Merit (FOM) RonQg condition. Furthermore, an experimental verification was carried out on the prototype DC-DC conversion circuit board of the proposed method [23]. The gate signal of the proposed method was generated by FPGA using a simple algorithm and demonstrated its operation under closed loop digital voltage mode control.

3.2. Operation Principle and Design Considerations of the Proposed Current Path Narrowing Method

A large conduction loss occurs when the entire load current flows through the sense resistor, so that the conventional sense resistor system has been used only for applications in small current applications. On the other hand, adding a MOSFET, a current detection amplifier, a calibration ADC, etc. for compensation increases the cost of VRM.

Our proposal is based on resistance current detection incorporating low loss technology. The circuit diagram of the DC-DC converter using the proposed method is described in the Fig. 3.2. The power stage includes a sensing resistor Rsen, a high-side switch Q_{HS}, low-side switch Q_{LS}, auxiliary switch Q_{aux}. The resistor is connected between Q_{LS} and ground. Similar to a general synchronous buck DC-DC converter, Q_{HS} and Q_{LS} are driven by complementary gate drive signals. The current detection is conducted by sampling the voltage of Rsen for a short duration in a switching cycle. The inductor current IL is distributed to the branch with Qaux when the ADC holds the current value in the internal Sample and Hold circuit (S/H). The proposed method uses the loss suppression mode only when the sample and hold circuit is in the hold mode. Therefore, the proposed operation does not hinder the voltage control operation of the DC-DC converter.

Figure 3.3 shows the timing chart of proposed method. Q_{HS} turns on and the switching node voltage, V_X becomes approximately a value close to V_{IN} for the period T_{ON} at time t_0. Q_{HS} turns off, then Q_{LS} and Q_{aux} simultaneously turn on and V_X decreases to 0 V at time t_1. Qaux turns off while Q_{LS} is on, then the ADC starts sampling the current signal at time t_2. Finally, when Q_{LS} turns off and Q_{HS} turns on, the next switching cycle starts.

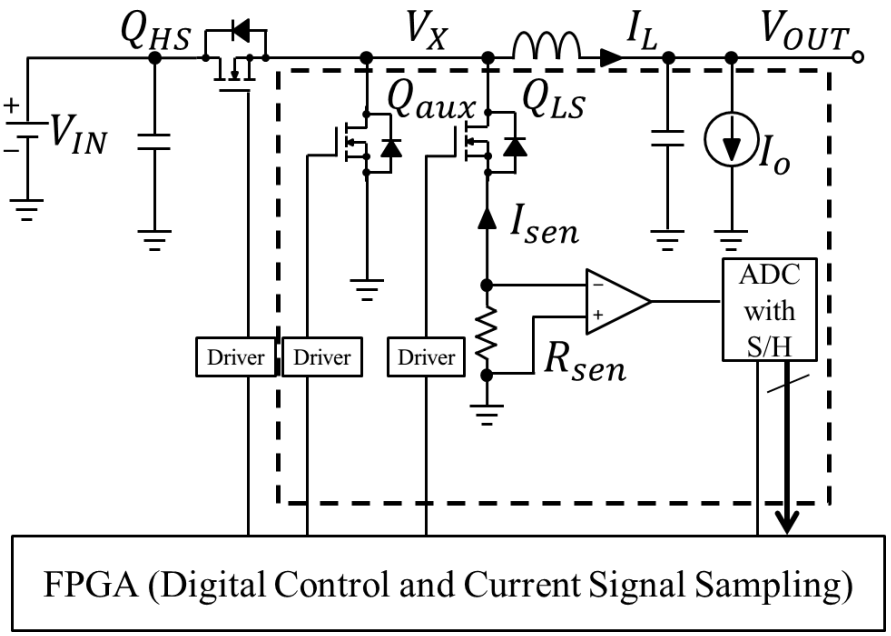


Figure 3.2. The block diagram of the synchronous buck DC-DC converter with the proposed current sensing method [25].

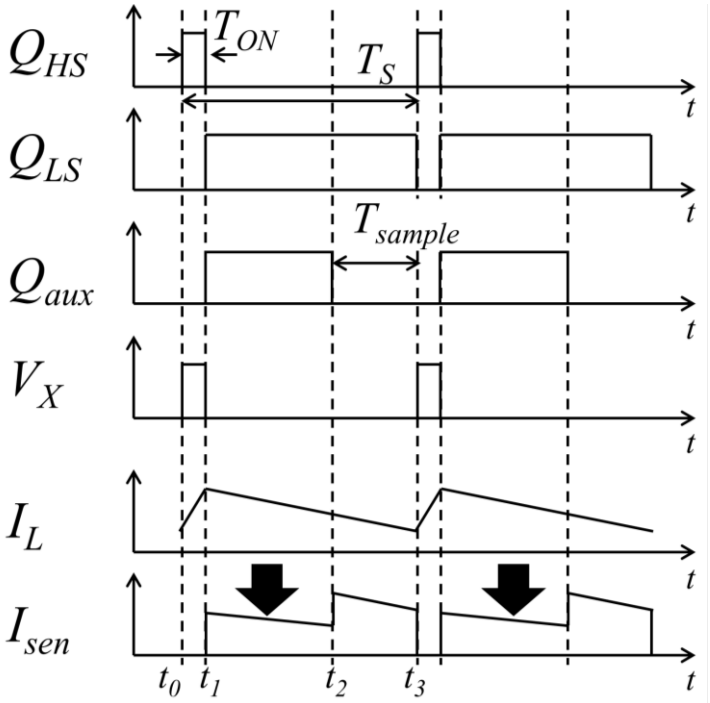


Figure 3.3. Timing diagram of the proposed method [25].

Because the parallel resistance of the branches with Q_{LS} and that with Q_{aux} is small, conduction loss from t_1 to t_2 is lower than that of t_2 to t_3. Consequently, a key point to realize low-loss is to design T_{sample} as short as possible. Here, a sampling duty cycle D_{sample} is defined as follows:

$$D_{sample} = T_{sample} / T_S , \qquad (1)$$

where T_S represents a switching period. Because the loss dissipated from t_2 to t_3 is relatively large, D_{sample} is a key parameter for realizing low-loss switched-mode DC-DC converters with the proposed method. The selection of the ADC is also an critical matter. Note that an acquisition time T_{ACQ} of the ADC should be shorter than T_{sample} to sample the current value correctly. ADCs with small T_{ACQ} often becomes expensive; hence designers should lengthen T_{sample} until the cost of the ADC becomes acceptable. It should be also noted that the duty cycle D_{ON} is limited by D_{sample} value which can be expressed as follows:

$$D_{ON} = T_{ON} / T_S , \qquad (2)$$

$$D_{ON} < 1 - D_{sample} , \qquad (3)$$

where T_{ON} represents an on-time of the gate driving signal of Q_{HS}. Given that D_{sample} is nearly 0.1, it is not an challenge for synchronous buck DC-DC converters with a small conversion ratio V_{OUT}/V_{IN}, because D_{ON} hardly exceeds 0.9 even when a large load step occurs. Other considerations include the additional switching loss in Q_{aux}, which is mainly caused by the gate charge Q_g and output capacitance C_{OSS}. The switching loss induced by C_{OSS} is often much lower than that of Q_g, so that it is neglected for the sake of simplicity in this thesis. To discuss about the design of the switching loss due to Q_g, on-resistances of Q_{LS} and Q_{aux} should be considered together because Q_g is often approximately inversely proportional to R_{ds} of MOSFETs under a constant FOM $R_{on}Q_g$. The effect of the parameters D_{sample}, R_{ds} and Q_g on the loss is carefully considered in Section 3.4 in terms of the equivalent circuit.

In addition, the effect on the failure rate accompanying the increase in the number of components of the MOSFET of the proposed method should be taken into consideration. Assuming server application as an example, the Mean Time Between Failure (MTBF) required for the server is 45,753 hours [23]. The failure rate of industrial products is defined as Fail in Time (FIT) as follows.

$$\mathrm{FIT} = 1/\mathrm{MTBF}/10^{-9}$$

Therefore, the failure rate required for the server is 21,856 FIT. The number of additional MOSFET in the proposed method is only one, and the FIT of the

semiconductor device is generally about 10 to 100 [24]. Since the failure rate when components are added can be obtained by the sum of FIT, the effect on the failure rate by adding one MOSFET in the proposed method can be said to be minor.

3.3. Equivalent Circuit Modeling

To predict the loss in switched-mode DC-DC converter with the proposed method, a systematic approach in deriving the equivalent circuit model as mentioned earlier [20]-[22] is conducted. Assuming that parasitic resistances can be modeled by linear resistances, the conduction loss including parasitic elements connected in series with the inductor can be expressed utilizing averaged equivalent resistance model as follows:

$$P_{cond} = R_{eq} I_{L,RMS}^2 \text{ ,(4)}$$

where R_{eq} is an averaged equivalent resistance and $I_{L,RMS}$ is a Root Mean Square (RMS) inductor current. R_{eq} can be derived by the product of the resistance of each branch and its duty cycle. The switching states of the synchronous buck DC-DC converter with the proposed method are illustrated in Fig. 3.4, where R_{HS}, R_{LS} and R_{aux} represent on-resistances of Q_{HS}, Q_{LS} and Q_{aux}, respectively, R_{DCR} represents a DCR of the inductor, and R_{PCB} represents a trace resistance of a Printed Circuit Board (PCB). From t_0 to t_1, I_L flows through R_{HS}, R_{DCR} and R_{PCB} for T_{ON}. From t_1 to t_2, I_L is divided to two branches. The branch currents are determined by the ratio of the series resistance of R_{LS} and R_{sen}, and R_{aux}. Then, from t_2 to t_3, I_L is concentrated to the branch with R_{sen} by turning off Q_{aux} to measure the current sensing voltage V_{sen} for T_{sample}.

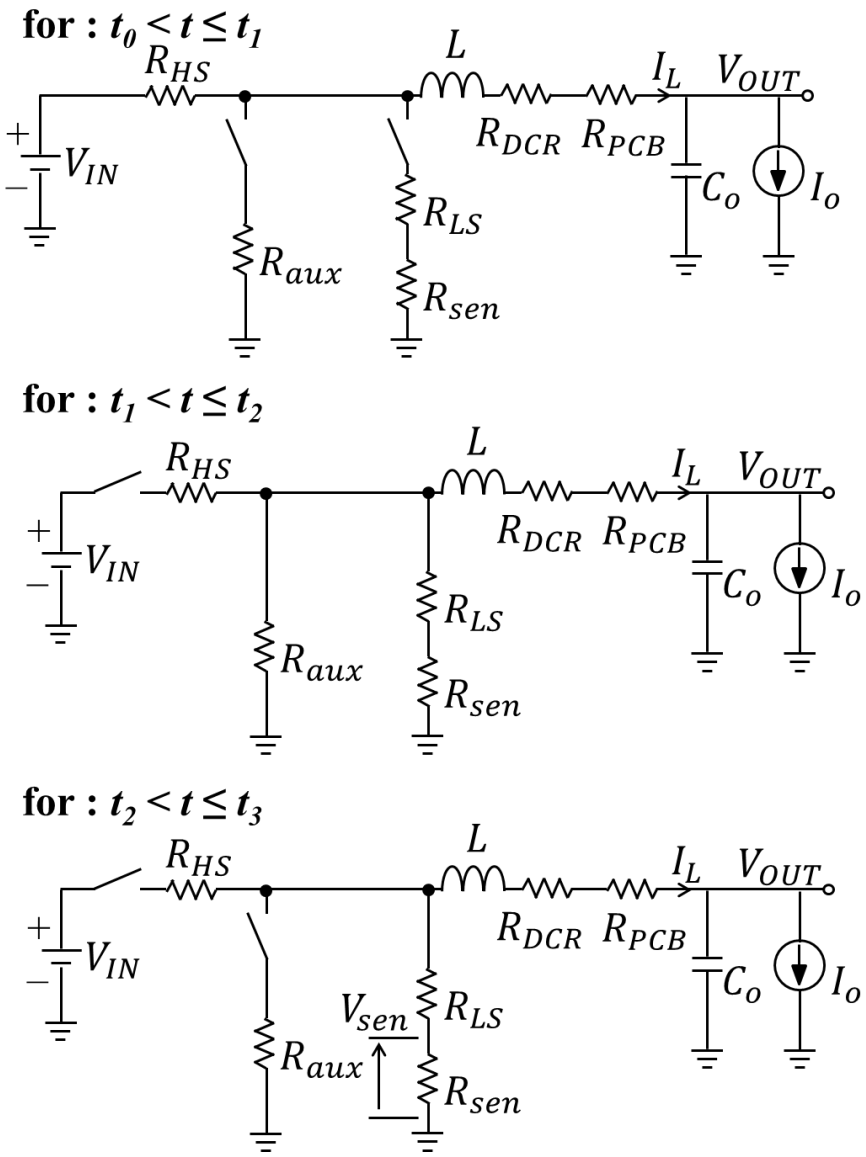


Figure 3.4. Switching states of the synchronous buck DC-DC converter with the proposed method [25].

The averaged equivalent resistance of the proposed method is derived by the following equation:

$$R_{eq,prop} = D_{ON} R_{HS} + (D_{OFF} - D_{sample})\{R_{aux} \,||\, (R_{LS} + R_{sen})\} + D_{sample} (R_{LS} + R_{sen}) + R_{DCR} + R_{PCB}, \qquad (5)$$

where D_{OFF} is (1-D_{ON}).

As a matter of course, additional switching losses in Q_{aux} must be taken into account. The switching loss induced by the gate charge is expressed as follows:

$$P_{gate} = Q_g \, V_{drv} \, f_{SW}, \qquad (6)$$

where V_{drv} is an amplitude of a gate voltage swing and f_{SW} is a switching frequency. In order to compare the proposed method with the conventional methods which do not require the auxiliary switch, the amount of the gate charge should be equivalent. Here, the sum of the gate charges of Q_{LS} and Q_{aux} is defined as

$$Q_{g,total} = Q_{g,LS} + Q_{g,aux} . \qquad (7)$$

MOSFET with low $R_{on}Q_g$ leads to high efficiency in switched-mode DC-DC converters [26], [27]. The on-resistance of MOSFETs is inversely proportional to the gate charge Q_g under the constant $R_{on}Q_g$. Assuming that $R_{on}Q_g$ of each MOSFET is constant, the on-resistance of a MOSFET with gate charge $Q_{g,total}$ can be expressed as:

$$R_{LS,total} = R_{LS} \,||\, R_{aux}. \qquad (8)$$

For comparison purpose, the low-side switch utilized in conventional resistive sensing methods is assumed to have the on-resistance $R_{LS,total}$ in Section 3.4 which makes the amount of the total switching loss equivalent to the proposed method.

3.4. Benchmark of Resistive Current Sensing Methods

The objective of the proposed method is to provide current sensing circuit with lower loss and higher accuracy than conventional methods. In order to understand the merits of the proposed method under practical design constraints, a parametric

estimation is performed. In this section, performances of various resistive current sensing methods including the proposed method are benchmarked using typical specifications of resistive current sensors listed in Table 3.I. Tolerances of resistances and temperature coefficients are taken into account in this estimation. We focused on sensing resistor, inductor DCR and R_{ds} for example because they are popular in commercial VRMs due to its accuracy, loss, noise immunity and cost. As a case study, single-phase synchronous buck DC-DC converters with various resistive sensing methods are evaluated. Furthermore, a design methodology of a current sensing circuit using the proposed method is derived and presented in terms of an averaged equivalent resistance.

Table 3.I. Typical specifications of resistive current sensors.

	Tolerance of resistance	Temperature coefficient (ppm/°C)
Sensing resistor	1%	20
Inductor DC resistance (DCR)	5%	3,900
MOSFET R_{ds}	10%	4,000

3.5. Effect of Parasitic Inductance on Accuracy

Since the current fluctuates in the signal waveform in the proposed method, it is necessary to evaluate whether or not the parasitic inductor affects the accuracy. Here, circuit simulation using SIMETRIX considering the parasitic inductor component of the sense resistor is performed. Fig. 3.5 shows the schematic diagram of the simulated circuit. I1 and I2 is current pulse generator, and C1 is a 10 pF parasitic capacitance of PCB, R1 is a 2 mΩ sensing resistor, and L1 is a parasitic capacitance. At the right hand side, a differential amplifier circuit whose gain is 10 is shown. It is simulated with the parasitic inductance parameters of 0.5 nH and 5 nH, respectively. The simulated waveforms are shown in Fig. 3.6. The bottom pane shows the applied two step current pulse which has 100 kHz switching frequency, 0.5 A of first step amplitude and 1.0 A of second step amplitude. The top pane shows the output signal voltages. Among the

waveforms shown in the top pane, the blue one shows the case where L1 is 0.5 nH, and the one of red shows the case where L1 is 5 nH. A spike with an amplitude of 100 mV is observed in the output waveform, but the spike diminishes after 5 to 10 μs. Therefore, if sampling is carried out after ensuring an appropriate settling time after the current fluctuation, current detection with high accuracy is possible even if there is an influence of parasitic inductance.

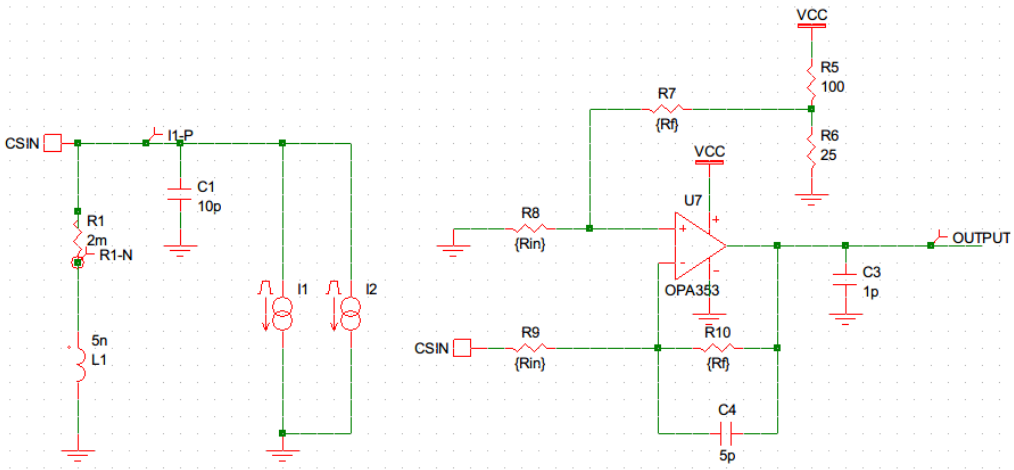


Figure 3.5. Schematic diagram for evaluating the effect of the parasitic inductance.

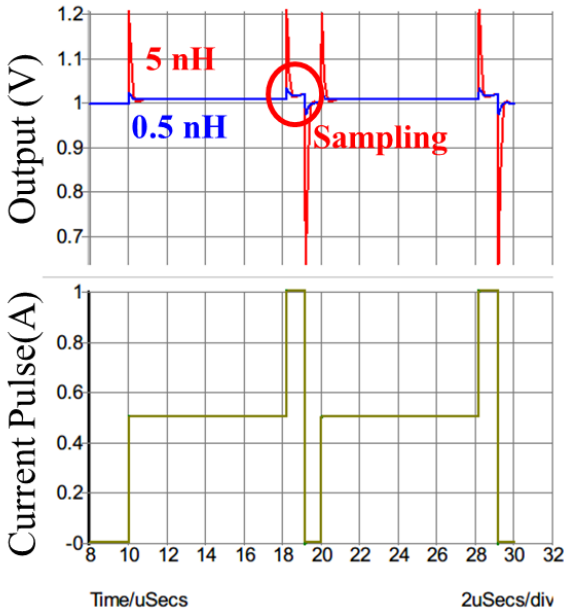


Figure 3.6. Simulated waveforms for evaluating the effect of parasitic inductance.

3.6. Averaged Equivalent Resistance Estimation

In order to predict the conduction loss, the average equivalent resistances of synchronous buck DC-DC converters with various resistive sensing methods are analyzed. The derivation of the equivalent resistance of the proposed method $R_{eq,prop}$ is described in Section 3.3. Note that the on-resistance of the low-side switch with the conventional methods are represented as $R_{LS,total}$ in this section to equivalently compare R_{eq} with the proposed method which utilizes Q_{aux} in addition.

Connecting R_{sen} in series with the load as described in Fig. 3.1, namely R_{sen} sensing for convenience, is the most classical approach for current sensing in switched-mode DC-DC converters. The inductor current continuously flows through R_{sen} in this method. Hence, the equivalent resistance of the converter using R_{sen} sensing is given as:

$$R_{eq,Rsen} = D_{ON} R_{HS} + D_{OFF} R_{LS,total} + R_{DCR} + R_{PCB} + R_{sen}. \qquad (9)$$

Inductor DCR and R_{ds} sensing do not require R_{sen} in the current branch because they use parasitic resistances of the inductor or MOSFET. Although inductor DCR sensing requires RC network connected in parallel with the inductor to provide matching of the time constant, it does not affect to the equivalent resistance because most of the current flows through the inductor. It should be considered that using inductor DCR sensing, DCR value of the inductor should be designed to be large to obtain noise immunity [16]. Hence, the equivalent resistance of the converter using inductor DCR sensing is given as:

$$R_{eq,DCR} = D_{ON} R_{HS} + D_{OFF} R_{LS,total} + R_{DCR,sen} + R_{PCB}, \quad (10)$$

where $R_{DCR,sen}$ is a DCR value which is sufficiently large to obtain noise immunity for current sensing.

Nevertheless neither an additional sensing resistor nor the inductor selection constraint exists in R_{ds} sensing; hence, the equivalent resistance of the converter using R_{ds} sensing is given as:

$$R_{eq,Rds} = D_{ON} R_{HS} + D_{OFF} R_{LS,total} + R_{DCR} + R_{PCB}. \qquad (11)$$

Resistance values utilized in this numerical estimation are as follows: D_{ON} = 0.083, D_{OFF} = 0.917, R_{HS} = 6.7 mΩ $R_{LS,total}$ = 1.8 mΩ, R_{DCR} = 0.2 mΩ, $R_{DCR,sen}$ = 0.7 mΩ, R_{PCB} = 0.19 mΩ. Equivalent resistances of each current sensing method derived from (5), (9)-(11) are described in Fig. 3.7 under R_{sen}=0.8 mΩ. The horizontal axis represents the sampling duty cycle defined in (1) to evaluate the merit of lowered R_{eq} of the proposed method. It is assumed that Q_{LS} and Q_{aux} are the same MOSFETs: R_{LS} = R_{aux} = 2 $R_{LS,total}$, for simplicity.

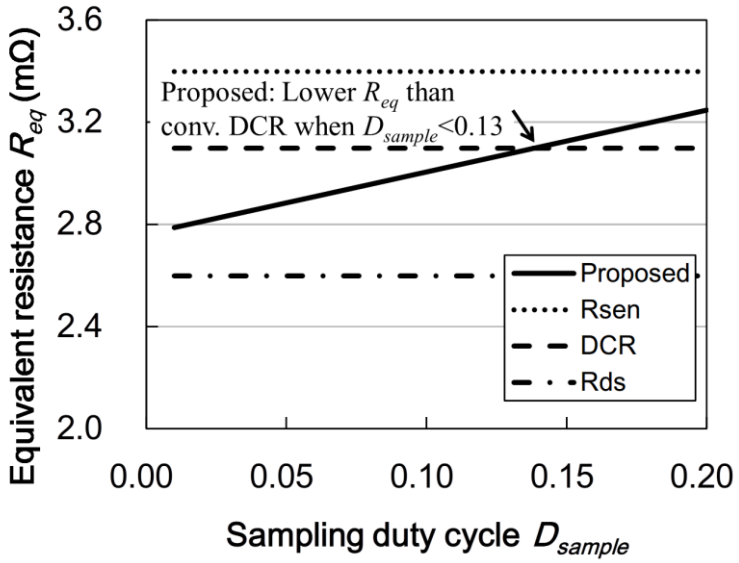
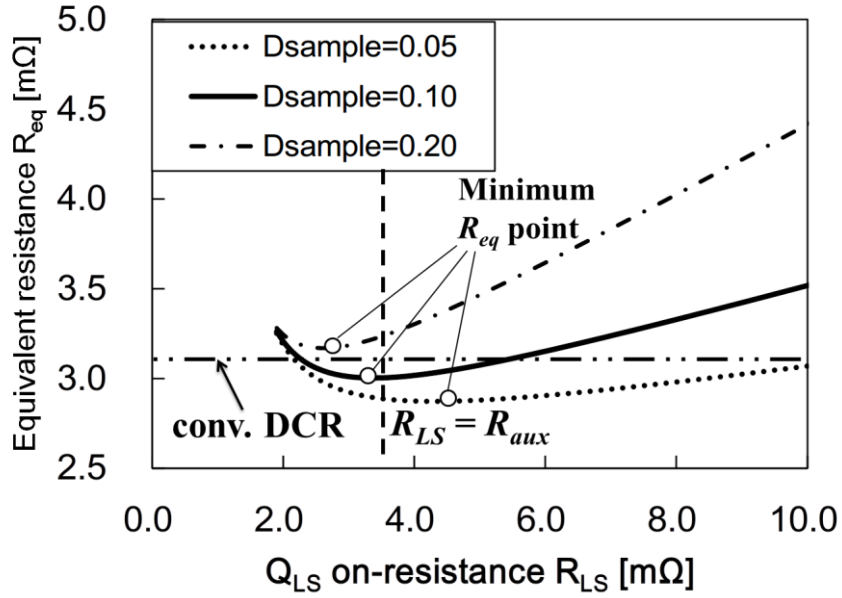


Figure 3.7. The averaged equivalent resistance of the proposed method as a function of the sampling duty cycle D_{sample} [25].

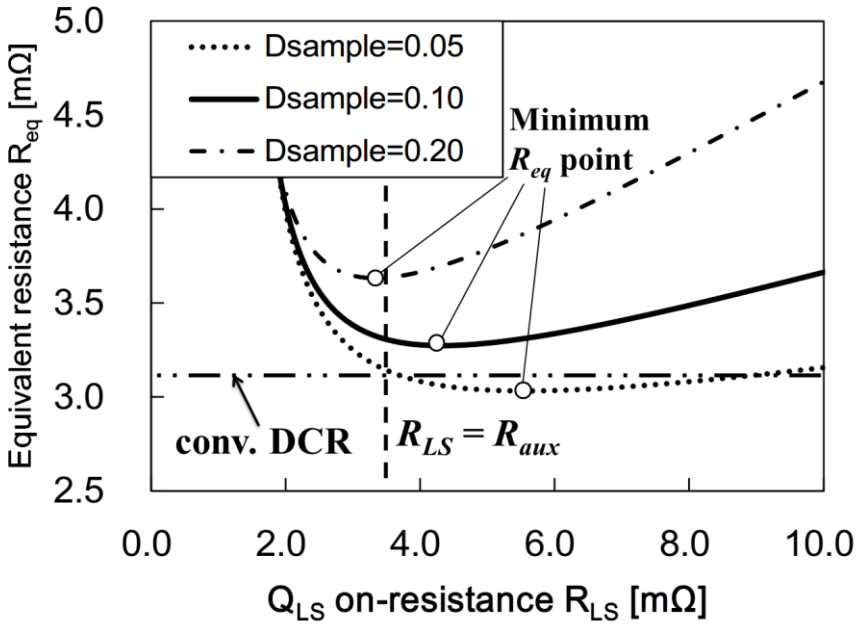
Conventional R_{sen}, inductor DCR and R_{ds} sensing have R_{eq} of 3.4 mΩ, 3.1 mΩ and 2.6 mΩ, respectively. In the proposed method, the equivalent resistance intensively depends on D_{sample} since as D_{sample} decreases, the duration that Q_{aux} is on lengthens. When D_{sample} is lower than 0.13, the equivalent resistance with the proposed method becomes even lower than that with the conventional inductor DCR sensing. In the case D_{sample} = 0.13, T_{sample} becomes 1.3 μs assuming that the switching frequency is 100 kHz. This is feasible to sample the current signal with ADCs with an acquisition time of ~1 μs. It suggests that the proposed method can lower the loss with an acceptable cost for practical applications such as VRMs, battery chargers, power management ICs and etc.

In order to further reduce the loss, the design methodology of MOSFETs in the proposed method is clarified. Since the auxiliary switch Q_{aux} can be regarded as another low-side switch, R_{HS} and $R_{LS,total}$ can be determined by minimizing the sum of all losses such as conduction loss, switching loss and overlap loss. This is a similar manner utilized in the design of common switched-mode DC-DC converters as described in [28]. After R_{HS} and $R_{LS,total}$ are determined, the equivalent resistance can be calculated.

The equivalent resistance of the proposed method as a function of R_{LS} given by (5)-(8) is plotted in Fig. 3.8 with D_{sample} values of 0.05, 0.10 and 0.20. R_{eq} of the converter using the conventional DCR sensing is also indicated for comparison. Finding the minimum R_{eq} point, the optimum R_{LS} and R_{aux} can be determined which will be useful to select Q_{aux} and Q_{LS}. In the case of R_{sen} = 0.8 mΩ as described in Fig. 3.8(a), the optimum combinations of {R_{LS}, R_{aux}} are calculated as {4.3 mΩ, 3.1 mΩ}, {3.4 mΩ, 3.8 mΩ} and {2.6 mΩ, 5.9 mΩ} for D_{sample} are 0.05, 0.10 and 0.20, respectively. The optimum R_{LS} decreases and R_{aux} increases with the increase of D_{sample} because the duration which Q_{aux} is on decreases. When R_{LS} = R_{aux} and D_{sample} = 0.10, R_{eq} is 3.0 mΩ which is nearly equal to the minimum R_{eq}, consequently the same MOSFET should be selected as Q_{LS} and Q_{aux} to reduce Bill Of Material (BOM) cost and complexity. It is worth noting that in the case R_{sen} is relatively large as 2.0 mΩ, the impact of the optimization of R_{LS} and R_{aux} becomes more significant as described in Fig. 3.8(b). Applying the proposed method, R_{eq} of 3.0 mΩ can be obtained by designing the {R_{LS}, R_{aux}} as {5.6 mΩ, 2.7 mΩ} with D_{sample} = 0.05, which is slightly lower than the conventional inductor DCR sensing even when R_{sen} is large.



(a)



(b)

Figure 3.8. The equivalent resistance of the proposed method as a function of the on-resistance R_{LS} with (a) Rsen = 0.8 mΩ and (b) Rsen = 2.0 mΩ [25].

The noise immunity is an also critical demand of resistive current sensing circuits because the current signal is often in the order of 1 mV to 50 mV. A solution to establish the system tolerant to the noise is to increase the resistance of sensors; nonetheless, it increases the conduction loss. The equivalent resistance of the proposed method which is optimized by the above-mentioned scheme is described in Fig. 3.9 as a function of R_{sen} under D_{sample}=0.10. The slope of the equivalent resistance with the proposed method is 0.14 mΩ/mΩ while that with the conventional R_{sen} sensing is 1.0 mΩ/mΩ, which validates the effectiveness of the loss reduction strategy of the proposed method. The equivalent resistance with the proposed method is 4.4 mΩ when R_{sen} = 10 mΩ which is 65% lower than that with the conventional method. This result implies that in addition to improve the noise immunity, current sense amplifiers which is often utilized to obtain approximately 10 mV/mV gain can be removed with the proposed method.

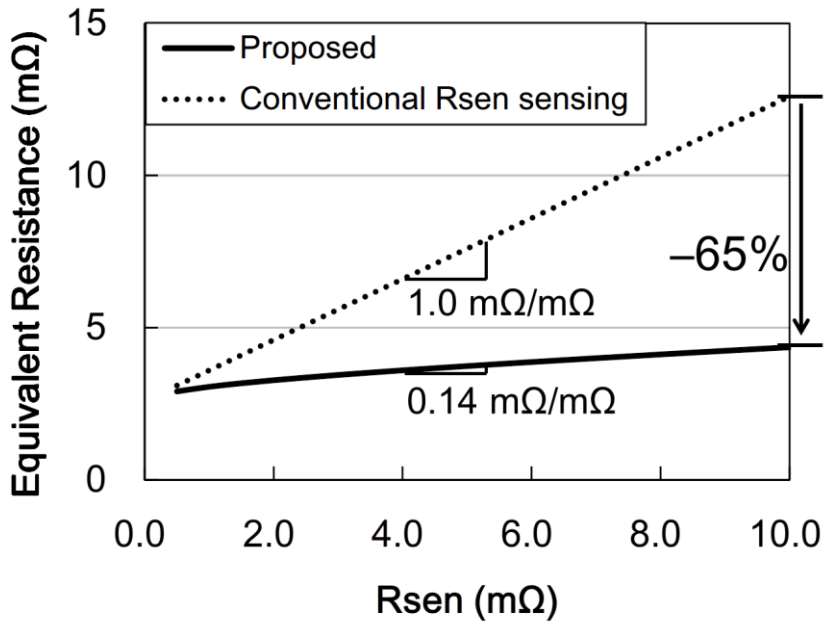


Figure 3.9. Optimized equivalent resistance of the proposed method as a function of sensing resistance under D_{sample}=0.10 [25].

3.6.1. Accuracy

For resistive sensors, keeping high accuracy over a wide temperature range is critical for increasing system reliability. For the sake of comparison, a simple estimation is performed for evaluating the accuracy. Assuming that the resistance of the sensor is a maximum allowable value in the given component tolerance, the resistance change rate from the desirable value including temperature dependence is expressed by the following equation:

$$\Delta = (1 + \varepsilon) \{1 + TC\,(T\text{-}T_{nom})\}, \qquad (12)$$

where ε is a component tolerance, TC is a temperature coefficient, T is an ambient temperature, and T_{nom} is a nominal temperature. The resistance change rates of resistive sensors with typical specifications calculated from (12) are described in Fig. 3.10 as a function of the temperature. The nominal temperature is 20°C. The accuracy of the sensing resistor is as small as 1% at 125°C while the inductor DCR and MOSFET R_{ds} are 48% and 56%, respectively. Because of the small component tolerance and temperature dependence, the sensing resistor does not require any external temperature compensation circuits and calibration circuits. Accordingly, the proposed method using the sensing resistor is an appropriate choice for applications which requires high reliability.

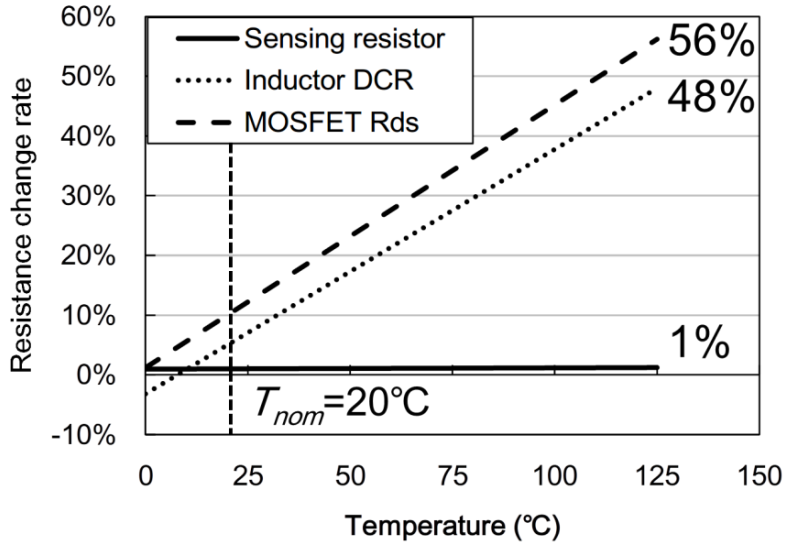


Figure 3.10. The temperature dependences of the resistance change rate of various resistive sensors varied from the desired value [25].

3.6.2. Comprehensive Benchmark

Various resistive sensing methods are benchmarked considering both loss and accuracy based on the results of the estimation described in the previous subsection. The benchmark of the resistive sensing methods is described in Fig. 3.11. The horizontal axis shows the accuracy at 125 ℃, which is the temperature condition where the deviation of the resistance value of the sensor from the desirable value is the maximum in general electronic equipment, that is, the worst case temperature condition. The vertical axis represents the whole conduction loss of switched mode DC-DC converters calculated from (4) when $I_{L,RMS}$ = 20 A. In this benchmark, R_{sen} is 2.0 mΩ and D_{sample} is 0.10. The conduction loss with the proposed method is 28% lower than that with the conventional R_{sen} sensing keeping high accuracy of 1%, because the proposed method utilizes the sensing resistor with the loss-reduction scheme. Furthermore, the accuracy with the proposed method is improved by 47% in compared with that with the conventional inductor DCR sensing with a slightly higher conduction loss. Hence, current sensing circuit providing accurate and low-loss features which is sufficiently applicable for future power management applications including VRMs can be realized with the proposed method.

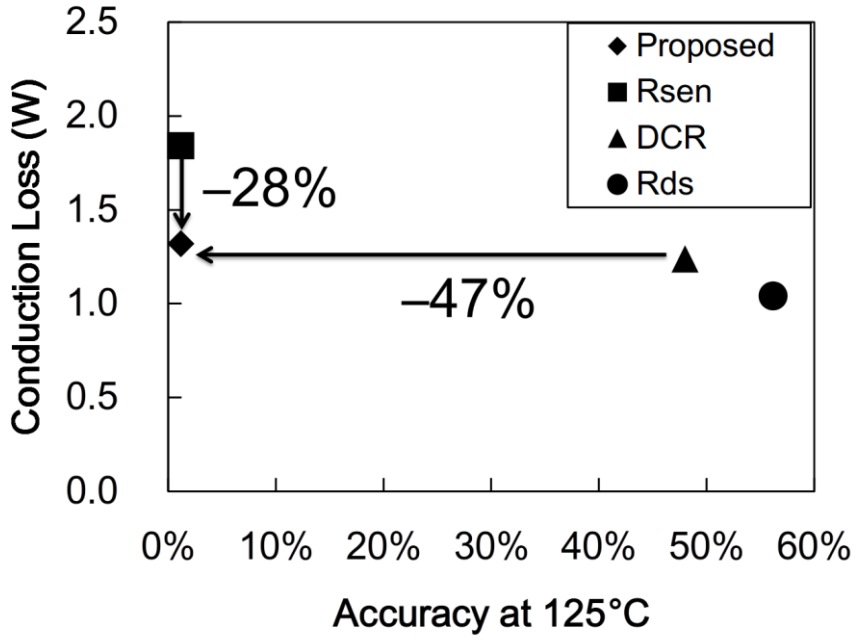
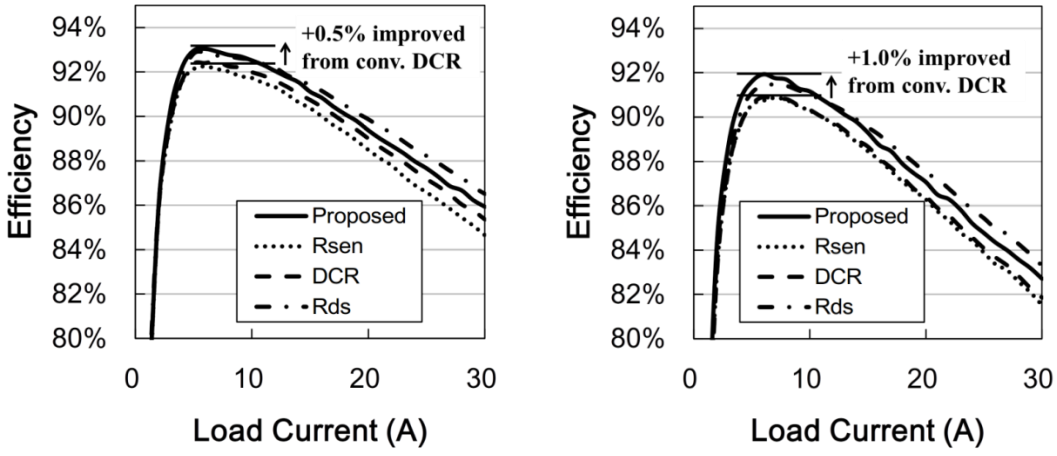


Figure 3.11. Benchmark of various resistive sensing methods [25].

3.6.3. Efficiency Evaluation

To validate the effectiveness of the proposed method, transient simulations of 12 V-to-1.0 V single-phase synchronous buck DC-DC converters with various resistive sensing methods are carried out on Hspice. Parameters utilized in this simulation are as follows: V_{IN}=12 V, V_{OUT}=1.0 V, f_{SW} = 300 kHz, L = 230 nH. The parameters of resistive components of R_{sen}, R_{DCR}, $R_{DCR,sen}$, R_{PCB} are same to the previous subsections. The MOSFET models of RJK0305DPB is utilized as a high-side switch, and RJK0452DPB are utilized as low-side and auxiliary switches. The temperature coefficients of R_{sen} and inductor DCR are 20ppm/°C and 3900ppm/°C, respectively. The efficiency curves from 0 A to 30 A at 25°C and 125°C are plotted in Fig. 3.12. The converter is evaluated under Continuous Current Mode (CCM) and closed-loop operation. At 25°C, the peak efficiency with the proposed method is 93%, which is 0.5% higher than that with the conventional DCR sensing. The peak efficiency improvement with the proposed method in compared with the DCR sensing is further improved to 1.0% at the high-temperature of 125°C due to the difference of inductor DCR value which is greatly dependent on the temperature.



(a) **(b)**

Figure 3.12. Efficiencies of synchronous buck DC-DC converters with various current sensing methods from 0 A to 30 A at (a) 25°C and (b) 125°C [25].

3.7. Experimental Results

The prototype current sensing circuit implemented in the synchronous buck DC-DC converter with 12 V input- and 1.0 V output-voltage, load current up to 20 A, applying the proposed method is designed and constructed to demonstrate the current sensing with the proposed loss-reduction operation. The experimental setup is described in Fig. 3.13. The power stage of the synchronous buck converter is digitally controlled by Xilinx Spartan-6 FPGA under CCM operation with digital voltage mode control. The high-side, low-side and auxiliary switches are SIRA00DP, and the MOSFET drivers are ISL6609A. WSR31L000FEA is used as the sensing resistor, and it has 2.0 mΩ resistance, 1% tolerance and 20ppm/°C temperature coefficient. The voltage across the sensing resistor is amplified by the operational amplifier OPA353, and its output signal is digitalized using 12 bit ADC AD7492. The switching frequency is 100 kHz, inductance is 2.2 μH, and total output capacitance is 2 mF. In this thesis, as is widely recognized in the relevant field, we evaluated the effect of the load of the DC - DC converter equivalently by using the electronic load ELS-304 instead of the microprocessor.

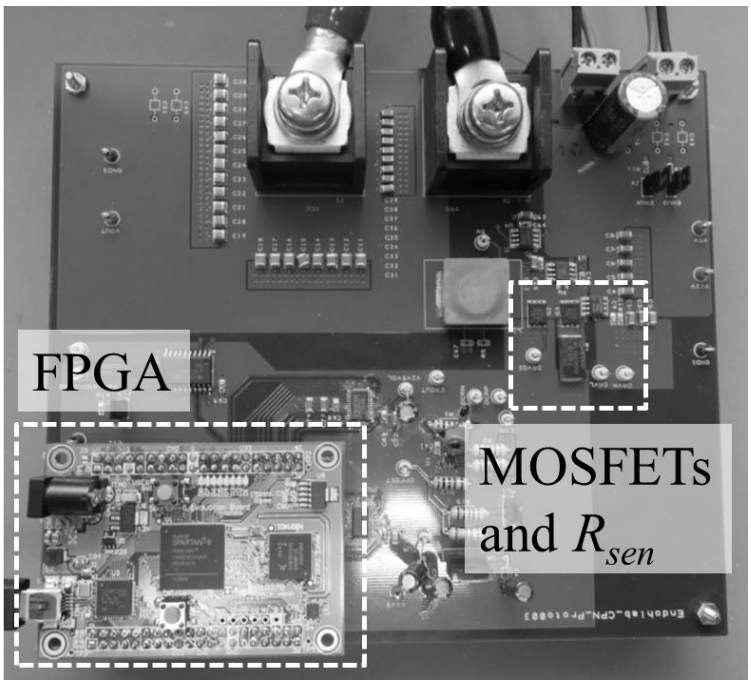


Figure 3.13. Experimental setup [25].

The measured gate driving voltage waveforms of the high-side, low-side and auxiliary switches are described in Fig. 3.14. The high-side and low-side switches are controlled by non-overlapping and level-shifted gate driving voltages generated by the FPGA and the MOSFET driver. The gate driving signal of the auxiliary switch is generated by the simple algorithm which forces to turn off the auxiliary switch 1.0 μs before the next switching cycle, thereby keeping T_{sample}=1.0 μs and D_{sample}=0.10.

The measured waveforms of the current sensing signal and the estimated digital current value at the load current I_O=20 A is described in Fig. 3.15. While the auxiliary switch is off and the low-side switch is on, the inductor current is concentrated to the branch with the low-side switch, and it can be observed as the increase of the current sensing signal 1.0 μs before the next switching cycle. The estimated current value is represented by 12 bit hexadecimal numbers (HEX). It is confirmed that the current value is sampled in every switching cycle. The measured average value of the output code within a range from 0 A to 20 A load is described in Fig. 3.16. The output code has a good linearity, which indicates that the current signal is sampled accurately during the proposed operation. The measured Least-Significant Bit (LSB) of the current sensing circuit was 33.8 LSB/A, which corresponds to +3.3% of the calculated value 32.8 LSB/A. (Note: This is calculated from the resistance, amplifier gain and the LSB of the ADC.)

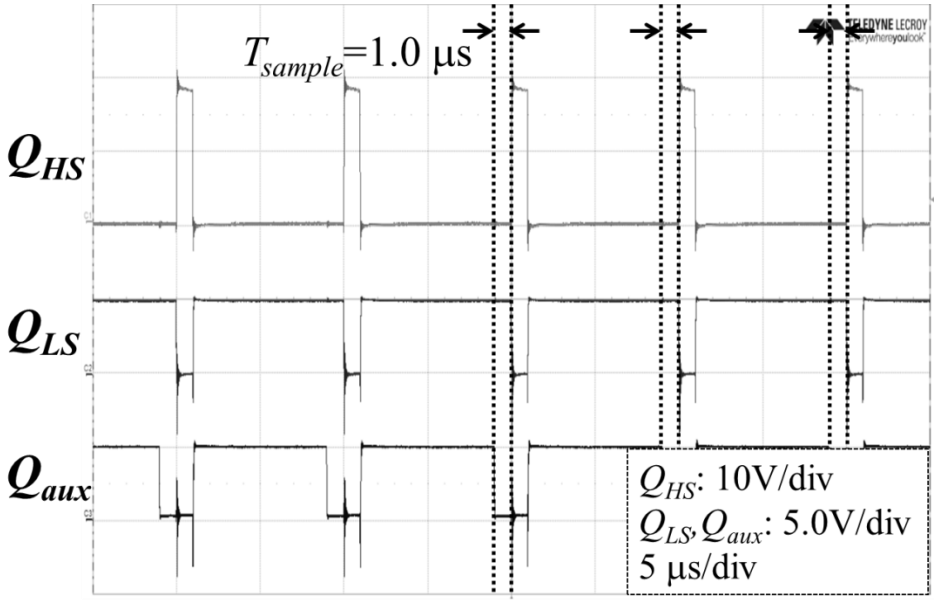


Figure 3.14. The measured gate driving voltages of high-side, low-side and auxiliary switches [25].

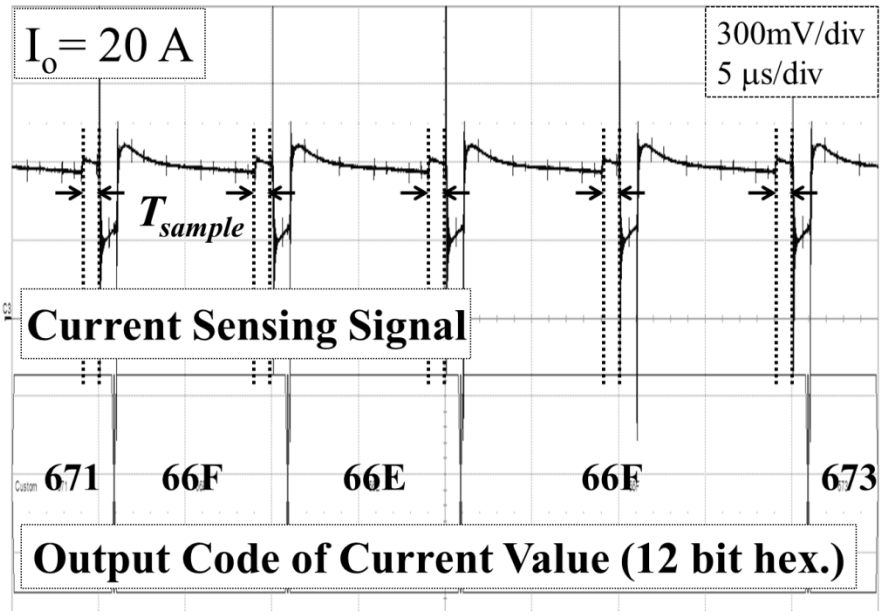


Figure 3.15. The measured waveforms of the current sensing signal and the estimated digital current value at I_O=20 A [25].

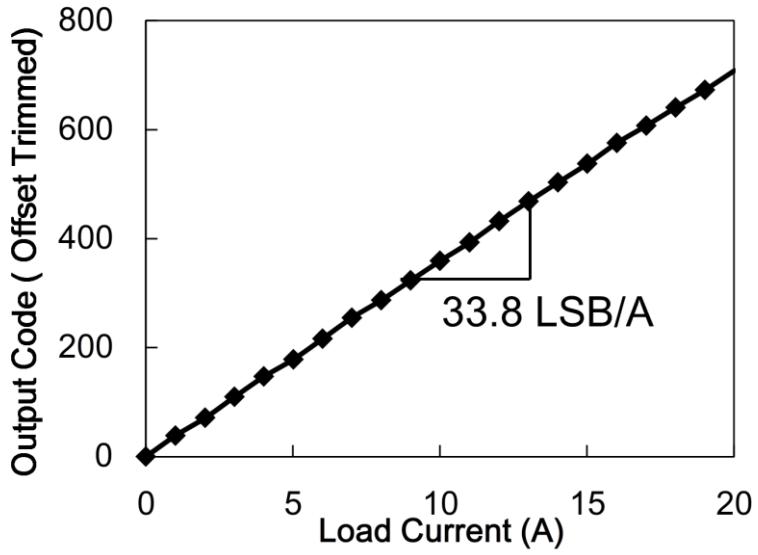


Figure 3.16. The average measured value of the output code of the prototype current sensing circuit from 0 A to 20 A load current represented in decimal [25].

3.8. Conclusion

Current sensing method with high accuracy and low-loss features utilizing sensing resistor is proposed. The proposed method utilizes an auxiliary switch to suppress the conduction loss in the sensing resistor. A parametric estimation using typical specifications of resistive sensors is performed in terms of the averaged equivalent resistance and accuracy, which suggests the importance of designing sampling duty cycle small in the proposed method. The benchmark result based on the parametric estimation indicated that the proposed method with sampling duty cycle of 0.10 can archive 47% higher accuracy with a slightly higher conduction loss in compared with the conventional inductor DCR sensing.

Furthermore, the prototype current sensing circuit applying the proposed method is constructed on the digitally controlled synchronous buck DC-DC converter with 12 V input- and 1.0 V output-voltage, load current up to 20 A. The proposed sensing sequence was experimentally verified. The digital output of the current sensing circuit has a good linearity within a load range from 0 A to 20 A, and the measured LSB was 33.8 LSB/A which is +3.3% from the ideal value. From the above, the current sensing circuit with the proposed method is a promising candidate for future DC-DC converter applications including VRMs.

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Chapter 4

Power Management System Using Switch Toggling Technique for Equalizing Thermal Distribution in Power Electronic Circuits

4.1. Introduction

In recent years, power consumption constraint in IT systems became very stringent. For example, in battery-powered application like smartphones and tablet PCs, long battery life is one of the most significant commercial values. Low power operation is of course essential also in desktop or server systems for energy saving.

In IT systems, power electronic circuits are operated in light load condition whose load current is much less than maximum load in majority of time. Remarkably in light load, efficiency of power electronic circuits is degraded less than several tens of percent from peak efficiency. Thus, to achieve low power operation, improving light load efficiency in power electronic circuit such as buck converters is appreciable effective approach.

Adaptive control techniques are under development for light load efficiency improvement. In adaptive control, circuit parameters such as switching frequency, MOSFET gate drive voltage and etc. are dynamically modulated adaptive to load current level. The critical matter for adaptive control design is to achieve high efficiency without sacrificing other key features like ripple voltage level and circuit area.

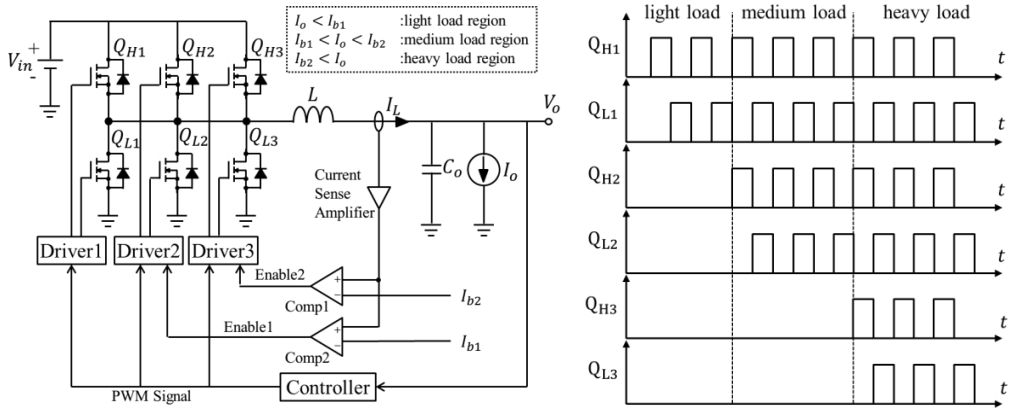
The switching frequency modulation is a practical way because switching loss and gate loss are scaled down with switching frequency [1]. Nonetheless, ripple voltage level is increased inversely proportional to switching frequency, and Electronic Magnetic Interference (EMI) design becomes more challenging.

The gate voltage modulation is also effective because gate loss is proportional to square of gate voltage [2]. Nonetheless, its implementation becomes more complicated to generate a couple of gate drive voltage.

In adaptive control with many parallel MOSFET such as Adaptive FETs Modulation (AFM) [3] and width segmentation scheme [4], a couple of MOSFETs are connected in parallel and the number of driven MOSFETs is modulated. In Fig. 4.1, conventional parallel MOSFET topology with adaptive control is described [3]. These techniques are promising because switching frequency can be designed to be constant, and it is unnecessary to generate a couple of gate drive voltage.

Nonetheless, a principle of thermal design for these techniques has never given yet. Thermal design is very critical for power electronic circuits because reliability of power MOSFETs severely degrades when junction temperature exceeds 100°C. When MOSFETs are connected in parallel, heat generation in each MOSFET becomes nonequivalent, hence the thermal design becomes more complicated [5,6].

In this chapter, heat generation concentration in parallel MOSFET topology with adaptive control is analyzed. Furthermore, a novel switch toggling technique for parallel MOSFET topology is proposed to achieve uniform thermal distribution.



(a) (b)

Figure 4.1. (a) Schematic and (b) key waveforms of conventional parallel MOSFET topology [3].

4.2. Heat Generation Concentration Issue in Parallel MOSFET Topology

In conventional adaptive control, the number of driven MOSFET is modulated to optimize parasitic capacitance and resistances of MOSFETs for maximizing the efficiency over a wide load range. In conventional adaptive control described in Fig. 4.1, one of the MOSFET drivers is always enabled, and the others are only enabled when the load current exceeds boundary current value I_{b1} and I_{b2}, in other words, changes from light load to medium or heavy load [3].

Nonetheless, this technique has an unsuitable aspect for light load operation. Conduction loss in parallel MOSFET topology can be expressed as follows,

$$P_{conduction} = R_{ds} I_o^2 / n_{driven} \quad (1),$$

where R_{ds} is on resistance of MOSFET, and I_o is load current, and n_{driven} is the number of driven MOSFET. In Fig. 4.2, normalized loss in each MOSFET by maximum value numerically calculated from eq. (1) is described. The load current range is from 10 A to 100 A and the boundary current values are 33 A and 66 A for low voltage high current buck converter assumption. In this case, three MOSFETs with 3.5 mΩ on resistance R_{ds} are connected in parallel. It can be seen that the loss near at boundary current is 98% of the loss at the maximum load. From this profile, it is expected that a couple of severe problems occur in thermal design.

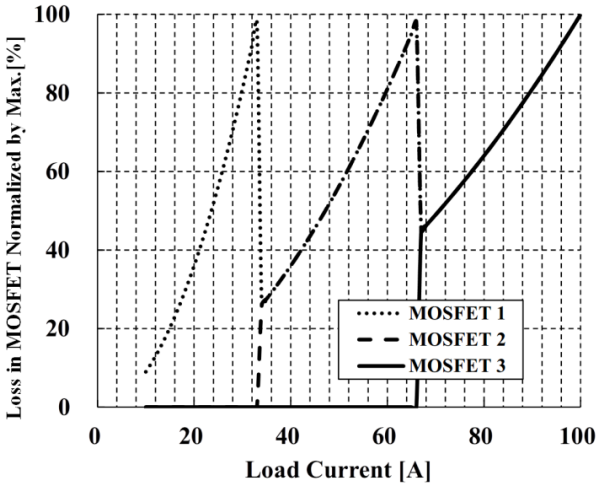


Figure 4.2. Loss in each MOSFET normalized by maximum value in parallel MOSFET topology [14].

Firstly, near at the boundary current, large heat generation occurs in driven MOSFET. Accordingly, special thermal design is needed to endure the peak heat generation. Secondly, in MOSFETs which is driven only in medium or heavy load, large thermal transient occurs between different load regions. The thermal transient incurs harmful thermal cycles. It is well known that frequent thermal cycles lead to failure such as solder cracking due to thermal stress. Thirdly, the efficiency degrades because the on resistance increases with junction temperature increase.

One of effective solution of the problem due to the heat concentration is a thermal connection. Heat pipes are widely used for thermal connection on the mother board, and are mainly used for connecting the semiconductor device and the radiator part of the heat sink [5]. For example, it is reported that a heat pipe with a diameter of 1.28 cm and a length of 50 cm has a very low thermal resistance of 0.3 ℃/ W [6]. However, thermal connection using a heat pipe has problems such as increase in size and cost, design restrictions on motherboard layout, low thermal conductivity between package and mounter. Consequently, a novel technique for achieving uniform thermal distribution of MOSFETs using electrical control is required.

4.3. Proposed Switch Toggling Technique

A circuit diagram of conventional adaptive control is described in Fig. 4.3. In conventional technique, load current comparators are directly connected to drivers. Accordingly, driver1 is always enabled, and driver2 and driver3 are enabled when load current exceeds boundary current I_{b1} and I_{b2} respectively. In this configuration, above mentioned heat concentration problem occurs. In Figure 4.4, circuit diagram of the proposed switch toggling technique is described. In the proposed technique, the toggling block is connected between load current comparators and drivers. A major concept of the proposed technique is to toggle driven MOSFET cycle-by-cycle.

The key waveforms of the proposed technique are described in Fig. 4.5. Fig. 4.5(a) and Fig. 4.5 (b) show the case of one MOSFET is driven and two MOSFETs are driven respectively. In Fig. 4.5(a), each MOSFET is driven once in three switching cycles, hence conduction loss and switching loss are distributed to all the parallel MOSFETs. In this case, the temperature increase of MOSFET is simply expected to be suppressed as much as one-third of conventional technique. It becomes two-third in Fig. 4.5(b) in the same way. Note that when three MOSFETs are driven, the operational sequence becomes identical to conventional technique.

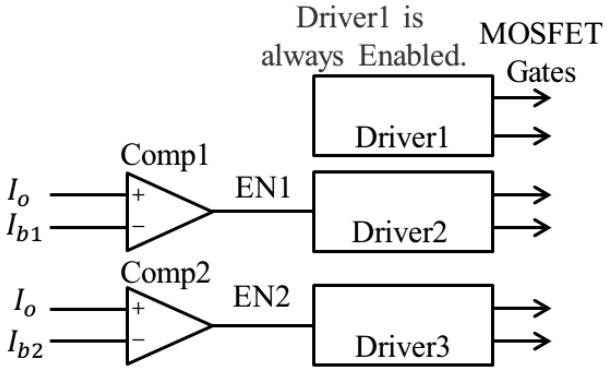


Figure 4.3. Schematic of the controller of conventional AFM technique [14].

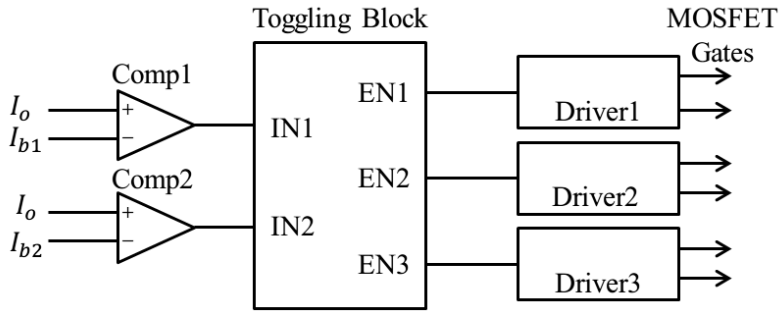


Figure 4.4. Schematic of the controller of the proposed switch toggling technique [14].

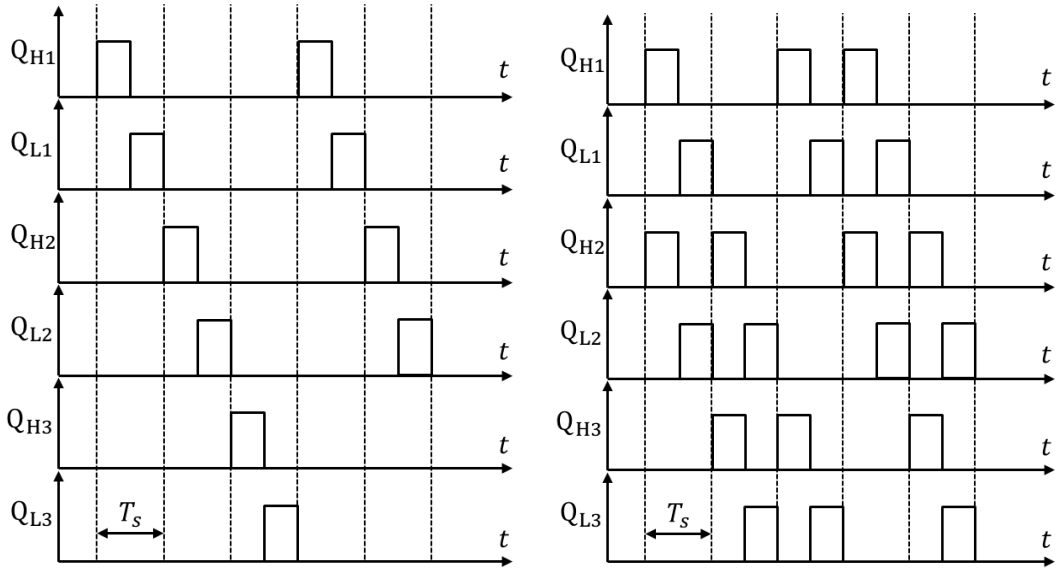


Figure 4.5. Key waveforms for the proposed technique when (a) one MOSFET is driven and (b) two MOSFETs are driven [14].

The toggling block is able to be implemented with simple digital circuit. The toggling signal generator for light load region which one driver is enabled is described in Fig. 4.6. "100" serial signal is generated from switching clock. Then, the signal is input to shift register. Note that 4 bit shift register is utilized for generating sequence for medium load region. Enable signal generator for medium load region which two drivers are enabled is described in Fig. 4.7. Enable signal for medium load region is simply generated from OR gate connected to the output of shift register.

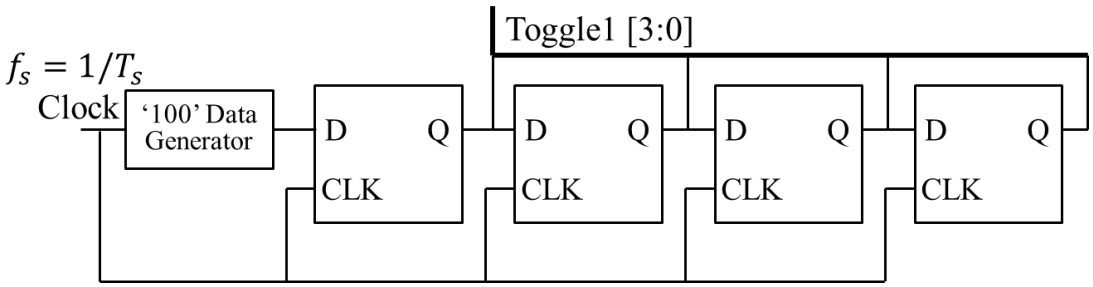


Figure 4.6. Schematic of enable signal generator for the light load region [14].

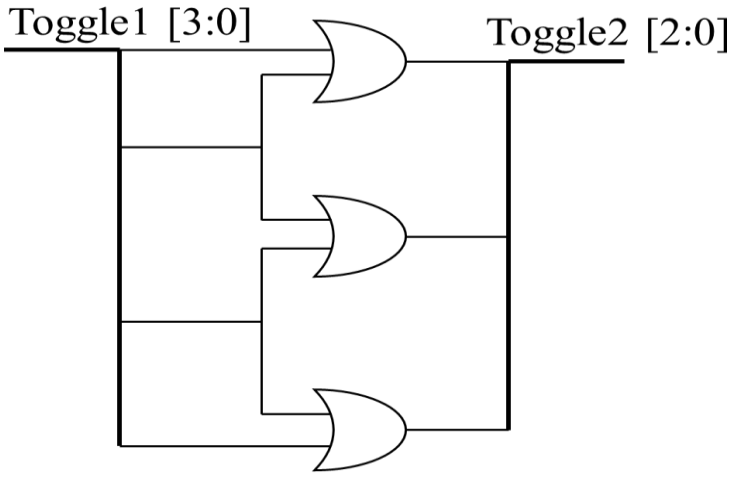


Figure 4.7. Schematic of enable signal generator for the medium load region [14].

In Fig. 4.8, load region selection circuit is described. Each sequence is selected by MUX controlled by load region signal S0 and S1. The input for the case when S0 is 1 and S1 is 0 is grounded. This is because it is not utilized since load current is divided into three regions. Load region signal generator is described in Fig. 4.9. Load current comparator is connected to D flip-flop, consequently the inductor current value at the start of the switching cycle is utilized to decide load region. Hence, load region signal is updated every switching cycle.

These digital circuits have to be operated at switching frequency f_s. In the proposed technique, high performance circuit is unnecessary because f_s is always from several hundreds of kHz to MHz.

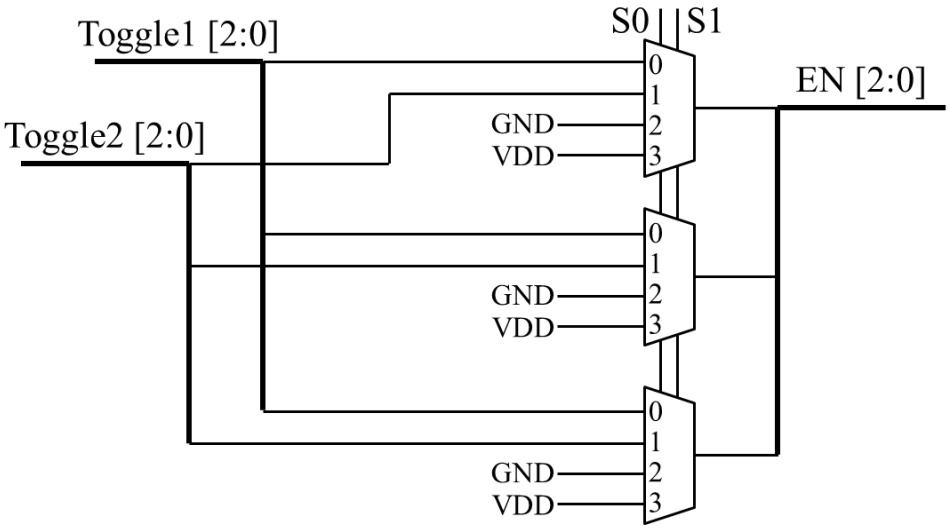


Figure 4.8. Schematic of load region selector circuit [14].

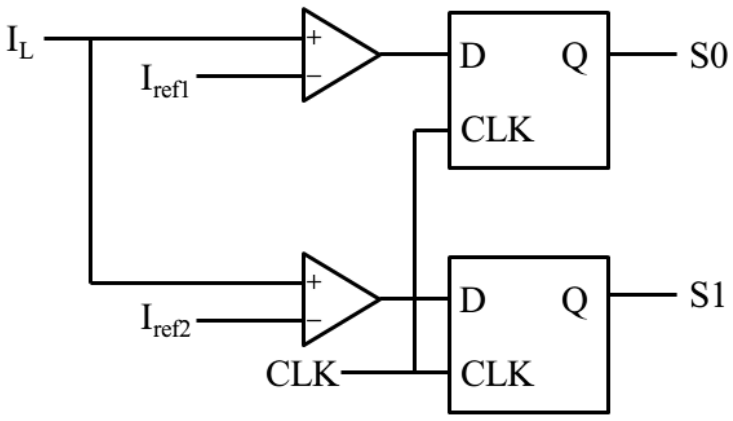


Figure 4.9. Schematic of load region signal generators [14].

4.4. Results and Discussions

A single phase buck converter with three parallel MOSFETs described in Fig. 4.10 is simulated by HSPICE from Synopsys to verify the merit of the proposed technique. Input voltage is 12 V and output voltage is 1.0 V which is regulated by peak current mode control. MOSFET gates are driven from 5.0 V auxiliary power supply. High-side MOSFETs are driven with bootstrap driver because these MOSFETs are n-channel. The parameters of the simulated circuit are described in Table 4.I. SPICE models of MOSFET from Renesas [9,10] are utilized, and digital circuit is simulated with TSMC 0.18 µm model [11]. Conduction loss, switching loss, gate loss and which are measure losses in power electronic circuits are taken into account in this simulation.

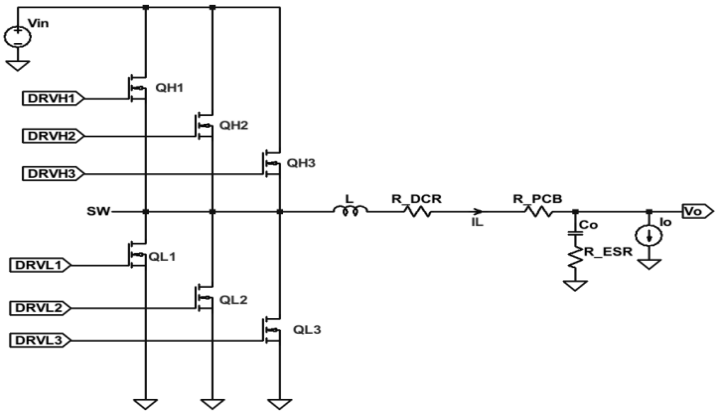
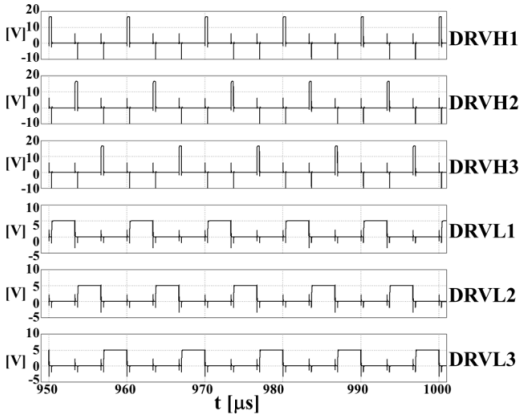


Figure 4.10. Schematic of simulated 12 V to 1.0 V buck converter constructed with three MOSFETs that are operated with conventional and proposed techniques [14].

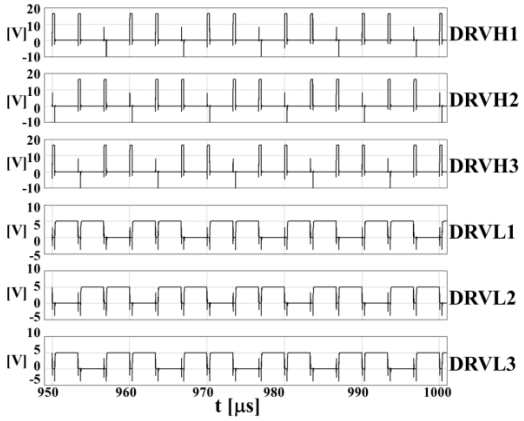
Table 4.I. Parameters of the simulated buck converter [14].

Symbol	Description	Value
V_{in}	input voltage	12 V
V_{5V}	input voltage	5.0 V
V_o	output voltage	1.0 V
L	inductance	230 nH
R_{DCR}	inductor DC resistance	0.2 mΩ
C_O	output capacitance	2.48 mF
R_{ESR}	capacitor ESR	0.15 mΩ
R_{PCB}	PCB trace resistance	0.2 mΩ
Q_{H1}-Q_{H3}	high-side MOSFETs	RJK0305DPB
Q_{L1}-Q_{L3}	low-side MOSFETs	RJK0452DPB
f_s	switching frequency	300 kHz
Ib1	boundary current	22.5 A
Ib2	boundary current	45.0 A

Simulated waveforms are described in Fig. 4. 11(a) and Fig. 4.11(b). Fig. 4.11(a) describes the case of the load current is 20 A that one MOSFET is driven, and Fig. 4.11(b) describes the case of the load current is 40 A that two MOSFET are driven. In Fig. 4.11(a), for both high-side MOSFET gate drive voltage DRVH1~3 and low-side MOSFET gate drive voltage DRVL1~3, MOSFETs are driven once in three switching cycles. In Fig. 4.11(b), high-side and low-side MOSFETs are driven twice in three switching cycles. In the waveforms, drive voltage drops below 0 V when the MOSFET is not driven. This is because high dV/dt of SW node causes charging current in MOSFET gate parasitic capacitance. It has little harmful effect because gate resistance of each MOSFET limits the charging current. Hence it can be said that the MOSFET drive voltages are correctly toggled in each case. The efficiencies are 87.4% and 86.8% when load current values are 20 A and 40 A respectively.



(a)



(b)

Figure 4.11. Gate voltage waveforms under (a) 20 A and (b) 40 A load current [14].

For evaluating MOSFET junction temperature increase, the average value of $V_{ds}I_d$ under circuit operation is evaluated as MOSFET loss inside package P_d because only heat generation in MOSFET package should be considered. Consequently conduction loss, switching loss and etc. are taken into account, but gate loss is excepted because the most of gate loss occurs in external gate resistance and MOSFET drivers which are generally located at the outside of MOSFET package. The amount of junction temperature increase from ambient temperature ΔT is expressed as follows [12],

$$T = P_d \theta_{ja} \qquad (2)$$

where θ_{ja} is junction to ambient thermal resistance. All on-board type MOSFETs utilized in this simulation are packaged in LFPAK.

It is well known that thermal resistance strongly depends on copper area of Printed Circuit Board (PCB). In this estimation, thermal resistance is set to 40 K/W for LFPAK on 20 mm x 20 mm FR4 4-layer PCB with thermal via [13].

The ΔT of each MOSFET for the conventional technique and proposed technique is described in Fig. 4.12 and Fig. 4.13. Fig. 4.12 describes the case when load current is 20 A that is light load region, and Fig. 4.13 describes the case load current is 40 A that is medium load region. For evaluation purpose, conventional technique is also simulated in the same circuit configuration except that QH1 and QL1 is always driven, and the others are not driven in Fig. 4.12. In Fig. 4.13, QH1, QH2, QL1 and QL2 are always driven, and the others are not driven in the same way. In Fig. 4.12, the maximum junction temperature increase of low-side MOSFETs in conventional technique is 58.5 K. With the proposed technique, it is decreased to 24.0 K. From the results, the maximum junction temperature increase of high-side and low-side MOSFETs are suppressed by 64% and 59% when one MOSFET is driven, and 32% and 27% when two MOSFETs are driven respectively. These results indicate that thermal design of the power electronic circuits becomes very simple. Furthermore, small package MOSFETs with large thermal resistance can be selected to implement with small circuit area.

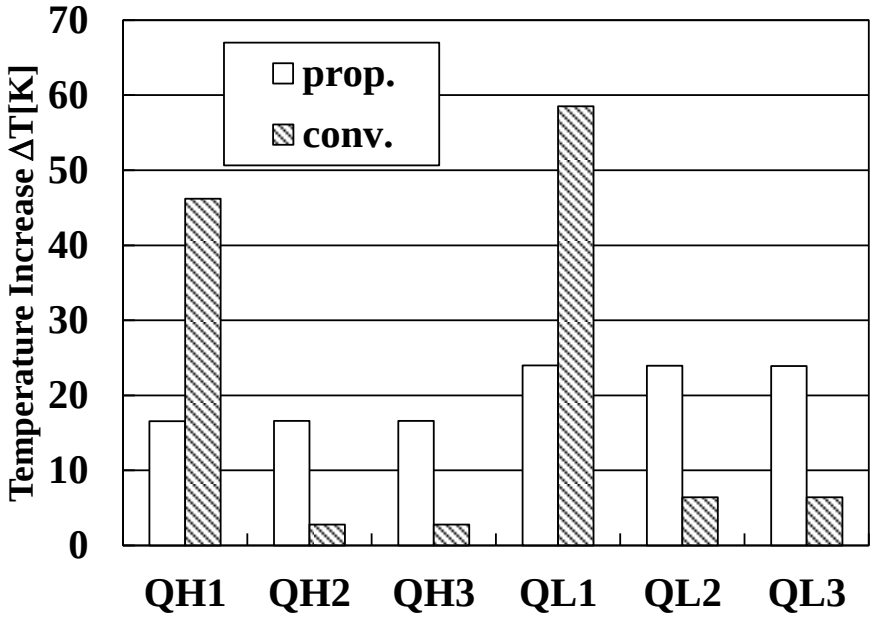


Figure 4.12. Temperature increase ΔT in each MOSFET (QH1~3, QL1~3: See Fig. 3.10.) under conventional adaptive control and proposed switch toggling technique in the case of 20 A load current [14].

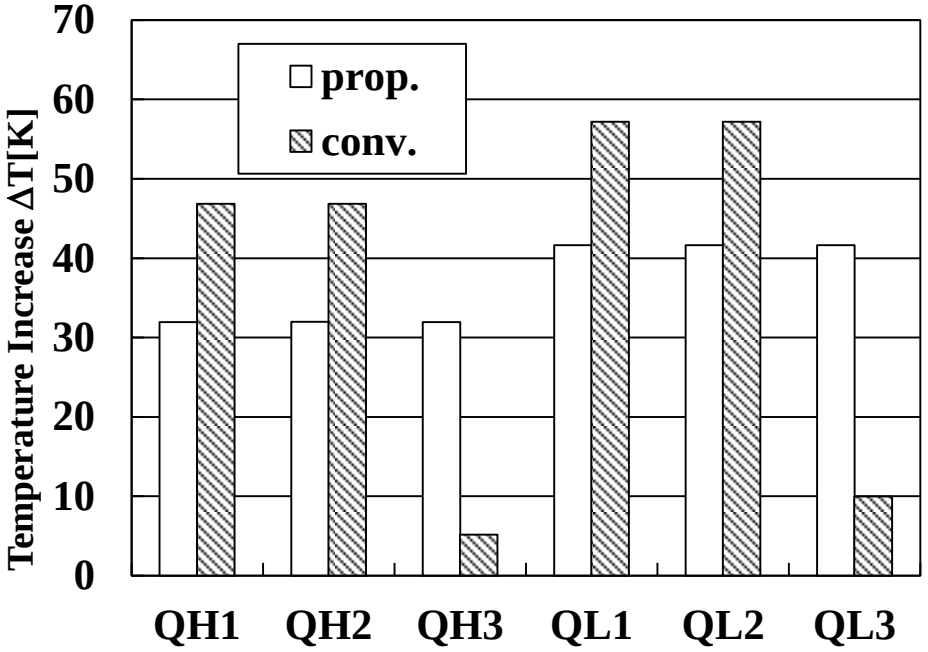


Figure 4.13. Temperature increase ΔT in each MOSFET (QH1~3, QL1~3: See Fig. 3.10.) under conventional adaptive control and proposed switch toggling technique in the case of 40 A load current [14].

4.5. Conclusions

In this chapter, loss in parallel MOSFET topology with adaptive control is analyzed. From numerical estimation, conduction loss in MOSFET at near the boundary current reaches 98% of loss at the maximum load. To overcome this problem, switch toggling technique is proposed and simulated. From the results, in case that three MOSFETs are connected in parallel, maximum temperature increase of high-side and low-side MOSFETs are suppressed 64% and 59% when one MOSFET is driven, and 32% and 27% when two MOSFETs are driven respectively. Furthermore, on resistance of the low-side MOSFET under circuit operation is decreased by 13% because operating temperature of MOSFET is decreased. It is promising result for efficiency improvement of power electronic circuits.

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Chapter 5

Inductor Current to Digital Converter with Small Number of Components for Improving Compactness

5.1. Introduction

Inductor current plays key role in DC-DC converters. Inductor current information obtained from inductor current sensing circuit is utilized for many reasons. In Fig. 5.1, the example of circuit diagram of DC-DC buck converter with current sensing circuit is described. In this case, dedicated current sensing resistor R_{sense} is connected to inductor. The small voltage across R_{sense} is amplified by shunt amplifier, and inductor current signal V_{sense} is converted to digital data by ADC to use in digital controller.

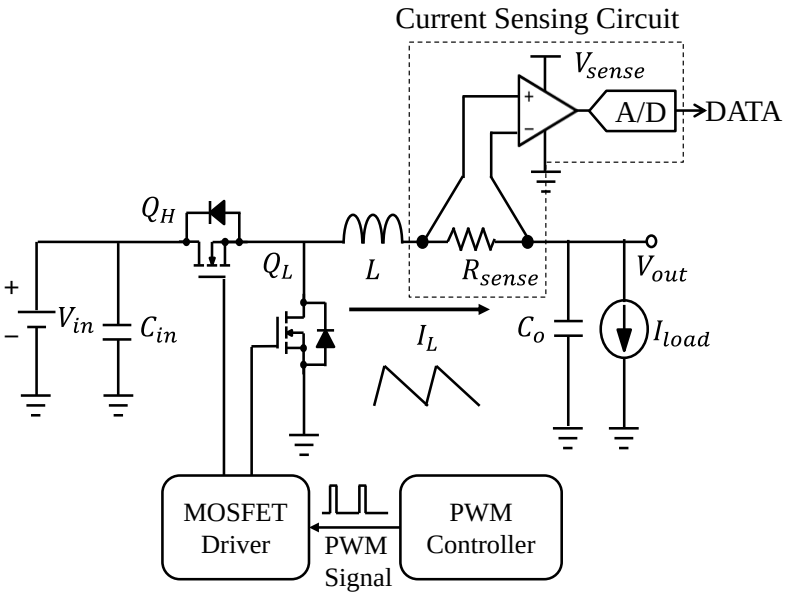


Figure 5.1. Simplified circuit diagram of DC-DC buck converter with current sensing circuit.

In Continuous Current Mode (CCM) operation, inductor current waveform becomes periodic triangle waveform as described in Fig. 5.2. Inductor current consists of two components; DC component I_{DC} which corresponds to average inductor current, and ripple component I_{ripple} which corresponds to peak to peak value of inductor current. Because DC component equals the output current of the DC-DC converter in steady state, it is utilized to over current protection (OCP) for high reliability, current sharing in multi-phase converters, and adaptive control for light load efficiency enhancement [1]. On the other hand, ripple component is also critical because instantaneous inductor current value information is utilized to generate Pulse Width Modulation (PWM) control signal. For example, ripple component information is utilized in many control techniques such as current mode control and hysteresis control [2-4].

Recently, digitally controlled high frequency DC-DC converters have been developed for the merits of controller flexibility, improved performance, and programmability. In many digitally controlled DC-DC converters, inductor current signal V_{sense} is converted to digital data by ADC. Nonetheless, using classical implementation as described in Fig. 5.3, two channels of ADC were utilized for convert DC component and ripple component separately [5]. In this case, DC component is input through ripple cut-off RC filter to suppress error due to ripple component.

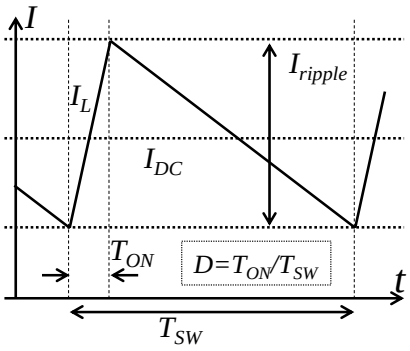


Figure 5.2. DC component and ripple component of inductor current.

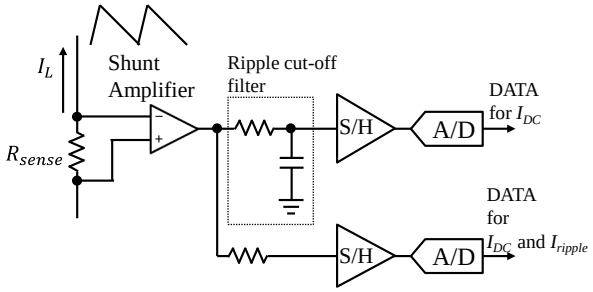
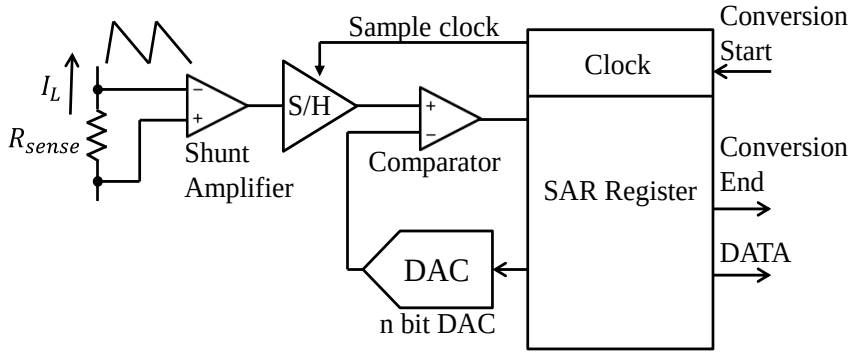
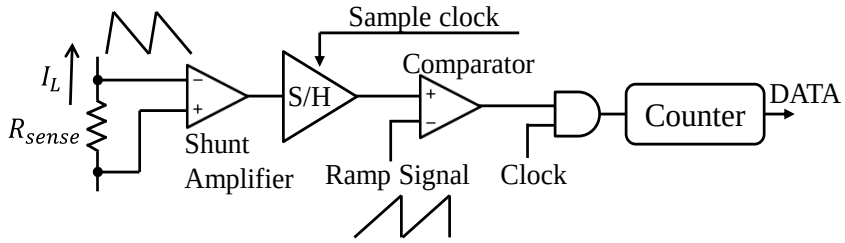


Figure 5.3. Block diagram of the conventional inductor current digitalizing system.

In Fig. 5.4(a), conventional Successive Approximation Register (SAR) ADC is described [6,7]. Once input signal is hold by Sample and Hold (SH) circuit, SAR ADC successively compares input signal with Digital-to-Analog Converter (DAC) output. To convert analog signal to n bit code, n bit DAC is required. In Fig. 5.4(b), conventional Single Slope (SS) ADC is described [8,9]. In SS ADC, input signal is compared with periodic ramp signal by comparator. The pulse duration of the comparator output is detected by counter. The counter output becomes proportional to input signal, hence input signal is converted to digital data. SS ADC is quite simple topology, nonetheless its conversion time becomes large for counting pulse duration. Because SAR and SS ADC convert instantaneous value of input signal, it is challenging to convert DC and ripple component of inductor current in certain switching cycle with small number of components. The other dedicated techniques to estimate inductor current are also developed [10-12]. Nonetheless additional components such as S/H circuit and low sampling rate ADC is required, and these techniques cannot convert ripple component to digital data. Accordingly, it is an challenge to make digitally controlled DC-DC converters more affordable in conventional implementation.



(a) Successive Approximation Register (SAR) ADC.



(b) Single-Slope (SS) ADC.

Figure 5.4. Conventional AD converters for digitalizing inductor current.

In this chapter, novel Inductor Current to Digital Converter (ICDC) is presented. The proposed ICDC can convert DC and ripple component of inductor current to digital data simultaneously, and it operates with significantly small number of components. Its concept and conversion characteristic for both DC and ripple component are evaluated by SPICE mixed signal simulation.

5.2. Proposed Inductor Current to Digital Converter

In Fig. 5.5, block diagram of the proposed ICDC is described. The concept of the proposed ICDC is to reduce redundancies in conventional implementation with ADC for digitalizing inductor current. The ICDC is composed of comparator, Register for Successive Approximation (SA) operation, coarse DAC, counter, and inductor current estimation logic. To convert inductor current signal to digital data once in switching cycle, falling edge of PWM signal from PWM controller is utilized to start conversion instead of sample clock in conventional ADCs. Because DAC is utilized only for coarse AD conversion performed at the start of operation, required DAC bits can be suppressed in comparison with conventional SAR ADC. The inductor current estimation logic estimates DC and ripple component from transition of comparator output and coarse data from SAR register, accordingly SH circuit is not required.

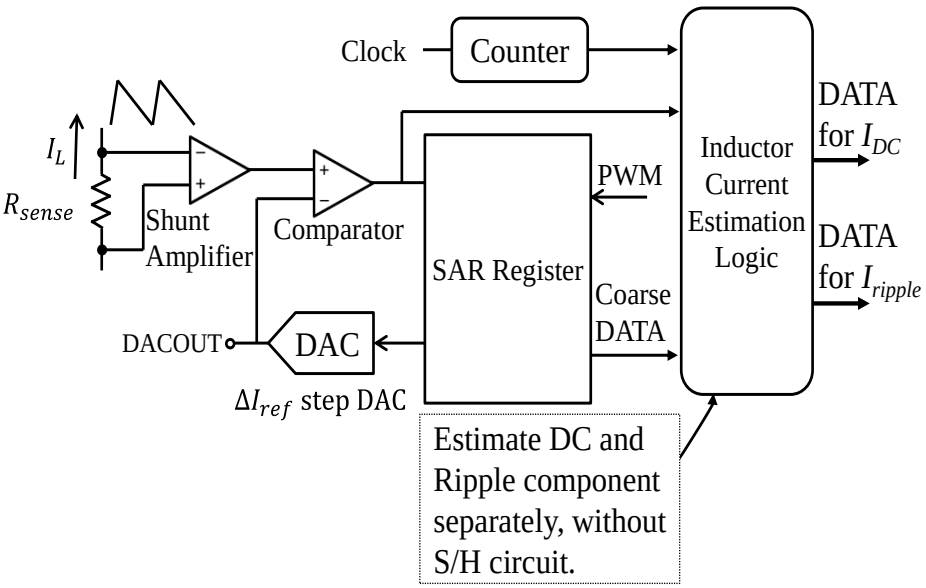


Figure 5.5. Block diagram of the proposed Inductor Current to Digital Converter (ICDC) [13].

In Fig. 5.6, operational principle of the proposed ICDC is illustrated. I_{DAC} indicates current value corresponds to output signal of DAC. In steady state, DC component and ripple component of inductor current in single switching cycle can be expressed as follows:

$$I_{DC} = \frac{I_{ref(i)} - I_{ref(i-1)}}{t_2 - t_1}\left(\frac{t_3}{2} - t_1\right) + I_{ref(i)}$$

$$= \frac{I_{ref}}{t_2 - t_1}\left(\frac{t_3}{2} - t_1\right) + I_{ref(i)} \qquad (1),$$

$$I_{ripple} = \frac{I_{ref(i)} - I_{ref(i-1)}}{(t_2 - t_1)} \quad t_3 \quad (2),$$

where t_1 and t_2 are time at first and second transition of comparator since SAR operation finished, t_3 is time at rising edge of PWM signal, $I_{ref(i)}$ is current value corresponds to DAC output when first comparator transition since SAR operation finished for i=0, 1, ...,7, and I_{ref} is current value corresponds to LSB of DAC. For the sake of clarity, it is assumed that inductor current I_L is converted into 8 bit digital data for I_{DC} and I_{ripple}.

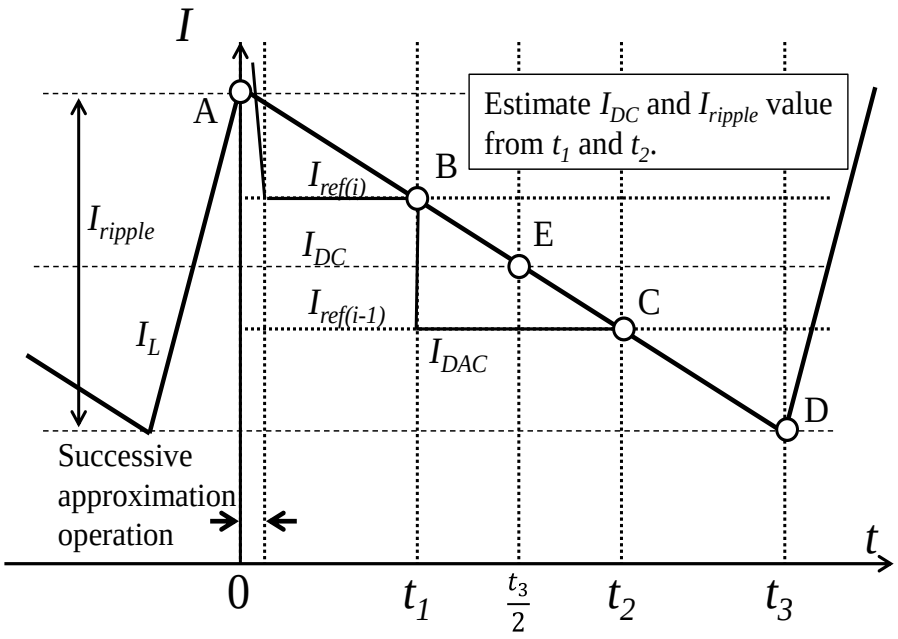


Figure 5.6. Operational principle of the proposed ICDC [13].

The inductor current estimation algorithm in the proposed ICDC is described in Fig. 5.7. n_{SAR} indicates the number of bit of coarse SAR ADC. Firstly, when falling edge of PWM signal is detected, coarse SAR AD conversion begins. To realize both adequate input range and simplicity, n_{SAR} is set to 3. The output coarse data of SAR ADC i is sent to inductor current estimation logic. The relationship between $I_{ref(i)}$ and I_{ref} is given by

$$I_{ref(i)} = i\, I_{ref} \quad (3).$$

Secondly, t_1 and t_2 value is stored to register by detecting counter value at comparator output transition. Then, when rising edge of PWM signal is detected, t_3 is stored. Finally, when falling edge of PWM signal is detected again, eq. (1) and eq. (2) is calculated by inductor current estimation logic, hence I_{DC} and I_{ripple} is converted to digital data.

Because the operation principle of proposed ICDC is different from the conventional ADCs, different design consideration exists. In first, because the inductor current signal must intersect $I_{ref(i)}$ and $I_{ref(i-1)}$ in single switching cycle, I_{ref} is decided by minimum input ripple value as follows,

$$I_{ref} = \frac{1}{2}\, I_{ripple,min} \quad (4).$$

Typical ripple current value of buck converter can be expressed as follows,

$$I_{ripple} = \frac{(1-D)V_{out}T_{sw}}{L} \quad (5),$$

where D is duty cycle, V_{out} is output voltage, T_{sw} is switching period, and L is inductance. Generally, inductance in DC-DC converters has 10-15 % tolerance. Due to the component tolerance, I_{ripple} varies from -13% to 17% from typical value. In this chapter, the input range is designed to convert I_{ripple} from -20% to +20% of typical value.

Then, the conversion range of DC component is decided. When the DC component becomes maximum value, the valley value of inductor current becomes identical to the output of DAC whose input is 1 LSB lower than maximum value. Consequently, maximum input of DC component is expressed as follows,

$$I_{DC,MAX} = (2^{n_{SAR}} - 2)I_{ref} + \frac{I_{ripple}}{2} \quad (6).$$

Theoretical quantization error is decided by clock period because DC and ripple component is finally calculated by using (t_2-t_1) value detected by counter. To convert input signal to n bit data, required clock period t_{clk} is expressed as follows,

$$t_{clk} = \frac{1}{2}\frac{I_{ripple,err}(t_2 - t_1)^2}{t_3 I_{ref} - (t_2 - t_1)I_{ripple,err}} \quad (7),$$

where $I_{ripple,err}$ is quantization error in the ICDC design. In this case, the clock frequency should be larger than 65 MHz clock to convert inductor current to 8 bit digital data.

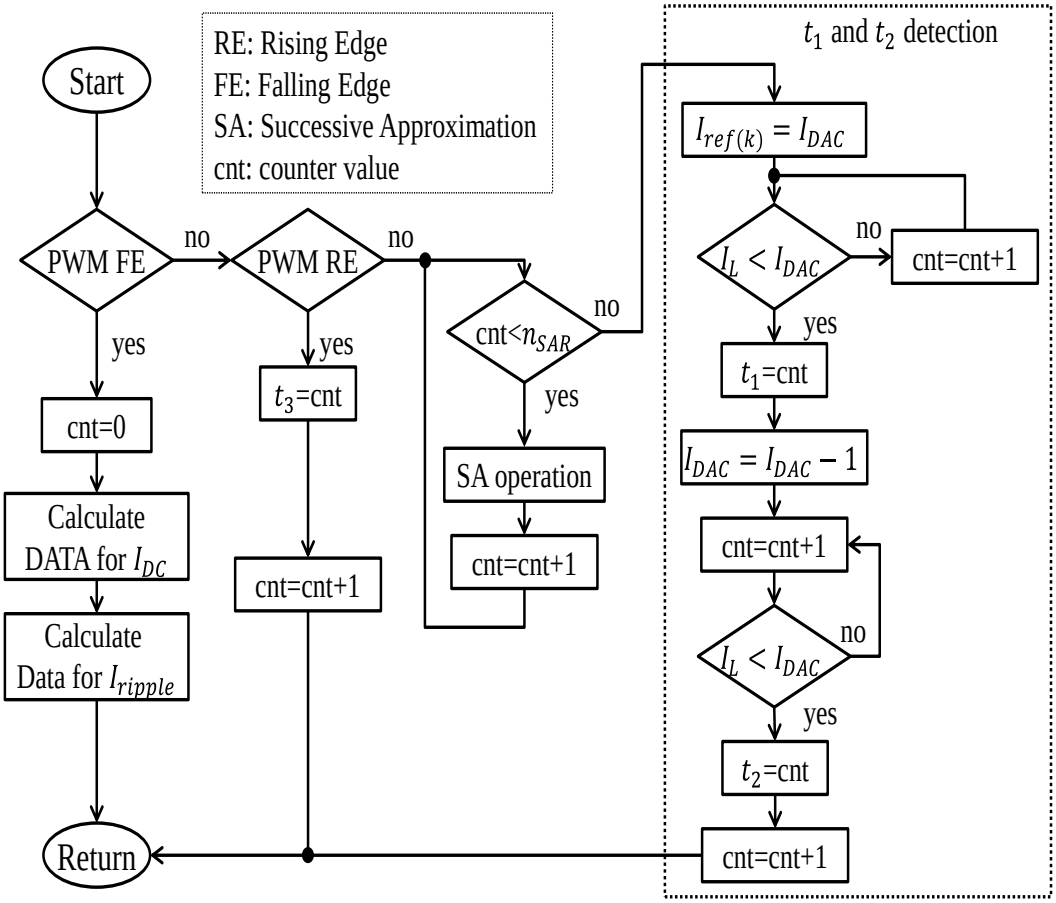


Figure 5.7. Flow chart of the digitalizing algorithm of the proposed ICDC [13].

5.3. Simulated Results and Discussions

To verify the operation, the proposed ICDC is simulated with 12 V to 1.0 V DC-DC buck converter. The block diagram of the ICDC connected to DC-DC buck converter is described in Fig. 5.8. The major parameter of DC-DC buck converters is as follows: inductance L is 2.2 μH, output capacitance C_O is 250 μF, and switching frequency f_{sw} is 100 kHz. Inductor current signal is sensed by current sensing resistor and amplified by shunt amplifier to be 50 mV/A. Inductor current estimation logic in ICDC operates with 70 MHz clock frequency. The simulated waveform of the proposed ICDC is described in Fig. 5.9. The output code of data for I_{DC} and I_{ripple} were 160 which corresponds to 10.0 A and 161 which corresponds to 5.01 A respectively.

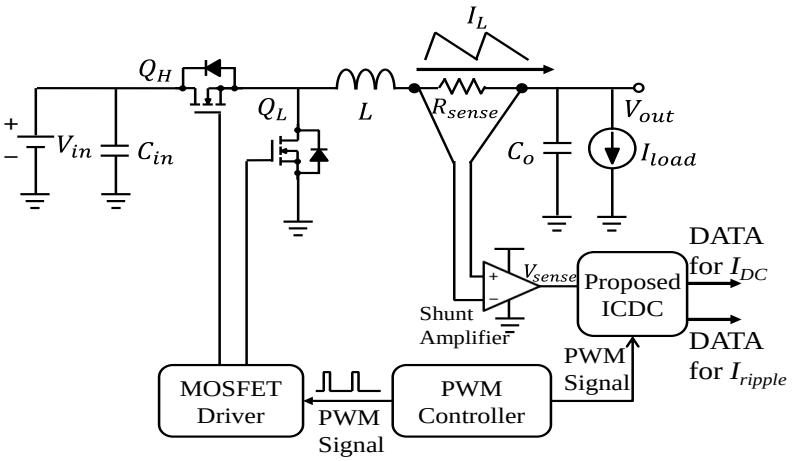


Figure 5.8. Block diagram of the proposed ICDC connected to buck converter [13].

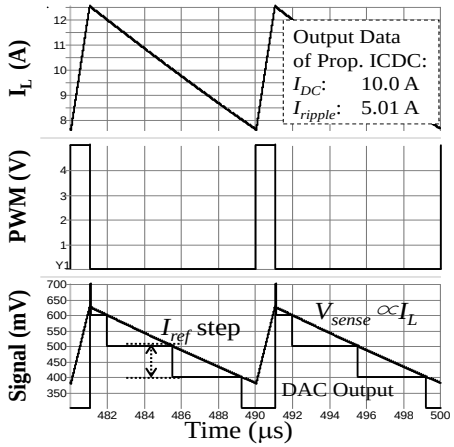


Figure 5.9. Simulated waveforms of the proposed circuit connected to 12 V to 1.0 V 100 kHz buck converter [13].

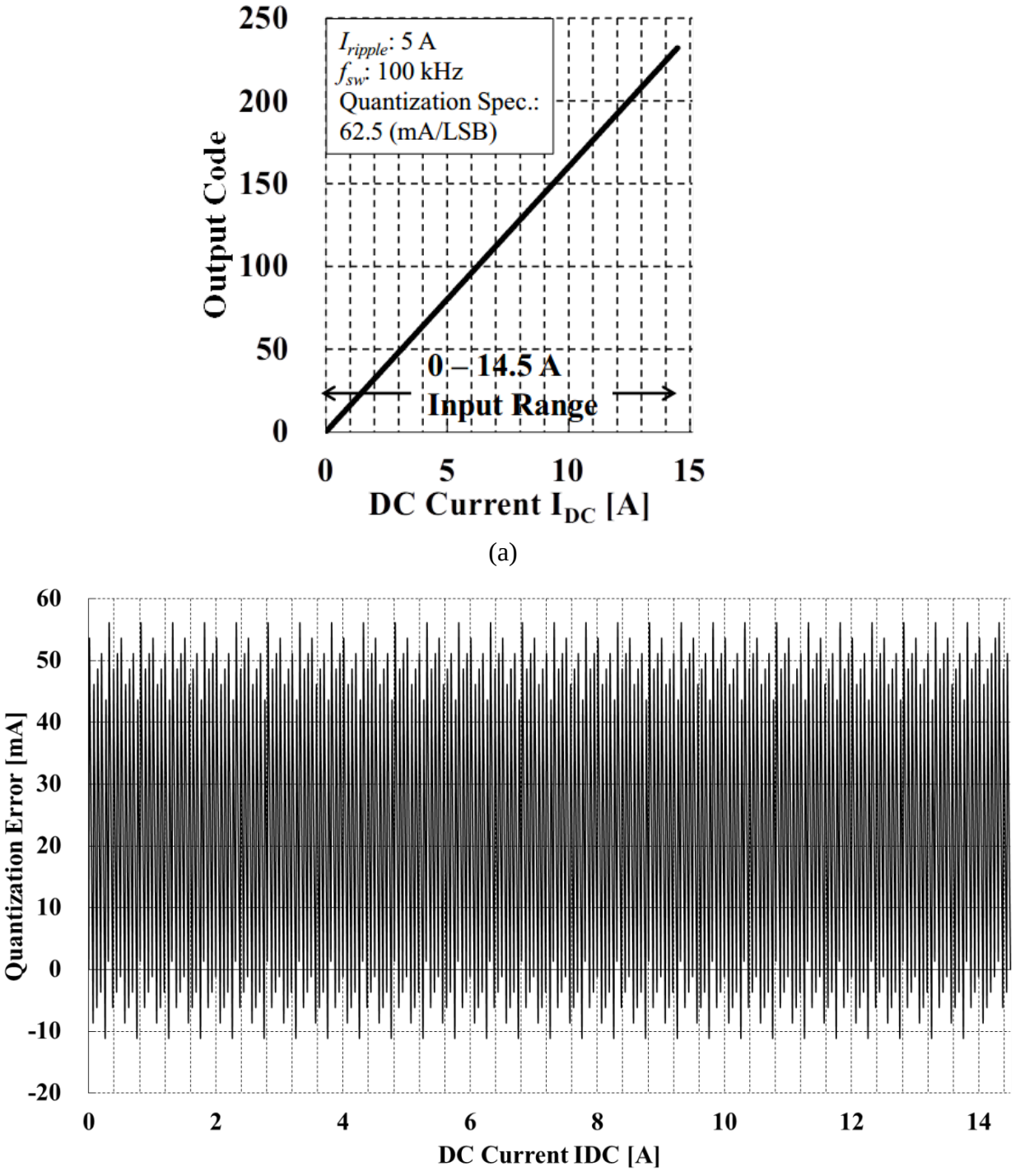
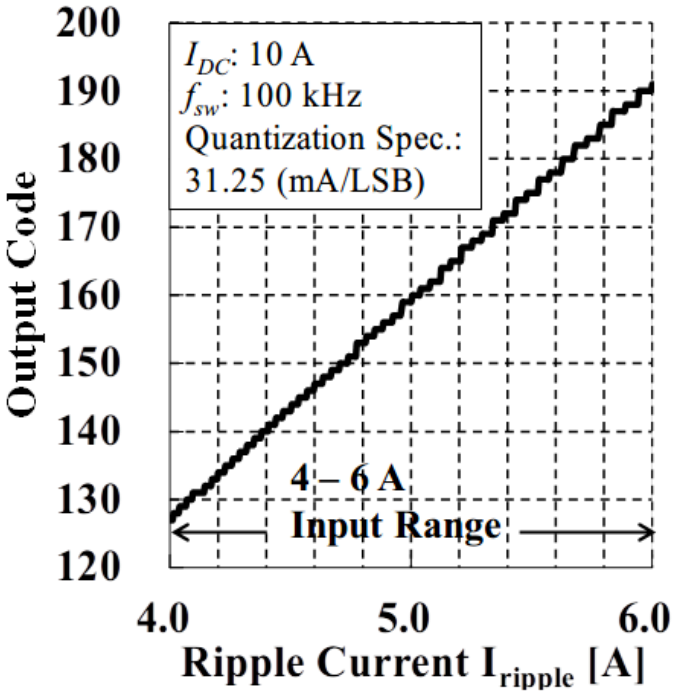
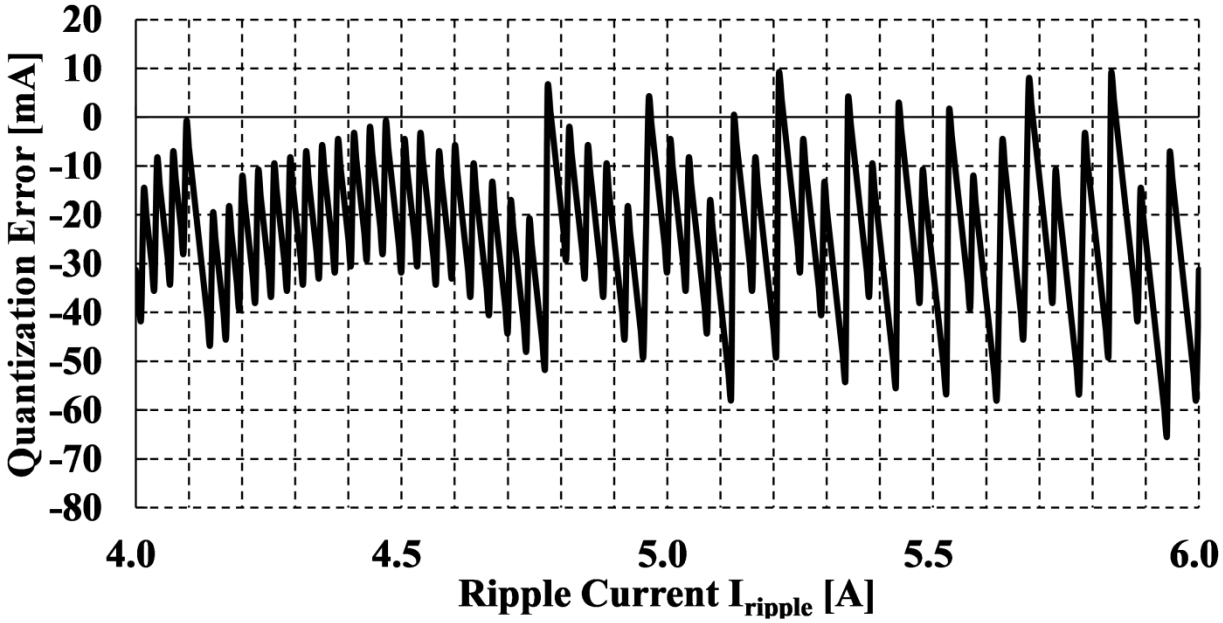


Figure 5.10. (a) Conversion characteristic and (b) quantization error of DC component of proposed ICDC from 0 A to 14.5 A range [13].



(a)



(b)

Figure 5.11. (a) Conversion characteristic and (b) quantization error of ripple component of proposed ICDC from 4 A to 6 A range [13].

Conversion characteristic and quantization error of DC component with 5 A ripple current, 0.10 duty cycle, 100 kHz switching frequency are described in Fig. 5.10. The output code of DC component is quantized to be 62.5 mA/LSB. Input range of DC component was 0 A to 14.5 A which is sufficient to convert inductor current in DC-DC converters. Conversion characteristic and quantization error of ripple component with 5 A DC current, 0.10 duty cycle, 100 kHz switching frequency of are described in Fig. 5.11. The output code of ripple component is quantized to be 31.25 mA/LSB. Maximum quantization error of ripple component was 65 mA which is in good agreement with designed value from eq. (7). The input range of ripple component was 4 A to 6 A which is sufficient to convert ripple component considering component tolerance such as inductance. The comparison of number of required components in the proposed ICDC and conventional 2 channels SAR ADC based implementation for converting DC and ripple component to digital data is listed in Table 5.I. The circuit performance and complexity is calculated for 8 bit conversion of the same DC component range 0 A - 14.5 A with ripple component 5 A. The quantization error of the proposed ICDC is suppressed in compared with conventional ADCs. The required number of DAC bit is significantly shrunk to 3 bit. The proposed ICDC operates without S/H circuit and ripple cut-off filter because of the merit of novel estimation algorithm.

Table 5.I. Summary of number of required components for 8 bit conversion of the proposed ICDC and conventional ADC based inductor current digitalizing system [13].

		Proposed ICDC	Conventional SAR ADC based system
Circuit Performance	Sensing Range	0 A - 14.5 A I_{DC} with 5 A I_{ripple}	
	Quantization Error	65 mA	76 mA*
Complexity	DAC bits	3	8
	Sample and hold circuit	0	2
	Ripple cut-off filter	0	1
	Input channels	1	2

* This is equivalent to the value of sensing range 19.5 A (I_{DC}+I_{ripple}) divided by 2^8.

5.4. Conclusions

Concept of inductor current to digital converter is presented. The feature of the proposed ICDC is to convert DC and ripple component of inductor current to digital data separately and simultaneously with small number of elements, which was hard for conventional ADCs. Proposed ICDC is designed and simulated with 12 V to 1 V buck converter, and successfully converted the 10 A of DC component with 5 A of ripple component to digital data. Input range of DC and ripple component are 0 A to 14.4 A and 4 A to 6 A with 65 mA maximum quantization error respectively, which are sufficient to convert inductor current in DC-DC converter to digital data. Accordingly, the proposed ICDC is promising candidate to inductor current digitalizing circuit in digitally controlled DC-DC converter.

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Chapter 6

CMOS DC-DC Converter Using Vertical Body Channel MOSFET

6.1. Introduction

Low-loss and stable DC-DC converter with very high operation frequency is an important part for the power supply of microprocessors. [1-3] Constructing high operation frequency converters miniaturizes the volume of huge components (e.g. inductor, output capacitor). One of the hugest components in DC-DC converters are inductors. Significantly in the applications over 100 MHz, only nH order of inductance is needed, hence it becomes possible to use significantly miniature inductor which is able to implement on the package substrate [4]. Since the inductor is possible to realize within few mm^2, the inductor size develops into more miniature than that of an on-board type inductor (5-10 mm^2) utilized under an operation frequency less than one megahertz. Consequently, over 100 MHz converter design endows us to considerably miniaturize the dimension of the DC-DC converter within few mm^2. To accomplish a significantly high operation frequency such as 100 MHz, CMOS DC-DC converters realized with advanced digital CMOS technology [3-12] attracts a lot of attention. It is experimentally verified that a planar CMOS technology based DC-DC converter attained over 90% efficiency operated in 1 MHz frequency with V_{IN} = 3.0 V, V_O = 1.2 V in the previous study [13]. Another study has reported a 100 MHz frequency, (V_O/V_{IN} = 2.4 V / 3.3 V) conversion ratio, and 90% efficiency DC-DC converter [9]. Meanwhile, what is still difficult in this engineering field is to accomplish efficiency exceeding 90% with a low conversion ratio such as 3.3 V / 1.2 V, and a significantly high operation frequency over 100 MHz utilizing planar CMOS, thus efficiency improvement is eminently desired. A CMOS DC-DC converter is incorporated in modern microprocessors for a couple of advantages [5-7].

The conversion ratio defined as V_{OUT}/V_{IN} is one of the critical requirements of the CMOS DC-DC converter. For the microprocessor power supply, it is important to conduct voltage step-down from a higher voltage to a lower voltage since it makes possible to reduce the energy dissipation of upstream power conversion circuits,

improves the reliability of the tight voltage control, and reduces the number of input or output pins [5,6,9-11]. In order to improve efficiency around 100 MHz region, constructing power stage with a couple of MOSFETs connected in serial, referred as cascode bridge, is usually adopted, since serialized advanced digital CMOS devices provides less gate charge Q_g and on-resistance R_{on} compared to a monolithic high-voltage CMOS device.

The power stage is composed of two-by-two p-channel and n-channel MOSFETs for efficient power conversion in conventional CMOS DC-DC converters utilizing planar CMOS process, as described in Fig. 6.1. As described in the red broken square, the cascode bridge has an PMOS power switch on the high-side. V_{hr} is a 1/2 level supply voltage of the input voltage V_{in}, and it is referred as half-rail voltage. V_{hr} is provided by an external half-rail power supply circuit [11]. M2 and M3 gate is common and connected to V_{hr}. The positive input of the drivers for M1 and M4 is also V_{hr}. The center node of M1-M2 and M3-M4 V_{hr} are kept to be 0.5 V_{in} by V_{hr} in the off-state. This makes possible to handle the large input voltage efficiently even though operational frequency is very high. It is hard to attain an approximately 90% efficiency with a low V_O/V_{IN} under +100 MHz operation frequency even in the cascode bridge based CMOS DC-DC converters, thus more reduction of loss is necessary. It is a challenge that the conduction loss dissipated due to p-channel MOSFETs which has high on-resistance lowers the efficiency of the conventional CMOS DC-DC converter. Furthermore, the PMOS power switch on the high-side possess a more huge size in comparison with the n-channel MOSFET to attain enough current capability since the p-channel MOSFET suffers from low mobility compared to the n-channel MOSFET. The gate loss turns out considerable under high operation frequency because a bulky transistor has a bulky load capacitance.

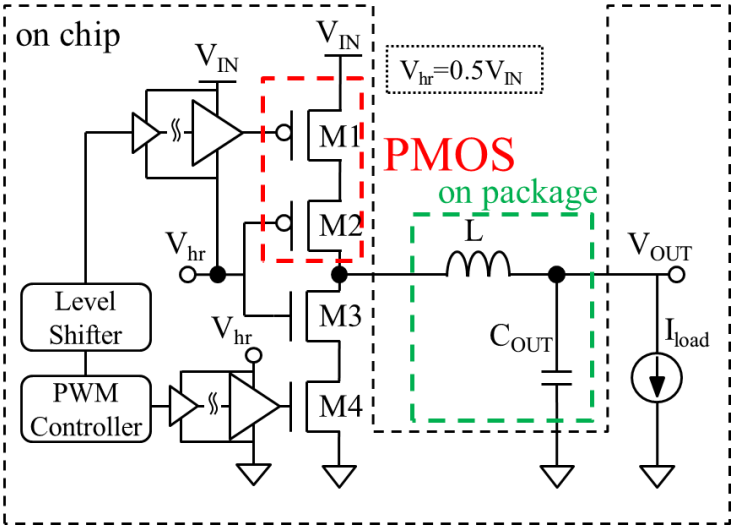


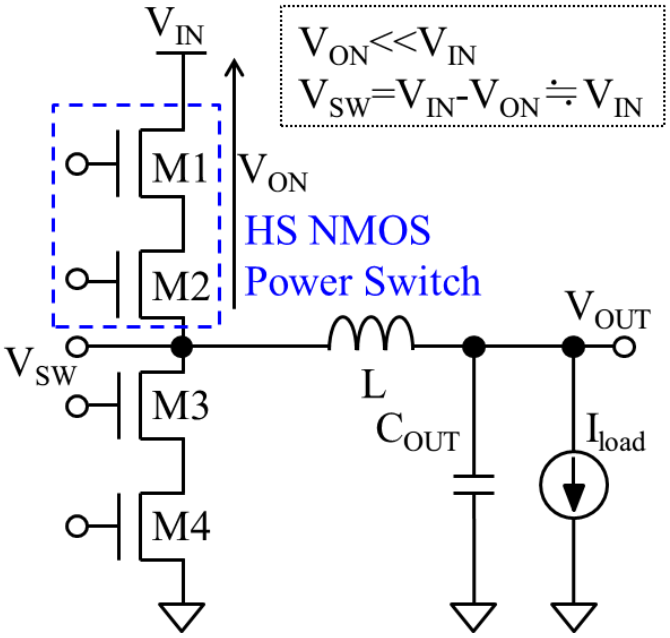
Figure 6.1. Circuit diagram of the conventional converter with HS PMOS configuration [33].

Nonetheless, utilizing n-channel MOSFETs on the high side (HS) with a planar CMOS technology is difficult. Figure 6.2(a) illustrates a circuit diagram of including two MOSFETs cascode bridge with NMOS power switch on the high-side. The switching node voltage V_{sw} rises to (V_{IN}-V_{ON}) where V_{IN} and V_{ON} are is the input voltage and the on-state voltage drop of the HS NMOS power switch, respectively. The NMOS power switch on the high-side is on, and it is surrounded by the blue broken square. A high voltage approximately equal to V_{IN} is applied to the source of the n-channel MOSFET of the HS power switches M1 and M2 because the on-state voltage drop V_{ON} is lower than V_{IN}. Due to the back-bias effect, a serious performance degradation of the output characteristics of M1 and M2 is occurred when the bodies of M1 and M2 are connected to ground, as described in Fig. 6.2(b). V_{gate} is a overdrive gate voltage which drives M1 and M2. V_{ON} is a voltage which is applied across the drain of M1 and the source of M2. In the planar CMOS process without a triple well, the performance of the HS NMOS power switch is degraded depending on the negative back-bias voltage -$V_{IN.}$ It suggests that the HS NMOS power switch on-resistance might increase by about 95% when the input voltage is 3.3 V. Well isolation with a triple well process is necessary in order to relieve the influence of back-bias in planar CMOS technology. Nonetheless, additional area is required then large parasitic capacitance is generated due to the additional p-n junction by using the triple well. Specifically for high-input-voltage usages including CMOS DC-DC converters, the performance

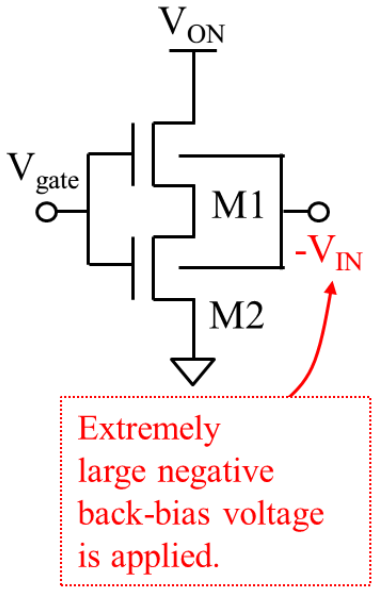
degradation turns to be considerable.

A CMOS DC-DC converter with an HS NMOS configuration using a triple well process had been investigated in previous study [12]. In this conventional work, the body of the HS power switch was tied to the source. This connection needs to use the triple well isolation in order to control body node potential in planar CMOS technology. It generates a delay in the switching of the CMOS DC-DC converters due to well contact, and this incurs increase in switching loss [8]. Hence, the HS NMOS configuration with a planar CMOS technology including triple well process is undesirable for future CMOS DC-DC converters for microprocessors.

This study proposes a CMOS DC-DC converter which includes a cascode NMOS power switch on the high-side, utilizing a vertical BC MOSFET to improve efficiency. Transient simulation of the proposed CMOS DC-DC converter have been carried out under 100 MHz operation frequency with a low conversion ratio (V_O/V_{IN} = 1.2 V / 3.3 V), which is able to be miniaturized in few mm^2. In order to make the most of outstanding performance which does not affected by the back-bias effect, the proposed CMOS DC-DC converter is constructed with vertical BC-MOSFETs. Whether back bias exists or not is one of the biggest differences between vertical BC MOSFET and standard planar MOSFET without additional well structures [14-18]. Furthermore, for reliable driving of the proposed HS NMOS power switch, a new bootstrap driver is proposed. Concept of the proposal and principle of operation are described in Sect. 6.2. Benefits as a power switch in both on and off states are analyzed in Sect. 6.3. Finally, waveforms and performance including efficiency of the proposed and conventional CMOS DC-DC converters are simulated in Sect. 6.4.



(a)



(b)

Figure 6.2. (a) Schematic of a CMOS DC-DC converter including HS NMOS power switch, and (b) equivalent operating voltage condition of HS NMOS power switch when it is on-state [33].

6.2. Concept of the proposed CMOS DC-DC Converter

Since it makes possible to configure the CMOS DC-DC converter by an HS NMOS power switch which improves efficiency under high switching efficiency, it is desirable to use semiconductor devices which is a high-current and low-leakage device and does not affected by the back-bias effect. The appropriate technology seems to a vertical BC-MOSFET under a standard well structure in terms of the back-bias effect. In literature, the excellent performance of the vertical BC-MOSFET has been extensively studied [19-24]. Because of the back-bias free characteristic of vertical BC-MOSFET [25-28], the vertical BC-MOSFET can be adopted to an HS NMOS power switch without sacrificing performance and additional well structures. In order to miniaturize the transistor size with the same on-resistance, or lower the on-resistance with the same transistor size, an n-channel MOSFET is a superior switching component than a p-channel MOSFET for CMOS DC-DC converters. In addition, excellent scalability for future nanoscale transistors of the vertical BC-MOSFET meets the requirements for high density integration of future microprocessors [29-32].

In Fig. 6.3, a block diagram of the proposed CMOS DC-DC converter with a vertical BC-MOSFET is described. The power stage is composed of a cascode bridge for attaining high efficiency under very high operation frequency of 100 MHz in the proposed CMOS DC-DC converter. The cascode bridge includes a bootstrap driver for the HS NMOS power switch, a level shifter, a PWM controller, a HS NMOS power switch, and a driver for the LS power switch. As power sources, the primary input voltage V_{IN} and the half-rail voltage V_{hr} are used. V_{hr} is expressed as follows:

$$V_{hr} = 0.5\, V_{IN}. \quad (1)$$

Circuit parameters of passive elements (e.g. output capacitor, bootstrap capacitor, and inductor) are set up supposing they are used on the package substrate, which is equivalent to the conventionally developed converters [5-7]. The cascode bridge in the proposed converter is configured by HS NMOS cascode power switch (M1, M2) and an LS NMOS cascode power switch (M3, M4). The body is not tied to the source, since there is no need to adjust the potential during switching in a vertical BC-MOSFET. A gate driving voltage higher than $V_{IN}+V_{TH}$ is necessary both for M1 and M2 in order to turn on the proposed HS NMOS power switch. Therefore, it cannot

be driven utilizing a conventional CMOS buffer circuit. A bootstrap driver is utilized to obtain a gate drive voltage which is higher than $V_{IN}+V_{TH}$ in the proposed converter. The voltage at the bootstrap node V_{BST} is directly connected to M1 and the high-voltage input of the buffer. The buffer output is connected to the gate of M2. P-channel For rectifying the charge from V_{hr} to $V_{BST,}$ MOSFET M5 and n-channel MOSFET M6 are located as boot switches. In order to the cut-off voltage which is applied in reverse and reaches V_{IN} at maximum, they are connected in series. Thus the gate driving voltage is obtained. The gate of M5 is connected to the switching node V_{SW}, the source of M5 is connected to the half-rail voltage V_{hr}, and C_{BST} is an external bootstrap capacitor which is utilized to generate a higher voltage than V_{SW} by a charge pump principle. M6 is wired by diode connection to supply the charge from V_{hr}. M5 and M6 supply charges to C_{BST} to be (V_{hr}-V_{TH}) when V_{SW} is 0 V. The switching node voltage V_{SW} and the bootstrap node voltage V_{BST} rise at the same time with the capacitive coupling of C_{BST} when M2 is driven. M5 and M6 automatically turn off since the gate voltage of M5 becomes roughly equal to V_{IN} and V_{BST} becomes larger than V_{IN}, respectively, in this transition. Thus, a V_{BST} higher than ($V_{IN}+V_{TH}$) is attained. Thus, M 1 and M 2 are turned on.

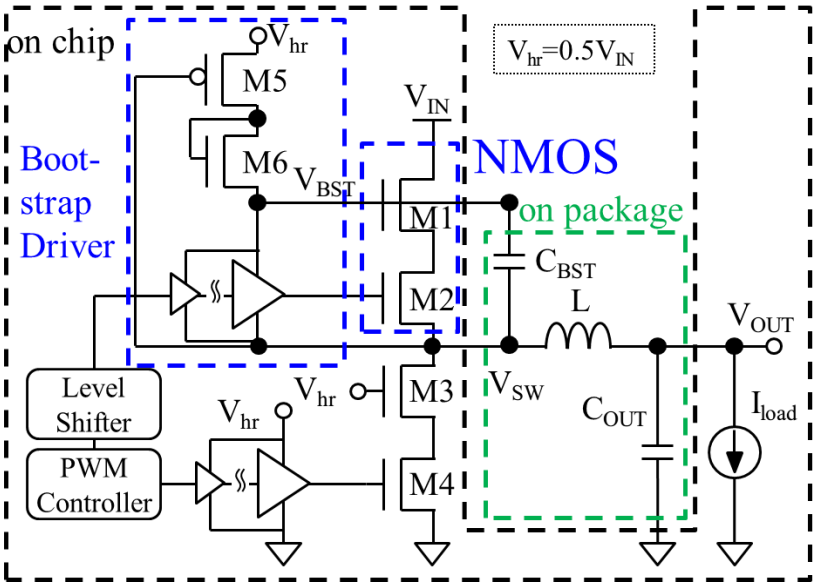


Figure 6.3. Block diagram of the proposed converter which includes HS NMOS power switch (M1-M2) and dedicated bootstrap driver [33].

Figure 6.4 shows a timing chart of the proposed bootstrap driver for cascode bridge which contains HS NMOS power switch configured by the vertical BC MOSFETs. In order to automatically switch M1 and M3, the V_{gs} of M1 and the V_{gs} of M3 are kept to be equal to V_{hr}. By the PWM signal output from the controller, the V_{gs} of M2 and M4 complementary turns on. At the timing of the switching node voltage swings from ground to V_{IN}, the bootstrap node voltage V_{BST} swings from V_{hr} to (V_{IN}+V_{hr}). The V_{gs} of M1 can be represented as (V_{BST}-V_{SW}), and consequently, the V_{gs} of M1 is made to V_{hr}. Therefore, M1 turns on without drivers, which causes additional loss.

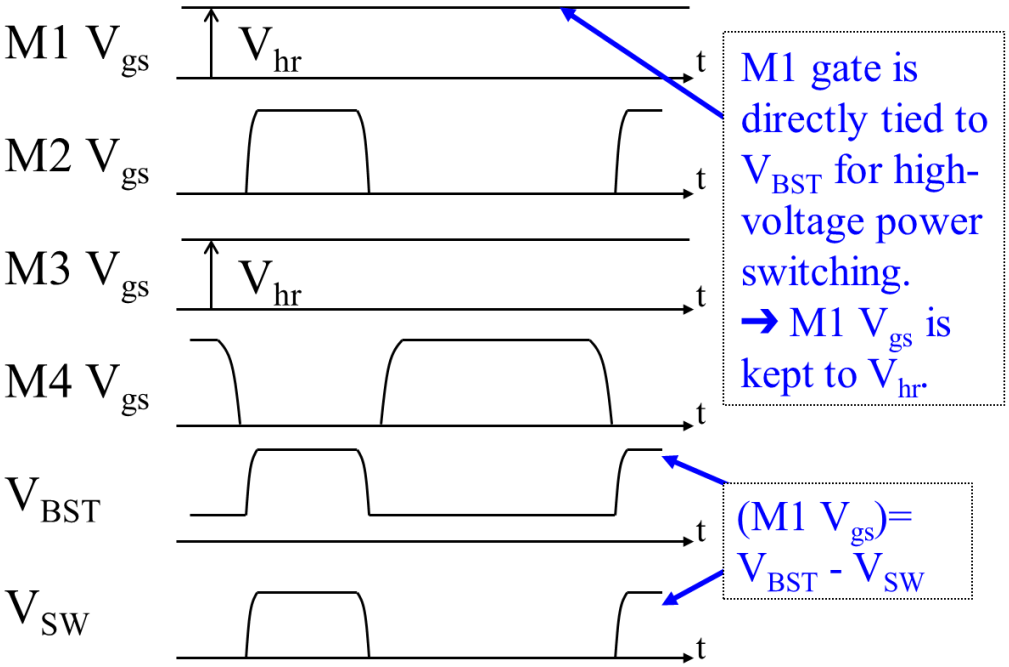


Figure 6.4. Timing chart of the proposed bootstrap driver for cascode power stage which contains HS NMOS power switch [33].

6.3. Merits of vertical BC-MOSFET for power switch

6.3.1. Back-bias effect free characteristic

In order to verify the merit in DC-DC converters, the benefits of the vertical BC-MOSFET for a power switch is estimated. Figure 6.5 illustrates the structure of the vertical BC-MOSFET. In the vertical BC-MOSFET, the source, gate, and drain are arranged vertically. The sides of the silicon pillar are wrapped by the gate oxide film for 360 degrees. The channel region is isolated from the substrate by an n+ region. This chapter proposes that the vertical n-channel MOSFET is utilized as an HS power switch for characteristics free from back-bias effect, as its channel and the substrate are discrete.

Figure 6.6 describes the simulated current-voltage characteristics of a monolithic n-channel vertical BC-MOSFET compared with an n-channel planar MOSFET. The model parameters of planar and vertical BC MOSFETs are experimentally extracted for HSPICE BSIM4. The size of transistor W/L is 5 μm/0.18 μm. It is defined that the gate width of the vertical BC-MOSFET is equivalent to the circumference of the silicon pillar. The back bias voltage V_b for 0 and -3.3 V is applied to evaluate the influence of a high input-voltage for CMOS DC-DC converter usage. Since the vertical BC-MOSFET is fully depleted, increase of its threshold voltage can be absolutely ignored.

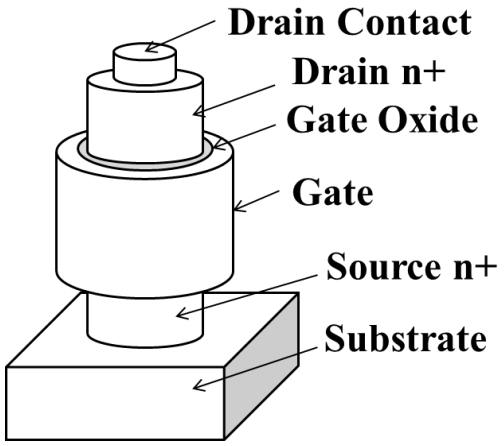
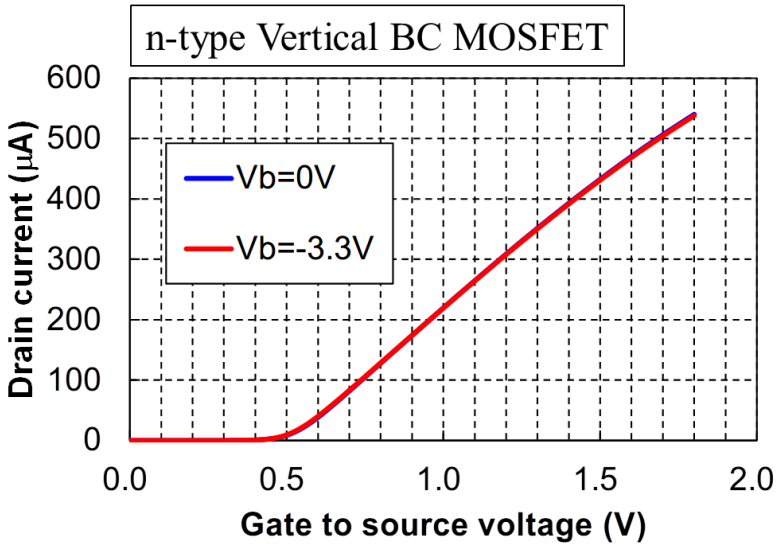
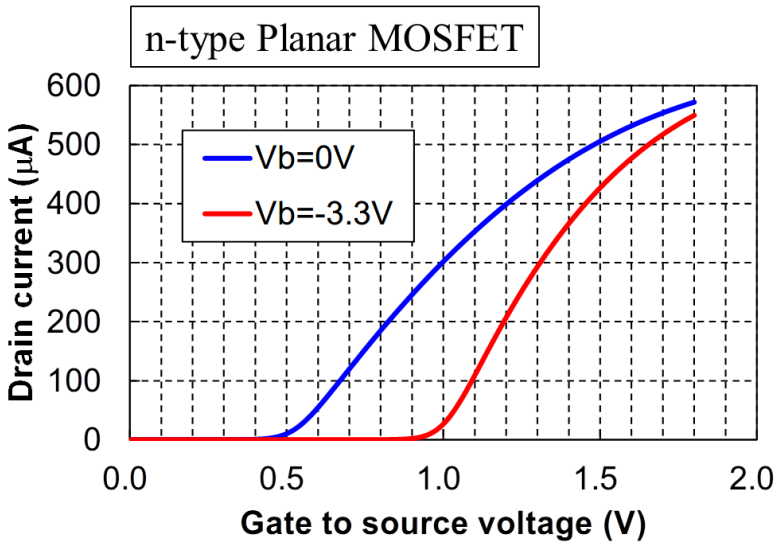


Figure 6.5. Typical structure of the vertical BC-MOSFET [33].



(a)



(b)

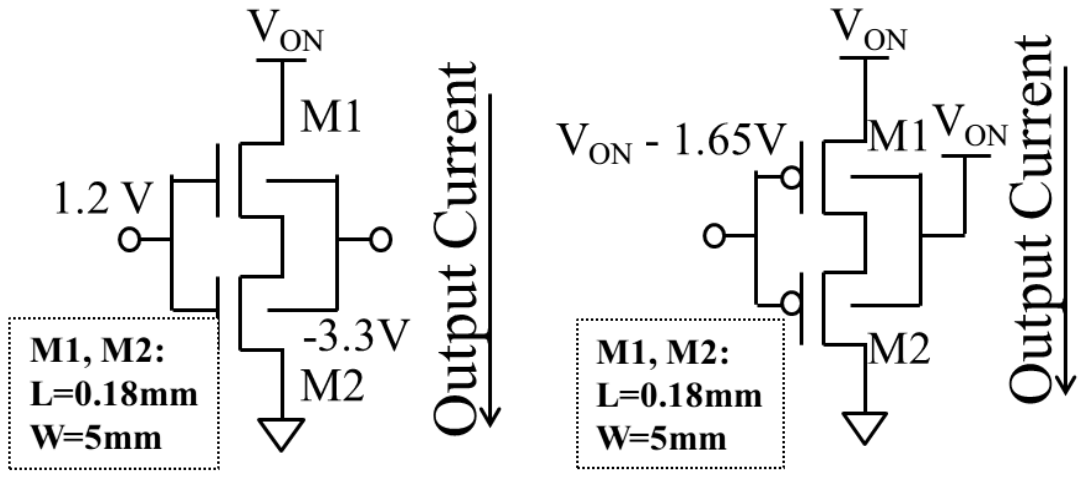
Figure 6.6. Current-voltage characteristics of (a) n-channel vertical BC-MOSFET compared to (b) n-channel planar MOSFET for 0 and –3.3 V back-bias voltage V_b. The transistor size W/L is 5 μm/0.18 μm [33].

6.3.2. Performance as a power switch: on-state

The equivalent bias condition which is supposed for the HS NMOS configuration in the converter is illustrated in Fig. 6.7(a). The transistor size W/L of both M1 and M2 are 5 μm/0.18 μm. The HS power switch voltage drop in on-state V_{ON}

is applied to the drain of M1. As a back-bias, a dc voltage of -3.3 V is applied to the body node of M1 and M2. In order to take the voltage drop of the boot switch and the charge distribution from C_{BST} to parasitic capacitive elements into account, the gate voltages of M1 and M2 are 1.2 V, which is lower than the V_{hr} of 1.65 V. The equivalent bias condition supposing the HS PMOS power switch in on-state is illustrated in Figure 6.7(b). M1 and M2 are p-channel MOSFETs. For M1 and M2, the transistor size W/L is 5 μm/0.18 μm which is equal to the condition applied to the n-channel MOSFET. The gate voltage of M1 and M2 are (V_{ON}-1.65) V. The body node voltage of M1 and M2 is V_{ON}.

Figure 6.8 shows the output current benchmark of the n-channel and p-channel MOSFETs of planar and vertical BC-MOSFETs, respectively, supposing the HS power switch usage. The proposed vertical n-channel MOSFET described by the blue line is +85% superior to the conventional planar p-channel MOSFET described by the red line at 0.10 V V_{ON}. The above-mentioned difference in the current capability corresponds to the proposed vertical HS NMOS power switch that accomplishes 46% lower on-resistance than the conventional planar HS PMOS power switch. Meanwhile, the conventional HS power switch with a planar n-channel MOSFETs outputs a tiny current under the same conditions. Since it has a potential to realize an HS NMOS power switch without sacrificing performance, the vertical BC-MOSFET seems appropriate CMOS device for configuring a cascode CMOS DC-DC converter.



(a) (b)

Figure 6.7. Equivalent bias condition of HS power switch: (a) n-channel MOSFET and (b) p-channel MOSFET in on-state [33].

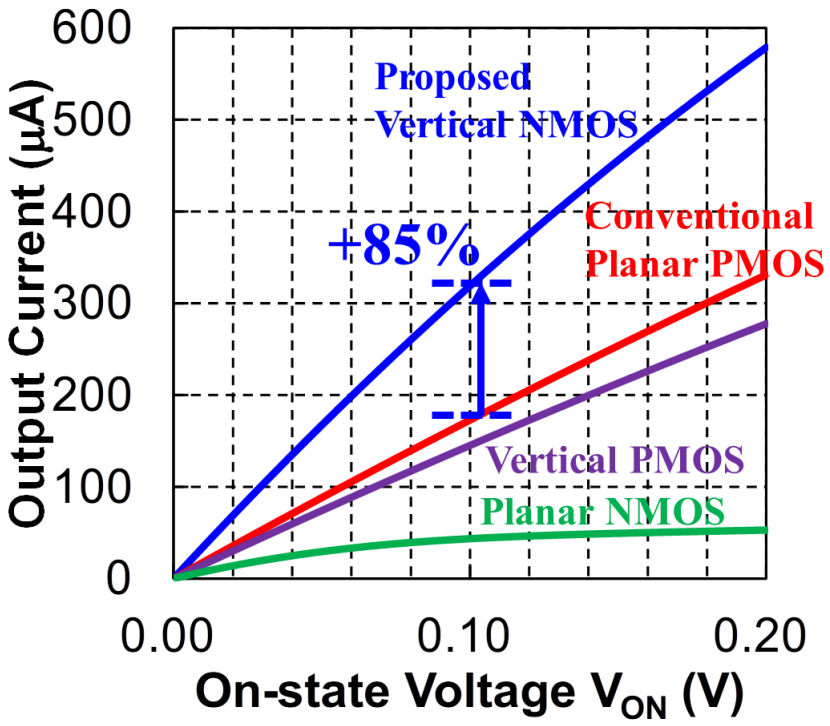
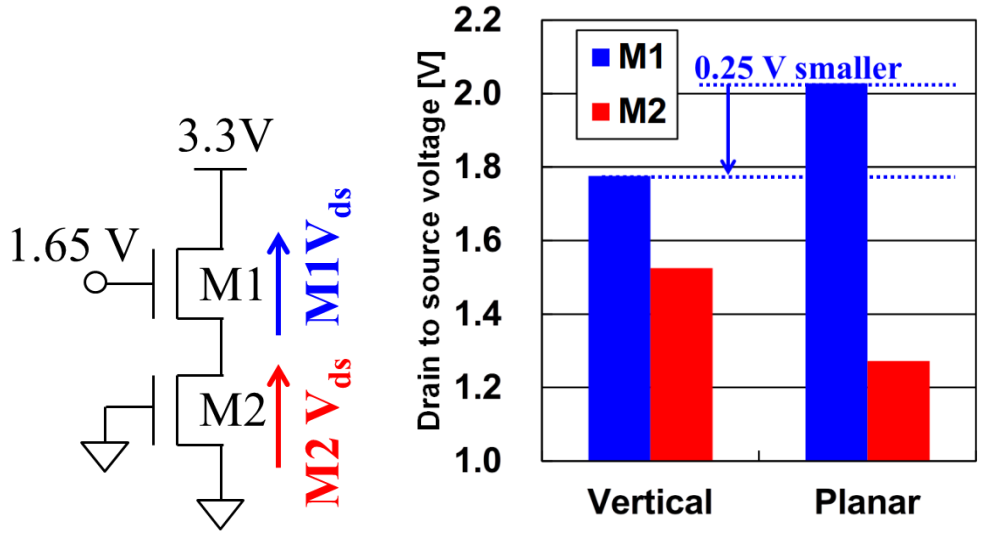


Figure 6.8. Output current benchmark of n- and p-channel MOSFETs of planar and vertical BC-MOSFETs, respectively, for cascode HS power switch usage [33].

6.3.3. Performance as a power switch: off-state

The circuit is designed not to occur that the transistor's V_{gs} and V_{gd} exceed the CMOS process voltage in the cascode bridge. Therefore, it is critical to equalize the drain-to-source voltage in the off-state in order to handle a large input voltage V_{IN}. The voltage distribution in the cascode switch in the off-state is analyzed for evaluating the off-state performance. Figure 6.9(a) illustrates the bias condition in the LS power switch of the cascode bridge circuit in the off-state. The input voltage is 3.3 V, the M1 gate voltage is 1.65 V, and the M2 gate is 0 V in this case. M1 automatically turns off with rising source voltage and its V_{gs} becomes lower than V_{TH} at the transition from the on-state to the off-state. Figure 6.9(b) describes the simulated voltage distribution of drain-to-source voltage of vertical MOSFET compared to planar type MOSFET. The drain-to-source voltage of M1 was 0.25 V lower than that of the conventional planar MOSFET in the vertical BC-MOSFET. Consequently, the voltage distribution of two MOSFETs in the off-state becomes more uniform than that of the planar MOSFET by utilizing the vertical BC-MOSFET. This is owing to the threshold voltage shifts which

are caused by the back-bias effect in the planar MOSFET. From this result, since it can handle a higher input voltage at the same CMOS process voltage, a lower conversion ratio can be attained by utilizing the vertical BC-MOSFET than by utilizing the planar MOSFET,



(a) (b)

Figure 6.9. (a) Equivalent bias condition of LS NMOS power switch in off-state.
(b) Benchmark of drain-to-source voltage distribution between vertical BC and planar MOSFETs in off-state [33].

6.4. Simulation results and discussion

The circuit simulation of the proposed CMOS DC-DC converter which includes a cascode bridge circuit with an HS NMOS power switch is carried out by HSPICE. The parameters utilized in this simulation are listed in Table 6.I. Under the equivalent conditions excluding the driver of the HS power switch and the level shifter, a conventional converter with an HS PMOS power switch is also simulated. The input voltage V_{IN} is 3.3 V and the output voltage V_{OUT} is 1.2 V. The transistor model is BSIM4 0.18 μm vertical BC-MOSFET which was extracted from experimental results both for the proposed and conventional converters. All transistor size L/W of the power transistors M1, M2, M3, and M4 are equal. In all load current levels, the proposed and conventional converters are with the continuous conduction mode (CCM). The control scheme is a voltage mode control. The circuit temperature is 25 °C.

Table 6.I. Parameters of the simulated converter [33].

Input voltage V_{IN}	3.3 V
Input voltage V_{hr}	1.65 V
Output voltage V_{OUT}	1.2 V
Inductance	4 nH
Output capacitance	10 µF
Bootstrap capacitance	4.5 nF
Crossover frequency	10 MHz
Operation frequency	100 MHz

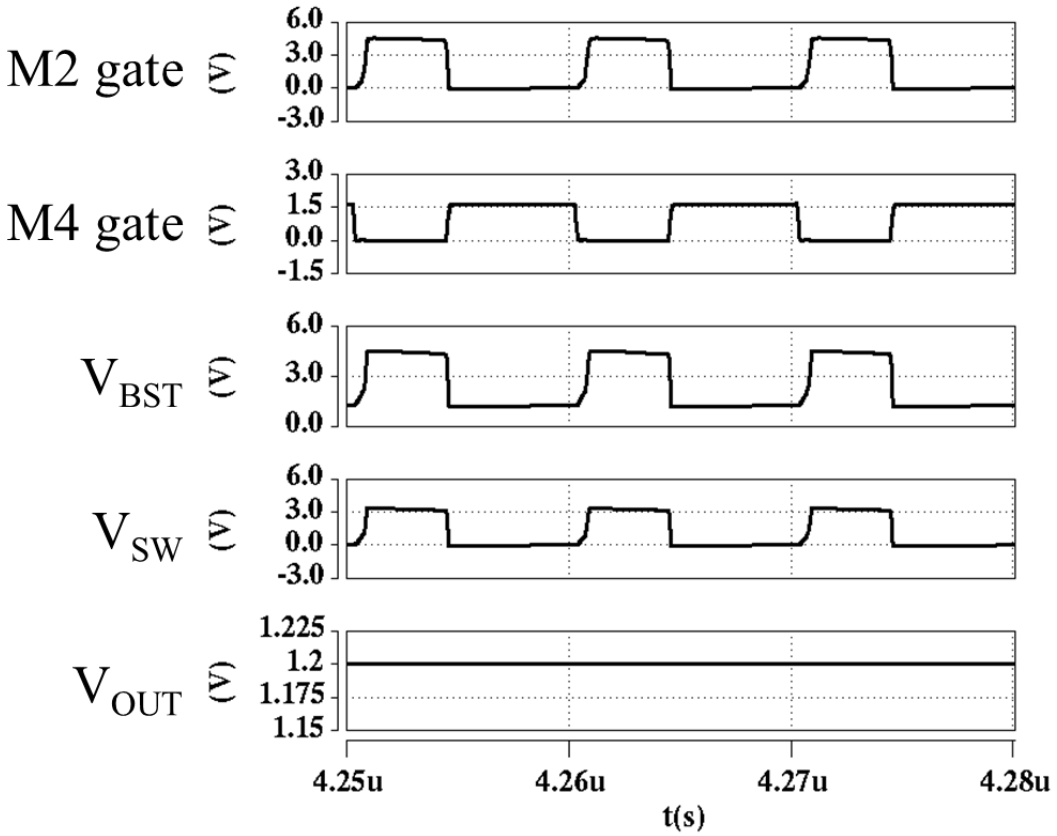


Figure 6.10. Simulated waveform of the proposed converter at 0.5 A load [33].

Figure 6.10 shows waveforms of the proposed converter when the load current level is 0.5 A. The gates of M2 and M4 are driven complementarily. Bootstrap node voltage V_{BST} rises and falls from 1.65 to 5.0 V alternatingly. It can be seen that the output voltage V_{OUT} is regulated to 1.2 V. The bootstrap driver designed for the HS NMOS power switch successfully works, since the 3.3 V 100 MHz switching of V_{SW} is observed.

Figure 6.11describes an efficiency curves of the proposed and conventional converters. Here, the definition of the efficiency is as follows:

$$\eta = P_{OUT} / (P_{IN} + P_{hr}), \quad (2)$$

where P_{OUT} is the output power dissipated in the current sink I_{load}, and P_{IN} and P_{hr} are the input powers from V_{IN} and V_{hr}, respectively. The efficiency is given by averaging the power variables during steady state, then calculating them by Eq. (2) inside the simulation. The proposed and conventional converters with the HS PMOS configuration are compared with the same power transistor size for M1, M2, M3, and M4 as reference data. The peak efficiency of the proposed converter is 84%. This is 3% higher than that of the conventional converter. From a loss point of view, the loss is diminished by 16% by utilizing the proposed converter. In addition, the efficiency is 81%, which is 11% higher than that of the conventional converter in a heavy load region at 2 A load current, which corresponds to 38% loss reduction. This difference can be guessed that it is caused by a conduction loss generated by the p-channel MOSFET because conduction loss becomes larger in the heavy load region. Figure 6.12 shows the efficiency of the proposed converter as a function of load current under various temperatures. Efficiencies from 0 A to 2.5 A are plotted from -25 to 100 °C at intervals of 25 °C. Peak efficiencies were 84% at 0.55 A and 100 °C, and 85% at 0.70 A and 25 °C. Efficiency curves decline since conduction loss becomes large under heavy loads larger than 1.5 A. Due to the on-resistance increase of MOSFETs M1-M4, the negative slope at heavy loads is steepened at high temperatures.

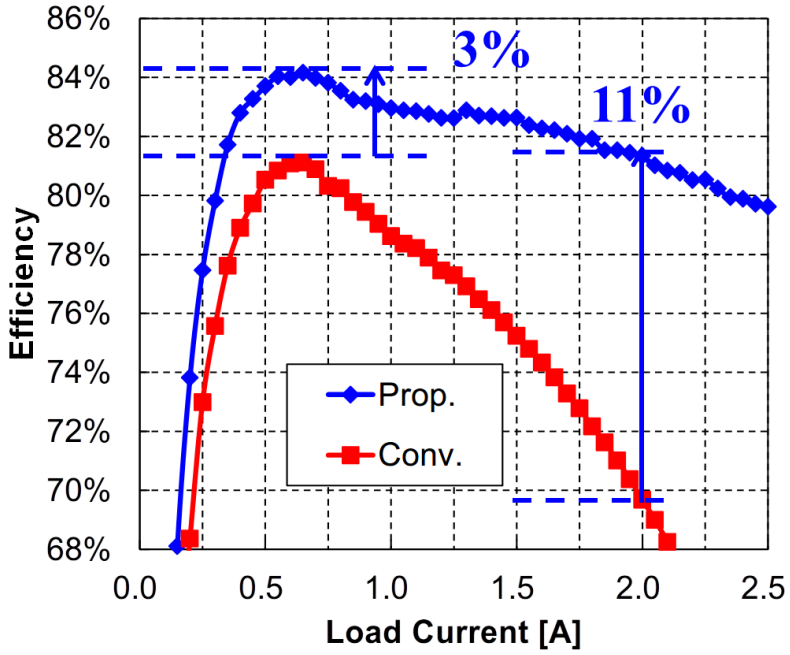


Figure 6.11. Efficiency benchmark of the proposed and conventional converters [33].

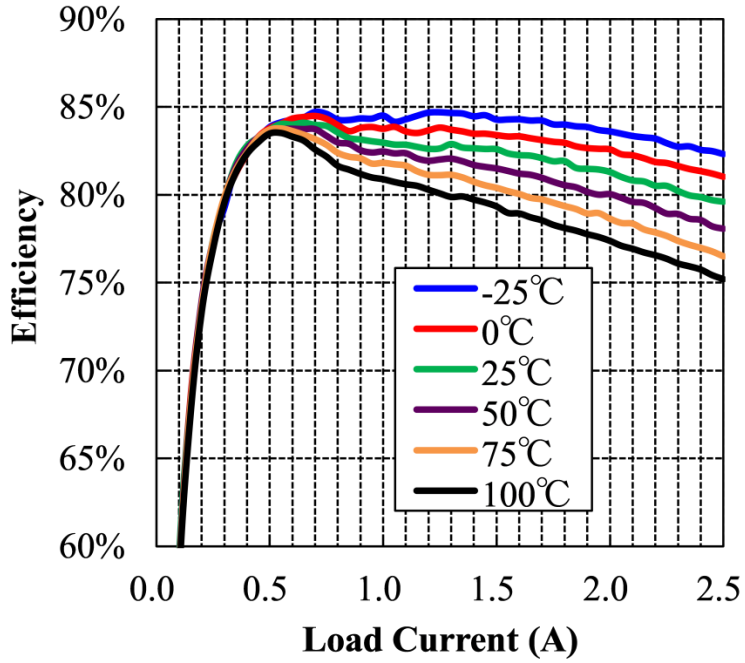


Figure 6.12. Efficiency benchmark of the proposed converter for various temperatures from -25 to 100 °C [33].

The losses in MOSFETs in power stage M1 - M4 at 0.5 A load current are shown in Fig. 6.13. The losses in M1 and M2 are remarkably reduced by 43% and 46%, respectively, since the vertical n-channel MOSFET has high mobility and is free from the back-bias effect. This result agrees well with the difference between mobility of p-type and n-type of MOSFET. The increase in small loss in the LS power switch of M3 and M4 is attributed to the fact that the period of the steady-state duty cycle of the converter lengthens in the conventional converter, thus the period that the LS power switch is on is shorten.

The efficiency of the proposed converter as a function of the total power transistor size is compared to the conventional converter and described in Fig. 6.14. The simulated parameters are equal to that in Table 6.I. The MOSFETs M1 – M4 with identical size are used, and the size is swept. The vertical axis indicates the efficiency at 0.5 A load, while the horizontal axis indicates the total power transistor size W x L. The peak efficiency of the proposed converter was 84.9% with 2070 μm^2 total power transistor size. This is 4.2% higher than that of the conventional converter in a 26% more miniature total MOSFETs (M1-M4) size. It should be noted that M1 – M4 are simulated with the identical transistor size; nonetheless, the optimum size might vary with the conversion ratio of V_{OUT}/V_{IN}. Consequently, the proposed converter can attain a notably higher efficiency with a more miniature size than the conventional converter.

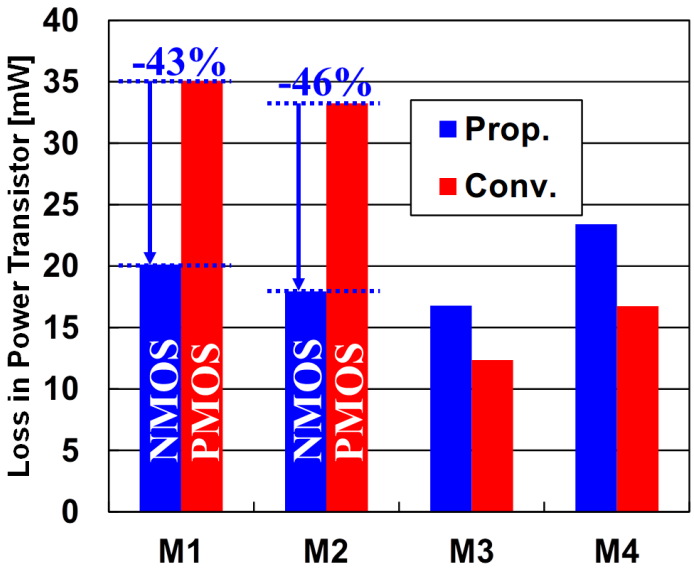


Figure 6.13. The loss of the MOSFET (M 1 - M 4) constituting the power switch in the case of a load current of 0.5 A [33].

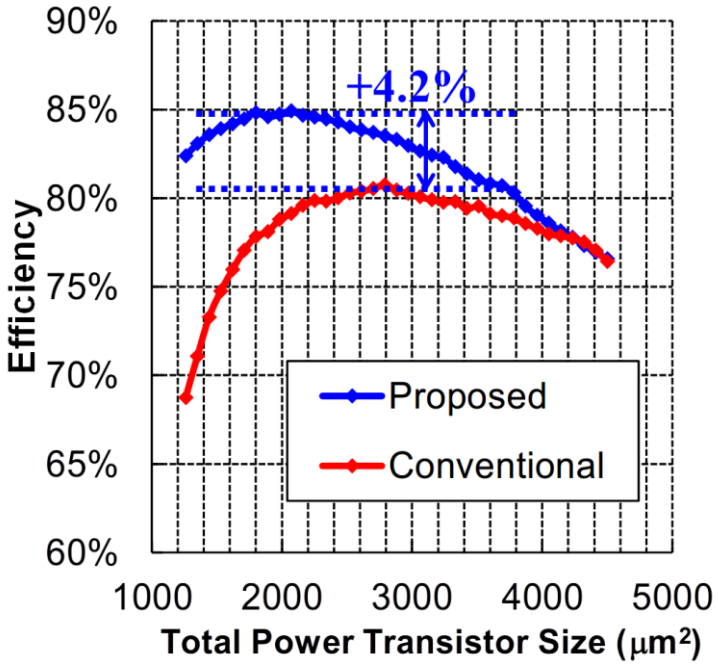


Figure 6.14. Efficiency as a function of total power transistor size of proposed converter compared to the conventional converter [33].

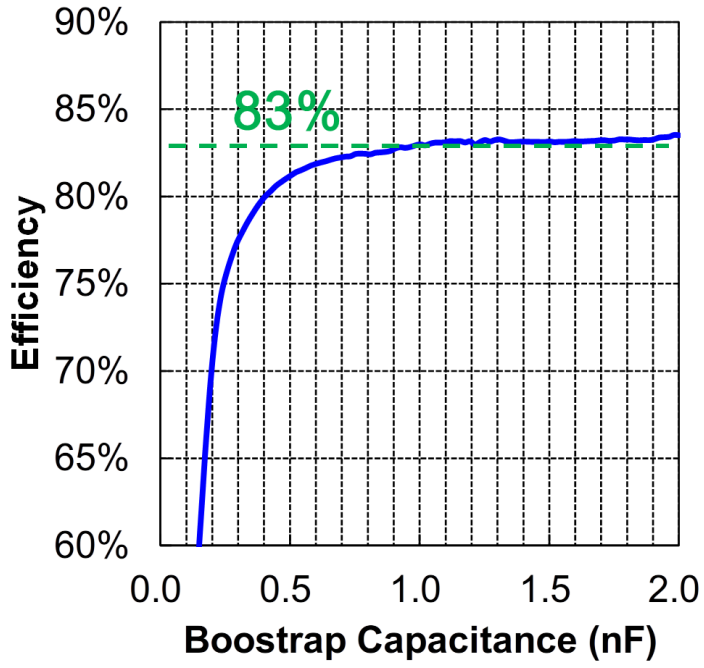


Figure 6.15. Efficiency of the proposed converter as a function of bootstrap capacitance when load current is 0.5 A [33].

6.5. Conclusions

A CMOS DC-DC converter with a cascode bridge which includes HS NMOS power switch and a dedicated bootstrap driver configured by vertical BC MOSFET is proposed for efficiency improvement under very high operation frequency. The output current simulation result under the bias condition supposing the HS power switch suggested that the HS power switch with vertical n-channel MOSFETs has excellent characteristics that is able to obtain 85% larger current than the conventional planar p-channel MOSFET at 0.10 V on-state voltage. Furthermore, the off-state drain-to-source voltage distribution of the cascode switch with vertical BC-MOSFETs became more uniform than that of a planar MOSFET.

In addition, under the identical power transistor size, the proposed and conventional converters with 3.3 to 1.2 V conversion, 100 MHz operation frequency, and 2.5 A output current are simulated. At the peak and heavy loads, the proposed converter accomplished 3% and 11% higher efficiencies, respectively, than the conventional converter. Furthermore, efficiency as a function of the power transistor size indicated that the proposed converter can attain a 4.2% higher peak efficiency than the conventional converter with 26% smaller total transistor area. The above results suggests that the proposed converter with a cascode power stage including HS NMOS configuration using a vertical BC-MOSFET is a promising candidate toward next generation CMOS DC-DC converters.

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Chapter 7

Layout Design of Multi-pillar Type Vertical Body Channel MOSFET for CMOS DC-DC Converters

7.1. Introduction

DC-DC converters are key blocks for VLSI circuits such as microprocessor units, micro-controller units and etc. In order to reduce a conduction loss due to the Printed Circuit Board (PCB) trace, there is a demand to place DC-DC converters close to the load. It is found that the power dissipation in VLSI can be significantly suppressed by integrating DC-DC converters on-chip utilizing advanced digital CMOS, because it enables to realize per-core Dynamic Voltage and Frequency Scaling (DVFS) and low output impedance[1-8]. In order to convert the input-voltage V_{IN} into low output-voltage V_{OUT} utilizing low-voltage CMOS device efficiently, a cascode power switch which utilizes two MOSFETs connected in series as one power switch is widely applied in commercial CMOS DC-DC converters[1,6] as described in Fig. 7.1.

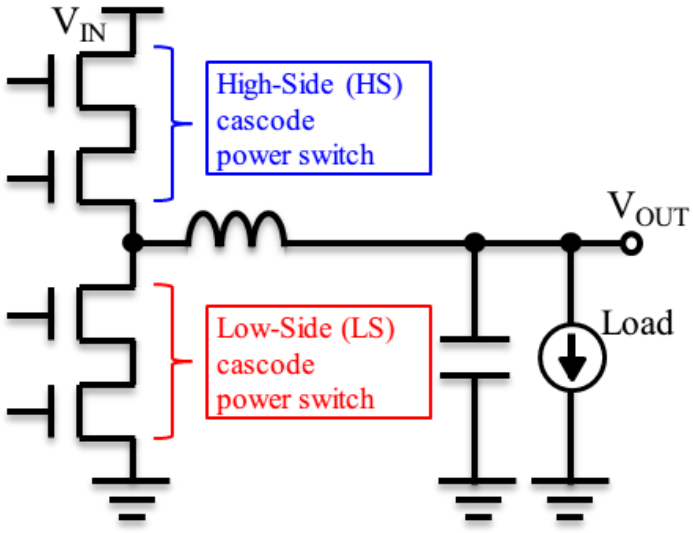


Figure 7.1. Schematic of the power stage of a CMOS DC-DC converter utilizing the cascode power switches [30].

The most critical requirements for CMOS DC-DC converters are high-efficiency and compactness under the operating condition of significantly high operation frequency (~100 MHz) and high-to-low voltage conversion (V_{IN} ~ 2.0 V, V_{OUT} ~ 0.8 V). In order to achieve compactness, operating the power switches under significantly high frequency is essential to reduce the size of passive elements such as inductors and capacitors in addition to suppress a transistor size. The high-to-low voltage conversion is essential to reduce power consumption and input-current of VLSI chip. Since the loss of power switches such as conduction loss and switching loss occupies large portion of the total loss in CMOS DC-DC converters, the study of CMOS DC-DC converters utilizing advanced digital CMOS device which has high current drivability, back bias free characteristic and compactness is exceptionally demanded.

A vertical Body-Channel (BC) MOSFET is one of the most promising devices for CMOS DC-DC converters because it provides high current drivability, back-bias free characteristic and compactness owing to its three-dimensional structure[9-17]. Figure 7.2 describes a bird's eye view of the vertical BC MOSFET. The vertical BC MOSFET arranges the source, gate and drain vertically. The top and bottom contacts and the bottom diffusion region contain certain parasitic resistance, thus the performance depends on the layout. Thanks to its high current drivability, a power switch composed of the vertical BC MOSFET can obtain low on-resistance in small transistor size. Owing to the back-bias free characteristic of the vertical BC MOSFET, High-Side N-type MOSFET (HS-NMOS) topology will be easily available without additional well structures such as a triple-well structure, and it further enhances the conversion efficiency of CMOS DC-DC converters in compared with High-Side P-type MOSFET (HS-PMOS) topology generally adopted to CMOS DC-DC converters utilizing planar CMOS device [18].

Multi-pillar type vertical BC MOSFET which is described in Fig. 7.3 has been proposed and its characteristics have been studied [19-22]. For a conventional non-cascode power switch composed of multi-pillar vertical BC MOSFET, it is found that a large drain current can be attained by locating bottom contact among silicon pillars because the effect of the parasitic resistance of bottom diffusion region is miniaturized [19]. Applications of multi-pillar vertical BC MOSFETs for charge pump circuit, CMOS inverter, core circuit of dynamic random access memory (DRAM) and etc. have been studied [23-29]. Nonetheless, a decidedly efficient and compact transistor layout of the cascode power switch which is suitable for CMOS DC-DC converters has

not found until yet.

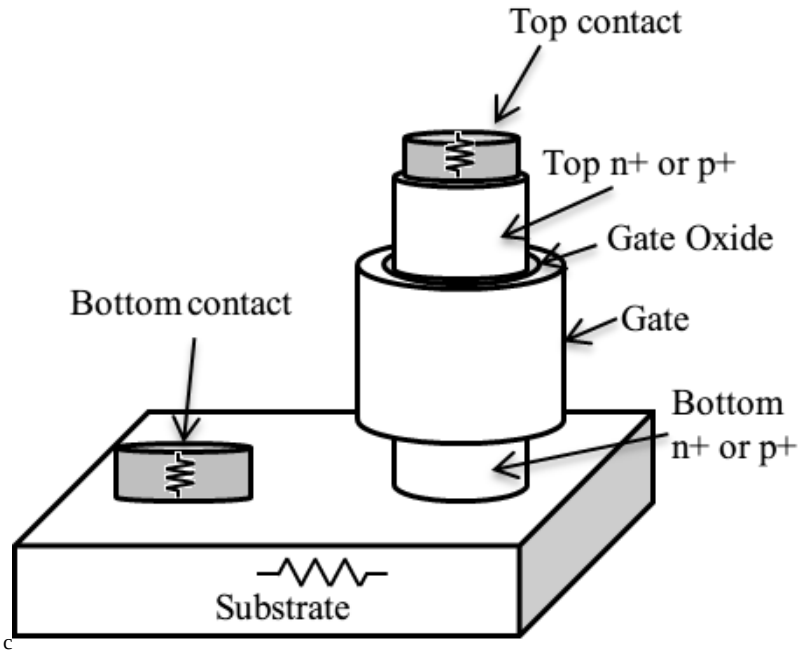


Figure 7.2. Bird's eye view of the vertical Body-Channel (BC) MOSFET [30].

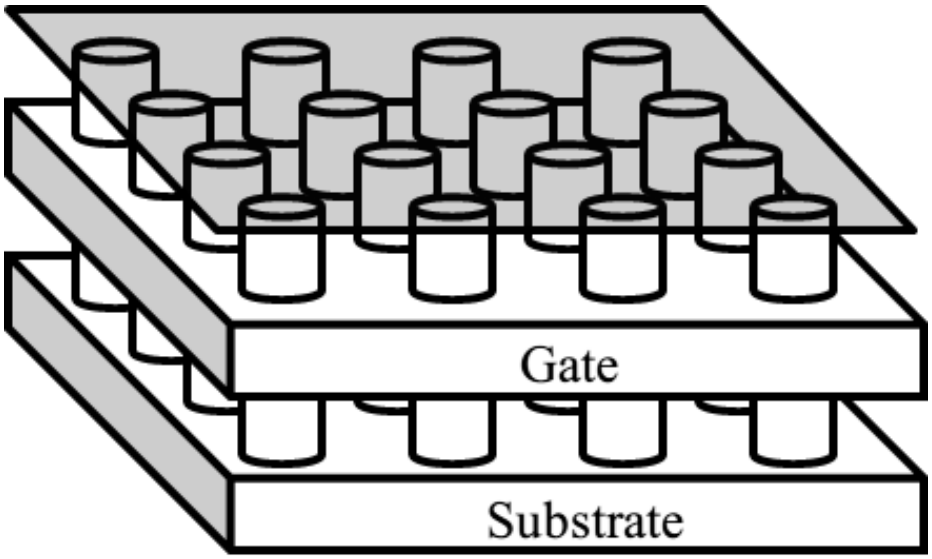


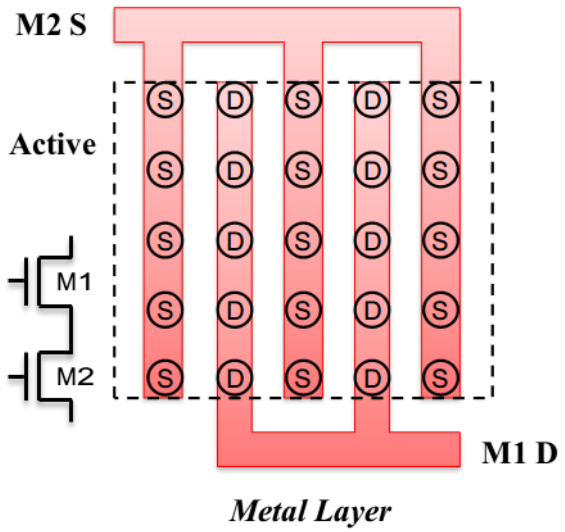
Figure 7.3. Bird's eye view of the multi-pillar type vertical BC MOSFET [30].

This chapter presents a novel transistor 0layout of multi-pillar type vertical BC MOSFET [30]. The series resistance of a cascode power switch composed of multi-pillar type vertical BC MOSFET is evaluated by utilizing the experimentally extracted BSIM4 transistor model of 60 nm vertical BC MOSFET. The loss utilizing the cascode power switch composed of multi-pillar type vertical BC MOSFET is comprehensively analyzed, which revealed the optimum design for achieving greatly efficient and compact CMOS DC-DC converters under the operating condition of 100 MHz operation frequency and low conversion ratio: the output-voltage V_{OUT} = 0.8 V and the input-voltage V_{IN} = 2.0 V.

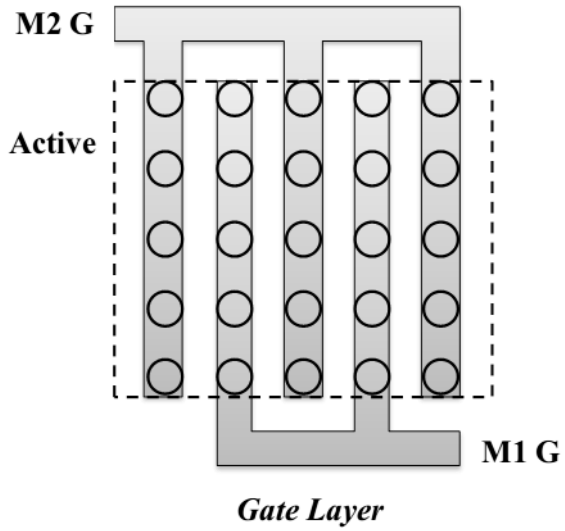
This chapter is organized as follows. The proposed layout of multi-pillar type vertical BC MOSFET is described in Sect. 7.2. The loss estimation and optimum design of a CMOS synchronous buck DC-DC converter is derived in Sect. 7.3. The efficiency and benchmark result of the 2.0 V to 0.8 V, 100 MHz CMOS DC-DC converter utilizing the proposed multi-pillar layout is presented in Sect. 7.4.

7.2. Proposed layout of multi-pillar type vertical BC MOSFET

For improving efficiency of CMOS DC-DC converters, utilizing cascode power switches which connects two MOSFETs in series is one of the most practical approaches. The top view of the proposed layout of multi-pillar type vertical BC MOSFET for cascode power switches is described in Fig. 7.4. "S" and "D" represent silicon pillars which utilize top node as source with bottom node as drain, and top node as drain and bottom node as source, respectively. The area surrounded by the broken square represents an active region, in other words, diffusion region on the substrate. In the transistor layout, the lower finger indicates M1 and the upper finger indicates M2. The metal and gate layer have a Stacked and Multi-Fingered (SMF) structure. The proposed layout shares the source of M1 and the drain of M2 on the diffusion layer instead of connecting the terminal via bottom contacts to reduce the effect of parasitic elements such as diffusion resistance and contact resistance.



(a)



(b)

Figure 7.4. Proposed stacked and multi-fingered layout of the multi-pillar type vertical BC MOSFET: (a) metal layer and (b) gate layer [30].

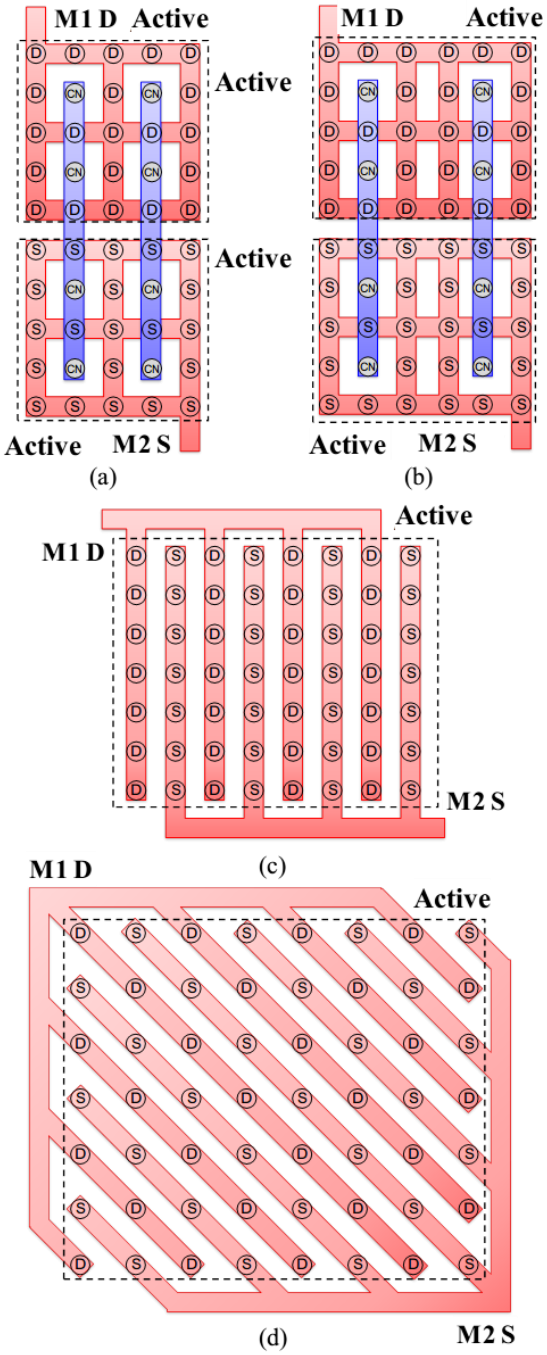
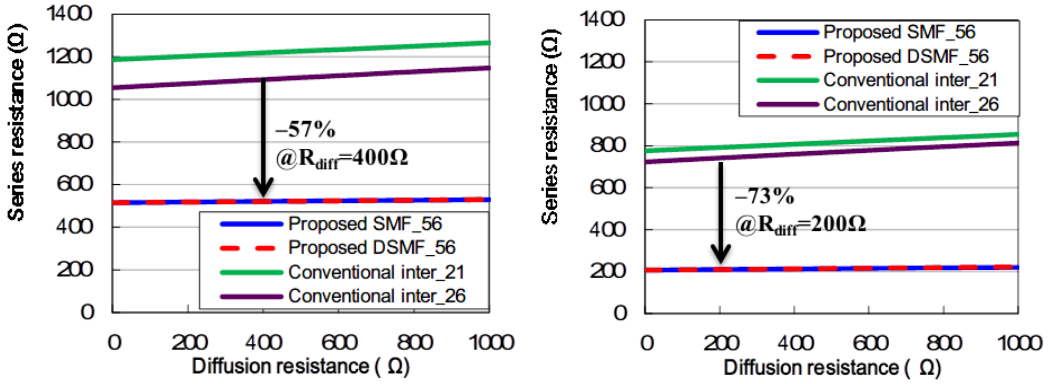


Figure 7.5. Layouts of multi-pillar type vertical BC MOSFETs for CMOS DC-DC converter applications: (a) conventional inter_21, (b) conventional inter_26, (c) proposed SMF_56, and (d) proposed DSMF_56 [30].

In order to verify the advantage of the proposed multi-pillar layout technique, the series resistance across the drain of M1 and the source of M2 is evaluated in compared with the conventional layout which has bottom contact among silicon pillars [19]. The evaluated layouts of multi-pillar type vertical BC MOSFET is illustrated in Fig. 7.5. The conventional layouts with the bottom contact are described in Figs. 7.5(a) and 7.5(b), namely *inter_21* and *inter_26*, and they have 4 intermediate bottom contacts which is represented as "CN" among 21 and 26 silicon pillars in each MOSFET, respectively. The MOSFETs M1 and M2 are connected in series via the bottom contacts to construct a cascode power switch. Hence, *inter_21* has 42 silicon pillars in the 5×10 pillar space, and Inter_26 has 52 silicon pillars in 6×10 pillar space. The proposed layouts are described in Figs. 7.5(c) and 7.5(d), namely *SMF_56* and *DSMF_56*, have 56 silicon pillars and *DSMF_56* has Diagonal connections in addition to the Stacked and Multi-Fingered layout (DSMF). Hence, *SMF_56* has 56 Si pillars in 8×7 pillar space, and *DSMF_56* have 56 silicon pillars in $8\sqrt{2} \times 7\sqrt{2}$ pillar space.

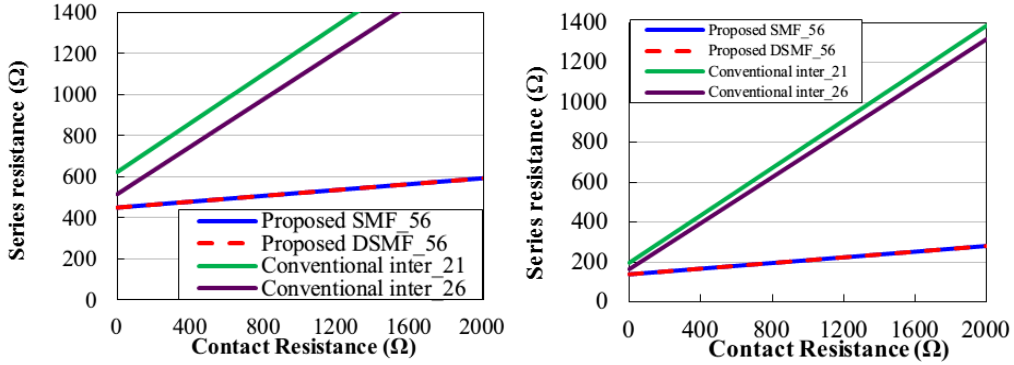
The series resistance across the drain of M1 and the source of M2 is evaluated by HSPICE simulation utilizing the resistance network model described in Ref. 19. The BSIM4 transistor models which is experimentally extracted from fabricated n-channel and p-channel 60 nm vertical BC MOSFETs are utilized [11]. The gate length and gate width of the fabricated vertical BC MOSFETs are 100 nm and 60π nm, respectively. The series resistance across M1 and M2 utilizing the proposed layouts as a function of the pillar-to-pillar diffusion resistance R_{diff} is described in Fig. 7.6, in compared with that of the conventional layouts. The contact resistance R_{co} of top and bottom contacts is constant as 1000 Ω. In the case of the p-channel MOSFET, the series resistance utilizing the proposed layouts is 57% lower than that of the conventional *inter_26* layout when $R_{diff} = 400\ \Omega$. In the n-channel MOSFET, the series resistance is 73% lower than that of the conventional *inter_26* layout. Both *SMF_56* and *DSMF_56* have significantly lower series resistance than the conventional layouts. The series resistance as a function of the contact resistance is also described in Fig. 7.7. The pillar-to-pillar diffusion resistances are constant as 400 Ω for p-channel MOSFET and 200 Ω for n-channel MOSFET. It can be observed that the series resistance of the conventional layouts becomes much larger than the proposed layouts with the increase of the contact resistance, because the conventional layouts connect the source of M1 and the drain of M2 via bottom contacts which have large parasitic resistance. Since the increase of the series resistance due to the contact resistance can be suppressed by utilizing the proposed layout, the proposed

SMF layout can lower the conduction loss in CMOS DC-DC converters.



(a) (b)

Figure 7.6. Diffusion resistance dependence of the series resistance of M1-M2 with the proposed and conventional layouts: (a) p-channel MOSFET and (b) n-channel MOSFET [30].



(a) (b)

Figure 7.7. Contact resistance dependence of the series resistance of M1-M2 with the proposed and conventional layouts: (a) p-channel MOSFET and (b) n-channel MOSFET [30].

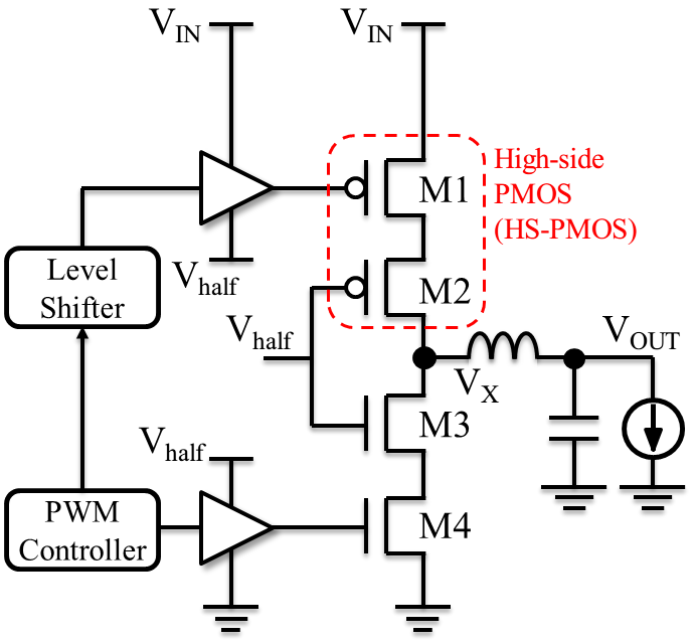
7.3. Loss estimation and optimum design of CMOS DC-DC converters with the proposed layout

In order to reveal the optimum design of the CMOS DC-DC converters whose cascode power switches are composed of multi-pillar vertical BC MOSFETs, the loss of each MOSFET in CMOS DC-DC converters is analyzed for both of HS-PMOS and HS-NMOS topologies. Figure 7.8(a) describes a circuit diagram of the CMOS DC-DC converter with HS-PMOS topology. The HS cascode power switch is composed of M1 and M2, and the Low-Side (LS) cascode power switch is composed of M3 and M4. V_{half} represents the half-rail input-voltage which is generally generated by an external linear regulator, and V_X represents the switching node voltage. The HS-PMOS topology is widely adopted in CMOS DC-DC converters utilizing planar MOSFETs for power switches due to its simple circuit configuration. Figure 7.8(b) describes the HS-NMOS topology proposed in Ref. 17. By utilizing the HS-NMOS topology with vertical BC MOSFET, a conduction loss can be lowered without additional well structures such as a triple-well structure, because the mobility of the n-channel MOSFET is much higher than the p-channel MOSFET, and the on-resistance increase due to the back bias effect becomes negligible.

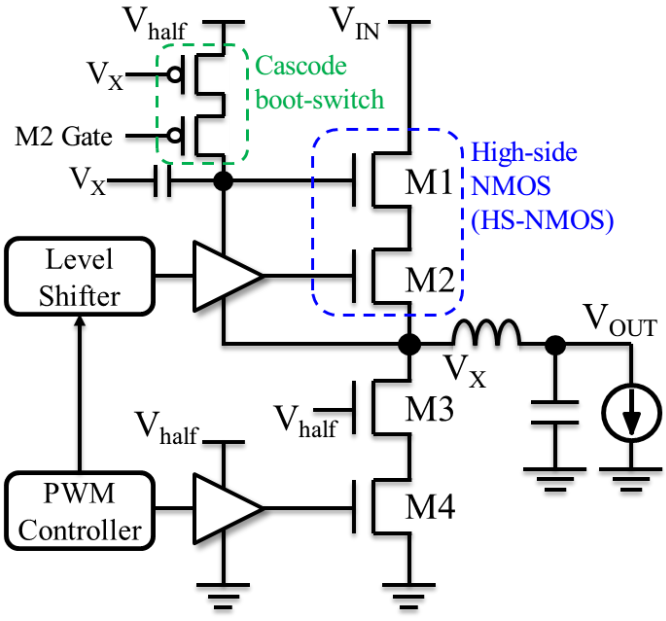
The conduction loss in each MOSFET can be expressed as following equation,

$$P_{cond} = \alpha \frac{r_{ds}}{W} \left(I_L^2 + \frac{I_R^2}{3} \right) \quad (1)$$

where r_{ds} is an on-resistance per gate width, W is a gate width of the MOSFET, α is a duty cycle of the MOSFET, I_L is an inductor current, and I_R is a ripple current. The parasitic resistances R_{diff} and R_{co} are included to the on-resistance.



(a)



(b)

Figure 7.8. Schematic of the cascode CMOS DC-DC converters: (a)HS-PMOS and (b)HS-NMOS topologies [17].

The switching loss can be estimated by summing the energy of the charge of parasitic capacitances. The equivalent circuit models of HS and LS cascode power switches in the case of HS-PMOS topology is described in Figs. 7.9(a) and 7.9(b), respectively. The switching losses due to parasitic capacitances for MOSFETs M1-M4 can be expressed as following equations:

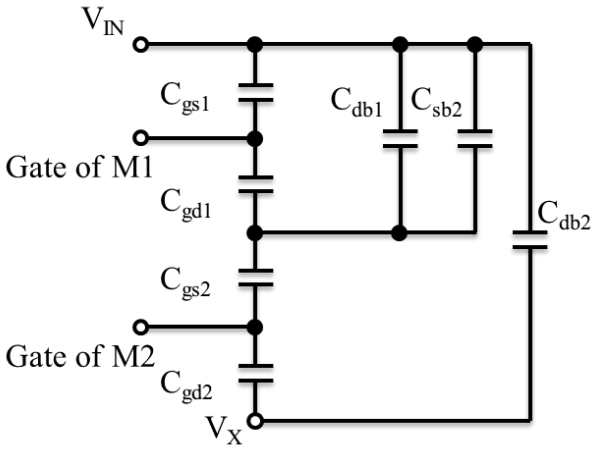
$$P_{cap(M1,p)} \approx \left\{C_{gs1}\left(V_{IN} - V_{half}\right)^2 + C_{gd1}\left(V_{half} + V_{Pdrv} - 2V_{IN} - V_{th,p}\right)^2 + C_{db1}\left(V_{half} - V_{IN} - V_{th,p}\right)^2\right\} f_{SW} \quad (1)$$

$$P_{cap(M2,p)} \approx \left\{C_{gs2}\left(V_{IN} - V_{half} + V_{th,p}\right)^2 + C_{gd2}V_{IN}^2 + C_{db2}V_{IN}^2 + C_{sb2}\left(V_{IN} - V_{half} + V_{th,p}\right)^2\right\} f_{SW} \quad (2)$$

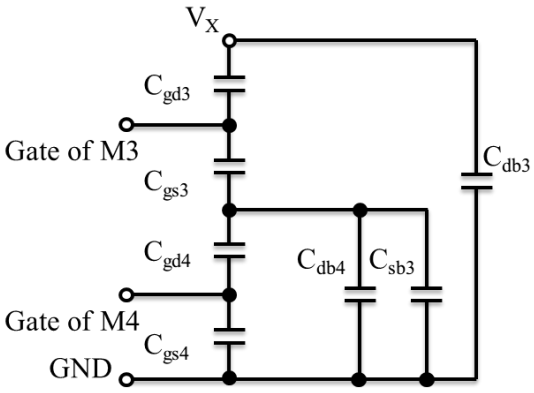
$$P_{cap(M3,n)} \approx \left\{C_{gs3}\left(V_{half} - V_{th,n}\right)^2 + C_{gd3}V_{IN}^2 + C_{db3}V_{IN}^2 + C_{sb3}\left(V_{half} - V_{th,n}\right)^2\right\} f_{SW} \quad (3)$$

$$P_{cap(M4,n)} \approx \left\{C_{gs4}\,V_{Ndrv}^2 + C_{gd4}\left(V_{half} - V_{th,n} + V_{Ndrv}\right)^2 + C_{db4}\left(V_{half} - V_{th,n}\right)^2\right\} f_{SW} \quad (4)$$

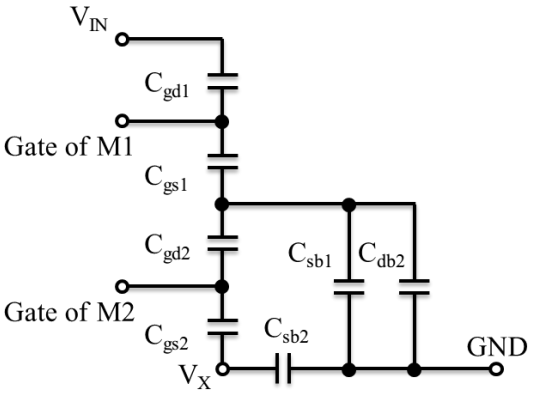
where C_{gsi}, C_{gdi}, C_{dbi}, and C_{sbi} are gate-to-source capacitance, gate-to-drain capacitance, drain-to-bulk capacitance, and source-to-bulk capacitance of the MOSFET Mi, respectively. $V_{th,p}$ and $V_{th,n}$ represent the threshold voltage of p-channel and n-channel MOSFETs. V_{Pdrv} and V_{NDrv} are the gate driving voltages of HS and LS power switches, and f_{SW} is a operation frequency of the converter. In the case of the HS-NMOS topology is applied, the model of HS cascode power switch must be replaced to the HS-NMOS model described in Fig. 7.9(c).



(a)



(b)



(c)

Figure 7.9. Models of the power switches M1–M4 and the voltage swings at the terminals of various cascode configurations: (a) HS-PMOS, (b) LS-NMOS, and (c) HS-NMOS [30].

Hence, Eqs. (2) and (3) are also replaced to the following equations:

$$P_{cap(M1,n)} \approx \left\{C_{gs1}\left(V_{Ndrv,bst} + V_{th,n}\right)^2 + C_{gd1}\left(V_{IN} + V_{Ndrv,bst} - V_{half}\right)^2 + C_{db1}\left(V_{IN} - V_{half} + V_{th,n}\right)^2\right\} f_{SW} \quad (5)$$

$$P_{cap(M2,n)} \approx \left\{C_{gs2}\, V_{Ndrv,bst}^2 + C_{gd2}\left(V_{Ndrv,bst} + V_{half} - V_{th,n}\right)^2 + C_{db2}\left(V_{IN} - V_{half} + V_{th,n}\right)^2 + C_{sb2}V_{IN}^2\right\} f_{SW} \quad (6)$$

where $V_{Ndrv,bst}$ is the boot-strap gate driving voltage of the HS-NMOS cascode power switch. Figures 7.10(a)- 7.10(c) show the gate width models of the driver transistors in the CMOS DC-DC converter of the HS-PMOS, LS-NMOS, HS-NMOS switches, respectively, where W_{Mi} is the gate width of MOSFET M_i, *ap* and *an* are tapering factors of p-channel and n-channel MOSFETs, *b* is the ratio of gate widths of p-channel and n-channel MOSFETs. The output of the HS driver is connected to M1 in the case HS PMOS topology, while it is connected to M2 in the case of HS NMOS topology. Utilizing these models, the switching loss generated at gate drivers can be derived by calculating the energy of parasitic capacitances of the all the driver transistors considering the tapering factors as following equations, for the driver of HS-PMOS cascode power switch:

$$P_{drive(M1,p)} \approx \frac{1}{ap - b - 1}\{b\left(2C_{gd,PMOS} + C_{gs,PMOS} + C_{db,PMOS}\right) + \left(2C_{gd,NMOS} + C_{gs,NMOS} + C_{db,NMOS}\right)\}(V_{IN} - V_{Pdrv})^2 f_{sw} W_{M1} \quad (7)$$

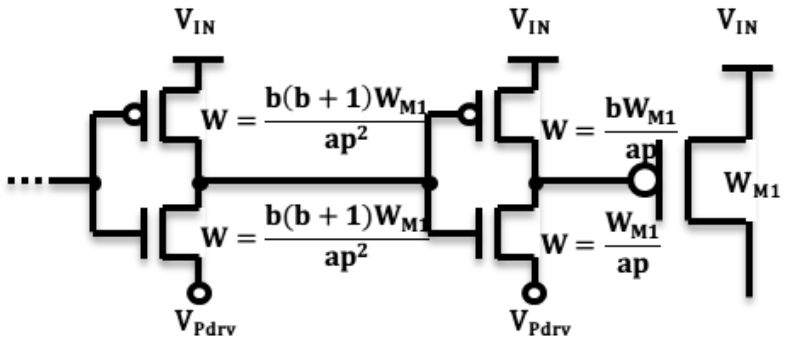
for the driver of LS-NMOS cascode power switch:

$$P_{drive(M4,n)} \approx \frac{1}{an - b - 1}\{b\left(2C_{gd,PMOS} + C_{gs,PMOS} + C_{db,PMOS}\right) + \left(2C_{gd,NMOS} + C_{gs,NMOS} + C_{db,NMOS}\right)\}V_{Ndrv}{}^2 f_{sw}\, W_{M4} \quad (8)$$

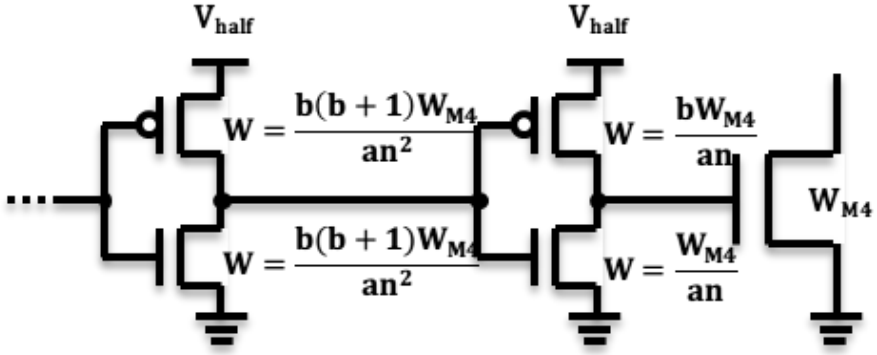
for the driver of HS-NMOS cascode power switch:

$$P_{drive(M2,n)} \approx \frac{1}{an - b - 1}\{b\left(2C_{gd,PMOS} + C_{gs,PMOS} + C_{db,PMOS}\right) + \left(2C_{gd,NMOS} + C_{gs,NMOS} + C_{db,NMOS}\right)\}V_{Ndrv,bst}{}^2 f_{sw} W_{M2} \quad (9)$$

where $C_{gd,PMOS}$, $C_{gs,PMOS}$, and $C_{db,PMOS}$ represent gate-to-drain, gate-to-source, drain-to-bulk capacitances per gate width of p-channel MOSFET, and $C_{gd,NMOS}$, $C_{gs,NMOS}$, and $C_{db,NMOS}$ represent those of n-channel MOSFET.



(a)



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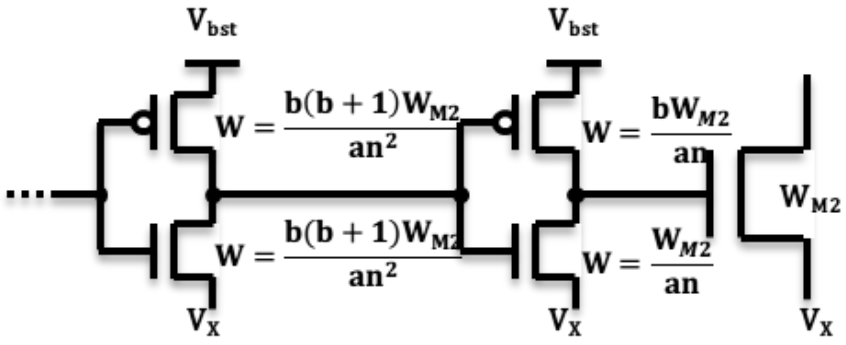


(c)

Figure 7.10. Gate width models of driver transistors: (a) HS-PMOS, (b) LS-NMOS and (c) HS-NMOS [30].

The loss of the MOSFETs M1-M4 utilizing the proposed SMF layout is analyzed from Eqs. (1)-(10) and described in Fig. 7.11 as a function of the gate width. The operating conditions of the CMOS DC-DC converter are as follows: V_{IN} = 2.0 V, V_{half} = 1.0 V, V_{OUT} = 0.8 V, I_L = 0.5 A, I_R = 0.5 A, and f_{SW} = 100 MHz. The multi-pillar

type vertical BC MOSFETs which utilize the Bottom Node as the Drain (BND) and Bottom Node as the Source (BNS) are individually evaluated. When the gate width is small, the conduction loss becomes dominant while the switching loss becomes dominant when the gate width is large, owing to the gate width dependence of both conduction loss and switching loss. The optimum gate width of each MOSFET can be derived by finding the minimum value of the loss. The loss of M2 utilizing HS-NMOS topology with BNS and M3 with BND is larger than that with the opposite bottom node polarity. This is induced by the switching loss due to the parasitic capacitance on the bottom diffusion layer connected to V_X which swings from 0 V to V_{IN} in every switching cycle. Note that in order to share the drain and source on the diffusion layer, the source of M1, the drain of M2, the source of M3, the drain of M4 must be the bottom node in HS-NMOS topology, or the additional bottom contacts which increase the series resistance will be required. Therefore, the most preferable combination for CMOS DC-DC converters is M1 with BNS, and M2 with BND, M3 with BNS and M4 with BND utilizing the HS-NMOS topology, which has the lowest losses of 11 mW, 8.8 mW, 8.1 mW, and 8.2 mW, respectively.

Figure 7.12 describes the optimum gate width of M1-M4 as a function of the duty cycle. The optimum gate width of MOSFETs M1 and M2 which compose the HS cascode power switch exceeds 40 mm when the duty cycle is 0.80 in the case of HS-PMOS topology. Meanwhile, in the case of HS-NMOS topology, the optimum gate width is below 30 mm at the duty cycle is 0.80, which indicates the HS-NMOS topology makes CMOS DC-DC converters compact.

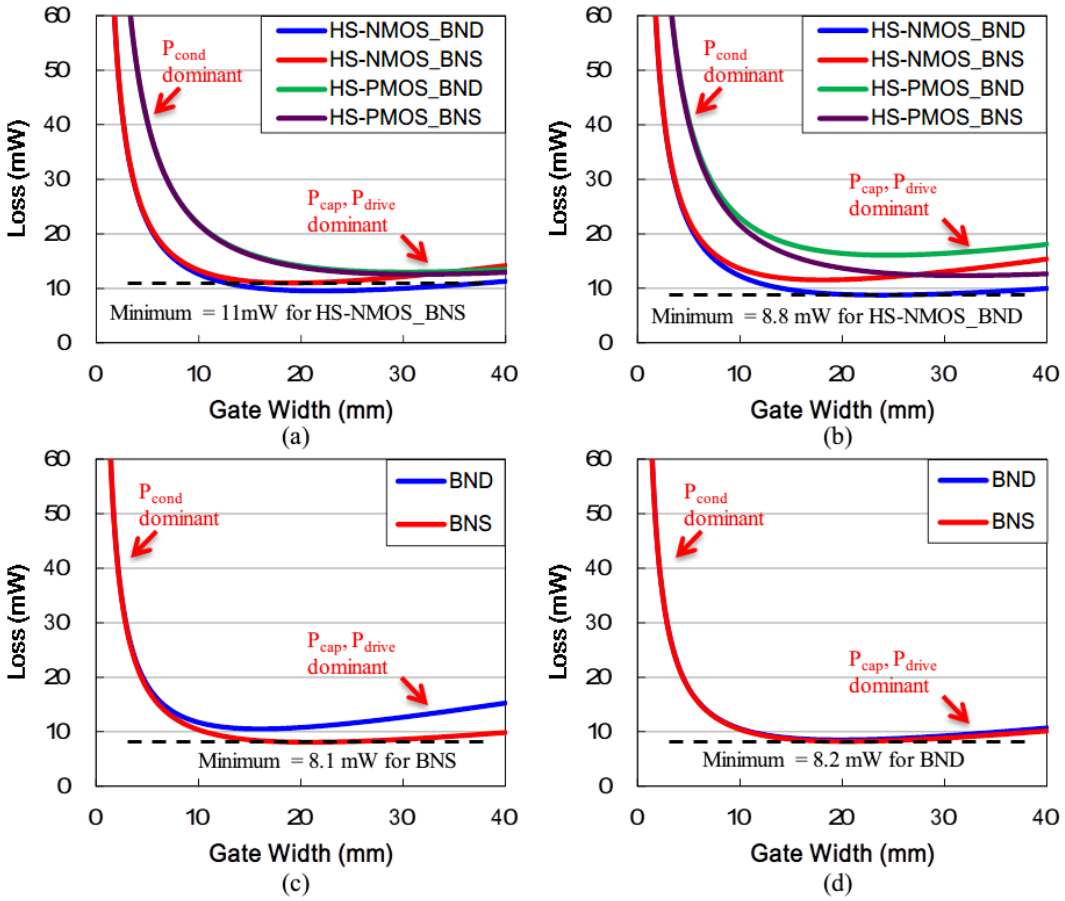


Figure 7.11. Loss of the power switches as a function of the gate width: (a) M1, (b) M2, (c) M3, and (d) M4 [30].

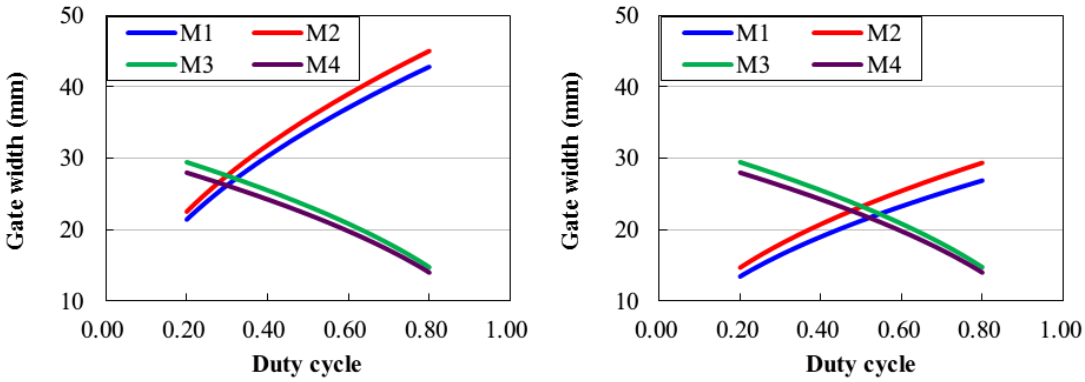


Figure 7.12. Optimum gate widths of MOSFETs M1-M4 for (a) HS-PMOS and (b) HS-NMOS topologies [30].

Figure 7.13 describes the total optimum gate width of M1-M4 with the proposed SMF layout. Utilizing the HS-NMOS topology, the total gate width can be suppressed by 27% from the HS-PMOS topology at the duty cycle is 0.80. The total loss of the power MOSFETs M1-M4 at the optimum gate widths are described in Fig. 7.14. The impact of reduction of the optimum gate width and the total loss becomes significant according to the duty cycle because the on-time of HS cascode power switch becomes long. The total loss with the HS-NMOS topology is suppressed by 16% in compared with the HS-PMOS topology at the duty cycle is 0.80. Hence, in order to realize the greatly efficient and compact CMOS DC-DC converter, the HS-NMOS topology with the proposed SMF layout is suitable for future on-chip power conversion.

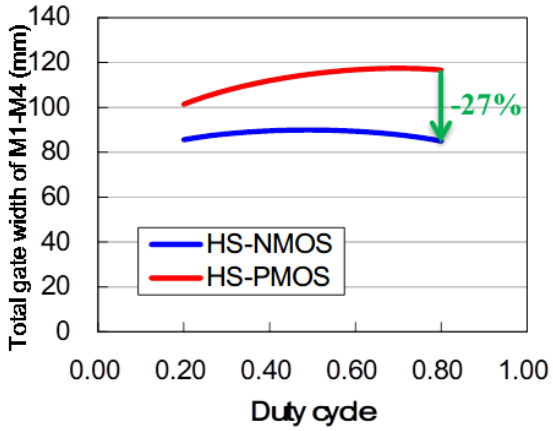


Figure 7.13. Duty cycle dependence of total gate width of the power switches M1-M4 with the proposed layout [30].

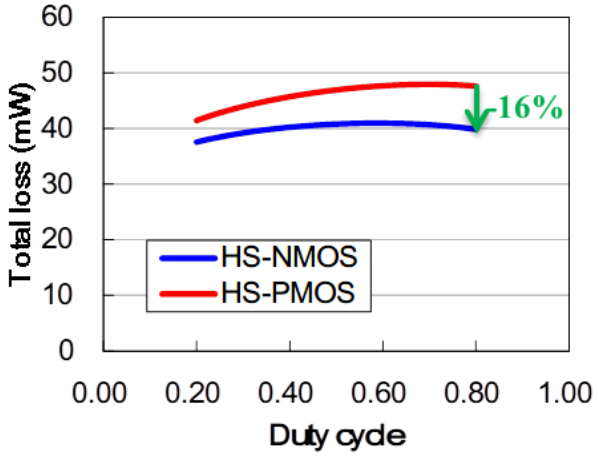
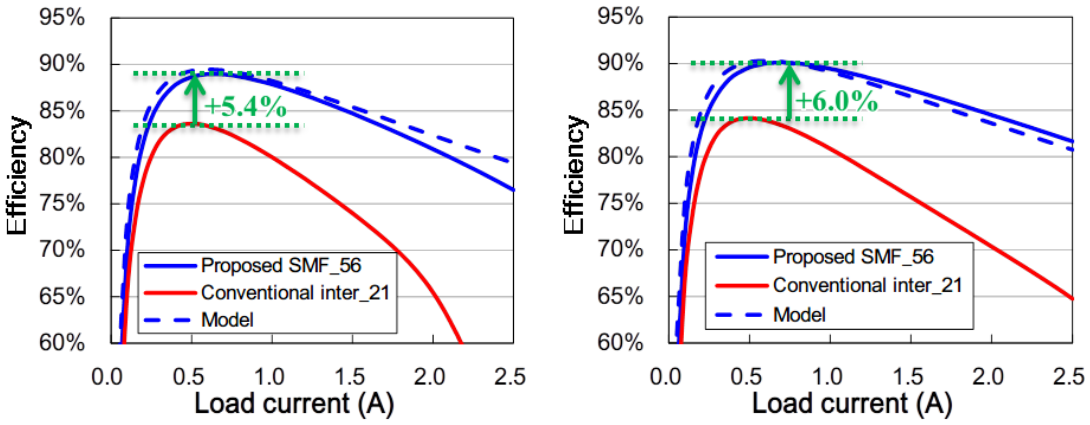


Figure 7.14. Duty cycle dependence of total loss of the power switches M1 to M4 with the proposed transistor layout [30].

7.4. Results of the DC-DC Converter and its Bench-marking

The transient simulation of the cascode CMOS DC-DC converters which are described in Figs. 7.8(a) and 7.8(b) is carried out to validate the advantage of the proposed multi-pillar layout with 60 nm vertical BC MOSFET. The parameters utilized in this estimation are listed in Table 7.I.

The efficiency curves are described in Fig. 7.15. The broken line represents the model value numerically calculated from Eqs. (1)-(10). The efficiency of the converter with the conventional *inter_21* layout whose number of silicon pillars is identical to the converter with the proposed layout is also indicated for the comparison purpose. It can be seen that the numerical model values are in good agreement with the transient simulation value within a full load range from 0 A to 2.5 A. The peak efficiencies are 89.0% for HS-PMOS and 90.1% for HS-NMOS topology. In compared with the CMOS DC-DC converters with the conventional *inter_21* layout, the peak efficiencies of the converters with the proposed *SMF_56* layout is enhanced by 5.4% and 6.0 % for HS-PMOS and HS-NMOS topologies, respectively.



(a) (b)

Figure 7.15. Efficiency curves of the CMOS DC-DC converters with the multi-pillar vertical BC MOSFET with R_{diff}=200 Ω and R_{co}=1000 Ω for (a) HS-PMOS and (b) HS-NMOS topologies [30].

The benchmark table of the CMOS DC-DC converters with the proposed *SMF_56* layout in compared with the conventional *inter*_21 layout is listed in Table 7.II. Because the bottom contact is removed by the shared source and drain in the proposed *SMF_56* layout, the size of MOSFETs M1-M4 is suppressed by 16% for both HS-PMOS and HS-NMOS topologies. Furthermore, at the heavy load region which has the load current I_O = 2 A, the efficiency improvements are as much as 15.4% and 14.1% for HS-PMOS and HS-NMOS topologies respectively, thanks to the advantage of the parasitic elements reduction by utilizing the proposed SMF layout.

7.5. Conclusions

A novel transistor layout of multi-pillar type vertical BC MOSFET is proposed to realize greatly efficient and compact cascode CMOS DC-DC converters. The proposed multi-pillar layout features the stacked and multi-fingered structure, and the drain and the source are shared on the bottom node of multi-pillar type vertical BC MOSFETs instead of connecting via bottom contacts, thus the loss due to the parasitic elements such as the contact resistance, pillar-to-pillar diffusion resistance, and bottom junction capacitance can be suppressed. From the analytical results of the loss in each MOSFET which forms cascode power switches, it is revealed that the total optimum gate width and total loss with the HS-NMOS topology are 27% and 16% smaller than that with HS-PMOS topology, respectively.

Furthermore, in order to validate the advantage of the proposed layout, CMOS DC-DC converters with HS-PMOS and HS-NMOS topologies with the proposed multi-pillar layout are individually simulated utilizing BSIM4 transistor models which are experimentally extracted from fabricated 60 nm vertical BC MOSFETs. From the results, by utilizing the proposed layout, the peak efficiency became approximately 90% under the condition of f_{SW} = 100 MHz, V_{IN} = 2.0 V, and V_{OUT} = 0.8 V, which is 5.4% and 6.0% higher than that utilizing the conventional layout for HS-PMOS and HS-NMOS topologies respectively, reducing the total transistor size by 16% at the same time. From all of the above, the proposed layout of the multi-pillar type vertical BC MOSFET is a promising candidate for greatly efficient and compact CMOS DC-DC converter applications.

Table 7.I. Parameters of the simulated CMOS DC-DC converters for both HS-PMOS and HS-NMOS topologies [30].

Input voltage V_{IN}	**2.0 V**
Half-rail voltage V_{half}	**1.0 V**
Output voltage V_{OUT}	**0.8 V**
Inductance	**4 nH**
Output capacitance	**10 µF**
Bootstrap capacitance (High-side NMOS only)	**400 pF**
Crossover frequency	**10 MHz**
Switching frequency f_{SW}	**100 MHz**
MOSFET model	**BSIM4 60 nm Vertical BC MOSFET model extracted from experimental data.**

Table 7.II. Benchmark table of the CMOS DC-DC converters utilizing the proposed multi-pillar layout in compared with that of the conventional multi-pillar layout [30].

Topology	**HS-PMOS (See Fig. 7.8 (a))**		**HS-NMOS (See Fig. 7.8 (b))**	
Multi-pillar layout	**Prop. SMF_56**	**Conv. Inter_21**	**Prop. SMF_56**	**Conv. Inter_21**
Area of M1-M4 (F^2)	**2,376,120** ← –16%	**2,828,715**	**1,901,200** ← –16%	**2,263,333**
Peak efficiency	**89.0%** ← +5.4%	**83.6%**	**90.1%** ← +6.0%	**84.1%**
Efficiency at I_O=2 A	**80.9%** ← +15.4%	**65.5%**	**84.5%** ← +14.1%	**70.4%**

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Chapter 8

Conclusions

8.1. Summary and Conclusion

In chapter 3, accurate and low-loss current sensing method utilizing a precision sensing resistor is presented. The proposed method utilizes an auxiliary switch to suppress the conduction loss in the sensing resistor. A parametric estimation utilizing typical specifications of resistive sensors is performed in terms of the averaged equivalent resistance and accuracy, which suggests the importance of designing sampling duty cycle small in the proposed method. The benchmark result based on the parametric estimation indicated that the proposed method with sampling duty cycle of 0.10 can archive 47% higher accuracy with a slightly higher conduction loss in compared with the conventional inductor DCR sensing.

Furthermore, the prototype current sensing circuit utilizing the proposed method is constructed on the 12 V to 1.0 V, 20 A digitally controlled synchronous buck DC-DC converter, and the proposed sensing operation is demonstrated. The digital output of the current sensing circuit has a good linearity within a load range from 0 A to 20 A, and the measured LSB was 33.8 LSB/A which is +3.3% from the ideal value. From the above, the current sensing circuit with the proposed method is a promising candidate for future DC-DC converter applications including VRMs.

In chapter 4, loss in parallel MOSFET topology with adaptive control is analyzed. From numerical estimation, conduction loss in MOSFET at near the boundary current reaches 98% of loss at the maximum load. To overcome this issue, switch toggling technique is proposed and simulated. From the results, in case that three MOSFETs are connected in parallel, maximum temperature increase of high-side and low-side MOSFETs are suppressed 64% and 59% when one MOSFET is driven, and 32% and 27% when two MOSFETs are driven respectively. Furthermore, on resistance of the low-side MOSFET under circuit operation is decreased by 13% because operating temperature of MOSFET is decreased. It is promising result for efficiency improvement of power electronic circuits.

In chapter 5, a concept of inductor current to digital converter is presented. The feature of the proposed ICDC is to convert DC and ripple component of inductor

current to digital data separately and simultaneously with small number of components, which was hard for conventional ADCs. Proposed ICDC is designed and simulated with 12 V to 1 V buck converter, and successfully converted the 10 A of DC component with 5 A of ripple component to digital data. Input range of DC and ripple component are 0 A to 14.4 A and 4 A to 6 A with 65 mA maximum quantization error respectively, which are sufficient to convert inductor current in DC-DC converter to digital data. Therefore, the proposed ICDC is promising candidate to inductor current digitalizing circuit in digitally controlled DC-DC converter.

In chapter 6, for improving efficiency under very high operation frequency, we proposed DC - DC converter with power stage by cascode bridge of high side NMOS configuration composed of vertical type MOSFET. From the performance simulation result of the cascode power switch under the high side condition, we found that The proposed high-side switch with vertical NMOS attains outstanding performance that is +85% superior to the conventional planar p-channel MOSFET at a voltage of 0.10 V in terms of the on current. Furthermore, we clarified the advantage that the voltage distribution in the off-state of the proposed cascode power switch with the vertical NMOS is more uniform than when using the planar type.

The proposed and conventional CMOS DC-DC converters with specification that is 3.3 V-1.2 V, 100 MHz switching, and 2.5 A output capability, are simulated with the identical MOSFET size. The proposed CMOS DC-DC converter attained 3% higher efficiency at peak, and 11% higher efficiency at heavy loads, respectively, compared to the conventional CMOS DC-DC converter. Furthermore, efficiency as a function of the MOSFET size suggested that the proposed CMOS DC-DC converter is able to accomplish higher peak efficiency by 4.2% than the conventional CMOS DC-DC converter with -26% total MOSFET size in power stage. Therefore, proposed DC - DC converter with power stage by cascode bridge of high side NMOS configuration composed of vertical BC MOSFET is considered extremely useful for future CMOS DC - DC converters.

In chapter 7, a novel transistor layout of multi-pillar type vertical BC MOSFET is proposed to realize efficient and compact cascode CMOS DC-DC converters. The proposed multi-pillar layout features the stacked and multi-fingered structure, and the drain and the source are shared on the bottom node of multi-pillar type vertical BC MOSFETs instead of connecting via bottom contacts, thus the loss due to the parasitic elements such as the contact resistance, pillar-to-pillar diffusion resistance, and bottom

junction capacitance can be suppressed. From the analytical results of the loss in each MOSFET which forms cascode power switches, it is revealed that the total optimum gate width and total loss with the HS-NMOS topology are 27% and 16% smaller than that with HS-PMOS topology, respectively.

Furthermore, in order to validate the advantage of the proposed layout, CMOS DC-DC converters with HS-PMOS and HS-NMOS topologies with the proposed multi-pillar layout are individually simulated utilizing BSIM4 transistor models which are experimentally extracted from fabricated 60 nm vertical BC MOSFETs. From the results, by utilizing the proposed layout, the peak efficiency became approximately 90% under the condition of f_{SW} = 100 MHz, V_{IN} = 2.0 V, and V_{OUT} = 0.8 V, which is 5.4% and 6.0% higher than that utilizing the conventional layout for HS-PMOS and HS-NMOS topologies respectively, reducing the total transistor size by 16% at the same time. From all of the above, the proposed layout of the multi-pillar type vertical BC MOSFET is a promising candidate for efficient and compact CMOS DC-DC converter applications.

8.2. Future Works

This thesis is devoted to present novel power management techniques and highly efficient and highly embedded CMOS DC-DC converters toward future microprocessor power supply. This thesis proved the validities of the proposed circuits or techniques quantitatively; however some future works are remains to be adopted in practical use for industry.

Chapter 3 presented and demonstrated a novel current path narrowing method for highly accurate and low-loss current sensing. The prototype board with a DC-DC converter composed of silicon power MOSFETs demonstrated its loss reduction scheme under the operation. Since the DC - DC converter demonstrated in this research is one kind, the influence of the error generated by the attenuation term of the choke inductor such as the ripple current could not be quantitatively evaluated, and thus it is a future work. In addition, it remains some room for improvement by applying low-loss GaN-on-Si power device because the implementation of the proposed method is not constrained to the kind of power devices. By adopting GaN-on-Si power devices which are expected for higher frequency and lower loss than Si power devices, the loss caused by power semiconductor devices will shrink, and then the impact on the ratio of loss

reduction in DC-DC converters becomes more significant. Therefore, the demonstration using GaN-on-Si power devices will have a certain value.

In chapter 4, a novel switch toggling technique is presented to suppress temperature increase in adaptive FET drive modulation, which is a key efficiency enhancement technique within wide load current range. This thesis verified the effect of temperature increase by using an equivalent thermal circuit which is operated under HSPICE circuit simulation. Despite this estimation is valid in ideal conditions, more practical estimation including whole components and wirings on the motherboard should be performed using electro-thermal simulators. The proposed technique is also appropriate for applications which vary the load within wide range, exploration and demonstration with the other promising applications such as IoT smart sensors might be important for future.

Chapter 5 presented a novel inductor current to digital converter which has a small number of components compared to the conventional ADCs. The proposed circuit is systematically evaluated and verified using analog-mixed-signal simulation using Simetrix. Even though the proposed circuit might consume less size because the proposed circuits uses components which are similar to the conventional ADCs, the quantitative evaluation of the size of the proposed circuit compared to the conventional ADCs should be performed under the same process technology.

Chapter 6 proposed a novel high-side NMOS cascode DC-DC converter using vertical BC MOSFETs. The proposed circuit uses vertical BC-MOSFETs because it is free from the performance degradation due to back-bias effect. This thesis verified the high-input-voltage capability by using BSIM4 vertical BC MOSFET model extracted from experimental data, the robustness to the high-voltage considering the all p-n junctions should be experimented more carefully using actual cascode power switch composed of vertical BC-MOSFETs. In addition, despite the high-voltage level shifter have been verified using vertical BC MOSFETs in a literature [1], more analog RF circuit verification such as feedback circuits, ADCs should be verified to realize highly efficient and highly embedded DC-DC converters completely made of vertical BC MOSFETs.

Chapter 7 provided a novel transistor layout with multi-pillar type vertical BC MOSFETs for highly efficient and compact cascode CMOS converters. The proposed transistor layout is verified in the single-stacked multi-pillar vertical MOSFET. Since the vertical BC MOSFETs are expected to achieve compact LSI with vertical stacking

[2], the proposed layout should be evaluated using the two or more vertically stacked multi-pillar type vertical BC MOSFETs.

Finally, in order to completely prove the validity of the techniques proposed in this thesis to the engineering field, it is necessary to conduct an overall verification integrating all of the future microprocessor (e.g. NV-MPUs), motherboard DC-DC converter, and CMOS DC-DC converter using the vertical BC-MOSFET and its power management circuit which are proposed in this research from view point of the total system.

References for Chapter 8

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List of Publications

Journals

1. **Kazuki Itoh** and Tetsuo Endoh, “Loss Analysis and Optimum Design of a Highly Efficient and Compact CMOS DC-DC Converter with Novel Transistor Layout Using 60 nm Multi-pillar Type Vertical Body Channel MOSFET,” Jpn. J. Appl. Phys., (in press).
2. **Kazuki Itoh**, Masakazu Muraguchi, and Tetsuo Endoh, “Integrated voltage regulators with high-side NMOS power switch and dedicated bootstrap driver using vertical body channel MOSFET under 100 MHz switching frequency for compact system and efficiency enhancement,” Jpn. J. Appl. Phys., vol. 56, no. 4S, p. 04CF14, Apr. 2017.
3. **Kazuki Itoh** and Tetsuo Endoh, “A Novel Alternating Voltage Controlled Current Sensing Method for Suppressing Thermal Dependency,” IEICE Trans. Electron., vol. E97–C, no. 5, pp. 431–437, 2014.
4. **Kazuki Itoh** and Tetsuo Endoh, “Low-Loss Design of Highly Accurate Current Sensing with Current Path Narrowing Method for Switched-Mode DC-DC Converters and its Demonstration,” IEEE Trans. Power Electron., (in peer review).
5. **Kazuki Itoh** and Tetsuo Endoh, “Novel inductor current to digital converter and its concept evaluation,” Jpn. J. Appl. Phys., (in preparation).
6. **Kazuki Itoh** and Tetsuo Endoh, “Switch Toggling Technique of Parallel MOSFET Topology for Power Electronics Circuits with Uniform Thermal Distribution,” Jpn. J. Appl. Phys., (in preparation).

International Conferences

1. **Kazuki Itoh** and Tetsuo Endoh, “Highly Efficient and Compact CMOS DC-DC Converter with Novel Transistor Layout of 60 nm Multi-pillar Type Vertical Body Channel MOSFET,” in International Conference on Solid State Devices and Materials, Sept. 2017.
2. **Kazuki Itoh**, Masakazu Muraguchi, and Tetsuo Endoh, “Novel inductor current to digital converter and its concept evaluation,” in 2016 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD), 2016, pp. 77–82.
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Patents

1. **Kazuki Itoh** and Tetsuo Endoh, “スイッチング回路装置及び降圧型DC—DCコンバータ,” 特願 2016-186254, Sept. 23 2016 (出願済).