Mechanical Properties and Reliability of Lead-Fee Solder Joints with Various Surface Finishes

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Mechanical Properties and Reliability of Lead-free Solder Joints with Various Surface Finishes

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Chapter 1

Introduction

1.1 Electronic packaging

Since the invention of the transistor in 1947, electronic packaging technology has had a great influence on modern society. It has grown into a large industry with a market of more than one trillion USD with very rapid growth and development compared to other industries. The development of electronic packaging technology followed Moore's law until the 1990s. Recently, it has reached the physical limit of semiconductor integration processes due to the miniaturization of electronic products, such as smartphones. Thus, current semiconductor package technology needs to satisfy miniaturization, and be multifunctional, highly integrated, low cost, and have excellent electrical properties.

Wire bonding and tape automated bonding (TAB) methods have been adapted for chip bonding in conventional semiconductor and electronic packaging fields. However, these methods have been reported to exhibit reliability problems, such as low chip integration, delay in the transmission of electrical signals, and high heat generation rates. To overcome these problems, the flip-chip bonding method has been studied worldwide to increase the number of I/Os and enable high-speed signal processing

using solder bumps [1-2]. The ball grid array (BGA) package, which is mainly used in the flip-chip bonding method, accounts for a significant portion of the market share [3]. Due to the high importance of the BGA package as an interconnection material, many studies have investigated solder joint properties, interfacial reactions with the metal layer, mechanical deformation behavior of solder joints, thermal-mechanical properties, and thermal fatigue properties of the solder [4].

1.2 Lead-free solder

In the early days of electronic packaging development, 63Sn-37Pb and Pb-Sn-based alloys were extensively used as materials for mechanical, thermal, and electrical connections. However, now Pb and its compounds are subjected to environmental regulations (such as the restriction of hazardous substances (RoHS), waste electrical and electronic equipment (WEEE), and end-of-life vehicles (ELV) directives) due to their toxicity and environmental pollution problems [4]. Hence, an eco-friendly and high performance lead-free solder alloy should be employed to replace the Sn-Pb-based solder. The melting point, wetting properties, and economic feasibility of the solder alloy should be considered for solder joint applications, which are critical for the quality of electronics parts. According to Kang [5] and Glazer [6], the Sn-52In alloy has the advantages of a low melting point and outstanding ductility, while it has the disadvantage of high cost due to the scarcity of In. The Sn-57Bi alloy achieved joint formation at low temperature, but it resulted in low contact. The Sn-3.5Ag alloy

exhibits excellent mechanical and creep properties. However, many studies have been conducted to add a third element, such as Bi, In, Cu, and Zn, to fabricate a three-element alloy in an attempt to lower the melting point and improve wetting properties [7-10].

In addition to the solder alloy, it is important to study the under bump metallization (UBM) method. Cu-based UBM is most commonly employed in conventional Pb-Sn solder bonding technology. However, the Cu is rapidly diffused into the solder, resulting in a highly brittle intermetallic compound (IMC) in the current lead-free solder bonding technology. The interfacial reaction between the solder and UBM has a significant effect on the mechanical properties of electronic packaging and many reports of this phenomenon have been published [11]. In addition, studies regarding methods to replace the Cu-based UBM have been conducted. It has been revealed that Ni-based UBM have relatively low diffusion into the solder and can replace the conventional Cu-based UBM [12]. Currently, much research is being conducted on electroless Ni(P) and interest in this material is growing [13].

1.3 Surface finishes

ENIG, a Ni-based surface finish, has been used extensively in ball grid array (BGA) packaging for the past fifteen years. However, an increase in brittle fractures at the solder joint with an ENIG surface finish has been reported when the Pb-Sn solder was replaced with lead-free solders [14-16]. Such brittle fractures originated from thermal

stresses occurring at the solder joint as a result of the accelerated IMC growth and low creep rate of the lead-free solder with increasing soldering temperature. Much research continues to be devoted to solving this problem. Recently, many studies on PCB surface finishes were performed in order to reduce brittle fractures; the surface finish significantly affects the mechanical and electrical reliability of a solder joint. Mei et al. [17] reported the fracture mechanism in the IMC region of an SAC/ENIG joint. The three proposed mechanisms of failure were (1) weakening of the inner joint due to P segregation, (2) weakening of the joint due to defects from contamination and oxidation during or after plating process, and (3) continuous nanovoid formation at the interface between the Ni(P) and IMC layers. In general, Ni_3P, $Ni_{12}P_5$ + Ni_3P, $Ni_{12}P_5$, Ni_2Pn, Ni_2SnP, and Ni_3Sn were formed as IMCs during interfacial reactions between Ni(P) and Sn [18-19]. Since nanovoids existed in the Ni_2SnP layer located between the Ni_3Sn_4 and Ni_3P layers, it was highly vulnerable to failure via crack propagation through the voids [20-21]. To suppress nanovoid formation and P segregation, ENEPIG surface finishes have been prepared by plating an electroless Pd layer onto an electroless Ni layer, which can reduce Ni diffusion [22-23]. ENEPIG surface finishes, unlike ENIG systems, have a Pd layer between the Ni (P) and Au layers which inhibits Ni from diffusing toward the solder during the soldering process. Thus, the ENEPIG layer deters overgrowth of the IMC and gives it high levels of reliability [24-26]. This type of surface treatment also makes wire bonding possible [27]. Currently, a soft Au process is used for wire bonding, but since the formed Au layer must be thick, it makes

the process costly. Since Au and Al wire bonding and solder bonding can be used simultaneously [28], it is possible to reduce the cost by replacing Au with Al. There are several studies which have highlighted stability problems with the palladium compound, and further research is needed to improve the durability [29-30].

1.4 Mechanical properties

In addition to investigating solder compounds in the electronic packaging field, many studies have evaluated the mechanical properties. Since electronic devices have recently evolved from desktop to hand-held products, the importance of good drop shock properties of portable products, such as smartphones, is increasing [31]. The drop shock characteristics of solder joints in mobile devices are reduced with miniaturization and high integration. Thus, the demand for devices with drop shock resistance is increasing. Brittle fractures are generally observed as the failure mode of solder joints during drop shock [32]. The conventional shear strength test has been performed at velocities below 300 μm/s. Only low strain rates can be used to characterize bulk solder properties at solder joints. Song reported that the high-speed shear test can adequately simulate drop shock [11]. With increasing strain rate, the failure mode transitioned from ductile fracture in the solder to brittle fracture in the IMC region. The shock that occurs when actual electronic devices are dropped is instantaneous. Thus, many studies have been performed in accordance with the increasing interest in high-speed shear strength tests to determine the mechanical

properties of electronic packaging of small mobile electronic devices by applying rapid impacts (unlike conventional test methods) [11, 33].

1.5 Literature review

1.5.1 Electronic packaging

The term “electronic packaging” refers to all hardware in the electronics industry, except for internal chips (ICs). Meanwhile, it means to fill the box and organize the form according to the dictionary. Electronic packaging can also be defined as the final commercialization stage of semiconductor and electronic devices that are packed with plastic resin and ceramics for mounting the microcircuit chip on a substrate. There are four main functions of electronic packaging in the field of semiconductor and electronic devices: (1) The packaging protects the ICs from the external environment. For example, it is difficult to maintain a stable state when even small changes in environmental conditions are present, since the ICs, having the size about 1/1000 the thickness of a human hair, contain a patterned microcircuit. Therefore, the packaging is required to protect the microcircuit. (2) The electronic packaging acts as an electrical connection between the ICs and other components. A direct electrical connection is difficult due to the small chip, which cannot be discriminated by the naked eye. (3) The packaging acts as a heat conductor to cool the internal circuitry during chip operation. Internal heating is directly responsible for the deterioration in

performance and reliability in electronic devices. When the temperature of a chip increases by 10 °C, the lifetime and switching delay were decreased by 50% and 2%, respectively. Hence, optimum performance cannot be achieved and the electronic devices cannot be used for long periods when the internal heat generated by highly integrated large-capacity chips is not effectively released to the external environment. (4) The electric packaging supplies power to operate the chip.

In the past, advanced electronic packaging was not required as its main purpose was to provide an electrical connection and protect the chip from the external environment. Over time, the demand for highly integrated high-performance chips has been increasing. Accordingly, high thermal and electrical performances are also required. Currently, complete systems consisting of the chip, packaging, and device are common and the growing demand is not limited to high performance and miniaturization of the previously mentioned electronic devices. In addition, a low production cost is desired.

To fulfill these requirements, through-hole mountings were replaced by highly integrated surface mountings for semiconductor packages. At the same time, the fine pitch of the internal pin gap was developed based on the demand for small and lightweight pins to enable a higher number of pins with increasing I/O number and facilitate high integration. Electronic packaging can be classified into four levels, as shown in Figure 1.1. The zeroth level packaging refers to the interconnection at the chip level, while the first level packaging is the interconnection forming a single- or multi-chip module [34]. Second level packaging refers to bonding the first level

packaging on a printed circuit board (PCB), and third level packaging is the final stage of bonding to a mother board. As previously mentioned, electronic devices such as smartphones and main frames of computers are examples of electronic packaging.

1.5.2 Lead-free solder alloy

After the first development of lead-free solder, various kinds of solder alloys have been proposed. Most studies have been conducted on binary and ternary metals alloy [35-37] with a few investigating quaternary metals alloy [38]. The lead-free solder alloy material must be environmentally friendly and have a similar melting point to the conventional Pb-Sn solder. In addition, the material should possess outstanding wettability, electrical and thermal conductivity, and have similar mechanical strength and reliability to the conventional Pb-Sn solder. In terms of cost, an inexpensive material is preferred. The requirements for lead-free solder materials in the electronic packaging field are as follows.

1) Melting point: the temperature of reflow should not exceed 255 °C, in order to maintain thermal stability of the components and PCB materials.
2) Process suitability: the selected materials should be easily made into bars, paste, and wire.
3) Toxicity: it should not pose any threats to human health or the environment.
4) Physical, mechanical and electrochemical properties: the material should have

outstanding electrical and thermal conductivity, high wettability on the metal substrate, and excellent mechanical properties (e.g. fatigue properties). In addition, it should have outstanding corrosion and oxidation resistance.

5) Cost: the solder alloy material should be inexpensive, as higher costs in the electronic device and electronic packaging industries will increase the product cost.

Sn-based lead-free solder, which is produced by the addition of small amount of various elements (e.g. In, Bi, Zn, Ag, Sb, and Cu) into Sn, is the most-studied lead-free solder alloy for substituting the existing Pb-Sn solder. The characteristics of the candidate solder alloys mentioned in the literature and the potential candidates for lead-free solder compositions are presented in Table 1.1 and 1.2, respectively [39]. These will be described in detail here.

1.5.2.1. Sn

Sn has outstanding wetting properties and hence has been traditionally used as the main component of most solder materials for electronic components. Sn has a melting point of 231 °C and two different crystal structures in the solid state. The stable diamond structure of α-Sn can be found at temperatures below 13 °C. When the temperature drops below 1 °C, a phase transition known as ‘tin-pest’ occurs, to β-Sn (a body-centered tetragonal structure).

1.5.2.2. Sn-Ag

The eutectic composition of Sn-Ag-based alloys is Sn-3.5Ag. Compared to the conventional Pb-Sn solder, it has a higher melting point of 221 °C. The microstructure of Sn-3.5Ag solder is composed of Sn dendrites and a Ag_3Sn IMC. The tensile strength is higher than that of Pb-Sn eutectic solder and its susceptibility to deformation has been reported to be low [6]. Recently, Sn-3.5Ag has been actively studied as the most promising candidate to substitute Pb-Sn-based alloys. However, it has the disadvantage of lower wettability compared to the Pb-Sn eutectic solder. To overcome this problem, ternary solders are being developed [5].

1.5.2.3. Sn-Cu

The eutectic composition of Sn-Cu-based alloys is Sn-0.7Cu and the melting point is 227 °C, which is slightly higher than the common Pb-Sn solder. There are only few studies related to this alloy to date, most being performed by companies such as Motorola. Although the creep properties are lower compared to the conventional Pb-Sn solder, it has an outstanding fatigue life and low cost [5-6, 40]

1.5.2.4. Sn-Bi

The eutectic composition of Sn-Bi-based alloys is Sn-58Bi. It is a low-temperature

solder alloy with a melting point of 138 °C. The solubility is reduced with decreasing temperature and the Bi forms coarse precipitates during solidification, which has adverse effects on the mechanical properties [5-6].

1.5.2.5. Sn-In

The eutectic composition of Sn-In-based alloys is Sn-52In and it has a very low melting point of 117 °C. It has excellent ductility and wettability, but widespread commercialization is difficult due to the scarcity and high cost of In [5].

1.5.2.6. Sn-Zn

The eutectic composition of Sn-Zn-based alloys is Sn-9Zn and it has a melting point of 198 °C, which is similar to the common Pb-Sn eutectic solder. It has disadvantages of low wettability [41] and high reactivity (easy oxidization of Zn). To improve the wettability and mechanical properties, many studies are being conducted to add third, fourth, and fifth elements [42-43].

1.5.2.7. Sn-Ag-Cu

The melting point of the Sn-3.5Ag alloy can be lowered, while the wettability and mechanical strength can be improved, by the addition of Cu. Thus, this alloy has become one of the most commonly used solders. In the case of the Sn-3.5Ag-0.7Cu

solder, the melting point (217 °C) is lower than Sn-3.5Ag. Moreover, the mechanical properties, such as tensile strength, thermal fatigue and creep, are superior to the Pb-Sn eutectic solder [10]. It has also been shown that the formation of the Ag_3Sn IMC within the solder can be inhibited by optimizing the amount of added Ag [44].

1.5.2.8. Sn-Ag-Bi

The addition of Bi into the Sn-3.5Ag alloy has the advantage of lowering the melting point and improving the wettability and mechanical properties [10]. In particular, Bi concentrations less than 2% can significantly improve the strength through solid-solution strengthening. When the Bi concentration was increased, fine precipitates of Bi, which was not incorporated into Sn, were formed within the solder alloy during cooling, resulting in higher brittleness and lower ductility.

1.5.2.9. Sn-Ag-Zn

In the case of the Sn-3.5Ag alloy, a Ag_3Sn IMC was formed within the solder. When stress was focused on the IMC, the mechanical properties deteriorated due to crack generation between the solder matrices. In order to prevent this phenomenon, many studies are being performed where Zn is added into the Sn-Ag-based solder. The most promising composition among the Sn-Ag-Zn-based alloys is Sn-3.5Ag-1.0Zn, with a melting point of about 217 °C. Zn can be used to improve the strength and creep resistance of the Sn-3.5Ag solder alloy with a low mutual solubility; it has good

solubility in Ag and negligible solubility in Sn. However, its application for soldering is limited due its low corrosion resistance and wettability, since Zn is readily oxidized in an ambient atmosphere. Recently, soldering using this material has been performed under a nitrogen gas atmosphere and flux manufacturing technology was developed to overcome the Zn oxidation problem. Thus, the applicability of this material has increased. It has also been reported that the addition of Zn into Sn-3.5Ag can result in excellent mechanical properties by suppressing dendrite formation and refining Ag_3Sn [8].

1.5.3 Surface finish types

Surface finishing can be defined as the surface processing (before the router process or after shipment inspection in the PCM manufacturing) to achieve specific objectives. Surface finishing is carried out for preventing oxidation of the Cu pad in the insert mount technology (IMT) and surface mount technology (SMT) processes and improving the mounting of components. In addition, it enhances the solderability by removing the heat and flux in the soldering process. Surface finish technologies that are currently employed in the electronic component industries can be classified as either hot air solder leveling (HASL), organic solderability preservative (OSP), electroless Ni immersion Au (ENIG), electroless Ni electroless Pd immersion Au (ENEPIG), electroless Ni auto-catalytic Au (ENAG), immersion Sn, or immersion Ag. A comparison of the characteristics and cost according to the type of surface finish is

shown in Table 1.3, and these technologies will be discussed in more detail in the following sections.

1.5.3.1. Hot air solder leveling (HASL)

HASL is one of the common surface finish methods for the process using Pb-Sn-based alloys. After melting, the alloy is buried in the substrate which is moved using a conveyor belt under a stream of hot air to produce a solder layer with uniform thickness. However, it is difficult to control the thickness of Sn-Ag-Cu-based alloy using hot air since its melting point is higher than the Pb-Sn-based alloy. When using hot air, the thickness of the surface finish film deposited on the Cu pad of a PCB is not uniform, preventing mounting of the components with defects in the SMT process. Moreover, the problem of solder bridging occurs with narrow pad spacings due to the high circuit density of substrates with fine pitch patterns [45-47].

1.5.3.2. Organic solderability preservative (OSP)

OSP surface finishing has been widely used to replace the HASL technique. In this method, an organic compound (such as alkyl imidazole) is selectively deposited with a thickness of 0.2–0.5 μm on the Cu pad to prevent oxidation. Since the organic compound is similar to flux, it also can be referred to as a pre-flux finish. This surface finish method is highly suitable for fine pitch patterns since the film is selectively formed on the Cu pad. As the use of mobile devices, such as smart phones, personal

digital assistants (PDA), and portable multi-media players (PMP) increases, superior impact resistance is required. The OSP method has been widely used owing to its low cost and relatively low waste generation during surface finishing with the plating method, which is an advantage in terms of environmental impacts.

When a scratch was generated on a Cu pad with organic compound deposited onto it from careless handling of the products, the exposed Cu easily oxidized in ambient air. This results in reliability problems for long term storage [45-47]. Moreover, it is highly vulnerable to multiple heat treatments when mounting different types of packages.

1.5.3.3. Electroless Ni immersion Au (ENIG) and electroless Ni electroless Pd immersion Au (ENEPIG)

ENIG surface finishing is generally carried out by plating an electroless Ni(P) layer with a thickness of 3–6 μm on a Cu pad. Subsequently, a thin Au layer with a thickness of 50–100 nm was plated on top of the nickel layer. This method overcomes some of the disadvantages of HASL and OSP methods and has outstanding handleability, storability, and solderability. It accounts for about 15% of the current surface finish market and the market share is still gradually increasing. The plated Ni(P) layer is used to prevent the rapid diffusion into Cu layer during Au substitution plating. In addition, it helps to prevent reliability problems due to IMC overgrowth since it suppresses the diffusion reaction between Cu and Sn. Brittle fractures were

observed at the interface of the solder and Ni/Au layer originating from the black pad defect phenomenon due to galvanic corrosion of Ni in the P-rich layer formed between the IMC and the Ni(P) layer during soldering [16-19]. According to Jang [19], an increase in P concentration can be observed when the amount of impurities in the Ni(P) plating solution increases due to partial segregation of P atoms. Accordingly, this affects the solderability by promoting the oxidation of Au and Ni atoms during Au substitution plating. A recent international standard recommended a minimum plating thickness of 3 μm and P concentration of 8–10% for the electroless plated Ni(P) layer.

In an attempt to resolve the black pad problem, the ENEPIG surface finish method is being actively studied to replace ENIG. The ENEPIG method involves plating a Au layer with a thickness of 50–100 nm over an electroless Pd layer of 50–100 nm plated on a 3–6 μm electroless Ni(P). This method has the advantage of wide applicability as both Au and Al wire bonding and soldering can be performed. However, due to stability problems with Pd compounds, many studies are being focused on improving the reliability and up-scaling this technique [22-23].

1.5.3.4. Electroless Ni auto-catalytic Au (ENAG)

The ENAG surface finish method is carried out by plating a 0.1–0.3 μm Au layer on top of an ENIG Au layer using an auto-catalytic method. The Au layer of ENAG is a suitable surface finish for wire bonding. As a cyanide-free process, it can improve the corrosion resistance by inhibiting void formation. However, there exist only few

studies reporting the effect of Ni(P) plating, P concentration, and Au thickness on the reliability of the xxxx.

1.5.3.5. Immersion Sn and Ag

The immersion Sn surface finish method can generate a film with uniform surface roughness. It is suitable for high-density circuit applications since Sn, with good wettability, is used. However, typical problems, such as Sn plating and the formation of whiskers, cannot be prevented, resulting in a cavity or temporary short circuit. Several limitations of this method have been reported in previous studies, related to the components falling out of the PCB after the SMT process and soldering not being possible due to very poor wetting behavior after multiple heat treatments. If the surface is touched due to careless handling, oxidation occurs rapidly due to salt from the hands and scratches can be easily formed due to the low strength of Sn [45-47]. Moreover, it has limited practical application due to the high cost of Ag.

1.5.4 Chemistry of ENIG and ENEPIG surface finishes

Methods to form a metal film on a substrate by reducing metal ions from a metal salt solution can be categorized as electroplating, where metal ions are deposited by means of an external power supply, or electroless plating, which does not require an external power supply. Depending on the mechanism through which metal ions

acquire electrons, electroless plating can be subcategorized into immersion plating (galvanic displacement), in which electrons are acquired by substitution reactions, and autocatalytic plating (commonly called electroless plating because it is a representative electroless plating method), in which electrons are acquired from a reducing agent.

Electroless plating has the following advantages: it enables plating on a non-conductive surface, it does not require an external power supply, the target surface can be plated with a uniform thickness regardless of the current distribution, it lends itself well to mass production, and it has excellent adhesion and wear resistance. The main drawbacks are a high production cost, because the source of metal ions is chemical precursors, and the short service life of the plating solution due to contamination by the reaction byproducts [48-49]. Electroless nickel plating (EN) was introduced by Brenner and Riddell in 1946. While a range of reducing agents, such as sodium hypophosphite ($NaH_2PO_2 \cdot H_2O$), sodium boron ($NaBH_4$), and boronized dimethylamine (DMAB), can be used for EN, sodium hypophosphite is the most commonly used due to its low cost and convenient handling [50-51]. Characteristics of the two aforementioned methods of electroless plating are as follows.

1) Immersion plating

If two metals with different ionization tendencies are in contact, the metal with higher ionization tendency emits electrons, thereby being oxidized into metal ions, while ions of the metal with lower ionization tendency gain electrons and are reduced

into metal [48]. The larger the difference in standard reduction potential values between the two materials, the greater the plating rate. Immersion plating is based on this mechanism of electron transfer between metals triggered by different ionization tendencies. Since an immersion plating bath does not need any extra reducing agent, its main components are metal ions, acid, complexing agent, antioxidant, and pH adjusting agent. As the thickness of the plating film increases, the plating rate decreases towards zero. Table 1.4 shows the ionization tendencies of some metals commonly used in immersion plating.

2) Electroless plating

In the electroless plating technique, the plating metal is deposited onto the target surface catalyzed by reducing metal ions, i.e. transferring electrons, in a plating solution using a reducing agent. The mechanism of electroless plating can be divided into an oxidization stage, in which the reducing agent loses electrons to the plating solution and becomes oxidized, and the deposition stage in which metal ions receive electrons and are deposited onto the target surface forming a metal film [48].

reducing agent $\rightarrow$ oxide (of the reducing agent) + xe^- (electron)

M^{x+} (metal ion) + xe^- (electron) $\rightarrow$ M (metal film)

The above two equations are combined as follows:

M^{x+} (metal ion) + reducing agent $\rightarrow$ M (metal film) + oxide (of the reducing agent)

An electroless plating solution is composed of metal ions, reducing agent, pH adjusting agent, and catalytic poison (to prevent the plating tank and pump from being plated) [49].

3) Chemical reactions involved in electroless Ni(P) plating

The equations below show the chemical reactions taking place during the ENIG and ENEPIG surface finish methods using sodium hypophosphite as the reducing agent.

Main reactions:

$$Ni^{2+} + H_2PO_2^- + H_2O \rightarrow Ni + H_2PO_3^- + 2H^+ \quad (1)$$

$$H_2PO_2^- + H_2O \rightarrow H_2PO_3^- + H_2 \quad (2)$$

2^{nd}-order reactions:

$$2H^+ + 2e^- \rightarrow H_2 \quad (3)$$

$$H_2PO_2^- + H \rightarrow P + OH^- + H_2O \quad (4)$$

Equations (1)–(4) represent Ni reduction, sodium hypophosphite consumption, hydrogen generation, and P generation, respectively. The potential and pH at which electroless plating occurs can be predicted by examining the reduction potential of Ni and sodium hypophosphite given in Equation (1) using the Pourbaix diagram [52]. The pH and potential ranges where Ni and $H_2PO_3^-$ ions are in a stable state are pH 2–7 and -0.3–-0.8 vs. SHE, respectively, as can be determined from Equation (1), whereby the utilization efficiency of sodium hypophosphite is lower than 50% (not all of the $H_2PO_3^-$ ions are consumed for reducing Ni). Table 1.5 summarizes the advantages and disadvantages of the ENIG surface finish method [50].

4) Chemical reactions involved in electroless Pd plating

In the ENEPIG surface finish method, the plating solution in contact with the Ni(P) layer is an autocatalytic electroless Pd plating solution based on an ethylenediamine-Pd complex using salts of formate, phosphite, or hypophosphite and a reducing agent. Table 1.6 shows an example of a standard composition of electroless Pd plating solution, and Figure 1.2 compares the thickness of the plating film of each surface finish method.

a) Electroless Pd plating using formate as reducing agent

Figure 1.3(a) shows a potential–pH diagram for an electroless plating solution of ethylenediamine with formic acid (HCOOH) as reducing agent. It

can be seen that Pd ions are in a stable state, bound with ethylenediamine, in the range of pH 5.5–12. This suggests that it is thermodynamically possible to implement electroless Pd plating using formic acid as the reducing agent. Factors influencing the deposition rate are Pd concentration and the temperature of the plating solution. In this plating solution, carbonate is generated as a result of a side reaction which depends on the progress of the plating reaction. However, even when hydrogen carbonate ions are accumulated, the deposition rate is rarely affected. Consequently, a film with uniform surface finish and high density is formed and the plating solution exhibits excellent stability. The equations below show the chemical reactions involved in Pd plating using formate as the reducing agent.

$$RCOOH + H_2O \rightarrow CO_2 + ROH + 2H^+ + 2e^- \quad (5)$$

$$Pd^{2+} + 2e^- \rightarrow Pd \quad (6)$$

b) Electroless Pd plating using phosphite as reducing agent

In the electroless Pd-P plating solution using phosphite as the reducing agent, the P content is lower than that in the solution using hypophosphite as the reducing agent. The P content is positively correlated with the deposition rate. A decrease in the deposition rate with increasing hypophosphite

concentration results in both a decrease in adsorption of Na_2PO_3 on the precipitate and in the activity of the precipitate, due to an increase in P content.

Figure 1.3 (b) shows the potential-pH diagram of hypophosphite along with hypophosphite. The equations below show the chemical reactions involved in the Pd plating using phosphite as the reducing agent.

$$H_3PO_3 + H_2O \rightarrow H_3PO_4 + 2H^+ + 2e^- \quad (7)$$

$$H_3PO_2 + 3H^+ + 3e^- \rightarrow P + 3H_2O \quad (8)$$

$$Pd^{2+} + 2e^- \rightarrow Pd \quad (9)$$

c) Electroless Pd-P plating using hypophosphite as reducing agent

Figure 1.3 (b) shows the potential–pH diagram showing the electroless Pd plating solution of ethylenediamine using hypophosphite as reducing agent. It can be seen that Pd ions exist as compounds with ethylenediamine in the range of pH 5.5–12. Hence, electroless Pd plating is thermodynamically possible using hypophosphite and phosphite as reducing agents. While the deposition rate increases with increasing Pd concentration, the P content decreases. In contrast, while the deposition rate is not significantly influenced by pH, the P content decreases as pH increases. In addition, the pH affects the surface quality of the plated film; uniform films are formed under

normal conditions and cracks are likely to occur under low concentrations of reducing agent or high pH conditions. The equations below show the chemical reactions involved in Pd plating using hypophosphite as the reducing agent.

$$H_3PO_2 + H_2O \rightarrow H_3PO_3 + 2H^+ + 2e^- \quad (10)$$

$$H_3PO_2 + H^+ + e^- \rightarrow P + 2H_2O \quad (11)$$

$$Pd_2^+ + 2e^- \rightarrow Pd \quad (12)$$

In the above redox reactions, the standard potential of the reducing agent (formic acid) is -0.20 V, the reduction potential of phosphite is -0.28 V, and the potential of the hypophosphite-type reducing agent is -0.50 V. Hypophosphite has the highest reactivity because it has the lowest potential. In addition to the reduction reaction, P is generated when phosphite or hypophosphite is used as the reducing agent, and a Pd–P alloy layer is formed during Pd plating as a result of the eutectoid reaction. When a carboxylic acid (e.g. formic acid) is used, a pure Pd plating layer is formed.

d) Chemistry of immersion Au plating

The equation below shows the chemical reaction involved in immersion Au plating.

$$2Au^{+} + 2e^{-} \rightarrow 2Au0 \quad (13)$$

1.5.5 Interfacial reactions

An IMC is generally formed between UBM and Sn-based solder by the interdiffusion of Sn and UBM atoms. The UBM is classified as Cu- or Ni-based. When the UBM reacts with the solder in reflow, Sn-Cu and Sn-Ni IMCs are generated. The Sn-Ni binary phase diagram is presented in Figure 1.4 and the Sn-Cu binary phase diagram is presented in Figure 1.5. The characteristics of each IMC are shown in Table 1.7.

1.5.5.1. Sn-Ni-based reaction

The IMCs formed by the interfacial reaction between Sn and Ni are Ni_3Sn, Ni_3Sn_2, and Ni_3Sn_4, and these are discussed in detail in the following text.

1) Ni_3Sn: As shown in Figure 1.4, this IMC is divided into high-temperature Ni_3Sn and low-temperature Ni_3Sn. The low-temperature Ni_3Sn exists at room temperature and has a regular Mg_3Cd(D019)-type hexagonal close packed (hcp) structure with lattice constants a = 0.4286 Å and c = 0.4242 Å. The high-temperature Ni_3Sn occurs above 920.5 °C and has an Fe_3Al(D03) type cubic structure.
2) Ni_3Sn_2: This IMC has a NiAs-type hexagonal structure at room temperature with

lattice constants a = 0.4081 Å and c = 0.5174 Å. At high temperature, the presence of either hexagonal or orthorhombic structures has been reported in the literature.

3) Ni_3Sn_4: This compound has a CoSn(B35)-type monoclinic structure consisting of 14 atoms per unit cell. The lattice constants are a = 1.2222 Å, b = 0.4064 Å, c = 0.5225 Å, and $\beta = 103.48^{\circ}$.

Following Ni_3Sn_4 formation by reaction between Sn and Ni, Ni_3Sn_2 is formed from the reaction between Ni_3Sn_4 and Ni. Finally, Ni_3Sn is formed by the reaction between Ni_3Sn_2 and Ni. However, the Ni_3Sn_4 IMC is mostly found as the result of an interfacial reaction between Sn-based solder and Ni UBM. According to Haimovich [53], this phenomenon is related to the higher driving force for Ni_3Sn_2 and Ni3Sn formation compared to Ni_3Sn_4 at 250 °C. However, Ni_3Sn_4 is generally formed and grown at the interface between Ni and Sn-3.5Ag solder due to the significant effect of the interfacial energy with the matrix generated during nucleation growth and the thermodynamic driving force during formation of Ni-Sn intermediates. The activation energy barrier for nucleation growth is proportional to (3 × interfacial energy)/(2 × driving force).

1.5.5.2. Sn-Cu-based reaction

The IMCs formed through interfacial reactions between Sn and Cu are Cu_6Sn_5 and Cu_3Sn, which are discussed in detail here.

1) Cu_6Sn_5 (η-phase): As can be seen in Figure 1.5, the η'-phase is the η-phase at room temperature. At temperatures above 186 °C, this compound has a simple superlattice of NiAs(B81)-type hexagonal symmetry with a = 4.2 Å and c = 5.09 Å, consisting of 20% copper and 80% vacancies. In addition, a long period superlattice η'-phase having a five times larger lattice constant is formed at temperatures below 186 °C. The melting point of the η-phase is 676 °C and metal bonding is mainly formed between Cu and Sn.
2) Cu_3Sn (ε-phase): The high temperature phase has a structure with Cu0Ti-type orthorhombic symmetry with lattice constants of a = 2.755 Å and b = 4.722 Å. The melting point is 415 °C and the rules for a long period superlattice are as = 2a, bs = 8b, and cs = c.

Cu_6Sn_5 is likely to grow inwards towards the solder rather than towards the UBM Cu. Tu [54] showed that the rearrangement for Cu_6Sn_5 growth took place at the Cu_6Sn_5/Sn interface and the IMC growth occurred within the solder due to interstitial diffusion of Cu inside Sn and the higher diffusion of Cu compared to Sn in Cu_6Sn_5. Cu_3Sn was not observed due to difficult nucleation during room temperature aging, while Cu_6Sn_5 was observed. When the two layer specimen was aged for a long period

at 150 °C (after Sn was completely consumed at room temperature), the Cu_3Sn infiltrated the layer Cu_6Sn_5 at the interface of the two layers and grew with a parabolic dependence on time. The growth of Cu_3Sn is a diffusion-controlled reaction.

1.5.5.3. Sn-Ag-Cu/Ni-based reactions

The IMC formed between Sn-Ni is usually Ni_3Sn_4. However, Hwang, et al. [55] reported a very thin (around 50 nm) Ni_3Sn_2 IMC below a Ni_3Sn_4 layer resulting from the interfacial reaction between electrolytic Ni and Sn-3Ag-6Bi. Kao and Duh [12] observed the effect of Cu addition on the interfacial reaction between electrolytic Ni UBM by fixing the Ag amount at 3.9 wt%. When 0.2 wt% Cu was added, only $(Ni_{1-x}Cu_x)_3Sn_4$ IMC was observed. Two types of IMC, $(Ni_{1-x}Cu_x)_3Sn_4$ and $(Cu_{1-y}Ni_y)_6Sn_5$, could be obtained by the addition of 0.4 wt% Cu and $(Cu_{1-y}Ni_y)_6Sn_5$ was observed with the addition of more than 0.6 wt% Cu. In the case of electroless Ni(P)/Au UBM, a $(Ni_{1-x}Cu_x)_3Sn_4$ IMC was formed when the Cu within the solder was less than 0.5 wt%. Two types of IMC, $(Ni_{1-x}Cu_x)_3Sn_4$ and $(Cu_{1-y}Ni_y)_6Sn_5$, were found for 0.5 wt% Cu addition and the $(Cu_{1-y}Ni_y)_6Sn_5$ IMC was observed for more than 0.5 wt% Cu. Sohn et al. [56] investigated the dependence of the morphology of the IMC layer and spalling phenomena on the solder deposition method, P concentration in Ni(P), and solder thickness. A higher P concentration enhanced spalling due to increased solder volume. Needle-shaped IMC morphologies exhibited higher spalling compared to chunk-shaped ones due to the increasing number of channels for Sn penetration in needle-

shaped structures. The Sn that penetrated into the IMC reacted with Ni_3P, resulting in a Ni_3SnP layer. On the other hand, Ni_3Sn_4 delaminated from the Ni_3SnP surface.

1.5.5.4. Sn-Ag-Cu/Cu-based reaction

For Sn-Ag and Sn-Ag-Cu solder, the IMCs formed by the interfacial reaction with the Cu UBM are Cu_6Sn_5 and Cu3Sn. Only Cu_6Sn_5 was observed at room temperature, while Cu_3Sn was generated in the Cu UBM and Cu_6Sn_5 was formed within the solder during high-temperature aging. In addition, voids were generated in the Cu_3Sn intermetallic compound when the reaction temperature was high. As the volume of the solder became larger, the consumption of Cu increased and the thickness of the IMC reduced [57].

1.5.6 Black pad formation during ENIG surface finishing

With increasing demand for ENIG as a PCB surface finish, related problems have increasingly been reported (accompanied by extensive research activities to address such limitations). Among the problems reported thus far, the most serious one is the black pad phenomenon occurring in the Ni(P) layer, which results in brittle fractures and is the major factor lowering package reliability [31-32, 58-60]. The name “black pad” comes from the black color observed on the Ni(P) layer [31]. This phenomenon has been investigated for about a decade by a consortium in the PCB industry in an

attempt to eliminate the problem by identifying the mechanism and root causes. Kim [32] demonstrated that the black pad phenomenon is ascribable to enhanced corrosion occurring during the immersion Au process. The difference in potential between Au^+ ions on the Ni(P) layer leads to the formation of Ni_2^+ ions. Excessive generation of Ni_2^+ ions while bonding to Au^+ ions results in corrosion. Excessive consumption of Ni ions while bonding can also induce corrosion. Furthermore, excessive consumption of Ni ions on the Ni(P) layer causes the P content to increase accordingly. In the subsequent soldering process, the elevated P content deteriorates wettability and adhesion.

1.5.6.1. Black pad mechanism

Currently known causes of the black pad defects can be summarized as follows:

1) According to Biunno [31], the rate of Au grain growth is relatively slow at a nodule boundary or junction. Since the concentration of Au ions is not homogeneous in a nodule boundary, crevices are formed along the boundaries or at junctions. Therefore, the Au layer grows non-uniformly, and micro-galvanic cells are formed between the Ni(P) and Au layers, making the boundaries prone to corrosion. Figure 1.6(a) shows a schematic of black pad formation and Figure 1.6(b) shows how black pads can be formed by applying a 1 V potential. Furthermore, excessive consumption of the Ni ions from the Ni(P) layer in the immersion Au process results in increasing the P content in the consumed region.

From these results, it was concluded that the current flowing through the PCB increases the corrosion activity at the Ni(P) layer, thus accelerating oxidation.

2) Kim et al. [32] noted that corrosion starts at a nodule boundary as it is the place where substitution of Ni atoms for Au atoms occurs more intensely; the corrosion then expands towards the interior of the nodule. Accordingly, major and minor spikes are found at the nodule boundaries and interiors, respectively. In the immersion Au plating process, it was also observed that concentration cells are formed when the plating solution circulates, and corrosion occurs in the pad spikes. The smaller the pad area, the larger the region where the plating solution cannot circulate, resulting in a growth of the black pad. Figure 1.7 is a schematic of the size-effect induced concentration cell formation.

3) Osenbach et al. [58] stated that low-density interfaces are formed during the Ni(P) growth due to secondary-phase precipitation, and corrosion occurs during the immersion Au process, resulting in mud cracks appearing on the Ni(P) surface. Figure 1.8 shows a schematic of the corrosion caused by secondary-phase precipitation.

4) Won et al. [59] reported that an uneven Au layer is formed due to the adsorption of excess citrate ions along the nodule boundary, resulting in black spots. It was

also noted that this tendency increased as the pH of the Au plating solution decreased. Figure 1.9 depicts the phenomenon of an uneven Au layer leading to black pad formation.

5) Kim et al. [60] reported that nodules on a Ni(P) layer having different P contents induced the formation of micro-galvanic cells, whereby a nodule with lower P content undergoes corrosion during the immersion Au process. Figure 1.10 depicts this process of micro-galvanic corrosion.

1.5.6.2. Factors influencing black pad formation

The following outlines the causative factors for black pad formation [32, 60-61]. Variables such as the amount of Ni(P) plating solution used, P concentration, oxidation of Ni (P) layer, organic impurities, and galvanic reaction, are known to be associated with black pad formation.

1) The use of larger amounts of Ni(P) plating solution are related with a higher likelihood for black pad formation. Since Ni ions are consumed in a Ni(P) plating solution through the reduction reaction, these Ni ions should be replaced in the solution to enable continuous use. This Ni ion supplementation is called metal turn over (MTO). As the MTO increases, phosphite is generated as a reaction byproduct, which reduces the deposition rate of Ni plating. Moreover, as the number of plating cycles increases, the P content increases and organic

impurities are generated in the photo solder resist (PSR), both of which induce oxidation of the Ni surface and result in black pad formation on the Ni surface during the immersion Au process.

2) The P concentration of a Ni(P) plating solution is categorized into high-range (≥ 10 wt.%), mid-range (6–9 wt.%), and low-range (≤ 5 wt.%) concentrations. The P content in a Ni(P) plating solution was found to change depending on the pH and types of additives and complexing agents. As a general rule, the higher the P concentration, the higher the likelihood for oxidation. Figure 1.11 shows the changes in the surface structure of a Ni(P) layer depending on P concentration.

3) The black pad phenomenon related to the oxidation of the Ni(P) surface occurs due to exposure to air before undergoing the immersion Au process. Hence, it has been suggested that the time between Ni(P) and immersion Au processes should be reduced as much as possible and that contamination should be avoided by supplying sufficient pure water during the water cleaning process. Figure 1.12 shows the surface defects induced by Ni(P) oxidation.

4) The organic impurity-induced contamination of the Ni(P) layer is the root cause of the black pad phenomenon. Most of the impurities in a Ni(P) plating solution

come from the PSR ink on the surfaces of the dry film and PCB used in the process. The amount of organic impurities increases in proportion to the amount of plating solution used. As the amount of organic impurities increases, the plated surface shows an increasingly needle-like structure, which affects the anti-corrosion property of the crystalline Ni(P) coating. As a result, the substitution reaction in the immersion Au process accelerates, resulting in spalling phenomenon that reduces adhesion. Figure 1.13 shows corrosion of the Ni layer due to organic impurities eluted from the PSR.

The Cu pad surface of a PCB is greatly influenced by the pre-treatment for the ENIG surface finish. In particular, organic impurities from the chemical pre-treatment remain on the Cu surface. When Pd is added as a catalyst in the subsequent process, the Ni(P) plating density is lowered, resulting in black pads and spalling during the immersion Au process. Figure 1.14 depicts the changes in the Cu surface morphology caused by the adsorption of organic impurities.

5) The black pad effect occurs from galvanic corrosion (as a result of the difference in potential between two metals in electrical contact when exposed to a corrosive solution). Here, galvanic corrosion occurs due to the difference in potential arising from different sized PCB pads during the immersion Au process, where the smaller pad is more prone to corrosion.

1.6 Thesis structure

This thesis consists of five chapters, which will be outlined here.

In Chapter 1, the role and structure of electronic packaging are explained and the different surface finishes described. Current development priorities in the field, such as lead-free solder, are also discussed. Also included are the chemical reactions involved during the surface finishing methods relevant to this study, as well as interfacial reactions. Finally, an overview of the issues of current interest is provided.

In Chapter 2, the solder strength and brittle failure characteristics of Sn-3.0Ag-0.5Cu (SAC305) solder and Ni-based surface finishes (ENIG and ENEPIG) are evaluated. The dependence of the mechanical properties on the number of MTOs of a Ni(P) plating solution is evaluated by means of high-speed shear strength (HSS) tests, drop tests, and analysis of the brittle failure, as categorized into five ranges. In particular, the reason for the sudden decrease in mechanical reliability after three MTO cycles for ENIG surface finishes is elucidated.

In Chapter 3, a novel plasma-type surface finish is evaluated as a solution for the deterioration of the mechanical properties resulting from multiple heat treatments, which is often identified as a weakness of the Cu-based surface finish. It is shown that the performance of the proposed plasma surface finish was maintained up to five heat treatment cycles by measuring wettability and spreadability. Furthermore, the superiority of the plasma surface finish is demonstrated by comparing its performance

with that of the state-of-the-art OSP surface finish.

In Chapter 4, the processability of the plasma surface finish is evaluated after coating a metal mask for SMT processing as a possible application. The enhanced post-coating characteristics are demonstrated by means of bridge and printability testing, and the related mechanisms are discussed. Furthermore, a method of detecting the presence of a coating film, which is not detectable by visual inspection or optical observation, is presented so that coating layers can be conveniently analyzed without requiring extra equipment in industrial settings.

Finally, Chapter 5 provides an overall summary and the conclusions of this dissertation.

1.7 Figures

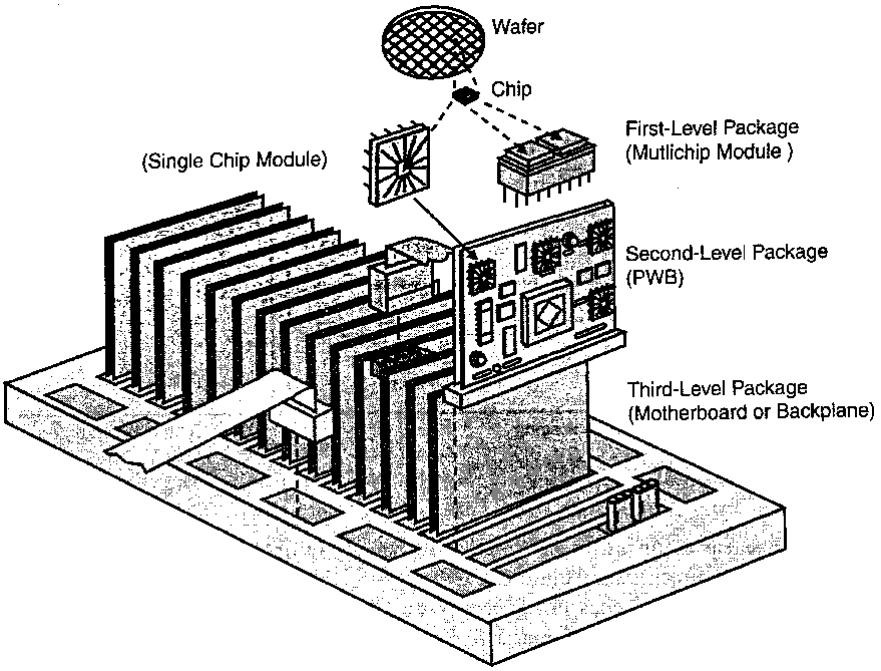


Figure 1.1 The hierarchy of electronic packaging. Reproduced from Tummala, 2001 [34].

Table 1.1 Mechanical properties of selected binary alloys [6].

	Sn-Bi	Sn-In	Sn-Ag
Elongation	Strain rate sensitive		Acceptable ductility at high strain rate
Creep resistance	Exceed Sn-Pb (20-65oC)	Inferior to Pb-Sn in most respects	Extremely creep resistant
Isothermal fatigue	Extremely good at low strain		Excellent at large strain amplitude
Thermal fatigue	Perform better at low cycle		Perform extremely well

Table 1.2 Comparison of thermal properties of lead-free solder alloys [39].

Solder (weight per cent)	Melting temperature, T_M (°C)	Solidus temperature, T_S (°C)	Liquidus temperature, T_L(°C)
60Sn-40Pb	183	183	187
Sn-3.5Ag (SA)	223	221	221
Sn-3.8Ag-0.7Cu (SAC)	217	217	217
Sn-3.9Ag-0.1Cu (SAC)	220.40	217.31	222.71
Sn-3.0Ag-0.5Cu	217.64	217.64	217.64
Sn.3.5Ag-0.5Cu (SAC)	221.58	–	216.92
Sn-3.8Ag-0.7Cu (SAC)	217.73	–	–
Sn-1.1Ag-0.45Cu-0.25Mn	–	217.39	227.63
Sn-1.07Ag-0.58Cu-0.037Ce	–	217.65	226.14
Sn-3.8Ag-0.7Cu-0.5Zn	216.23	212.06	–
Sn-3.8Ag-0.7Cu-1Zn	216.65	212.61	-
Sn-3.8Ag-0.7Cu-1.5Zn	216.86	213.32	–
Sn-3.0Ag-0.5Cu-0.25Al_2O_3	222.3	–	–
Sn-3.0Ag-0.5Cu-0.5Al_2O_3	222.7	–	–
Sn-3.0Ag-0.5Cu-1Al_2O_3	223.0	–	–
Sn-3.8Ag-0.7Cu-2Bi	213.08	–	–
Sn-3.8Ag-0.7Cu-4Bi	206.48	–	–
Sn-3.0Ag-0.5Cu 0.25Ti	220.95	–	216.73
Sn-3.0Ag-0.5Cu-0.5Ti	220.86	–	216.75
Sn-3.0Ag-0.5Cu-1Ti	219.47	–	216.59
Sn-3.5Ag-0.7Cu-0.5TiO_2	224.1	217.7	–
Sn-3.0Ag-0.5Cu-0.5ZrO_2	–	217.08	221.63
Sn-3.0Ag-0.5Cu-1ZrO_2	–	217.12	221.65
Sn-3.0Ag-0.5Cu-3ZrO_2	–	217.25	221.95
Sn-3.0Ag-0.5Cu-0.5$SrTiO_3$	217.7	–	–

Table 1.3 Properties of different PCB surface finishes.

	Types of surface finish				
	ENIG	ENEPIG	OSP	Immersion Ag	Immersion Sn
Reflow	○	○	△	○	△
Wire bonding	○	○	X	△	X
Flip chip bonding	○	○	X	△	X
Joint strength	△	○	○	○	X
Lead-free type	○	○	○	○	○
Cost	X	X	○	X	△

○: good, △: normal, X: bad

Table 1.4 Ionization trend and standard reduction potential of reactions commonly observed in plating.

Ionization trend	Reaction	Reduction potential (V)
High ionization 	$K^+ + e^- \Leftrightarrow K(s)$	-2.93
	$Ca^{2+} + 2e^- \Leftrightarrow Ca(s)$	-2.868
	$Mn^{2+} + 2e^- \Leftrightarrow Mn(s)$	-1.185
	$Zn^{2+} + 2e^- \Leftrightarrow Zn(s)$	-0.762
	$Cu_2S + 2e^- \Leftrightarrow 2Cu(s) + S^{2-}$	-0.560
	$Ni^{2+} + 2e^- \Leftrightarrow Ni(s)$	-0.250
	$Sn^{2+} + 2e^- \Leftrightarrow Sn(s)$	-0.136
Reference	$2H^+ + 2e^- \Leftrightarrow H_2(g)$	0.000
	$AgBr(s) + e^- \Leftrightarrow Ag(s) + Br^-$	+0.071
	$N_2H_4(aq) + 4H_2O + 2e^- \Leftrightarrow 2NH_4^+ + 4OH^-$	+0.110
	$Cu^+ + e^- \Leftrightarrow Cu(s)$	+0.522
	$Ag^+ + e^- \Leftrightarrow Ag(s)$	+0.800
	$Pd^{2+} + 2e^- \Leftrightarrow Pd(s)$	+0.915
Low ionization	$Pt^{2+} + 2e^- \Leftrightarrow Pt(s)$	+1.188
	$Au^+ + e^- \Leftrightarrow Au(s)$	+1.830

Table 1.5 Typical characteristics of the ENIG surface finish method [50].

Advantage	Disadvantage
Coated film	
- Uniformed thickness - High hardness - Good corrosion resistance - Good wear resistance - Low ductility	- Slow deposition rate than electroplating - Brittle deposit
Process	
- No electrical connection - No power supplies needed - Coating on non-conducting substrate	- High temperature process (90 °C) - Short bath life - Careful analytical control of bath is required

Table 1.6 Composition of electroless Pd solutions.

	Chemicals	Role of chemicals
Metallic salt	Pd	Supply for deposited metal
Reducing agent	Formic acid Hypophosphorous acid Phosphorous acid Etc.	Reducing metal that the metal ions by injection electrons
Complexing agent	Ethylenediamine Citric acid Potassium Potassium stannate EDTA Etc.	Complex with metal ions and remains ionic state stable in plating solution.
Stabilizer	Amine Sulfur Heavy metal Etc.	Acts to suppress the reduction reaction of other than the surface to be plated / Prevents: generated hydrogen gas from reaction the precipitate and reducing agent be caused by aging plating solution.
pH adjusters	Sodium hydroxide Sulfuric acid Etc.	Adjust plating speed, reduction efficiency, stability and etc.

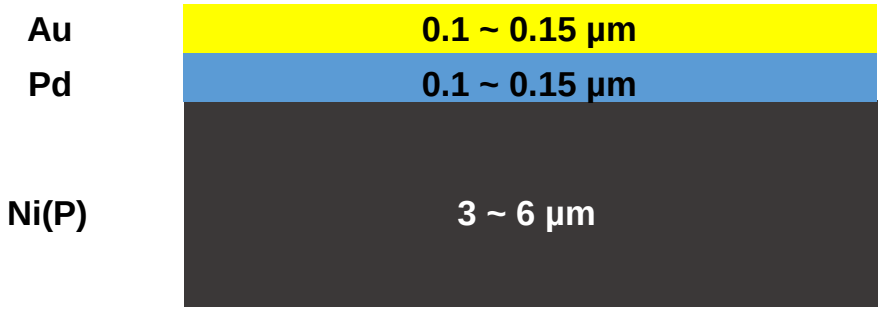
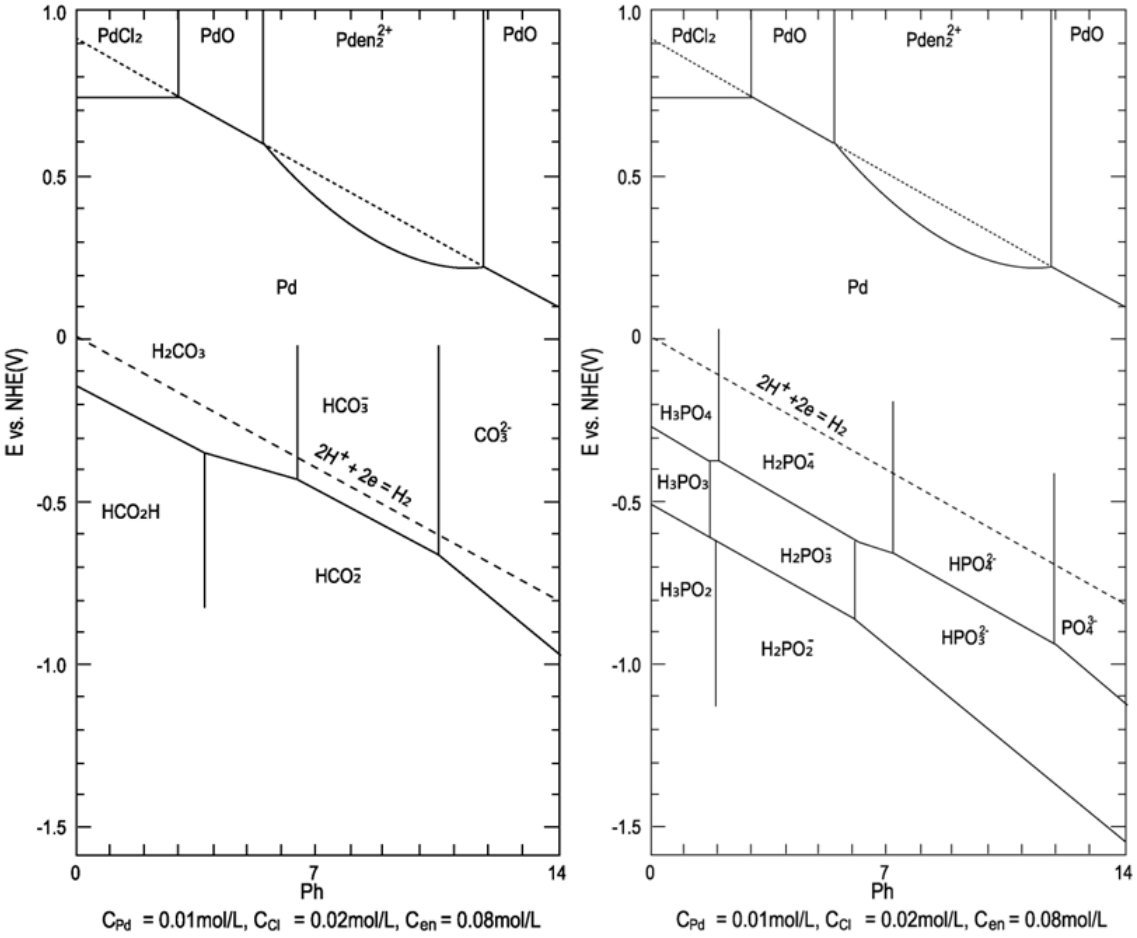


Figure 1.2 Plating thickness of surface finishes.



(a) (b)

Figure 1. 3 Potential-pH diagram; (a) $HCOO^{-}$-HCO^{3} and (b) $H_2PO_2^{-}$, HPO_3^{2-}, and PO_4^{3-}.

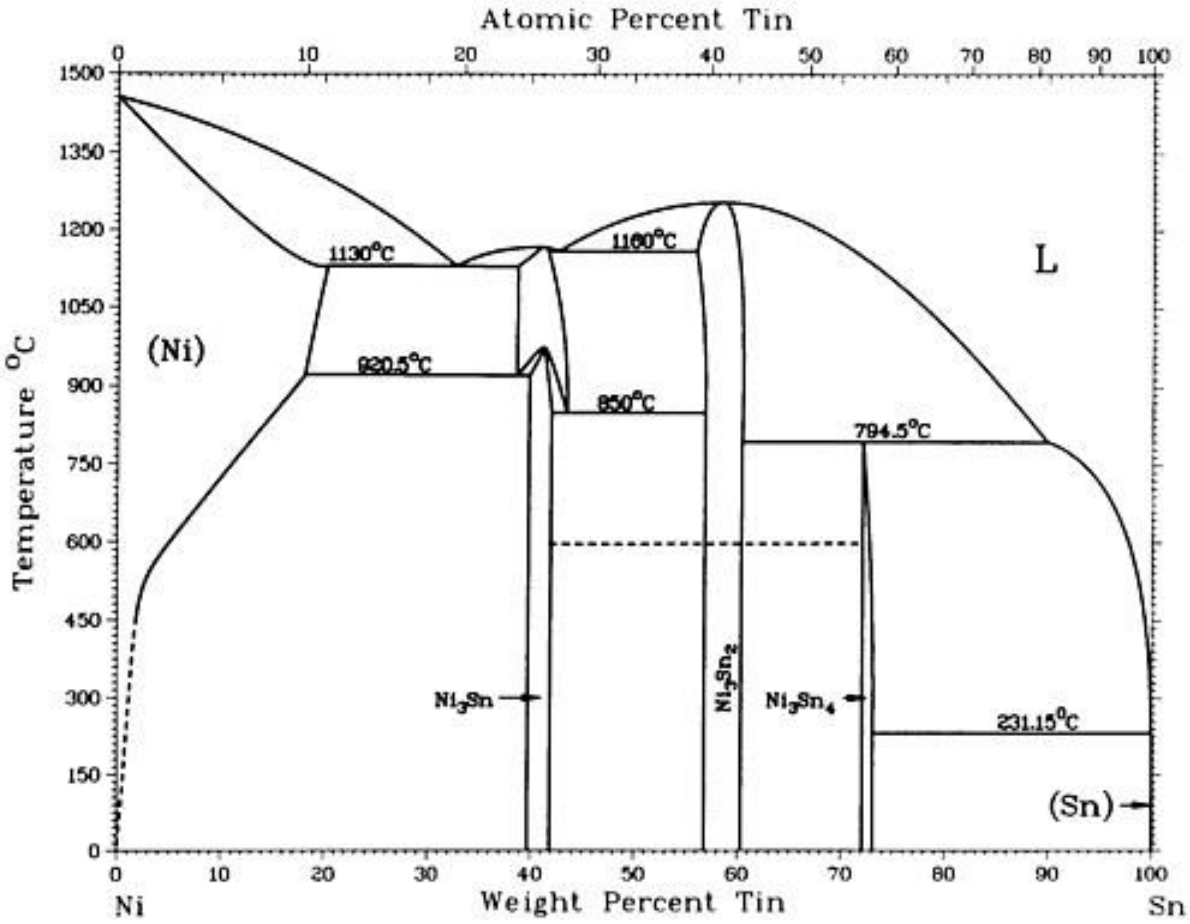


Figure 1. 4 Sn-Ni binary phase diagram.

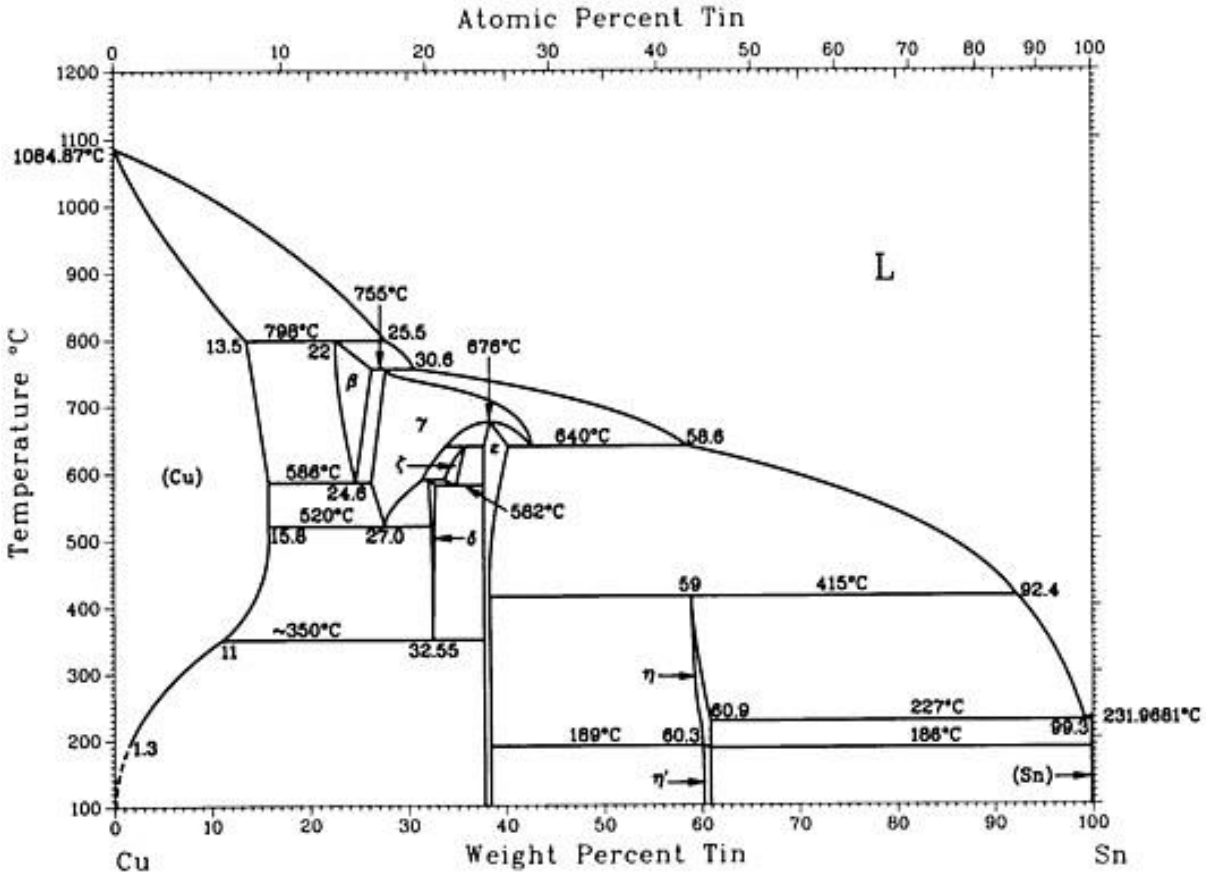
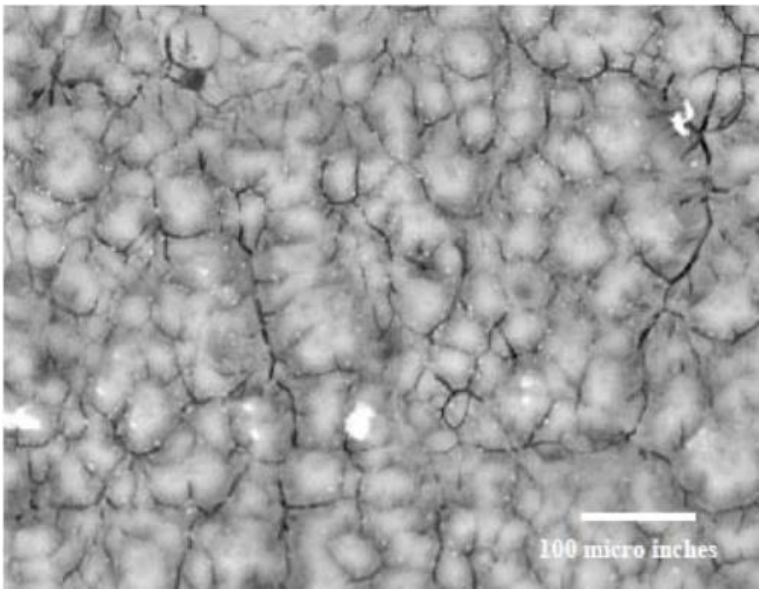


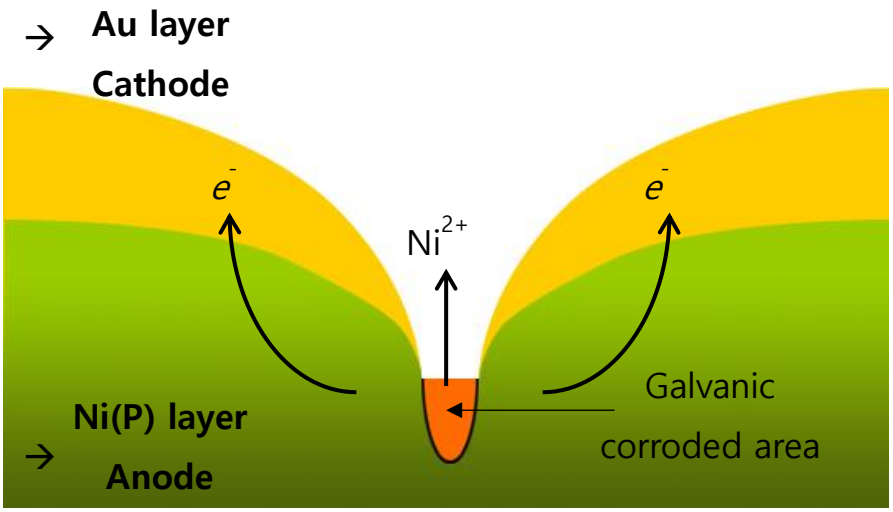
Figure 1. 5 Sn-Cu binary phase diagram.

Table 1.7 Room temperature properties of intermetallic compounds determined here.

	Cu_6Sn_5	Cu_3Sn	Ni_3Sn
Vickers Hardness (kg/mm^2)	378 ± 55	343 ± 47	365 ± 7
Toughness ($MPa.m^{-1/2}$)	1.4 ± 0.3	1.7 ± 0.3	1.2 ± 0.1
Youngs Modulus (GPa)	85.56 ± 1.65	108.3 ± 4.4	133.3 ± 5.6
Poisson's Ratio	0.309 ± 0.012	0.299 ± 4.4	0.330 ± 0.015
Thermal Expansion (ppm/°C)	16.3 ± 0.3	19.0 ± 0.3	13.7 ± 0.3
Thermal Diffusivity (cm^2/s)	1.045 ± 0.015	0.240 ± 0.024	0.083 ± 0.008
Heat Capacity (J/g.deg)	0.286 ± 0.012	0.326 ± 0.012	0.272 ± 0.012
Resistivity (μΩ .cm)	17.5 ± 0.1	8.93 ± 0.10	28.5 ± 0.1
Density (mg/cc)	8.28 ± 0.02	8.90 ± 0.02	8.65 ± 0.02
Thermal Conductivity (W/cm.deg)	0.341 ± 0.051	03704 ± 0.098	0.196 ± 0.019



(a)



(b)

Figure 1.6 Schematic diagrams showing black pad formation mechanisms; (a) voltage induced black pad formation, and (b) micro-galvanic cell formation at sharp nodule boundaries [31].

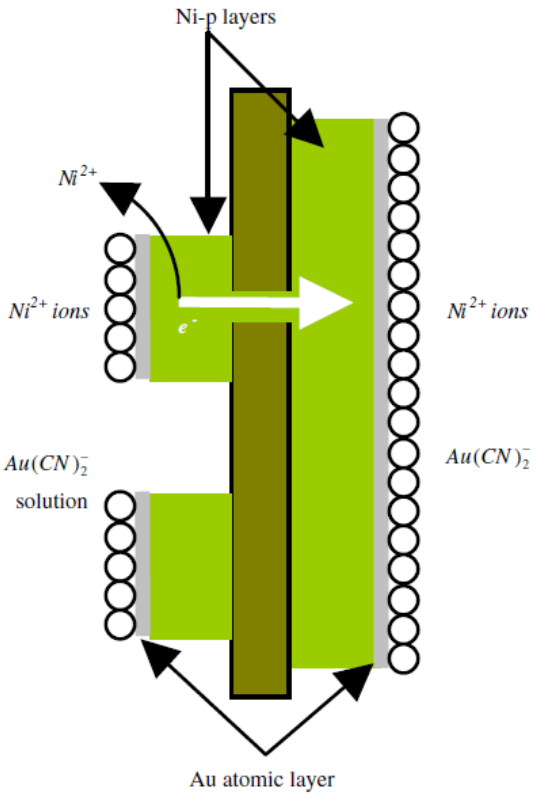


Figure 1.7 Schematic diagram showing the size-effect induced concentration cell formation [32].

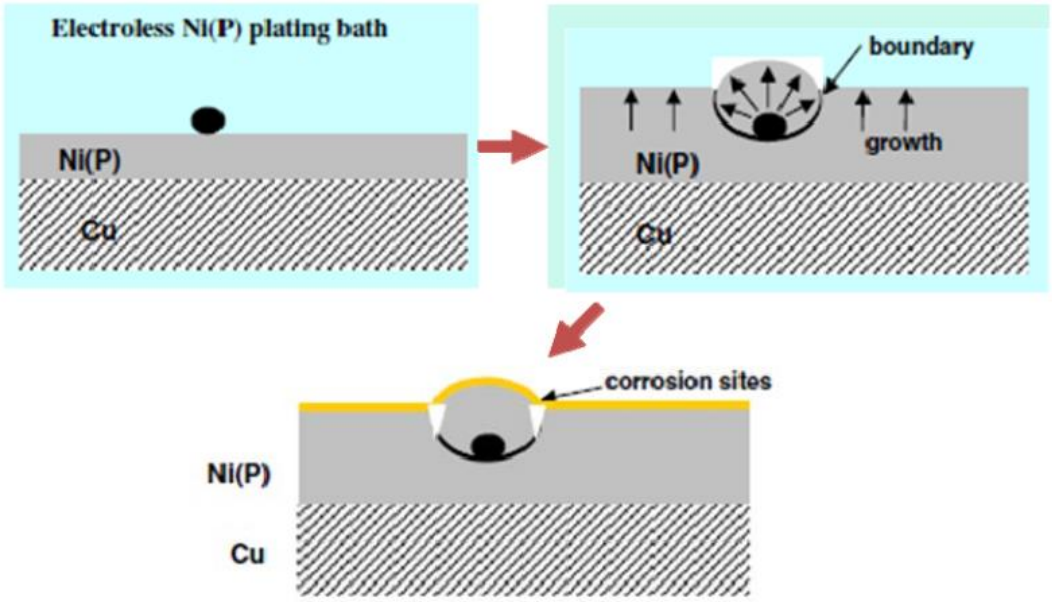


Figure 1.8 Schematic diagrams showing corrosion induced by secondary-phase precipitation during Ni(P) film growth [58].

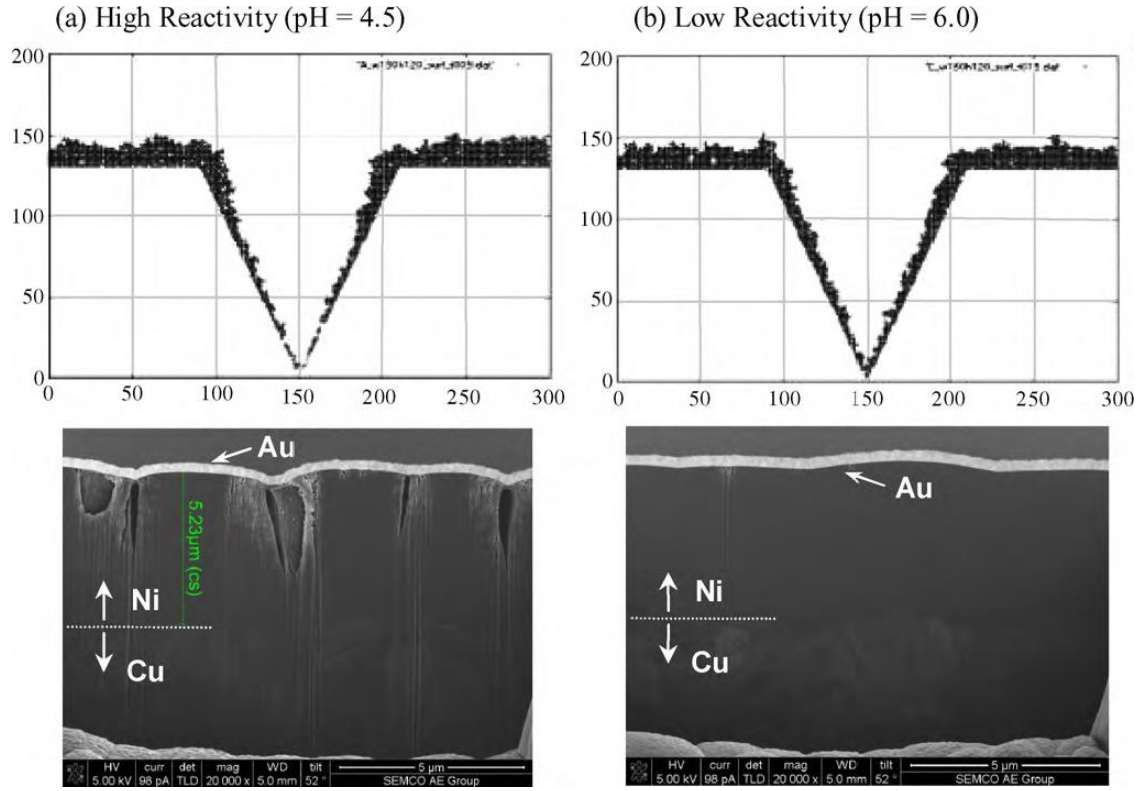


Figure 1.9 Simulated Au layer growth modes at (a) high reactivity and (b) low reactivity. The values shown on both the x and y axes are of arbitrary dimensionless form, where only the relative geometric ratio is important. Cross-sectional SEM images (20k×) of the corresponding Ni-P/Au interfaces are also shown. [59].

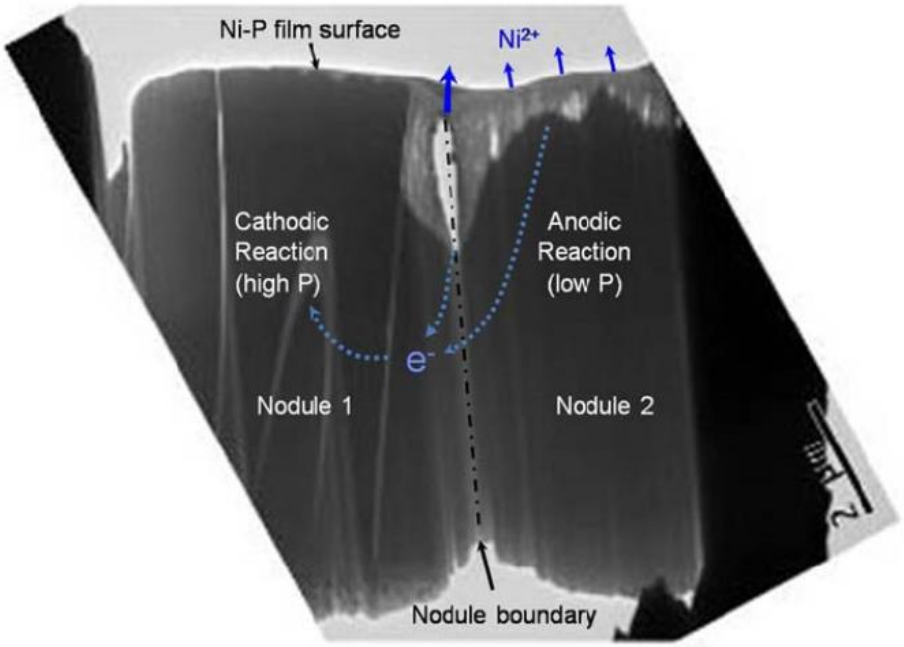
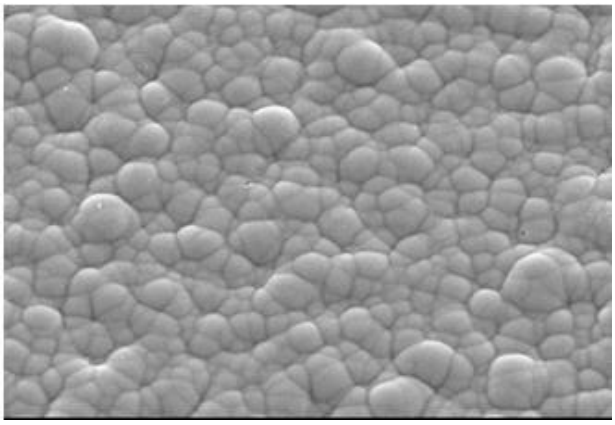
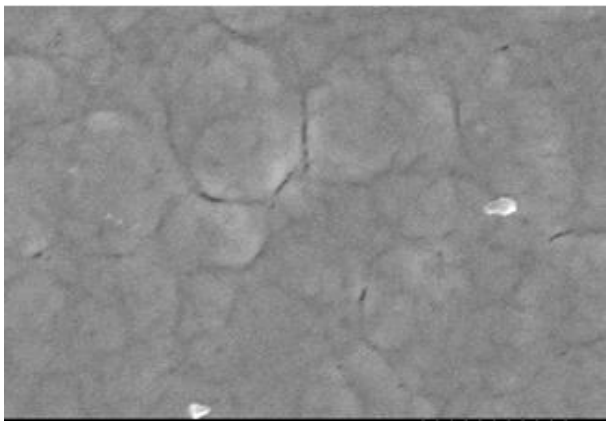


Figure 1.10 TEM image showing micro-galvanic corrosion induced by concentration gradients in P across Ni(P) nodules [60].

(a) P content: under 5%



(b) P content: 6 – 9%



(c) P content: upper 12%

Figure 1.11 Changes in the surface morphology of Ni(P) as a function of P concentration.

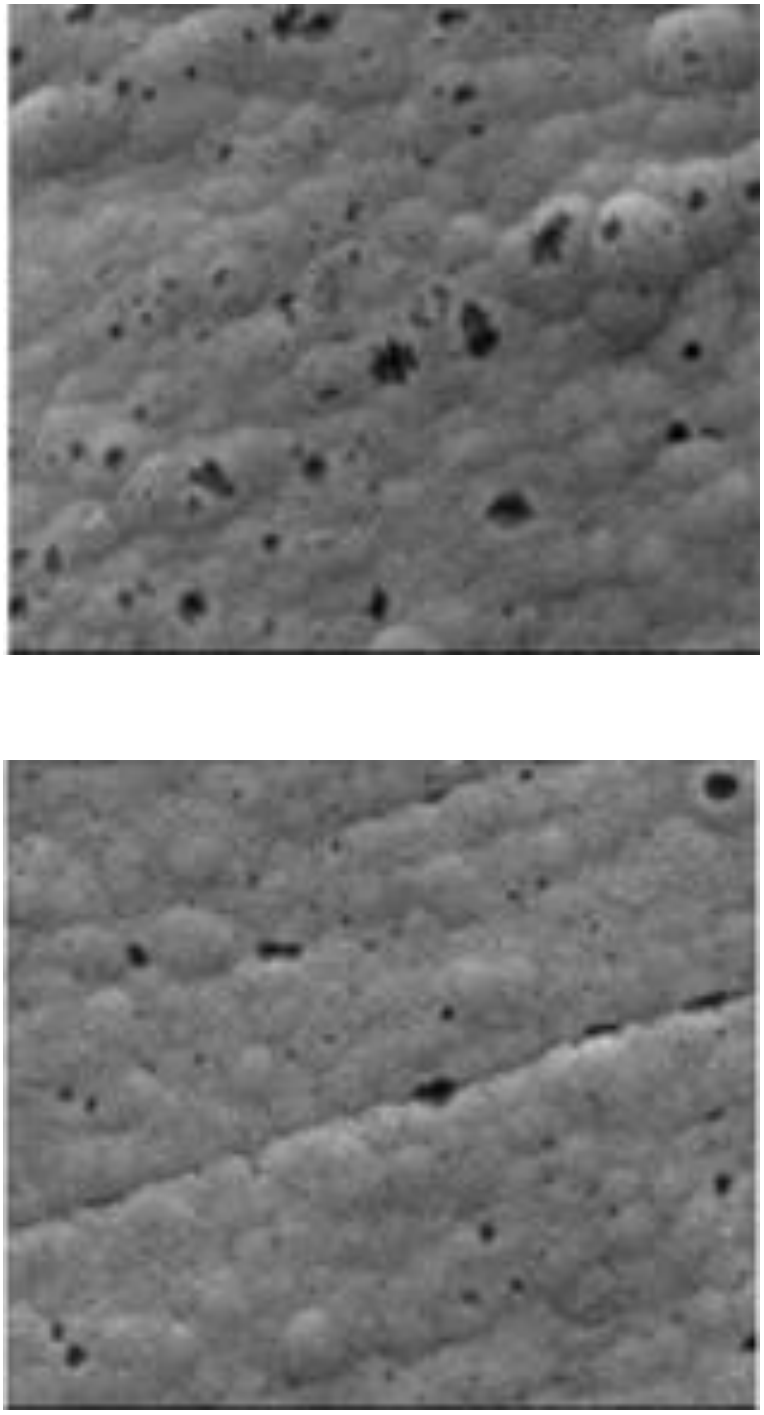
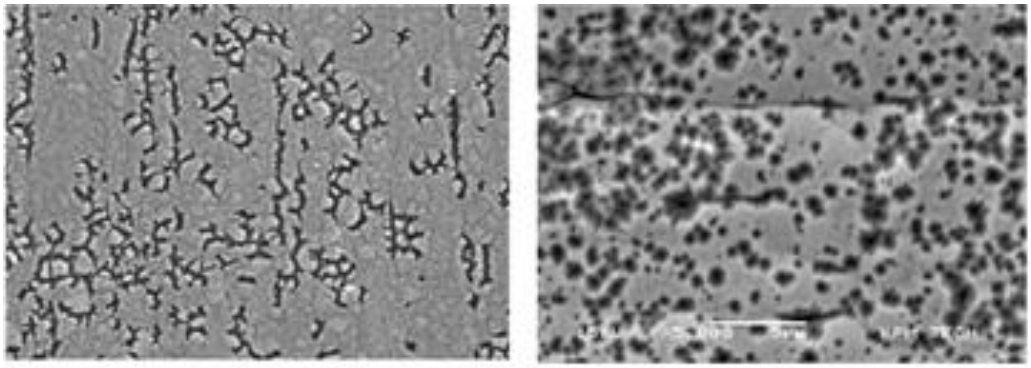


Figure 1.12 SEM micrographs showing contamination induced by Ni(P) oxidation.



(a) Corrosion of Ni(P) surface

(b) Cross-sectional observation

Figure 1.13 TEM images showing corrosion of the Ni(P) layer resulting from organic impurities. (a) Surface morphology and (b) cross-sectional image.

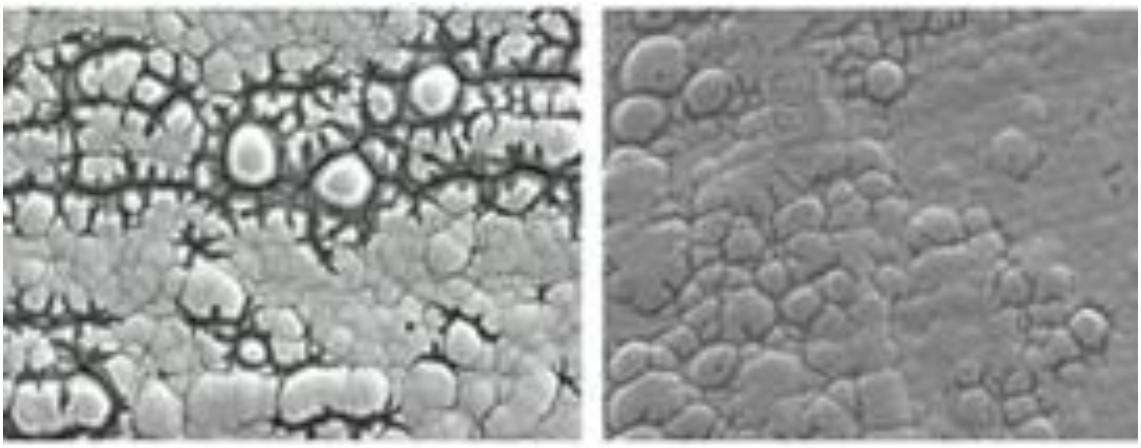


Figure 1.14 Changes in the Cu substrate morphology as a result of organic impurities.

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Chapter 2

Effect of Ni-Sn interfacial microstructure on brittle fracture of solder joint

2.1 Introduction

ENIG and ENEPIG methods have been widely adopted for surface finishing Cu bond pads due to their effectiveness as diffusion barriers against fast reaction with Sn-rich solder alloys [1-2]. The structure of the IMC layer at the interface between the Sn-3.0Ag-0.5Cu (SAC) solder and ENIG or ENEPIG layer is complex; the interface has been shown to be composed of $(Cu, Ni)_6Sn_5$, Ni-Sn-P, and P-rich layers (Ni_3P or Ni_2P)

[3]. The thickness of the Ni-Sn-P layer located between $(Cu,Ni)_6Sn_5$ and a P-rich layer was about a few tenths of a nanometer and the Ni-Sn-P layer possessed nanovoids with diameters of 10–20 nm [4]. Previous studies showed that brittle fracture at the interface resulted from poor adhesion of the P-rich layer and/or nanovoids formed in the Ni-Sn-P layer [5]. During solder reflow, the Au from the ENIG process was dissolved into the molten SAC solder, resulting in Ni(P) being exposed to the molten solder and subsequent formation of interfacial phases composed of Sn and Ni(P). Hence, the plating conditions of the Ni(P) affected the interfacial microstructure, which was related to the brittle fracture behavior of the solder joints.

In this chapter, the bath life (an important plating condition for Ni(P)) was varied and the microstructure of the SAC solder joint on the ENIG and ENEPIG surface finish was evaluated. The bath lives of the Ni(P) in this study were defined by MTOs (of 0 or 3) which indirectly represented the bath life. An MTO of 0 is a freshly made bath where no additional metal was supplemented. An MTO of 3 represented a bath with three times the amount of metal as the original concentration, which was almost a waste bath. In industry, a long bath life (or high MTO) is considerably important since it reduces costs related to preparing the bath and increases productivity of the plating. However, there exist no guidelines regarding how long the plating bath can be used before reliability problems occur after solder reflow of the Ni-based surface finish.

To understand the relationships between the bath life of Ni(P) in the ENIG and ENEPIG surface finish processes and reliability of the solder joint, and interfacial

microstructure, the brittle fracture behavior of SAC solder joints on ENIG and ENEPIG surface finishes were evaluated with different Ni(P) bath lives. The brittle fracture behavior was determined using high-speed shear (HSS) tests. In addition, the interfaces of SAC/ENIG and SAC/ENEPIG samples were observed with field emission scanning electron microscope (FE-SEM) and transmission electron microscope (TEM); the results are presented in this chapter.

2.2 Experimental

2.2.1 PCB design and surface finish

The PCB used in this study was a solder mask defined (SMD)-type FR-4 board, as shown in Figure 2.1. The diameter and thickness of a Cu pad on the test PCB were 400 μm and 10 μm, respectively. The thickness of the photo-imageable solder mask (PSR) of the test PCB was 15 μm. The Cu pad was finished using either the ENIG or ENEPIG method. The thickness of Ni and Au for ENIG was 5 μm and 0.05 μm, respectively. The ENEPIG surface finish was carried out similarly to the ENIG process up to the Ni(P) plating step. Subsequently, the surface was finished using a Pd layer and then a Au layer, both with thicknesses of 0.05 μm. The bath life of Ni(P) was either 0 or 3 MTO. The P concentrations of the Ni(P) were 6.98 and 7.74 wt% for 0 and 3 MTO, respectively. The process flow diagram of the ENIG and ENEPIG methods is shown in Figure 2.2.

The PCB design for the drop shock test is illustrated in Figure 2.3. The PCB for the drop shock test was manufactured based on JEDEC Standard D22 B111 [6]. A daisy chain was mounted to determine a pass/failure of the test. The configuration of the daisy chain on the PCB for the drop shock test is shown in Figure 2.4. The dimensions of the substrate and Cu pad opening were 132 × 77 mm and 400 μm, respectively. The BGA (AssemTech) contained 62 balls, a size of 450 μm, and pitch of 0.8 mm.

2.2.2 Metal turn over (MTO)

The MTO represents the amount of Ni ions added to compensate for those consumed by the reduction reaction. This is necessary as the plating quality deteriorates during the plating process. A higher MTO resulted in lower precipitation efficiency due to phosphite formation in the Ni(P) plating solution. In addition, an increase in the concentration of P and organic impurities from the PSR ink of the PCB were found to reduce the quality of the Ni(P) plated layer [7-9]. Figure 2.5 shows a schematic diagram of the Ni(P) plating solution with increasing MTO. The bath lives of the Ni(P) in this study had MTO values of 0 and 3, which represent the amount of supplemented metal.

2.2.3 Soldering process

Solder balls were mounted on the ENIG- and ENEPIG-finished Cu pads. For the

solder ball mounting, Sn-3.0wt%Ag-0.5wt%Cu (SAC305) solder paste (Senju, M705-SHF) was printed on the surface finished Cu pad and then a SAC305 solder ball (Ducsan Hi-Metal) with a diameter of 450 μm was mounted on the printed SAC305 solder paste. After solder ball mounting, the test PCB was reflowed in a reflow oven (Heller, 1809UL) with a peak temperature of 251 ºC. Figure 2.6 shows the SAC305 reflow profile and Figure 2.7 shows optical micrographs of the test sample after reflow.

2.2.4 Mechanical properties

2.2.4.1. Solder joint strength and brittle fracture

The shear strength and brittle fracture behavior was evaluated with a high-speed shear tester (Dage, 4000HS) [10-11]. The distance between the shear tool and the top of the PSR on the test PCB was 50 μm. The shear speed (i.e., strain rate) of the HSS test was varied from 0.1 to 2.0 m/s. An average shear strength was calculated from measurements of 25 samples for each experimental condition. Figure 2.8 shows a schematic of the HSS test layout. After the HSS test, the fracture surface was observed using optical microscopy and an FE-SEM (FEI Inspect F). The fracture surface was classified into five different ranges (100%, 75%, 50%, 25%, and 0%) corresponding to the fraction of the area over which a brittle fracture was observed. The 75%, 50%, 25%, and 0% brittle fracture represented the ranges 75–100%, 50–75%, 25–50%, and 0–25%, respectively. An average brittle fracture rate was calculated from the results

for 25 samples for each test condition. Figure 2.9 shows each classified modes and constant of brittle fracture. In this study, the brittle fracture rate was defined as follows:

$$\text{Brittle fracture rate (\%)} = \frac{\sum(A_i \cdot N_i)}{N_{tot}} \times 100 \quad (1)$$

where A_i, N_i, and N_{tot} are a brittle fracture parameter and number of samples for each brittle fracture mode (i), and the total number of samples, respectively. Here, A_i was designated as 1, 0.75, 0.5, 0.25, or 0 for the 100%, 75–100%, 50–75%, 25–50%, and 0–25% brittle fracture modes, respectively. For example, the numbers of samples corresponding to each fracture mode for the 0 MTO sample for a 0.3 m/s condition were 1, 4, 8, 5, and 7 for 100%, 75–100%, 50–75%, 25–50%, and 0–25%, respectively. Cross-sectional imaging of the joint interface was also observed using FE-SEM with energy dispersive spectroscopy (EDS) and TEM (JEOL JEM 4010). The TEM sample was prepared using a focused ion beam system (FIB, Helios 600).

2.2.4.2. Drop shock reliability

Drop shock testing was performed based on JEDEC standard xxx under the conditions shown in Table 2.1. The pulse duration and impact acceleration were 0.5 ms and 1500 G, respectively, according to the most widely used B test condition [12]. The failure criterion was defined as when the resistance at the daisy chain was more than 100 Ω. The BGA was mounted using the SMT process and a photograph of the prepared sample is shown in Figure 2.10. The BGAs were mounted at U2, U4, U8,

U12, and U14. It was revealed that the U8 package had the most PCB warpage due to the shock.

2.3 Results and discussion

2.3.1 HSS strength and brittle fracture behavior

2.3.1.1. ENIG surface finish

The HSS strengths of the SAC/ENIG with different MTO values of Ni(P) are shown in Figure 2.11, for strain rates between 0.1 and 2.0 m/s. The HSS strength decreased as the strain rate increased for all samples. In general, the strength of the Sn-base solder increased with increasing strain rate (i.e. strain rate hardening occurred). As the strain rate increased, the solder matrix was strengthened and the fracture site moved to the weaker IMC layer. Higher shear speeds resulted in more fractures occurring in the IMC layers. Therefore, the shear strength of SAC/ENIG joints decreased with increasing shear speed. For the solder joint of the 0 MTO sample, the average shear strength was 6.51 kgf/mm^2 which decreased to 5.43 kgf/mm^2 as the strain rate increased from 0.1 to 2.0 m/s. It has been reported that the shear strength of a SAC solder joint decreased with strain rate when the strain rate was higher than 0.1 m/s [13]. Sn-based solders have been shown to experience strain rate hardening during shear tests [14]. We observed the failure site moving from the solder to the weaker IMC layers as the strain rate increased, which resulted in decreasing shear strength

with increasing strain rate. The HSS strength was dependent on the bath life of Ni(P). The 0 MTO samples showed a higher HSS strength than the 3 MTO samples; the average HSS strength at 2.0 m/s was 5.79 kgf/mm^2 and 4.74 kgf/mm^2 for 0 and 3 MTO, respectively.

To understand the effect of the Ni(P) bath life on the fracture behavior of SAC/ENIG, the fracture surface after the HSS test was observed using SEM. EDS analyses showed that the ductile fracture surface was mainly composed of Sn and the brittle fracture surface was composed of Ni, Sn, P, and Cu, which indicated that the ductile fracture occurred at the solder region and the brittle fracture occurred at the IMC layer. Since the total number of samples was 25, the brittle fracture rate derived from Eq. (1) was 37.0% for the 0 MTO sample under a strain rate of 0.3 m/s. Figure 2.12 shows the brittle fracture rate of the SAC solder joint on ENIG (0 and 3 MTO) with varying strain rate. The brittle fracture rate increased as the strain rate increased. Under a strain rate of 0.5 m/s, the 0 MTO samples showed a lower brittle fracture rate than the 3 MTO samples. As the strain rate increases to 2.0 m/s, most samples showed almost 100% brittle failure due to the high strain rate.

2.3.1.2. ENEPIG surface finish

The HSS strengths of SAC/ENEPIG as a function of MTO are shown in Figure 2.13. The joint strength of both 0 and 3 MTO samples showed a tendency to decrease within

1.0 kgf/mm^2 when the strain rate increased. The 0 MTO samples showed a higher HSS strength than the 3 MTO samples; the average HSS strength at 2.0 m/s was 6.82 kgf/mm^2 and 6.54 kgf/mm^2 for 0 and 3 MTO, respectively.

The brittle fracture rate of the ENEPIG surface finish was calculated using Eq. (1) and is shown as a function of strain rate in Figure 2.14. At 0 MTO, the brittle fracture rate was 0% up to 0.3 m/s strain rate and increased to 30% at strain rates above 2.0 m/s. Although the 3 MTO samples exhibited a higher brittle fracture rate, the 0 MTO samples reached 70% at a strain rate of 2.0 m/s, indicating a higher brittle fracture rate than the ENIG samples. The strength and brittle fracture properties of 0 MTO were superior to those of 3 MTO for both ENIG and ENEPIG surface finishes. As the bath life of the Ni(P) plating solution increased, the mechanical properties of the solder joint deteriorated.

2.3.1.3. Main effect and interaction

The main effect and interaction were analyzed in accordance with joint strength and brittle fracture properties of ENIG and ENEPIG surface finishes. The joint strength of the ENEPIG surface finish was better than that of the ENIG finish. Furthermore, the ENEPIG surface finish exhibited a lower decrease in strength with increasing strain rate. In conclusion, the best mechanical properties were observed for the ENEPIG surface finish at 0 MTO.

2.3.2. Microstructure and IMC thickness

The SAC305 solder has a melting point of 217 °C [15] and consists of an inner primary Sn phase, a Ag_3Sn-type dendrite structure, and a Cu_6Sn_5 phase [16]. As the distribution of the Ag_3Sn-type dendrite structure and Cu_6Sn_5 phase increases, the solder becomes brittle [17]. Figure 2.15 shows the internal solder system deposited onto ENIG and ENEPIG surface finishes. From FE-SEM/EDS observations, a similar distribution of the inner primary Sn, Ag_3Sn, and Cu_6Sn_5 phases was found for both types of surface finished samples. Thus, the effect of surface finish on the inner solder structure was negligible. Figures 2.16 and 2.17 show cross-sectional SEM micrographs of the IMC layer for the SAC/ENIG and SAC/ENEPIG systems. In this study, the thickness of the Au layer was 0.05 μm, which was thin enough to dissolve into the molten SAC solder during reflow. Therefore, no Au compound was formed in the solder matrix or at the interface. After Au dissolution into the SAC solder, the Ni(P) was exposed to molten SAC solder, which resulted in $(Cu,Ni)_6Sn_5$ formation at the joint interface. The thickness of the $(Cu,Ni)_6Sn_5$ layer in the SAC/ENIG system depended on the bath life of the Ni(P) plating solution. The average thickness of the $(Cu,Ni)_6Sn_5$ layer was 1.24 μm for the 0 MTO sample and 2.71 μm for the 3 MTO sample. Both 0 and 3 MTO samples showed shallow pits at the solder joint interface and the pit size of the 3 MTO sample was larger than that of the 0 MTO sample. Image analysis calculated areas of the P-rich layer for the 0 and 3 MTO samples of 4.59 and 6.65 μm^2, respectively. Hence, the thickness of the P-rich layer for the 3 MTO sample

was higher than that of the 0 MTO sample. Since the P-rich layer was formed by Ni diffusion toward the $(Cu,Ni)_6Sn_5$ IMC layer, the thickness of the P-rich layer correlated with that of the IMC thickness. The thick IMC and P-rich layers of the 3 MTO sample indicated that the amount of Ni diffusion through the interface was higher for this sample than that of the 0 MTO sample. In addition, the shallow pitted region of the 3 MTO sample had a thicker P-rich layer than rest of the interfacial region, indicating that more Ni diffusion occurred in this region. Therefore, these shallow pits played a role as a fast diffusion path for Ni.

On the other hand, the IMC thickness in the ENEPIG surface finish samples was 1.07 μm for the 0 MTO sample and 1.22 μm for the 3 MTO sample. An increase in IMC thickness was observed in both ENIG and ENEPIG samples with increasing MTO where that of the ENEPIG sample was about 1.2 times higher than for the ENIG sample. Figure 2.19 and Figure 2.20 show TEM micrographs of IMCs grown in the ENIG and ENEPIG systems, respectively for both MTO conditions. These results indicated significant growth of the IMC layer in the ENEPIG surface finish system. The P-rich layer of the ENEPIG surface finish sample was found to be thinner than that of the ENIG surface finish sample. The P-rich layer was generated from the remaining concentration of P, which showed a relative increase due to Ni ion diffusion (and IMC formation) in the Ni(P) layer. Hence, a thinner P-rich layer indicates better control of the Ni diffusion. Accordingly, thinner IMC and P-rich layers were formed in the Pd layer of the ENEPIG surface finish due to the controlled Ni, Sn, Cu diffusion

compared to the ENIG system, resulting in a lower brittle fracture rate since the growth of the brittle IMC layer was inhibited.

2.3.2.1. Nanovoids

In order to understand the decrease in joint strength and increase in brittle fracture behavior with increasing MTO, the microstructure after surface finishing was analyzed. Figures 2.19 and 2.21 show the microstructure as a function of the MTO of the surface finish for ENIG and ENEPIG systems. Figure 2.19 shows that Au ions diffuse into the Ni(P) layer for both ENIG 0 MTO and 3 MTO conditions. On the contrary, Figure 2.21 shows that for the ENEPIG samples, the diffusion of the Au ions into the Ni(P) layer is prevented by the Pd layer. However, the diffusion of Pd ions into the Ni(P) layer under 3 MTO conditions for the ENEPIG system was observed. In the process of soldering, the Au and Pd layers were dissolved into the solder, and then the IMC was formed as the Ni(P) layer on the Ni(P)/SAC interface decayed. However, an uneven Ni(P) layer caused a decrease in solderability. Yoon et al. [18] showed that the nodule size of the Ni(P) layer changed with variations in pH of the plating bath, and solderability decreased with increasing RMS of the film. Therefore, it is very important to maintain a stable plating quality of the Ni(P) layer.

To understand the brittle fracture behavior of the Ni(P) plating solution as a function of MTO, the ENIG and ENEPIG surface finish samples were analyzed by TEM after soldering. Figure 2.21 shows the cross-sectional microstructure analyzed by

TEM of the $(Cu,Ni)_6Sn_5$ IMC and P-rich layers of the ENIG surface finish sample as functions of MTO. Nanovoids were observed in the NiSnP layer formed between P-rich and $(Cu,Ni)_6Sn_5$ layer for both the 0 MTO and 3 MTO samples. The nanovoids in the 3 MTO sample were larger than those of the 0 MTO sample; 20–40 nm and 5–10 nm, respectively. Figure 2.22 shows TEM images of the microstructure of cross-sections of ENEPIG surface finish sample. No nanovoids were observed, regardless of the MTO condition. Three mechanisms for nanovoid formation are proposed; (1) the Kirkendall void mechanism resulting from the difference in Sn and Ni diffusivity during the solder reflow process [4,7,19], (2) the result of incorporated organic material [3], and (3)…. Laurila et al. [3] reported that nano-sized features, which appeared to be “voids” were actually organic nano-particles when analyzed by high-resolution phase contrast TEM. Such organic nanoparticles on the PCB surface probably originated from the Ni(P) plating bath. The plating bath for the 3 MTO sample was almost a waste solution, which possessed more organic contaminants than the 0 MTO sample. If the number of nanovoids increases due to organic contaminants falling from the PSR ink onto the surface of the PCB, then the number of nanovoids should increase with the size of the PCB. Therefore, the nanovoids should increase, not only for 3 MTO, but also for MTOs of 1 and 2. However, this is unlikely, as the degradation in the mechanical properties was observed only for an MTO of 3, as shown in Figures 2.11 and 2.13. Lastly, Chung et al. [19] have reported that nanovoid generation is a result of galvanic corrosion caused by the potential differences between

the Ni(P) and Au layers. They also stated that the P content in that case was 5–9 wt.%. In this study, nanovoids were observed, as shown in Figure 2.17(b), where the P content of the 3 MTO was 9.62 wt.%. Therefore, it is proposed that the reason the number of nanovoids increased for the ENIG 3 MTO sample was galvanic corrosion between the Ni(P) and Au layers in the immersion Au plating process.

In contrast, even though a defect in the Ni(P) layer was observed for the ENEPIG 3 MTO in Figure 2.19(b), nanovoids were not observed in Figure 2.20(b). In order to understand this phenomenon more clearly, thermal aging was carried out for 100 h at 150 °C. After the thermal aging, nanovoids was observed on the ENEPIG sample. A cross-sectional TEM micrograph of the 0 MTO ENEPIG sample is shown in Figure 2.24(a), where nanovoids with a diameter of about 5 nm were observed, while nanovoids with a diameter of about 10–20 nm were found for the 3 MTO sample shown in Figure 2.24(b). The reason for the larger nanovoids in the as-reflowed sample was that Kirkendall voids grew during the process of diffusion of internal microstructure. Both Figures 2.23 and 2.24 indicate that the size of the nanovoids was greater for the 3 MTO sample than for the 0 MTO sample, for both ENIG and ENEPIG surface finishes. This is consistent with the results of the analyses of the mechanical properties and microstructures of the as-deposited samples.

2.3.3 Brittle fracture mechanism of ENIG surface finish with increasing MTO

The fracture surface after the HSS test was observed using optical microscopy, as

shown in Figure 2.25. For the 3 MTO sample, circular features were observed on the fracture surface. We prepared another fracture surface sample and SEM with EDS mapping was carried out, as shown in Figure 2.26. In the EDS mapping of the 3 MTO sample (b), the circular features were clearly observed in the Sn map, however the brightness within the circular features was very low, indicating that these features did not contain Sn. The interfacial phase that did not contain Sn was the P-rich layer (Ni_3P). Therefore, it is concluded that the circular features on the fracture surface of the 3 MTO sample were P-rich. Figure 2.27 shows a cross-sectional SEM micrograph of the fracture surface region outside the circular features, where the fracture occurred mainly in the $(Cu,Ni)_6Sn_5$ IMC and at Ni-Sn-P layers. To confirm the phase of the circular features, a cross-section of one of these features on the fracture surface was observed using TEM, as shown in Figure 2.28, where it can be seen that the circle was mainly composed of P-rich material. The Ni-Sn-P phase was also observed in the cross-section. For the circular feature on the fracture surface, the crack propagated mainly through the P-rich layer. Such features were possibly formed due to the thick P-rich layer in the 3 MTO sample. In summary, the fracture in the 0 MTO sample occurred in $(Cu,Ni)_6Sn_5$ and Ni-Sn-P layers the fracture in the 3 MTO sample occurred in these layers as well as the P-rich layer. Previous studies reported that the brittle fracture at the interface resulted from weak adhesion of the P-rich layer and/or nanovoids formed in the Ni-Sn-P layer [20-21].

In conclusion, the 3 MTO sample had thicker $(Cu,Ni)_6Sn_5$ and P-rich layers than the

0 MTO sample. The thick P-rich layer of the 3 MTO sample resulted in circular features on the fracture surface. In addition, the 3 MTO sample showed large nanovoids at the solder joint interface. Hence, the interface of the 3 MTO sample was weaker than that of the 0 MTO sample and showed enhanced brittle fracture behavior.

2.3.4 Dependence of brittle fractures on nanovoid size

In order to more clearly understand the correlation between nanovoid size and brittle fracture behavior, the percentage of brittle fracture was plotted as a function of nanovoid size (measured from the TEM images), as shown in Figure 2.29. As shown in Figure 2.29 (a), the nanovoid size for the ENIG 0 MTO sample was around 15 nm for the initial condition and around 40 nm after thermal aging, while the ENEPIG 0 MTO sample had nanovoids under 2 nm for the initial condition which did not grow significantly after thermal aging. The thickness was the highest for the ENIG 3 MTO sample, followed by ENIG 0 MTO, ENEPIG 3 MTO, and ENEPIG 0 MTO. The percentages of brittle fracture followed the same order as the thickness values, indicating a proportional relationship between nanovoid size and brittle facture. Table 2.2 displays the nanovoid size and percentage brittle fracture data.

2.3.5 Drop shock reliability

According to the drop shock test results of SAC/ENIG and SAC/ENEPIG samples,

all failure occurred in the U8 package, as shown in Figure 2.30. The failure of the ENIG surface finish occurred after 4 cycles for the 0 MTO samples and 1 cycle for the 3 MTO samples. Meanwhile, the failure of the ENEPIG surface finish occurred after 9 cycles and 31 cycles for 0 MTO and 3 MTO samples, respectively. Hence, the SAC/ENEPIG joint had better drop shock reliability compared to the SAC/ENIG joint. Figure 2.32 shows SEM images of cross-sections of fracture regions after the drop shock tests. Cracks were observed at the interface between the $(Cu,Ni)_6Sn_5$ and P-rich layers in both ENIG and ENEPIG surface finish samples. The decrease in drop shock reliability with increasing MTO originated from increasing IMC thickness due to nanovoid formation in the NiSnP layer, which proportionally increased the brittleness.

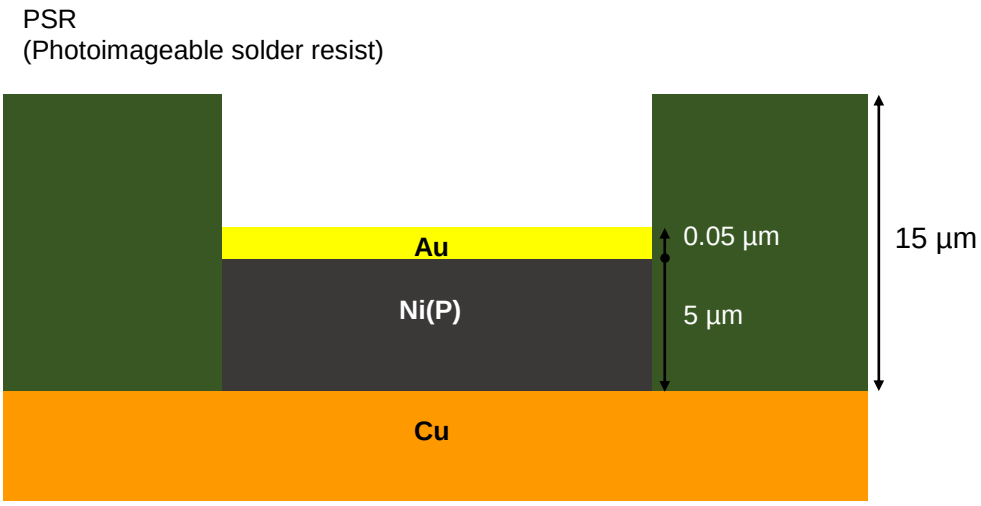
2.4 Summary

The effect of the bath life of Ni(P) in ENIG on the brittle fracture behavior of the SAC solder joint was investigated in this study. After reflow, the 0 MTO sample had a lower $(Cu,Ni)_6Sn_5$ thickness than the 3 MTO sample. The thickness of the P-rich layer in the 3 MTO sample was higher than that of the 0 MTO sample. The 3 MTO sample had large shallow pits at the interface between the $(Cu,Ni)_6Sn_5$ and Ni(P) layers after reflow. The pitted region of the 3 MTO sample had a thick P-rich layer and possibly enhanced Ni diffusion, yielding the corresponding thick $(Cu,Ni)_6Sn_5$ layer. The brittle fracture behavior of the 0 MTO sample was superior to that of the 3 MTO sample. During the HSS testing, the fracture normally occurred at multiple sites in the

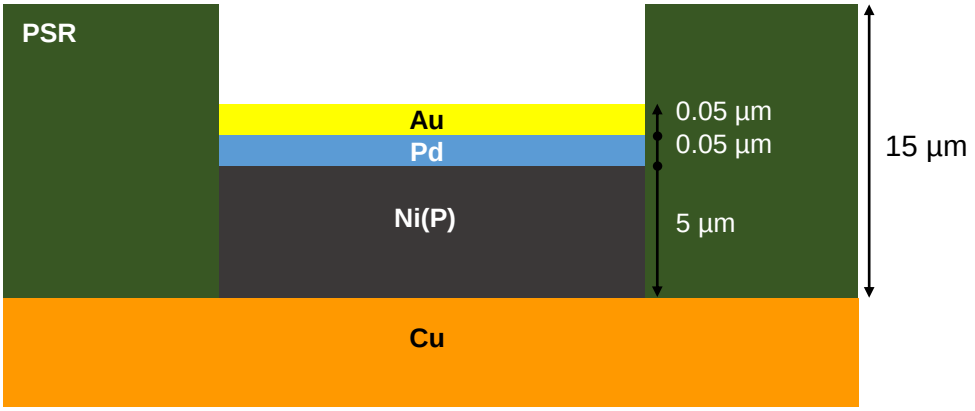
$(Cu,Ni)_6Sn_5$, Ni-Sn-P, and P-rich layers. However, the 3 MTO sample showed circular features on the brittle fracture surface which were identified as exposed P-rich layers. The size of the nanovoid in the Ni-Sn-P layer was higher in the 3 MTO sample than in the 0 MTO sample. The weak interfacial microstructures (thick P-rich layer and large nanovoids) appeared to increase the brittle fracture rate of the 3 MTO sample.

2.5 Figures

Figure 2.1 Photograph of the PCB tested for joint strength measurements.



(a) ENIG surface finish



(b) ENEPIG surface finish

Figure 2.2 Schematic images of the test substrates. (a) ENIG surface finish, and (b) ENEPIG surface finish.

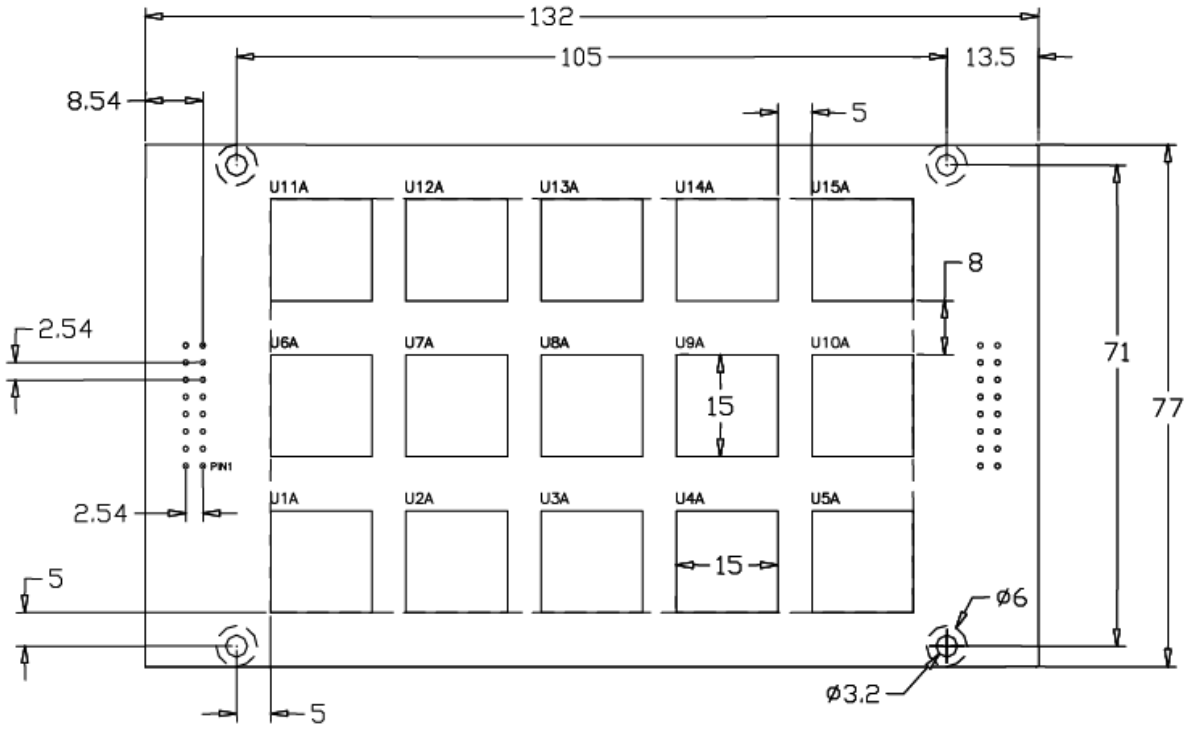
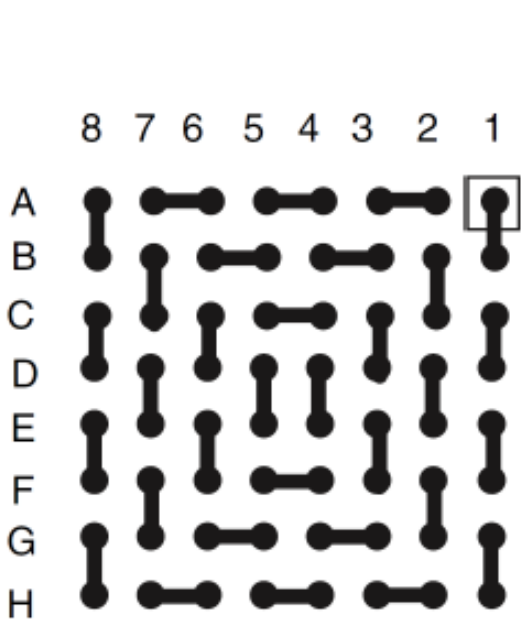
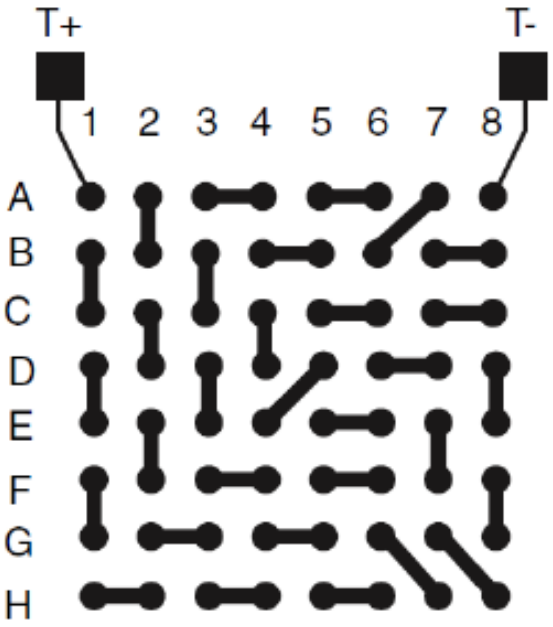


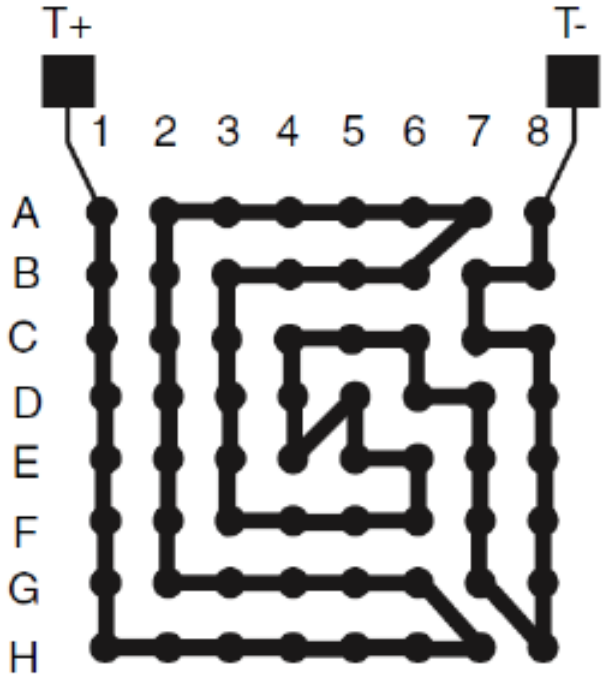
Figure 2.3 Schematic diagram of the PCB used for the drop shock tests.



(a) Ball side



(b) Test PCB side



(c) After mounting to test PCB

Figure 2.4 Schematic diagrams of the daisy chains in this study. (a) Ball side, (b) test PCB side, and (c) after mounting to the PCB.

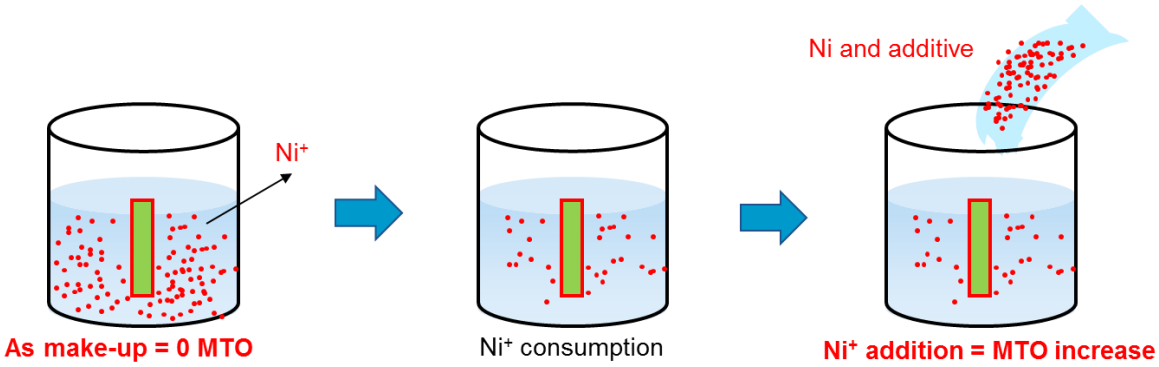


Figure 2.5 Schematic showing the metal turn over (MTO) of the plating solution.

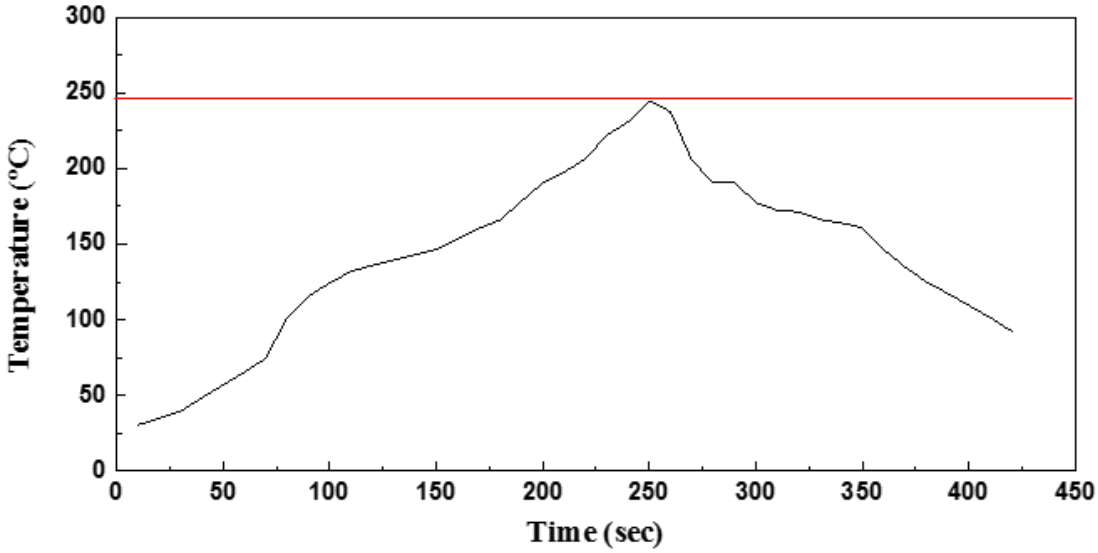


Figure 2.6 Temperature vs. time reflow profile for the Sn-3.0Ag-0.5Cu solder.

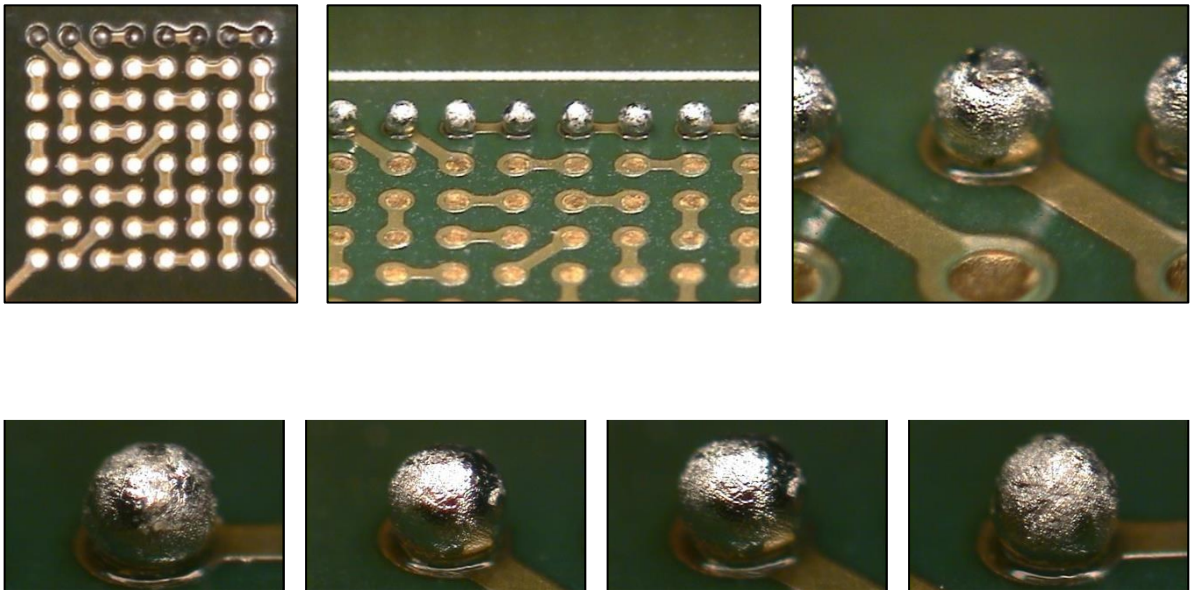


Figure 2.7 Optical micrographs of the SAC305 solder balls on the surface-finished test PCB.

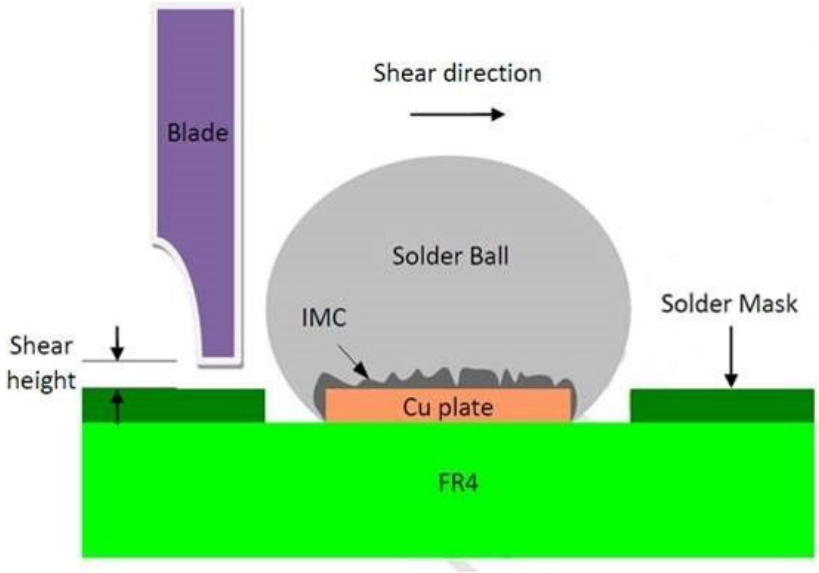


Figure 2.8 Schematic showing the HSS test setup.

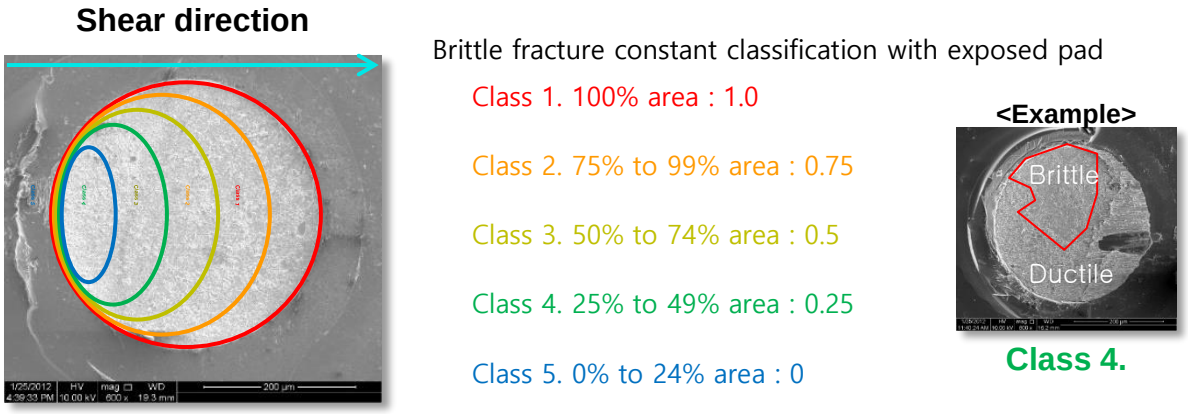


Figure 2.9 Definition of the percentage of brittle fracture ranges.

Table 2.1 Experimental conditions and equations for drop tests.

Service condition	Equivalent drop height (inches) / (cm)	Velocity change (in/s) / (cm/s)	Peak acceleration (G)	Pulse duration (ms)
H	59 / 150	214 / 543	2900	0.3
G	51 / 130	199 / 505	2000	0.4
B	44 / 112	184 / 467	1500	0.5
F	30 / 76.2	152 / 386	900	0.7
A	20 / 50.8	124 / 316	500	1.0
E	13 / 33.0	100 / 254	340	1.2
D	7 / 17.8	73.6 / 187	200	1.5
C	3 / 7.62	48.1 / 122	100	2.0

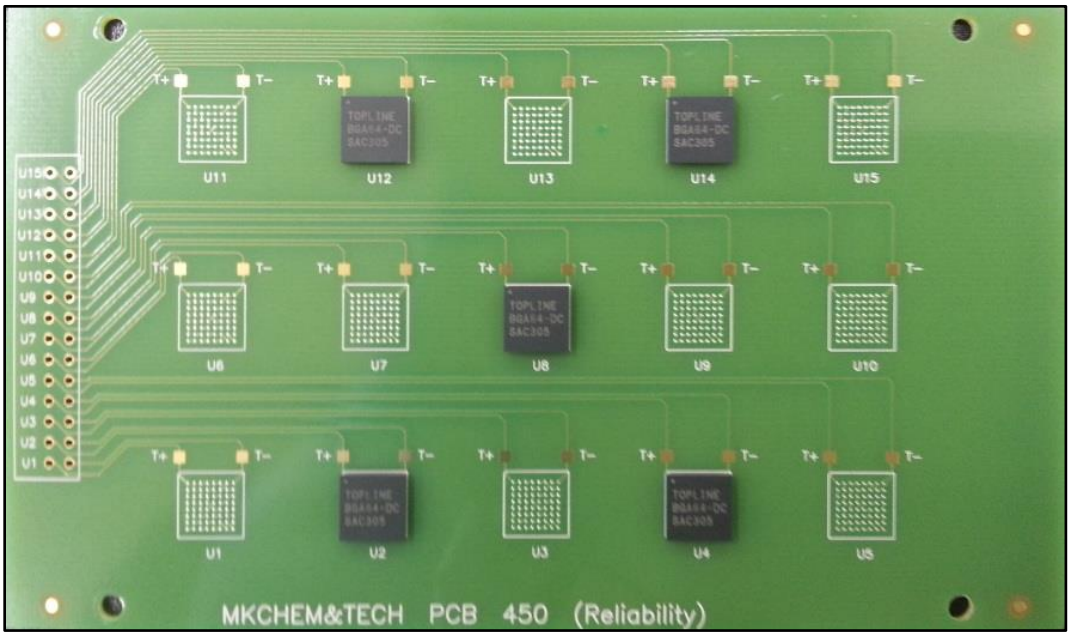


Figure 2.10 Photograph showing the BGA mounting configuration on the test PCB.

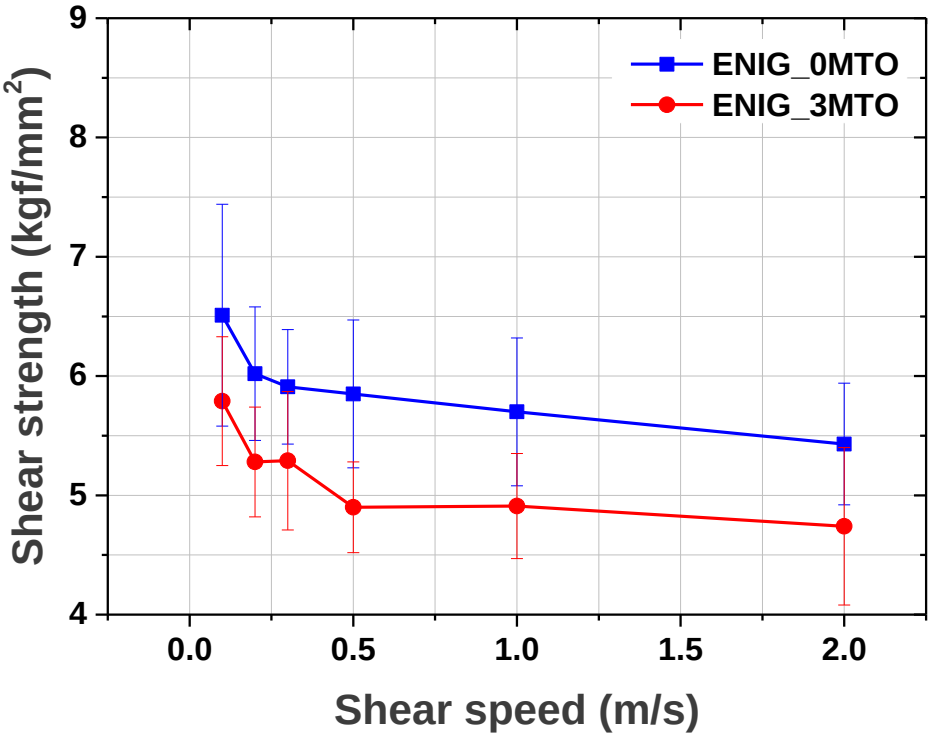


Figure 2.11 High-speed shear strength as a function of shear speed for SAC/ENIG samples with different bath lives of Ni(P).

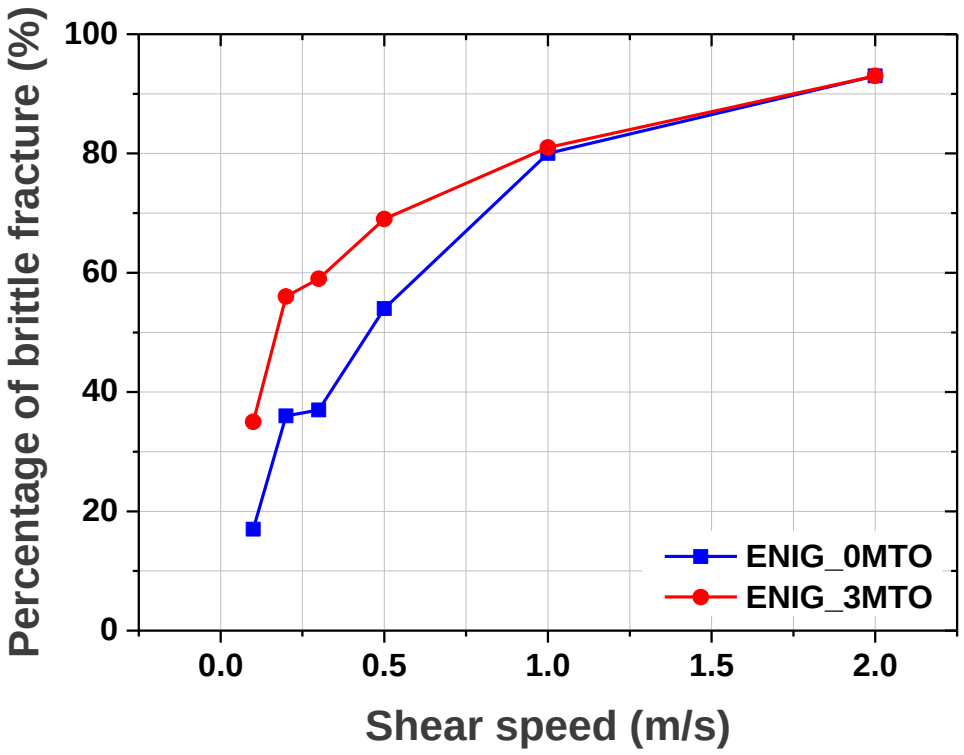


Figure 2.12 Percentage of brittle fracture rate as a function of shear speed for the SAC/ENIG samples with different bath lives of Ni(P).

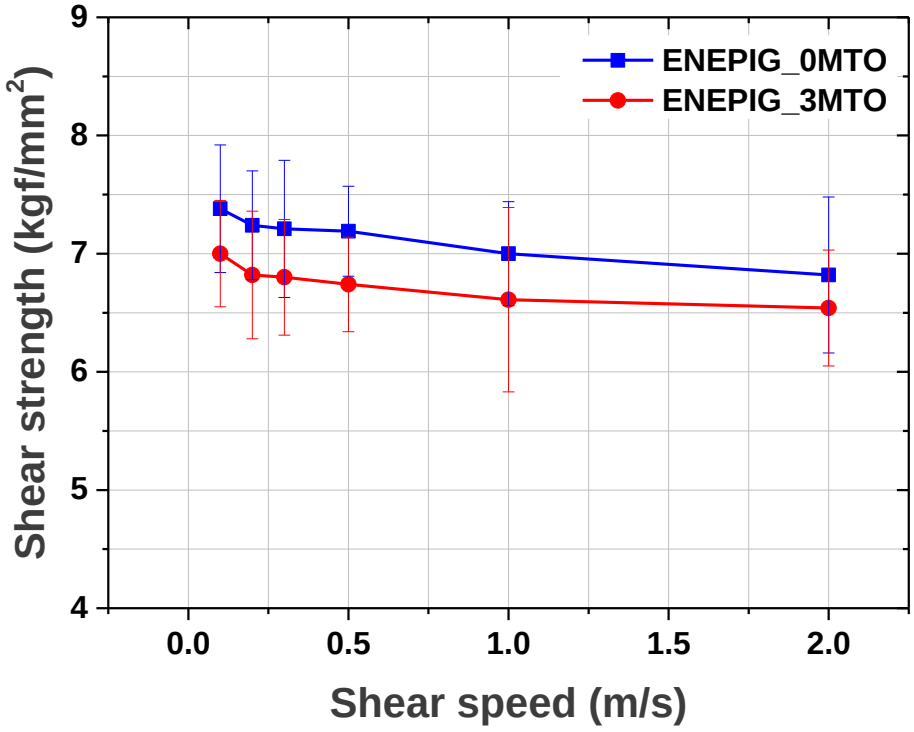


Figure 2.13 **High-speed shear strength as a function of shear speed for SAC/ENEPIG samples with different bath lives of Ni(P).**

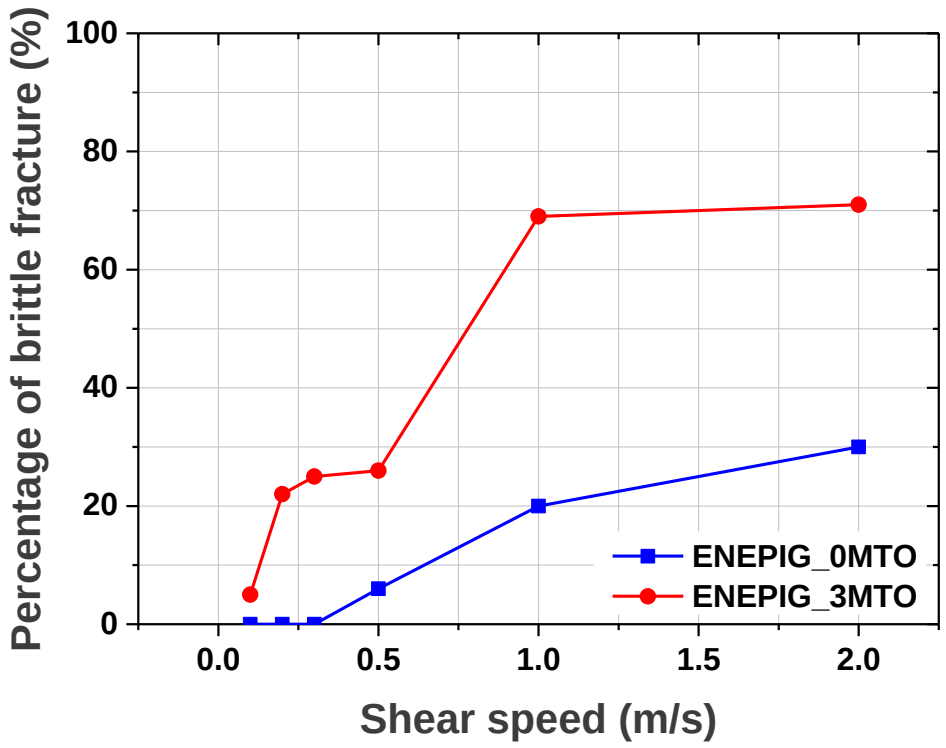


Figure 2.14 Percentage of brittle fracture as a function of shear speed for the SAC/ENEPIG samples with different bath lives of Ni(P).

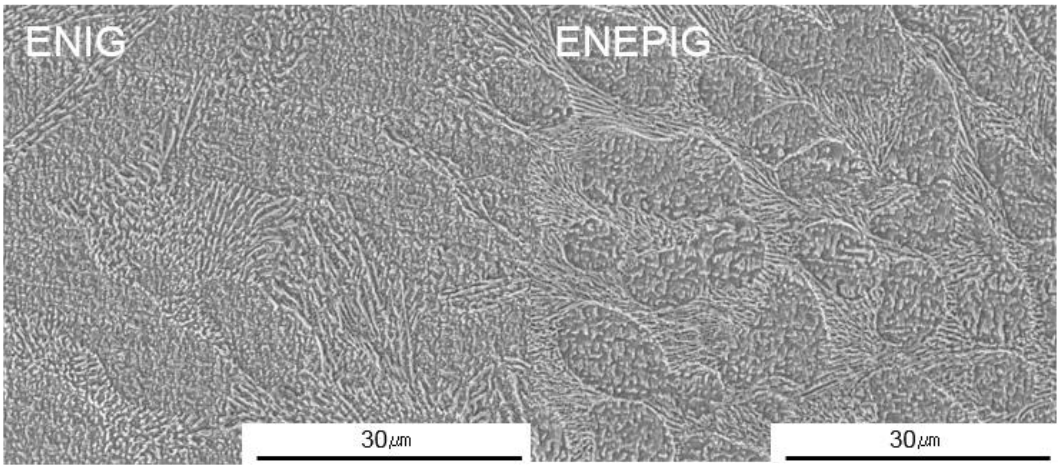
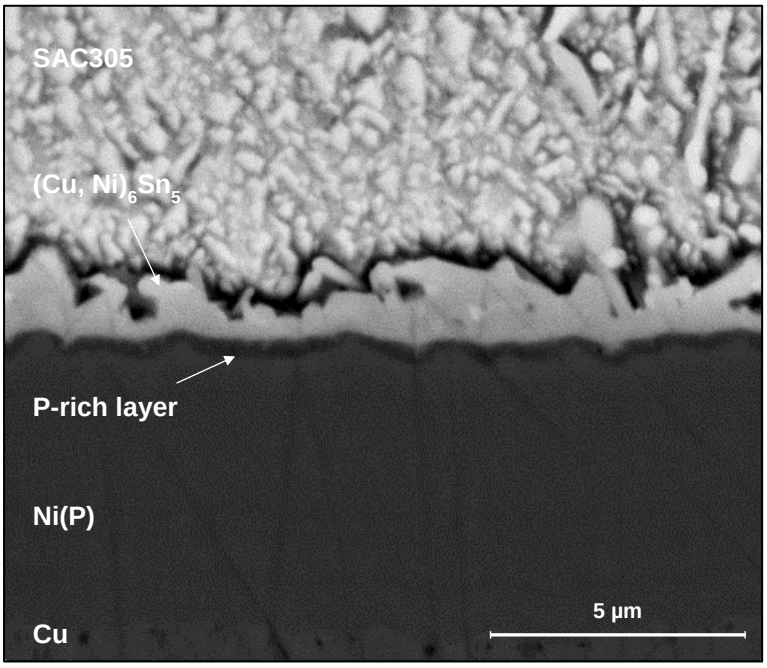
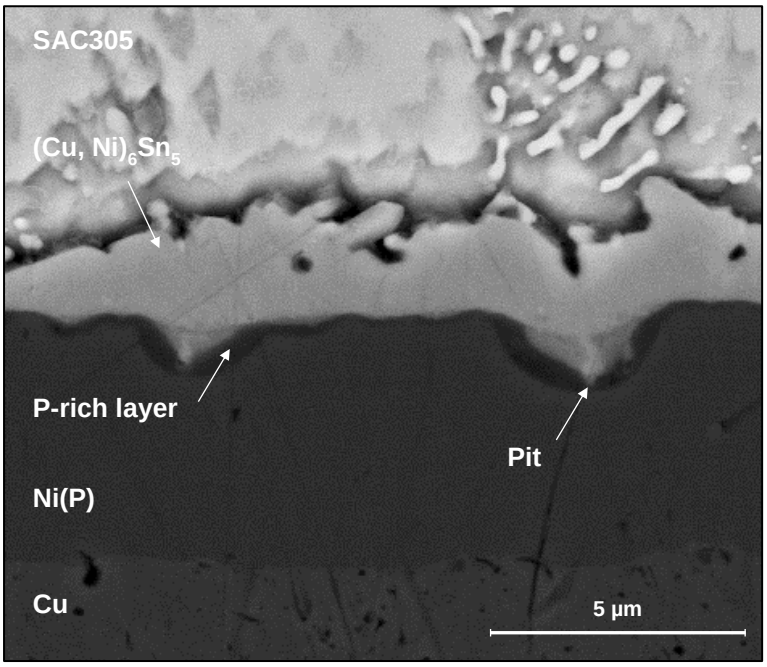


Figure 2.15 SEM images showing the microstructure of bulk solder for the ENIG and ENEPIG samples.

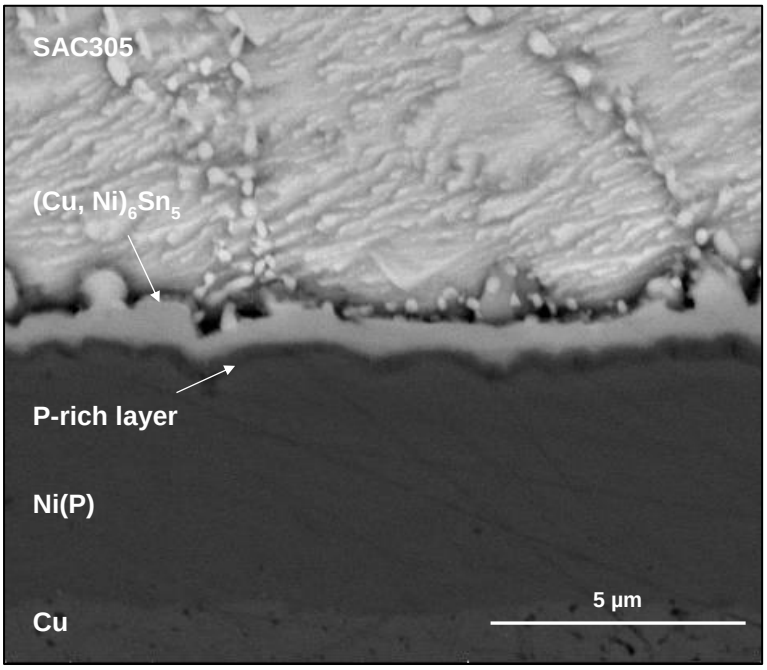


(a) ENIG 0 MTO sample

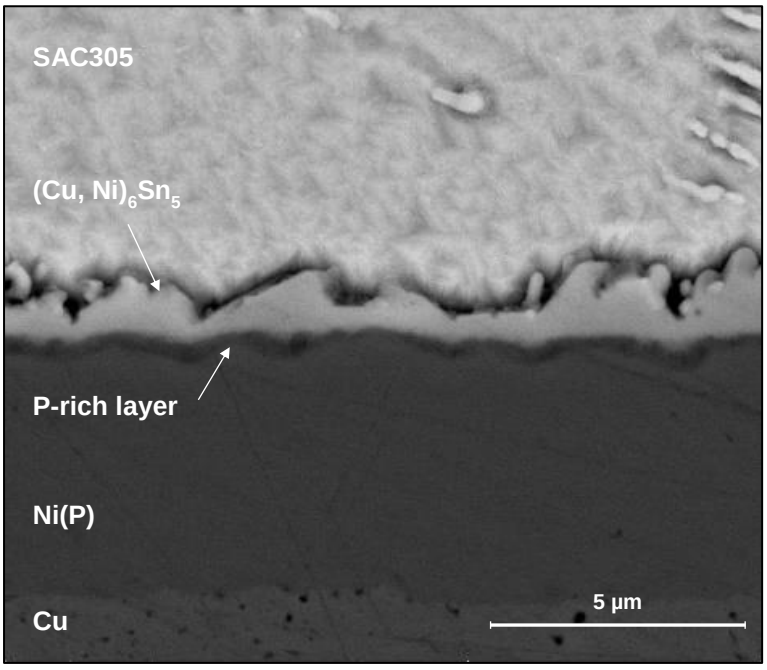


(b) ENIG 3 MTO sample

Figure 2.16 Cross-sectional SEM micrographs of the SAC/ENIG for a bath life of (a) 0 MTO and (b) 3 MTO.



(a) ENEPIG 0 MTO sample



(b) ENEPIG 3 MTO sample

Figure 2.17 **Cross-sectional SEM micrographs of the SAC/ENIG for a bath life of (a) 0 MTO and (b) 3 MTO.**

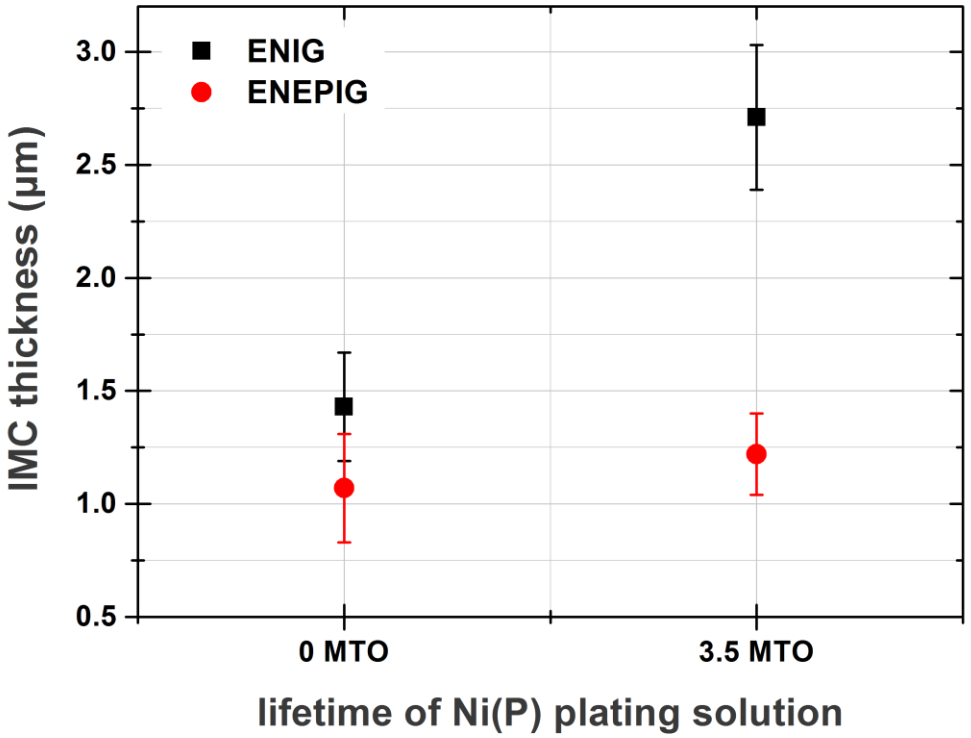
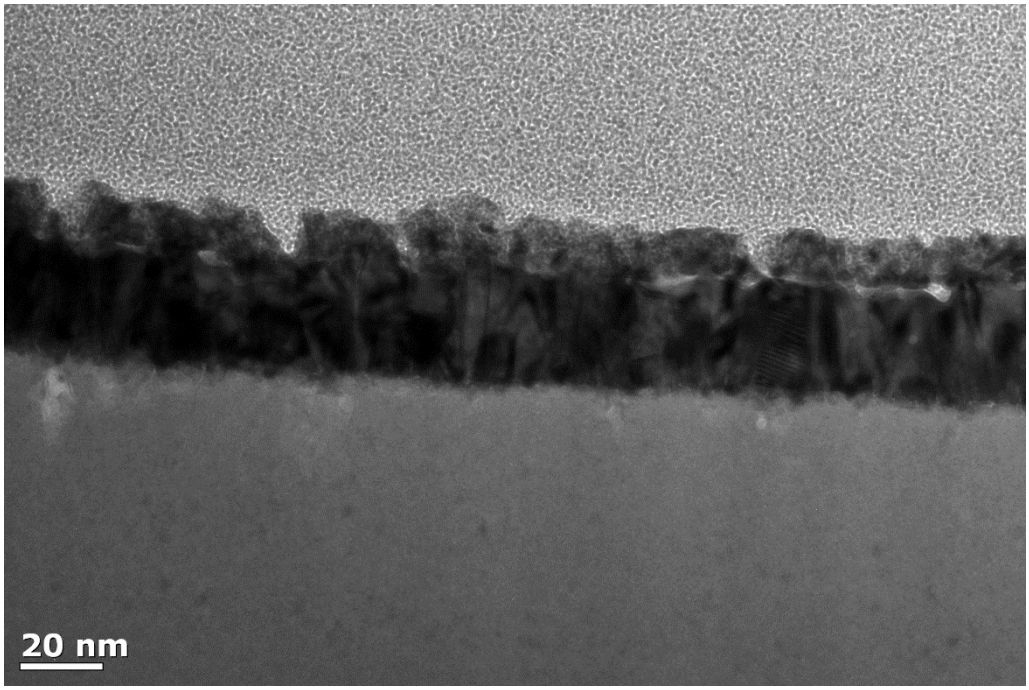
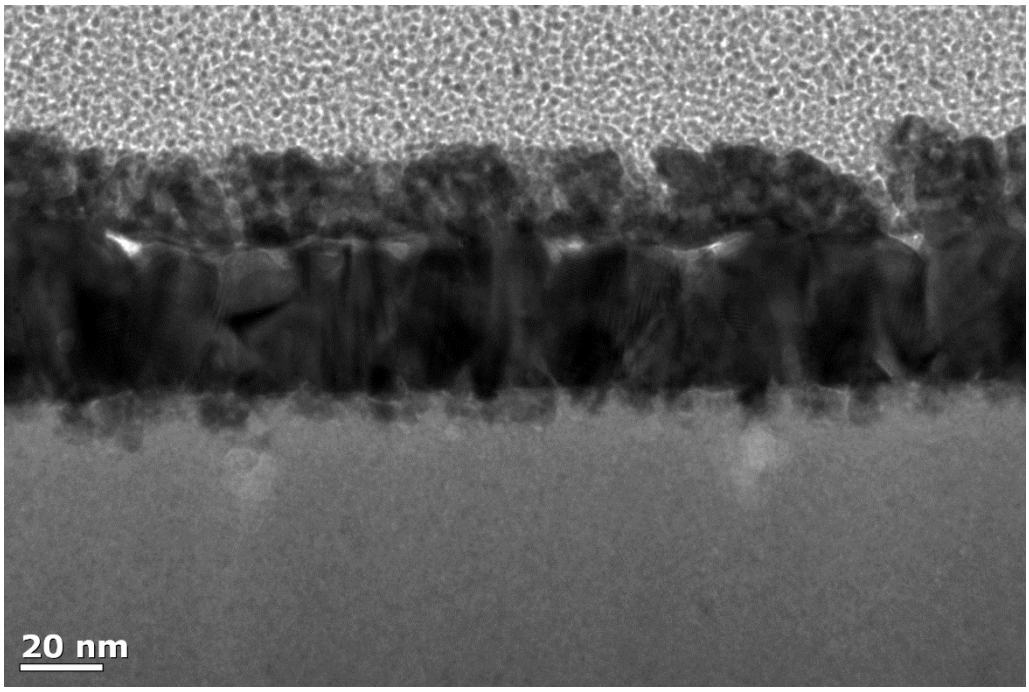


Figure 2.18 Comparison of IMC thickness for ENIG and ENEPIG samples with different plating solution lifetimes.

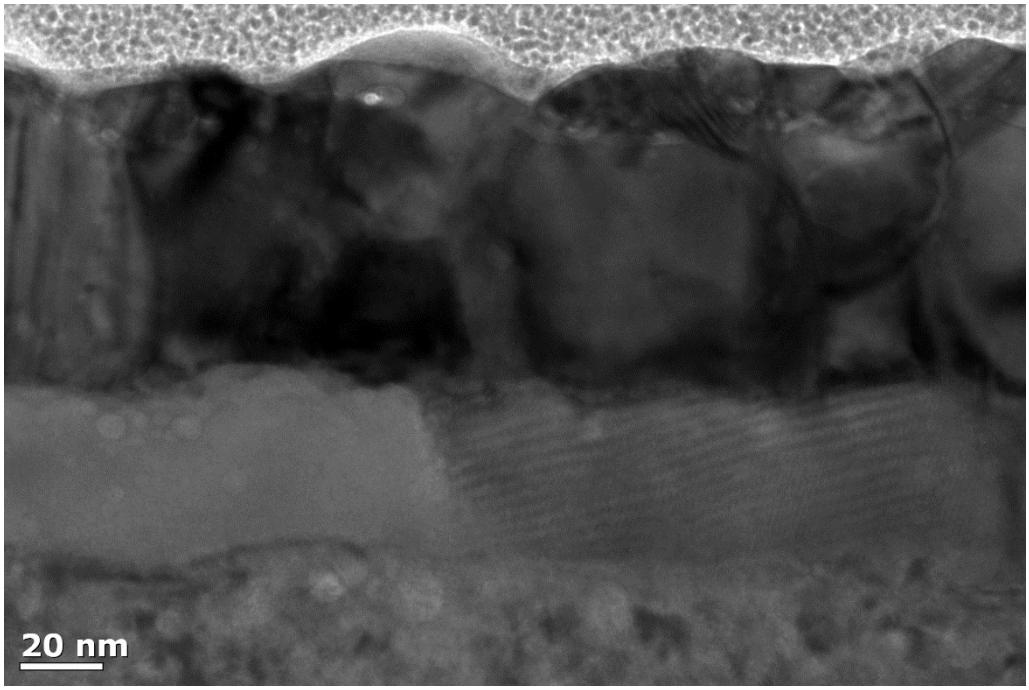


(a) ENIG 0 MTO sample

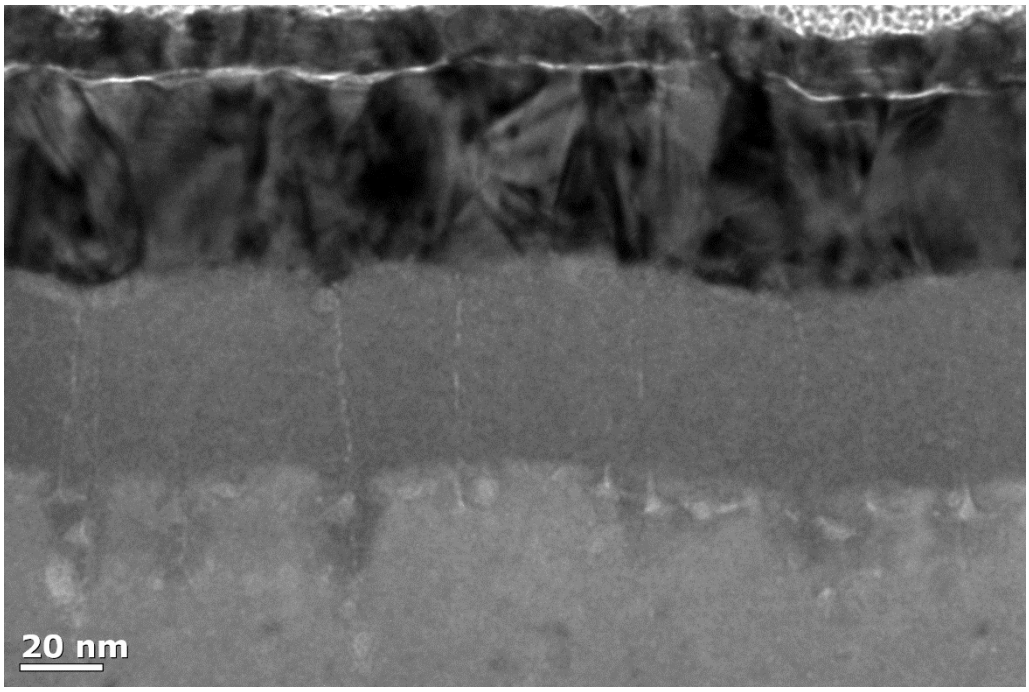


(b) ENIG 3 MTO sample

Figure 2.19 Cross-sectional TEM micrographs of as-deposited ENIG samples. (a) 0 MTO and (b) 3 MTO.

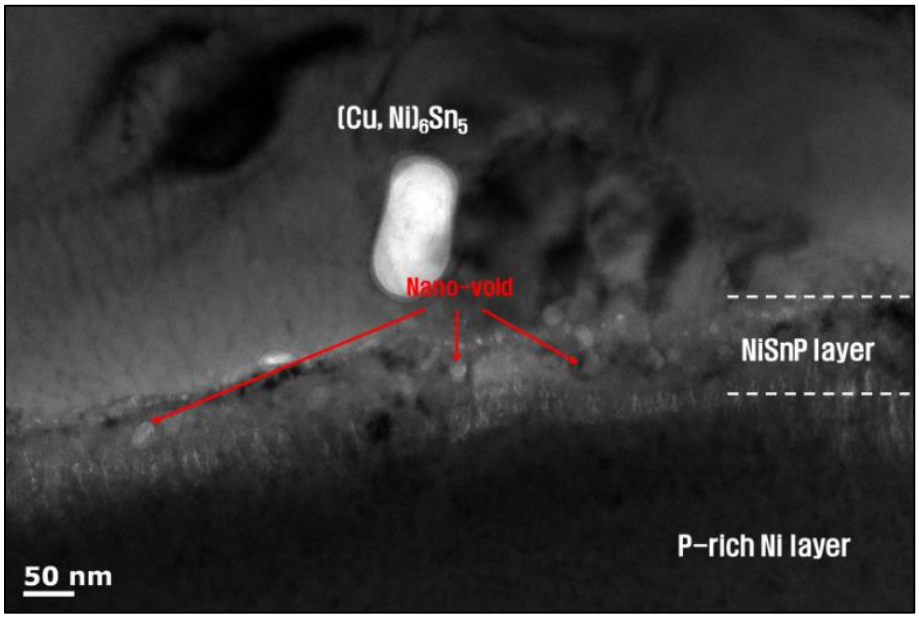


(a) ENEPIG 0 MTO sample

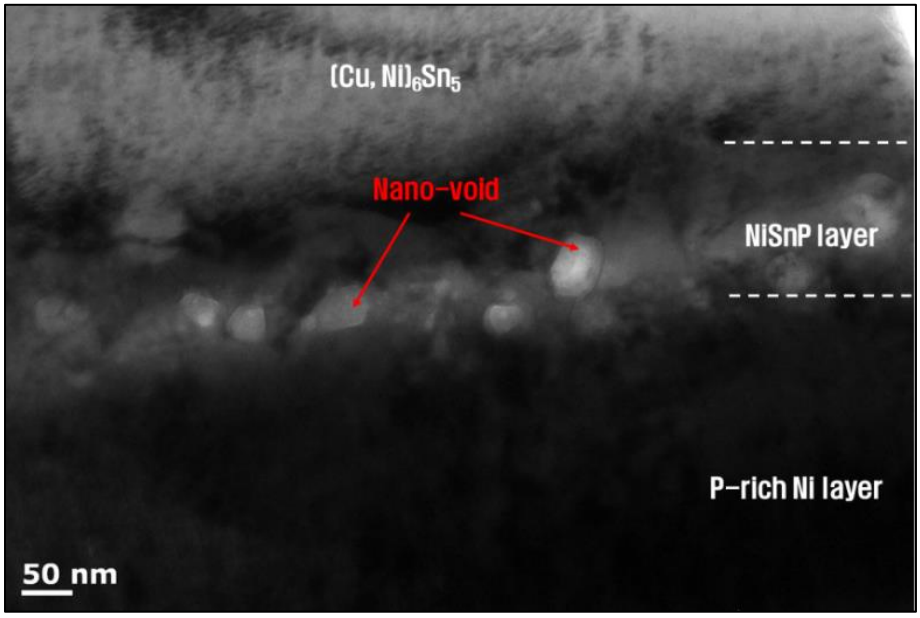


(b) ENEPIG 3 MTO sample

Figure 2.20 Cross-sectional TEM micrographs of as-deposited ENEPIG samples. (a) 0 MTO and (b) 3 MTO.

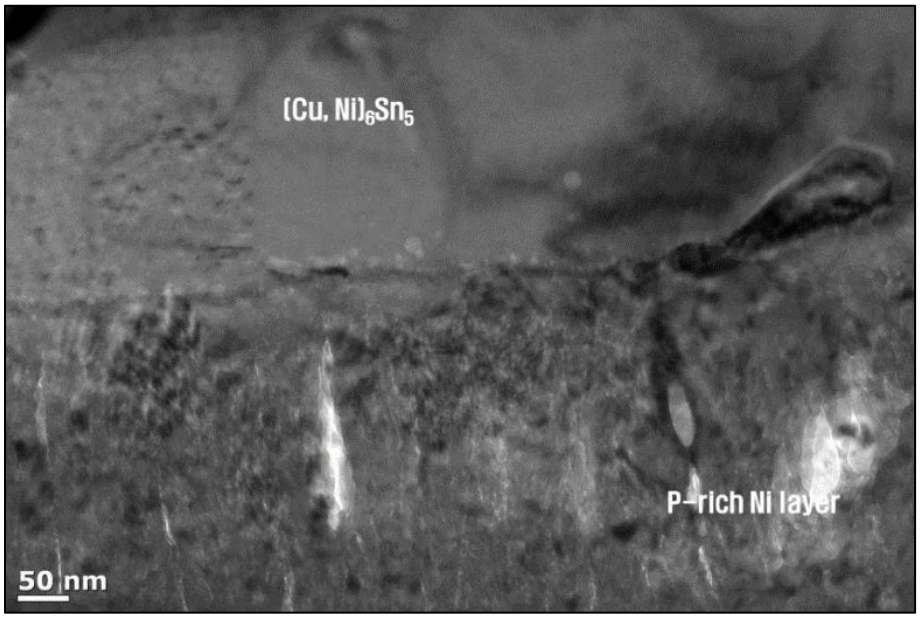


(a) ENIG 0 MTO sample

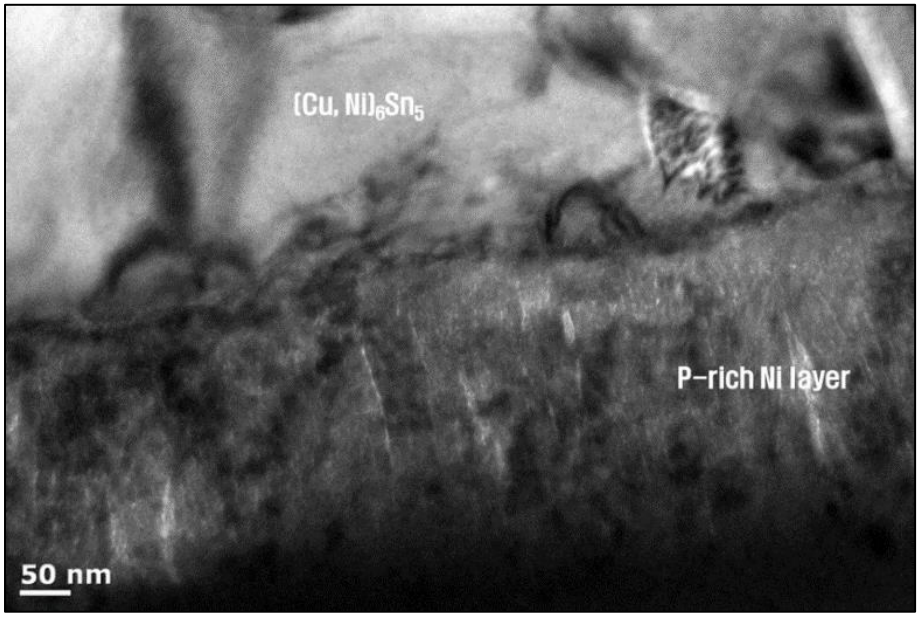


(b) ENIG 3 MTO sample

Figure 2.21 Cross-sectional TEM micrographs of SAC/ENIG samples. (a) 0 MTO and (b) 3 MTO.

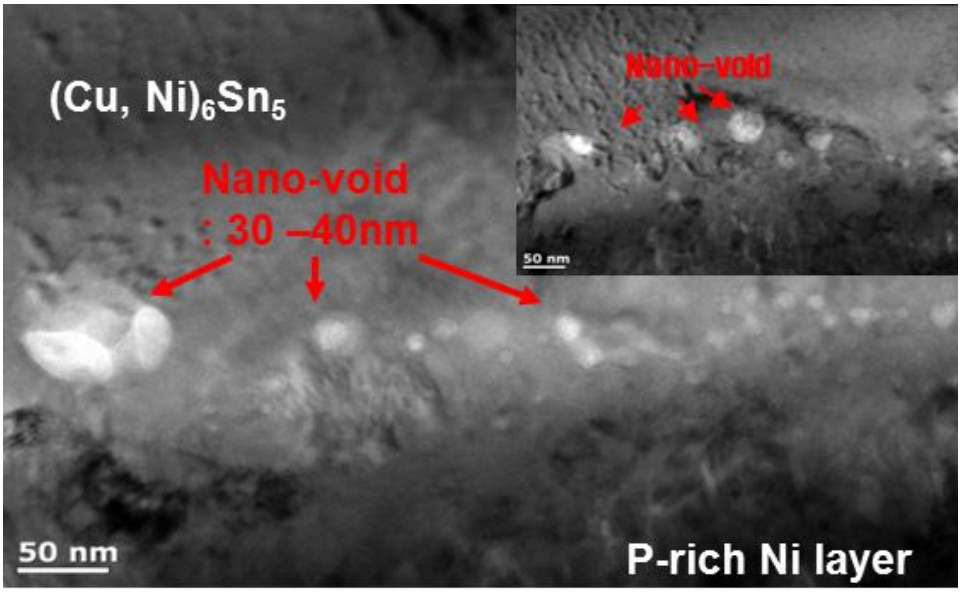


(a) ENEPIG 0 MTO sample

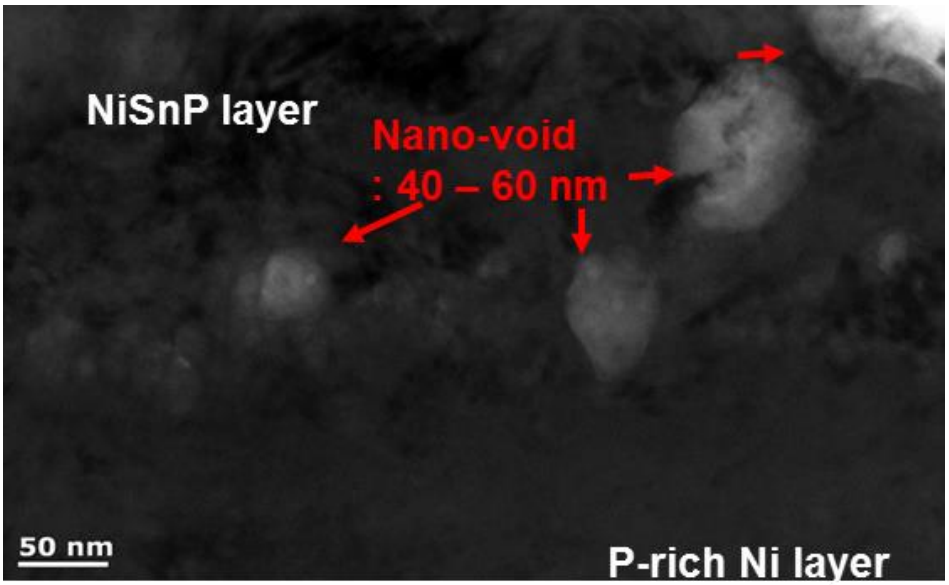


(b) ENEPIG 3 MTO sample

Figure 2.22 Cross-sectional TEM micrographs of SAC/ENEPIG samples. (a) 0 MTO and (b) 3 MTO.

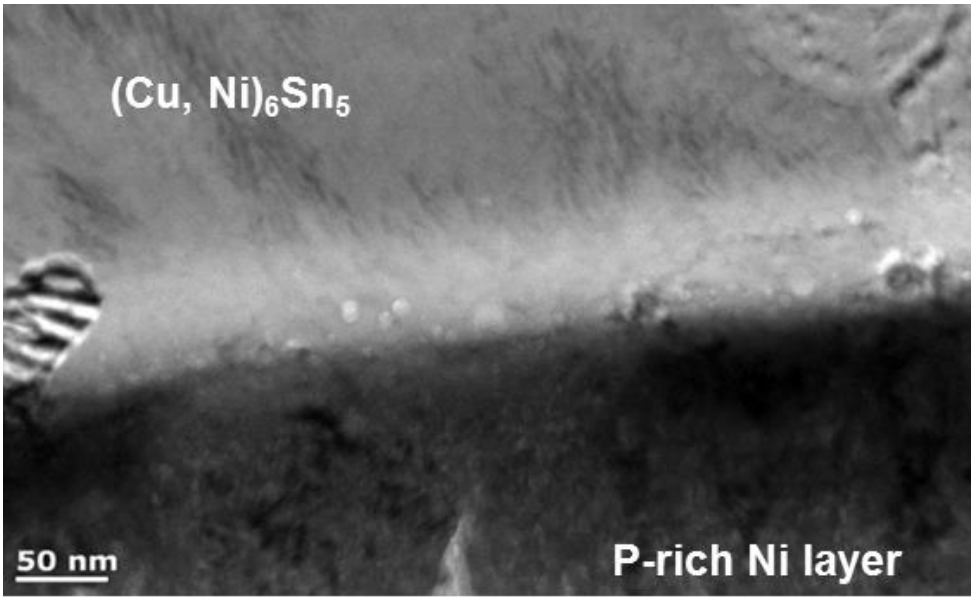


(a) ENIG 0 MTO sample

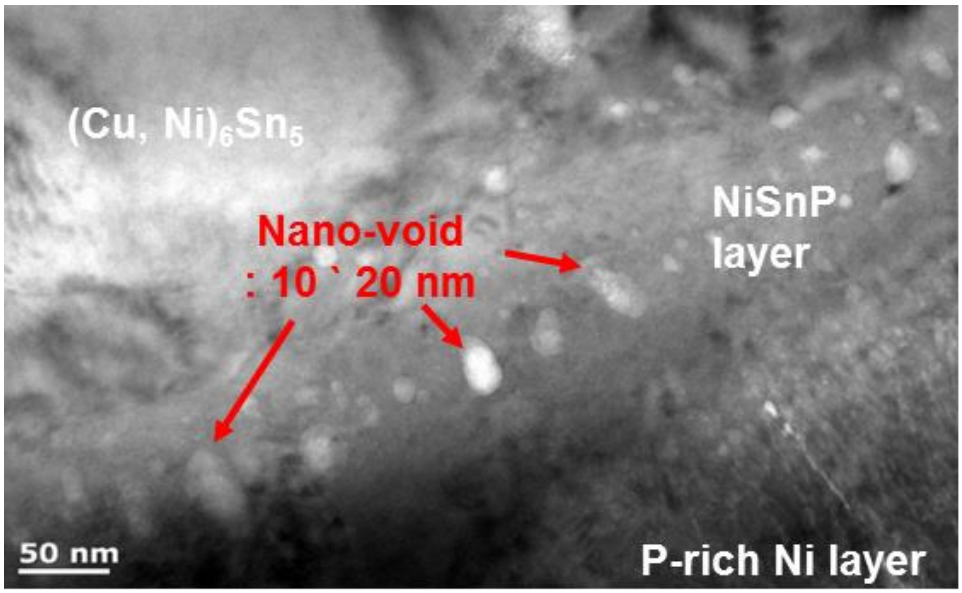


(b) ENIG 3 MTO sample

Figure 2.23 Cross-sectional TEM micrographs of SAC/ENIG after thermal aging at 150 °C for 100 h. (a) 0 MTO and (b) 3 MTO.

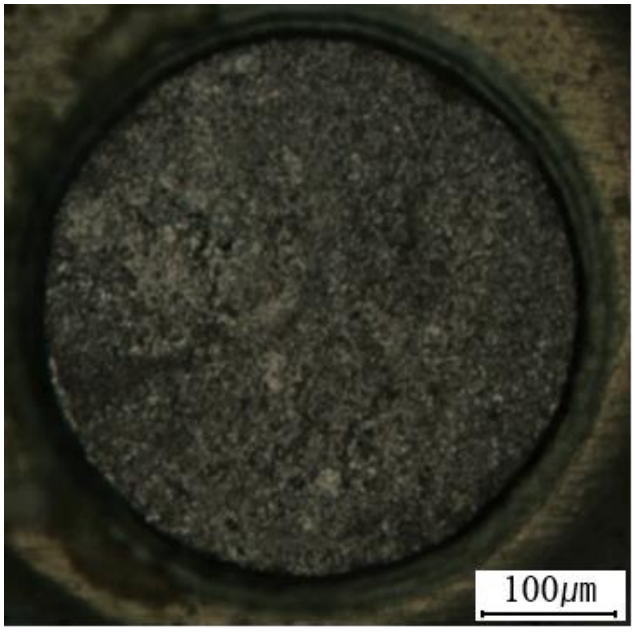


(a) ENEPIG 0 MTO sample

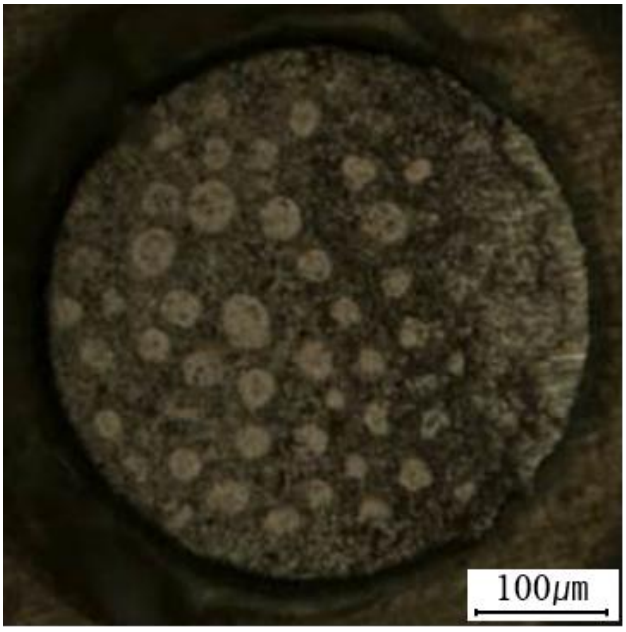


(b) ENEPIG 0 MTO sample

Figure 2.24 Cross-sectional TEM micrographs of SAC/ENEPIG after thermal aging at 150 °C for 100 h. (a) 0 MTO and (b) 3 MTO.

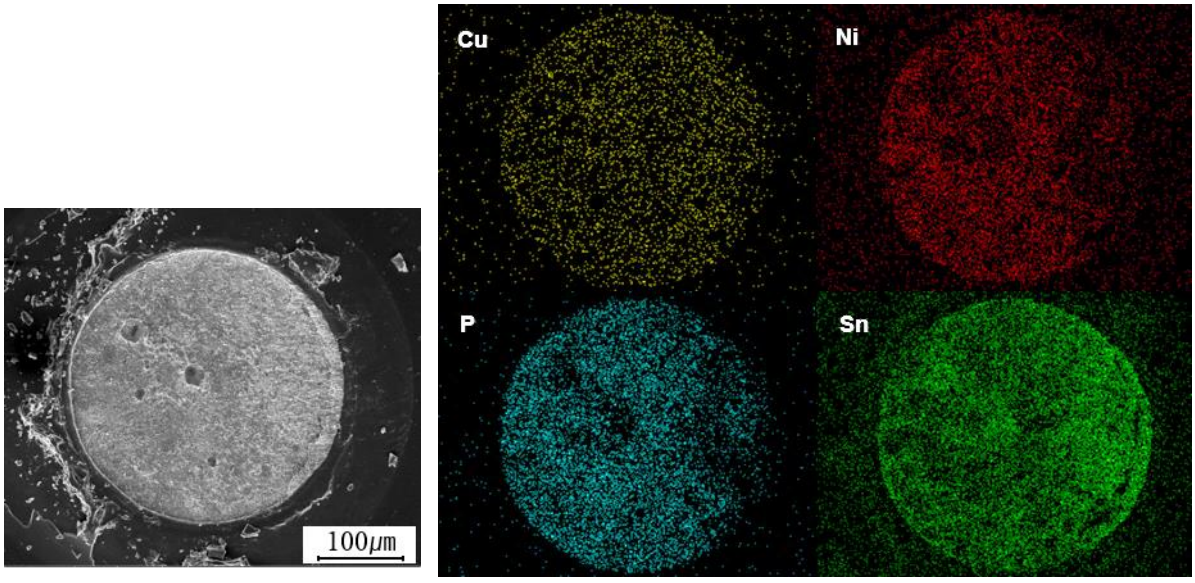


(a)

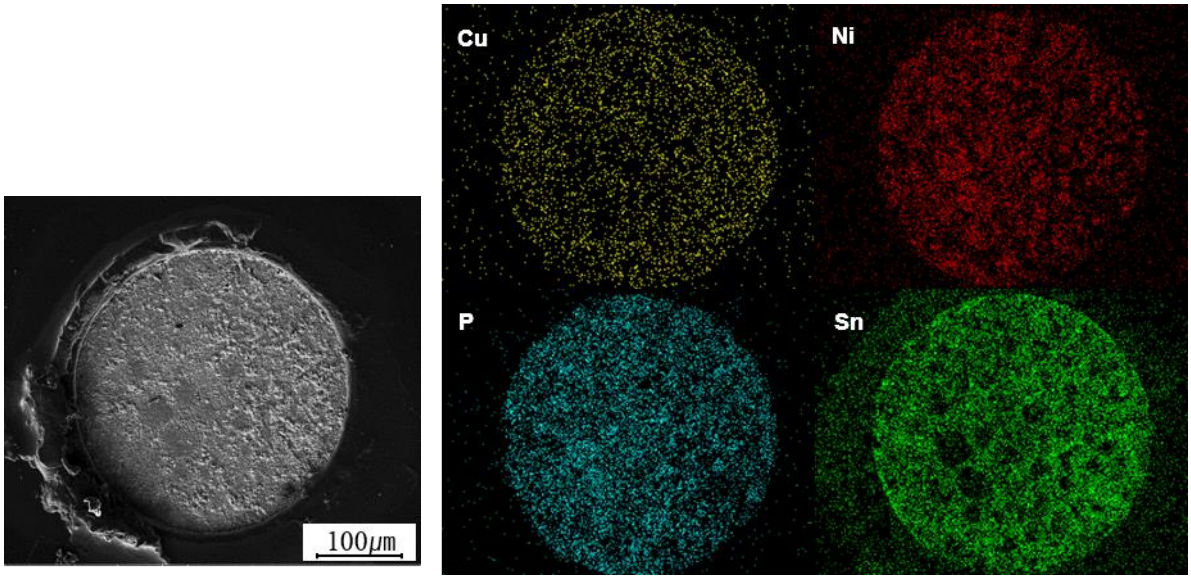


(b)

Figure 2.25 Optical micrographs of the fracture surfaces after HSS testing for (a) 0 MTO and (b) 3 MTO samples.



(a)



(b)

Figure 2.26 SEM images and EDS maps of the fracture surfaces after HSS testing for (a) 0 MTO and (b) 3 MTO samples.

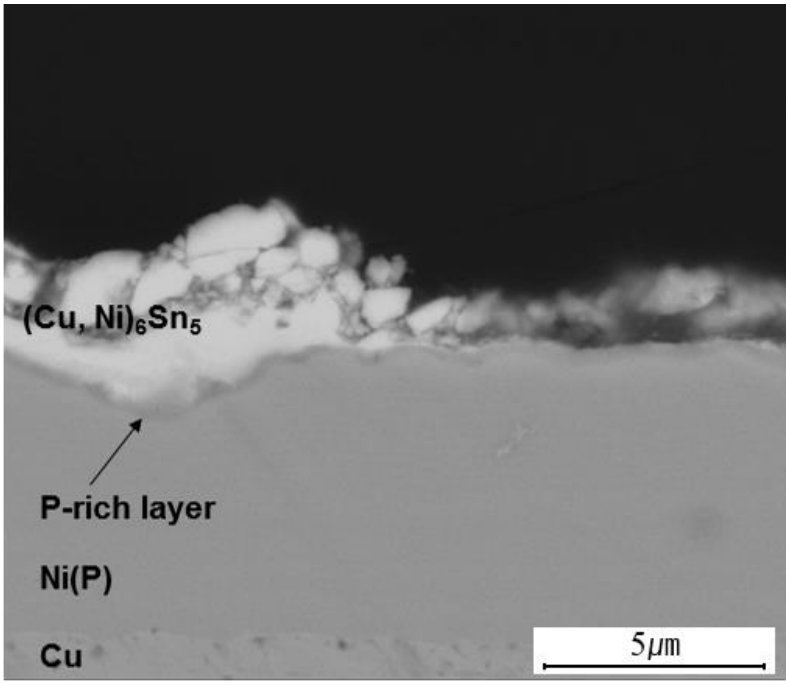


Figure 2.27 Cross-sectional SEM image of a representative section of the fracture surface (away from the circular features).

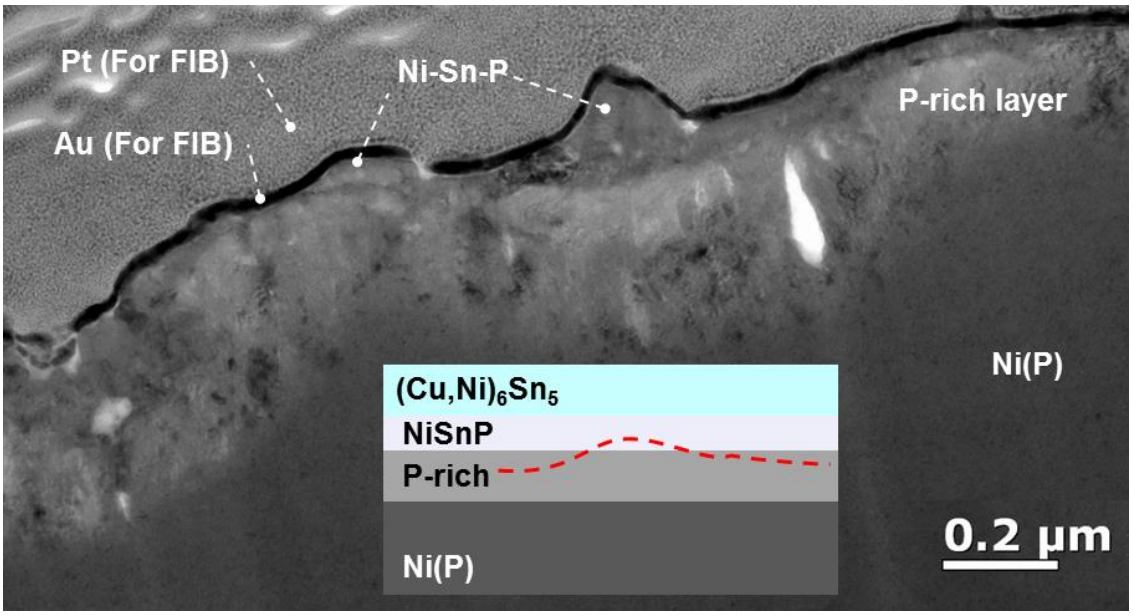
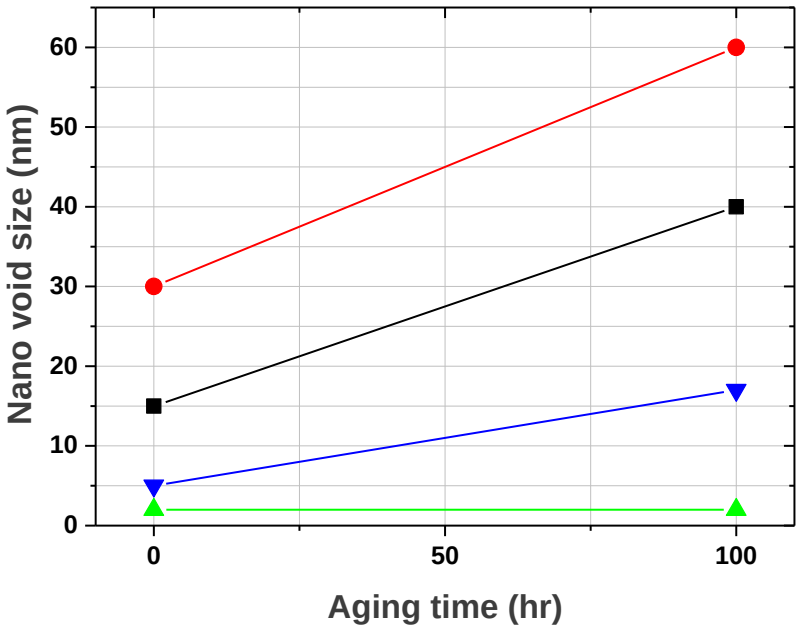
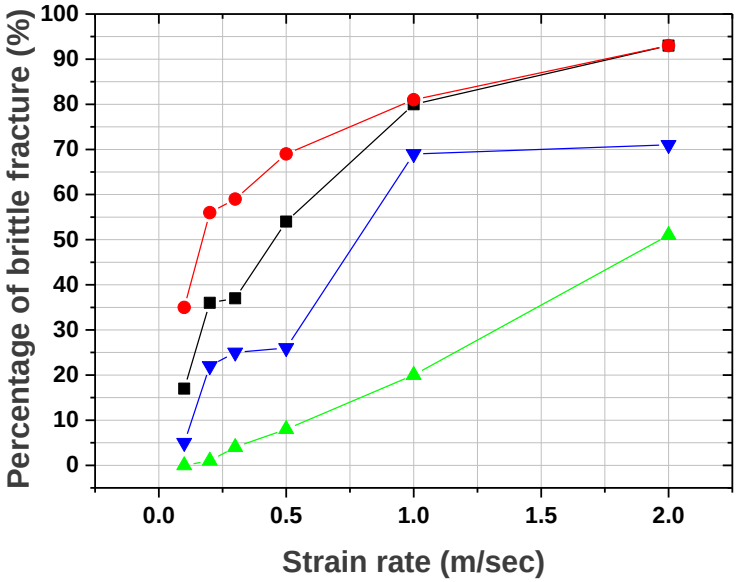


Figure 2.28 Cross-sectional TEM micrograph of a circular feature on the fracture surface shown in Fig. 6.



(a) Nanovoid size with thermal aging



(b) Percentage of brittle fracture with increasing strain rate

Figure 2.29 (a) Nanovoid size as a function of thermal aging time. (b) Percentage of brittle fracture with increasing strain rate.

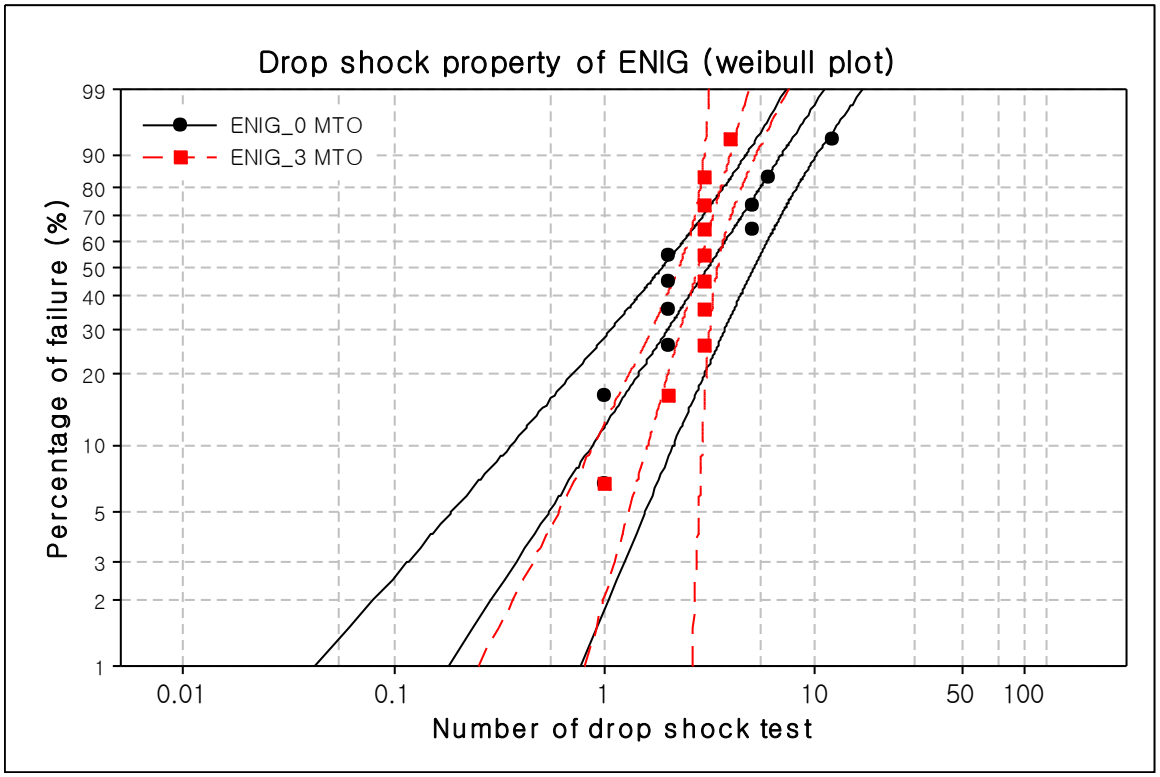


Figure 2.30 Results of drop shock tests of ENIG samples.

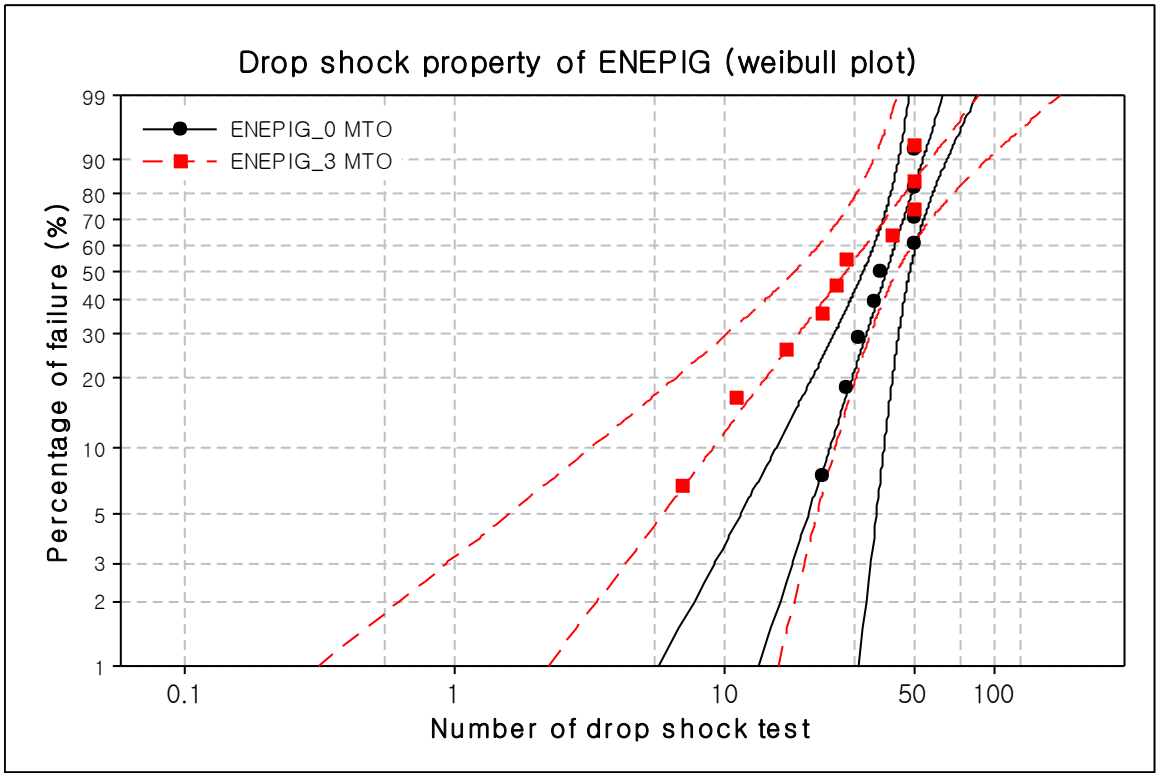


Figure 2.31 Results of drop shock tests of ENEPIG samples.

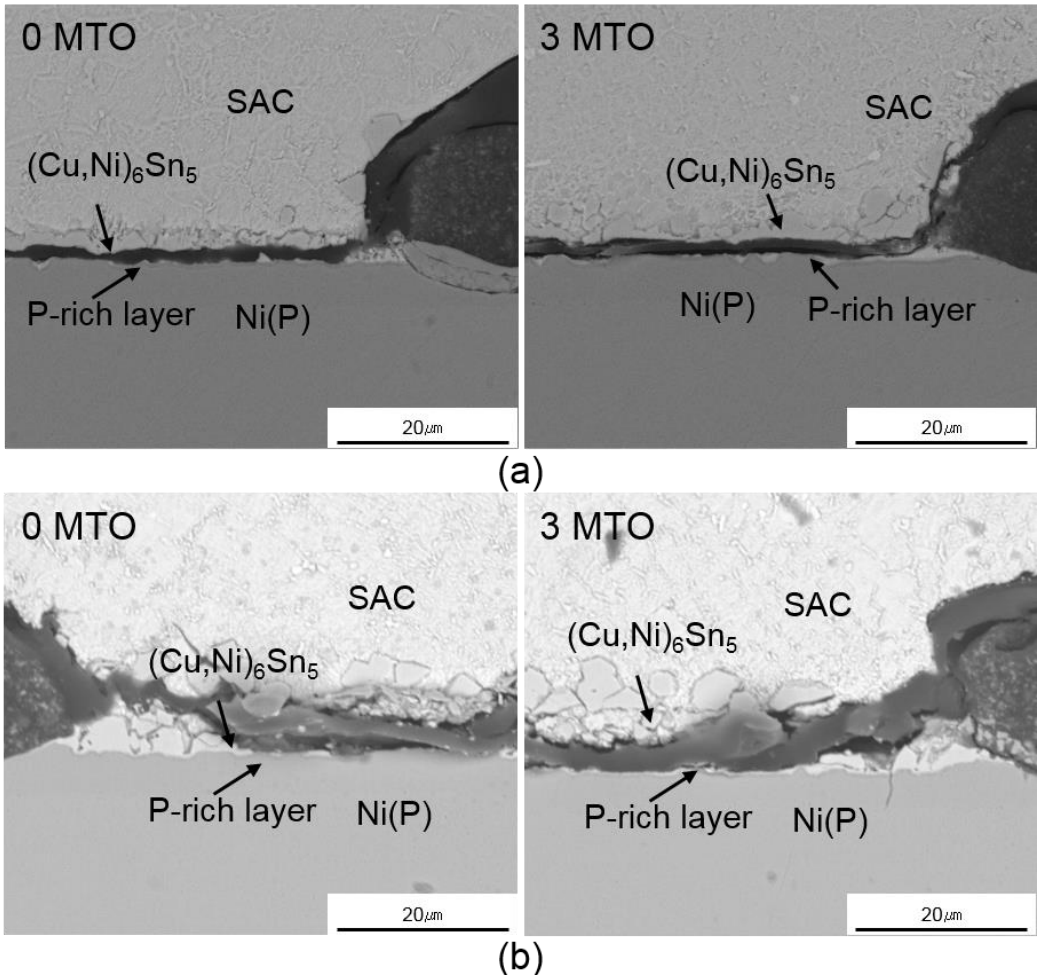


Figure 2.32 Cross-sectional SEM images of the fractures generated after drop shock tests of (a) ENIG and (b) ENEPIG samples under 0 MTO and 3 MTO conditions.

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Chapter 3

Effect of multiple heat-treatments on Sn-Cu interfacial reactions

3.1 Introduction

The soldering process and reliability of the joints between the components highly depend on the quality of the surface finish of a PCB [1-3]. To ensure high quality solder interconnects, the PCB surface finish should have high solderability, low processing cost, low thermal stress, and a long shelf life. In addition, the thickness of the IMC, composition, microstructure, mechanical properties, and reliability of solder

joints are strongly dependent on the surface finish layers [3-5]. Among conventional surface finishes (such as OSP, immersion Sn, immersion Ag, and electroless Ni immersion Au) OSP is the most common as it has a simple processing method, low cost, and adequate solderability, and is also considered to have low environmental impact [6-11]. However, the OSP surface finish has several disadvantages, such as a short shelf life, low corrosion resistance, and poor multiple soldering behavior [5, 12]. In particular, the latter is one of the most important parameters for the high quality assembly of complex electronic modules [13-14]. For example, double-sided PCBs are subjected to at least two reflow processes. During this procedure, the bottom side of the PCB is exposed to high temperature under an air atmosphere. If wave soldering and rework processes are used for the assembly of the electronic module, at least four heat treatments are required. Therefore, the surface finishes that are not soldered at each step of the process can be degraded by the oxidizing environment during heating. For these reasons, a PCB surface finish with high stability during multiple soldering steps is essential to ensure the reliability of solder joints. Figure 3.1 shows a schematic of a multiple heat treatment process.

The plasma surface finish is a thin and protective coating that is a potential replacement for conventional surface finishes as it has several advantages. The shelf life of a plasma-finished PCB is over one year, and the corrosion resistance of the plasma finish layer is generally higher than those of conventional surface finishes. The plasma surface finish is more environmentally friendly than current wet chemical

processes, as it eliminates the use of water, precious and semi-precious metals including Au, Pd, and Ni, and is a safer process for operators [15]. Nevertheless, detailed studies regarding the reliability of the plasma finish and comparisons of the plasma and OSP finishes remain insufficient. Therefore, in this study, we investigate the effects of multiple heat treatments on the solderability (or wettability) of plasma- and OSP-finished Cu coupons using a wetting balance test with Sn-3.0Ag-0.5Cu (SAC305) solder. In addition, we formed SAC305 solder balls on the two different PCB substrates and investigated the interfacial reactions and mechanical shear properties of solder joints formed during multiple reflow processes. The relationships between solderability, interfacial reactions, and shear force applied to the solder joints are discussed.

3.2 Experimental

3.2.1 PCB design and surface finishes

The PCBs used in this study were SMD FR-4-type. A schematic of the test PCBs is shown in Figure 3.2. The diameter of the Cu pads on the PCB was 400 μm, and the thicknesses of the Cu pads and PSR were 10 and 15 μm, respectively. For the plasma surface finish, an organic thin film was deposited onto the Cu pad of the test PCB using PE-CVD (JESAGI Hankook Corp., Korea). Figure 3.3 shows a schematic of the plasma surface finish process. The precursor used in the plasma coating process was

fluorocarbon. Conventional OSP-finished PCBs were also used in this study as a reference for comparing the quality of the plasma surface finish. The microstructures of the plasma- and OSP-finished layers were analyzed using TEM (JEOL JEM 4010).

3.2.2 Wetting force and time

To understand the effects of the plasma and OSP surface finishes on the solder wetting properties, Cu wetting test coupons with dimensions of 1.0 × 3.0 × 0.3 mm^3 were prepared. The solderability of the two surface finishes was measured by a wetting balance tester (MALCOM, SP2). A SAC305 solder was used in the wetting test. The wetting temperature was 250 °C and the sample immersion speed, depth, and time were 5 mm/s, 5 mm, and 10 s, respectively. Ten measurements were made at each test condition in order to improve the statistical confidence level of the results. The maximum wetting force (F_{max}) and zero-cross time (T_0), were used to assess the wetting behavior of the surface finishes. To simulate the effect of multiple reflow processes (i.e., multiple heat treatments) on the solderability of the two surface finishes, the test coupons were heat treated in a reflow oven (Heller, 1890UL) under typical SAC305 reflow conditions (as described by the heating profile shown in Figure 3.4). The peak temperature of the reflow profile was approximately 242 ºC. The wetting tests were performed after the samples had experienced either zero, two, or four heat treatments. In the solder spreading test, SAC305 solder paste was screen-printed on the OSP- and plasma-finished PCBs, and then the PCBs were reflowed. The

diameters of the printed solder paste and Cu pads on the PCB were 300 and 400 μm, respectively. OM was used to observe the surfaces of the PCBs after testing. The spreading areas were characterized using image analysis software and the spreading ratios were calculated as the increase in area as a percentage.

3.2.3 Soldering and multiple heat treatments

Soldering was performed in order to evaluate the interfacial reactions and mechanical strength of the joints between the SAC305 solder alloy and the two different surface finishes. Firstly, SAC305 solder paste (Senju, M705-SHF type 5) was printed on the test PCB (Figure 3.2) using a stencil mask. Secondly, SAC305 solder balls (Duksan Hi-Metal, Korea) with a diameter of 450 μm were placed on the printed SAC305 solder paste. Then, the test PCB was heated in a reflow oven (Heller, 1890UL) using the temperature profile shown in Figure 3.4. To investigate the multiple solderability of the surface finishes, the test PCBs were heat treated various times in the reflow oven under the same conditions. After multiple heat treatments, solder paste and balls were applied to the test PCBs and reflowed to form solder joints. The multiple reflows were performed up to five times. For example, samples heat treated three times were subjected to two heat treatments without soldering, and finally a third reflow process with the solder alloy. After the reflow processes, cross-sectional samples were prepared for characterization of the interface. Common metallographic practices, grinding and polishing, were used to prepare the samples. The

microstructures and chemical compositions were analyzed using FE-SEM (FEI Inspect F) and TEM equipped with EDS.

3.2.4 Mechanical properties

Ball shear tests were performed on the reflowed samples using a shear tester (Dage 4000) with a shear tool height of 50 μm and a shear speed of 300 μm/s. On the other hand, the high-speed shear strength and brittle fracture behavior were evaluated with a high-speed shear tester (Dage, 4000HS). The distance between the shear tool and the top of the PSR on the test PCB was 50 μm. The shear speed (strain rate) of the HSS test was varied from 0.1 to 2.0 m/s. The average shear strength of twenty-five solder balls, after the minimum and maximum outlier values had been removed, was recorded. After the ball shear testing, the fracture surfaces were investigated thoroughly using SEM and EDS.

3.3 Results and discussion

3.3.1 Corrosion resistance with multiple heat treatments

To evaluate the corrosion resistance of the solder joints, a salt spray test was performed and the samples characterized after 0, 6, and 15 h. Figure 3.5 (a) shows optical microscopy images of the pads for OSP and plasma finishes at the initial conditions (before heat treatment). Figure 3.5(b) shows that the corrosion had

progressed after 6 h, where the surface of the plasma-finished pad showed low corrosion. Figure 3.5(c) shows the corrosion after 15 h, where the pad of the OSP-finished sample was corroded more than the plasma-finished one by the salt spray test.

3.3.2 HSS strength and brittle fracture behavior with multiple heat treatment

The shear strength of the solder joints on OSP- and plasma-finished samples were evaluated with high-speed shear testing by varying the strain rate (from 0.1 to 2 m/s), as shown in Figure 3.6. For the solder joint on the OSP finish, the shear strength was 6.9 kgf/mm^2 at a strain rate of 0.1 m/s and increased to 8.1 kgf/mm^2 as the strain rate increased to 2.0 m/s. The shear strength of the solder joint on the plasma-finished sample was 6.9 kgf/mm^2 at 0.1 m/s and increased to 7.6 kgf/mm^2 as the strain rate increased to 2.0 m/s (i.e., similar values to that of the OSP sample).

The fracture mode was determined by observing the fracture surface of twenty-five samples. In this study, the brittle fracture rate was defined as shown in Equation (1) of Chapter 2. Figure 3.7 shows the brittle fracture rate after single reflow. For the OSP- and plasma-finished samples, the brittle fracture rates were 30.6% and 38.9%, respectively. The brittle fracture rate of the plasma finish was similar to that of the OSP finish after single reflow. Figure 3.8 shows SEM micrographs of the cross-sections of the OSP- and plasma-finished samples after the single reflow. The thicknesses of the IMC layers of the OSP- and plasma-finished samples were 3.2 μm and 2.9 μm, respectively. EDS analyses revealed that the IMC layers were Cu_6Sn_5 for

both samples. To investigate the effects of multiple reflow, the bare PCB with the OSP and plasma finishes were reflowed four times and then solder balls were attached and the sample reflowed (a total of five reflows). The solder joint properties were also examined using the HSS test. The shear strengths as a function of strain rate are shown in Figure 3.9. The shear strengths for both OSP- and plasma-finished samples were similar after multiple reflows, 36.1% and 44.4%, respectively, as shown in Figure 3.10. The plasma-finished samples showed lower brittle fracture than the OSP samples. Figure 3.11 shows cross-sectional SEM micrographs of the IMC layers, where the thicknesses were 4.2 μm and 5.0 μm for the plasma- and OSP-finished samples, respectively.

Based on Equation (1), the total brittle fracture rate of the OSP finish was lower than that of the plasma finish. In addition, the percentage of brittle fracture for the OSP and plasma finishes tended to increase with multiple reflow [16]. Under single reflow conditions, the 100% brittle fracture rate of the plasma sample was higher than that of the OSP sample. However, the brittle fracture rate of the plasma finish after the fifth reflow was lower than that of the OSP finish. These trends demonstrate that the plasma finish has advantages during multiple reflows compared to the standard OSP finish.

3.3.3 Evaluation of wettability

Excellent wetting properties are very important for solder alloys to ensure a reliable connection between the solder and the components. The solderability of the SAC305

alloy with different surface finishes was measured using a wetting balance test. This alloy system is technically important because it is generally recognized as the first choice for a Pb-free solder [4]. Figures 3.12 and 3.13 show the wetting force and zero-cross time as a function of the number of heat treatments for the different surface finishes. For each surface finish, F_{max} and T_0 were calculated by averaging ten sets of wetting data (where the error bars represent the standard deviation of these data sets). In the case of the plasma surface finish, the wetting force did not change with further heat treatments. On the other hand, the wetting force of the OSP surface finish rapidly decreased with additional heat treatments. The zero-cross times for both surface finishes increased with increasing number of heat treatments, however, those for the OSP finish increased more rapidly than those of the plasma finish. The plasma-finished samples had higher wetting forces and shorter zero-cross times than the OSP surface finish.

Figure 3.14 shows OM images of the test coupons after the wetting tests, where 0, 2, and 4 refer to the number of heat treatment cycles before wetting. Interesting results were observed for the OSP samples. In the case of the sample heat treated four times, the wetting reaction did not occur, as shown in Figure 3.14 (a). On the other hand, the wetting reactions occurred for the plasma samples irrespective of the number of heat treatments, as shown in Figure 3.14 (b). These results are consistent with the wetting test results shown in Figures 3.12 and 3.13. These results indicate that the OSP surface finish degraded after multiple reflows. Similar results are reported in the literature [15,

17]. It has been reported that the solderability of the OSP finish reduced after two reflow cycles. On the other hand, we have demonstrated that the solderability of plasma-finished PCBs was still high after multiple reflow cycles, making it suitable for the fabrication of complex electronic devices.

Figure 3.15 shows OM images of the spreading test samples for 1, 3, and 5 reflow cycles, along with a schematic diagram illustrating the reflow process for both the OSP- and plasma-finished PCBs. The percentages refer to the spreading ratios. In the case of the plasma-finished sample, the initial spread ratio was around 120%, which dropped slightly to around 115% after reflowing. The spread ratio of the initial OSP-finished sample was similar to that of the plasma-finished sample, but decreased to around 108% after three reflow cycles and further to 77% after five reflows.

3.3.4 Microstructural observations

The morphologies of the OSP- and plasma-finished PCB substrates were analyzed using TEM. Figure 3.16 shows cross-sectional TEM images of the OSP- and plasma-surface finished Cu substrates. The Cu substrates are the bulk regions of the right hand sides of the images and the white layers are the surface coatings. The Au, Pt, and C layers indicated on the images were deposited as protection layers for TEM sample preparation. In addition, the thicknesses of the OSP- and plasma-coated layers are indicated by red arrows in Figure 3.16 (a). The OSP layer was irregular and the thickness ranged from 5 to 70 nm. On the other hand, the plasma-coated layer had a

uniform thickness around 20 nm. The plasma coating process involved plasma polymerization, the formation of polymeric materials under the influence of plasma [18], which allows the deposition of continuous organic films from the gas phase on a metal substrate. The plasma process creates a dense and highly cross-linked polymer coating on metal substrates.

In order to evaluate the effect of the surface finish on the soldering and interfacial reactions, a reflow process was conducted using the SAC305 solder. Figure 3.17 shows cross-sectional TEM images of the OSP and plasma samples after soldering. The plasma surface finish was applied across the whole of the PCB and was removed by the soldering process only in the areas where flux and solder were applied. In this study, the plasma-coated layer was removed by the combined action of the flux and the high reflow temperature. As a result, the Cu layer beneath the plasma-coated layer was then in direct contact with the molten solder, resulting in the formation of Cu-Sn IMCs at the interface. The interfacial reactions and IMC formation in this solder system are well known and have been reported in previous studies [19-20]. During the reflow process, the SAC305 solder was in the molten state and typical scallop-shaped Cu_6Sn_5 IMCs formed at the interfaces. In addition, thin Cu_3Sn layers were observed between the Cu_6Sn_5 IMC and the Cu substrate. Most Sn-based solder alloys form these two reaction layers (Cu_6Sn_5 and Cu_3Sn) at the interface between the solder and Cu substrate. Consequently, similar interfacial structures were observed at the interfaces of the solder joints for both samples.

3.3.5 Effect of multiple heat treatment on shear force and soldering area

Figure 3.18 shows cross-sectional SEM images of the multiple-reflow SAC305 solder joints with the two different surface finishes. From the TEM results shown in Figure 3.17, we confirmed that Cu_6Sn_5 and Cu_3Sn formed as reaction products at the interfaces. A close examination of the cross-sectional SEM images revealed that the thicknesses of the interfacial IMCs for the two surface finishes were similar (as shown in Figure 3.19).

Figure 3.20 shows the results of the ball shear tests performed to evaluate the effect of the surface finish and interfacial reactions on the mechanical reliability of the SAC305 solder joints as a function of multiple heat treatments. In the case of the plasma coating, the shear force remained nearly constant at approximately 5.2 kgf despite multiple reflows. On the other hand, the shear force decreased rapidly after five reflow processes for the OSP substrate. The shear force for the single reflow OSP joint was approximately 4.7 kgf, which decreased slightly after three reflows, and finally decreased dramatically to a value of 3.2 kgf after five reflow cycles. Overall, the shear force for the plasma substrate was consistently higher than that for the OSP substrate. As the shear force is related to the force required to fracture the solder joint, a high value indicates a stronger joint.

Figure 3.21 shows cross-sectional SEM images of the entire SAC305 solder joints areas with different surface finishes and reflow cycles. In the case of the plasma

substrate, the SAC305 solder alloy covered all of the Cu pad area (indicated by the white dashed line), even after multiple reflows. On the other hand, for the OSP substrate, the SAC305 solder did not perfectly cover (i.e., react with) the Cu pads. This was due to the deterioration of the OSP surface finish after multiple heat treatments. The un-reacted parts of the Cu are indicated by the white arrows in Figure 3.21 (c) and (e). These results are consistent with those from the wetting tests shown in Figures 3.12–3.14.

Another interesting observation of this study was that voids formed at the OSP/solder interfaces after multiple heat treatments (although not at the plasma finished interface). These voids are indicated by the black arrows in Figure 3.21. Yoon et al. studied the relationship between the interfacial reactions, void formation, and mechanical reliability of SAC305/OSP-finished Cu joints [20]. In that study, several voids formed at the interface of the OSP-finished Cu joint subjected to a temperature-humidity test. The voids were caused by the oxidation of the OSP-finished Cu substrate during testing. Shear tests were also performed and it was found that the mechanical reliability of the solder joint was degraded by these voids at the interface. It is interesting to note that the formation of the Cu_6Sn_5 IMC in the SAC305 solder matrix was significantly retarded for the SAC305/plasma finish joint compared to the SAC305/OSP finish system where several relatively large Cu_6Sn_5 IMC features were observed in the OSP joints, as shown in Figure 3.21 (a), (c), and (e).

The fracture surfaces after ball shear testing were examined using SEM in order to

verify the variations in the shear force. Figure 3.22 shows the fracture surfaces of the two types of SAC305 solder joints for 1, 3, and 5 reflow cycles. The direction of the shear is indicated by the black arrow in Figure 3.22. From these fracture surfaces we can conclude that the failure mode was consistently related to the bulk for the plasma-finished substrate, regardless of the number of reflow cycles. Similarly, in the case of the OSP-finished substrate, bulk solder failures were observed for the samples subjected to one and three reflow cycles. However, a significantly different fracture surface was observed for the SAC305/OSP joint after five reflow cycles, where there were many voids observed at the interface. In addition, the shearing area decreased significantly for the OSP joint reflowed five times. In Figure 3.22(c), the area of the Cu pad is indicated by a white dashed circle and the area of the un-reacted Cu is shown by the white arrow. The results shown in Figure 3.22 are consistent with those of the interfacial microstructures from the cross-sectional SEM micrographs shown in Figure 3.21. In conclusion, the reduced bonding area and void formation resulted in an abrupt decrease in the shear force in the OSP joint after multiple heat treatments.

3.3.6 Cu oxidation resistance of plasma surface finish

It was observed that the plasma surface finish did not exhibit any change in the bond strength and soldering area after undergoing multiple heat treatments. In order to determine the reason for this, Fourier transform infrared spectroscopy (FTIR, Georgia Tech.) was carried out. Figure 3.23 shows the results of the FTIR analysis for the as-

deposited plasma surface finish. This film was found to be a CF_2 layer, identified by its characteristic peak at a wavenumber of 1200 cm^{-1}. In addition, a carbonyl component at 1736 cm^{-1} and a CH_x component at 2800 cm^{-1} were detected. Additionally, a cuprous oxide component was detected at a wavenumber of 640 cm^{-1} from the plasma surface finish following surface treatment [21]. This component was found to be created when the CF_2 layer was exposed to air before deposition in the surface treatment chamber. This issue regarding the formation of cuprous oxide would need to be addressed by adding a cleaning process before employing vacuum for plasma surface treatment.

According to Ramirez, et al., as the number of heat treatments increases, the Cu ions of the PCB pad are found to diffuse to the inside of the OSP layer [22]. In addition, a number of previous studies on Cu oxidation have reported the limitations of OSPs [23-27]. In order to compare the Cu oxidation layer formed on the plasma surface finish and the OSP surface after multiple heat treatments, FTIR analysis was conducted and the results as a function of number of heat treatments are shown in Figures 3.24 and 3.25. As shown in Figure 3.24, when the number of heat treatments increases, increasing quantities of Cu_2 oxide can be found on the OSP surface. In general, similar quantities of this oxide were observed up to the third heat treatment, but after the fourth treatment, the quantities increased drastically. As confirmed by the TEM micrograph shown in Figure 3.16, Cu transported from a thin region in the uneven OSP layer combined with oxygen to form a Cu_2O layer. On the other hand, in

the plasma surface finish of Fig. 3.24, there was no change observed in the Cu_2O peak, even after the fourth heat treatment. Hence, the plasma surface finish has high oxidation resistance for multiple heat treatments, and is verified as a Cu-based surface finish that could replace the common OSP material.

3.4 Summary

In this study, the effects of multiple heat treatments on the wettability, interfacial reactions, and mechanical reliability of SAC305 solder on plasma surface-finished PCBs were investigated, and the results compared to those for the SAC305/OSP system.

Wetting and spreading tests showed that the plasma-finished samples had higher wetting forces and shorter zero-cross times than the OSP surface finish. The wetting force (and hence solderability) was not dependent on the number of heat treatment for the plasma surface finish, whereas the wetting force rapidly decreased with each additional heat treatments for the OSP surface finish. In the case of the multiple heat-treated OSP sample, the wetting reaction did not occur due to the degradation of the OSP.

The plasma-coated layer was uniformly formed on the Cu pad with a thickness of about 20 nm. This layer was removed by the combined action of the flux and the high reflow temperature used. This resulted in the Cu layer coming into direct contact with the molten solder and forming Cu-Sn IMCs at the interface. In the reflow reaction with

SAC305 solder, the morphology and thickness of the interfacial IMCs for the two surface finishes were similar.

From ball shear tests it was found that the shear force for the plasma substrate was consistently higher than that for the OSP substrate. In the case of the plasma substrate, the shear force was independent of the number of reflows, while it decreased rapidly after five reflow cycles for the OSP substrate. The poor wettability, reduced bonding area, and void formation of the OSP finish after multiple heat treatments resulted in degradation of the joint. These results clearly indicate that the plasma surface finish was superior to the conventional OSP finish with respect to wettability and joint reliability.

3.5 Figures

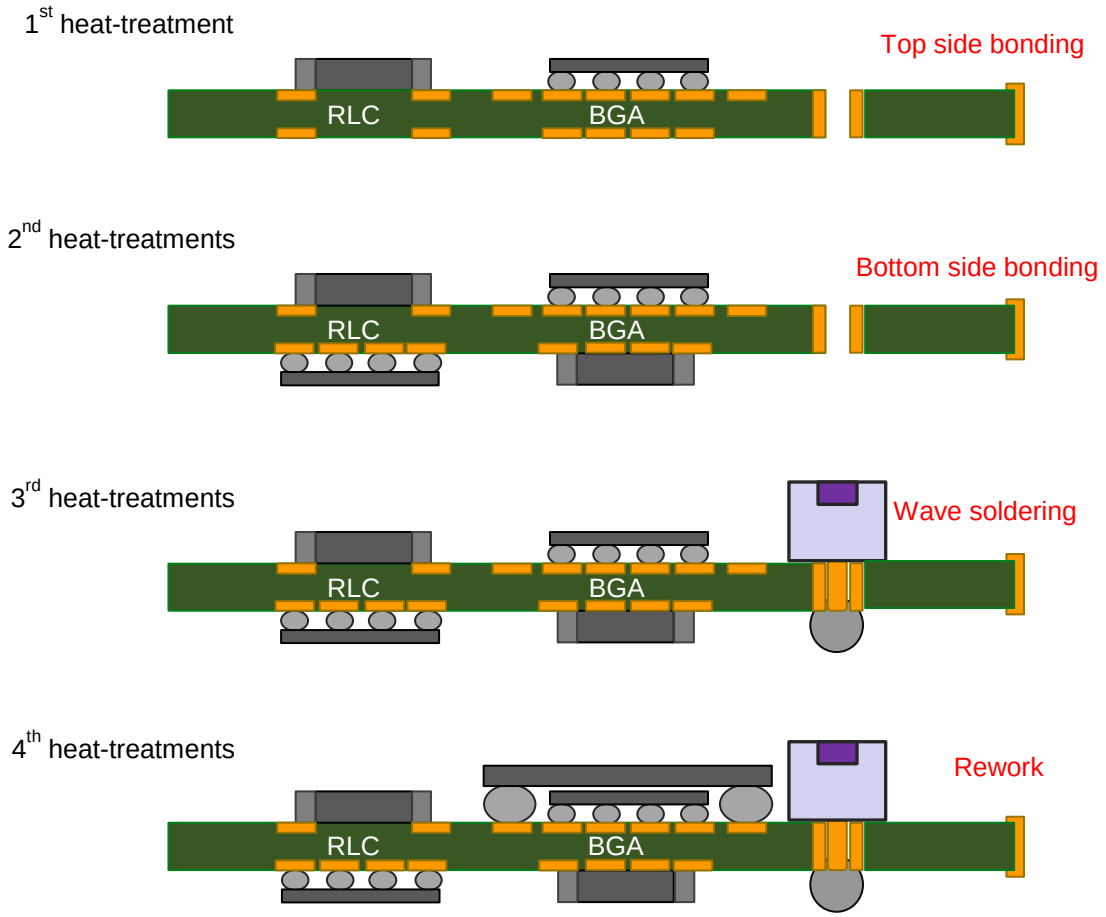


Figure 3.1 Schematics showing the multiple heat treatment process.

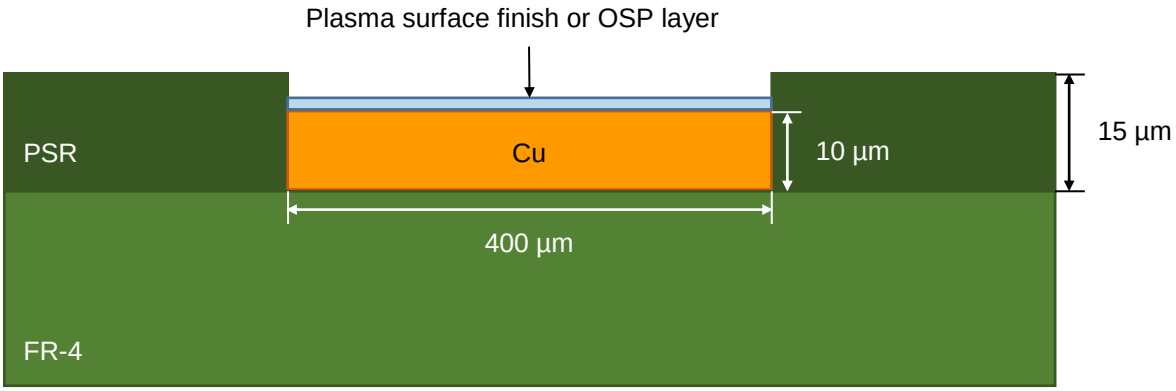


Figure 3.2 Schematic illustration of the test samples used in this study, showing the FR-4 PCB, photo solder resist (PSR), Cu pads, and surface finish layers.

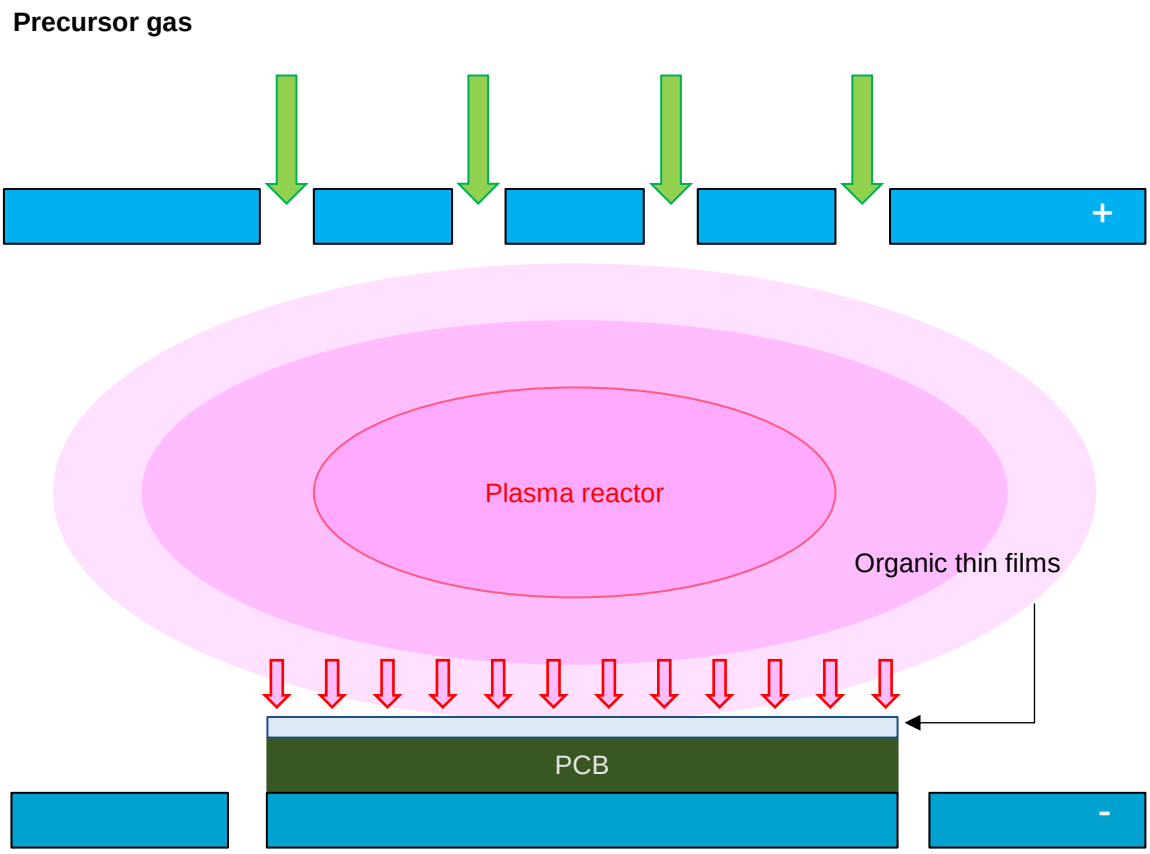


Figure 3. 3 Schematic of the plasma surface finish process.

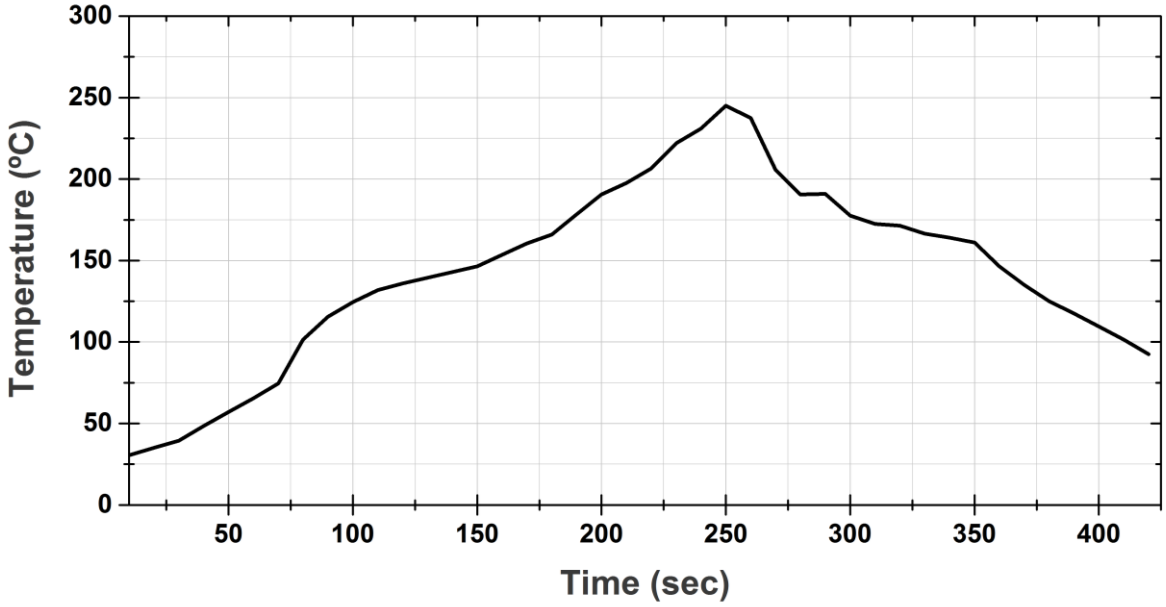
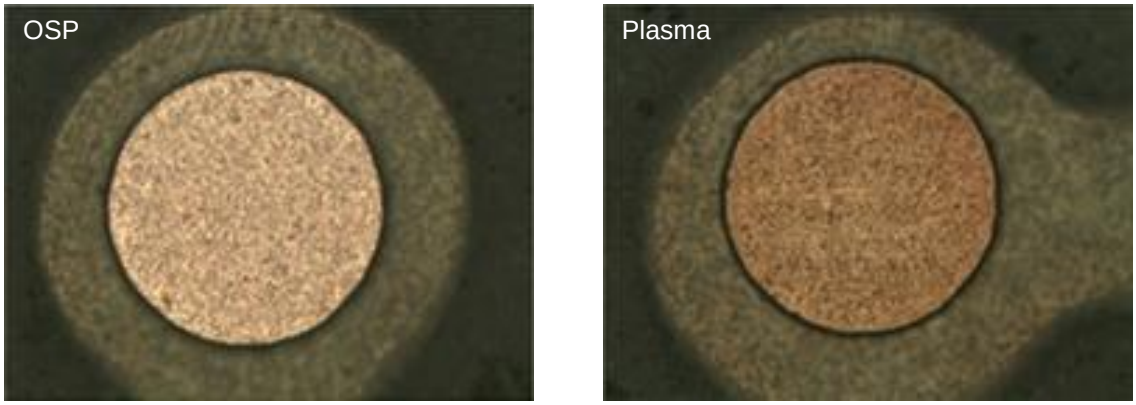
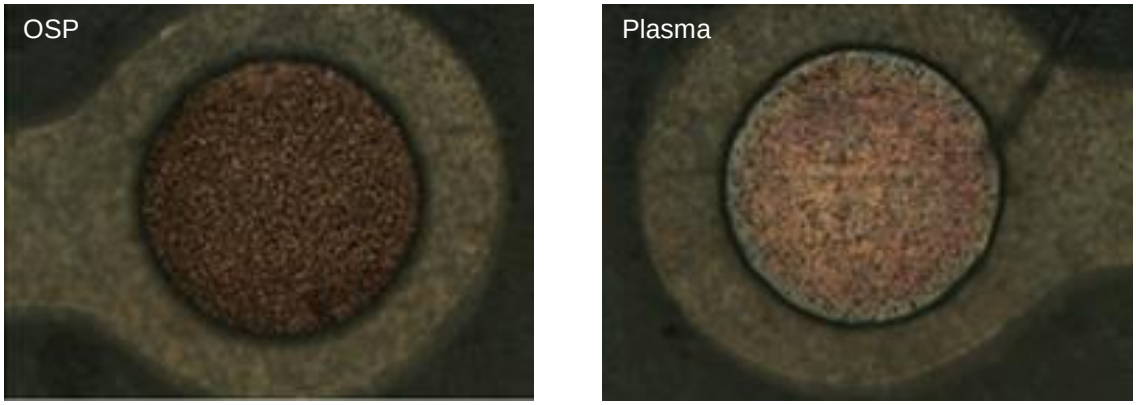


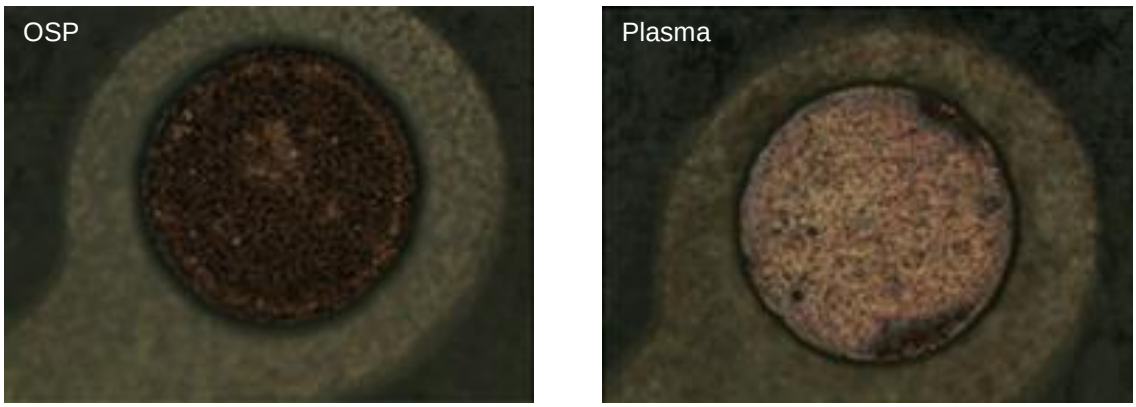
Figure 3.4 Temperature vs. time reflow profile for the Sn-3.0Ag-0.5Cu solder.



(a) Initial condition



(b) After 6 hours



(c) After 15 hours

Figure 3.5 Optical microscopy images of the Cu pad after salt spray test for OSP and plasma samples, after (a) 0, (b) 6, and (c) 15 h.

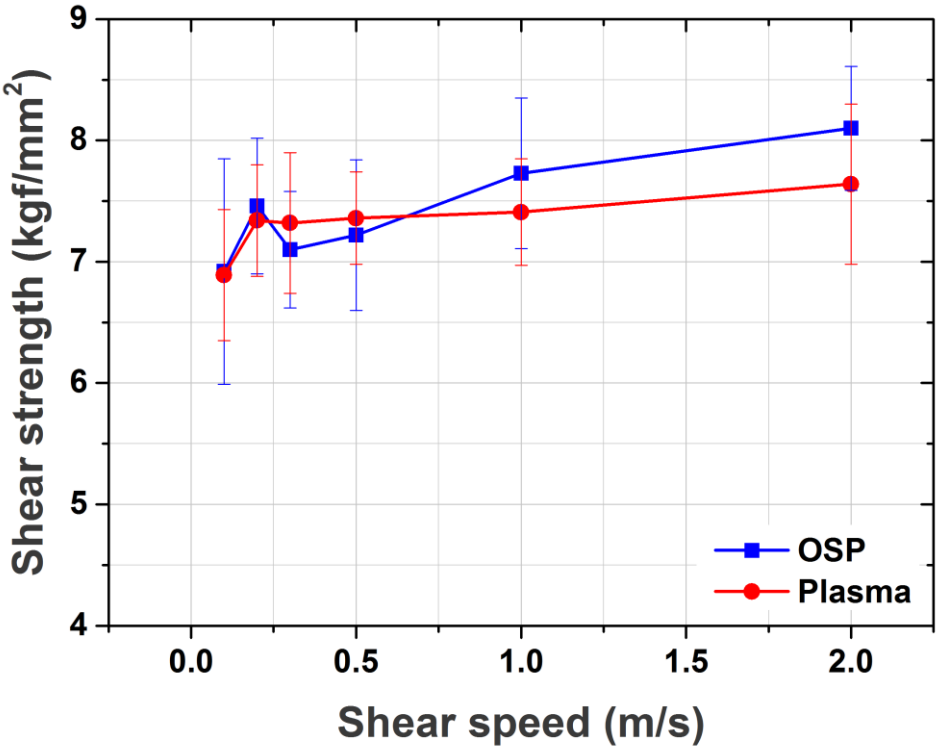


Figure 3.6 Shear strength as a function of shear speed for OSP- and plasma-finished samples after a single heat treatment.

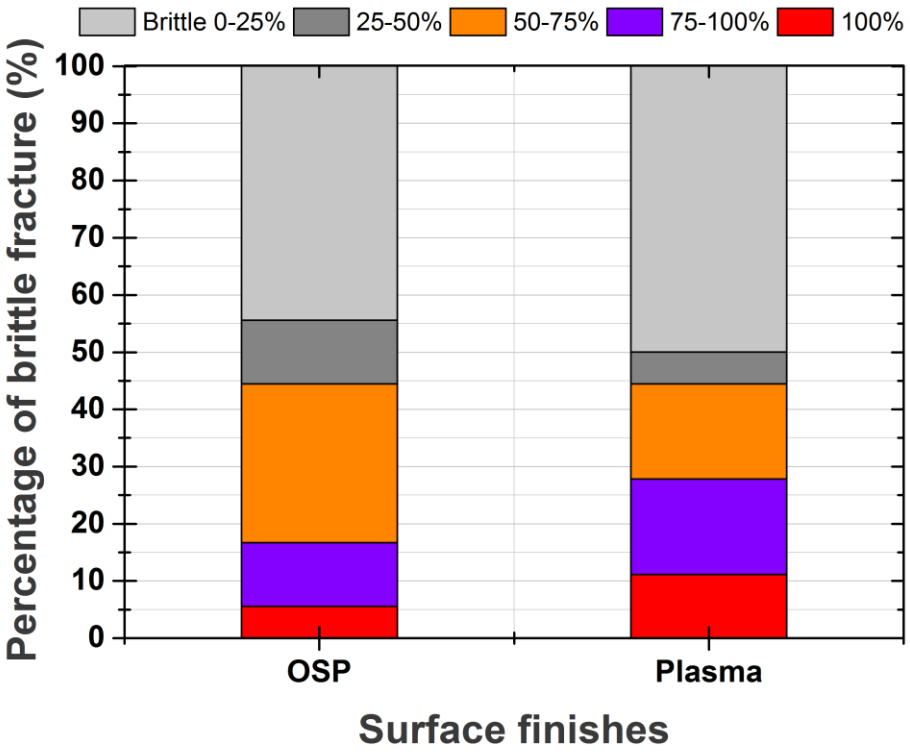
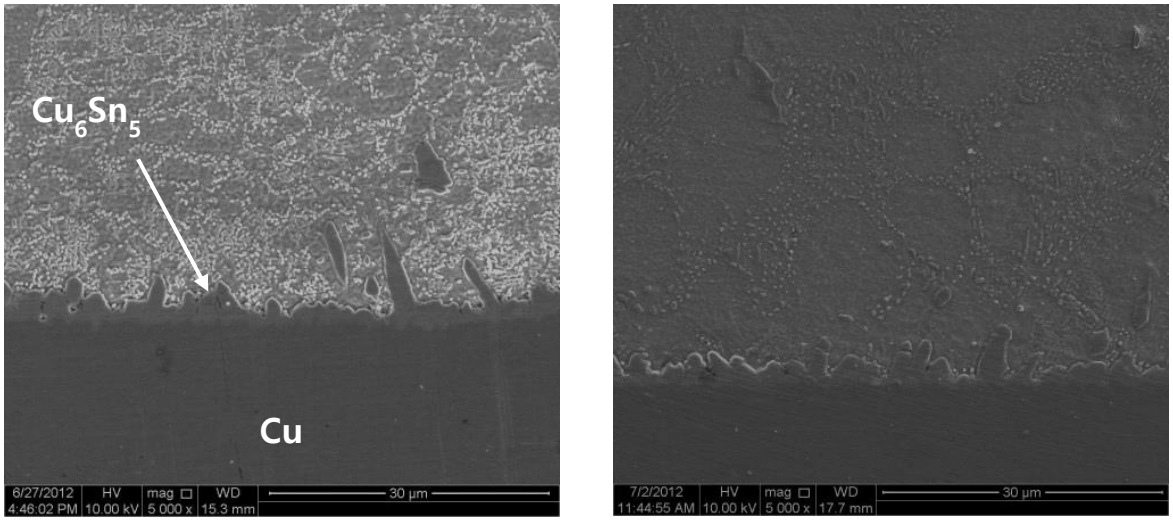


Figure 3. 7 Brittle fracture rate of OSP- and plasma-finished sample after a single reflow.



(a) OSP finish (b) Plasma finish

Figure 3.8 SEM micrographs comparing the morphology of the IMC layers of the (a) OSP- and (b) plasma-finished samples after a single heat treatment.

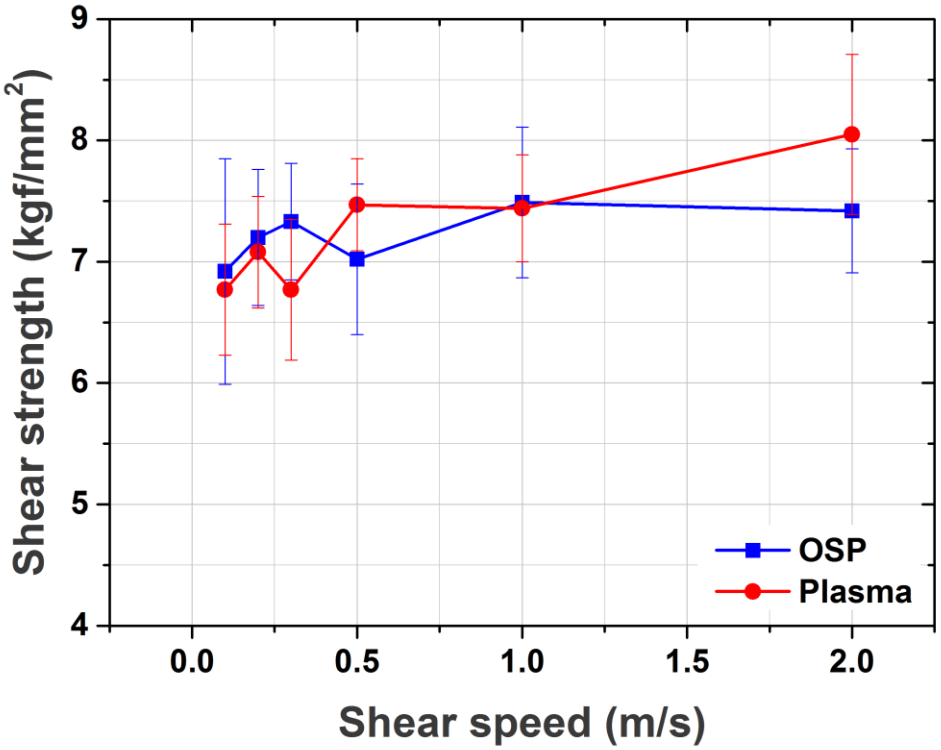


Figure 3.9 Comparison of high-speed shear strengths of OSP- and plasma-finished samples as a function of shear speed after five heat treatment cycles.

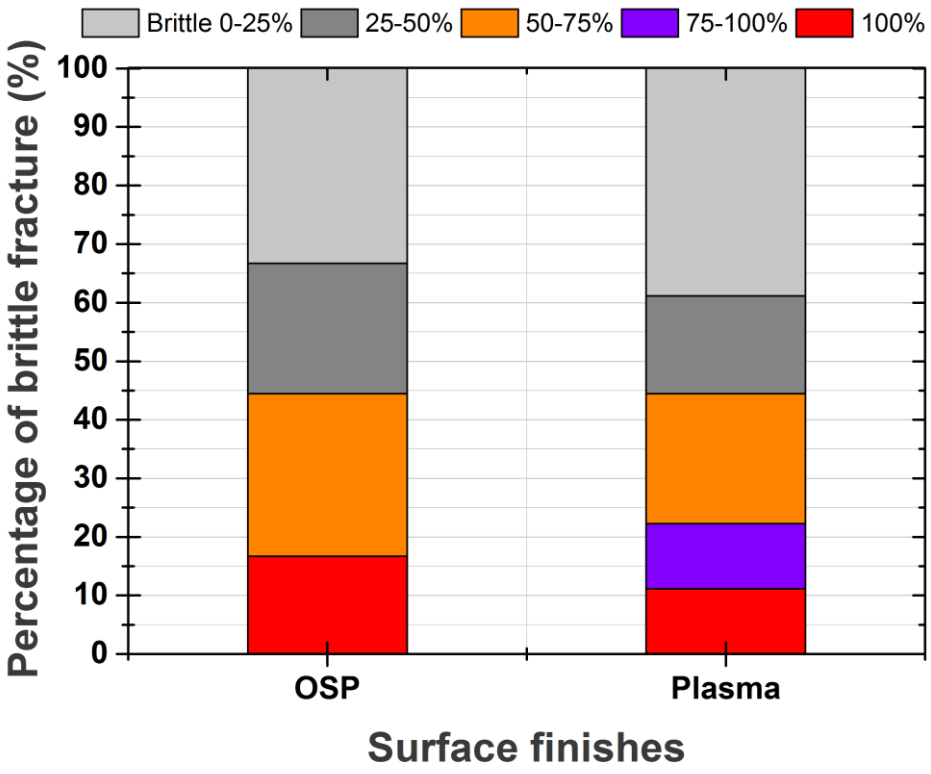
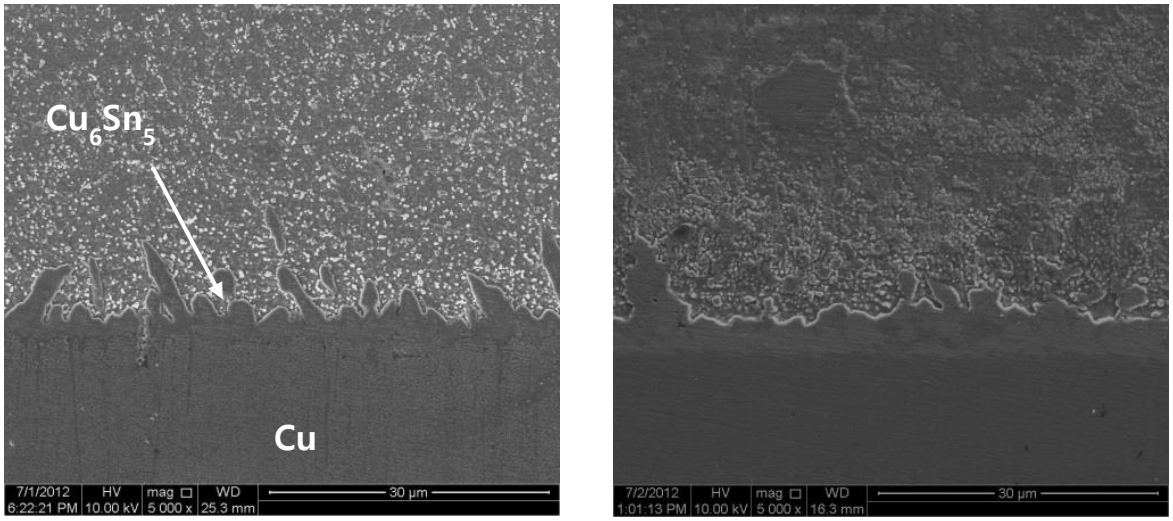


Figure 3.10 Percentage of brittle fracture of OSP- and plasma-finished sample after five reflow cycles.



(a) OSP finish (b) Plasma finish

Figure 3.11 Cross-sectional SEM micrographs comparing the IMC layers of the OSP- and plasma-treated samples after multiple heat treatments.

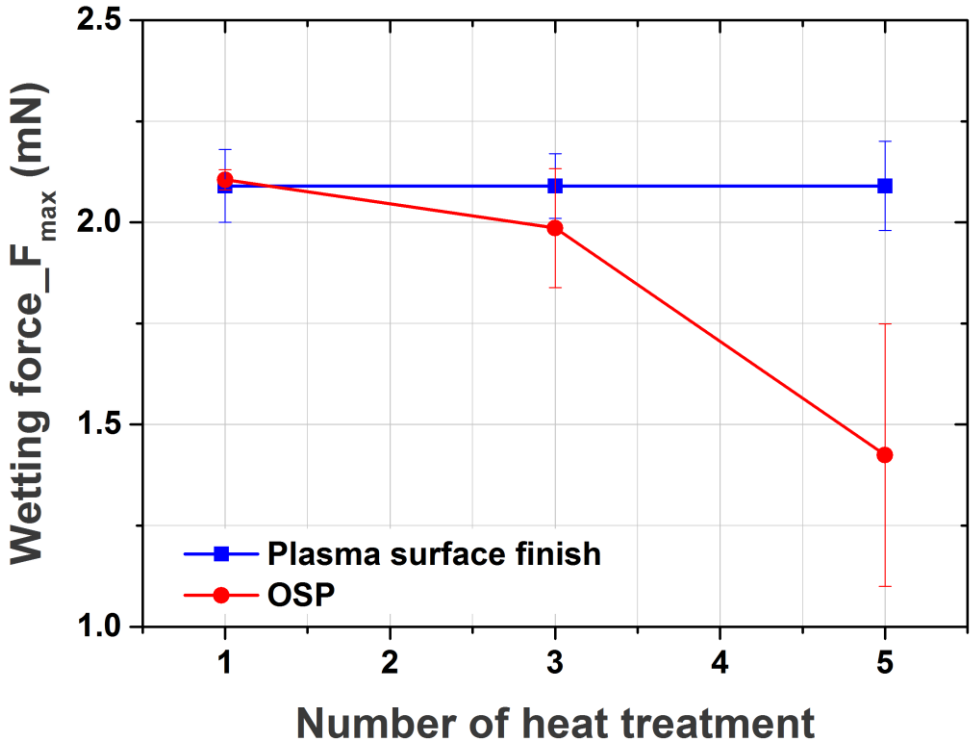


Figure 3.12 Wetting forces of the plasma and OSP surface finishes as a function of heat treatment cycle.

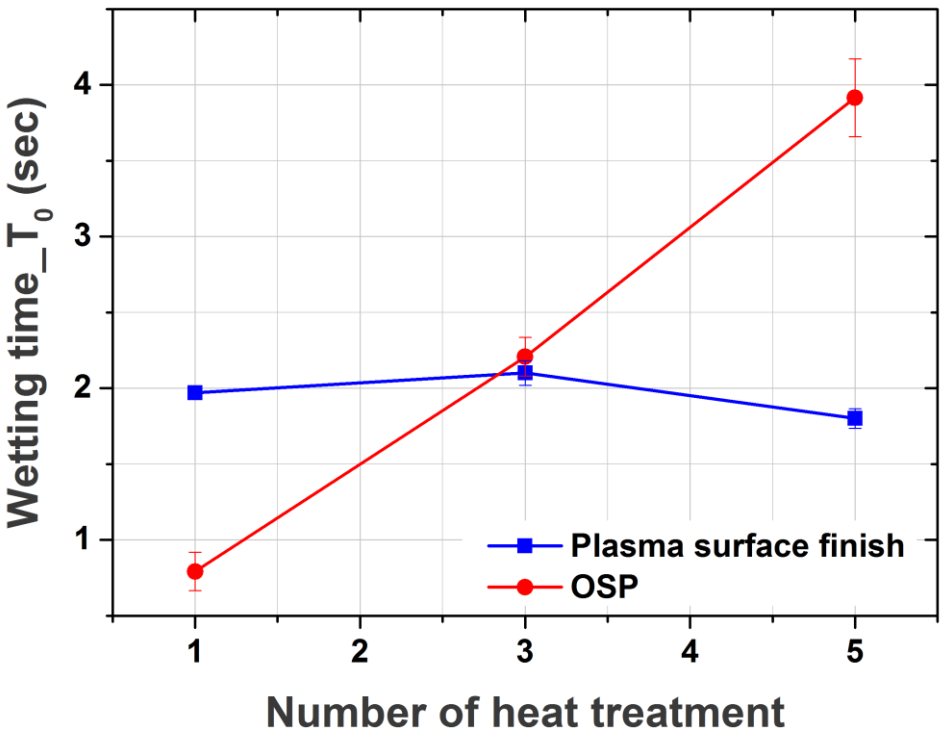


Figure 3.13 Wetting times of the plasma and OSP surface finishes as a function of heat treatment cycle.

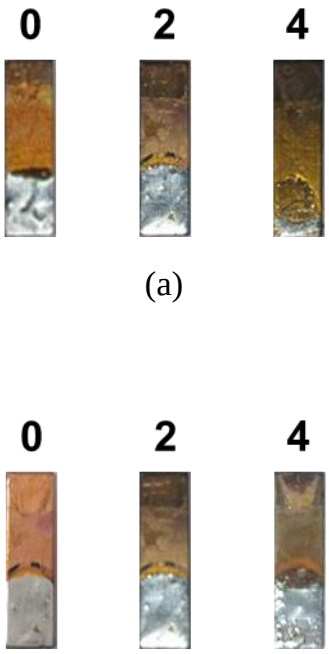


Figure 3.14 OM images of the test coupons after wetting tests. (a) OSP and (b) plasma surface finishes subjected to 0, 2, or 4 heat treatment cycles before wetting.

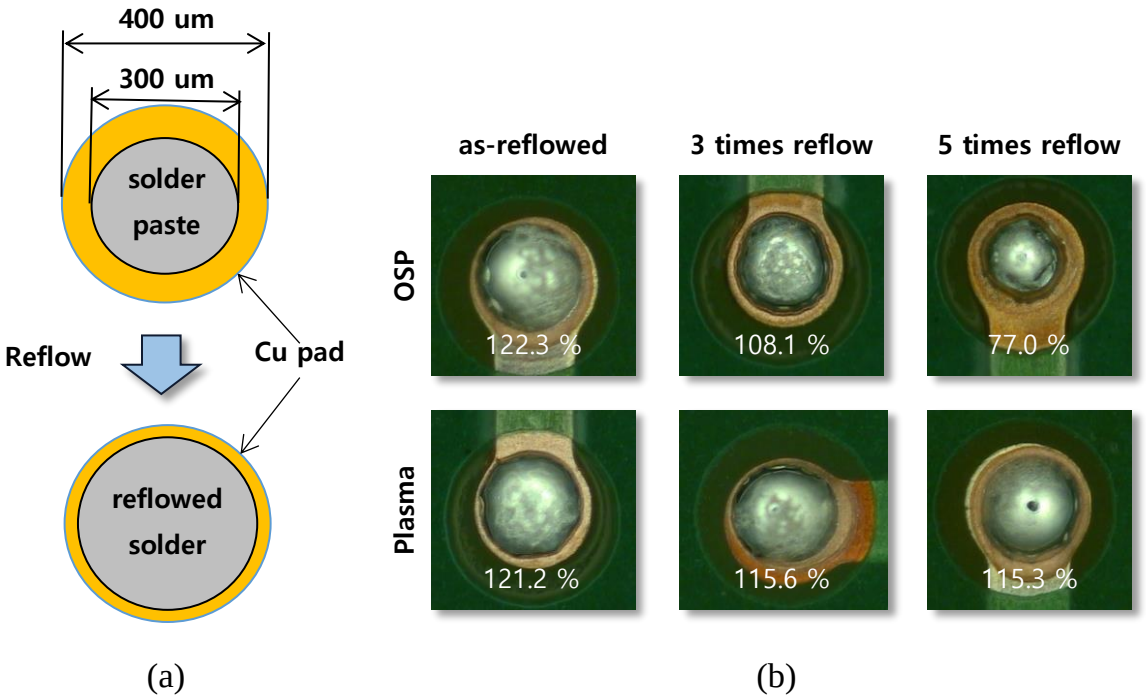
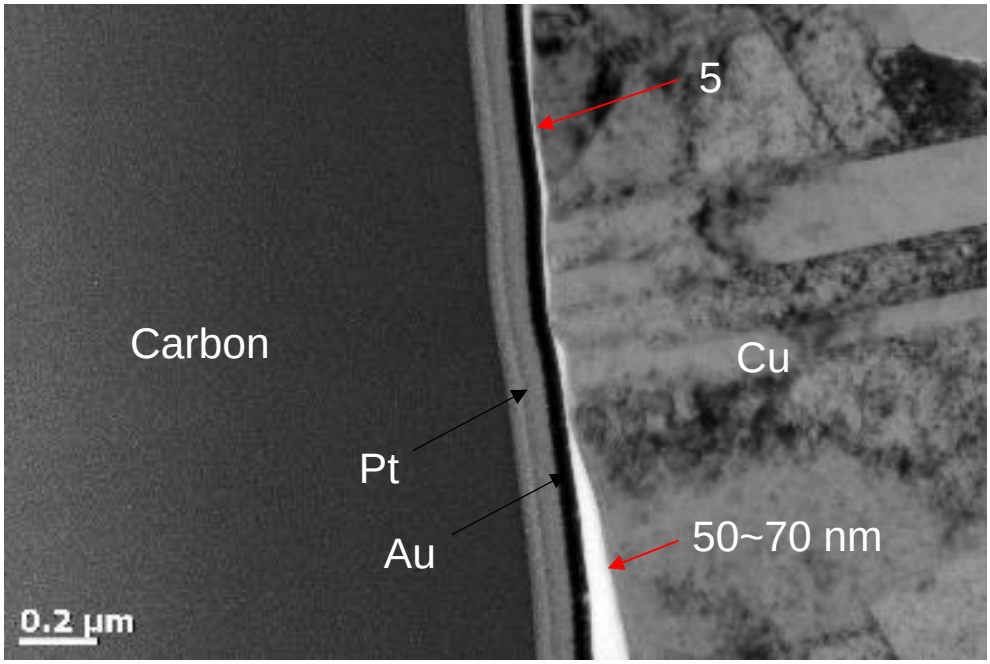
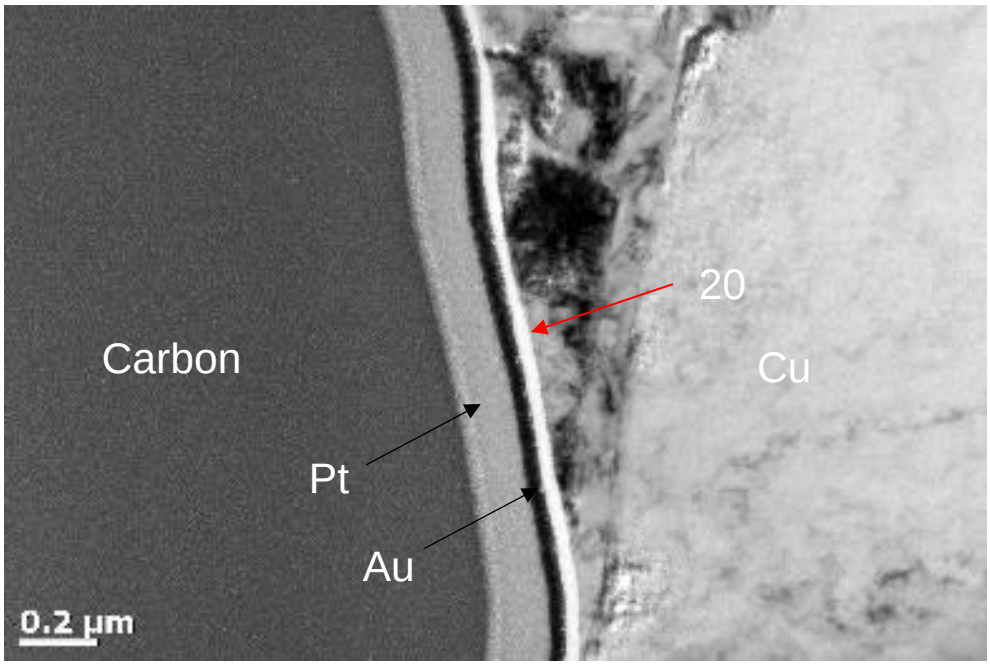


Figure 3.15 (a) Schematic illustration of the solder spreadability test. (b) OM images of the soldered PCBs after spreading tests for OSP- and plasma-finished samples subjected to multiple heat treatments.

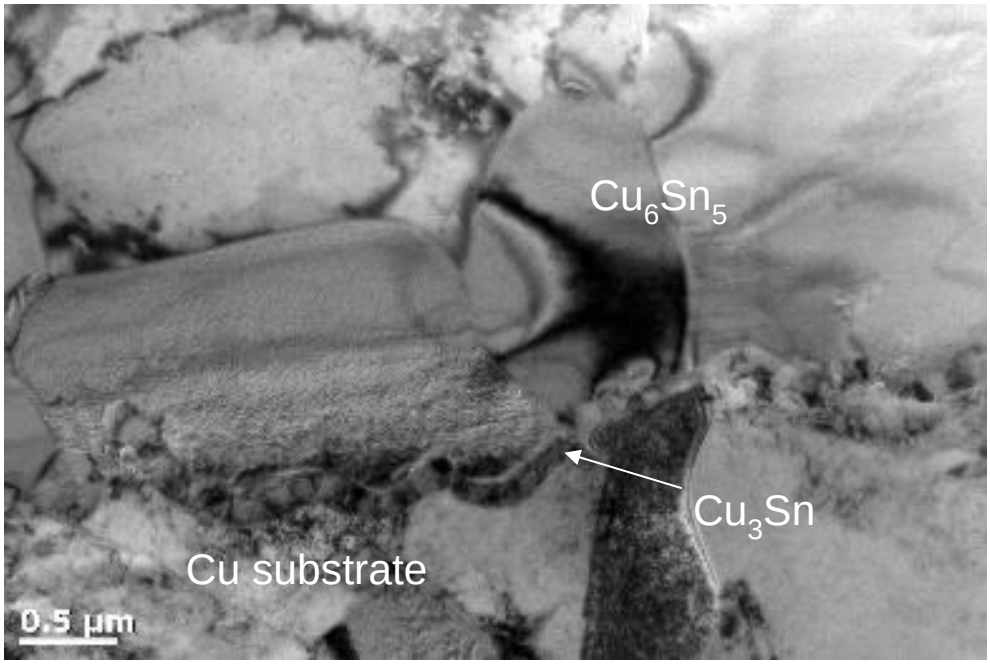


(a)

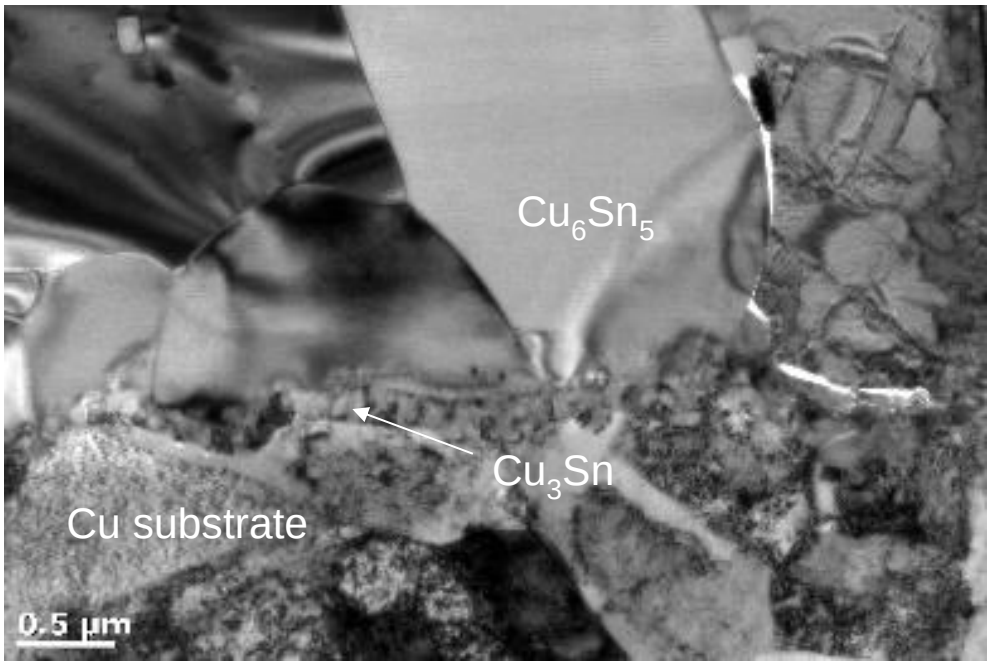


(b)

Figure 3.16 Cross-sectional TEM micrographs of the (a) OSP and (b) plasma surface finished Cu substrates, where the surface finish layers are the white films.



(a)



(b)

Figure 3.17 Cross-sectional TEM images of the (a) OSP and (b) plasma surface finished samples after soldering showing the formation of IMC grains.

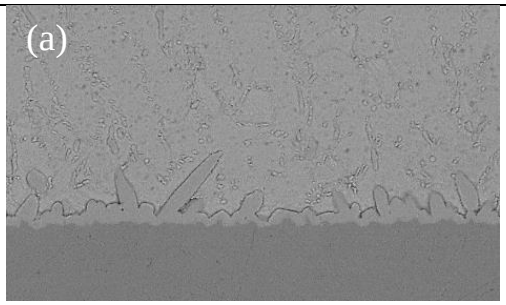
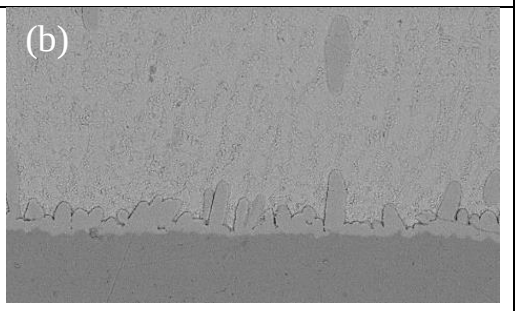
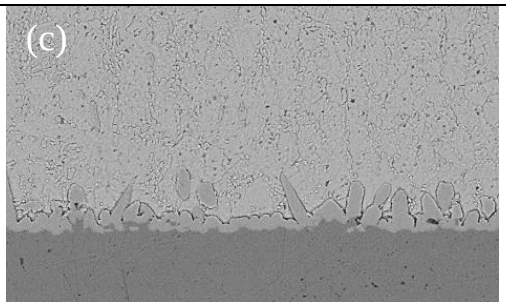
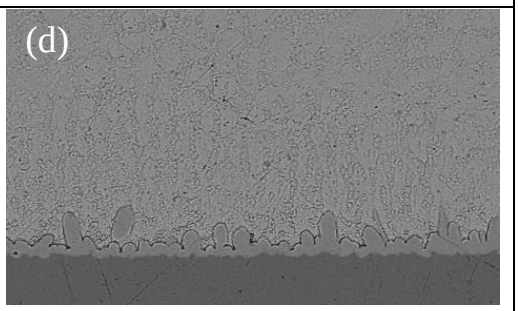
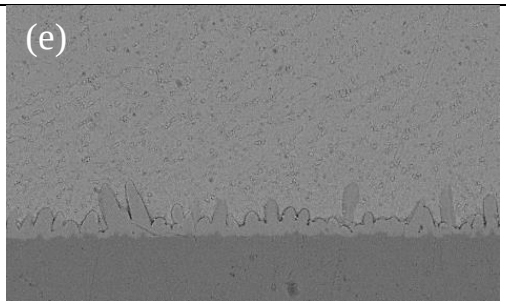
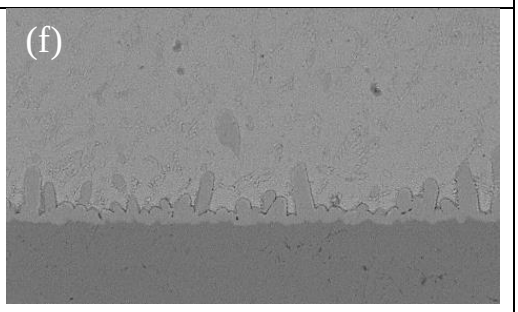
	OSP	Plasma
1 time		
3 times		
5 times		

Figure 3.18 Cross-sectional SEM micrographs of the SAC305 solder joints with different surface finishes after multiple reflows.

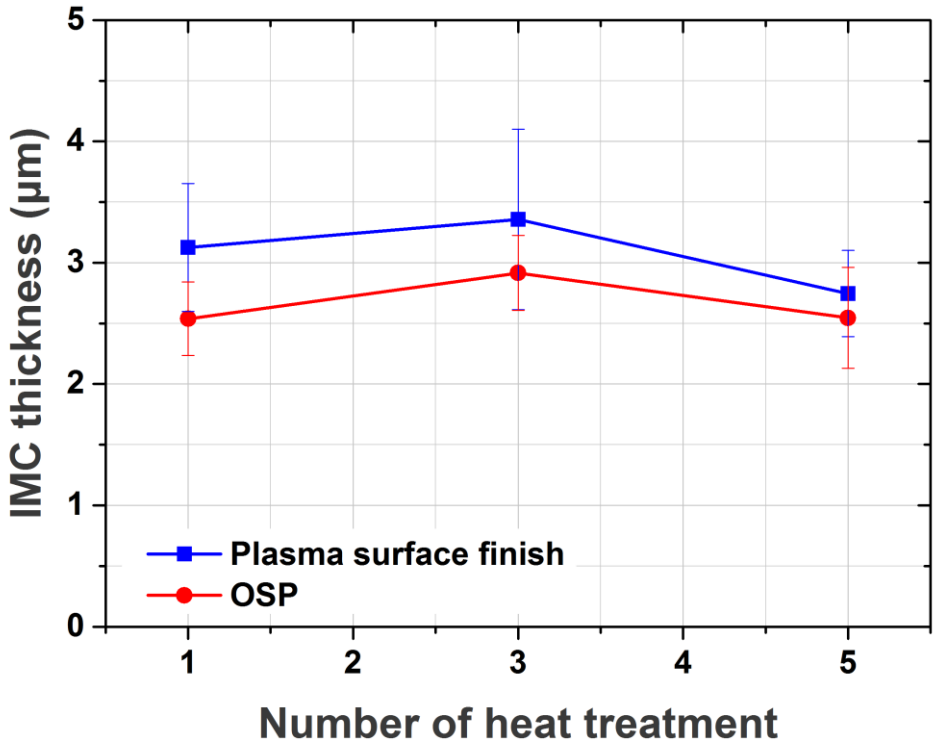


Figure 3.19 Average thicknesses of the IMC layers within the SAC305 solder joints for the OSP and plasma surface finishes as a function of reflow heat treatments.

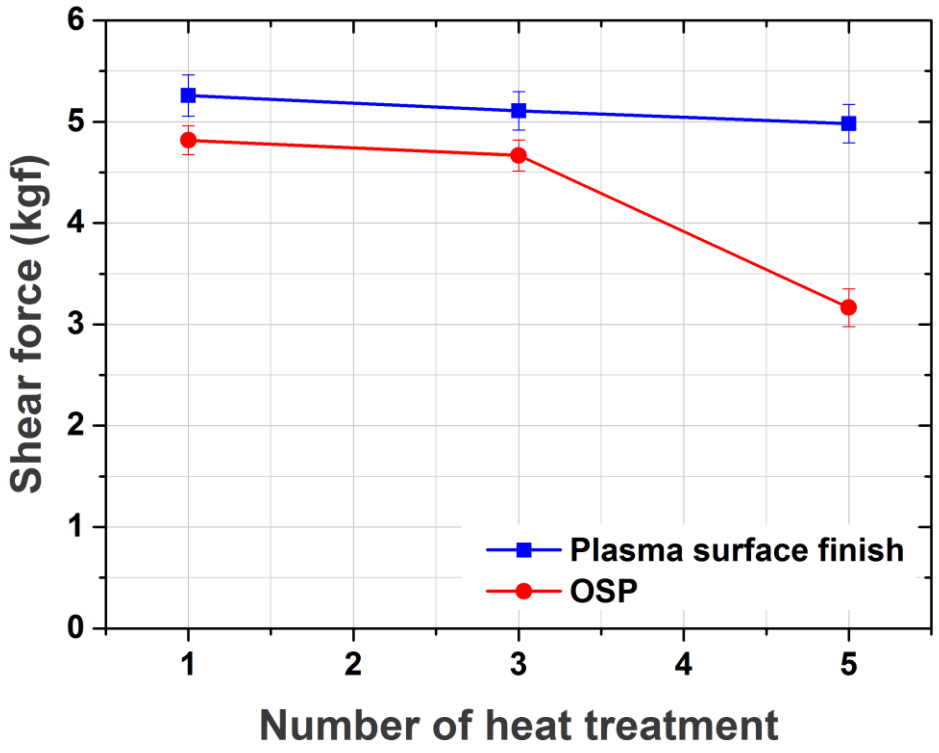


Figure 3.20 Average shear force of the SAC305 solder joints with different surface finishes after multiple reflows.

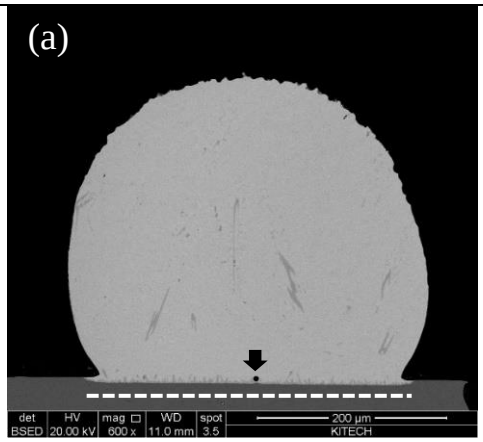
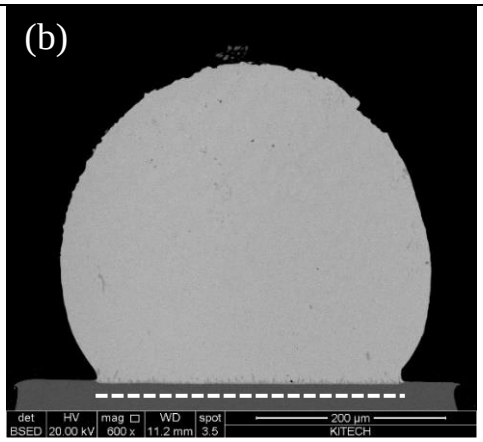
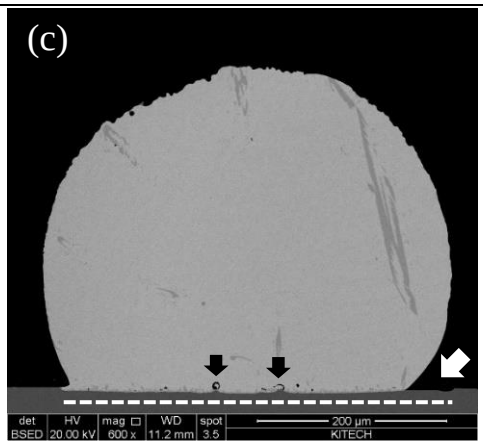
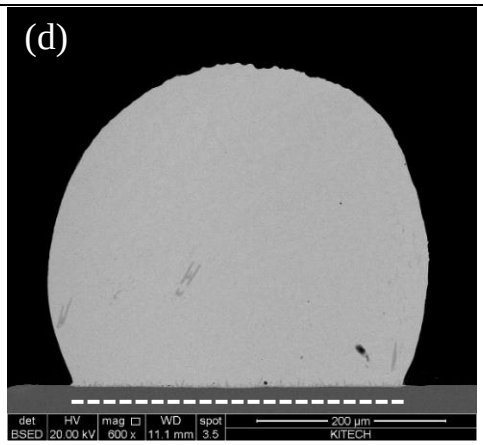
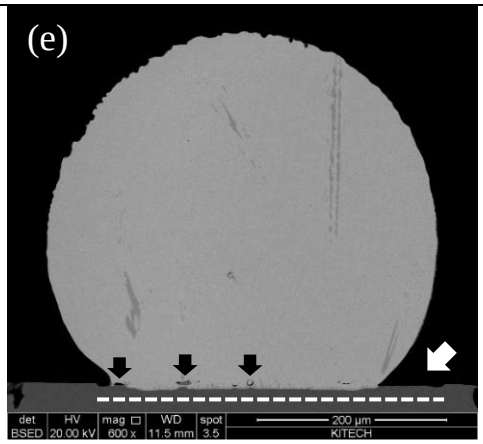
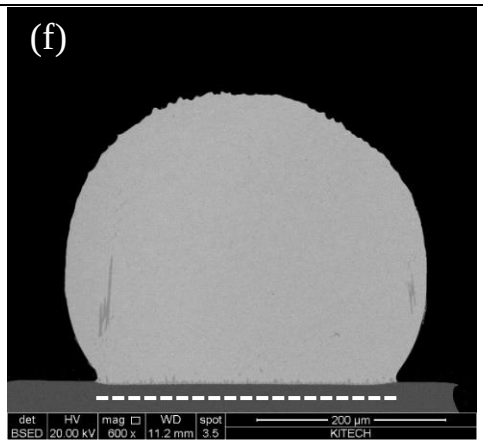
	OSP	Plasma
1 time		
3 times		
5 times		

Figure 3.21 Cross-sectional SEM micrographs of the multiple-reflow SAC305 solder joints with different surface finishes. The white dashed lines indicate the Cu pad, the white arrows indicate the unreacted area of the Cu pad, and the black arrows indicate voids developed at the interfaces.

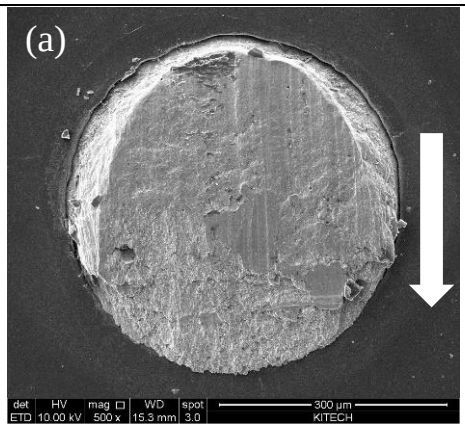
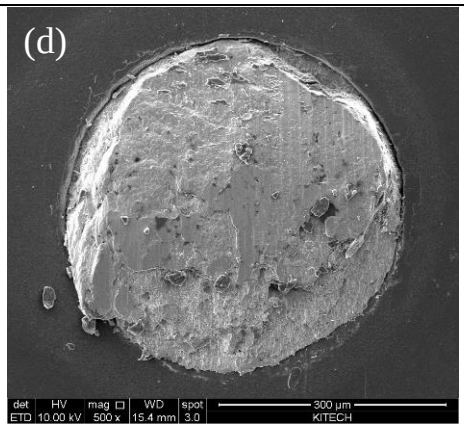
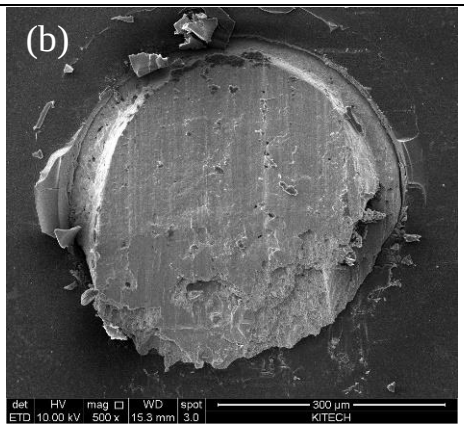
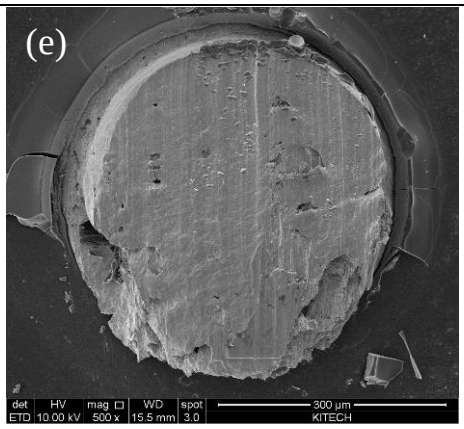
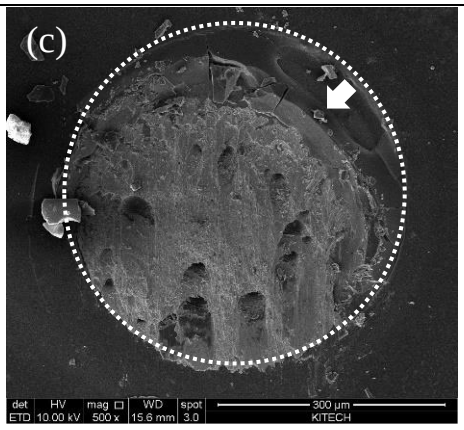
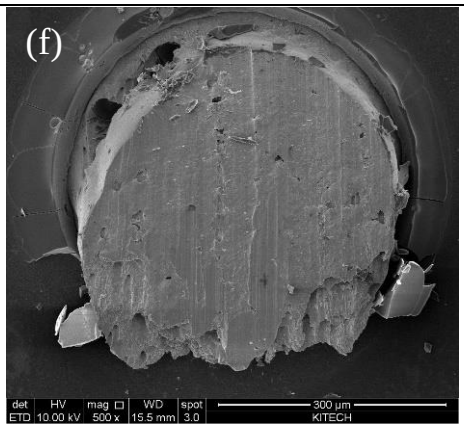
	OSP	Plasma
1 time		
3 times		
5 times		

Figure 3.22 SEM micrographs of the fracture surfaces of the solder joints after shear testing. The white dashed circle indicates the area of the Cu pad, the white arrows indicate the unreacted area with the Cu pad, and the black arrow indicates the direction of shear.

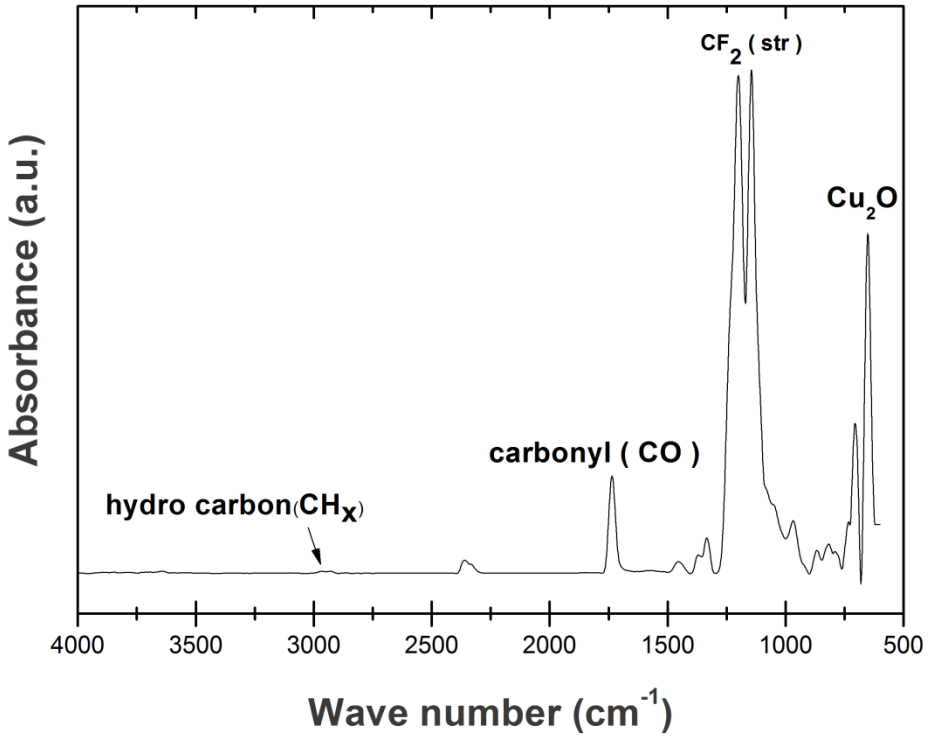


Figure 3.23 FITR analysis of the plasma surface finish layer.

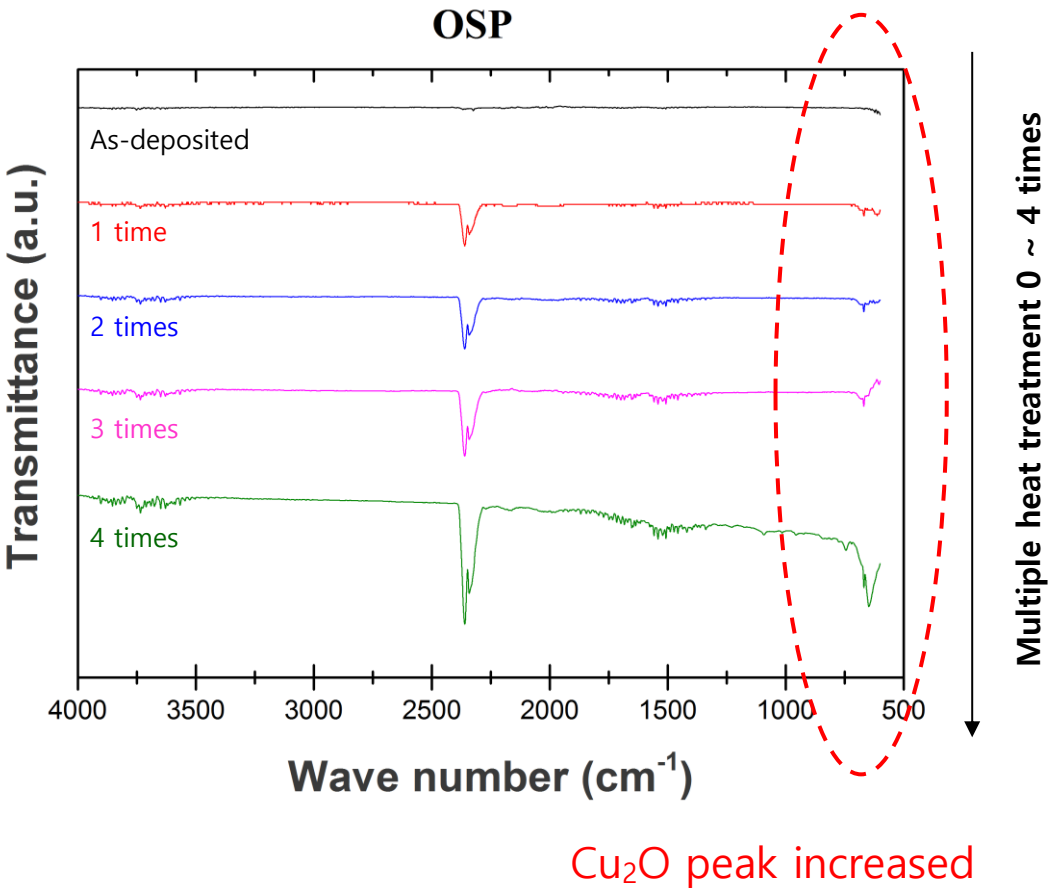


Figure 3.24 FTIR analysis of the Cu_2O peaks for the OSP-finished sample after multiple heat treatments.

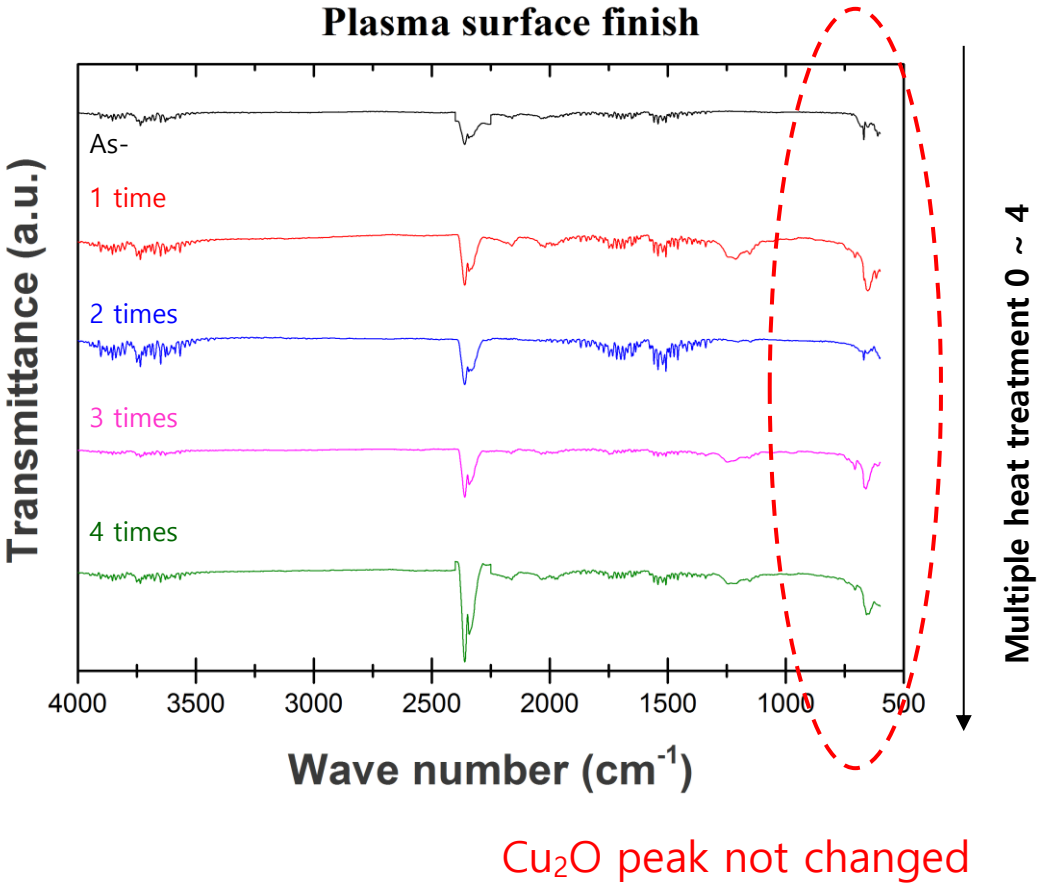


Figure 3.25 FTIR analysis of the Cu_2O peaks for the plasma surface finish after multiple heat treatments.

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Chapter 4

Solder printability of a stencil with a hydrophobic organic coating

4.1 Introduction

The requirements of recent high-performance mobile devices have driven the use of miniaturized electronic components, such as 0603 (0.6 mm × 0.3 mm) and 0402 (0.4 mm × 0.2 mm) passive chips and fine pitch BGA packages under 0.5 mm in pitch [1-2]. The adoption of fine-pitch components in electronic circuitry necessitates the reduction of the stencil aperture size for solder paste stencil printing. Normally, a decrease in the stencil aperture size yields low solder printability, which is a potential source of soldering failures [3]. Therefore, the solder printing properties should be

enhanced to enable miniaturized components. To improve the printability of small pads, hydrophobic-organic-coated stencils have been widely studied [4-5]. Although recent studies showed the superiority of hydrophobic coatings, the detailed relationship between hydrophobicity and printability has not yet been reported.

In this study, the effects of hydrophobic organic thin film coatings (i.e., the plasma surface finish method) on solder printability are presented, including their impact on printing efficiency and the solder bridging rate. The hydrophobic organic film was deposited onto the SUS304 stainless steel stencils by plasma-enhanced chemical vapor deposition (PECVD) [6]. The microstructure of the aperture wall was observed using SEM and TEM and the relationship between wall microstructure and printing efficiency is discussed. The solder bridging rate was also evaluated for hydrophobic-thin-film-coated stencils in this study.

4.2 Experimental procedures

4.2.1 PCB design and hydrophobic coating

Hydrophobic organic thin films were deposited on the conventional SUS304 laser-cut stencil using PECVD [7]. The thickness of the SUS304 laser-cut stencil was 100 μm. The stencil aperture size was the same as the pad size of the test PCBs. Figure 4.1 shows the PCB land design used in this study. The test PCB had three sections: 0603 and 0402 pads, BGA pads, and solder bridging test pads. The 0603/0402 pads and

BGA pads were designed for printing efficiency tests. The size of the 0603 pads was 0.3 × 0.26 mm and that of the 0402 pads was 0.2 × 0.23 mm. The distance between the pads was 0.16 mm and 0.14 mm for 0603 and 0402, respectively. The BGA pads were circular with a diameter of 0.2 mm. The pitch size of the BGA was 0.35 mm. The total number of the pads per BGA circuit was 64. The specific design of the solder bridging test section shown in Figure 4.1 is shown more clearly in Figure 4.2. The lengths of the solder bridging test pads were varied from 0.5 to 1.5 mm and the width was 0.2 mm. The pitch of the solder bridging test pads was varied from 0.25 to 1.2 mm. Figure 4.3 shows a schematic of the cross-section of the test PCB. The PCB was of the non-solder mask defined (NSMD)-type [8]. The final surface finish using the ENIG method was applied to the test PCB [9].

4.2.2 Printing process and solder volume measurements

The type 5 (size range: 15–25 μm) solder paste (Senju Metal; Sn 96.5 wt%, Ag 3.0 wt%, and Cu 0.5 wt%) was printed on the PCBs through hydrophobic-film-coated-stencils using a screen printer (Minami, MK-878Mx) [10]. The processing conditions for solder printing are shown in Table 4.1.

The printing efficiency was calculated using the following equation:

$$Printing\ efficiency = \frac{Volume\ of\ printed\ solder}{Volume\ of\ maskhole} \quad (1)$$

The volume of the printed solder paste was measured using a solder paste inspection machine (SPI, Koh Young Tech KY-3020). The solder bridging rate was defined as the number of the bridged PCBs divided by total number of PCBs.

4.2.3 Microstructural observation of stencil aperture

The microstructure of the stencil aperture was observed using OM and FE-SEM (FEI Inspect F). Cross-sectioned samples of the coated stencil were also observed with TEM (JEOL JEM 4010). The TEM sample was prepared using FIB techniques (Helios 600). The surface roughness was measured with atomic force microscopy (AFM, Park Systems XE-100).

4. 3 Results and discussion

4.3.1 Hydrophobic coating on stencil

The hydrophobic properties of the organic thin film on the stencil were evaluated using a water droplet contact angle test; the water droplet observed on the stencil is shown in Figure 4.4 [11]. The contact angle of the water droplet on the uncoated stencil was 66.5° while that on the coated stencil was 100.8°. The higher contact angle for the thin-film coating confirms that the coated stencil was more hydrophobic than the uncoated stencil.

The stencil surface and the aperture wall were observed by cross-sectional TEM, as shown in Figure 4.5, to determine the thickness of the hydrophobic organic thin film. The Au and Pt layers were deposited for preparing the TEM samples. The carbon layer observed in the TEM originated from oil that was used in the rolling process of the SUS304 stainless steel sheets. The thickness of the hydrophobic organic thin film was about 1450 nm on the stencil surface and about 500 nm on the aperture wall.

4.3.2 Improvement of bridging rate

The solder bridging rate values as a function of pitch size are shown in Figure 4.6. Solder bridging was evaluated by counting the number of PCBs that showed solder bridges [12-13]. The solder bridging rate was defined as the number of bridged samples within the ten total samples. Figure 4.7 shows the solder bridging rates for the uncoated and coated stencils. The solder bridging rate for the uncoated stencil was 40% for a pad length of 0.5 mm. As the pad length increased, the bridging rate increased. In addition, the coated stencil showed a lower bridging rate than the uncoated stencil.

To observe the effect of hydrophobicity on the solder bridging properties, the solder paste was printed on a glass plate instead of the test PCB and observed through the glass just after printing (Figure 4.8). The width of the stencil aperture was 0.2 mm. The width of the solder paste printed through uncoated and coated stencils was 0.294 mm and 0.265 mm, respectively. This indicates that the spread of the solder paste after printing was lower through the coated stencil than through the uncoated stencil. Figure

4.9 shows a schematic of the solder printing process through the coated and uncoated stencils. Due to the hydrophobicity, the solder paste passing through the aperture of the coated stencil had a high surface tension. Therefore, the solder paste printed on the PCB had a low spread width that resulted in a low bridging rate.

4.3.3 Printing efficiency

Figure 4.10 shows the printing efficiency of 0603, 0402, and BGA pads using coated and uncoated stencils [14]. The 0603 pad had the highest printing efficiency among the three types of pads studied because they had the highest ratio of aperture area to aperture wall area. The average printing efficiency of the 0603 pads was 76.9% and 84.1% for the uncoated and coated stencils, respectively. The 0.35-mm pitch BGA showed the lowest printing efficiency since its ratio of aperture area to aperture wall area was lower than those of the other pads. The average printing efficiency of the BGA pads was 62.3% and 65.5% for the uncoated and coated stencils, respectively. When the ratio of aperture area to aperture wall area is low, the possibility of solder particles adhering to the aperture wall increases, thus reducing the printed solder volume deposited onto the product surface. The printing efficiency of the coated stencils was slightly higher than that of the uncoated stencils. However, the dramatic enhancement in printing efficiency reported for coated stencils [5], was not observed here.

4.3.4 Continuous printing

After applying the hydrophobic coating to the SUS stencil, the continuous printing process was carried out in order to emulate the real conditions of SMT processing. Figure 4.11 shows the results of up to thirty trials of continuous printing for the 0402, 0603, and BGA pads. The printability of the 0402 pad shown in Fig. 4.11(a) was 76.7% for the uncoated stencil and 77.7% for the coated stencil; a difference of only 1%. These differences for the 0603 pad and BGA pad were approximately 6% (Fig. 4.11(b)) and 2% (Fig. 4.11(c)), respectively, where the coated stencils resulted in a high printing efficiency. In the continuous printing process, the performance of the hydrophobic coating did not meet initial expectations (only minor improvements were observed). In order to understand why, an analysis was performed on the coated region.

Figure 4.12 shows SEM micrographs of the aperture wall of the uncoated and coated stencils. The upper regions of the SEM micrographs show the PCB side of the stencil aperture and the bottom regions show the squeezing side. On the aperture wall of the uncoated stencil (Figure 4.12 (a)), burrs from the laser cutting of the stencil aperture were observed at the PCB side. The marks from laser-cutting were also observed on the aperture wall. In addition, metal particles were observed on the aperture wall, which may also have been generated during the laser-cutting process. On the aperture wall of the coated stencil (Figure 4.12 (b)), the hydrophobic thin film covered the burrs and laser marks. However, the morphology of the thin film followed that of the underlying structure; therefore, the roughness was not reduced even though

the hydrophobic thin film covered the original surface of the aperture wall.

The roughness of the aperture wall was measured using AFM and is presented in Table 4.2. The upper and lower parts of the aperture wall had higher roughness than the center of the aperture wall. In the center of the aperture wall, the surface roughness was 27.5 and 66.0 nm for the uncoated and coated stencils, respectively. The surface roughness of the squeezing side was 125 and 129 nm for the uncoated and coated stencils, respectively. The surface roughness of the PCB side was much higher than that in other regions, since the PCB side had burrs from laser-cutting. Owing to the high roughness of the PCB and squeezing sides of the aperture wall, the solder paste adhered to these parts. Figure 4.13 shows the solder paste adhering to the squeezing side of the aperture. The high roughness of the aperture wall degraded printing efficiency and the improvement achieved using the hydrophobic coating was not as high as expected.

4.3.5 Hydrophobic stencil

After applying the hydrophobic coating to the SUS stencil, the printing efficiency did not increase as much as expected. To elucidate this, the entire printing process was examined. As shown in Fig. 4.14(a), solder paste remained on the stencil after squeezing. In addition, the blocked aperture was found to open about 2–3 s later. After the solder paste inside broke apart at the center, a part of it was transferred to the PCB. That remaining on the stencil aperture spread to the aperture wall. As seen in Fig. 4.12,

burrs were found on both the upper and lower parts of the stencil aperture, which were created during laser cutting of the aperture. The breaking of the solder paste was confirmed to be a result of these burrs. As illustrated in Fig. 4.14(b), when the solder paste separates after squeezing, it breaks when the frictional force between the solder paste and the aperture wall becomes greater than the viscoelastic forces of the solder paste. Therefore, developments in the technology of the laser-cutting process would allow further improvements in the performance of the hydrophobic coating. This coating process reduced the roughness of the surface, but the thickness of the layer was insufficient to cover the burrs and dimples formed in the aperture. Figure 4.15 shows the morphology of the SUS stencil surface and aperture. Before coating, some dimples can be seen on the surface, which are defects from rolling the SUS material. After applying the hydrophobic coating (Fig. 4.15(b)), the dimples under 500 nm on the surface were smoothly filled. However, the burrs formed on the aperture edge were still visible after coating.

4.3.6 Lifetime of the hydrophobic stencil

In the actual device production process, using complex analysis tools such as TEM for every part to identify the remaining quantity of hydrophobic coating is not viable. This chapter proposes a method for quality control of the coating that could be applied in a realistic production scenario. The first method involves dropping some water on the aperture of the coated stencil, shining an LED lamp on the water droplet formed on

the aperture, and observing the optical pattern generated by the interaction of the light with the droplet. As seen in the schematic diagram shown in Figure 4.16, light is reflected with a pattern of two concentric rings of points for the uncoated aperture where the formed water droplet is flat. On the other hand, for the coated stencil, the formed droplet is more spherical, due to the lower surface energy of the aperture, and the light is refracted to form as an outer ring with an inner ring of points. Hence, when this ring is observed, it can be concluded that there is some coating layer remaining.

The second method is based on the contact angle differences shown in Fig. 4.4. Isopropyl alcohol (IPA; a cleaning agent used in stencil cleaning) is dropped on the coated stencil surface and observe the phenomenon of the alcohol spreading quickly through the aperture. The lower surface energy of the coated aperture helps to rapidly spread the IPA. The IPA does not flow easily into the uncoated aperture, due to the solid edge effect, which occurs when the contact angle of the droplet on the solid edge falls within the following range:

$$\theta_0 \leq \theta \leq (180° - \phi) + \theta_0 \qquad (1)$$

where θ is the contact angle of the droplet on the solid edge, θ_0 is the original contact angle on the surface, and ϕ is the geometrical angle of the solid edge. The droplet does not flow to the aperture wall when θ is less than or equal to 180°, but when it is greater than 180°, the droplet flows to the wall surface [15]. For example, for the uncoated

stencil shown in Fig. 4.4(a), θ_0 is 66.5°, and the perpendicular wall is 90°, thus θ is 156.5°, and the droplet will not flow. On the other hand, once a hydrophobic coating is formed on the stencil, θ_0 becomes 190.8°, which allows the IPA to flow. Using this method, if the IPA remains on the surface, it implies that the properties of the coating layer are poor, and if it flows along the aperture, then the coated stencil is effective and can be used. Figure 4.17 shows a schematic diagram for each of these situations, where case 1 represents the uncoated stencil and case 2 the opposite side of the coated stencil. Case 3 represents the side of the coated stencil with the hydrophobic layer, which allows the IPA to flow.

4.4 Summary

The solder printing efficiency and solder bridging rate were evaluated for the hydrophobic-thin-film-coated stencils in this study. The printing efficiency of coated stencils was higher than that of uncoated stencils. As the pad size increased, the printing efficiency of both the uncoated and coated stencils increased. SEM observations of the aperture wall showed that the top and bottom had higher roughness than the middle. This roughness resulted in solder paste adhering to the aperture wall, which degraded the printing efficiency improvement expected from the hydrophobic thin film coating. The solder bridging rate of the coated stencil was lower than that of the uncoated stencil. The pattern of the printed solder paste that was pressed through the coated stencil was narrower than that using the uncoated stencil. An increase in the

surface tension of the solder paste with the coated stencil decreased the width (reduced the spreading) of the printed solder paste and therefore reduced undesirable bridging.

4.5 Figures

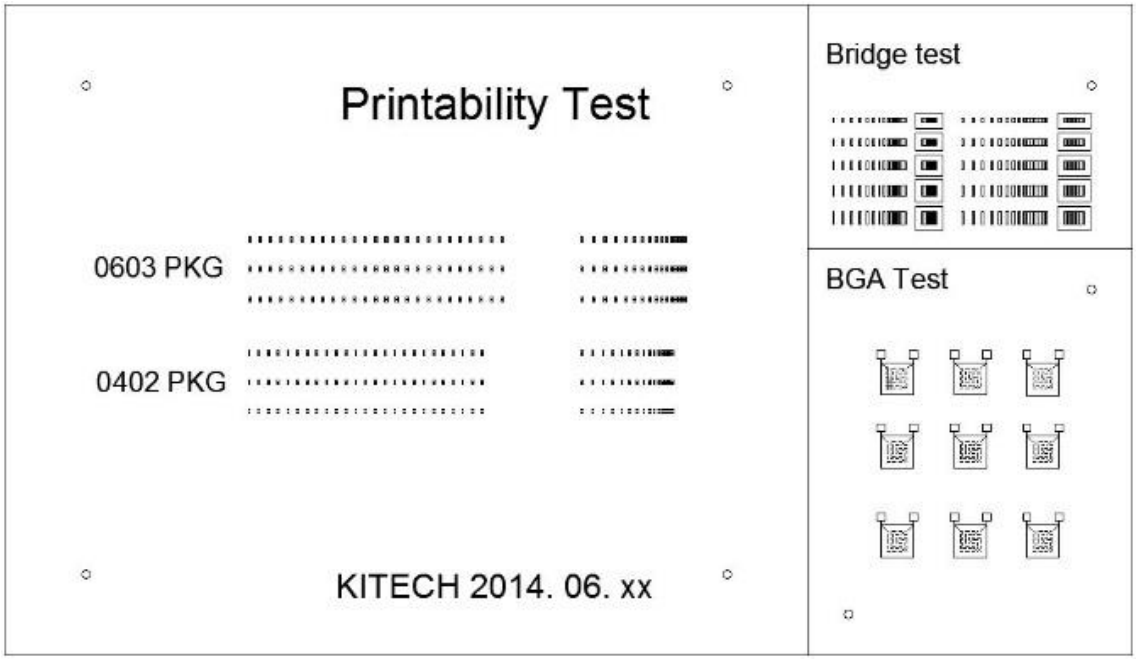


Figure 4.1 Schematic showing the design of the test PCB for the solder printability, bridging, and BGA tests.

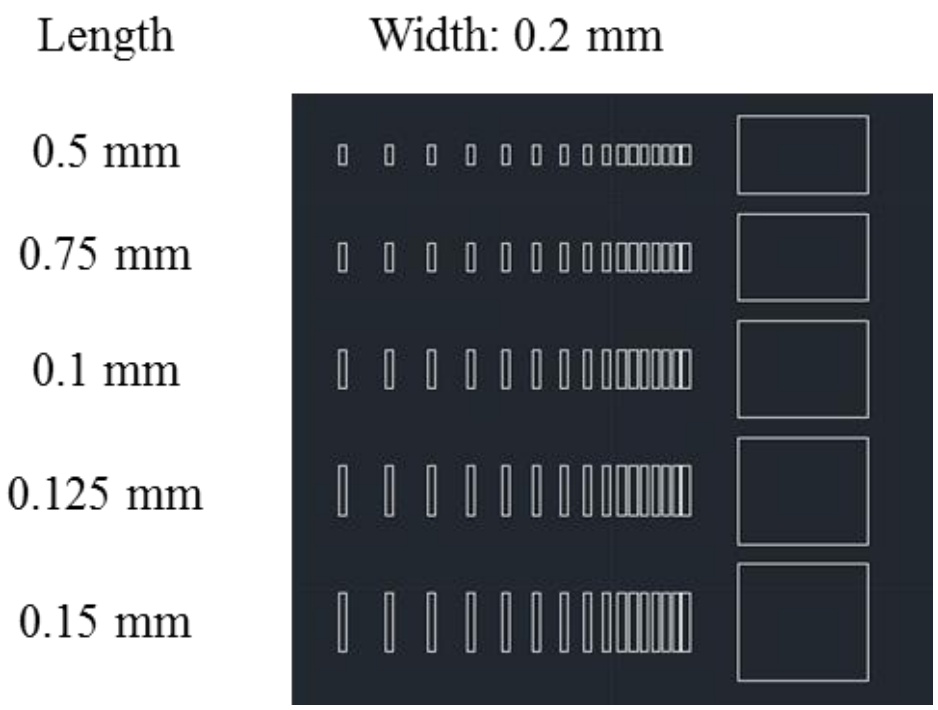


Figure 4.2 Schematic showing the design of the PCB pads for the solder bridging test.

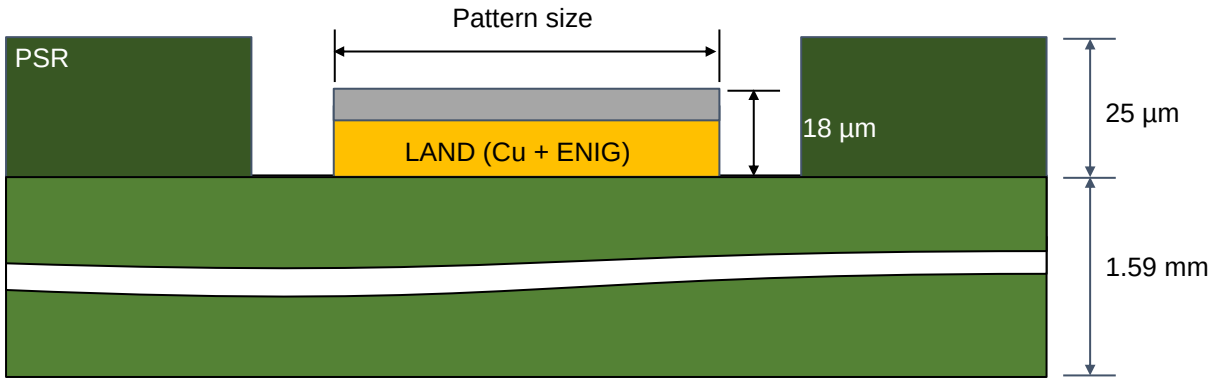
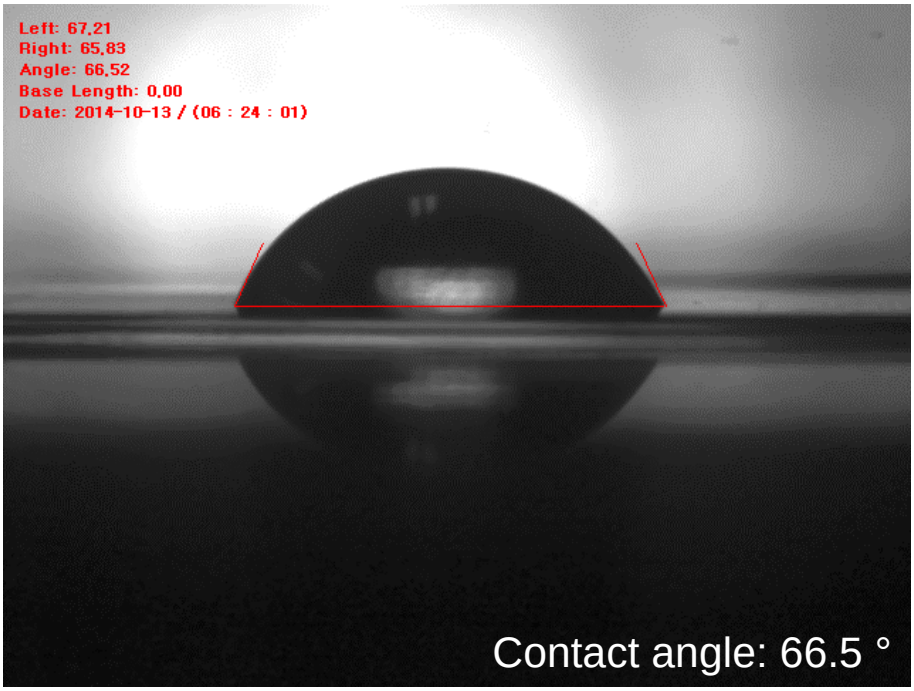


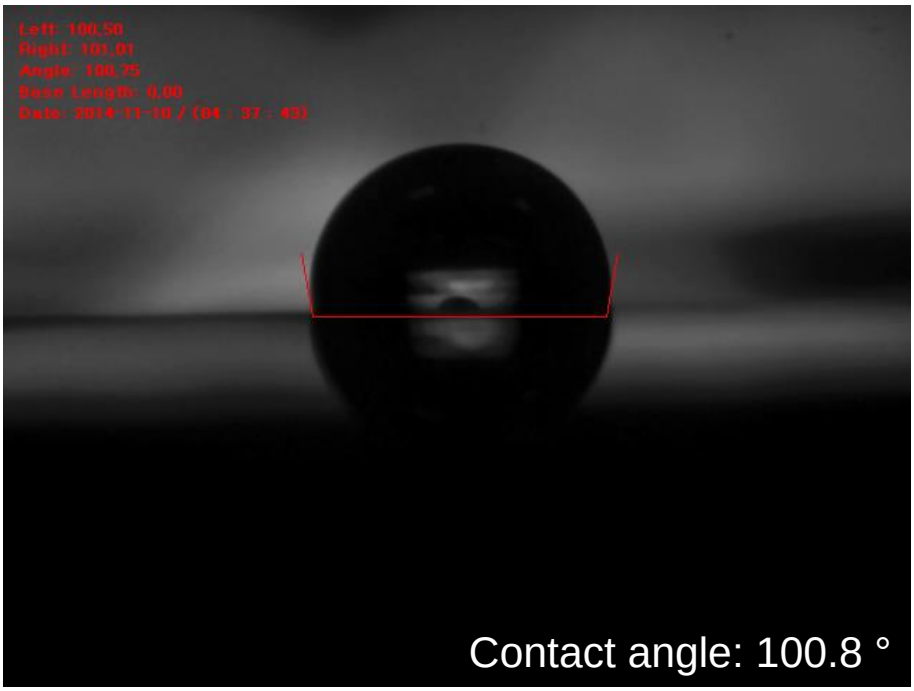
Figure 4.3 Schematic of the cross-section of the test PCB.

Table 4.1 Printing parameters.

Printing parameters	Setting value	Unit
Squeezing speed	40	mm/s
Squeeze angle	45	°
Clearance	-0.5	mm



(a)



(b)

Figure 4.4 Water droplet test images of the (a) uncoated and (b) coated stencils, showing the contact angles.

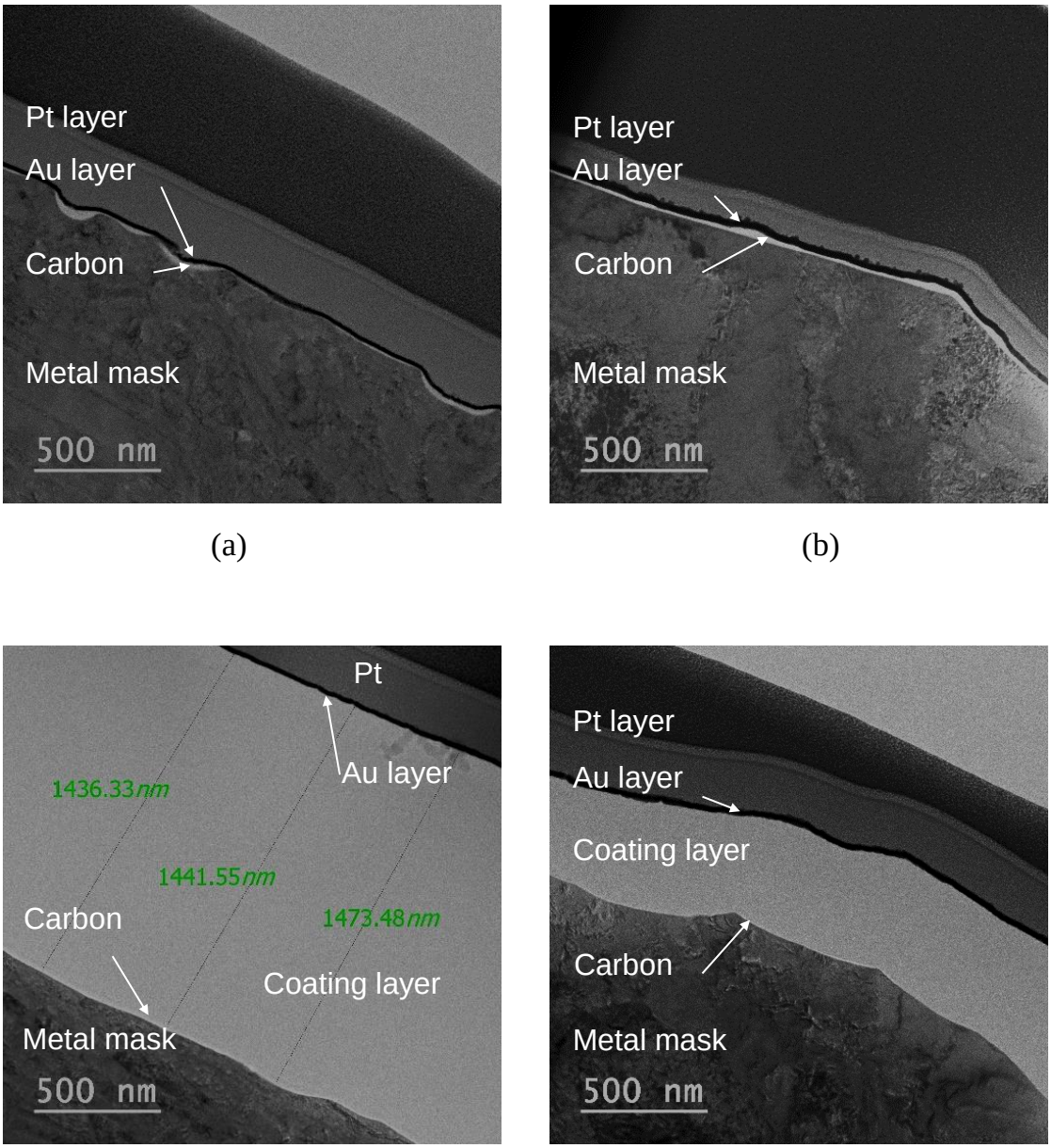


Figure 4.5 Cross-sectional TEM micrographs of the SUS304 laser-cut stencil: (a) uncoated stencil surface, (b) uncoated stencil aperture wall, (c) coated stencil surface, and (d) coated stencil aperture wall.

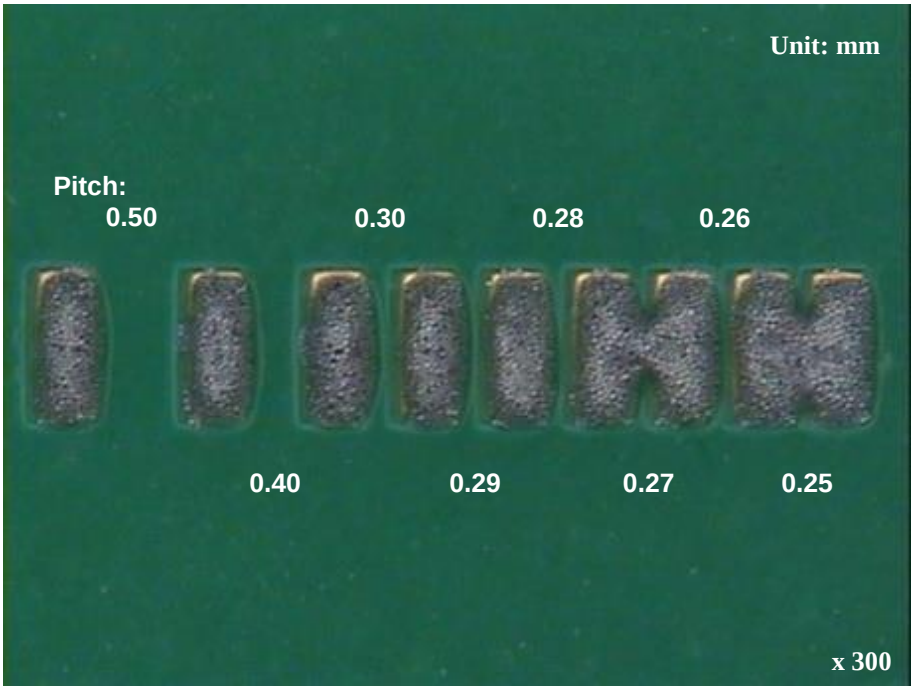


Figure 4.6 Optical micrograph of the solder bridging test sample.

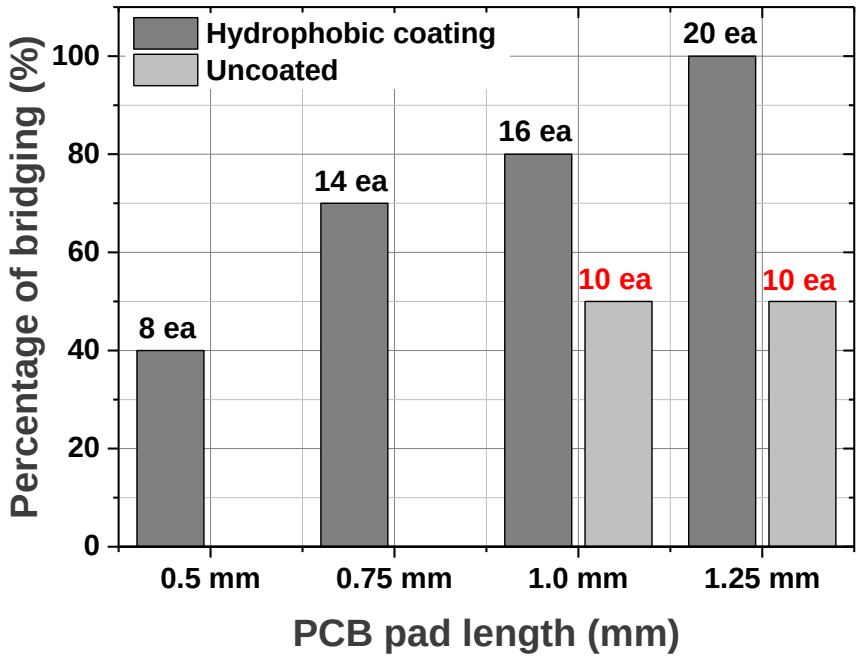
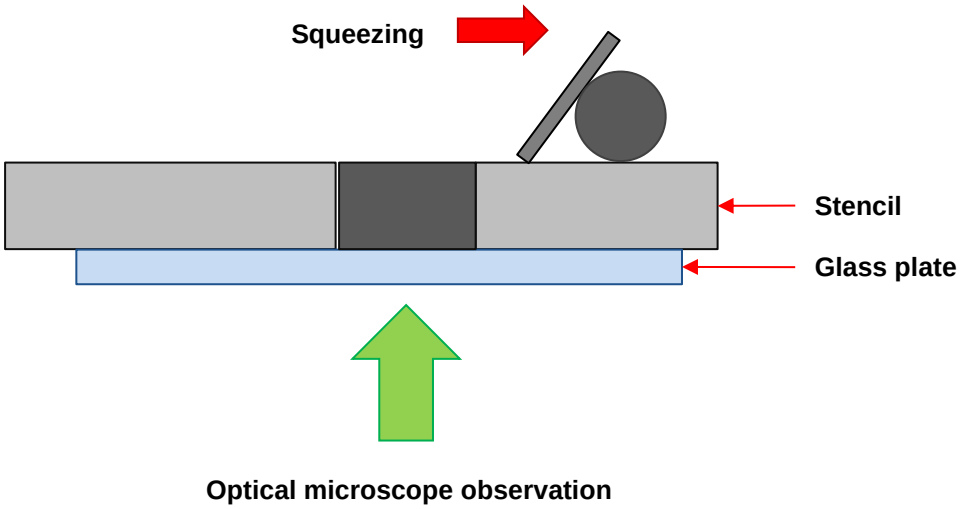
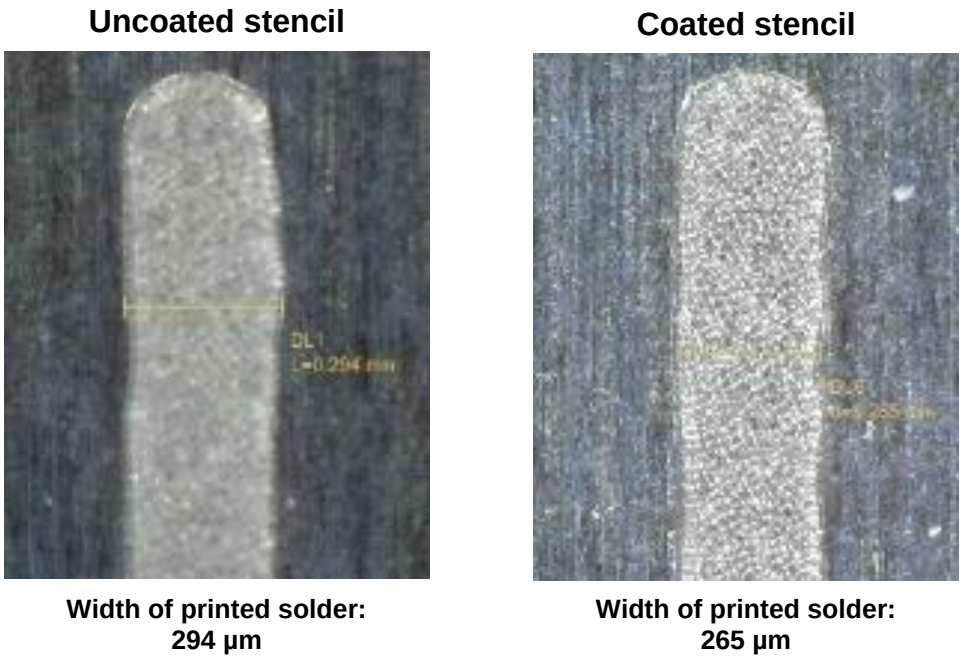


Figure 4.7 Percentage of bridged pads as a function of pad length for uncoated and coated stencils.

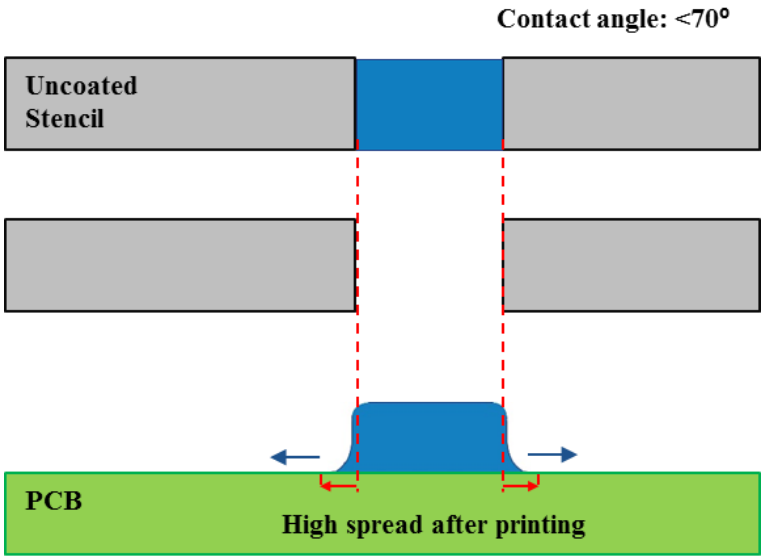


(a)

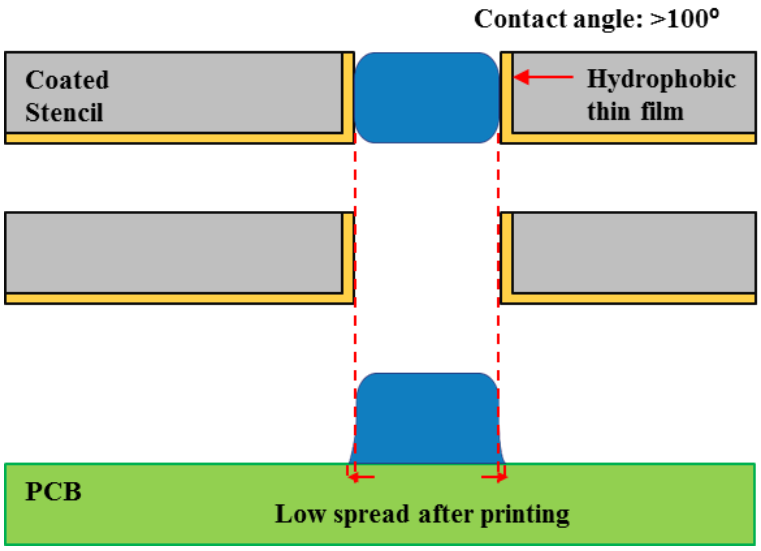


(b)

Figure 4.8 (a) Schematic showing observation of solder paste printing through the glass plate. (b) Micrographs of the printed solder paste observed through the glass plate for uncoated and coated stencils.



(a)



(b)

Figure 4.9 Schematics showing the solder printing process through (a) an uncoated stencil and (b) a coated stencil.

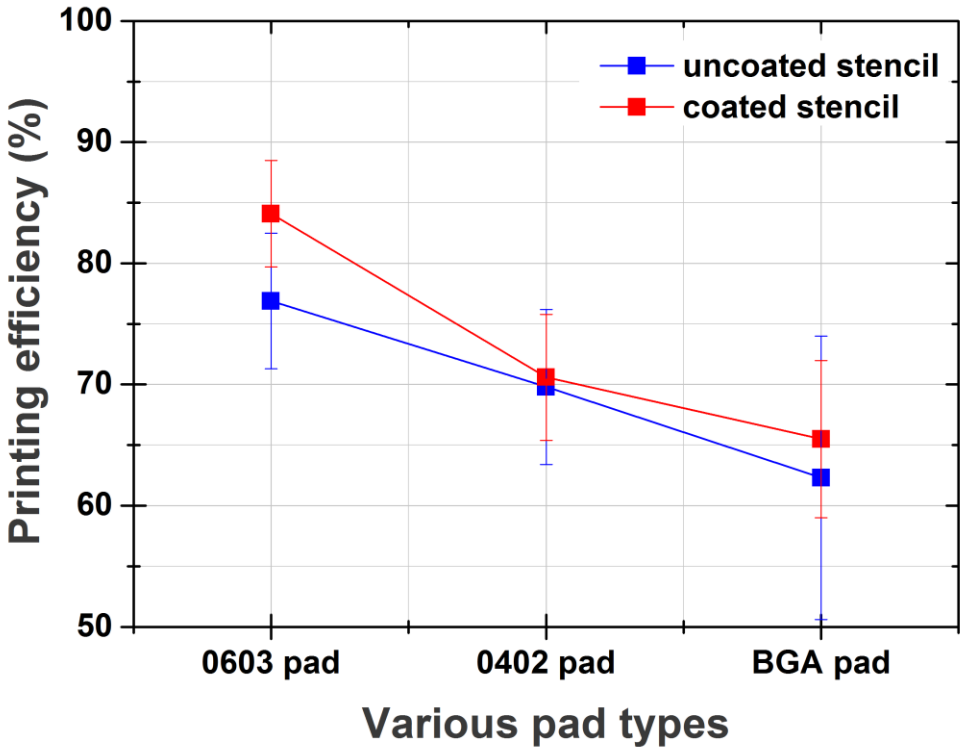
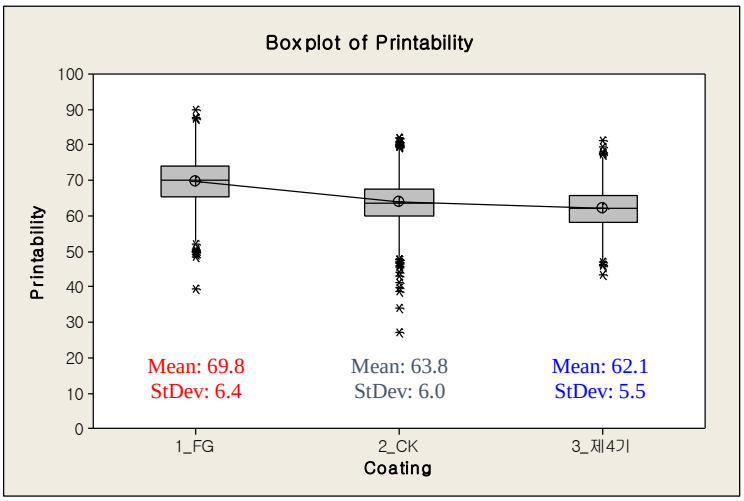
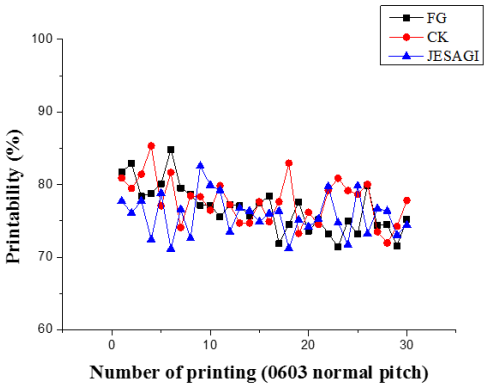
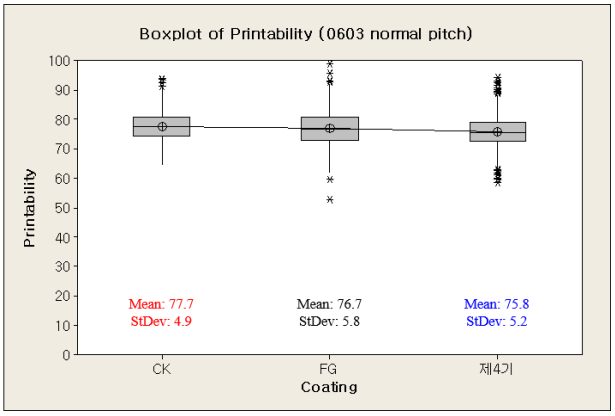
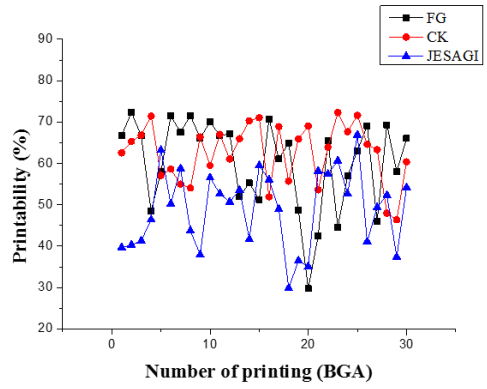


Figure 4.10 Printing efficiency for uncoated and coated stencils as a function of pad type.









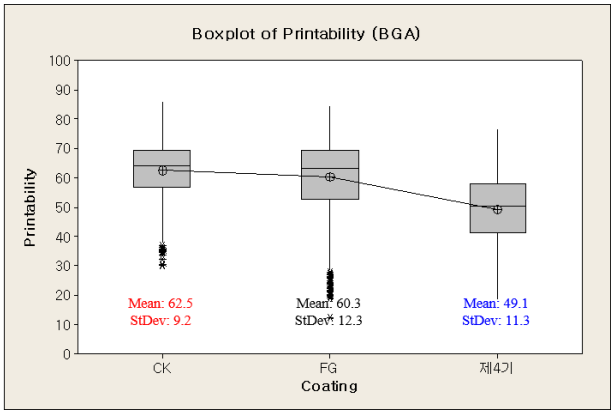
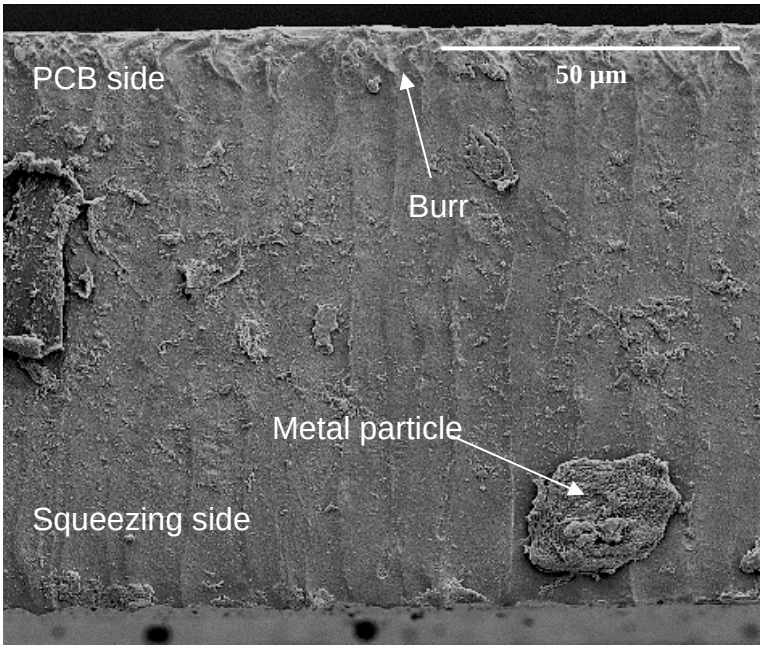
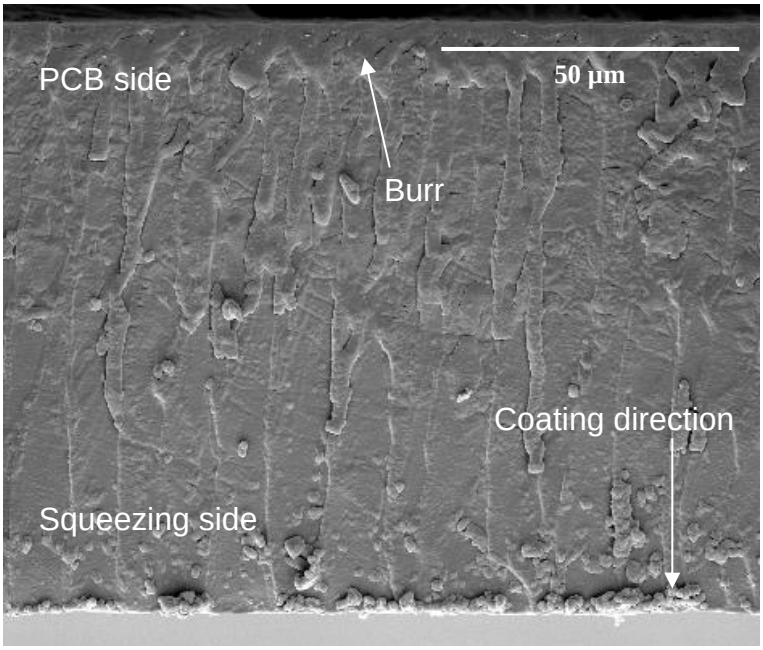


Figure 4.11 Results of continuous printing with various pad types.



(a)



(b)

Figure 4.12 SEM micrographs of the microstructure of the side walls of the aperture for (a) uncoated and (b) coated stencils.

Table 4.2 Surface roughness of the aperture wall measured by AFM for uncoated and coated stencils.

	PCB side (upper)	Middle side	Squeezing side (lower)
Uncoated stencil	255.5 nm	27.5 nm	125.4 nm
Coated stencil	302.6 nm	66.0 nm	119.8 nm

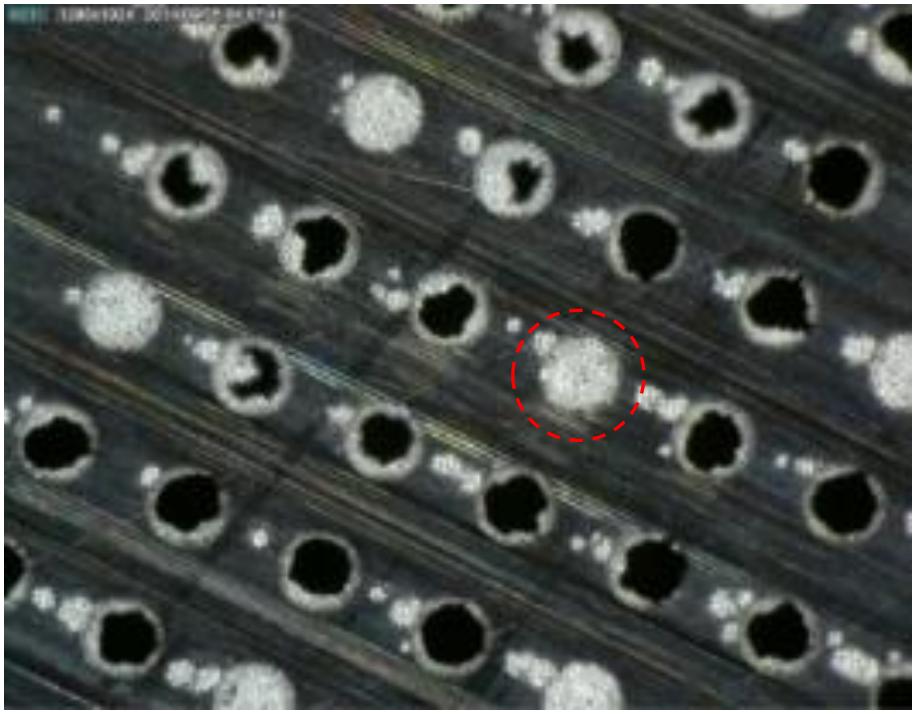
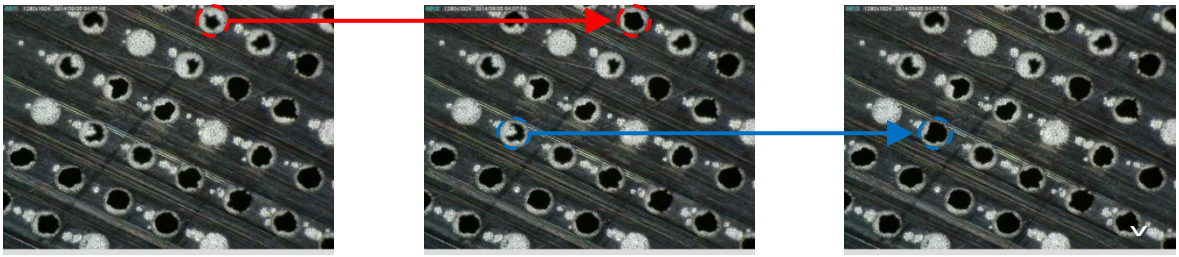
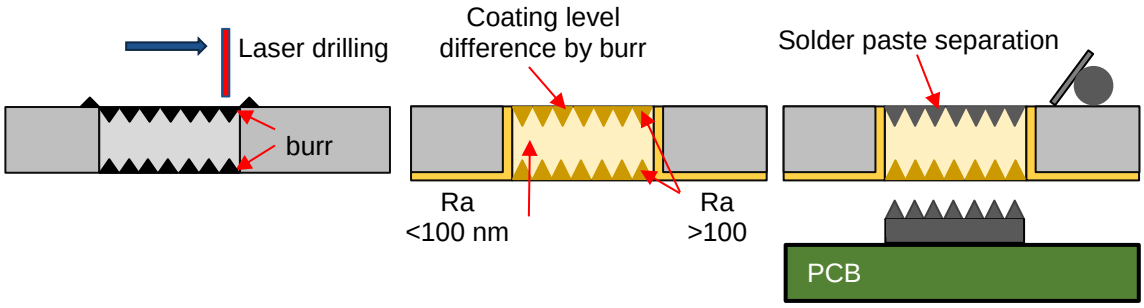


Figure 4.13 SEM micrograph showing solder paste adhering to the squeezing side of the aperture.



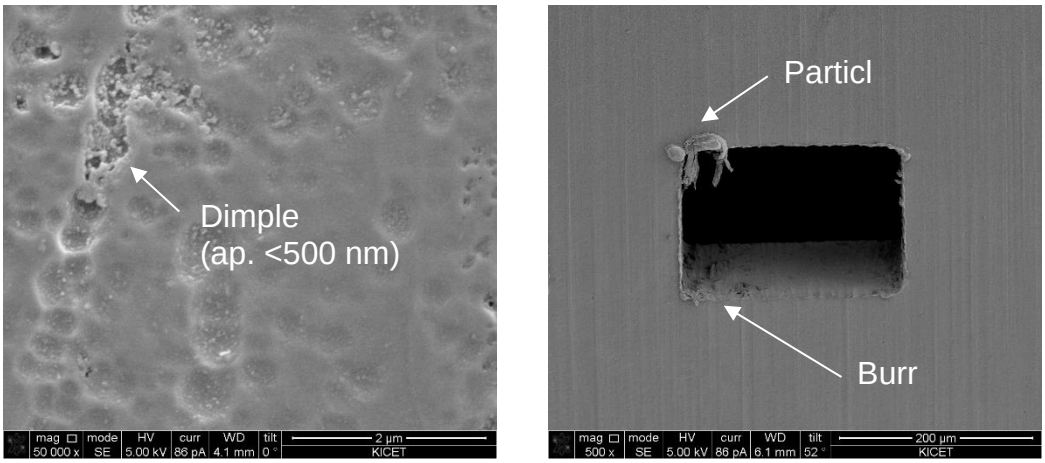
(a)



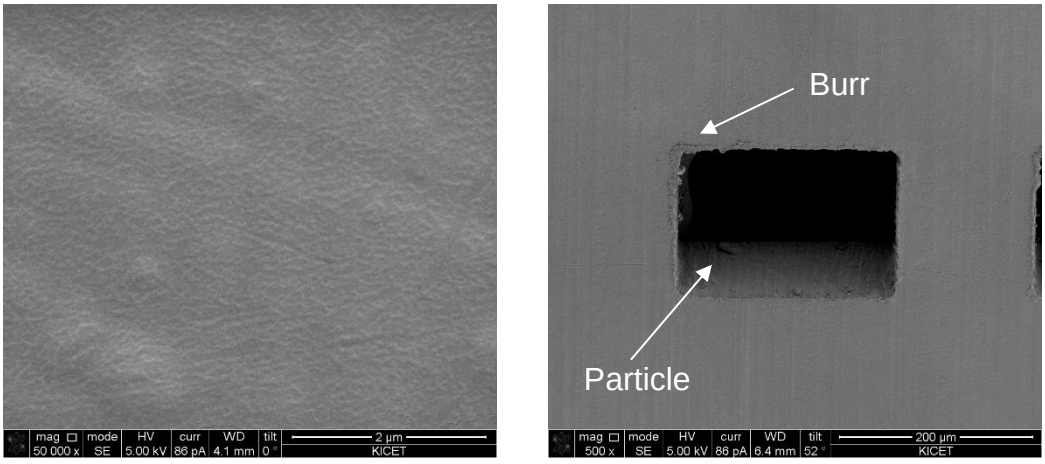
Solder paste friction force > Solder paste viscosity = Solder paste separation

(b)

Figure 4.14 (a) SEM micrographs of … . (b) Schematic of solder paste separation.

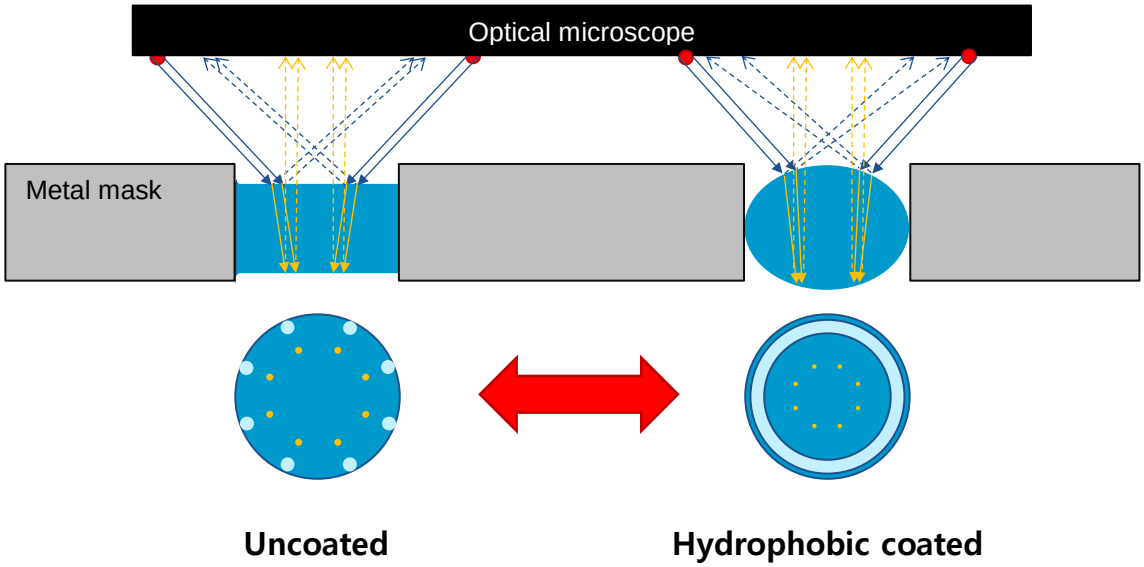


(a) Uncoated stencil

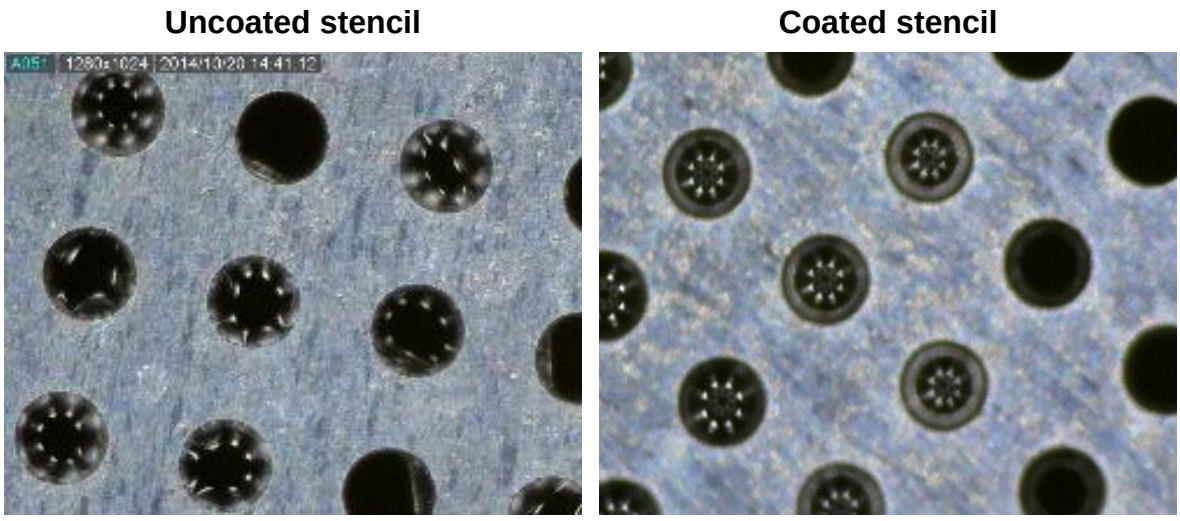


(b) Coated stencil

Figure 4.15 SEM micrographs of the surface and aperture of (a) uncoated and (b) coated SUS stencils.



(a)



(b)

Figure 4.16 (a) Schematic of the method for verifying the quality of the hydrophobic coating using an LED lamp. (b) SEM micrographs showing the different optical patterns for the uncoated and coated stencils.

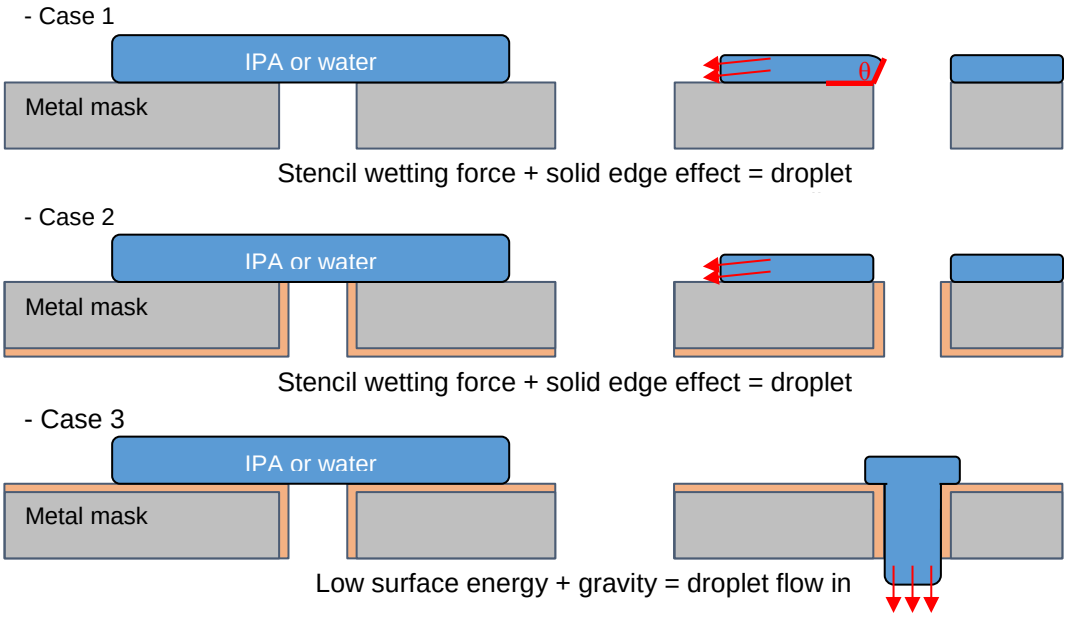


Figure 4.17 Schematic diagram showing the method for verifying the quality of the hydrophobic coating based on the solid edge effect.

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using surface tension and solid edge." *Sensors and Actuators A: Physical*, 139, pp. 343-349.

Chapter 5

Conclusions

In electronic packaging, the IMCs and interfacial reactions at the interface between the solder and substrate material can affect the reliability and properties of the solder joint. The substrate materials and surface-finishing materials on the joint pad can determine the interfacial reactions and IMCs formed, which affect the reliability and properties such as brittle fracture and shear strength after reflowing and during use of the device. Moreover, the requirements for high performance and high component density in electronic packaging are growing. Thus, a reduction in the stencil aperture size for solder printing on the surface-treated substrate is also important. In high-density electronics the decreasing stencil aperture size degrades solder printability, which results in processing failures during soldering. Therefore, a new technology is required for improving the solder printability. In this dissertation, new methods and approaches were demonstrated for improving the properties of the solder joint in electronic packaging.

In Chapter 2, the effect of the bath life of Ni(P) in ENIG on the brittle fracture behavior of the SAC solder joint was investigated. During reflow, the thicknesses of

the $(Cu,Ni)_6Sn_5$ and P-rich layer for 0 MTO were higher than that for 3 MTO. The 3 MTO sample showed large shallow pits at the interface between $(Cu,Ni)_6Sn_5$ and Ni(P) after reflow. The pitted region of the 3 MTO sample possessed a thick P-rich layer and the large pits of the 3 MTO sample possibly enhanced Ni diffusion, resulting in the formation of a thick $(Cu,Ni)_6Sn_5$ layer. The brittle fracture behavior of the 0 MTO sample was superior to that of the 3 MTO sample. During HSS tests, the fracture normally occurred at multiple sites in the $(Cu,Ni)_6Sn_5$, Ni-Sn-P, and P-rich layers. However, the 3 MTO sample showed circular features on the brittle fracture surface which were identified as exposed P-rich layers. The size of the nanovoid in the Ni-Sn-P layer was higher in the 3 MTO sample than in the 0 MTO sample. The weak interfacial microstructures (thick P-rich layer and large nanovoids) appeared to increase the brittle fracture rate of the 3 MTO sample.

In Chapter 3, the effects of multiple heat treatments (reflows) on the wettability, interfacial reactions, and mechanical reliability of the interface between the SAC305 solder and plasma-finished PCBs were investigated and compared to those for the SAC305/OSP system. For wetting and spreading tests, the plasma-finished samples had higher wetting forces and shorter zero-cross times compared with the OSP surface finish. The wetting force (and hence solderability) was not dependent on the number of heat treatments for the plasma surface finish, whereas the wetting force for the OSP surface finish rapidly decreased with increasing number of heat treatments. In the case of the multiple heat-treated OSP sample, the wetting reaction did not occur due to the

degradation of the OSP. The plasma layer was uniformly coated on the Cu pad with a thickness of about 20 nm and removed by the combined action of the flux and the high reflow temperature during the reflow process. In that case, the Cu layer was in direct contact with the molten solder, resulting in the formation of Cu-Sn IMCs at the interface. Thus, in the reflow reaction with the SAC305 solder, differences in the morphology and thickness of the interfacial IMCs for the two surface finishes were not observed. From ball shear tests, it was found that the shear force for the plasma substrate was consistently higher than that for the OSP substrate. In the case of the plasma substrate, the shear force was independent of the number of reflows, while it decreased rapidly after five reflow cycles for the OSP substrate. The poor wettability, reduced bonding area, and void formation of the OSP finish after multiple heat treatments could degrade the joint properties. These results clearly indicated that the plasma surface finish was superior to the conventional OSP finish with respect to wettability and joint reliability.

In Chapter 4, solder printing efficiency and solder bridging rate were evaluated for hydrophobic-thin-film-coated stencils. The printing efficiency of coated stencils was higher than that of uncoated stencils. The printing efficiency increased with increasing pad size, regardless of the hydrophobic coating. SEM observations of the aperture wall showed that the roughness of the top and bottom edges was higher than that of the inside. This roughness resulted in the solder paste adhering to the aperture wall and degraded the expected enhancement in printing efficiency from the hydrophobic

coating. Moreover, the solder bridging rate of the coated stencil was lower than that of the uncoated stencil. The pattern of the printed solder paste using the coated stencil was narrower than that using the uncoated stencil; this reduced spreading was attributed to the increased surface tension of the solder paste using the coated stencil. Therefore, The hydrophobic thin film coating on the stencil could reduce undesirable bridging.