# 原子オーダ平坦化シリコンの形成方法とその応用に関する研究

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# 論文内容要旨


The interface micro-roughness between gate oxide film and silicon substrate is one of the critical issues to the gate oxide film reliability and the performance of Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs). Especially with the device size shrinkage, the gate insulator films have been becoming thinner, which induces the effects of the electric field concentration due to the interface roughness increasing. It has also been known that, with the interface roughness suppressing, the current drivability, 1/f noise, and the lifetime and the breakdown characteristics of insulator films can be improved. The atomically flat interface has been proved to be usefully for the device characteristics improvement. However, the applications of these technologies are very difficult. In this dissertation, the low temperature atomically flattening for the large scale wafer has been developed and the application technologies have been investigated. The approaches include the low temperature atomically flattening technologies, single wafer cleaning technologies for atomically flat wafer, and the high reliable gate insulator films formation. All of these new process technologies can be applied to LSI fabrication on large scale wafers. There are 4 chapters in this dissertation.

The first chapter is introduction.

In chapter 2, technologies to realize low temperature atomically flattening on large scale wafers have been investigated. New vertical furnace which can realize ultra pure annealing ambient by suppressing the $H_2O$ and $O_2$ back diffusion from atmosphere has been developed. After annealing in Ar ambient above 800 °C, atomically flat surface appeared on the whole 200 mm wafer of Si(100). On the atomically flat surface, the average height of the steps is 0.135 nm, and on terrace, the atomically flat surface can be formed, shown as in Fig. 1. It has been found that only after annealing below 900 °C, slip-line defect cannot be generated in wafers. Atomically flattening is the Si atoms migrations of the surface layers, depends on the $H_2O$ and $O_2$ concentrations in Ar ambient, and is independent of wafer off angles. From the former research, only after annealing at ultra pure Ar ambient, the atomically flat surface can be formed.

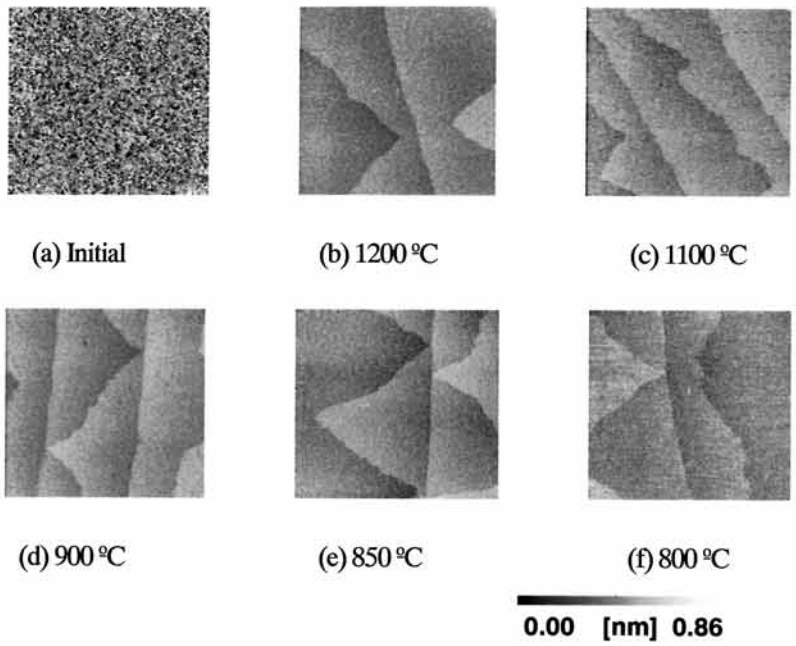


Figure 1. 1 μm × 1 μm AFM images of samples before and after annealing in Ar ambient at 1200 ºC, 1100 ºC, 900 ºC , 850 ºC and 800 ºC, respectively. The annealing time are 1hour at (b) 1200 ºC, (c) 1100 ºC, (d) 900 ºC, 9 hours at (e) 850 ºC, and 80 hours at (f) 800 ºC, respectively.

Atomically flattening speed can be increased by annealing at higher temperature or improving the gas-replacement efficiency near the wafer surface. After annealing in vertical furnace, atomically flat surface is formed at wafer edge and enlarge to the whole surface, due to the different gas-replacement efficiencies near the wafer surface. Increasing the As gas supply flow rate and widening the gap distance between wafers can reduce the $H_2O$ and $O_2$ concentrations near the wafer surface, and result in shortening the atomically flattening time for the whole surface. It is considered that by improving the gas flow pattern of the vertical furnace, the atomically flattening speed can be increased even with narrow space between wafers and low Ar gas supply flow rate. The cleaning process to fabricate device on atomically flat surface has been developed. Besides the alkali cleaning solution, the cleaning ambient has also effects on maintaining surface flatness. It is found that only cleaning in dark and $N_2$ ambient, the surface flatness can be maintained as before. For the single wafer spin cleaning process, with increasing the $O_2$ concentration in cleaning ambient, after cleaning, water marks appear easily on surface and are difficult to be removed. For large scale atomically flat wafers, new cleaning method in $N_2$ and dark ambient of spin cleaning has been found. It has been found that spin cleaning has different particle removal effects from batch cleaning. Not only the zeta potential, but also the hydrophobic surface is very important for particles removal. Without surfactant and megasonic, only FPM (0.5% HF, 1% $H_2O_2$) or DHF (0.5% HF) can remove particles. And the cleaning time for particle removal can be reduced to be 15 sec. This new cleaning method also has high metal and organic contamination removal effects. $H_2O_2$ is found to be necessary for metal contamination removal. After cleaning the metal impurities contaminated wafers by $O_3$-UPW of 30 sec, FPM (0.5% HF, 1% $H_2O_2$) of 30 sec, and $H_2$-UPW rinse of 30 sec, all the metal remaining is below $1 \times 10^{10}$ atoms/cm$^2$,

including Fe, Ni and Cu, which are very difficult to be removed, due to the high redox potentials. For the organic impurities contaminated wafers, after cleaning, the remaining is same as the ones without any organic contaminations. Moreover, the atomically flat surface can be maintained as before even after cleaning by DHF (0.5%HF) for 5 min at dark and $N_2$ ambient, shown in Fig. 2. Therefore, this new cleaning method can be applied to device fabrication on large scale atomically flat wafers. For gate oxidation method, it is confirmed that only after radical oxidation, the interface flatness can be maintained. Consequently, the combination of the low temperature atomically flattening technology, the new spin cleaning technology and the radical oxidation can be applied to LSI manufacturing.

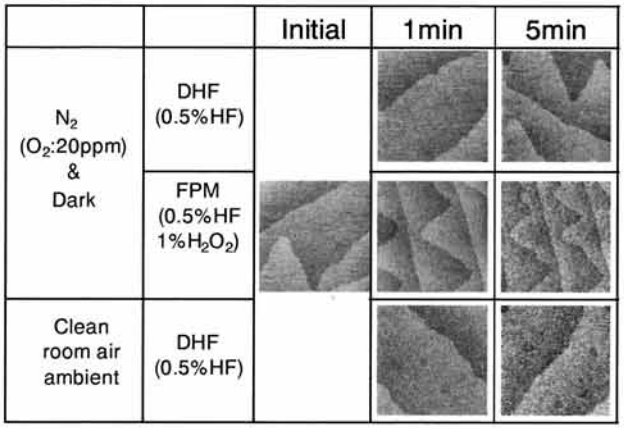


Figure 2. . 1 μm × 1 μm AFM images of samples before and after cleaning in dark and $N_2$ ambient by DHF(0.5%HF) and FPM (0.5%HF, 1%$H_2O_2$), and cleaning in clean room air ambient with light irradiation by DHF(0.5%HF), for 1 and 5 min, respectively.

Chapter 3 is about the formation of the high performance gate oxide film on atomically flat wafers, and the application technologies of atomically flattening process to LSI manufacturing. By utilizing the new cleaning technologies, capacitors have been fabricated to evaluate the gate oxide reliabilities, including $E_{bd}$ and $Q_{bd}$. The electrical field concentrates at the roughened areas. Therefore, for the capacitors owing radical oxide films, improving the interface flatness can improve the $E_{bd}$ and $Q_{bd}$, and much higher than the ones owing conventional thermal wet oxide films. Only fabricated by radical oxide film and owing atomically flat interface, $E_{bd}$ and $Q_{bd}$ can be drastically improved to be highest with much smallest variations, shown in Fig. 3. Forming the radical oxide films on conventional flat wafers, many defects are generated, due to the flattening effects on the roughened areas. From the simulation results, after isotropic oxidation on the roughened surface, the electric field concentration occurs at the valley areas of the roughened interface. With the stronger flattening effects, the electric filed concentration increased. For the radical oxidation which has higher flattening effects than the conventional wet oxidation, after oxidation, the initial failures occur. These results confirm that the radical oxidation can only be applied as gate oxide films for the device owing atomically flat interface. After $Q_{bd}$ measurement, the breakdown points were investigated by Infra Red Optical Beam Induced Resistance Change (IR-OBORCH). For the capacitors owing conventional

flat interface and radical oxide or wet oxide films, the breakdown spots randomly appear in the gate regions, and for the ones owing atomically flat interface and radical oxide, the breakdown spots appear only at the edge and corners of the gate regions. The reasons are considered of the fabrication process, including the field oxide isolation by Non-doped Silicon Glass (NSG), and the gate oxidation after active area formation. The deterioration of the oxide film at the edge areas and the electric field concentration at the edge and corner cause the decreasing of the breakdown characteristics at these regions. It is considered that the $E_{bd}$ and $Q_{bd}$ of the capacitors owing atomically flat interface and radical oxide should be larger by suppressing the electric field at edge and corner areas. Atomically flattening above 800 °C, COPs in wafer substrate can be effectively removed, same as at 1100 °C, and equivalent $Q_{bd}$ values can be obtained. The atomically flattening technologies can be applied for silicon-on-insulator (SOI) wafer flattening. After annealing in Ar ambient at 850 °C, SOI wafer can be atomically flattened without change of SOI layer thickness. After atomically flattening, the off angle which calculated by the terrace widths are larger than the specification values. And the variations of the off angles on the whole surface are also large. These results indicate that the off angle of the SOI wafers is very difficult to be controlled during wafer manufacturing. With less $O_2$ degasification isolation layer, i.e. thermal wet oxide films formed at 1000 °C, the active Si regions of patterned wafer can be atomically flattened at 900 °C. The patterned wafer atomically flattening can much reduce the LSI manufacturing process steps on atomically flat wafers.

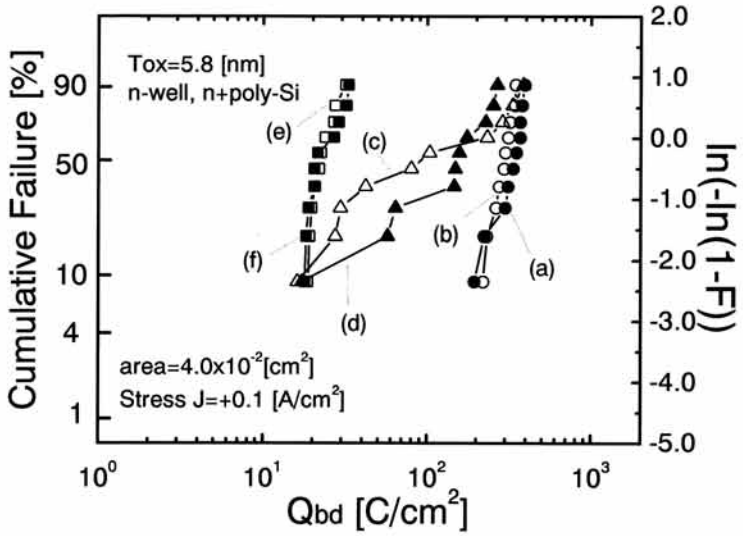


Figure 3. Weibull plot $Q_{bd}$ with radical oxide film on atomically flat surface by annealing in Ar ambient at (a) 1100 °C and (b) 800 °C, (c) conventional surface, (d) roughened atomically flat surface, wet oxide film (e) on atomically flat surface by annealing in Ar ambienr at 1100 °C, and (f) conventional flat surface, respectively. The measured area is $4.0 \times 10^{-2}$ cm$^2$.

Chapter 4 is the conclusion.

From the above results, the technologies are new developed and, including the low temperature atomically flattening technologies, the cleaning process for the device manufacturing on atomically flat surface, and the gate oxide reliabilities of $E_{bd}$ and $Q_{bd}$. These technologies are very available for the high performance LSI manufacturing

# 論文審査結果の要旨

シリコン集積回路において，ゲート酸化膜とシリコン基板間の界面ラフネスは，金属－酸化膜－半導体電界効果トランジスタ（MOSFET）の性能・信頼性を決定する重要な要因の一つである．昨今，MOSFET の微細化に伴いゲート絶縁膜の薄膜化が進み，ゲート長が 45nm の微細化世代において，Effective Oxide Thickness (EOT)は 1.0nm 程度まで薄膜化されてきており，界面ラフネスが一層強くトランジスタの性能・信頼性に影響を及ぼす状況になってきている．界面ラフネスの抑制は，電流駆動能力向上，低周波雑音低減，および絶縁膜寿命と絶縁破壊耐性の向上のために必要不可欠な開発課題である．これまでに，約 1200°C 程度の熱処理によるゲート酸化膜とシリコン基板の界面の原子オーダー平坦化が実現されており，原子オーダー平坦化界面はデバイス特性の改善に極めて有用であることが報告されているが，こうした高温の平坦化技術は現状の大口径ウェーハを使用する LSI 製造への応用が困難であった．本論文は，大口径ウェーハに適応可能なシリコンウェーハの原子オーダー平坦化技術と，その応用技術についてまとめたものであり，全文 4 章からなる．

第 1 章は，序論である．

第 2 章では，シリコンウェーハ原子オーダー平坦化と製造工程中でその平坦面を維持するための洗浄，酸化技術について述べられている．まず，酸素・水分濃度を 10ppb 以下に抑制した新しい熱処理装置を開発し，900°C 以下の温度でも Ar ガスアニールより，直径 200mm の Si(100)ウェーハがスリップライン欠陥の発生なしに全面原子オーダーで平坦化できることを明らかにしている．また，大口径原子オーダー平坦化ウェーハに適用可能な新しい枚葉洗浄装置を開発し，遮光かつ窒素雰囲気中で非アルカリ液を用いることにより，形成した原子オーダー平坦表面を維持しながら洗浄できることを明らかにしている．さらに酸素ラジカルを用いた 400°C 程度のシリコン酸化膜形成技術により，原子オーダー平坦面を維持しつつゲート絶縁膜を形成できることを明らかにしている．これらは，大口径シリコンウェーハ上に微細 MOS トランジスタを製造する上で，極めて重要な成果である．

第 3 章では，第 2 章で述べた原子オーダー平坦化技術を応用して作成した素子の電気的特性と Silicon on Insulator （SOI）ウェーハや $SiO_2$ パターン付きウェーハの原子オーダー平坦面形成について述べている．まず，試作した MOS キャパシタのゲート酸化膜の信頼性を評価している．原子オーダー平坦表面に形成した MOS キャパシタは，従来の素子に比べ，絶縁破壊電界強度が向上するとともに，初期故障が発生せず真性寿命が向上することを明らかにしている．ここで，シリコンウェーハが原子オーダー平坦化される際に，表面層の Crystal originated particles（COP）が除去され電気的特性を向上させていることも見出している．さらに，従来の 1200°C 程度の高温平坦化処理では不可能であった SOI ウェーハの原子オーダー平坦化が，シリコン層の厚さも変化させずに実現できることを明らかにしている．また， $SiO_2$ パターン付きウェーハ上のシリコン領域を原子オーダーで平坦化することも成功した．SOI ウェーハや $SiO_2$ パターン付きウェーハにおいて原子オーダー平坦化を実現したことは，超微細高集積 LSI 製造への適用が可能であることを示すものである．これらは，極めて有用な成果である．

第 4 章は，結論である．

以上要するに本論文は，大口径ウェーハに適応可能なシリコンウェーハの原子オーダー平坦化技術とその応用技術についてその成果を明らかにしたものであり，半導体工学の発展に寄与するところが少なくない．

よって，本論文は博士（工学）の学位論文として合格と認める．