A Study on Ultra High-Speed and Low Noise MOS Transistor Structures

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授与学位	博士（工学）
学位授与年月日	平成１８年３月２４日
学位授与の根拠法規	学位規則第４条第１項
研究科，専攻の名称	東北大学大学院工学研究科（博士課程）電子工学専攻
学位論文題目	A Study on Ultra High-Speed and Low Noise MOS Transistor Structures (超高速・低ノイズMOSトランジスタ構造に関する研究)
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論文内容要旨

Since the beginning of the integrated circuit (IC) era in 1959, the IC scale expanded from LSI (large-scale integration), VLSI (very large-scale integration) to ULSI (ultra large-scale integration). Historically, device scaling shrinking, quantified by Moore's law, realizes both the cost-down and enhanced performance. However, with reducing the device size into submicron or deep submicron region, there are some limitations, such as mobility degradation and flicker noise, we have to overcome. To breakthrough the limits of semiconductor devices, the purposes of this research are to indicate the solutions for the high-speed and lower 1/f noise semiconductor devices and elucidate the physical mechanism. And we will do the prediction of the limits of the devices for future else.

In Chapter 2 the device structures and characteristics of accumulation-mode MOSFETs on Si(100) are described. The novel CMOS structures consisted of inversion and accumulation mixed-mode will be shown. The mechanism the device is elucidated. In Chapter 3 it is experimentally shown the characteristics of accumulation-mode FD-SOI fabricated on Si(110) surface. The behavior and mechanism of accumulation-mode on different silicon surface orientation are shown. And at last, the predication of the limits of the devices is done and the optimized device structures for future are designed by device simulation. In Chapter 4 the characteristics of three-dimensional SOI devices are shown experimentally. And the device simulation for optimizing the device structures is done. It is shown through whole the thesis that the high-speed and low 1/f noise of semiconductor devices can be realized by using accumulation-mode at varied silicon oriented surface and FinFET. And the novel device structures are agreed with the future semiconductor devices much better than conventional inversion-mode devices. Finally, the accomplishments of this research will be summarized at Chapter 5.

In Chapter 2, the normally-off accumulation-mode FD-SOI n- and p-MOSFETs, figure 1, are fabricated successfully on Si(100) surface. It is demonstrated experimentally that the bulk body

current is existed at both the n- and p-MOSFETs fabricated on high doping SOI layer at $2x10^{17}cm^{-3}$. The current drivability increases with increase of the SOI layer doping concentration at accumulation-mode. The improved current drivability is realized by both the bulk body current component and the enhanced effective mobility due to the lower effective field at accumulation-mode is shown at figure 2. The mobility of accumulation-mode devices on low doping concentration is similar to that of inversion-mode. However, at the accumulation-mode, the coulomb scattering is much less than that at inversion layer at high doping concentration. And the mobility degradation caused by phonon scattering dependence of temperature is observed but is slighter than that at inversion. As the result, the accumulation-mode is able to provide the higher drain saturation current drivability at high temperature region and shows the better temperature characteristics compared with conventional inversion-mode. 1/f noise is reduced about one order of magnitude at both the accumulation-mode n- and p-MOSFETs, shown at figure 3 and4, on high doping concentration substrate. It is obviously that 1/f almost has no the dependence of effective filed but on the operation mode and bulk body current component. At last, the novel CMOS structures are proposed. The novel CMOS structure with accumulation-mode n-MOSFETs and inversion-mode p-MOSFETs is proposed for low 1/f noise applications and the novel CMOS structure with inversion-mode n-MOSFETs and accumulation-mode p-MOSFETs is proposed for high-speed applications.

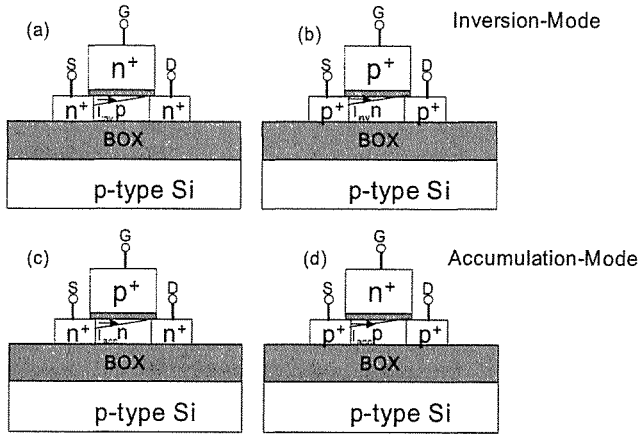

Fig. 1 Schematic of the inversion and accumulation-mode FD-SOI MOSFETs.

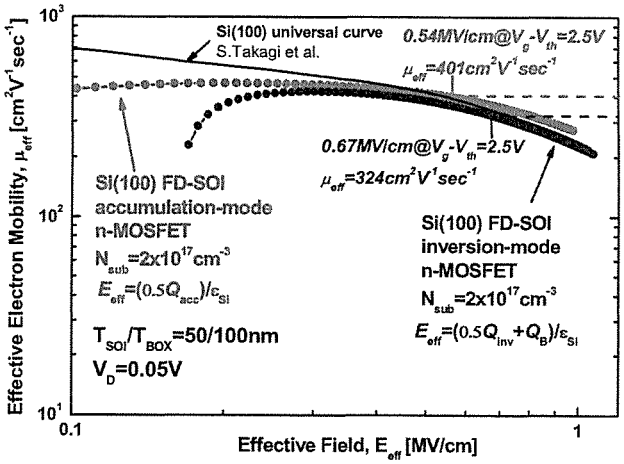

Fig.2 The effective electron mobility for inversion- and Accumulation-mode n-MOSFETs.

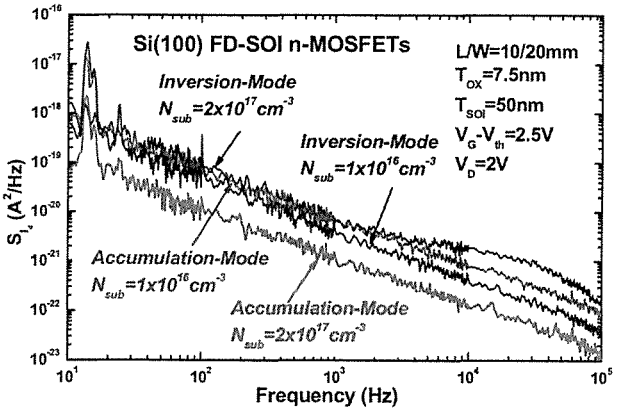

Fig.3 1/f noise characteristics for inversion-mode and accumulation-mode FD-SOI n-MOSFETs

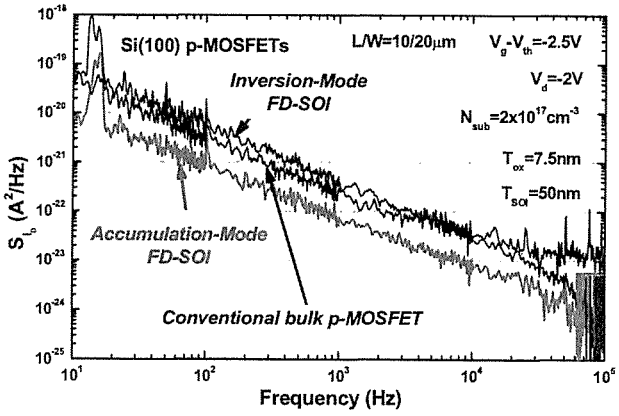

Fig.4 1/f noise characteristics for inversion-mode and accumulation-mode FD-SOI p-MOSFETs

In chapter 3, the normally-off accumulation-mode FD-SOI n- and p-MOSFETs are fabricated successfully on Si(110) surface. The current drivability increases with increase of the SOI layer doping concentration at accumulation-mode. The improved current drivability is realized by both the bulk body current component and the enhanced effective mobility due to the lower effective field at accumulation-mode n-MOSFETs on Si(110) surface. However, the current drivability improvement of p-MOSFETs is not observed by accumulation-mode due to there is no effective field dependence of hole mobility on Si(110) surface, shown at figure 5 and 6. 1/f noise is reduced at both the accumulation-mode n- and p-MOSFETs on high doping concentration substrate with $N_{sub}=5x10^{17}cm^{-3}$, shown at figure 7. At last, the novel CMOS structures are proposed. The novel CMOS structure with accumulation-mode nMOS and inversion-mode pMOS is the best solution for devices on (110) surface. The nMOS current drivability is almost as that of conversional inversion-mode nMOS on Si(100) surface. At the same time the pMOS current drivability is almost 2.5times larger than that of conversional inversion-mode pMOS on Si(100) surface, shown at figure 8.

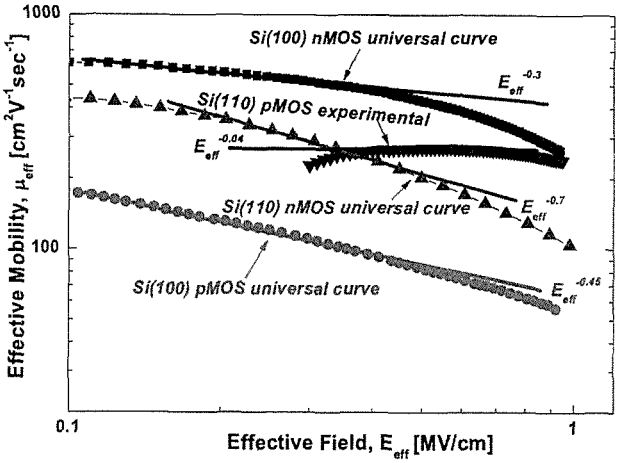

Fig.5 The effective electron and hole mobility dependence of effective field characteristics of inversion-mode on Si(100) and (110) surface.

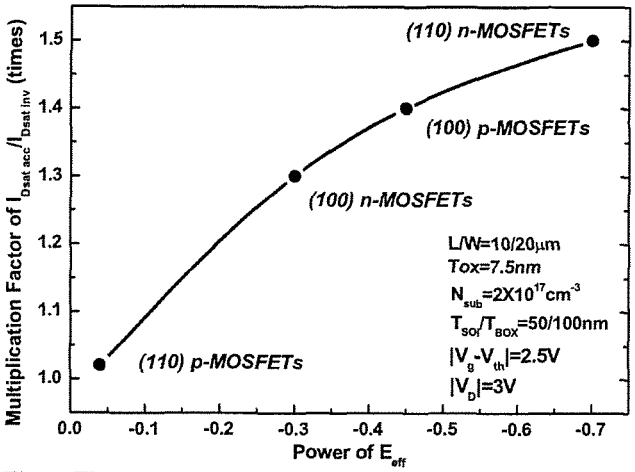

Fig.6 The relation between the multiplication factor of $I_{dsatacc}$/ $I_{dsatinv}$ and E_{eff} dependence of mobility. The stronger E_{eff} dependence of mobility induces the larger multiplication factor of $I_{dsatacc}$/ $I_{dsatinv}$.

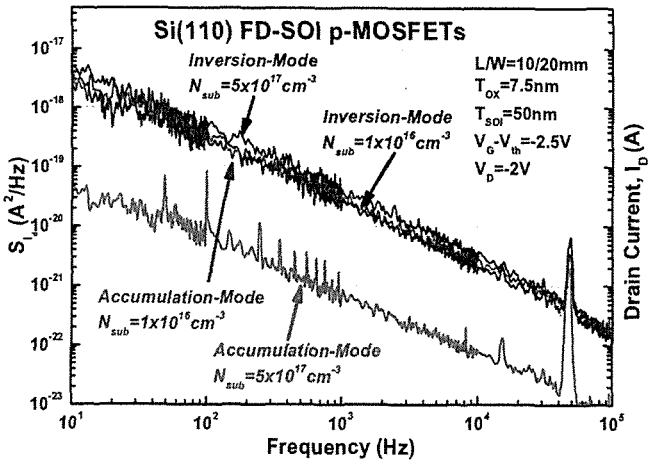

Fig.7 1/f noise characteristics for inversion-mode and accumulation-mode FD-SOI p-MOSFETs.

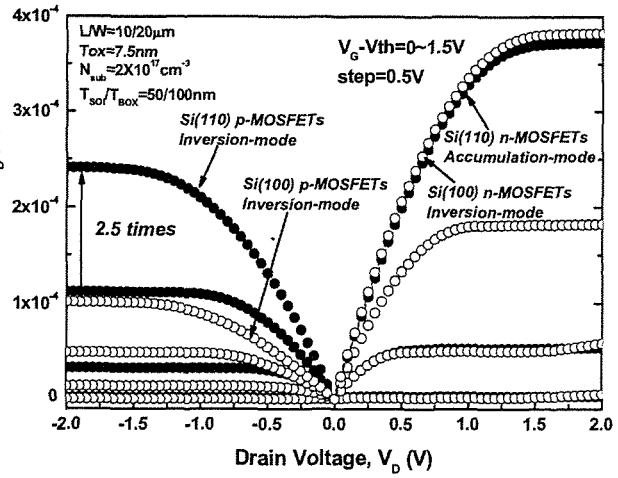

Fig.8 I_d-V_d characteristics for conventional CMOS on Si(100) and novel CMOS with Accumulation-mode nMOS and Inversion-mode pMOS on Si(110) surface.

In chapter 4, the normally-off accumulation-mode p-channel FinFETs are fabricated successfully on Si(100) surface. Figure 9 shows that ideal subthreshold slope characteristics, off-state leakage current are realized. The transconductance values at accumulation-mode p-channel FinFETs are improved from 1.8times to 3.5times compared with the accumulation-mode FD-SOI, shown at figure 10. Figure 11 shows that the current drivability for accumulation-mode p-channel FinFETs is improved 2.5times compared with the accumulation-mode FD-SOI. The accumulation-mode p-channel FinFET with Kr/O_2 gate oxide almost not shows the dependence on channel direct with the ideal S-factor values below 70mV/dec. On the other hand, accumulation-mode p-channel FinFET with thermal gate oxide shows the dependence on channel direct with the degraded S-factor values above 80mV/dec, shown at figure 12.

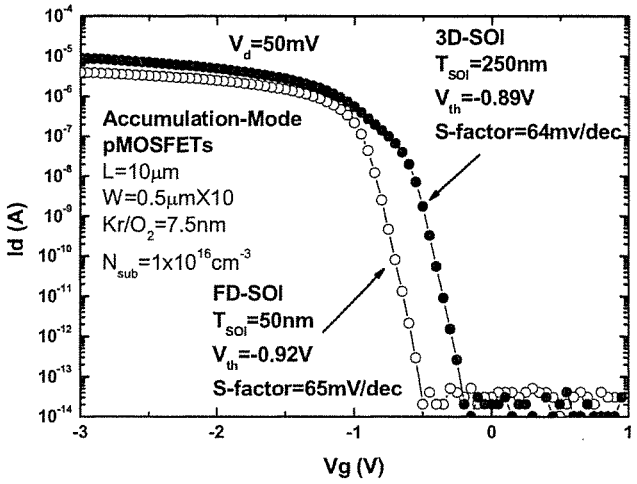

Fig.9 The I_d-V_g characteristics of both normally-off accumulation-mode p-channel FD-SOI and FinFET on Si(100) surface.

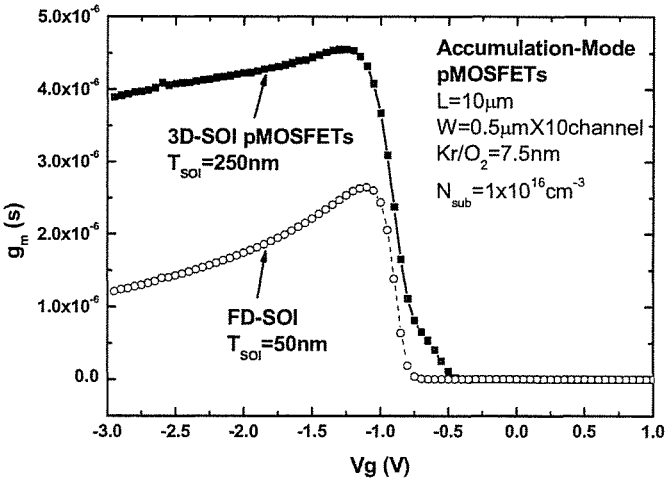

Fig.10 Characteristics of transconductance as the function of gate voltage. The values of accumulation-mode is larger than that of inversion-mode from 1.8times to 3.5times.

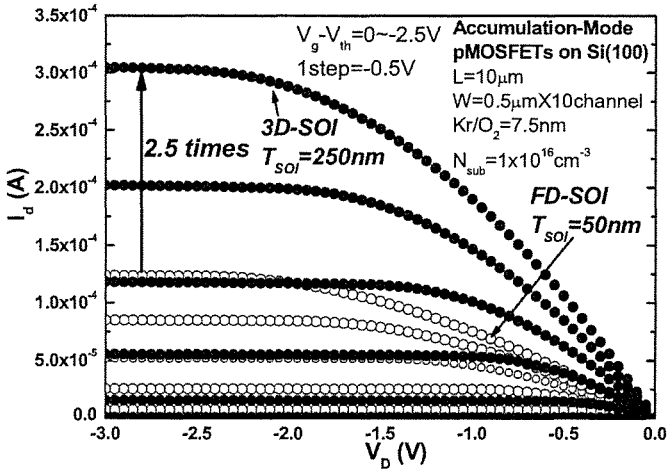

Fig. 11 The I_d-V_d characteristics for accumulation-mode p-channel FD-SOI and FinFET with the N_{sub} of $10^{16}cm^{-3}$ on Si(100) surface.

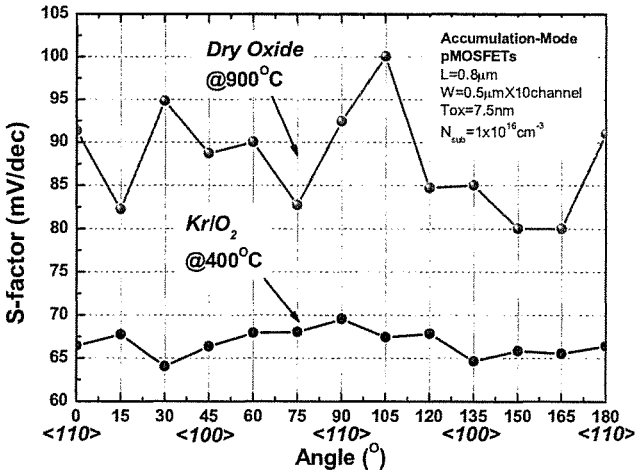

Fig. 12 The S-factor values dependence on channel direction.

論文審査結果の要旨

半導体集積回路の高性能化のためには，Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) の電流駆動能力の向上が必須である。従来は，シリコン結晶の(100)表面に形成した反転型 MOSFET (Inversion-Mode MOSFET) の素子寸法の微細化によって電流駆動能力の向上がなされてきた。しかし，現在では，微細化に伴う実効電界の増加による電流駆動能力の劣化やノイズの増加が深刻な問題として顕在化している。著者は，微細化が限界に達しつつある MOSFET の特性を構造的に克服することを目的とし，MOSFET を従来の反転型から蓄積型 (Accumulation-Mode) に変更するとともに，従来の(100)表面に加えて(110)表面も活用する 3 次元構造トランジスタを実現することで，電流駆動能力の向上と 1/f 雑音の低減を行った。本論文は，これらの研究成果を取りまとめたもので，全文 5 章よりなる。

第 1 章は序論である。

第 2 章では，(100)表面での Accumulation-Mode MOSFET のデバイス構造とその特性を原理的に示し，動作メカニズムを明らかにしている。Accumulation-Mode では空乏層がないため実効電界が低く抑えられ，移動度の低下が抑制されることにより，電流駆動能力が向上するとともに 1/f ノイズが 1 桁程度低減することを明らかにした。さらに，Accumulation-Mode ではインパクトイオン化によって発生するキャリアの蓄積が抑制されるため微細化に適することを明らかにした。これは，微細化に向けたデバイス構造設計指針を与えるもので，重要な成果である。

第 3 章では，(110)表面を用いる Accumulation-Mode MOSFET を導入し，その電気的特性について論じている。(110)表面上の Inversion-Mode MOSFET では，電流駆動能力が，p-MOSFET では(100)表面の 2.5～3 倍になるにもかかわらず，n-MOSFET では，0.6 倍程度に劣化してしまうことが問題となっている。これに対し，Accumulation-Mode MOSFET を導入することで，n-MOSFET の電流駆動能力劣化が抑制され，最も電流駆動能力の高い(100)表面上の n-MOSFET と同程度まで電流駆動能力が向上することを実証した。さらに 1/f ノイズが，n-MOSFET，p-MOSFET ともに 1 桁から 2 桁程度低減できることを明らかにした。これは，高性能のアナログ回路を実現する上で重要な成果である。

第 4 章では，微細化に伴う短チャンネル効果を抑制し電流駆動能力を向上させるための 3 次元構造トランジスタについて論じている。著者は 3 次元構造 Accumulation-Mode MOSFET を試作し，そのデバイス特性を評価した。等方性酸化でコーナー部の形状を制御して電界集中を抑制するとともに，ラジカル反応によるゲート絶縁膜形成技術を組み合わせ，理想的な特性を有する 3 次元構造トランジスタの作製に成功した。同一面積の従来型 2 次元構造トランジスタに比べて，相互コンダクタンスは 1.6～3 倍以上向上し，電流駆動能力は 2.5 倍以上向上することを実証した。これは，LSI の高性能化においてきわめて重要な成果である。

第 5 章は結論である。

以上要するに本論文は，様々な面方位を用いる 3 次元構造 Accumulation-Mode MOSFET の導入により，高速かつ低ノイズのデバイスを実現できることを示したもので，微細化限界に直面する半導体集積回路技術の課題を克服するものであり，半導体電子工学の発展に寄与するところが少なくない。

よって，本論文は博士(工学)の学位論文として合格と認める。