New Design Methodology for Integrated Circuits and Systems(集積回路及び集積システム設計手法に関する研究)

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号	2044
発行年	1997
URL	http://hdl.handle.net/10097/7317

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授与学位	博士（工学）
学位授与年月日	平成10年3月25日
学位授与の根拠法規	学位規則第4条第1項
研究科、専攻の名称	東北大学大学院工学研究科（博士課程）機械知能工学専攻
学位論文題目	New Design Methodology for Integrated Circuits and Systems - 集積回路及び集積システム設計手法関する研究
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論文内容要旨

Visual control of manipulators promises substantial advantages when working with targets whose position is unknown, or with manipulators which may be flexible or inaccurate. The reported use of visual information to guide robots, or more generally mechanisms, is quite extensive and encompasses manufacturing applications, teleoperation, fruit picking as well as robotic ping-pong, juggling, and balancing. The enormous amount of data produced by vision sensors and technological limitations in processing that data rapidly, has meant that vision has not been widely exploited as a sensing technology when high measurements rates are required. A vision sensor's output data rate, for example, is several orders of magnitude greater than that of force sensor for the same sample rate. Thus, special purpose hardware (special purpose computer system) is needed for the early stages of image processing in order to reduce the data rate to something manageable by a conventional computer.

The hardware design of a digital computer consists of three interrelated phases: system design, logic design, and circuit design. System design is concerned with the specifications and general properties of the system. This task includes the establishment of design objective and design philosophy, the formulation of computer instructions, and the estimation of the economic feasibility. The specifications of the computer structure are translated by the logic designer to provide the hardware implementation of the system. The circuit design specifies the components for the various logic circuits, memory circuits, and power supplies.

The performance of the design on the circuit design stage is simulated based on the compact analytical models of transistors used to build a circuit. The transistor models for circuit design have to describe the device physics as accurately as possible but at the same time be simple enough to allow for simulation of large circuits. Obviously, such models depend on the transistor fabrication technology and have to be updated for every new technology generation.

The extraordinary advances in integrated circuits (IC's) over the last 30 years are very well known, and this is the reason for the most rapid progress ever achieved in a technology by mankind. The underpinning for the remarkable advancement in IC technology has been the continued scaling of the metal-oxide-semiconductor (MOS) transistor to smaller feature sizes. Successively smaller devices have consistently resulted in higher levels of integration, higher performance, and greater reliability, all at a continually decreasing price per bit or per transistor. Throughout most of the 1970's MOS transistor scaling was very straightforward with no problems in approaching any kind of technical, material, or physical limits. In the late 1970's and early 1980's, the scaling to smaller feature sizes led to adverse hot-carrier problems, in which highly energetic electrons caused a slow degradation in device performance. This problem began to shift attention to metal-oxide-semiconductor field-effect transistor (MOSFET) design, and "drain engineering" produced the LDD (lightly doped drain) MOSFET structure. This basic structure permitted the continuation of the rapid advances in IC's during the 1980's and 1990's while suppressing hot-carrier reliability problems.

While the shift from NMOS to complementary MOS (CMOS) technology was the major factor in managing the chip power dissipation problems in the 1980's and 1990's, the continued rapid improve-

ments in circuit performance along with the continued increase in transistor count on the chip during the 1990's are resulting in power dissipation problems even for CMOS. This has altered the thinking considerably on power supply voltage and device operating voltage compared to the consensus views and projections in the late 1980's. That is, the device operating voltage is being reduced more rapidly today than envisioned in the 1980's, since the power dissipation is proportional to CV^2f and it is desired to increase the frequency f (performance) and the total capacitance C (level of integration).

In looking ahead to scaling the MOS transistor to and below 0.1 microns, in the next decade, the device scaling problems multiply rapidly and become very serious. In addition, serious obstacles, and in some cases limits, are being encountered in practically all areas of IC technology such as lithography, process control, interconnect parasitic resistance and capacitance, material requirements, and escalating development and manufacturing costs. The point is reached where new breakthroughs are urgently needed if IC technology is to advance to and below 0.1 μm. One among many other possible approaches to achieve such breakthrough is to use new transistor structures.

CMOS integrated circuits now are almost exclusively fabricated on bulk silicon substrates, and this is for two well-known reasons: the availability of high quality silicon substrates, and the possibility of growing a good quality oxide on silicon, a thing which is not possible on germanium or on compound semiconductors. Yet, modern MOSFETs made in bulk silicon are far from the ideal structure. Bulk MOSFETs are made in silicon wafers having a thickness of approximately 500 μm, but only the first micrometer at the top top of the wafer is used for transistor fabrication. Interactions between the devices and the substrate gives rise to a range of parasitic effects. One of these is the parasitic capacitance between diffused sources and drains and the substrate. This capacitance increases with substrate doping, and becomes larger in modern submicron devices where dopant concentration in the substrate is higher than in previous MOS technologies. Another parasitic effect found in bulk CMOS devices is called latch up, which consists in the unwanted triggering of a PNPN thyristor structure inherently present in all bulk CMOS structures. Latch up becomes a severe problem in devices with small dimensions.

If a Silicon-on-Insulator (SOI) substrate is used, quasi-ideal devices can be fabricated. The full dielectric isolation of the device prevents the occurrence of most of the parasitic effects experienced in bulk silicon devices. In an SOI CMOS inverter a latch up path is ruled out because there is no current path to the substrate. In SOI circuits the maximum capacitance between the junction and the substrate is the capacitance of the buried insulator. This capacitance tends towards zero if thick insulators are used. The absence of the latch-up, the reduced parasitic source and drain capacitances, and the ease of making shallow junctions are merely three obvious examples of the advantages presented by SOI technology over bulk. There are many other properties which allow SOI devices and circuits to exhibit performances superior to those of their bulk counterparts. Hence, SOI technology is now under intensive investigation as a possible candidate for future main-stream technology and the development of design tools for computer design using SOI technology becomes an important task.

It is the circuit design phase where the specific features of scaled down SOI circuits have to be taken into account. There are several areas of difficulties in scaling down the SOI MOSFET: influence of the parasitic source-and-drain series resistances, impact ionization phenomena, difficulties in achieving adequate drive current and adequate turn-off simultaneously and others. Accurate physics-based models of these phenomenon are most important both for design of the scaled down transistors and for accurate circuit simulation using SOI circuits.

Therefore, in the present work we concentrate on compact models for circuit design which accurately account for important physical phenomenon in SOI MOSFET. We then develop a software simulation tool for SOI circuits and systems by implementing an SOI models into well-known circuit simulator SPICE. Finally, we demonstrate circuit design of a highly-parallel computer system for image processing to be fabricated using three-dimensional SOI technology.

In the first chapter we describe the motivation for the research. In the second chapter the current status of the SOI MOSFET modeling is reviewed and existing problems are pointed out.

In the third chapter we develop a method to extract parasitic source-and-drain series resistances of the SOI MOSFET and than develop a new model for the impact ionization phenomena in SOI devices. Both parasitic series resistances and impact ionization phenomena were mentioned above as major limiting factors influencing design of the scaled devices. In the fourth chapter we address one more important problem of designing the scaled down SOI devices: achieving adequate drive current and adequate turn-off simultaneously. Firstly, a two-dimensional compact model for the potential distribution and the subthreshold slope (the rate at which the device turns off as the gate voltage is reduced) in the SOI device is developed and, than, issues of SOI device design with emphasis on achieving a proper threshold voltage are described. In the fifth chapter the compact model for the subthreshold current in SOI device is developed using potential distribution model obtained in chapter three. In the sixth chapter implementation of the SOI device model into the circuit simulation program SPICE is discussed. In the seventh chapter design of a computer to be fabricated using three-dimensional SOI circuits is demonstrated. The conclusions are made in the chapter eight. An acknowledgement is expressed in chapter nine, after which bibliography and list of publications follow.

In summary, in this work the mathematical methods, models and software tools were developed for the circuit design of VLSI systems based on SOI technology which is considered to be one of the candidates for the future mainstream technology.

The mathematical methods and models for physical phenomena crucial for successful scaling down of SOI devices, accurate circuit simulation and comparison with the performance of circuits and systems based on the bulk technology were developed.

1. The accurate mathematical method was developed to extract and model the parasitic source-and-drain series resistances of LDD MOSFETs. The method is based on measuring output resistances of transistors with varying channel length. New model for circuit simulation of the impact ionization current in SOI devices was developed. It was shown that an accurate model for the impact ionization current in submicron LDD SOI MOSFETs has to account for the voltage drop on the parasitic source-and-drain series resistances and the gate-voltage dependent saturation field in the expression for the maximum channel electric field E_m. It is demonstrated that the plot of $I_{IMP}/(I_D E_m)$ versus $1/E_m$ is a single straight line for a given technology.

2. New potential distribution model for the subthreshold region of operation of SOI MOSFET was developed and design issues for 0.1 μm SOI devices were thoroughly investigated. The model accounts for the nonlinear potential distribution inside the buried oxide without use of any fitting parameters. The analytical model is compared to the numerical device simulation results and a good agreement is found. Our model accurately describes the effect of the subthreshold factor decrease with increasing the substrate doping concentration in thin-film fully-depleted SOI MOSFETs. The model can be utilized to predict design criteria for scaling down thin-film fully depleted SOI MOSFETs and is suitable for use in circuit simulators such as SPICE.

3. A new two-dimensional model for subthreshold current in fully-depleted silicon-on-insulator metal-oxide-semiconductor field effect transistor (SOI MOSFET) is developed. The model is based on analytical approximation of two-dimensional Poissons's equation solution, drift-diffusion current equation and accounts for the drain-induced barrier lowering and channel-length modulation in weak inversion. The model provides a convenient tool for the design of submicron SOI MOSFETs. The model adequately describes the submicrometer devices, and, at the same time, is simple enough to be implemented in circuit simulators.

The software design tool for SOI circuits was then developed by implementing an SOI structure into the circuit simulator SPICE which is an industrial standard for circuit simulation. The *device* and *model* cards for SOI device were developed, the linked list structures for internal representation of SOI devices and models were specified and the software code for their implementation was developed.

Finally, performance advantages of the SOI technology were demonstrated on the example of the design of the circuits of a highly-parallel computer system for image processing to be fabricated using three-dimensional SOI technology.

審査結果の要旨

ＳＯＩ（Silicon-On-Insulator）・ＭＯＳトランジスタは将来の超高速・低電力ＬＳＩ用半導体素子として注目されているが、微細寸法を有するＳＯＩ・ＭＯＳトランジスタに対する良好な素子モデルが提案されていないため、微細ＳＯＩ・ＭＯＳトランジスタを使ったＬＳＩの高精度回路設計が難しかった。著者は、微細寸法を有するＳＯＩ・ＭＯＳトランジスタに対する新しい素子モデルを提案し、これを用いたＬＳＩの高精度回路設計に関する研究を行った。本論文はこれらの成果をとりまとめたもので、全編８章より成る。

第１章は緒論である。

第２章では、微細ＳＯＩ・ＭＯＳトランジスタの基本素子モデルとして、従来の４端子モデルに疑似基板端子を加えた新しい５端子モデルを提案している。これらは有用な成果である。

第３章では、微細ＳＯＩ・ＭＯＳトランジスタ素子モデルの高精度化で重要な直列抵抗の新しい抽出方法を提案するとともに、より精度の高い物理モデルに基づいた衝突電離電流式を導いている。これらは重要な成果である。

第４章では、チャネル長０．１μｍまでの微細ＳＯＩ・ＭＯＳトランジスタのサブスレッショルド領域の特性解析に用いることのできる新しい解析モデルを提案し、計算機による厳密な数値解析結果と比較して良い一致を得ている。これらは有用な知見である。

第５章では、前章で提案した解析モデルを基にして、サブスレッショルド領域における電流－電圧式を導いている。これらは有用な成果である。

第６章では、前章までに提案したＳＯＩ・ＭＯＳトランジスタ素子モデルを回路解析用ＣＡＤツールであるＳＰＩＣＥシミュレータに組み込み、ＳＯＩ・ＭＯＳトランジスタを使ったＬＳＩの回路設計・解析を行う手法を確立している。これらは重要な成果である。

第７章では、前章で確立した回路設計手法を用いて、リアルタイム画像処理システムに使われる演算処理ユニットを設計し、ＳＯＩ・ＭＯＳトランジスタを用いることによって性能が飛躍的に向上することを明らかにしている。これらは有用な知見である。

第８章は結論である。

以上、要するに本論文は、将来の超高速・低電力ＬＳＩ用半導体素子として注目されているＳＯＩ（Silicon-On-Insulator）・ＭＯＳトランジスタに対する高精度素子モデルを提案し、これをＳＰＩＣＥシミュレータに組み込み、演算処理ユニットを設計することによって、その有用性を示したもので、集積回路工学および機械知能工学の発展に寄与するところが少なくない。

よって、本論文は博士（工学）の学位論文として合格と認める。