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LPSR: Novel Low Power State Retention Technique for CMOS VLSI Design

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Abstract: In mobile computing and mobile communication applications powered by battery, the battery life is a premier concern. Leakage power loss is critical in CMOS VLSI circuits as it leaks the battery even when devices are in idle state. To reduce subthreshold leakage power as well as total power in CMOS logic gates and circuits a new circuit technique called LPSR Technique is proposed in this work. Earlier well known techniques for leakage reduction and state retention are compared with this technique. This technique reduces maximum amount of leakage power during deep sleep mode, maximum power reduction during dynamic (clocked) mode and has a provision of preserving state in low power sleep mode. All the circuits are designed, simulated and low power performance evaluation is done using 90nm CMOS technology files in Cadence Design Environment

Key Words: LPSR Technique, leakage power, state retention, total power

1. INTRODUCTION

The ongoing technology scaling has resulted in the use of lower power supply voltages for CMOS circuits which has an associated effect of lower threshold voltages to enhance performance. Since the channel length for successive technology generations is reducing, threshold voltage and gate oxide thickness are also being scaled down to keep pace with the performance. Lower threshold voltage results in exponential rise in leakage current because transistors cannot be switched off completely. For a CMOS circuit, the total power dissipation includes dynamic and static components. The components of static power dissipation are subthreshold leakage, junction leakage, gate oxide leakage, gate induced drain leakage, punch through leakage [1], [2].

In a CMOS transistor ideally current flows from Source to Drain, when $V_{GS} > V_T$. In real transistors current does not abruptly cut-off below threshold, but drops off exponentially as given by equation (1). This sub-threshold leakage current for $V_{GS} < V_T$ is given by

$$I_{DS}=I_{DSO}\, e^{(VGS-VT)/(nvT)[1-e(-VDS/vT)]} \text{ -------(1)}$$

Where

$$V_T = V_{T0} - \square V_{DS} + \square [(\square_s + V_{SB})^{0.5} - (\square_s)^{0.5}] \text{ --------- (2)}$$

In these equations I_{DS0} is current at threshold(dependent on process and device geometry), V_{T0} is the zero bias threshold voltage, γ - is the linearized body effect coefficient, η represents the effect of V_{DS} on threshold voltage, n is the sub- threshold swing coefficient, v_T is thermal voltage respectively. The η term describes Drain Induced Barrier Lowering. Subthreshold conduction is enhanced by Drain Induced Barrier Lowering (DIBL) in which positive VDS effectively reduces V_T. Leakage current doubles for every 8^0 to 10^0K rise in temperature. The subthreshold leakage current can be reduced by increasing threshold voltage V_{TO}, increasing V_{SB} and reduction of V_{GS}, V_{DS} and lowering the temperature [3]. Many techniques for leakage power control make use of methods such as scaling supply voltage, reducing voltage swing and capacitance, reduction of switching activity or introduction of high resistance between the supply voltage and ground. Sleepy Transistor [4], Dual V_T CMOS [5], DRG Cache[6], multiple power gating[7], sleepy keeper [8], VCLEART [9], LECTOR[10], GALLEOR[11], Sleepy Pass Gate[12], low leak stable SRAM [13], ultra-low leak and state retention for inverters[14] , are some of the techniques for leakage reduction. Each method has its own merits and demerits. Some techniques use dual V_T transistors; high V_T

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transistors to reduce leakage and low VT transistors to improve speed of operation in critical sections of the circuit. In this paper novel LPSR technique to reduce leakage power and total power in combinational circuits and data path elements is proposed, which makes use of single VT transistors in all parts of the circuit to achieve low leakage power during sleep mode of operation and lower total power dissipation .This paper is organized as follows: section 1 deals with introduction and related work. Section 2 deals with review of some well-known published leakage reduction and state retention techniques. Section 3 proposes LPSR technique applied to gates and full adder. Simulation procedure and results are provided in section 4. Concluding remarks are given in section 5.

2. REVIEW OF EARLIER LOW LEAKAGE POWER TECHNIQUES

Some well-known techniques for leakage reduction and state retention are reviewed in this section. The performance of our proposed LPSR technique with respect to leakage power during active and sleep modes of operation as well as total power dissipation are compared with these existing methods in Section 4.

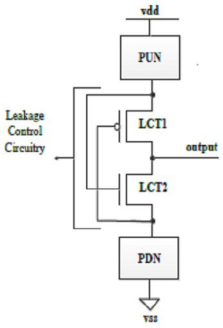

Fig -1: LECTOR Technique

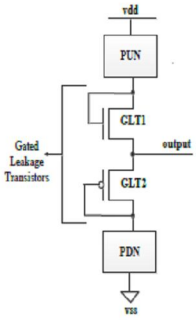

Fig -2: GALEOR Technique

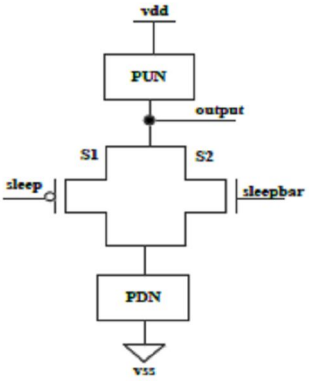

Fig -3: Sleepy Pass Gate Technique

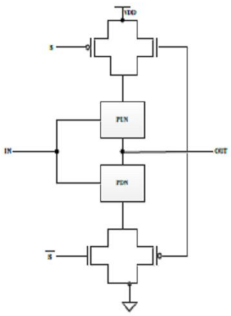

Fig -4: Sleepy Keeper Technique

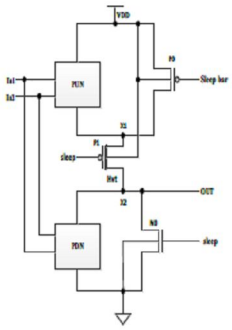

Fig -5: VCLEARIT Approach

The LECTOR method [10] inserts two extra Leakage Control Transistors (a P-type and an N-type) within the gate, in which the gate terminal of each Leakage Control Transistor is controlled by the source of the other. GALEOR [11] technique reduces the leakage current flowing through the CMOS logic gate using stack effect. These two techniques have very good low leak operation but there is no provision of sleep mode of operation.

In SLEEPY-PASS GATE [12] approach two sleep transistors PMOS and NMOS are connected in parallel and inserted between Pull-Up and Pull-Down Networks of a CMOS logic gate to form a pass gate like structure. This has large power dissipation during pulsed operation. SLEEPY KEEPER [8] uses a PMOS transistor in parallel to NMOS sleep transistor in the pull down path and NMOS transistor in

parallel to PMOS sleep transistor in the pull up path. The extra retention transistors are connected to the output so that during sleep mode the logic state is maintained, with high total power dissipation.

VCLEARIT [9], Method uses a combination of NMOS and PMOS devices to achieve leakage reduction. This technique provides a logic low state during sleep mode unlike previous circuits. This technique cannot retain state during sleep operation.

3. PROPOSED LOW POWER STATE RETENTION TECHNIQUE

A novel power reduction technique is proposed in this work. This LPSR technique is applied to NAND and NOR gates and the data path element full adder. The Section 3.1 deals with logic gates and Section 3.2 gives the application to full adder.

3.1 Logic Gates

The LPSR technique makes use of a pair of NMOS and PMOS transistors in the pull up and pull down paths of the CMOS circuit. General block diagram as well as schematics of LPSR NAND and NOR gates are as shown below.

The LPSR logic gate has four modes of operation.

a. Active Mode: both sleep control signals slp = 0 and slpb = 1 are used to switch on the sleep transistors in leakage control block. Thus the virtual ground node VG is at ground potential and the virtual power node VP is at VDD. The gate thus sees good potential difference across nodes VP and VG. The gate functions as per the truth table with good output logic levels.

b. Deep Sleep Mode: The sleep signals are held at slp = 1 and slpb = 0 states to switch off all the sleep transistors in both pull up and pull down leakage control blocks. Thus the actual power and ground path are broken and the circuit experiences lower

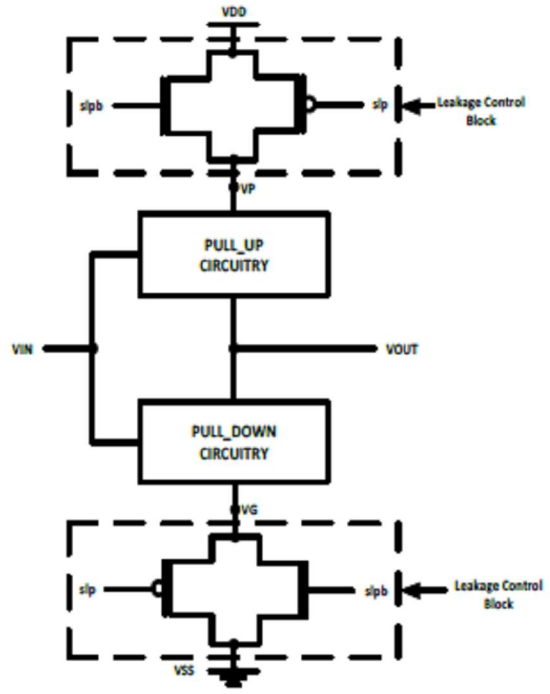

Fig -6: Generic LPSR Technique

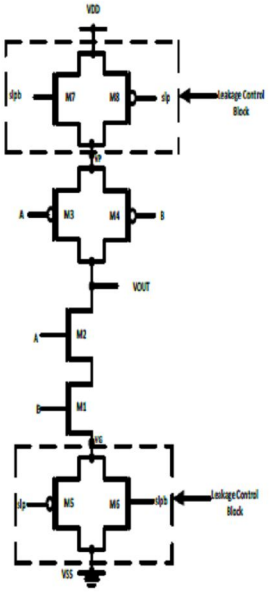

Fig -1: LPSR NAND

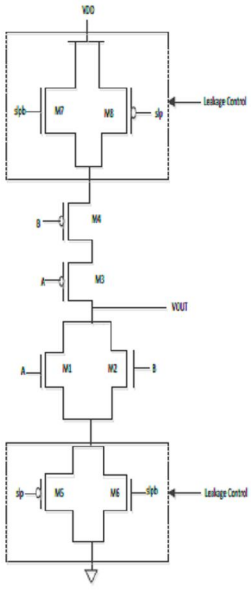

Fig -2: LPSR NOR

voltage across the nodes VP and VG. A very high resistance path is established between VDD and ground due to the parallel combination of the off resistance of sleep transistors and the leakage current

flowing through the circuit reduces significantly and hence lowest power dissipation.

c. State Retention Mode 1: The sleep signals are maintained at slp = 0 and slpb = 0. The circuit sees a higher than ground voltage at the node VG and full VDD at the node VP. The state retention takes place with low leakage current with the output at good logic 1 level.

d. State Retention Mode 0: The sleep control signals are maintained at slp = 1 and slpb = 1. The connection to actual ground is complete, the node VP is at lower VDD. Thus the state retention takes place with low leakage current with the output at good logic 0 levels.

3.2 Data Path Element: Full Adder

The LPSR Technique is applied to full adder. The performance is compared with full adder using the sleepy keeper technique. The schematic of the circuit is given below.

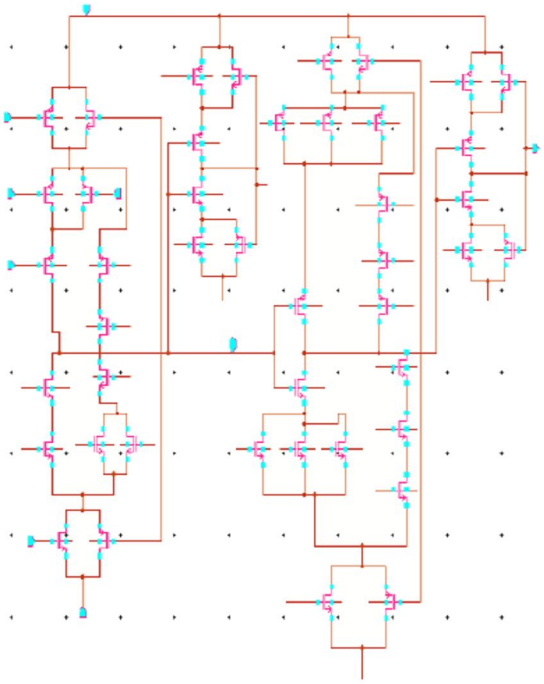

Fig -9: Full Adder (Sleepy Keeper Approach)

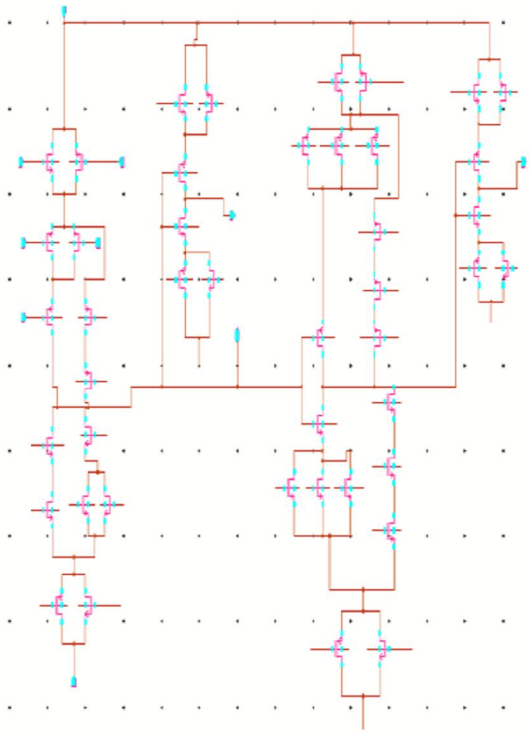

Fig -10: Full Adder (LPSR Approach)

4. SIMULATIONS AND RESULTS

All the gates are designed, simulated and functionality verified using 90nm CMOS technology files in Cadence Design Environment. We have used single VT transistors in all designs to show the performance benefits and comparison of different techniques. These techniques are applied to both NAND and NOR gate as representative combinational circuits. The operation of gates is verified for all input combinations. Static power for all input combinations during active and sleep (idle) mode as well as total (dynamic) power during clocked operation are all measured using cadence tools.

Table 1 provides the static power dissipation during active and sleep modes for all NAND gates. Table 2 neither provides the static power

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dissipation during active and sleeps modes for all NOR gates. During Active mode sleep control signals slp and slpb hold the respective sleep transistors in the ON state and in Sleep mode the sleep signals switch OFF the leakage control transistors. The sleep control signals slp and slpb are held at appropriate logic levels depending on whether NMOS or PMOS transistor is driven by them, to make transistor on or off. The actual signal values are given in tables of observation. Table 3 provides comparison of the total power dissipation of all the NAND and NOR gates during pulsed operation. For pulsed operation, transition period is taken as 2 us duration and all the gates are controlled by the sleep signals of same pulse width and period for the sake of comparison. Long sleep or inactive is also introduced to observe the performance during sleep period. Table 4 provides leakage power during active and sleep mode as well as total power dissipation for a full adder using sleepy keeper and LPSR technique.

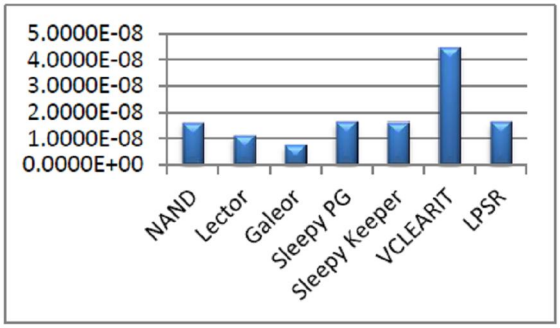

Fig -11: Active Mode Power Dissipation (NAND Gate)

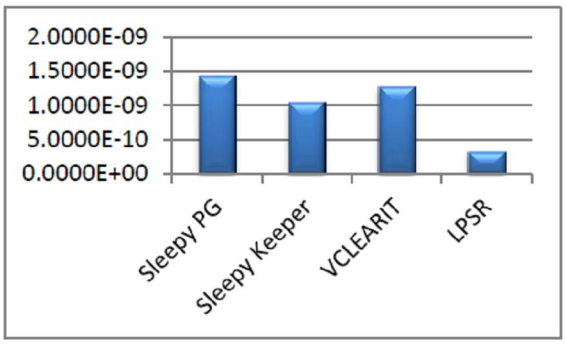

Fig -12: Sleep Mode Power Dissipation (NAND Gate)

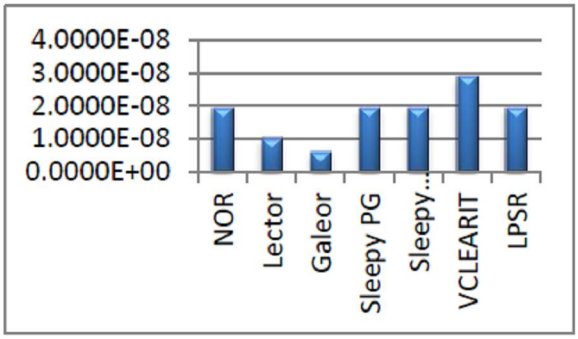

Fig -13: Active Mode Power Dissipation (NOR Gate)

Table -1: Static Power Dissipation for 2 Input NAND Gate

90 nm Technology with VDD = 1.1 Volt					
Gate	**Leakage power(in Watts) for input vectors in Active**				**Avg. Leakage Power in**
	0 0	**0 1**	**1 0**	**1 1**	
NAND	2.2070E-09	3.8012E-08	2.2529E-08	8.3128E-10	1.5894E-08
Lector NAND	2.1440E-09	2.1189E-08	1.9873E-08	4.6051E-10	1.09E-08
Galeor NAND	2.0975E-09	1.3330E-08	1.3312E-08	4.3963E-10	7.29E-09
Sleepy NAND (slp = 0, slpb =	2.6309E-09	3.8423E-08	2.2951E-08	8.3126E-10	1.6274E-08
Slp. Keeper NAND (slp = 0,	2.3770E-09	3.8115E-08	2.2686E-08	1.0025E-09	1.6045E-08
VCLEARIT NAND (slp = 0,	4.0335E-08	7.6071E-08	6.0634E-08	6.7230E-10	4.4428E-08
LPSR (slp = 0, slpb = 1)	2.6308E-09	3.8299E-08	2.2912E-08	1.2550E-09	1.63E-08

	Leakage power(in Watts) for input vectors in Sleep				
NAND	NA				
Lector NAND	NA				
Galeor NAND	NA				
Sleepy NAND	1.5412E-	1.5951E-09	1.8170E-09	7.5162E-10	1.43E-09
Sleepy Keeper NAND (slp = 1, slpb = 0)	9.7452E-10	1.4624E-09	1.7098E-09	7.2076E-12	1.0385E-09
VCLEARIT NAND (slp =1,	1.6874E-	1.2634E-09	1.2634E-09	8.3954E-10	1.2634E-09
LPSR (slp = 1, slpb = 0)	4.4613E-	4.1856E-10	4.0119E-10	1.1717E-11	3.19E-10

Table -2: Static Power Dissipation for 2 Inputs NOR Gate

Gat e	Leakage power(in Watts) for input vectors in Active Mode				Avg. Leakage Power in Watts
	0	0	1	1	
NO	7.6194E-	8.3954E-	2.4107E-	1.0695E-	1.9321E-08
Lector NOR	3.9917E-	6.6499E-	2.2405E-	1.0354E-	1.0204E-08
Galeor NOR	2.3853E-	6.5874E-	2.2151E-	1.0352E-	6.1859E-09
Sleepy NOR (slp = 0,	7.6566E-08	8.3954E-10	2.41071E-10	1.0686E-11	1.9610E-08
Sleepy Keeper NOR	7.6099E-08	1.0109E-09	4.1254E-10	1.8221E-10	1.9426E-08
VCLEARIT NOR (slp	1.1409E-07	8.8437E-10	4.4955E-10	2.5050E-10	2.8921E-08
LPSR (slp = 0, slpb =	7.6079E-	1.2634E-	6.6495E-	4.3462E-	1.9610E-08
	Leakage power(in Watts) for input vectors				
NO	N				
Lector NOR	N				
Galeor NOR	N				
Sleepy NOR (slp = 1,	3.3872E-09	8.2198E-10	2.4064E-10	1.0676E-11	1.1151E-09
Sleepy Keeper NOR (slp = 1, slpb = 0)	3.7926E-10	3.1959E-11	6.6671E-12	4.4556E-12	1.0559E-10
VCLEARIT NOR (slp = 1, slpb = 0)	1.6874E-09	1.2634E-09	1.2634E-09	8.3954E-10	1.2634E-09
LPSR (slp = 1, slpb =	3.5096E-	4.8406E-	1.0707E-	5.1292E-	1.0380E-10

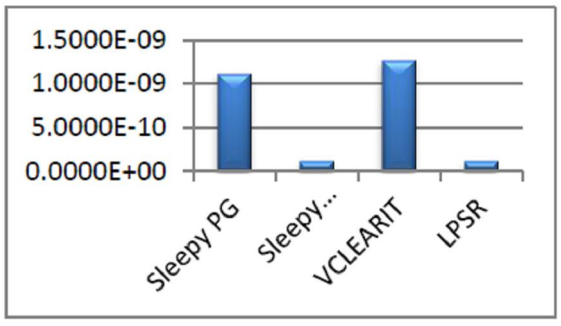

Fig -14: Sleep Mode Power Dissipation (NOR Gate)

Table -3: Static Power Dissipation for 2 Inputs NOR Gate

Gate	Total Power during Clocked Operation	Gate	Total Power during Clocked Operation
NAND	453.40E-09	NOR	556.10E-09

Lector NAND	492.60E-09	Lector NOR	621.10E-09
Galeor NAND	409.10E-09	Galeor NOR	522.20E-09
Sleepy NAND	114.40E-09	Sleepy NOR	201.40E-09
Sleepy Keeper NAND	2.6780E-08	Sleepy Keeper NOR	1.9340E-08
VCLEARIT NAND	38.26E-09	VCLEARIT NOR	39.820E-09
LPSR NAND	10.68E-09	LPSR NOR	15.57E-09

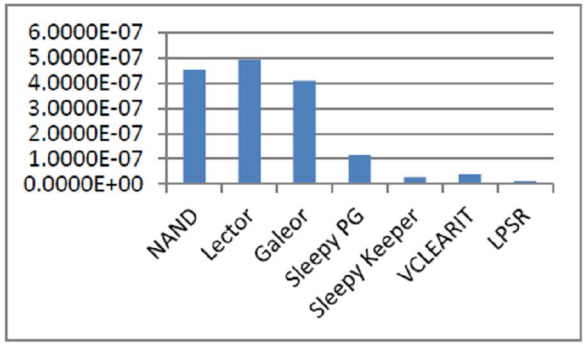

Fig -15: Total Power Dissipation (NAND Gate)

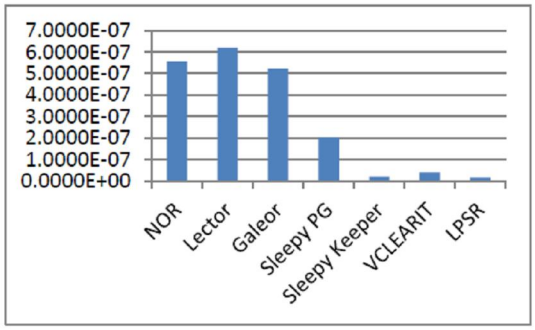

Fig -16: Total Power Dissipation (NOR Gate)

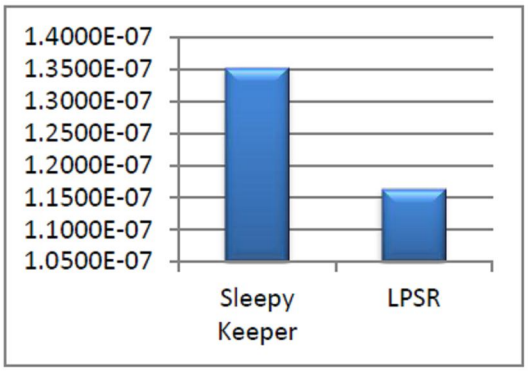

Fig -17: Active Mode (Full Adder)

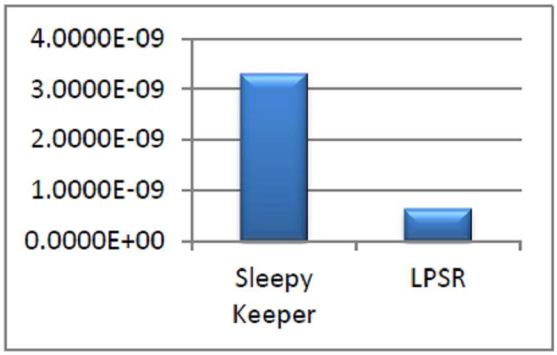

Fig -18: Sleep Mode (Full Adder)

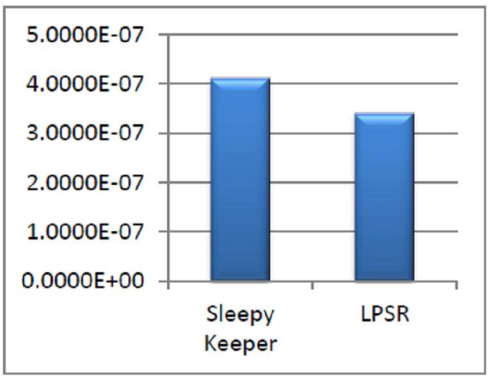

Fig -19: Total Power (Full Adder)

Table -4: Leakage Power, Average and Total Power Comparison of One-Bit Adder

Methods	Leakage Power Dissipation in Watts			
	Sleepy-Keeper		RSLR	
Input Vector	Active (slp = 1, slpb =	Sleep (slp =0, slpb	Active (slp = 0, slpb =	Sleep (slp =1, slpb = 0)

000	1.0303E-07	4.7288E-09	9.9004E-08	1.7590E-09
001	1.2218E-07	2.8227E-09	1.1819E-07	9.2595E-10
010	1.6029E-07	2.0247E-09	1.5621E-07	6.6231E-10
011	1.7240E-07	2.0902E-09	1.6813E-07	3.9996E-10
100	1.3827E-07	3.2470E-09	1.3424E-07	5.5480E-10
101	1.4249 E-07	2.0902E-09	1.3838E-07	3.3086E-10
110	1.3928E-07	4.6215E-09	1.3518E-07	2.8210E-10
111	1.0365E-07	4.8523E-09	9.9629E-08	1.8599E-10
Average Power	1.3520E-07	3.3096E-09	1.1635E-07	6.3751E-10
Total power	411.8E-09		341.0E-09	

5. CONCLUSION

During active mode of operation LECTOR and GALLEOR techniques provide maximum leakage reduction. But they suffer from the absence of sleep mode of operation and result in maximum power dissipation during pulsed operation. The sleepy keeper approach though maintains state during sleep mode at reduced levels results in large power dissipation during pulsed operation because the output terminal is permanently connected to leakage control circuit and there is no deep sleep state. The other techniques have intermediate results. The proposed LPSR technique has active mode static power on par with other sleepy techniques and the least static power during deep sleep state and good state retention at low power. This technique has least total power dissipation during pulsed operation. Since single V_T transistors are only used in all the designs to achieve ultra-low power operation, the novel technique provides new choice to the designers of low power VLSI circuits.

REFERENCES

[1] Y. Taur, A. Chandrakasan, W. J. Bowhill, and F. Fox, Eds. Piscataway, "CMOS scaling and issues in sub-0.25 µm systems in Design of High-Performance Microprocessor Circuits," NJ: IEEE, 2001, pp. 27–45.

[2] Kaushik Roy, Saibal Mukhopadhyay, Hamid Mahmoodi- Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Submicrometer CMOS Circuits," Proceedings of the IEEE, vol. 91, No. 2, February 2003.

[3] Neil Weste, David Harris Ayan Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, III Edition, Pearson Education.

[4] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J.Yamada, "1-V power supply high- speed digital circuit technology with multi-threshold voltage CMOS," IEEE J. Solid-State Circuits, vol. 30, pp. 847–854, Aug. 1995.

[5] L.Wei, Z. Chen, M. Johnson, K. Roy, Y. Ye, and V. De, "Design and optimization of dual threshold circuits for low voltage low power applications," IEEE Trans. VLSI Systems, pp. 16–24, Mar. 1999.

[6] Amit Agarwal, Hai Li, and Kaushik Roy,"DRG –Cache: A data retention gated ground cache for low power," Proceedings of the 39th Design Automation Conference, June 2002.

[7] Suhwan Kim, Stephen V. Kosonocky, Daniel R. Knebel, and Kevin Stawiasz ,"Experimental Measurement of A Novel Power Gating Structure with Intermediate

Power saving mode", Proceedings of the 2004 International Symposium on Low Power Electronics and Design (ISLPED).

[8] S. H. Kim and V. J. Mooney, "Sleepy keeper: a new approach to low leakage power VLSI design," VLSI-SoC 2006

[9] Lakshminathan, P. and Nunez," VCLEARIT: A VLSI CMOS: Circuit Leakage Reduction Technique for Nanoscale Technologies," Proceedings of the Advanced Low Power Systems Workshop, at the 21st ACM International Conference on Supercomputing (June 2007), pp. 15-22

[10] N. Hanchate and N. Ranganathan, "Lector: A technique for leakage reduction in CMOS circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 2, pp.196-205, February 2004.

[11] Srikanth Katrue and Dhireesha Kudithipudi,"GALEOR: Leakage reduction for CMOS circuits," 15th IEEE.

[12] M. Geetha Priya, K. Baskaran and D. Krishnaveni, "A Novel Leakage Power Reduction technique for CMOS VLSI Circuits", European Journal of Scientific Research, ISSN 1450-216X Vol.74 No.1 (2012), pp.96-105.

[13] Rajani H.P., Hansraj Guhilot and S.Y.Kulkarni, "Novel Stable SRAM for Ultra Low Power Deep Submicron Cache Memories", IEEE Recent Advances in Intelligent Computational Systems, RAICS 2011, in IEEE Explorer.

[14] Rajani H.P. and Srimannarayana Kulkarni, "Novel Sleep Transistor Techniques for Low Leakage Power in Peripheral Circuits, "International Journal of VLSI and Communication Systems, in Press.