Studies on Graphene Field Effect Transistors : Solution-Processed Gate Dielectrics and UV-Ozone-Processed Contact Resistance

Doctoral Thesis

Thesis Title

Studies on Graphene Field Effect Transistors:
Solution-Processed Gate Dielectrics and
UV-Ozone-Processed Contact Resistance

Department of Electronic Engineering
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Abstract

Graphene has been attracting considerable interest for various applications such as transparent electrodes, sensors, solar cells, and transistors due its outstanding electrical, optical and mechanical properties. A number of researchers have especially focused on developing graphene field-effect transistors (GFETs) to replace conventional silicon-based devices. Many challenges however still remain to be overcome. This research, aimed at developing high performance GFETs, is focused on improving the process design and the device structure of GFETs to fully extract graphene's excellent properties.

First, a novel gate dielectric deposition method has been developed based on a solution process. The process parameters are tuned to minimize the doping, strain, defect density in graphene during the gate dielectric deposition. As a result, a modified solution process is proposed, which consists of formation of an initial ultrathin Al_2O_3 seeding layer, spin-coating, oxygen-plasma treatment, post-deposition annealing (PDA). A high intrinsic carrier mobility of 8400 cm^2/Vs was obtained by minimizing the doping, strain and defects to graphene in top-gated GFETs.

Second, UVO_3 treatment during the contact electrode formation as well as fabrication of overlapped S/D to top-gate device are proposed to reduce the series resistance: the access and the contact resistance. As a result, low contact resistances, comparable to one of the best reported values, were achieved due to effective removal of interfacial contaminations and reduction of the access length.

Finally, a top-gated GFET, consisting of modified solution-processed gate dielectrics, UVO_3-treated contacts, and overlapped S/D to gate structure, was fabricated and characterized. As a result, a highest transconductance of 358 μS and a field-effect mobility of 301 cm^2/Vs, not achievable by either the solution-gate or the UVO_3 treated contacts alone, have been obtained. These high transconductance and the field-effect mobility values are attributed to both increase of the intrinsic mobility and reduction of the contact resistance. The intrinsic mobilities were actually as high as 8620 cm^2/Vs for holes and 8650 cm^2/Vs for electrons. A low contact resistance of 900 Ωμm was obtained. The combination of the solution-processed gate dielectric, UVO_3-treated contacts, and overlapped S/D to gate structure is quite promising for high performance GFETs.

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Introduction

1.1 Limitation of MOSFET Scaling

Since their beginning of early 1970's, silicon-based transistors have been successfully developed by downsizing the MOSFETs (Metal Oxide Semiconductor Field Effect transistors) according to the Moore's law [1,2]. In this law, the number of transistors in integrated circuits is doubled with every two years. As the MOSFET feature size scales down, the number of integrated circuits within a same size wafer exponentially increased, resulting in significant decrease of the production cost per transistor. The scaling down is still a most effective and important strategy for realizing high performance and low power consumption in MOSFETs up to now. Consequently, the technology node in mass production reached 14 nm in 2014.

While the scaling strategy has undoubtedly led to remarkable developments in semiconductor industry, it is also true that conventional MOSFET technology is facing physical and technological limits of scaling as the gate length (L_G) of the transistors becomes the order of few nanometer in size [3-7]. The challenges being faced are:

a) Subthreshold swing (*SS*) degradation

b) Threshold voltage (V_{Th}) roll-off

c) Drain-induced barrier lowering (DIBL)

d) Band-to-band tunneling (BTBT)

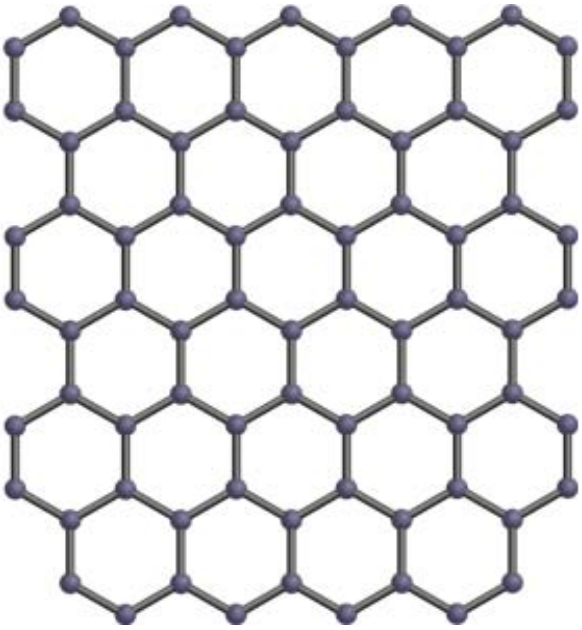
The thickness of the gate dielectrics has also been reduced concurrently to gain high enough current at low operation voltages. For thicknesses below 20 Å, however, the quantum mechanical direct tunneling occurs, resulting in significant increase of the gate leakage current into the gate oxide [8,9]. Consequently, the standby power consumption in devices in such ultrathin gate dielectrics increases exponentially, causing a most serious problem.

To solve these problems, a variety of new technology and materials are being developed, which include use of 3D structure, R-CAT (Recessed-Channel Array Transistor), high-k gate dielectrics, metal gate, ultra-shallow source/drain junctions, and strained silicon. Despite these efforts, however, many researchers are finding unbeatable physical limits for gate length less than 5 nm. We are therefore forced to find new solutions by employing alternative channel materials such as III-V compound semiconductor, carbon nanotube (CNT) and graphene. Among these materials, graphene is a strongest candidate to replace the silicon-based devices as a channel material due to its outstanding electrical properties.

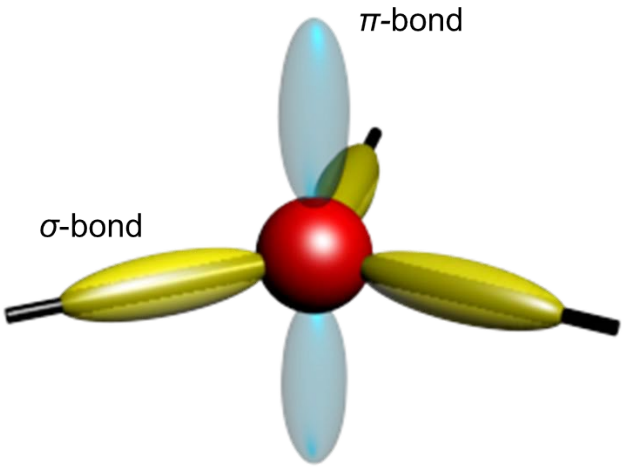
1.2 Graphene as an Alternative Material

1.2.1 Structural Properties of Graphene

Graphene is a flat monolayer of sp^2-bonded carbon atoms with a hexagonal honeycomb lattice. Graphene is a basic structural element of carbon allotropes such as graphite, carbon nanotubes and fullerenes. One carbon atom contains six electrons with a configuration of $1s^2\ 2s^2\ 2p^2$. Among these, the outer four $2s^2\ 2p^2$ electrons act as the valence electrons. In graphene, one 2*s* orbital interacts with the $2p_x$ and the $2p_y$ orbitals to form three sp^2-hybridized orbitals. These three orbitals are used to form three σ-bonds with the neighboring carbon atoms. They are directly linked within the a-b plane with angles of 120 degrees each other, resulting in the hexagonal structure of graphene [in Fig. 1.1 (a)]. This honeycomb structure gives a record breaking strength and excellent mechanical properties to graphene because the σ-bond is the strongest among the covalent bonds. The remaining valence electron sits in the p_z orbital, which is perpendicular to the graphene plane. π-electrons in graphene are relatively delocalized and weakly bound to the nuclei. The exceptional electronic properties in graphene are caused by this delocalized nature of π electrons [10].



(a)



(b)

Figure 1.1. (a) Atomic structure of graphene. (b) π- (blue) and σ- bonds (yellow) in graphene.

1.2.2 Electrical Properties of Graphene

Graphene is a 2D honeycomb lattice made of carbon atoms. This honeycomb lattice can be characterized with a basis of two atoms, labeled A and B in Figure 1.2. The primitive unit cell is an equilateral parallelogram with the lattice constant of a = 2.46 Å. Because the unit cell consists of two carbon atoms, the energy spectrum originating from the π orbitals has two bands and these π electrons per unit cell contribute to the electrical properties of graphene. The band structure of graphene can be described using a nearest neighbor tight-binding model as follows [11,12]:

$$E(k_x, k_y) = \pm\gamma\sqrt{1 + 4\cos(\frac{\sqrt{3}ak_x}{2})\cos(\frac{ak_y}{2}) + 4\cos^2(\frac{ak_y}{2})}\,, \tag{1.1}$$

where a is the lattice constant and γ is the nearest neighbor hopping energy.

Figure 1.3 shows the band structure of graphene by 3D plot of the nearest neighbor tight-binding dispersion. The upper half is the conduction (π^*) band and the lower half is the valence (π) band. The valence band is completely filled by electrons and the conduction band is empty. In Fig. 1.3, it is confirmed that the top of the valence band and the bottom of the conduction band meet at a point K, called the Dirac point. Graphene, therefore, is considered as a semi-metal or zero-bandgap material due to absence of the bandgap at the Fermi energy [13].

Around these K-points, the dispersion can be expressed as a linear relation as

$$E(|k|) = \pm\hbar\nu_F\,|k|\,, \tag{1.2}$$

where $\hbar$ is the reduced Plank constant and ν_F is the Fermi velocity. The value of ν_F is about $c/300$, with c being the speed of light. This dispersion relation implies that the carriers behave like a massless Dirac particle with a very large Fermi velocity [14]. These properties are in sharp contrast with those of classical semiconductors having a dispersion of $E = p^2/2m^*$, where m^* is the effective mass of the electrons.

The density of states (DOS) is an important property of electronic materials, which gives the

density of mobile electrons and holes present in the solid at a given temperature. In graphene, the DOS $g(E)$ is given by the following equation [13,15]:

$$g(E) = \frac{2}{\pi(\hbar v_F)^2} |E|, \tag{1.3}$$

where the energy E is measured from the Fermi energy E_F. From this equation, it is noted that the DOS value is zero at the Fermi energy ($E_F = 0$). This is the difference between graphene and regular metals that have large DOS at the Fermi energy.

The sheet carrier density in graphene can be expressed using $g(E)$ as

$$n = \int_0^\infty g(E) f(E_F) dE, \tag{1.4}$$

where $f(E_F)$ is the Fermi-Dirac distribution given by $f(E_F) = \{1 + \exp[(E - E_F) / k_B T]\}^{-1}$, k_B the Boltzmann constant and T the absolute temperature. Then, the sheet carrier density n_i in graphene is given by:

$$n_i = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_F}\right)^2 \approx 9\times 10^5 T^2 \quad (\text{electrons/cm}^2). \tag{1.5}$$

From this equation, the sheet carrier density in graphene is shown to have a squared-power dependence to T, in contrast to semiconductors having an exponential dependence on T. The only material-specific parameter is the Fermi velocity v_F. The intrinsic sheet carrier density of $n_i \approx 8 \times 10^{10}$ cm^{-2} is obtained at room temperature.

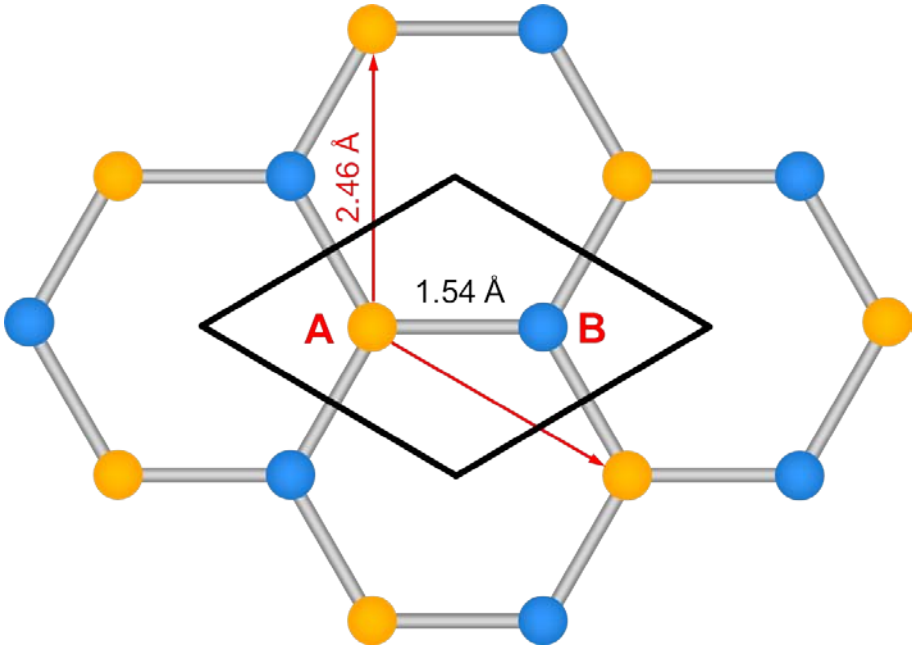


Figure 1.2. Lattice structure of graphene with basis of two atoms denoted as A and B.

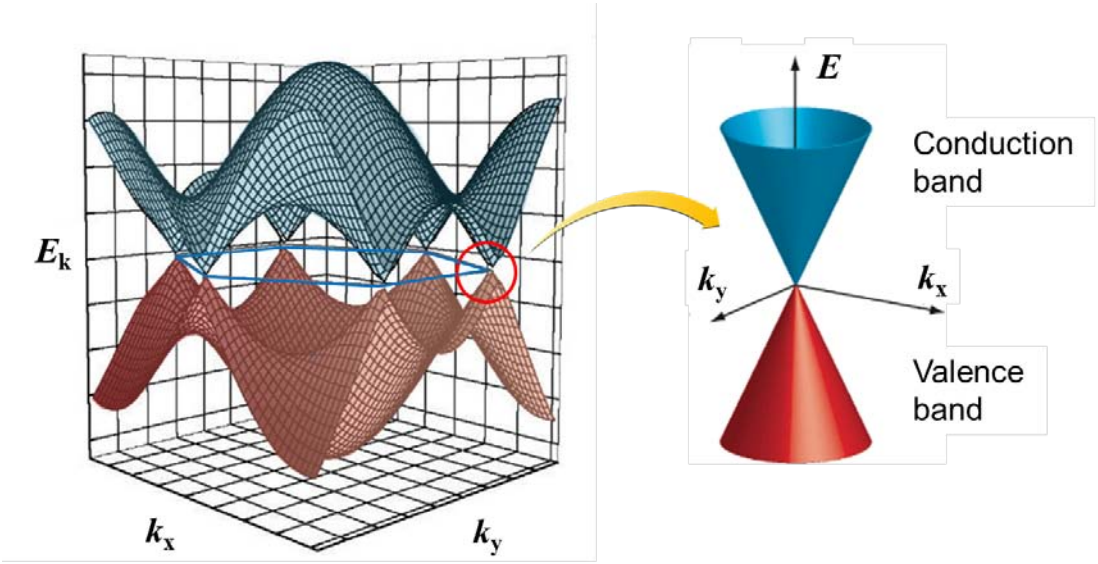


Figure 1.3. Band structure of graphene.

1.3 Graphene FET applications

As mentioned above, graphene has been attracting considerable interest for various applications such as transparent electrodes, sensors, solar cells, and transistors due to its outstanding electrical, optical and mechanical properties. Especially, a number of researchers have focused on development of graphene field-effect transistors (GFET) to replace conventional silicon-based devices because it is considered to show the highest charge carrier mobility of existing materials.

The first GFET device was reported by a Manchester group in 2004 [16]. They fabricated a back-gate type GFET by transferring an exfoliated graphene layer onto a Si substrate covered with a 300-nm SiO_2, and confirmed the occurrence of the field-effect modulation of carriers. Although these back-gated transistors have been very effective for the proof-of-concept purposes, they are not suitable for practical integrated circuits (IC) [17]. Practical GFETs need a top-gate structure. The first top-gated GFET was reported by Lemme *et al.* in 2007 using exfoliated graphene [18]. Since then, there have been numerous reports on top-gated GFETs using exfoliated graphene [19], graphene grown on metal substrates [20], and epitaxial graphene [21] to name a few. Even a wafer-scale graphene circuit was demonstrated in 2011 [22]. All these results strongly suggest possible use of graphene in the future electronic devices. Since its discovery in 2004, graphene has thus achieved splendid and skyrocketing developments in IC technology, which can be compared to other materials such as CNT, III-V compound semiconductor [17].

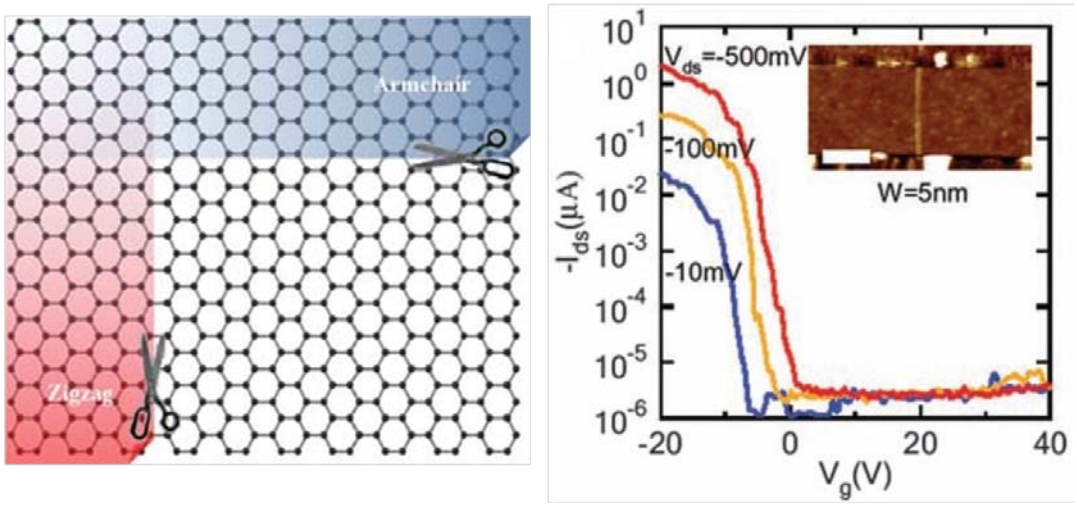
1.3.1 GFETs for logic applications

Graphene is a promising alternative to Si-based transistors owing to its exceptional electrical characteristics. They include ultrahigh carrier mobility and ability to form ultrathin channels, which permit both scaling down to even shorter channel lengths without detrimental short-channel effects as well as ability to realize high enough performance without further risky scaling down. There are however several issues in order for graphene to be applied in logic devices. The most important issue should be the fact that graphene is a semimetal with no band gap. In graphene, the valence and the conduction bands meet at a single point called Dirac point (Fig 1.3), which leads to miserably small on/off current ratios. To solve the problem, a number of researchers have been focused on development of bandgap engineering in graphene for applications of logic devices.

Among the most used techniques, graphene nanoribbon (GNR) with narrow width is one of the most promising approaches to open the bandgap (Fig 1.4) [23]. If width of GNR is below 10 nm, a bandgap of ~eV will be opened in graphene, which is enough to fabricate GFETs with on/off ratios of 10^7 or more at room temperatures [24]. To accomplish large scale production of GNR, numerous studies have been conducted such as electron beam lithographic patterning [25], cutting oxidized graphene [26], chemical synthesis [23], and scanning tunneling microscopy lithography [27].

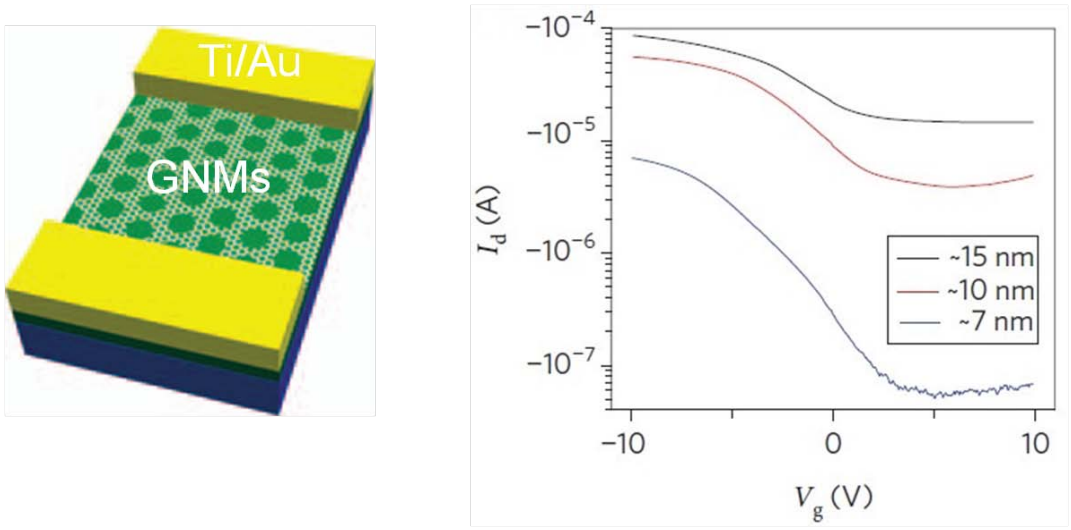
A variation of this GNR strategy is to use a graphene nanomesh (GNM) structure, in which an array of nanoholes are interconnected with GNR networks on the graphene sheet surface (Fig 1.5). This GNM-based FETs not only support the driving currents that are ~100 times greater than that of individual GNR based FETs but can be fabricated with much easier process as compared to GNR [28, 29].

Graphene bilayer FETs [30] have also been suggested to open the band gap in graphene. Although it has been extensively investigated experimentally and by device simulations, the on/off ratio of bilayer GFETs is not yet large enough for applications in logic devices.



(a) (b)

Figure 1.4. (a) Schematic of cutting the graphene sheet to obtain zigzag and armchair GNR (b) Transfer characteristics for a width of 5 nm and channel length of 130 nm GNR with Pd contacts and Si backgate. [24]



(a) (b)

Figure 1.5. (a) Schematic of GNM-FET (b) Transfer characteristics for GNMs with different estimated neck width of 15, 10 and 7 nm. [29]

1.3.2 GFETs for RF applications

As stated above, absence of the bandgap in GFET makes it difficult to switch off the current and is not best suitable for logic devices. In this context, graphene has found much more substantial interests in radio-frequency (RF) applications, in which a high on/off ratio is not essentially required. Significant progress has been therefore made on GFETs in RF applications. In realizing high performance in RF-FETs, it is not only the channel material with excellent carrier transport properties that matters, but minimizing the extrinsic parameters such as parasitic capacitance, the access resistance, and the contact resistance at the source/drain electrodes. Further scale down of the channel length is of course important. Since the first graphene RF transistors with a cut off frequency (f_T) of gigahertz was reported in 2008 [31], intensive efforts have been made on improvement of graphene-based RF transistors by changing the device structure to minimize the series resistances (contact and access) and the parasitic capacitance, and the gate length. Now the highest f_T reported for graphene RF transistors is 427 GHz [32]. However, this value is not as high as those of competing semiconductors such as InP high electron mobility transistor (HEMT) and GaAs metamorphic HEMT (mHEMT) (Fig.1.6) [17]. Therefore, we should develop further technologies for application of high performance graphene RF transistors.

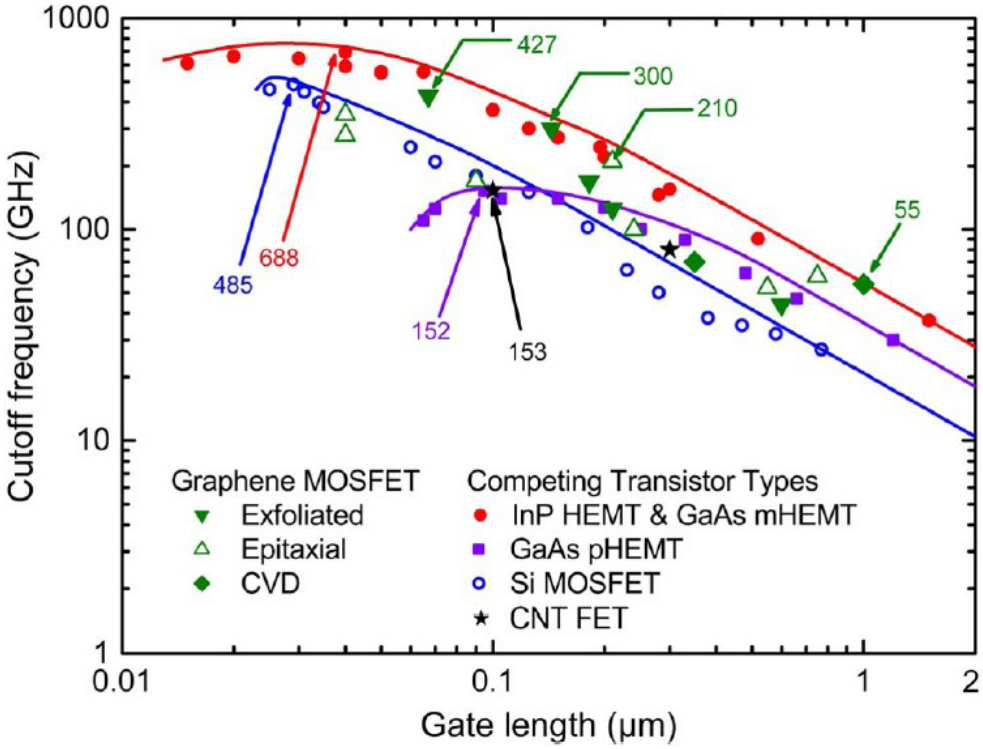


Figure 1.6. Comparison of cut off frequency between GFET and other devices, as a function of gate length L_G [17].

1.4 Challenges on GFETs

As stated above, graphene has been attracting explosive attention as a candidate for the new channel material owing to its extraordinary electrical properties, such as ultra-high carrier mobility and the 2D structure. As we have seen in section 1.3, GFET technologies have developed rapidly, which include the bandgap engineering, scaling of the gate length, novel device structures for high speed and frequency FET, in the past few years. As a result, GFETs are considered as a promising alternative for post-silicon electronics.

To develop high performance GFETs, however, many challenges still remain to be overcome for practical industrial applications. MOSFETs are basically three terminals devices, consisting of gate, source and drain. In Si technology, the gate electrode, metal or doped Si, is separated from the channel material via an insulating layer such as silicon dioxide or high-k materials. The charge carriers, electrons or holes, in the channel region are induced by an electric filed. When the drain voltage is applied, the carriers in the source (drain) region will flow through the channel to the drain (source) terminal. This is the performance of FET, i.e., control of the channel conductivity by the gate electric field and of the current between source and drain. With an extremely high mobility, graphene certainly has a great potential for high speed FETs. However, the excellent intrinsic properties of graphene are significantly deteriorated in actual GFETS, due to adverse effects caused during the fabrication process such as deposition of gate insulator and metals on graphene as well as annealing and lithographic processes. The GFET research is thus being focused on achieving high cut off frequency and high field effect mobility without losing the excellent properties of pristine graphene.

In FETs, f_T and μ_{FE} are expressed by the following equations, respectively.

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_G}, \tag{1.6}$$

$$\mu_{FE} = g_m \frac{L}{W}\frac{1}{C_{OX}V_d}. \tag{1.7}$$

As can be seen in equations 1.6 and 1.7, the transconductance (g_m), defined by the ratio of the drain current variation to that of the gate voltage, is proportional to both f_T and μ_{FE}. Thus, we notice that high f_T and μ_{FE} values are obtained by a high transconductance. For obtaining a high transconductance, it is in turn required to decrease the impurities in the channel region [33] and the access and the contact resistances [34,35].

Aiming at betterment of the performance in GFETs, I have focused on the following topics in this study:

a) Development of a novel gate dielectric deposition method, i.e., a solution process, for minimizing the doping, strain, defects in graphene during the gate dielectrics deposition.

b) Systematic investigation on the removal of contamination on graphene by use of oxygen plasma for low contact resistance.

c) Development of the overlapped S/D technology to reduce the access resistance.

1.5 Outline

The outline of this thesis is as follows. Chapter 2 describes development of a solution method for Al_2O_3 dielectric layers. Raman evaluation of the doping, strain, and defects in graphene caused by the formation of the solution-processed Al_2O_3 as well as its electrical characteristics such as dielectric constant, breakdown voltage and leakage current will also be presented. It will be shown that a modified solution process, consisting of insertion of an ultrathin Al_2O_3 seeding layer, spin-coating, oxygen plasma treatment, post-deposition annealing (PDA) at 250 ℃ for 2 hours, gives the minimum doping, strain and defects to graphene and its excellent electrical characteristics.

Chapter 3 describes the fabrication of top-gated GFETs using the modified solution process method. Evaluations will be made for various PDA temperatures. We obtain a high intrinsic carrier mobility of 8400 cm^2/Vs when the PDA temperature is set at 250 ℃, at which the defect density, hole doping, and stain in the graphene channel layer are minimized. The field-effect mobilities, however, are low in all devices. This can be attributed to a high series resistance consisting of the contact resistance between graphene and the metal electrodes and the access resistance under the ungated region between the gate and the source/drain electrodes.

Chapter 4 describes the effects of ultraviolet-ozone (UVO_3) treatment for reducing the contact resistance through removal of the interfacial contaminations. To remove the photoresist (PR) residue without introducing substantial damages to graphene, we carried out several analyses on graphene as a function of the UVO_3 time: the surface morphology by atomic force microscopy (AFM) and defects by Raman scattering spectroscopy. The contact resistance was evaluated independently by use of 2- and 4-point probe methods on back-gate GFETs. As a result, 3 min operation of the UVO_3 treatment was found to be the best; the surface morphology is identical with pristine graphene and the defect density was only slightly increased. The contact resistance on this graphene ranges from 100 to 400 Ωμm, which is comparable to one of the best reported values.

In chapter 5, the UVO_3 treated contacts will be applied to fabricate the overlapped S/D to top-gate devices for reducing the series resistance including the access and the contact resistance. After 3 min of the UVO_3 treatment, we obtain a lowest contact resistance of 900 Ωμm, comparable to one of the best reported values, as well as substantial betterment in the field-effect mobility.

Finally, chapter 6 describes the fabrication and characterization of top-gated GFETs, consisting of modified solution-processed gate dielectrics, UVO_3-treated contacts, and overlapped S/D to gate structure. As a result, highest transconductance of 358 μS and a field-effect mobility of 301 cm^2/Vs, not achievable by either the solution-gate or the UVO_3 treated contacts alone, have been obtained. These high transcondcutance and the field-effect mobility values are attributed to both increase of intrinsic mobility and reduction of the contact resistance. The intrinsic mobilities are actually as high as 8620 cm^2/Vs for holes and 8650 cm^2/Vs for electrons.

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2

Solution-processed gate dielectrics for GFETs

2.1 Introduction

One of the main reasons for the success of Si integrated circuits sits in the ideal interface between Si and its thermally grown oxide. The low interface trap density, the large bandgap offsets with Si, and the high breakdown reliability of the thermally grown silicon dioxide have made Si a platform for integrated circuits. These merits of Si more than compensate its mediocre carrier mobilities as compared to those of competing semiconductors such as Ge and GaAs [1,2]. The same situation applies to graphene, an emerging channel material for the next generation electronic devices. Despite its excellent carrier mobility [3,4] that leads to a wide variety of potential applications [5-7], the absence of graphene's natural oxide available as a gate insulator in GFETs leaves a critical issue toward industrialization of graphene in electronics. Deposition of dielectrics onto graphene, on the other hand, suffers difficulties from chemically inert (hydrophobic) nature of graphene [8,9], induced damages during plasma processings [10], and onsets of strain and doping during high temperature post-deposition annealings (PDA) [11,12]. Choice of right dielectric materials and of damage-free deposition techniques is key to realization of GFETs.

Doping during high-temperature annealing has been recently reported by Ryu et al.[13], who clarified that a substantial hole doping occurs in graphene under oxygen ambient at temperatures above 290 °C. They pointed out a correlation of this p-type doping to formation of bondings between oxygen and graphene's carbon atoms, which causes charge transfer from graphene to oxygen atoms.

If this is the case, lowering of the deposition and the PDA temperatures could substantially suppress the hole doping and enhance the mobility as well. In this context, we have noticed that a solution-process for gate dielectrics, consisting of a spin-coating of precursor liquid followed by PDA, should be advantageous. Solution-processed, or sol-gel, high-k gate dielectrics have been widely used in fabrication of organic thin-film transistors (OTFTs). No studies, however, have ever been made on this solution process to fabricate GFETs.

In this chapter, we examine the applicability of the sol-gel method for the gate dielectrics process in GFETs. We propose a "modified sol-gel method" (Fig 2.1), consisting of initial formation of natural oxide of Al, spin-coating of sol-gel precursor for Al_2O_3, oxygen-plasma treatment, and PDA at 250 ºC, as a process best suited for formation of GFET dielectrics.

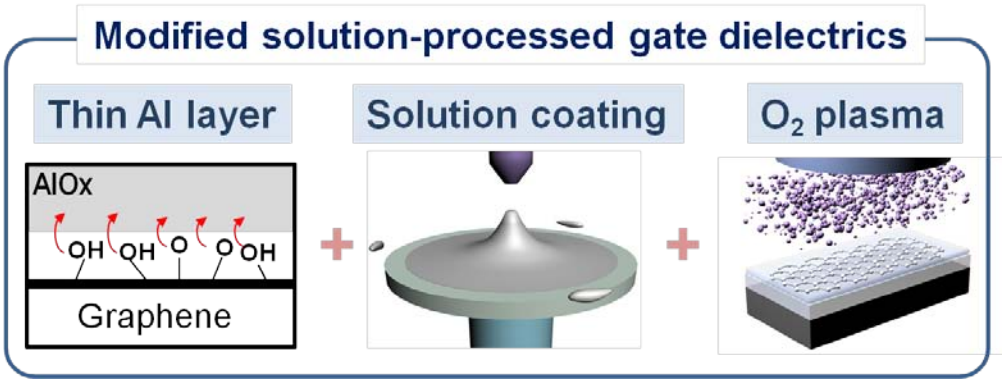


Figure 2.1. Composition of modified solution-processed gate dielectrics

2.2 Raman Evaluation of Doping and Strain in Graphene

2.2.1 Principle of Raman scattering spectroscopy

When incident light is applied to molecules, molecules will be excited into their higher energy states. The molecules in excited states drop to ground states through three mechanisms. Small particles with very small size compared to the wave length of incident radiation scatter the incident light almost equally into its backward direction. This type of scattering is called Rayleigh scattering (Fig 2.2(a)). Another type of scattering in which the scattered photon has either lower or higher energy than that of the incident light is called Raman scattering. Raman scattering effect was first reported by C. V. Raman and K. S. Krishnan. In Raman scattering, the difference in energy between incident and scattered photons corresponds to the energy required to excite a molecule to a higher vibrational mode.

If electromagnetic radiation is applied to molecules, energy is transferred according to the Bohr's quantum condition. We can express this using the following equation.

$$\Delta E = h\nu = h\frac{c}{\lambda}, \tag{1-1}$$

where $\Delta \boldsymbol{E}$ is the difference in energy between the two quantized states, h is the Plank's constant, c is the speed of light and λ is wavelength. This energy difference is identical with the energy difference between the two quantized states:

$$\Delta E = E_2 - E_1 \ , \tag{1-2}$$

where $\boldsymbol{E_2}$ is energy of excited state and $\boldsymbol{E_1}$ is energy of ground state. Therefore, molecules are excited by absorption of the energy $\Delta \boldsymbol{E}$ or de-excited by emission of energy $\Delta \boldsymbol{E}$. For the former case, the molecules absorb energy, and the scattered light loses just this amount of energy. The emitted photon has a lower energy than it had before. This type is called Stokes scattering (Fig 2.2(b)). On the other hand, if the already excited molecules lose part of their energy during their interaction with photons, the emitted photon has a higher energy than it had before. This type is called anti-Stokes scattering

(Fig 2.2(c)). The latter process is much more rare at room temperature, because most molecules are in their ground state. Thereby, Stokes scattering peaks are stronger than anti-Stokes scattering.

In spectroscopy, it is a common practice to use wave number ($\bar{\nu}$, cm^{-1}) instead of wavelength, ~~or~~ frequency, or energy of the light. The wave number and speed of light are described the following relation

$$\bar{\nu} = \frac{\nu}{c} = \frac{1}{\lambda}, \tag{1-3}$$

From equations 1-1, 1-2 and 1-3, variation of measured energy is expressed the following formula.

$$\Delta E = E_2 - E_1 = hc\bar{\nu}\ . \tag{1-4}$$

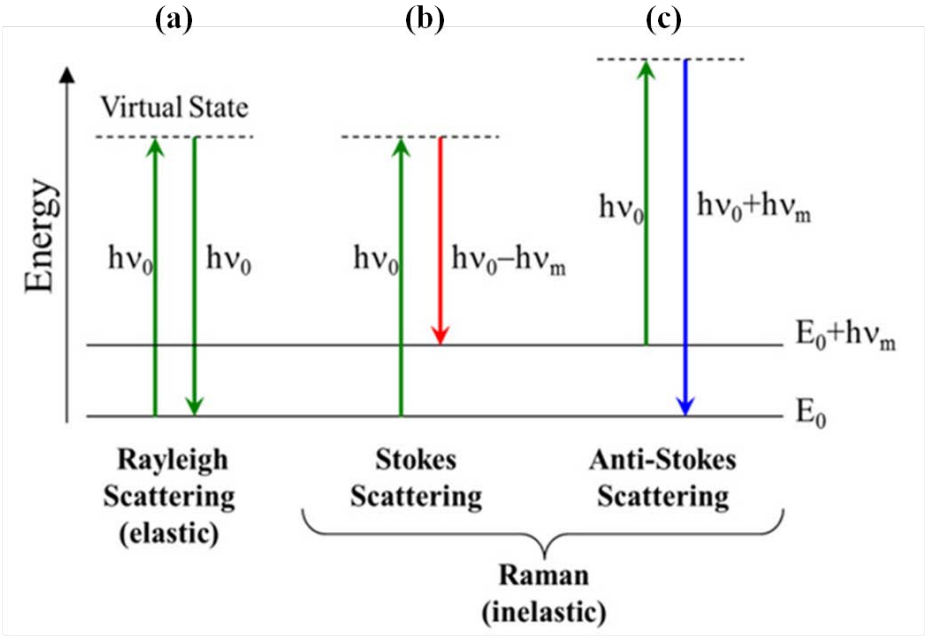


Figure 2.2. Quantum energy transitions for Rayleigh and Raman scattering.

2.2.2 Raman spectrum of graphene

By using Raman spectroscopy, we can obtain the phonon energy and the corresponding symmetry of the vibrational mode, resulting in obtaining the information of lattice structure of the material. In particular, Raman signal from graphene is very strong because graphene layer has a conical dispersion with a zero-band gap [14]. For this reason, we can easily detect the Raman signal of a graphene layer even though graphene has a single atom thickness.

Figure 2.2 shows a typical Raman spectra obtained for graphite and graphene. Two most intense features can be observed: the central peak is 1580 cm^{-1} and 2700 cm^{-1}, named G and G' (or 2D) band, respectively. In case of a disordered graphene or at the edge of graphene's grain, we also observe a D-band peak at around 1350 cm^{-1}, not shown in Figure 2.3.

The G band of graphene corresponds to a doubly degenerate phonon mode, E_{2g} symmetry, at the Brillouin zone (Fig 2.4(a)). The G band is only originating from a conventional first order Raman scattering process in graphene [15]. Figure 2.4 (b) shows the first-order G-band process in graphene. The incident radiation excites electrons from valence band to the conduction band. The excited electron is scattered by phonons of wave vector q and then electron and hole recombine, emitting scattered photon. Thus, the energy of difference between incident light and emitted photon corresponds to energy of phonon. In order to conserve the momentum, the mode at the Brillouin zone center, which located center of Γ point contributes to the Raman scattering because the light momentum is very small compared to the reciprocal Brillouin zone.

The G' band of graphene come from a second-order double resonant process [15]. As have seen Figure 2.5(a), the incident light excites electrons from valence band to conduction band. The electron is scattered by phonon of wave vector q from K to K' point. Since the Raman process must conserve energy and momentum, the electron must scatter back to K state before recombining with the hole. The electron thus is scattered back to the k state, and emits a photon by recombining with a hole at a k

state. This scattering process is second-order Raman scattering, involving two real electronic states of K and K' point and the G' peak of graphene is strongly generated in Raman spectrum.

The D band is due to A_1' vibration mode as shown in Figure 2.5 [16]. This mode can't be observed in complete lattice structure because of symmetry. The D band involves an phonon around the K-point like G' band. However, the D band requires a defect for the momentum conservation. Therefore, D band is rarely observed in exfoliated graphene with lower defect. On the other hand, in case of CVD (Chemical vapor deposition) graphene, D band can be generally examined in Raman spectrum.

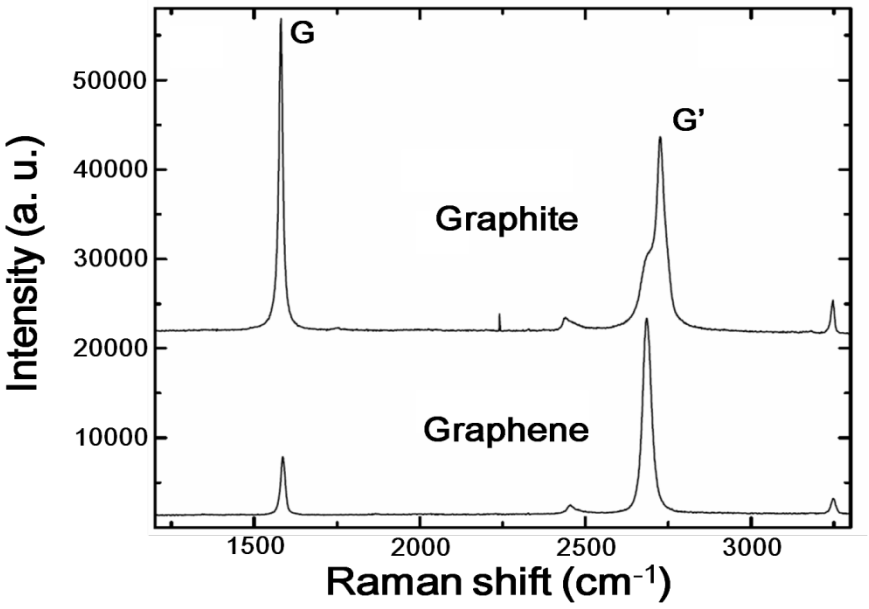
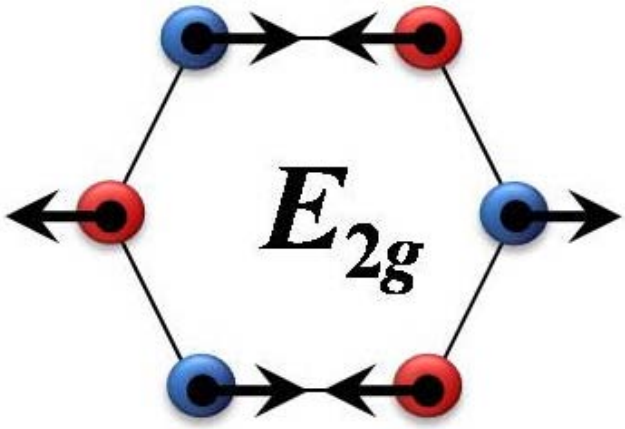
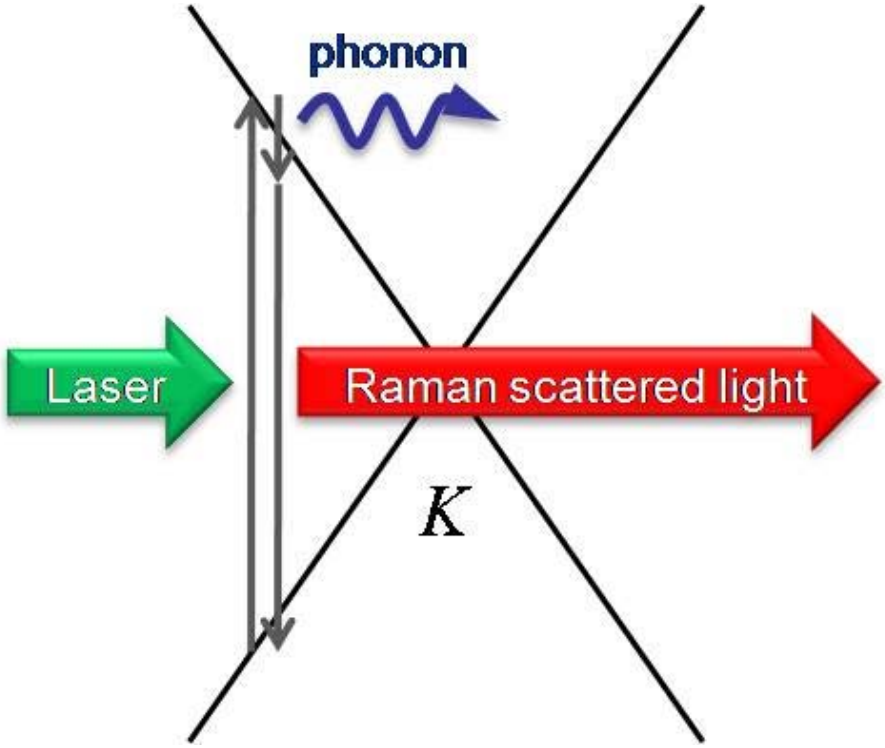


Figure 2.3. Raman spectrum of graphite and monolayer graphene [14].

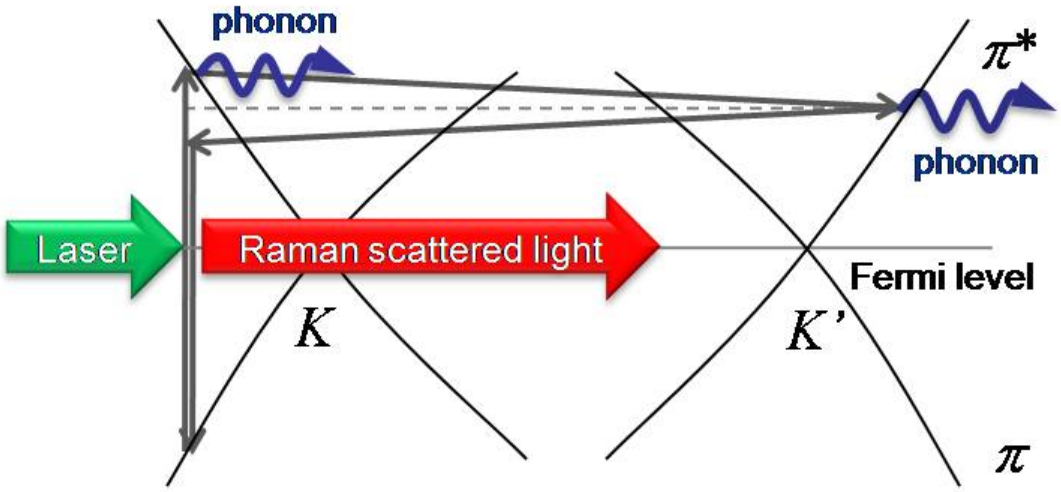


(a)

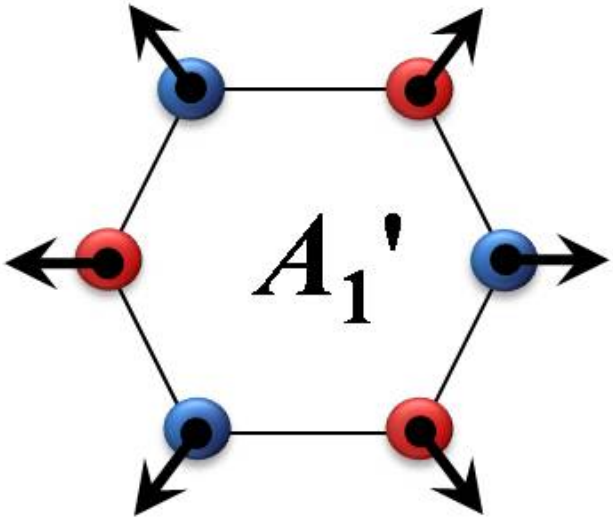


(b)

Figure 2.4. (a) G band vibration modes for the iTO (in-plane transverse optical) phonons at the Γ-point (b) First-order Raman scattering process.



(a)



(b)

Figure 2.5. (a) Second-order Raman scattering process. (b) D band A_1' vibration mode for the iTO phonon at the K-point.

2.2.3 Raman spectrum in doped graphene

Theoretically, the Fermi level is identical to the Dirac point in ideal, undoped graphene at 0 K. When extra electrons are induced in graphene, however, they will show strong effects on electrical properties because of the unique electronic structure of graphene. Figure 2.6 (a) shows the electronic band structures of undoped (upper) and p-type doped (lower) graphene. The Fermi level is significantly lowered in the latter even to accommodate small amount of holes because the density of state is very small in the vicinity of the vertex of the π- π^* electronic bands in this conical shape [17]. Figure 2.6 (b) shows the Raman G peak position as well as its peak width as a function of the gate voltage V_g measured at 295K [18]. The G peak position is shifted to higher energies with increase of the carrier (electron or hole) concentration. As one can observe, the peak position of the Raman G peak is quite sensitive to the carrier concentration.

Adiabatic Born-Oppenheimer approximation (ABO) can be valid when electrons are much lighter than nuclei (Fig 2.7(b)) [19]. In the dynamical sense, electrons can be regarded as particles that follow the nuclei motion ($u/\sqrt{2}$) adiabatically (Fig 2.7(d)), that is, they are dragged along with the nuclei without requirement of a finite relaxation time. However, ABO is no longer valid when the atomic motion is much faster than the electron's momentum relaxation time due to electron-phonon interactions [18]. In the case of graphene, the relaxation time of the G peak pulsation is ~ 3 fs, which is much smaller than typical electron-momentum relaxation time due to impurity, electron-electron and electron-phonon scatterings. Thus, excited electrons have no enough time to relax into the adiabatic ground state (Fig 2.7(c)). Therefore, electrons and phonons are strongly coupled, resulting in generating a strong G band frequency dependence on doping. The peak position and the intensity of the G' band also are changed by doping. However, the G' peak shows a different response to changes in the hole and electron concentrations; less sensitive than those of G peak due to no correlation with the non-adiabatic effects.

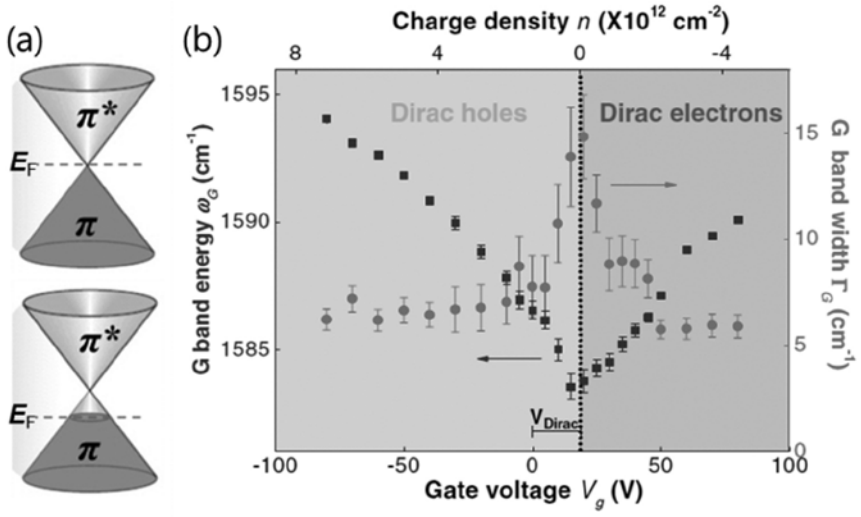


Figure 2.6. (a) Electronic structure of graphene: (up) undoped graphene (down) p-type doped graphene (b) G band energy (squares) and G band width (circles) as function of gate voltage and charge density [20].

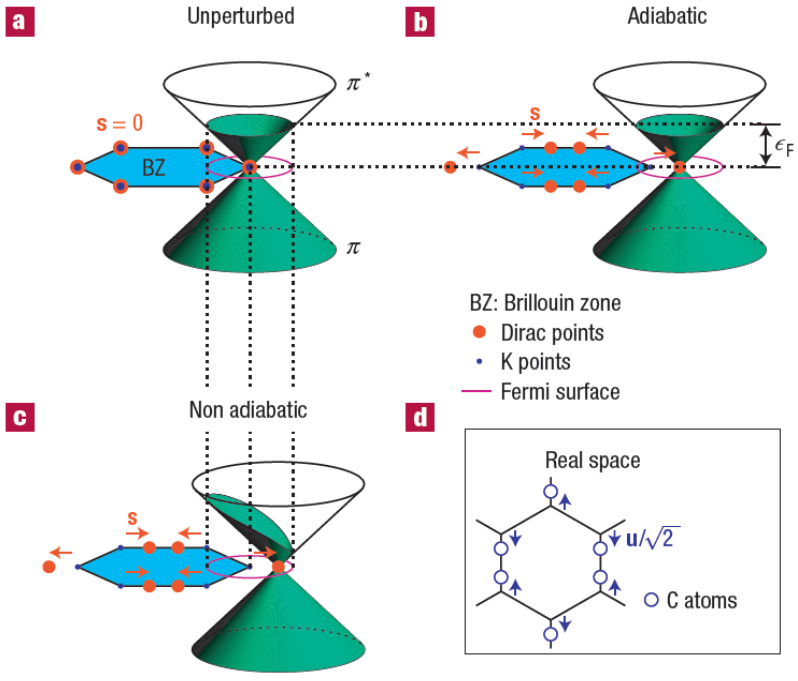
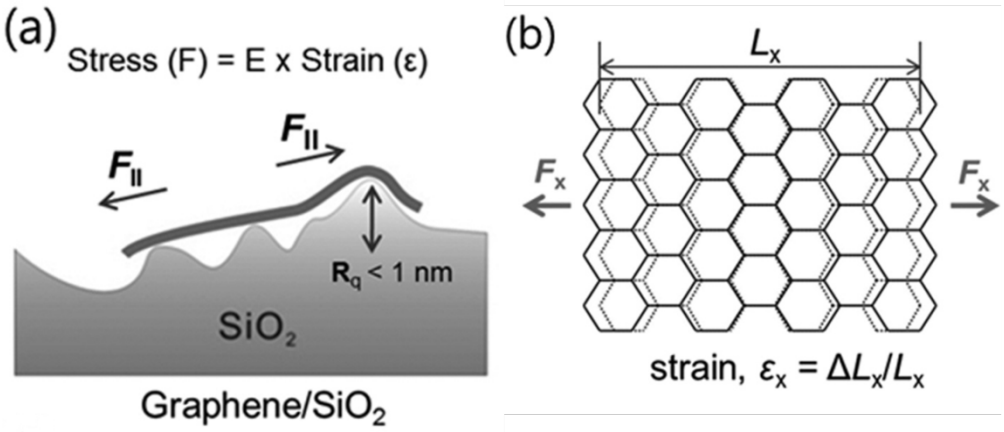


Figure 2.7. (a) Bands of perfect crystal; Bands in the presence of an E_{2g} lattice distortion within (b) ABO (c) non-adiabatic (d) Atomic pattern of the E_{2g} phonon [18].

2.2.4 Raman spectrum in strained graphene

Graphene is mostly used as a form attached to a substrate. Then stain can be induced after transferring exfoliated or CVD graphene to substrates or growing epitaxial graphene on SiC substrates. The graphene on SiC substrate grown epitaxially at temperatures above 1100 ºC exhibits compressive strain (ε) of around -1% at room temperature [21]. The graphene on SiO_2 substrates undergoes significant structural deformation with corrugation-induced strain at annealing temperature of 300 ºC [13]. Even graphene on SiO_2 substrates without annealing process is deformed due to strong adhesion with undulating substrates (Fig 2.8(a)) [13]. ε is defined as a relatively stretched or compressed length with applied stress to uniaxial direction, with $\varepsilon > 0$ for tensile and $\varepsilon < 0$ for compressive strain (Fig 2.8(b)). The electronic band structure is changed by strain in graphene, resulting in change of the D, G and G' peak positions in Raman spectrum. Generally, phonon frequency is decreased with increase of tensile strain. On the other hand, phonon frequency is increased under compressive strain. As a result, the frequency of Raman peak is linearly changed with biaxial strain as shown in Fig 2.8(c) [22].



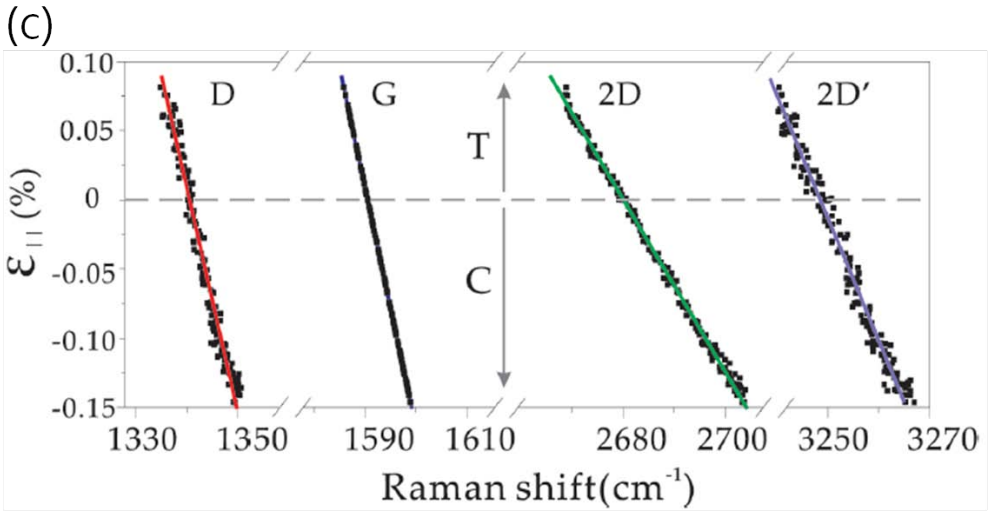


Figure 2.8. (a) Deformation of graphene on SiO_2 (b) Graphene lattice structure deformed by strain (c) D, G, 2D (G') peaks plotted as a function of the biaxial strain $\varepsilon_{\|}$ [22].

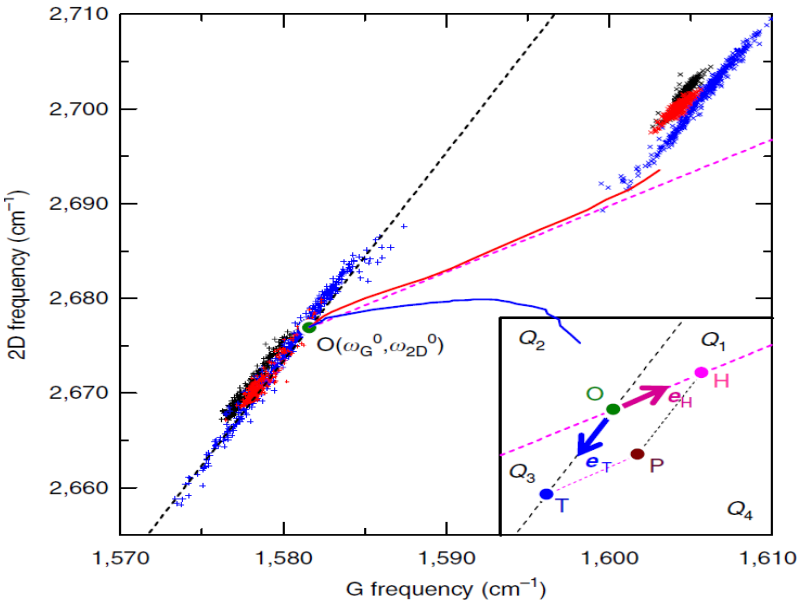
2.2.5 Separation of the impacts from charge doping and strain in graphene

As stated above, lattice vibrations in graphene are affected by various parameters, such as doping and strain, with high sensitivity. For this reason, Raman spectroscopy is widely used to measure the graphene's various properties with high sensitivity. The challenge, however, is that the phonon frequencies react simultaneously with various parameters. In particular, Raman frequencies of G (ω_G) and G' ($\omega_{G'}$) band, the most widely used ones, are dependent on both extra charges and strain as described above. Thus, the bimodal sensitivity of ω_G and $\omega_{G'}$ makes it difficult to independently determine either strain or charge density for quantitative interpretation.

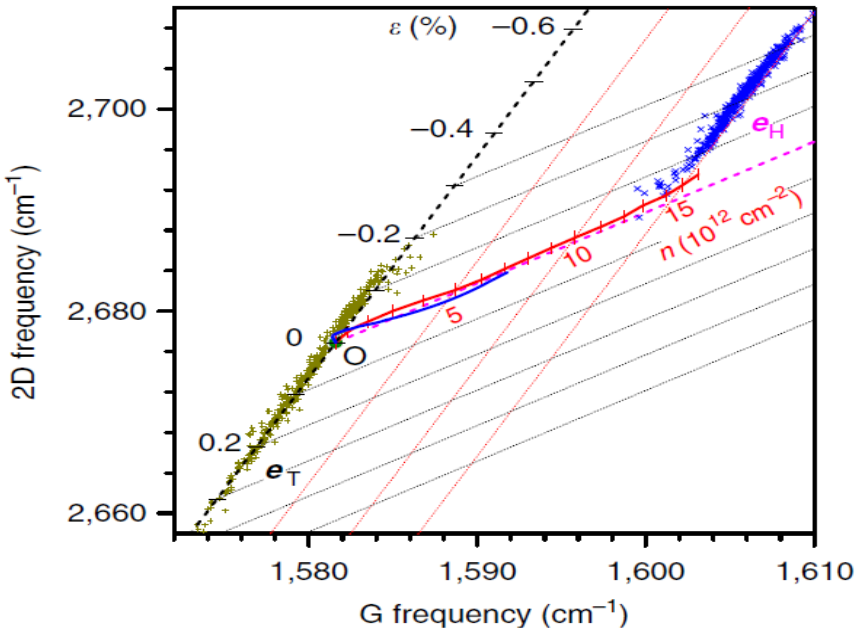
Recently, Lee *et al.* has reported that the effects of strain and charges can be separated from each other in terms of a correlation analysis of the two modes. It is based on the fact that the fractional variations in G and G' peak position caused by changing *n* (charge carrier concentration) are quite different from that is due to ε (strain) [11]. Lee *et al.*, set the G and G' peak positions (ω_G^0, $\omega_{G'}^0$) of a suspended graphene as the origin O of the ω_G versus $\omega_{G'}$ plot because the suspended graphene can be

viewed as nearly charge neutral and strain free (Fig 2.9(a)). In Figure 2.9 (b), the magenta dashed line is a linear fit obtained from a strain-free graphene with various hole concentrations. The blue dashed lines, drawn parallel to this line, therefore represent *equi*-strain lines. The hole doping induced by electrical gating leads to a quasi-linearity, $(\Delta\omega_{G'}/\Delta\,\omega_G)_n^{\,hole} = 0.70 \pm 0.05$, using two papers reported by the same group [23,24]. The black dashed line represents a theoretical prediction for a charge-neutral graphene under randomly oriented uniaxial stresses. The red solid lines, drawn parallel to this line, therefore represent *equi*-hole-concentration lines. $(\Delta\omega_{G'}/\Delta\,\omega_G)\varepsilon$ depends on the direction of the strain with respect to the crystallographic axes of graphene. G and G' mode of graphene under the stress splits into G^- (G'^-) and G^+ (G'^+) depending on the zigzag and arm-chair directions. While $(\Delta\omega_{G'}^{-}/\Delta\,\omega_G^{-})\varepsilon$ and $(\Delta\omega_{G'}^{+}/\Delta\,\omega_G^{+})\varepsilon$ of zigzag directions are 2.05 and 2.00, $(\Delta\omega_{G'}^{-}/\Delta\,\omega_G^{-})\varepsilon$ and $(\Delta\omega_{G'}^{+}/\Delta\,\omega_G^{+})\varepsilon$ of arm-chair directions are 1.89 and 3.00. $(\Delta\omega_{G'}/\Delta\,\omega_G)$. For the zigzag and arm-chair directions, the average is obtained as 2.02 and 2.44, respectively. As a result, we speculate $(\Delta\omega_{G'}/\Delta\,\omega_G)$ along any direction between the zigzag and arm-chair axes lie in the range 2.02-2.44. This value is in agreement with 2.2 ± 0.2 obtained from experiment. This analysis is useful to separate the effects of strain and excess charges in graphene materials and devices.

In this work, we use this analysis to be more quantitative on doping and strain in graphene during formation of gate dielectric.



(a)



(b)

Figure 2.9. (a) Correlation between the frequencies of the G and G' (2D) Raman modes of graphene. (b) The theoretical and experimental trajectories of (ω_G, $\omega_{G'}$) affected by hole concentration and strain.

2.3 Device Fabrication

Fabrication sequence of dielectric formation on graphene and MIM (Metal-Insulator-Metal) capacitor is illustrated in Figure 2.10.

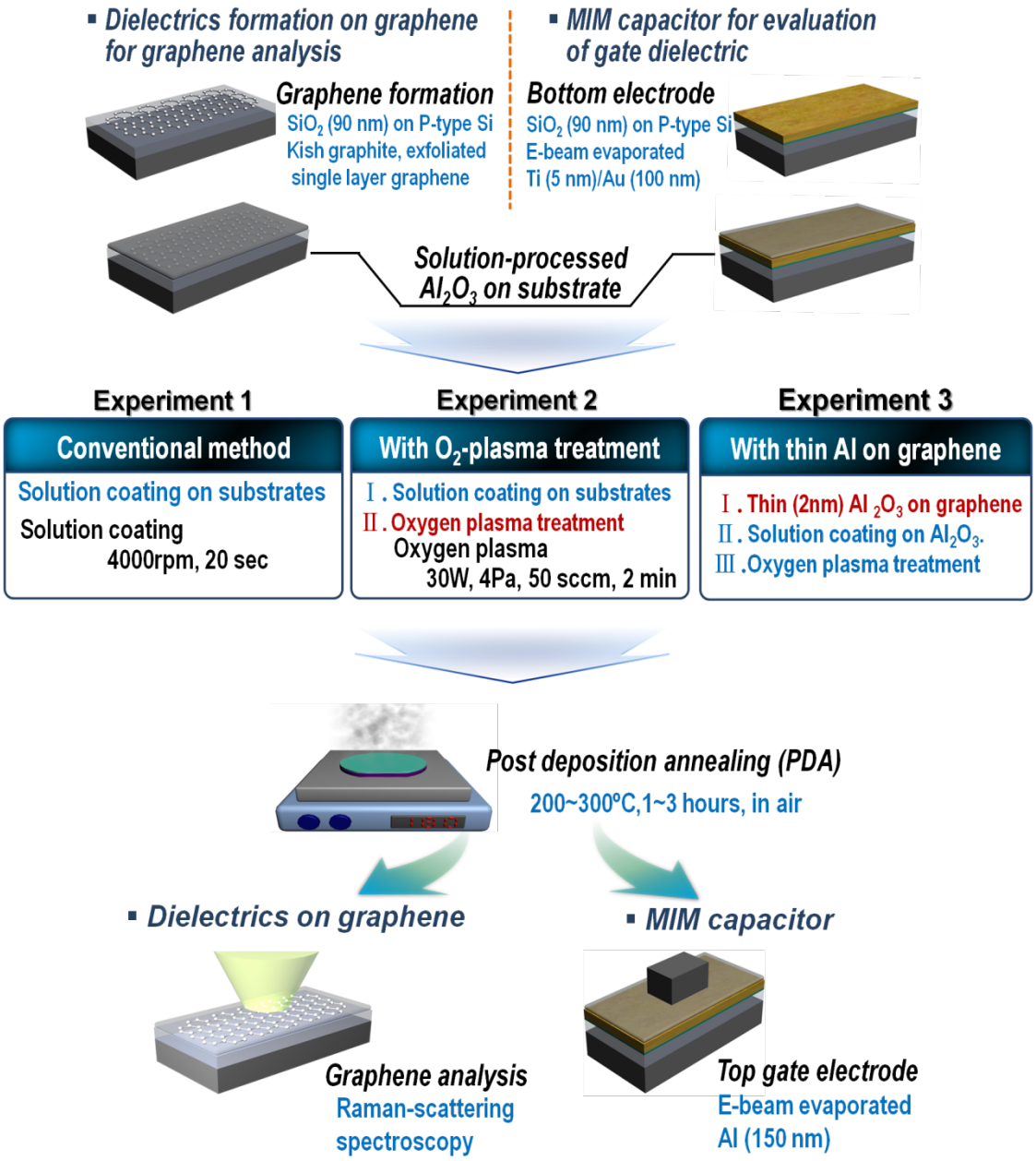


Figure 2.10. Fabrication sequences of dielectric formation on graphene and MIM capacitor.

Graphene layer was prepared by transferring a flake from kish graphite onto a Si substrate covered with a 90 nm-thick SiO_2 layer. In prior to the spin-coating of the Al_2O_3 precursor liquid, part of the samples experienced a deposition of an ultrathin (~2 nm) Al layer (Experiment 3). This is to form an initial natural oxide layer (seeding layer) on graphene. The Al_2O_3 precursor solution for the sol-gel method was prepared by mixing aluminum isopropoxide (Kojundo Chemical Laboratory Co., Ltd.) with xylenes and thinner. The concentration of the Al isopropoxide was 0.4 mol/L. The spin-coating was conducted at a rotation speed of 4000 rpm for 20 s at room temperature. Part of the samples were then exposed to an oxygen plasma for 2 min at 30 W operated at 4 Pa (Experiment 2, 3). Samples were finally annealed at 200, 250, and 300 °C in air for 1, 2, and 3 hours (PDA). Damages [25], dopings [18], and strains [26] of graphene induced during the dielectric film formation were characterized by Raman scattering spectroscopy. Dielectric properties of the solution-processed Al_2O_3 were evaluated by forming a metal-insulator-metal (MIM) capacitor on top of a SiO_2-covered Si substrates (inset of Fig. 1). Both the top electrode of Al (150 nm) and the bottom electrode of Au (100 nm) were deposited by using an e-beam evaporator. The thickness of the Al_2O_3 layers was measured by using spectroscopic ellipsometry. Electrical characteristics were measured at room temperature in the air ambient using Agilent B1500 semiconductor parameter analyzer.

2.4 Results and Discussion

Figure 2.11 shows the thickness of solution-processed gate dielectrics formed at 250 ℃ PDA as a function of Al_2O_3 solution/thinner ratios. After PDA at 250 ℃, thickness of solution-processed gate dielectrics formed by only Al_2O_3 solution is almost 30 nm. However, the thickness of gate dielectrics was decreased with increase of amount of thinner, 18, 10 nm at 1, 0.5 of Al_2O_3 solution/thinner ratios, respectively. However, a formed solution, at Al_2O_3 solution/thinner ratio of 0.3, couldn't deposit on graphene. We carried out to deposit on graphene using solution-processed gate dielectric of 10 nm thick.

Figure 2.12 shows the capacitance-voltage (*C-V*) characteristics of the solution-processed Al_2O_3 with and without oxygen plasma treatment, obtained in the high frequency (1MHz) regime using a MIM structure. The MIM structure is shown in the inset of Fig. 2.12 (a). As shown in the figure 2.12(a), the capacitances of the samples without the oxygen plasma treatments after 1, 2 and 3 hours PDA at 250 ℃ are 200, 300 and 315 pF, respectively. Since these values are insufficient for a FET operation, we decided to add post-coating oxygen-plasma treatment to accelerate the oxidation reactions at low temperatures. With the oxygen plasma treatment, a high capacitance of 400 pF or more has been obtained at even lower temperature of 200 ℃. At 250 ℃, the capacitance even exceeds 450 pF (Fig. 2.12 (b)).

Figure 2.13 (a) shows the dielectric constants of the solution-processed Al_2O_3, obtained from a *C-V* measurement operated in the high frequency (1 MHz) regime using the MIM structure. The thickness of the Al_2O_3 layer is 10 nm. The dielectric constants of the solution-processed Al_2O_3 (open squares), however, fall far below that of naturally oxidized Al_2O_3 even after a 3h PDA at 250 ℃. With the oxygen plasma treatment (solid squares), on the other hand, the dielectric constant as high as ~8.0 is obtained after a PDA at 250 ℃ for 2 hours. It should be noted that this value is comparable to that of ALD-grown, thin Al_2O_3 dielectric layer (7-9) [27] and is much higher than that of naturally

oxidized Al_2O_3 [28]. The mechanism of this oxygen-plasma treatment will be discussed at the end of this chapter. To test the breakdown properties, current density (*J*) - voltage (*V*) characteristics have been obtained (Fig. 2.13 (b)). All samples are processed with the post-coating oxygen plasma treatment as well as with PDA at 200 and 250 °C. The samples annealed at 250 °C showed markedly lower leakage currents ($<5\times10^{-9}$ A/cm^2 at 1MV/cm) and higher breakdown fields (3.5 MV/cm) than those annealed at 200 °C. These results indicate that the oxygen plasma treatment is very effective in improving the electrical characteristics of solution-processed gate dielectrics.

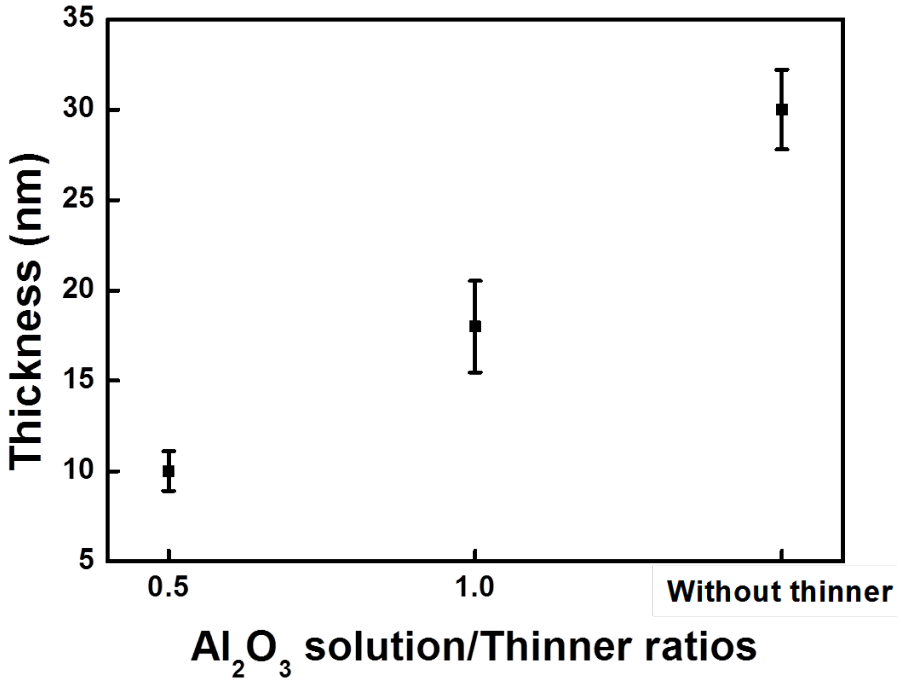
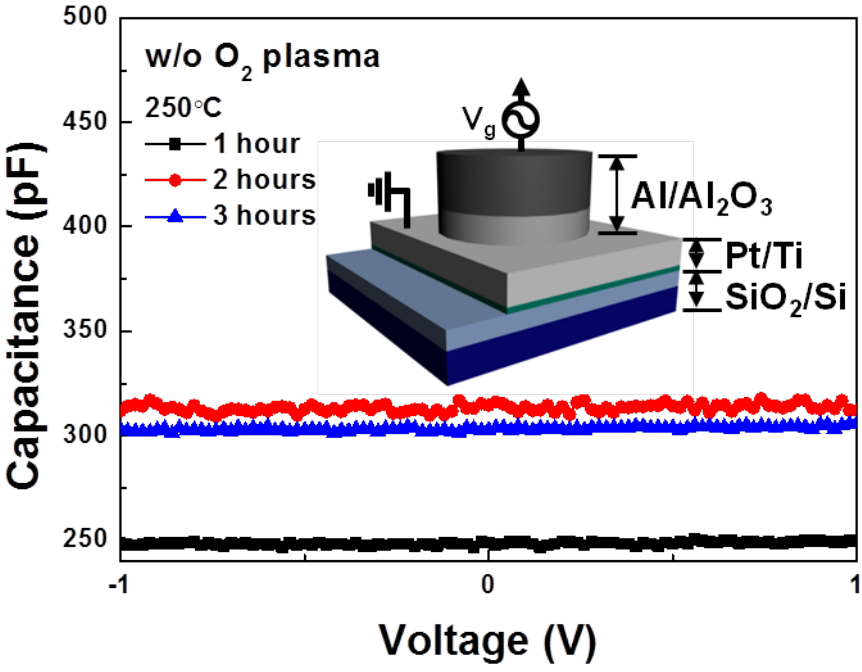
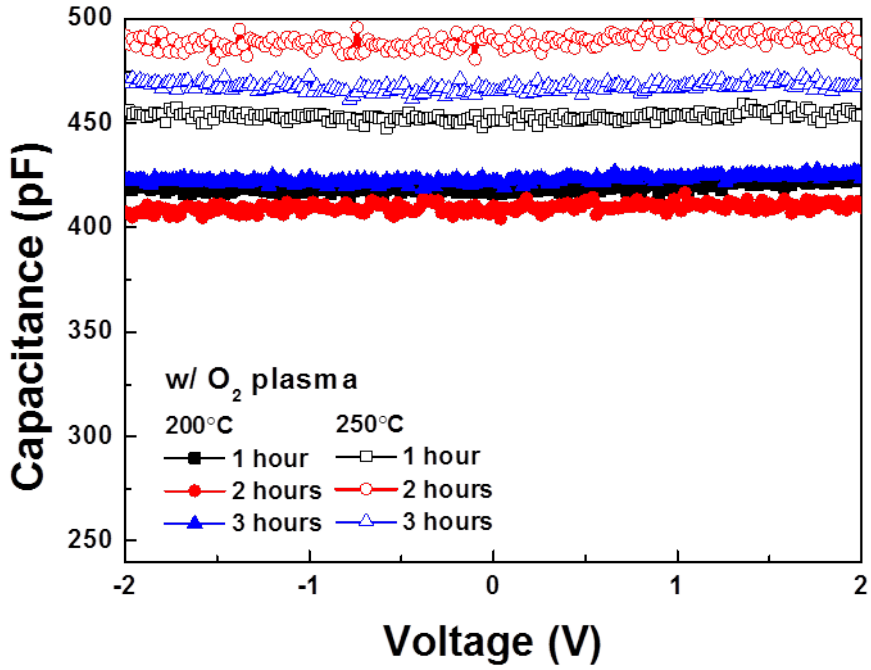


Figure 2.11. Thickness of solution-processed gate dielectrics formed at 250 °C PDA as a function of Al_2O_3 solution/thinner ratios.

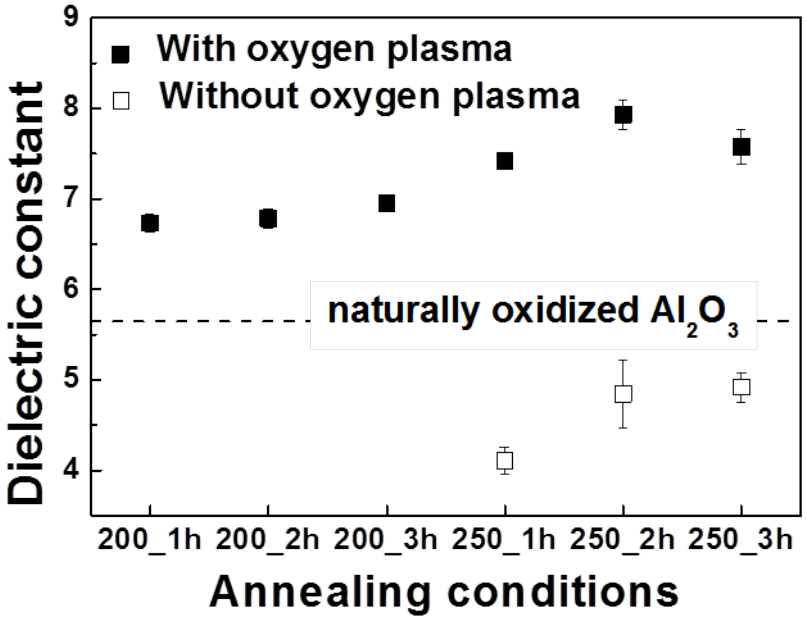


(a)

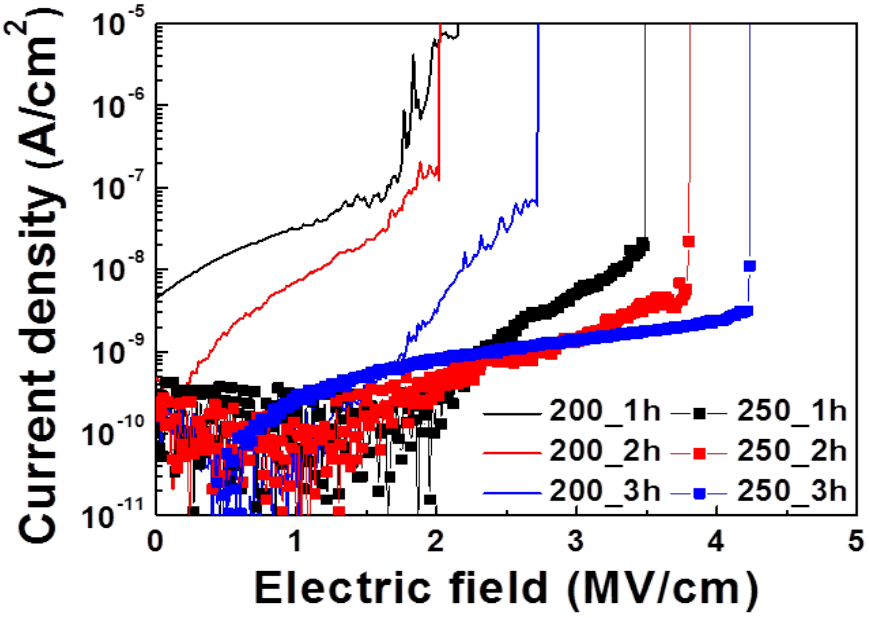


(b)

Figure 2.12. *C-V* characteristics of solution-processed gate dielectrics (a) without and (b) with oxygen plasma treatment.



(a)



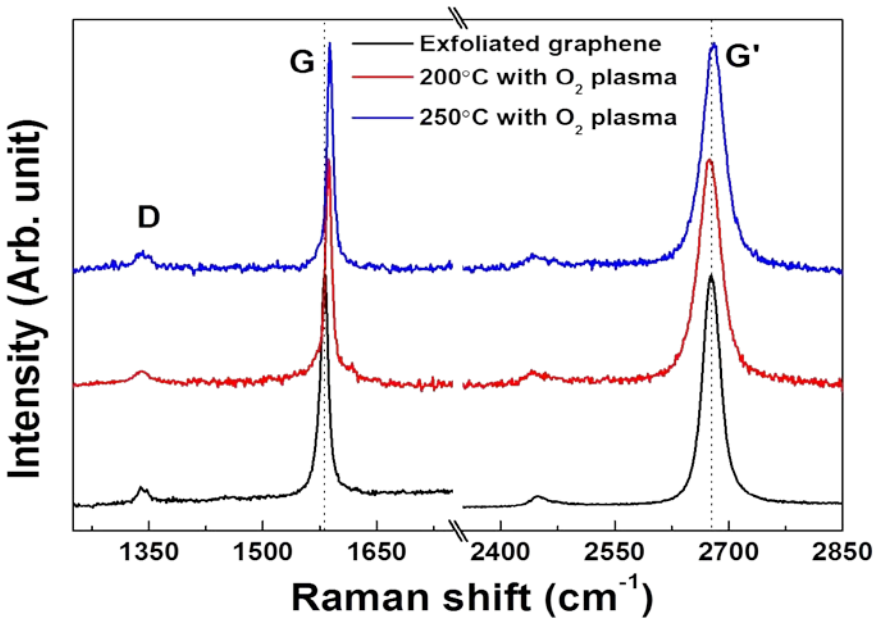
(b)

Figure 2.13. (a) Dielectric constant, as determined from *C-V* measurement, of the Al_2O_3 film with (solid squares) and without (open squares) oxygen plasma treatments as a function of the PDA temperature and time. (b) *J-V* characteristics of the Al_2O_3 MIM capacitor with oxygen plasma treatment.

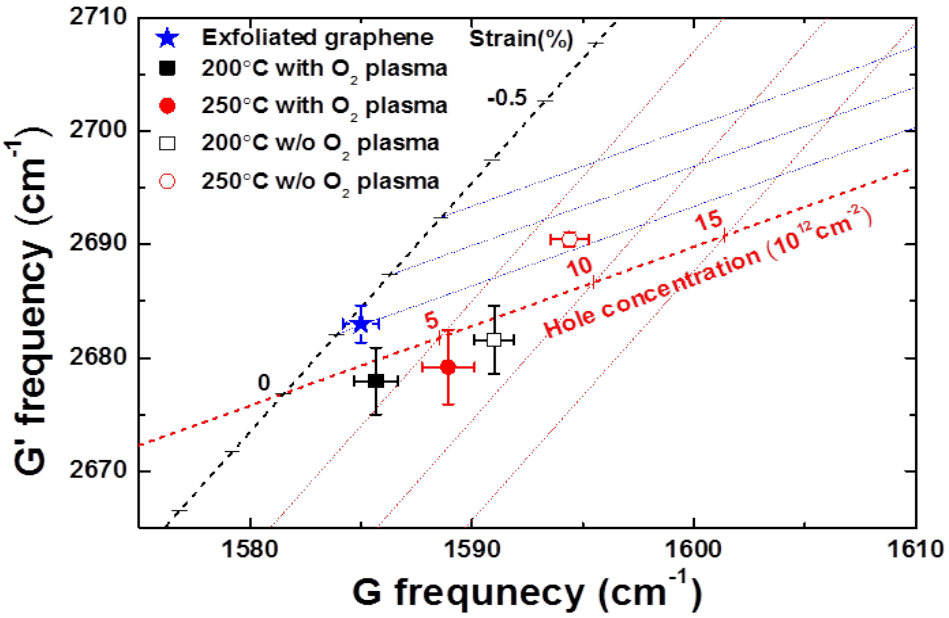
Although the dielectric and the breakdown properties of the dielectrics fabricated with solution/oxygen-plasma method seem quite promising, the doping levels are not yet ideal. Fig. 2.14 (a) shows Raman spectra of the samples annealed at 200 and 250°C for 2 hours after the oxygen plasma treatment, compared with that of exfoliated graphene. The main features of the spectrum, i.e. the positions of the D and G' peaks as well as the intensity of the D peak, are almost the same among the three samples. The only difference can be found in the G peak position, which noticeably blue-shifts with the increasing PDA temperature. A blue shift of the G band, in the absence of the G'-band shift, indicates a p-type doping [23]. The G band position is however a function not only of doping but also of strain. In the case of strain, the G' peak also shows a shift [11]. We have therefore plotted in Fig. 2.14 (b) the position of the G' peak against that of the G peak, both of which are known to be expressed by linear combinations of both doping and strain levels in graphene [11]. The magenta dashed line is a linear fit obtained from a strain-free graphene for various hole concentrations [24]. The blue dashed lines, drawn parallel to this line, therefore represent equi-strain lines. The black dashed line represents a theoretical prediction for a charge-neutral graphene under randomly oriented uniaxial stresses [29]. The red solid lines, drawn parallel to this line, therefore represent equi-hole-concentration lines. For oxygen-plasma-treated samples shown in solid symbols, the hole concentration increases with increasing PDA temperature, from 3×10^{12} to 6×10^{12} cm^{-2}. Samples without the oxygen-plasma treatment shown in open symbols, on the other hand, shows a strong hole-doping up to 7×10^{12} cm^{-2}.

As we have seen, the solution-processed dielectric film with the oxygen plasma treatment shows excellent dielectric properties as well as lower hole dopings. The hole doping levels of $3\text{-}6\times10^{12}$ cm^{-2}, however, are still higher than that of exfoliated graphene (1×10^{12} cm^{-2}). Since dopings sharply deteriorate the carrier mobility of graphene channel [30] we need to decrease the doping to even lower levels. Our working hypothesis here is that the p-type doping should originate from oxygen-related

species adsorbing on graphene before the gate-oxide deposition. Pirkle *et al.* [30] have recently demonstrated that a deposited Al layer on graphene reacts with such oxygen-related ad-species on graphene, resulting in the formation of AlO_x at the Al/graphene interface. Moreover, previous studies of Al thermal oxidation [32] show that the Al_2O_3 thickness on Al saturates at ~2 nm or less for oxidation temperatures lower than 300 °C. These findings suggest that an ultrathin (~2 nm) layer of Al may most effectively consume all the oxygen-related ad-species on graphene to become AlO_x. We have therefore decided to investigate the impacts of the natural oxide insertion, in prior to the solution-process formation of Al_2O_3, on the p-type doping in graphene. Figure 2.15 (a) shows the Raman spectra. The close-up of the D peak indicates that the D-peak rarely appears up to 250 °C regardless of the PDA time. At 300 °C the D peak markedly appears, indicating onset of damages. The G and G' peaks for 200- and 250 °C-annealed samples concurrently show a slight red shift with the PDA time. For the 300 °C-annealed sample, on the other hand, blue shifts are observed for both G and G' peaks. To be more quantitative, we have again plotted the G' peak position against the G peak position in Fig. 2.15 (b). The samples annealed at 200 and 250 °C are located in the vicinity of the charge neutral line, similar to suspended graphene [33]. High carrier mobilities can therefore be expected for the graphene under these dielectrics. The samples annealed at 300 °C, on the other hand, are strongly hole-doped up to 5×10^{12} cm^{-2} or more. This can be related to onset of oxygen penetration to graphene through thinner portions and/or pin-holes of the Al natural oxide layer having substantial surface roughness (~1.2 nm). This point will be discussed later. Based on these results, we propose a modified solution process for the gate dielectrics on graphene. The process consists of initial formation of natural oxide of Al (seeding layer), solution-process of Al_2O_3, oxygen plasma treatment, and PDA at 250 °C.

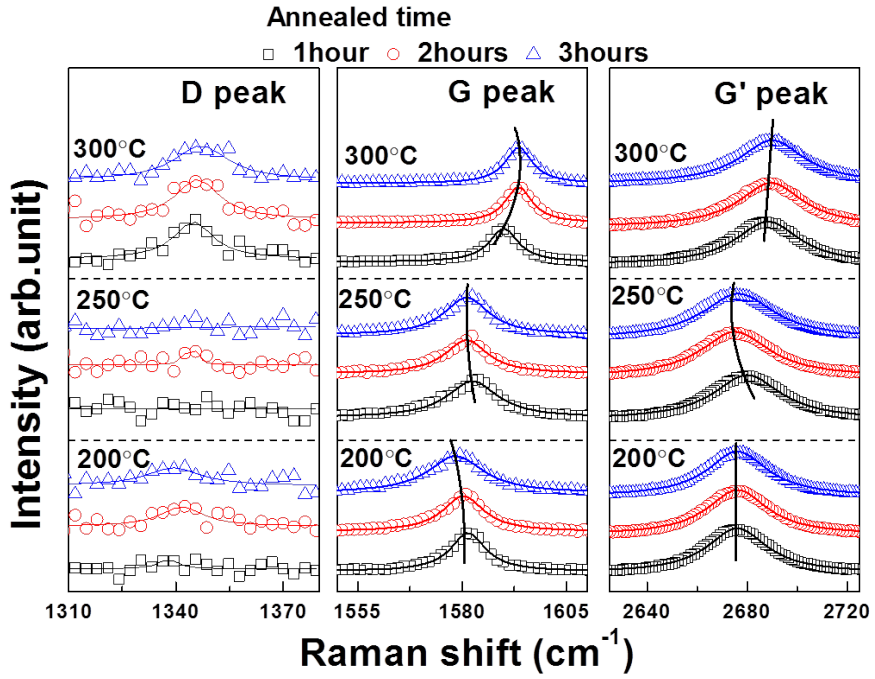


(a)

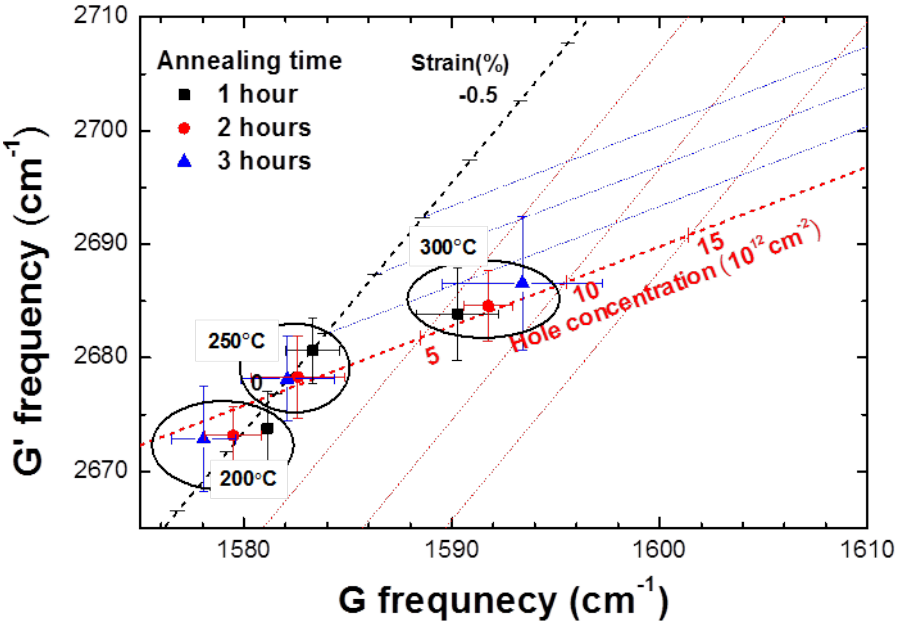


(b)

Figure 2.14. (a) Raman spectrum of oxygen-plasma-treated films as a function of the PDA temperature. (b) G' peak position versus G peak position of the films with (solid squares) and without (open squares) oxygen plasma treatment for several PDA temperatures.



(a)



(b)

Figure 2.15. (a) Raman spectrum of Al_2O_3 on graphene with initial insertion of natural oxide of Al. (b) G' peak position versus G peak position as a function of the PDA temperature and time for Al_2O_3 on graphene with initial insertion of thin Al layer and with oxygen plasma treatment.

Figure 2.16 shows the AFM images of the samples after deposition of (a) Al (2 nm) thin film and (b) the solution-processed Al_2O_3 films on the Al (2 nm) thin film with PDA at 250 ℃, both on graphene. In Fig 2.16 (a), the surface consists of Al clusters and the RMS (Root Mean Square) surface roughness is as large as 1.26 nm. In Fig. 2.16 (b), on the other hand, the RMS surface roughness of the solution-processed Al_2O_3 is strongly reduced to 0.34 nm. Based on this observation, a possible mechanism for the betterment of the dielectric properties of the Al_2O_3 film by use of the present modified solution-process method is discussed in Fig. 2.17. After the Al deposition and the spin-coating, the cross-section of the layers may look like the one shown by the close-up image shown in (I). The Al thin layer is sandwiched by oxygen atoms from both sides: one from the organic components in the solution film from the top side and the other from the remnant oxygen-related ad-species on the graphene surface from the bottom side. Part of these oxygen-related species can react with the Al film to form AlO_x. When this spin-coated film is exposed to the oxygen plasma (II), the active oxygen radicals in the plasma will react with the precursor molecules in the spin-coated film, commencing the formation of Al_2O_3 (III). During PDA at 250 ℃, the oxygen species in the solution-processed precursor layer may diffuse into Al thin film, but the lack of thermal energy, as depicted by a thinner saturating oxide thickness (~0.5 nm) of Al at this temperature [32], may impede further diffusion of oxygen-related species to graphene. When the annealing temperature is increased to 300 ℃, however, the higher thermal energy of the oxygen species, as indicated by a thicker saturating oxide thickness (~1.0 nm) of Al at this temperature [32], will allow their diffusion to graphene surface. Thinnest portion of the Al layer as well as pin-holes are suggested as a possible diffusion path to graphene. This accelerated diffusion of oxygen-species to graphene accounts for the observed doping and defects in graphene (IV). Without assist of this oxygen plasma, on the other hand, higher PDA temperatures are required to remove the organic fragments, which will drive onset of doping, strain, and mobility degradation of graphene [30,34].

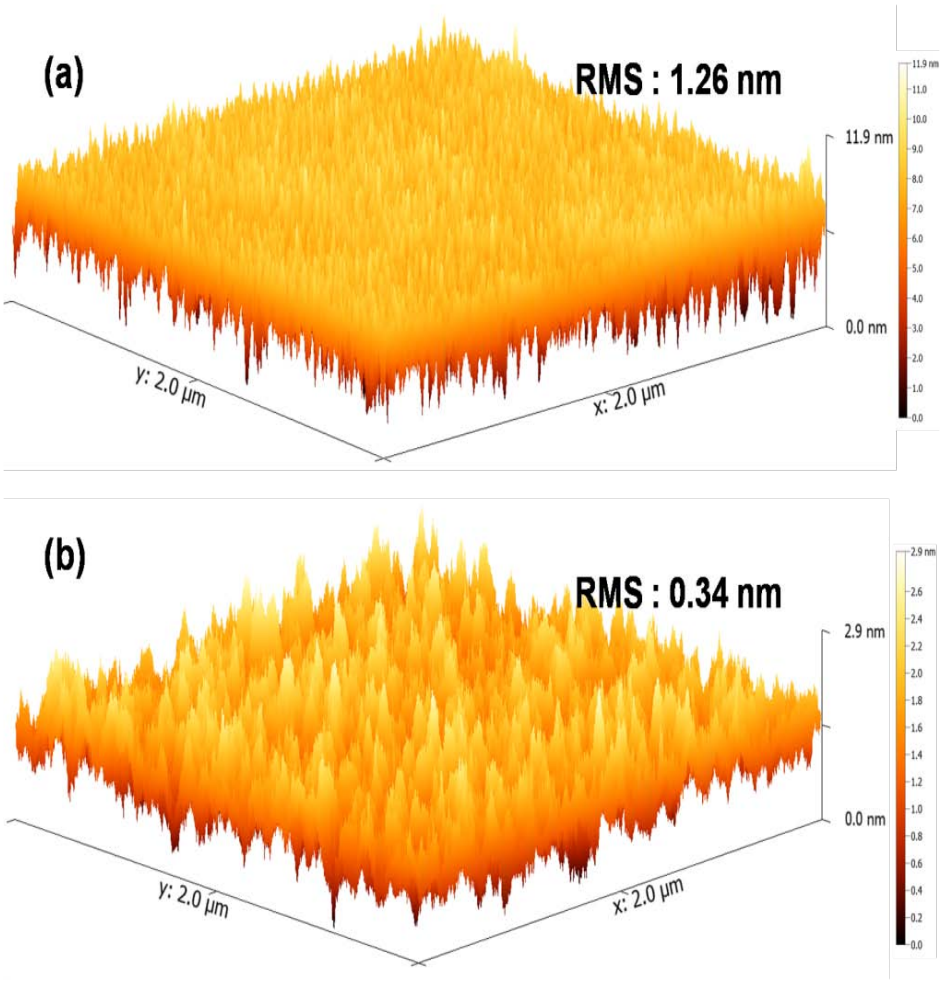


Fig 2.16. AFM images of (a) Al (2 nm) deposited film on graphene and of (b) solution-processed Al_2O_3 film on Al (2 nm) with oxygen plasma and PDA at 250 °C.

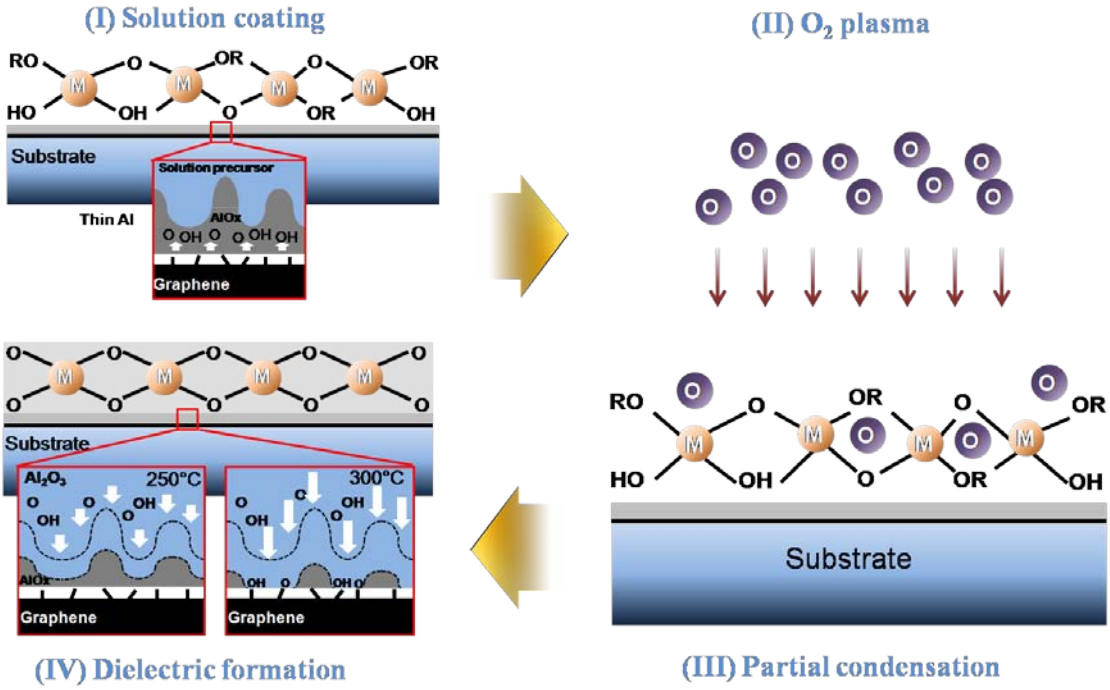


Fig 2.17. Schematic of the mechanism for the oxygen plasma growth for solution-processed Al_2O_3.

2.5 Conclusion

Based on a solution-process method, we have succeeded in fabrication of a gate dielectric Al_2O_3 thin film on graphene with a sufficiently high quality. We propose a modified solution-process method, which consists of initial formation of ultrathin Al natural oxide, spin-coating of Al_2O_3 precursor liquid, oxygen plasma treatment, and PDA. It was found that the PDA at 250°C for 2 hours gives a minimum doping and strain to graphene and a highest dielectric constant to Al_2O_3. Although this study was focused on minimizing the doping and strain in graphene during the gate-stack process, the strongly temperature-dependent doping found in this study can be utilized in controlling the threshold voltage of GFETs.

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3

Electrical properties of GFETs with solution-processed top-gate

3.1 Introduction

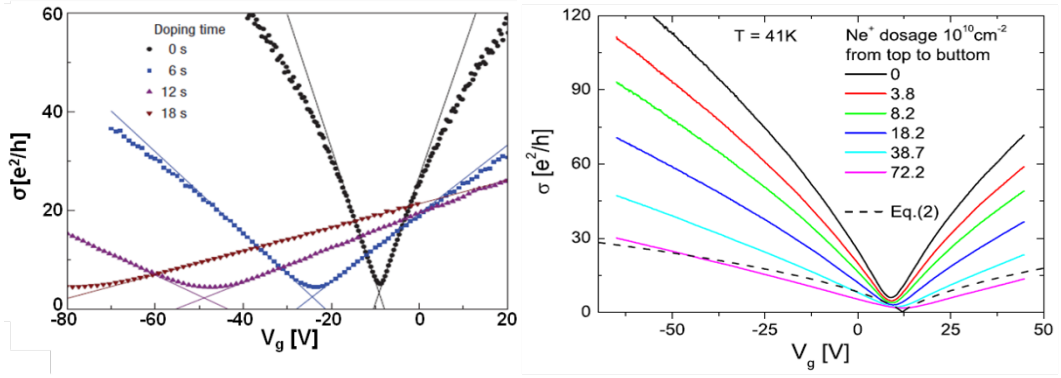
Graphene has attracted much attention as a new channel material for next generation electronic device applications due its extremely high mobility and electric-field induced carrier density modulation. For these reasons, remarkable development has been made on graphene-based electronic devices in the past few years. Actual graphene FETs (GFETs), however, suffer significant degradation of pristine properties due to impurities [1], defects [2], dielectric environment [3,4] in graphene sheet during the fabrication process of GFETs.

As stated above, it was reported that the mobility significantly decreases and the gate voltage of the minimum conductivity (Dirac point) shifts to more negative values with increase of potassium doping, which means increase of charged impurities (Fig. 3.1(a)). As the defect density increases, the mobility also significantly decreases and the reduction of σ_{min} by doping is roughly proportional to the reduction of the mobility (Fig. 3.1 (b)). Furthermore, it was reported that charge carrier mobility is dependent on dielectric constant surrounding the graphene sheet. There are two competing mechanisms. The impurity scattering can be strongly suppressed by using high-k dielectrics, while increasing the phonon scattering. By using low-k dielectrics, on the contrary, impurity scattering is dominant but the phonon scattering is lower than that of high-k dielectrics. The limitation of the

carrier mobilities (~10^4 cm^2/Vs) is attributed to the trade-off between the impurity scattering and the phonon scattering as shown Fig. 3.2 [3]. The gate dielectrics process in GFETs, in this respect, is required to minimize the defects and the doping in graphene during the gate dielectrics formation and to choose the dielectric materials with an appropriate dielectric constant.

In the previous chapter, we discussed the possibility of applying the solution-processed gate dielectrics in GFETs. We found, by using Raman-scattering spectroscopy, that defects, dopings, and strains are introduced in graphene during formation of gate dielectric films. It was however shown that the excellent electrical characteristics with minimum defects, dopings, and strains in graphene can be obtained by inserting an initial natural oxide seeding layer onto graphene, by adding an oxygen plasma treatment, and by tuning the PDA temperature. With the high suppression of hole doping and defects, we now have good reasons to expect high carrier mobility [5,6]. Few studies, however, have been made on these solution-processed gate dielectrics to fabricate GFETs [7]. In particular, no studies have been reported on the top-gated GFETs (TG-GFETs) with the solution-processed gate dielectrics.

In this chapter, fabrication of the TG-GFETs (Fig 3.1) with the solution-processed gate dielectrics will be described. It will be demonstrated experimentally that the Dirac point shift (doping) is closely related with decrease of the intrinsic carrier mobility in graphene.



(a) (b)

Figure 3.1. Conductivity versus gate voltage curves for (a) the pristine sample and three different doping concentrations [1] (b) pristine graphene and following Ne^+ ion irradiation doses with cumulative exposures indicated [2].

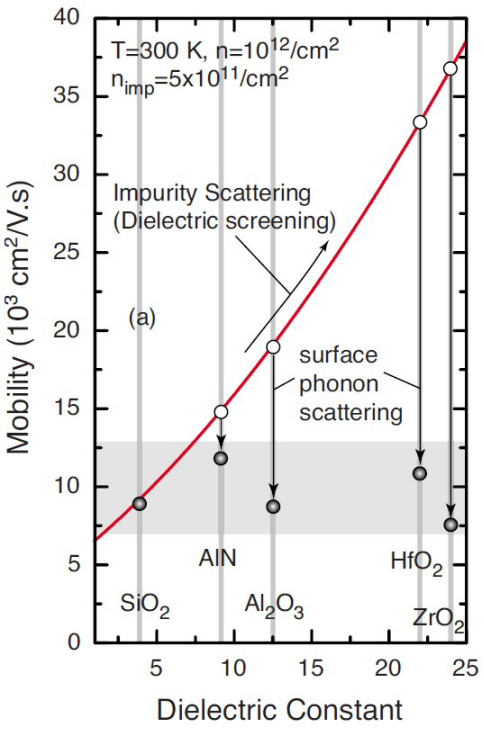


Figure 3.2. Carrier mobilities in graphene as a function of gate dielectric constant [3].

3.2 Definition of intrinsic mobility in GFETs

In discussing the impacts of deposition of gate dielectrics on the carrier mobility in graphene, we should firstly consider how to reasonably determine the mobility in GFETs. This is related to the choice of mobility models. Among various mobility models for GFETs, a common one is to select the linear regime, away from the Dirac point, in the transport σ versus V_g curve. We fit the curve with $\mu = \Delta\sigma/(C_g \Delta V_g)$ [8], where μ is the carrier mobility. The extracted mobility is then independent of the carrier density. The determination of the linear regime is somewhat irrational because the actual transport curves are nonlinear. Another method for extracting the mobility in GFET is to fit with $\mu = \Delta\sigma / C_g (V_g - V_{dirac})$ [9]. The charge carrier density n_G is induced by the gate voltage V_g, which is given by the following formula $n_G = \left(\frac{C_g}{e}\right)(V_g - V_{dirac})$, where C_g is the gate capacitance per unit area, e is the electron charge, and V_{Dirac} is the voltage at the minimum conductivity point (Dirac point) in the transport curve. This mobility depends on V_g, or the carrier density due to the nonlinearity of the transport curve. However, in the vicinity of the minimum conductivity, σ increases weakly on V_g, by the electron-hole puddle due to disordered distribution in charged impurities located at the interface between graphene and the gate dielectrics. Therefore, the carrier density n_G is not well defined in the vicinity of the minimum conductivity because of the potential fluctuations [10,11]. Having this in mind, the total carrier concentration in the graphene channel is given by

$$n_{tot} = \sqrt{n_0^2 + n[V_g]^2}\,, \tag{3.1}$$

where n_0 is the carrier density at the minimum conductivity. As a result, the total resistance (R_T) of GFET is expressed as the sum of the gate-voltage-dependant resistance and R_S as [12,13],

$$R_T = R_S + \frac{L}{We\mu_{\text{int}}\sqrt{n_0^2 + n^2}}\,, \tag{3.2}$$

where R_s is the sum of the access resistance ($2R_A$) and the contact resistance ($2R_C$). Also, W and L are the channel width and the length, respectively. By fitting the experimental R_T with this equation, we can extract the intrinsic mobility. We can thus eliminate the access and the contact resistance [14]. In this work, we use this equation to extract the intrinsic mobility.

3.3 Device fabrication

Based on the results in the previous chapter, top-gate GFETs have been fabricated using the gate dielectrics deposited with the modified solution method (Fig. 3.3). A CVD graphene was transferred onto a p-type Si substrate covered with a 90 nm-thick SiO_2 layer. Samples were then cleaned with acetone, ethanol and deionized (DI) water. After defining the source and the drain regions by image reversal process, the source and the drain electrodes (Ni/Au, 20/50 nm) were deposited on the graphene by electron-beam evaporation followed by a lift-off process. To form the top-gate dielectrics, the modified solution-processed gate dielectrics described in the previous chapter, has been conducted. Namely, a 2 nm-thick Al layer was first deposited onto graphene by electron-beam evaporation, which was naturally oxidized at a room temperature in a clean room for 12 hours. During this natural oxidation, oxygen-related ad-species on graphene are absorbed to form AlO_x. The spin-coating of the solution was carried out at a rotation speed of 4000 rpm for 20s. Subsequently, all samples were exposed to oxygen plasma for 2 min at 30 W in 4 Pa. Samples were then annealed at 200, 250 and 300 °C in air for 2 hours. To form the gate electrode, a 150-nm thick Al layer was deposited by electron beam evaporation and then the gate electrode region was pattered by a photo-lithographic process. Finally, Al and Al_2O_3 layer was etched by H_3PO_4 to form the source and the drain region openings. Figure 3.4 shows the schematic of the TG-GFET with the solution-processed Al_2O_3 film. The electrical characteristics of the TG-GFET were measured at room temperature in the air ambient using Agilent B1500 semiconductor parameter analyzer.

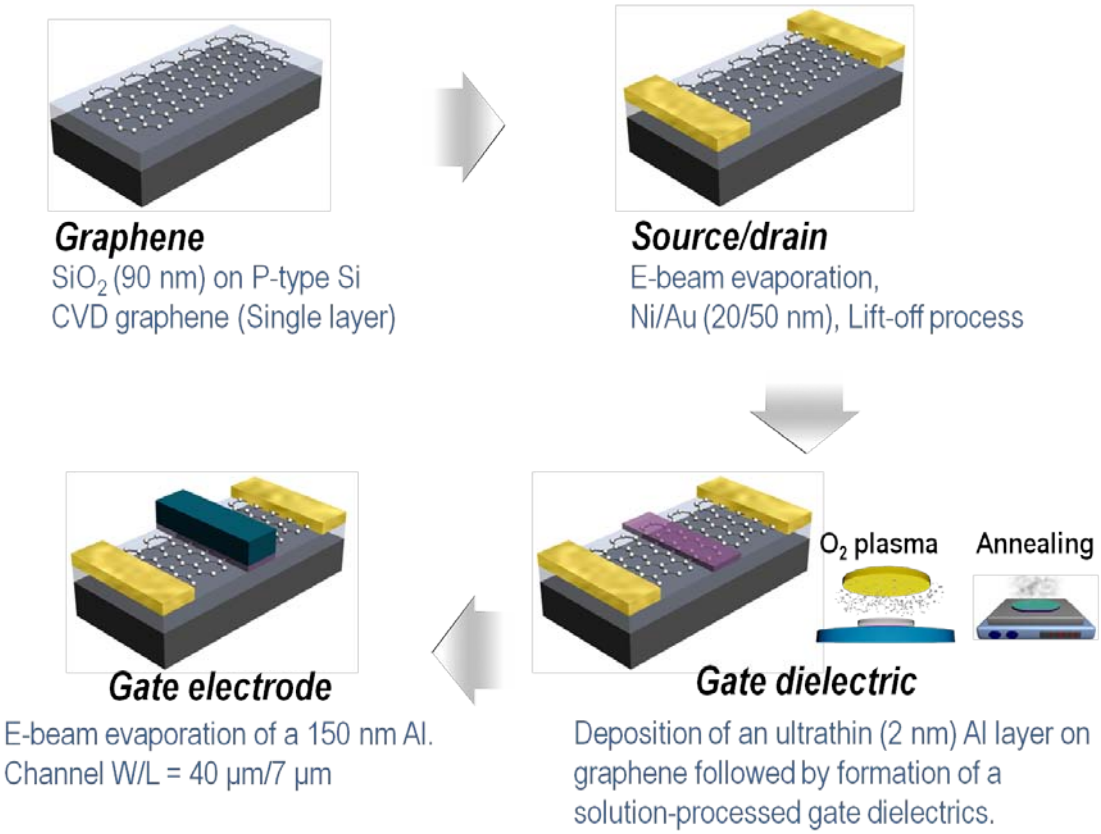


Figure 3.3. Fabrication flow of the TG-GFET with solution-processed gate dielectric.

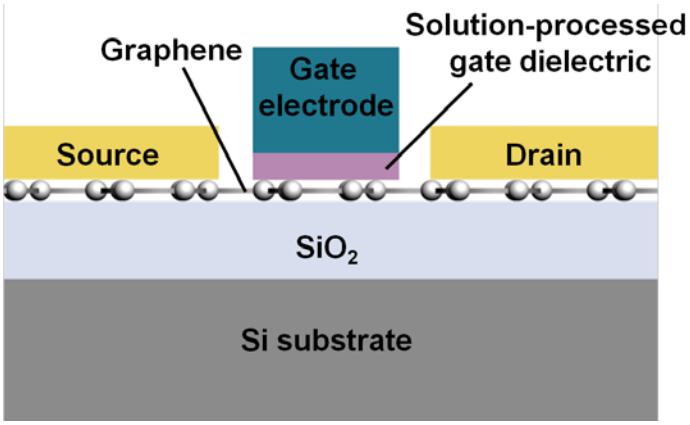


Figure 3.4. Schematic diagram of the TG-GFET with solution-processed gate dielectric.

3.4 Results and Discussion

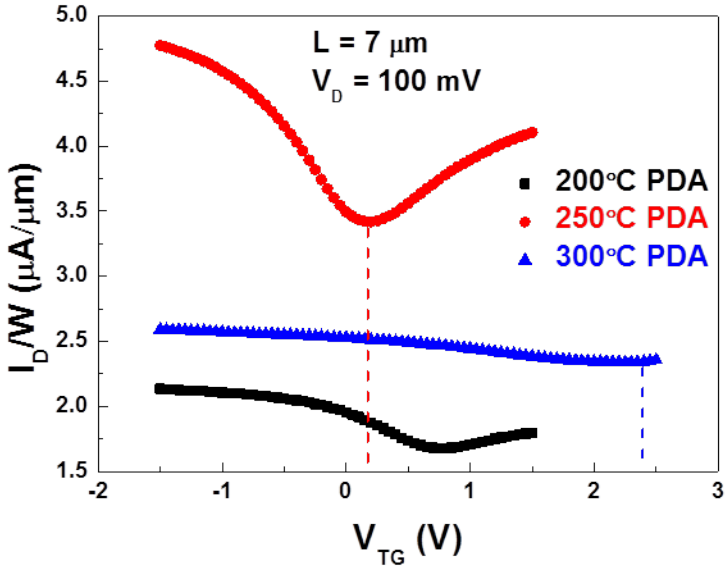
Figure 3.5 (a) shows the transfer characteristics of the drain current as a function of the gate voltage (I_D-V_G). The devices are TG-GFETs fabricated with the modified solution-processed Al_2O_3 gate dielectrics. The PDA temperature is varied for 200, 250, and 300 ℃. For the device processed with 250 ℃ PDA for 2 hours, the Dirac voltage, the top gate voltage at which the conductivity becomes minimum, is scarcely shifted: less than ~0.2 V. This indicates that the graphene underneath the gate dielectrics is almost at its charge neutral state. For the device processed with 300 ℃ PDA for 2hours, on the other hand, the Dirac voltage is remarkably shifted: more than 2 V. This suggests that the graphene underneath the gate dielectrics becomes p-type doped. These results are consistent with the results of measured Raman scattering spectroscopy in chapter 2.

Figure 3.5 (b) shows the total resistance as a function of the gate voltage (R_T-V_G). Device annealed at 250 ℃ PDA for 2 hours exhibits by far the lowest total resistance among the three devices. The reason why the device annealed at 250 ℃ PDA has such a low resistance is caused by increase of channel conductance, resulting from suppression of hole dopings and defect in graphene channel layer.

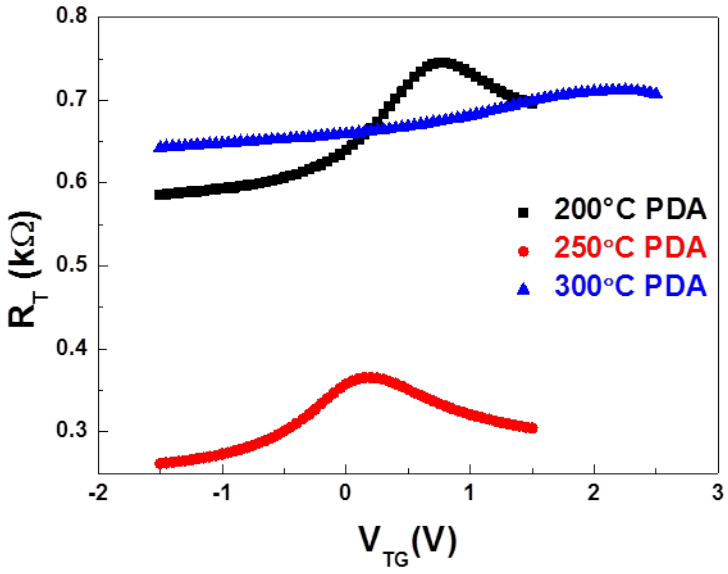
To extract the intrinsic mobility related to the channel conductance, the equation (3.2) in section 3.2 has been used. Before the extraction, accurate determination of the top gate dielectric capacitance is necessary. One method is to use a global back gate, which enables control of the carrier concentration in dual-gate FETs [13,15]. Since the Dirac voltage is linearly dependent on the ratio of the top and the back gate capacitance (C_{TG}/C_{BG}), we can extract the top gate capacitance on graphene using the Dirac voltage and C_{BG}. No information on the thickness and the dielectric constant is necessary. Figure 3.6 shows the Dirac voltage as a function of the back gate voltage of TG-GFETs with the solution-processed top gate dielectrics. All the devices have a 100 nm-thick SiO_2 layer on the Si substrate as the back-gate oxide and its C_{BG} value is estimated to be 0.0345 μF/cm^2. In the device formed at 200 ℃, C_{TG} is calculated to be 0.678 μF/cm^2 using the relation shown in Fig 3.6(a). By

using the same method, C_{TG} of the device formed at 250 and 300 ℃ are estimated to be 0.885 (Fig 3.6(b)) and 0.811 μF/cm^2 (Fig 3.6(c)), respectively. In accordance with the result shown in the previous chapter, the device annealed at 250 ℃ gives the highest top gate capacitance among the three PDA temperatures.

Figures 3.7(a)-(c) show the total resistance (R_T) as a function of the gate voltage (V_G) for devices with PDA at (a) 200, (b) 250, and (c) 300 ℃. The open squares are the measured data and solid red lines are the fitted curve using equation (3.2). The fitting is in good agreement with the experiment. The extracted intrinsic mobility μ_{int} was highest in the device with PDA at 250 ℃, which amounts as high as ~8430 cm^2/Vs. The residual carrier concentration (n_0) was 2×10^{11} cm^{-2}. For the GFETs with PDA at 200 and 300 ℃, μ_{int} of ~5000 and ~2470 cm^2/Vs and n_0 of 3.5×10^{11} cm^{-2} and 1×10^{12} cm^{-2} were obtained, respectively. Table 3.1 summarizes the intrinsic carrier mobility for electrons and holes as well as the residual carrier concentration for the three PDA temperatures. As can be seen, the intrinsic carrier mobility is increasing with decreasing residual carrier concentration. This result indicates that the intrinsic carrier mobility in the graphene channel is inversely correlated with the residual carrier concentration, which is proportional to the impurity concentration [10]. Combining the Raman spectroscopy data in chapter 1 and the intrinsic carrier mobility in this chapter, we conclude that the highest intrinsic carrier mobility obtained in the device with the PDA at 250 ℃ can be attributed to enhancement of channel conductance, resulting from minimum hole dopings and defects in graphene channel layer.

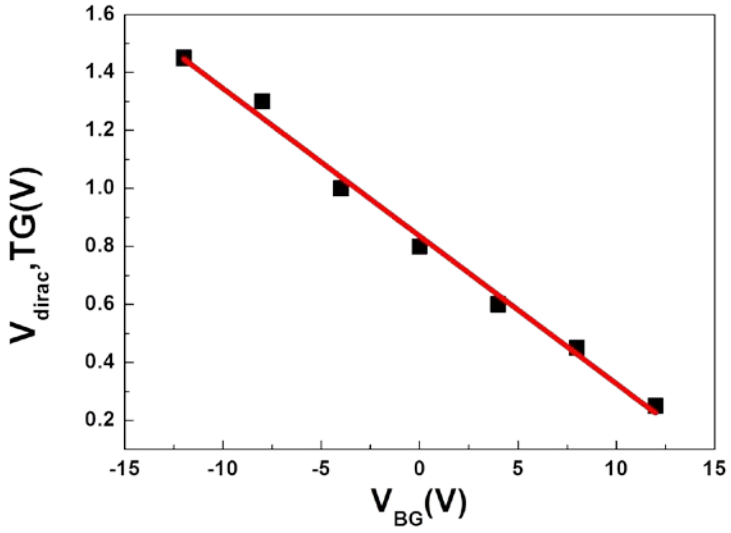


(a)



(b)

Figure 3.5. (a) Transfer characteristics of the drain current as a function of the gate voltage (I_D-V_G) with various PDA temperatures. (b) Total resistance as a function of the gate voltage (R_T-V_G) with various PDA temperatures.


1.6
1.4
1.2
1.0
0.8
0.6
0.4
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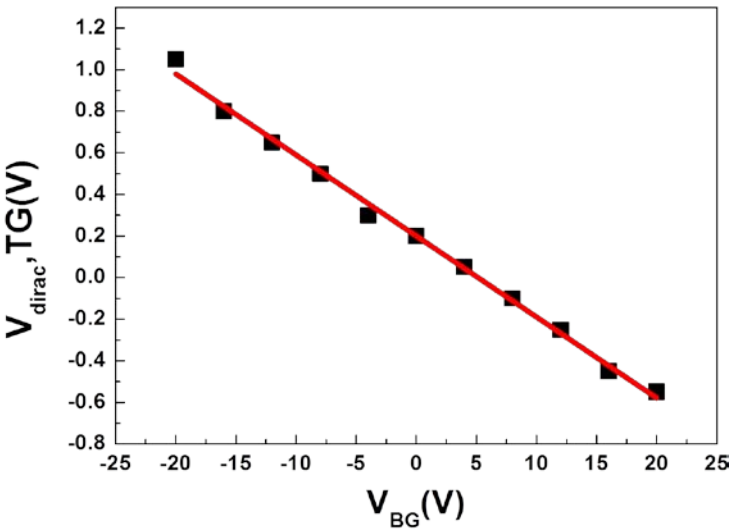
-15
-10
-5
0
5
10
15
V_dirac,TG(V)
V_BG(V)

(a)


1.2
1.0
0.8
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-0.4
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-0.8
-25
-20
-15
-10
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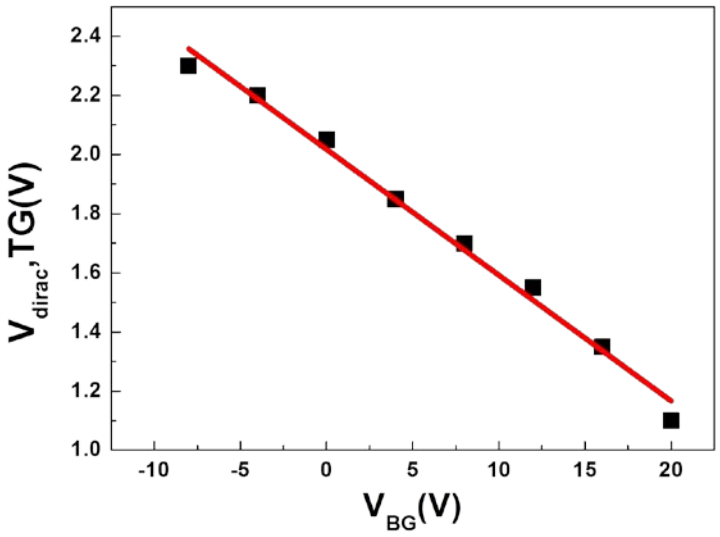
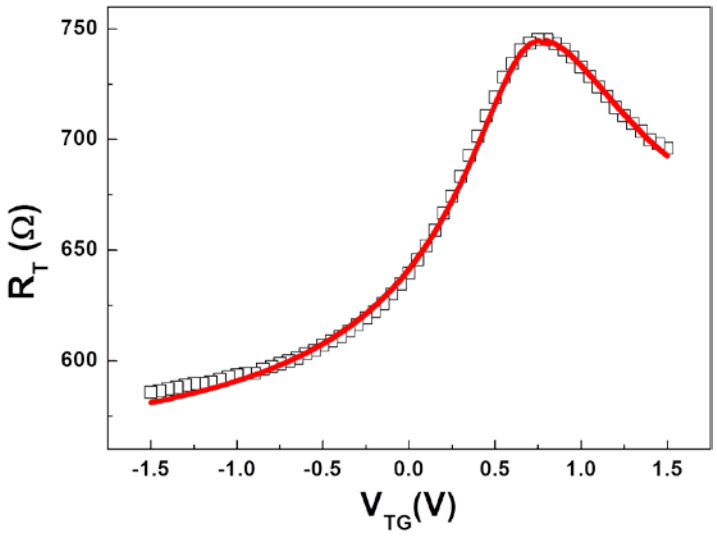
0
5
10
15
20
25
V_dirac,TG(V)
V_BG(V)

(b)

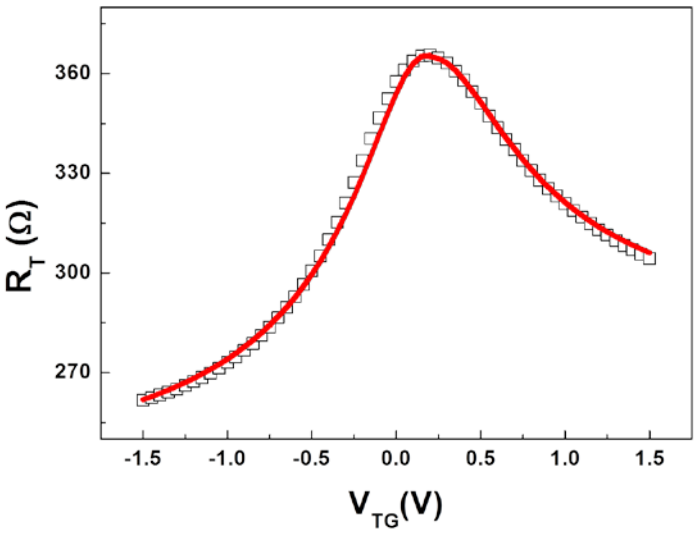


(c)

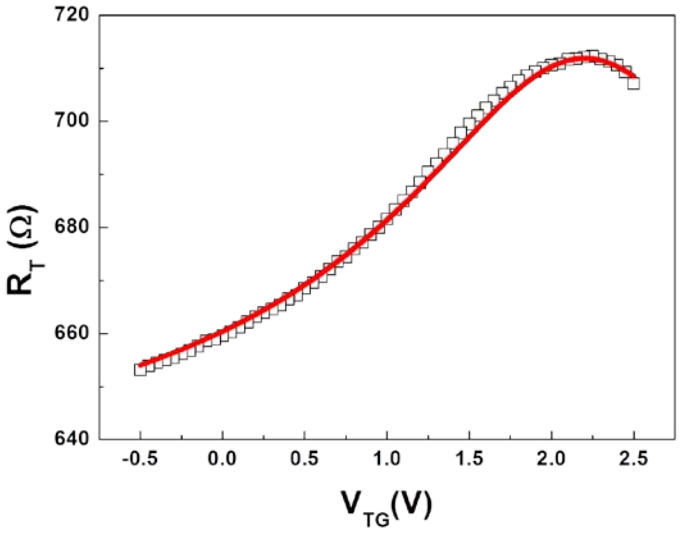
Figure 3.6. Dirac voltage as a function of the V_{BG} of TG-GFETs with solution-processed gate dielectric annealed (a) at 200 ℃ (c) at 250 ℃ (e) at 300 ℃



(a)



(b)



(c)

Figure 3.7. Measured R_T versus V_G (black square) of TG-GFETs with solution-processed gate dielectric annealed (a) at 200 ℃ (b) at 250 ℃ (c) at 300 ℃ and fitted result (red line) with equation, respectively.

Table 3.1. Comparison of the intrinsic carrier mobilities and residual carrier concentration at various PDA temperatures.

PDA (°C)	μ_{int} electron (cm^2/Vs)	μ_{int} hole (cm^2/Vs)	n_0 (cm^{-2})
200	4850	4980	3.5×10^{11}
250	8430	8400	2×10^{11}
300	-	2470	1×10^{12}

While the intrinsic carrier mobility reflects only the conductance in the channel region, the field effect mobility μ_{FE}, obtained from the transconductance, is greatly influenced by the series resistance as well (Fig 3.7). Figure 3.8 shows the field effect mobility of the TG-GFET with PDA at 250°C. The field effect mobility $\mu_{FE} = g_m \frac{L}{W} \cdot \frac{1}{C_{ox} \cdot V_d}$ for electrons and holes were 120 and 63 cm^2/Vs, respectively. In sharp contrast with the intrinsic mobility, these values are quite low, even lower than that of silicon transistors (490 and 95 cm^2/Vs for electrons and holes) [16]. Since the drastic difference between μ_{int} and μ_{FE} is attributed mostly to the series resistance, reduction of both the access and the contact resistance is clearly important key to realization of high performance GFETs.

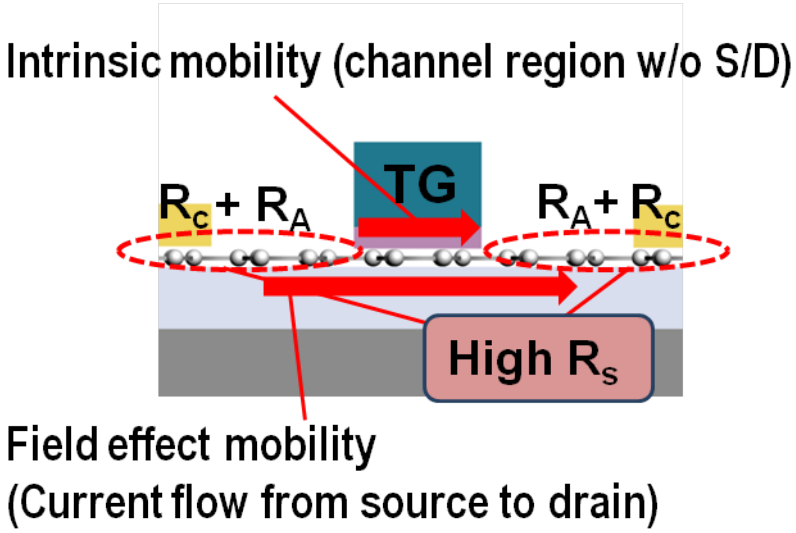


Figure 3.8. Comparison between intrinsic mobility and field effect mobility.

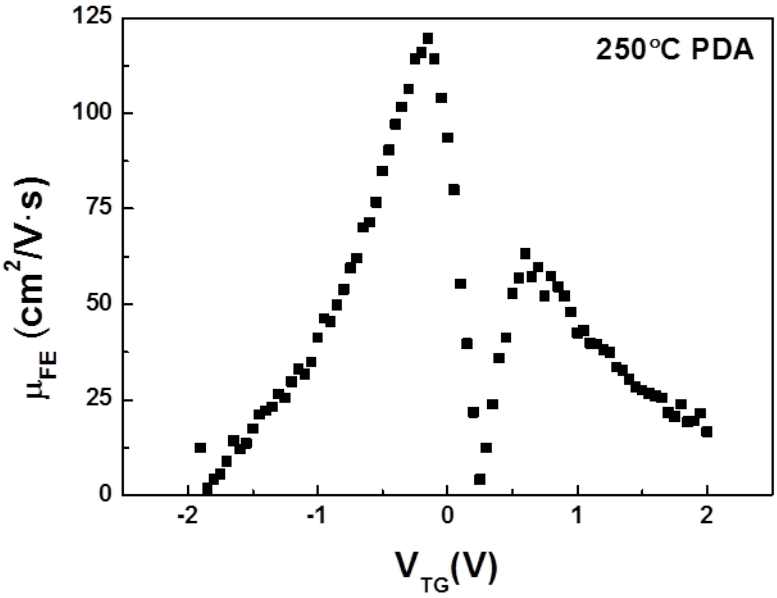


Figure 3.9. Field effect mobilities of TG-GFETs with solution-processed gate dielectric formed at 250°C.

3.5 Conclusion

TG-FETs with gate dielectrics deposited by the modified solution method have been fabricated. The gate process consists of initial formation of a natural oxide layer of Al, spin-coating of the sol-gel precursor for Al_2O_3, the oxygen plasma treatment, and PDA. PDA at 250 ºC was found ideal in achieving the high intrinsic carrier mobility (~8400 cm^2/Vs) in the temperature range (200-300 ºC) tested. With this high potential, the modified solution-processed gate dielectrics are quite promising for realizing high performance GFETs.

Reference

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4

UV-Ozone-processed contacts for GFETs

4.1 Introduction

In the previous chapter, a novel gate dielectric formation method called modified solution method, developed in chapter 2, has been applied to fabricate TG-GFETs. As a result, a quite high intrinsic mobility of ~8400 cm^2/Vs was obtained. However, the field effect mobility was significantly deteriorated from the high intrinsic carrier mobility. This is due to a low transconductance characteristic caused by a high series resistance including the access and the contact resistances [1,2].

Minimizing the contact resistance between metal and graphene is crucial in increasing the transconductance (g_m), on current (I_{on}), and the cut-off frequency (f_T) [2-5]. The present contact resistance in GFETs is quite high as compared to other competing devices such as InAs/AlSb HEMT (~100 Ω μm) [6] and InP HEMT (~50 Ω μm) [7]. One reason is the small density of states (DOS) of graphene around the Dirac point. The low DOS value suppresses the carrier injection from the metal to graphene, causing increase of the contact resistance. In the past few years, considerable endeavors have been made on reducing the contact resistance in GFETs. Previous studies reported that Ni or Pd electrodes show relatively low contact resistance while high contact resistance appears with Ti, Cr, Al electrodes [3,5,8,9]. It has also been reported that use of end contacts [10], edge contacts [11], and short contact length [2] show remarkably low contact resistances due to decrease of current crowding effect, leading to a non-uniform current density that is higher at edge of the metal contact [12]. They are all due to decrease of the charge transfer length. Another critical issue in minimizing the contact

resistance is the contamination at the metal/graphene interface during device fabrication. One major cause for this contamination is the residual photoresist after the photolithographic process. Several methods have been reported to remove the contamination. Plasma treatment is one of such recipes, and has actually shown reduction of contact resistance. Plasma treatment, however, is sometimes too aggressive, and graphene may be significantly degraded [13,14]. Thermal annealing is also reported to be very effective. This method however cannot be conducted after opening the contact window, i.e., image reversal, before deposition of the metal because thermal budge is not acceptable after a photolithographic processing [15]. We should therefore need to find a simpler and more reproducible way to reduce the contact resistance.

In this chapter, the ultraviolet ozone (UVO_3) treatment is examined to remove the photoresist (PR) residue on graphene to obtain low contact resistance. UVO_3 treatment is widely used in semiconductor device processings and in industries requiring clean interfaces. It is a convenient method for cleaning the surface of metals and semiconductors due to its not so aggressive reaction processes operated at room temperatures [16]. By using the UVO_3 method, we can expect removal of the interface contamination after the photolithographic process without causing much defects in graphene and degradation of electrical characteristics.

4.2 Device Fabrication

The fabrication sequence of a back-gated (BG) GFET with UVO_3 treated contacts is illustrated in Figure 4.1. A CVD graphene was transferred onto a p-type Si substrate covered with a 90 nm-thick SiO_2 layer. To define the active region, the graphene sheet was etched by an oxygen plasma treatment after an active pattering. The source/drain contact pattern was fabricated by using a conventional photoresist (AZ5214E). After opening a contact window in the photoresist, samples were treated with a commercial UVO_3 system at room temperatures for varied durations to remove the PR residue. Before deposition of the contact metal, the surface roughness and the defects in graphene were evaluated by using Atomic Force Microscopy (AFM) and Raman scattering spectroscopy, respectively. Ni/Au (20/50 nm) metal layers were deposited by an e-beam evaporator and patterned by a lift-off process. Finally, the samples were annealed in a vacuum system at 300 °C for 1 hour under a H_2/N_2 mixture ambient. Contact resistance was evaluated by combining the 2- and the 4-point probe methods for BG-GFETs (Fig. 4.7) [3,9]. The electrical characteristics were obtained by using a semiconductor parameter analyzer (B1500, Agilent Technology) at room temperature in air.

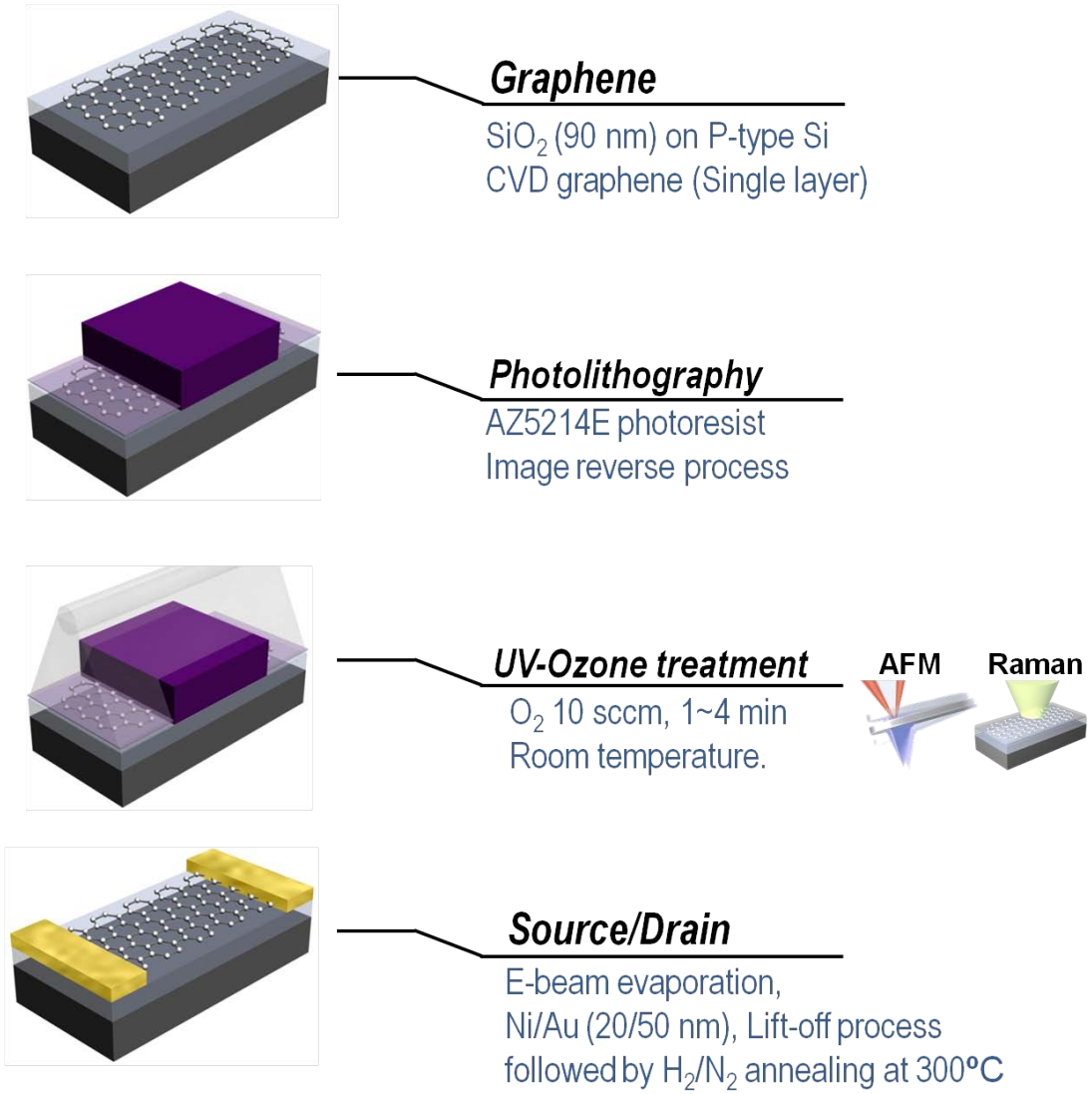
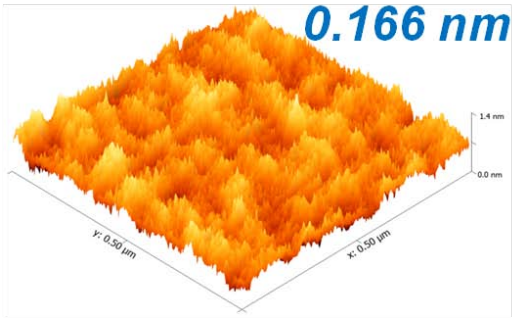


Figure 4.1. Fabrication sequences of BG-GFETs with UVO_3 treated contact.

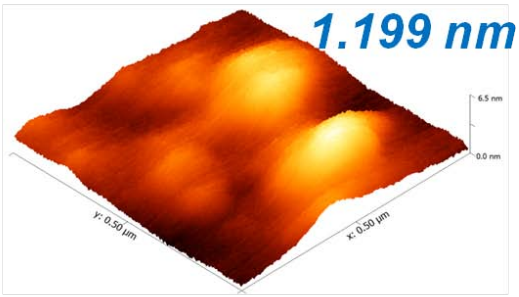
4.3 Results and Discussion

4.3.1 Surface morphology and defects to graphene

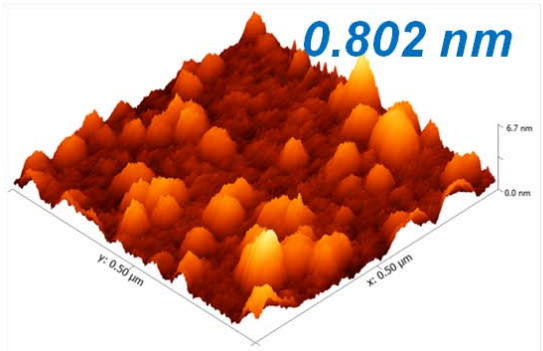
First, we demonstrate the aggressiveness and effectiveness of the UVO_3 treatment by AFM and Raman scattering spectroscopy. Figure 4.2 shows the surface morphology of the graphene before and after the UVO_3 treatment measured by AFM. Figure 4.2 (a) is for a pristine graphene and the surface roughness is determined to be 0.166 nm. After the photolithographic process, on the other hand, the RMS surface roughness is significantly increased to 1.199 nm (Fig 4.2 (b)). This indicates that part of the PR remains on the graphene surface after the photolithographic process. Figures 4.2 (c)-(f) sequentially shows evolution of the surface morphology for 1, 2, 3, and 4 min of UVO_3 treatment. The surface roughness decreases with the treatment, and is minimized at 3 min. No further changes occur after 3 min of the UVO_3 treatment. This indicates that the PR residue on graphene is effectively removed by the UVO_3 treatment. As for the degradation of graphene caused by the UVO_3 treatment, Raman scattering spectroscopy is very effective and convenient. Figure 4.3 shows the Raman spectrum of the graphene before and after the UVO_3 treatment. The D peak intensity, related to the defect density in graphene, starts to increase after 3 min of the UVO_3 treatment. This indicates that the PR residue on graphene is completely removed by 3 min of the UVO_3 treatment, and further treatment starts to degrade graphene. Figure 4.4 shows the RMS roughness and the I_D/I_G ratio as a function of the treatment time. After 3 min of the UVO_3 treatment, the RMS surface roughness is almost identical with the initial value of pristine graphene and the I_D/I_G ratios is about to increase. This indicates that 3 min is ideal for the UVO_3 treatment both to remove the PR residue and to suppress the defect formation. We therefore expect to achieve reproducible and reliable metal/graphene contacts by applying a 3-min UVO_3 treatment to graphene.



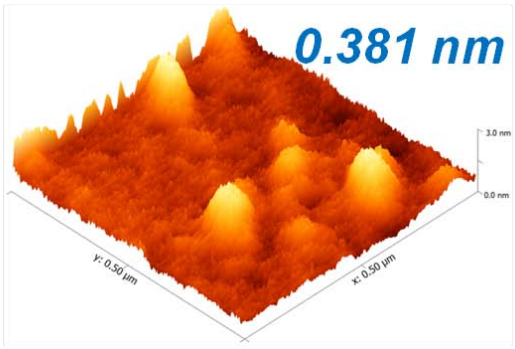
(a)



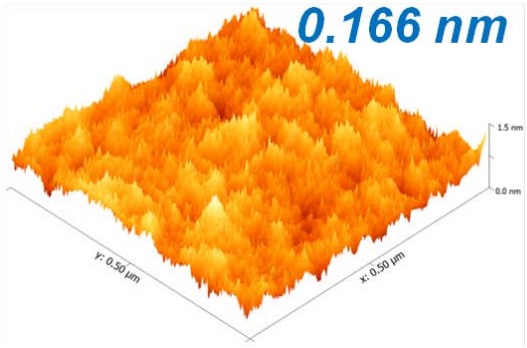
(b)



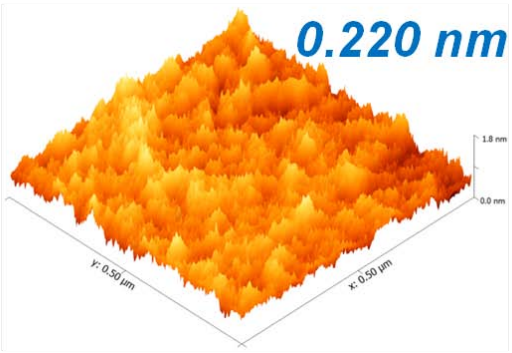
(c)



(d)



(e)



(f)

Figure 4.2. Surface morphology on graphene, measured by AFM, (a) in pristine graphene (b) after photolithography (c) UVO_3 for 1 min (d) UVO_3 for 2 min (e) UVO_3 for 3 min (f) UVO_3 for 4 min

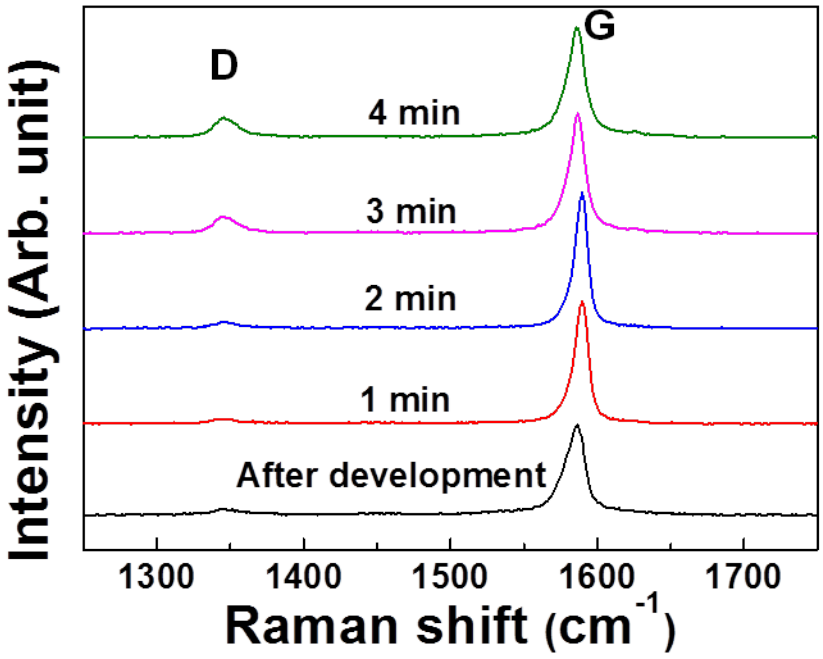


Figure 4.3. Raman spectrum of D and G peak before and after UVO_3 treatment.

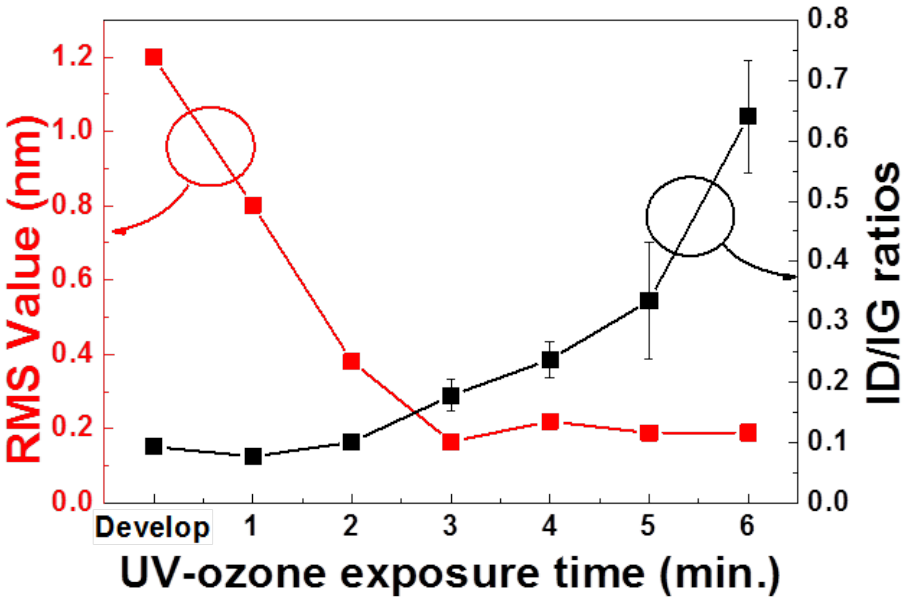
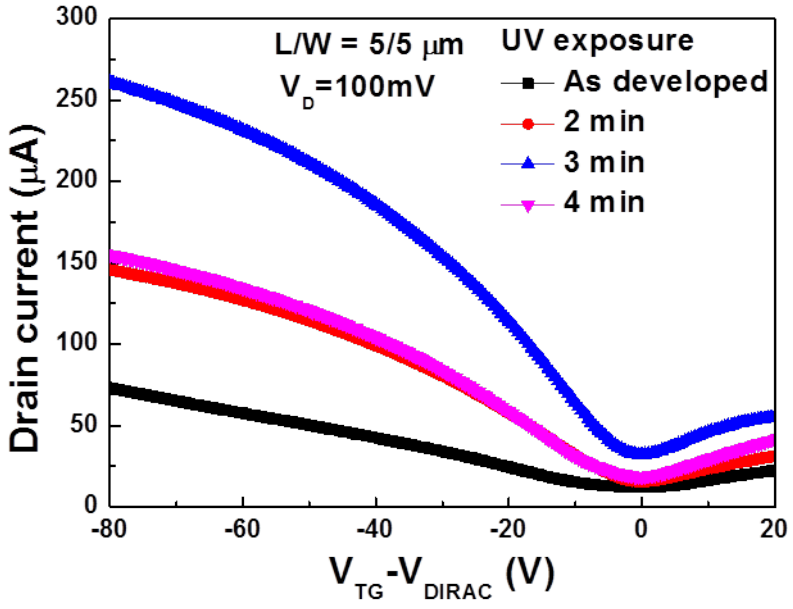


Figure 4.4. RMS value and I_D/I_G ratios, determined by AFM and Raman scattering spectroscopy, respectively, as a function of UVO_3 treated time.

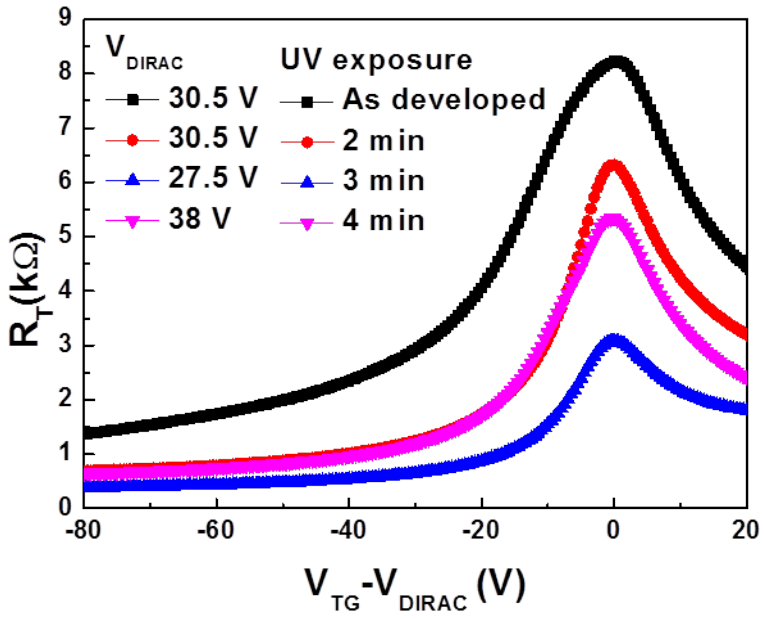
4.3.2 Electrical characteristics

Figure 4.5 (a) shows the drain current as a function of V_{TG}-V_{Dirac} (I_D-V_G) for BG-GFETs. In fabricating the contacts, the UVO_3 treatment has been applied. The drain current of the BG-GFET fabricated with 3 min of UVO_3 treatment is about three times larger than that of the *as-deposited* BG-GFET without the treatment. After 4 min of the UVO_3 treatment, however, the drain current is significantly decreased back to the same level as of the 2-min treatment. This is related to onset of defect formation by the UVO_3 treatment. Figure 4.5 (b) shows the total resistance as a function of V_{TG}-V_{Dirac} (R_T-V_G) for these BG-GFETs. This series of R_T-V_G characteristics show similar trends to that of I_D-V_G characteristics (Fig. 4.5 (a)). The lowest total resistance was observed for the device with the UVO_3 treatment of 3 min. As indicated in Fig. 4.5 (b), the Dirac point, the voltage giving the highest total resistance, is largely shifted to positive values above 27.5 V. This can be related to some charges and polar molecules adsorbing on the graphene channel layer [16]. With these positive Dirac voltages, the contact resistances in these devices are for holes. In TG-GFETs, on the other hand, the Dirac point will be located in the vicinity of 0 V as we will see in the next chapter.

Figures 4.6 (a) and (b) show the transconductance and the field-effect mobility as a function of V_{TG}-V_{Dirac}., respectively. The highest transconductance and the field-effect carrier mobility were obtained for a device treated by the UVO_3 treatment of 3 min. This result indicates that the improvement of the transconductance and the field-effect carrier mobility due to the UVO_3 treatment is attributed to its low contact resistance. From these results, we confirm that the UVO_3 treatment for 3 min after the photolithographic process is very effective to improve the electrical characteristics.

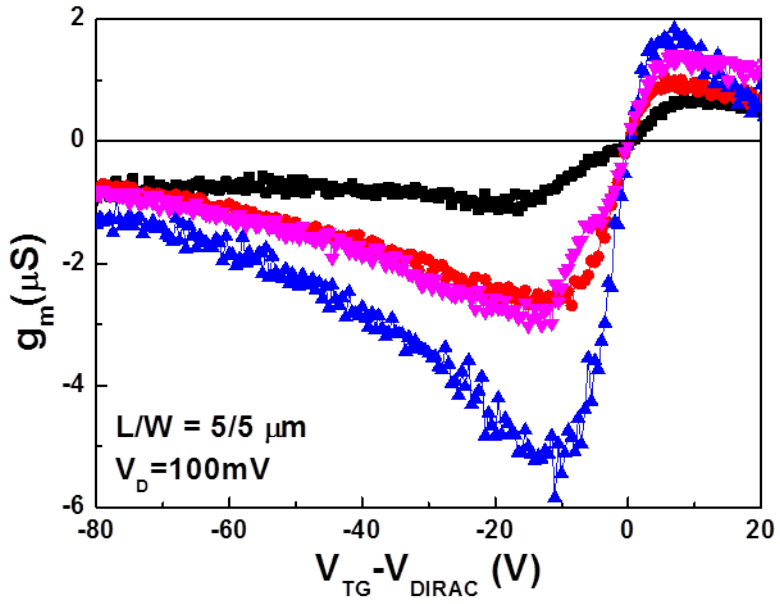


(a)

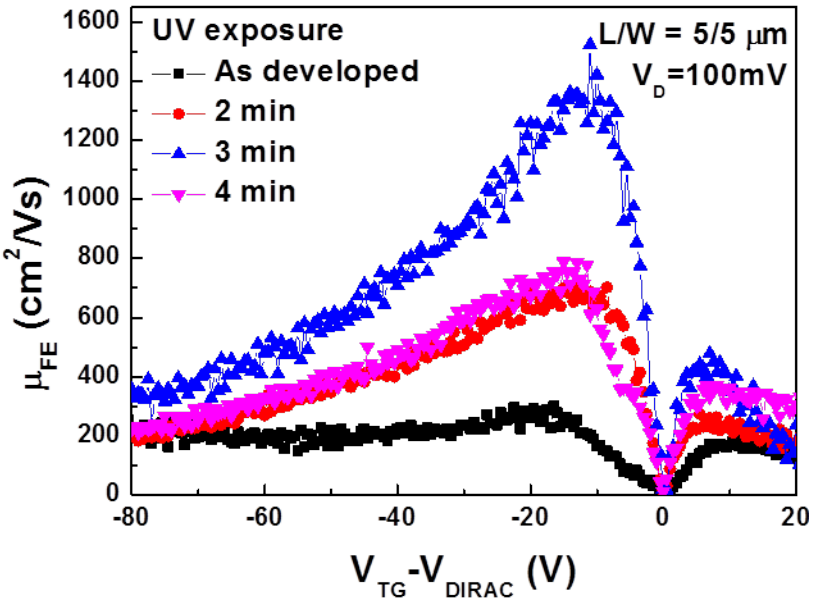


(b)

Figure 4.5. (a) Drain current as a function of V_{TG}-V_{Dirac} (I_D-V_G) (b) total resistance as a function of V_{TG}-V_{Dirac} (R_T-V_G); for BG-GFETs with UVO_3 treated contact.



(a)



(b)

Figure 4.6. (a) Transconductance and (b) field effect mobility; as a function of V_{TG}-V_{Dirac} for BG-GFETs with UVO_3 treated contact.

4.3.3 Extraction of the contact resistance

To be more quantitative, the contact resistance was extracted by combining the two- and four-point probe measurements. As can be seen in figure 4.7, the two-point probe measurement involves the sheet resistance in the channel layer and the contact resistance of interest. On the other hand, the four-point probe measurement only includes the sheet resistance in the channel layer because the inner pair of probes with high impedance is used for current sensing while the outer pair of probes are used as a current source. By combining the two measurements, therefore, we can extract the contact resistance. The normalized contact resistance is thus given by the following equation [3,9].

$$R_C W = \frac{1}{2}(R_{2p} - R_{4p})W \ , \tag{4.1}$$

where R_{2p} and R_{4p} is the resistance obtained from the two-point probe and the four-point probe measurements, respectively, and W is the width of the metal contact. R_cW is the normalized contact resistance.

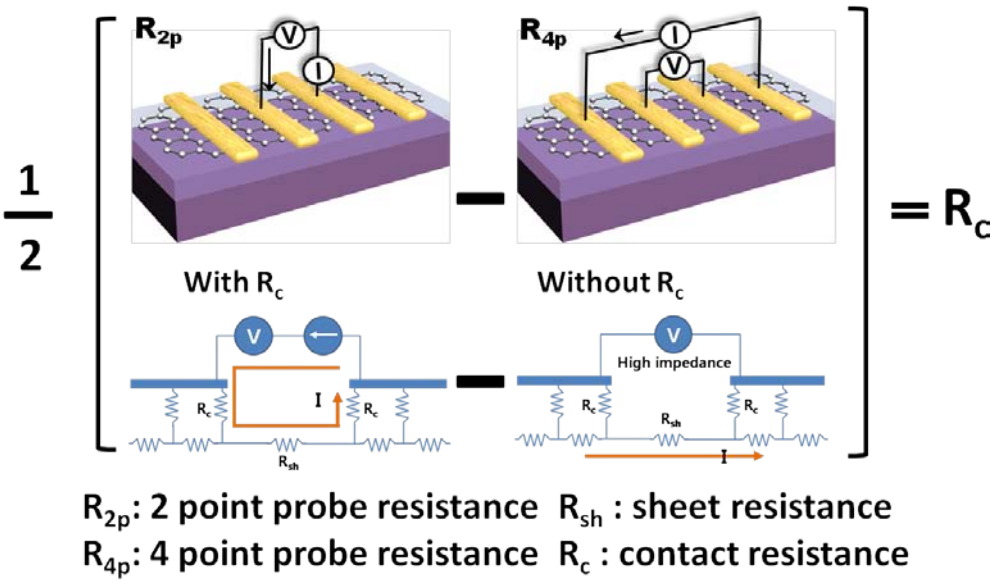
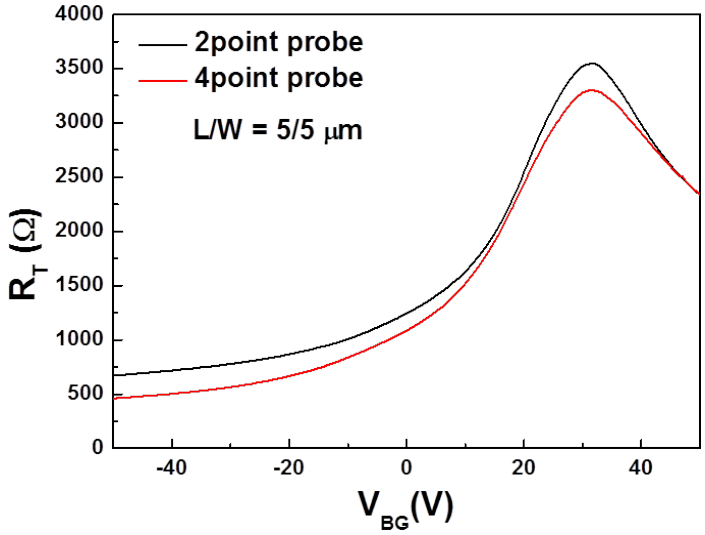
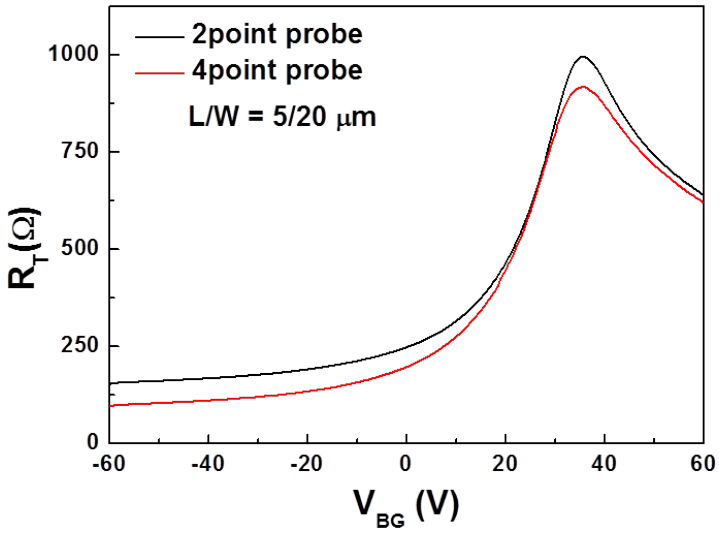


Figure 4.7. Schematic diagram how to extract the contact resistance.

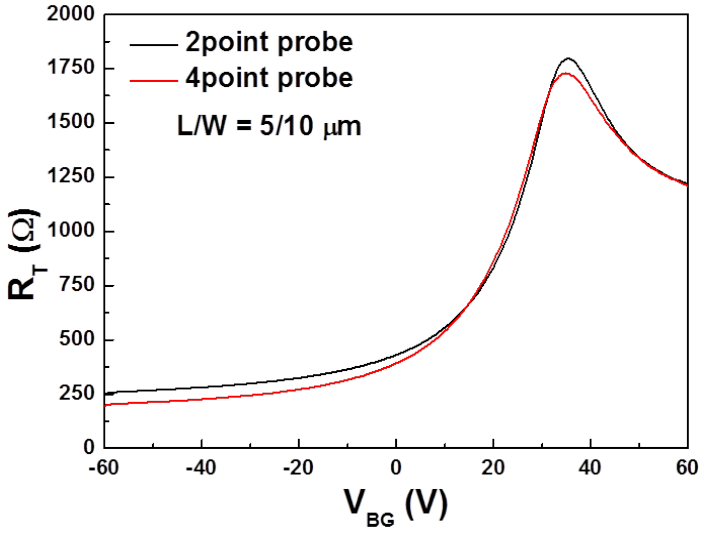
Figure 4.8 shows the total resistance as a function of the back gate voltage for various UVO_3 treatment time. In all the devices, the four-point probe method gives a lower total resistance than that of two-point probe method. The difference is due to the contact resistance component contained in the two-point probe resistance. The contact resistance was obtained using the saturated portion for V_{BG} values below -40 V. In Fig. 4.9, we plot the normalized contact resistance as a function of the UVO_3 treatment time. The normalized contact resistance decreases with increase of the UVO_3 treatment time until 3 min. At 4 min of the UVO_3 treatment, however, the contact resistance increases again. As described in section 4.3.1, the UVO_3 treatment until 3 min contributes to removal of the PR residue while the treatment after 3 min contributes to increase of defects in graphene. This observation is consistent with the behavior of the contact resistance obtained in this section. By using the UVO_3 treatment of 3 min, we obtain the lowest contact resistance ranging from 100 to 400 Ωμm, which is comparable or less than those reported in literatures on the same material systems [3,18]. It is thus demonstrated that the UVO_3 treatment is reproducible and effective in removing the PR residue after the photolithographic process, resulting in reducing the contact resistance between graphene and the metal electrodes.


2point probe
4point probe
L/W = 5/5 μm
R_T (Ω)
V_{BG}(V)
4000
3500
3000
2500
2000
1500
1000
500
0
-40
-20
0
20
40

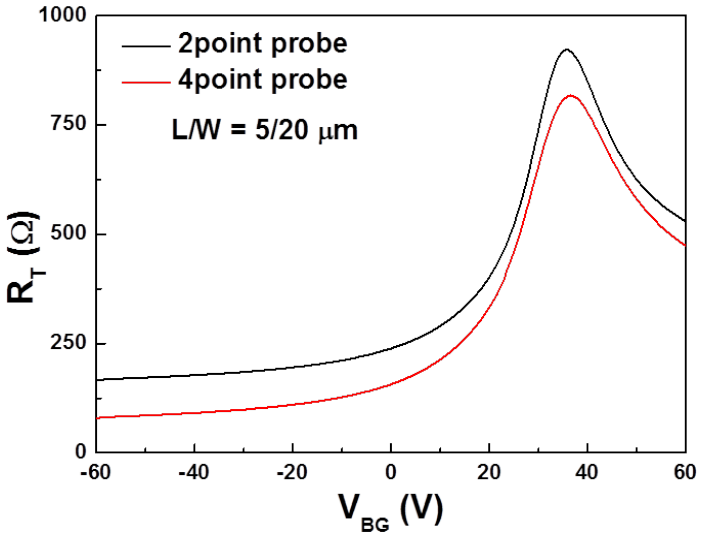
(a)


2point probe
4point probe
L/W = 5/20 μm
R_T(Ω)
V_{BG} (V)
1000
750
500
250
0
-60
-40
-20
0
20
40
60

(b)



(c)



(d)

Figure. 4.8. Total resistance as a function of back gate voltage using two and four point probe method for BG-GFETs with (a) as-developed (b) UVO_3 for 2 min (c) UVO_3 for 3 min (d) UVO_3 for 4 min.

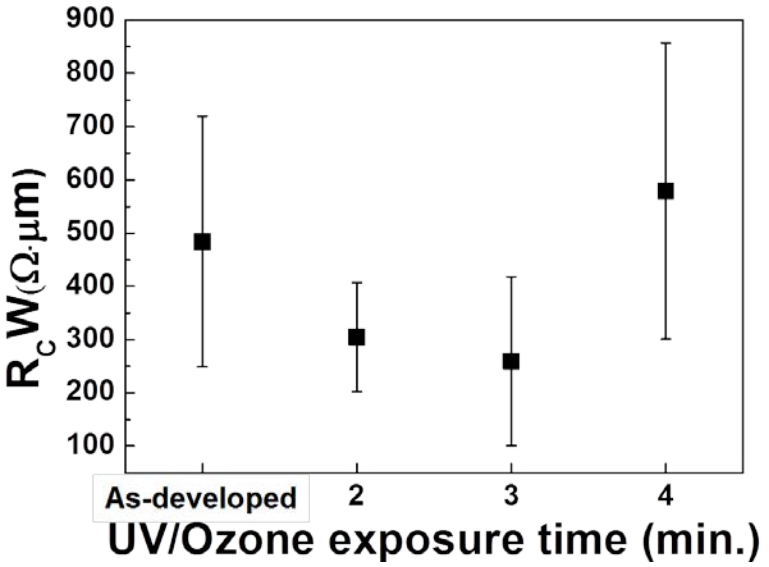


Figure 4.9. Normalized contact resistance as a function of UVO_3 treatment time in BG-GFETs.

4.4 Conclusion

In conclusion, we have demonstrated that the UVO_3 treatment is quite effective for reducing the contact resistance through removal of interfacial contaminations. We confirmed that the UVO_3 treatment after the photolithographic process is quite effective in removing the PR residue without inducing substantial damages to graphene. As a result, the transconductance and the filed-effect mobility characteristics are remarkably improved by the UVO_3 treatment of 3 min. Finally, a low contact resistance ranging from 100 to 400 Ωμm was obtained, which is comparable or less than the reported values made on the same material system. These results provide important insights for betterment of the GFET performance.

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5

Electrical properties of GFETs with a overlapped source/drain to top-gate and UV-ozone-processed contacts

5.1 Introduction

In the previous chapter, we discussed realization of low contact resistance using UVO_3 treatment and confirmed its effects in the performance of back-gated (BG) GFETs. Although many of the previous GFETs employed the BG device structure [1-3], the largest limitation of the BG-FET is the fact that only a single device on a chip can be operated at a given moment because the substrate as the gate electrode is common to all the devices within the chip. Furthermore, because the gate dielectric is thick (90 nm or more), high operation voltages are required. The back gate biasing is clearly difficult. Use of substrates other than Si, such as SiC, quartz, and flexible polymer substrates are also difficult without additional processes. For practical applications, therefore, use of top-gated (TG) device structure is a prerequisite. The TG-FET has several advantages in integrated circuit (IC) applications, such as the local gate biasing, low operating voltages, high integration density, wide selection of substrates, and dual-gate operations [4].

In chapter 3, we discussed the fabrication and evaluation of TG-GFETs with a solution-processed gate dielectric. The field effect mobility was however very low in sharp contrast with the high intrinsic mobility due to the high series resistance including the access and the contact resistances.

In chapter 4, we therefore achieved realization of low contact resistance using UVO_3 treatment. For better performance of GFETs, therefore, we need to achieve reduction of the access resistance. Most of the TG-GFETs have been accompanied with ungated regions between the gate and the source and drain (S/D) electrodes as shown in figure 5.1. This ungated region acts as the access resistance and has a strong negative influence on the device performance; the access resistance results in lowering of the current drivability, i.e., the transconductance [5,6]. Also, the ungated region is prone to form defects in the graphene by adsorbing molecules from the ambient [7,8] for instance.

In this chapter, we discuss fabrication of TG-GFETs with a overlapped S/D to gate structure and UVO_3-treated contacts. Employment of the former is to minimize the access resistance and the latter to reduce the contact resistance (Fig 5.2). It will be shown that the electrical characteristics such as transconductance, field effect mobility, and on-current are greatly improved.

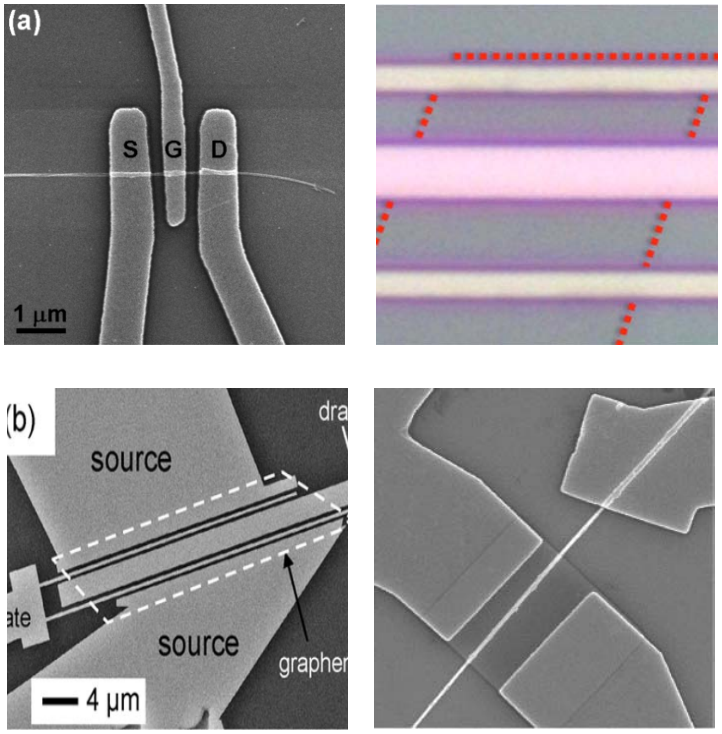


Figure 5.1. Graphene FETs with ungated region.

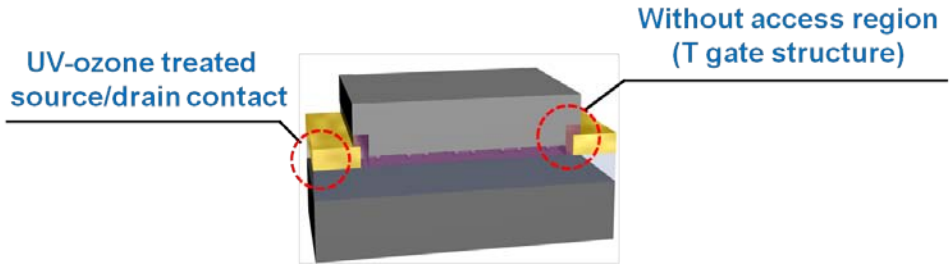


Figure 5.2. Schematic diagram of proposed TG-GFETs

5.2 Device Fabrication

The TG-GFETs with a overlapped S/D to gate and UVO_3-treated contacts were fabricated on a p-type Si wafer covered with a 90 nm-thick thermal SiO_2 layer. First, CVD graphene was transferred onto the Si substrate, and the substrates were cleaned with acetone, ethanol and deionized (DI) water. After defining the source and drain region by an image reversal process, UVO_3 treatment was carried out for 2, 3 and 4 min. The source and the drain electrodes (Ni/Au, 20/50 nm) were then fabricated on the graphene by use of electron-beam evaporation followed by a lift-off process. The samples were annealed in a vacuum system at 300 °C for 1 hour under the H_2/N_2 mixture ambient to remove the PR residue on the graphene channel. In order to form the top-gate dielectric layer, a 2 nm-thick Al was first deposited by electron-beam evaporator, which was then naturally oxidized at room temperature for 24 hours. A 150 nm-thick Al layer was then e-beam evaporated as the gate electrode, which was defined by a photolithographic process. Finally, the Al and Al_2O_3 layers were etched by H_3PO_4 to form the source and drain region openings. The channel dimensions are 40 μm in width and 3 μm in length. The electrical characteristics were obtained at room temperature in air by using a semiconductor parameter analyzer (B1500, Agilent Technology).

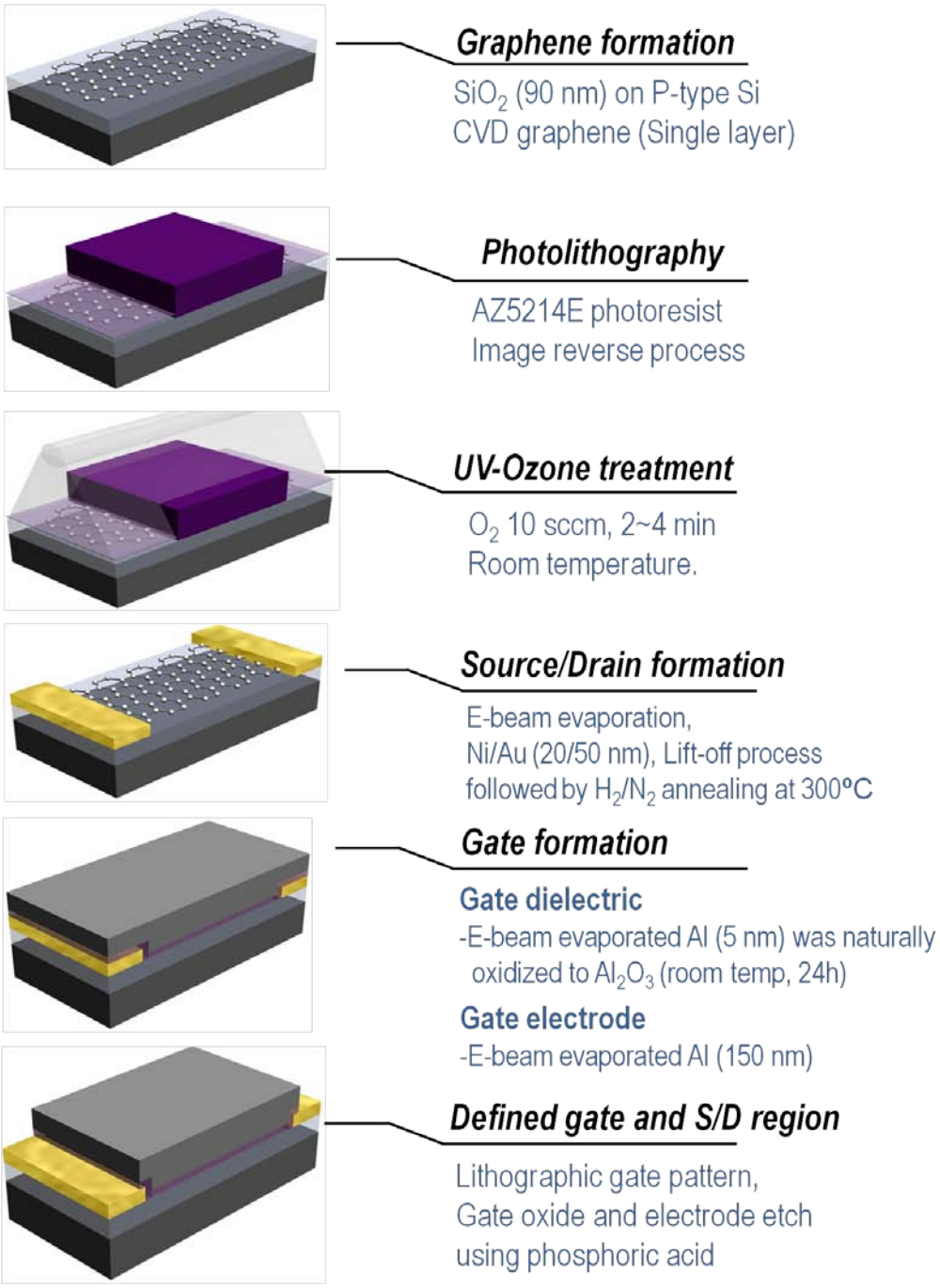
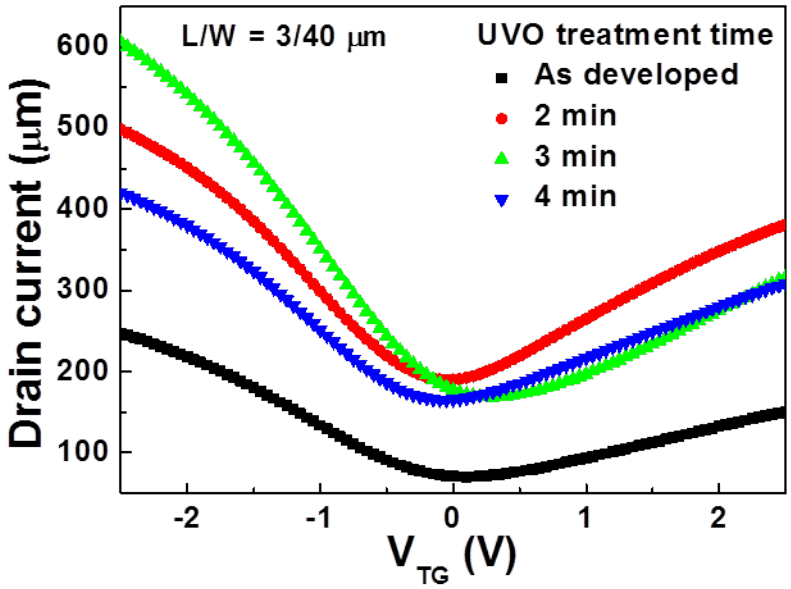


Figure 5.3. Fabrication sequence of TG-GFETs with overlapped S/D to gate and UVO_3 treated contacts.

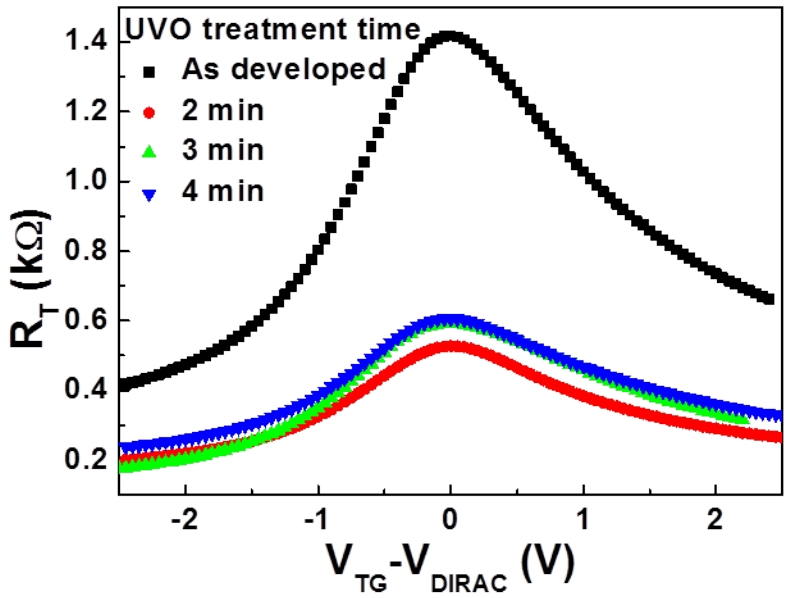
5.3 Results and Discussion

Figure 5.4 (a) shows the transfer characteristics of the drain current as a function of the top gate voltage (I_D-V_{TG}) of the GFETs. The Dirac voltage, the top gate voltage at which the conductivity becomes minimum, was quite close to zero voltage ranging between -0.05 and 0.3 V for all the devices. This indicates that the graphene underneath the top-gate dielectrics is almost at its charge neutral state. Clearly, the drain current is much higher in the UVO_3-treated devices than in untreated (*as-developed*) devices. This result indicates that the UVO_3 treatment is effective in improving the electrical characteristics of GFETs not only for BG-FETs but also for TG-GFETs. In particular, the devices UVO_3-treated for 2 and 3 min show the highest drain currents in the n and the p branch, respectively. Asymmetric electron-hole conduction was observed in all devices: much higher hole current flow than electron current. This point will be discussed later. Figure 5.4 (b) shows the total resistance as a function of the gate voltage (R_T-V_G). As seen in the I_D-V_{TG} characteristics, the total resistance is drastically lowered by use of the UVO_3-treated contacts. Based on this total resistance characteristics, we can extract the contact resistance by fitting with the equation (3.2).

Figure 5.5 (a) and (b) shows the transconductance and the filed-effect mobility of the GFETs. As described in the previous chapter, the highest hole transconductance and the field effect mobility were obtained in the device UVO_3-treated for 3min. All data considered, UVO_3 treatment for 3 min is found most effective in increasing the on-current and improving the electrical characteristics for the TG-GFETs. We also find that the hole transconductances and field-effect mobilities are much higher than that of electron as seen in the I_D-V_{TG} characteristics.

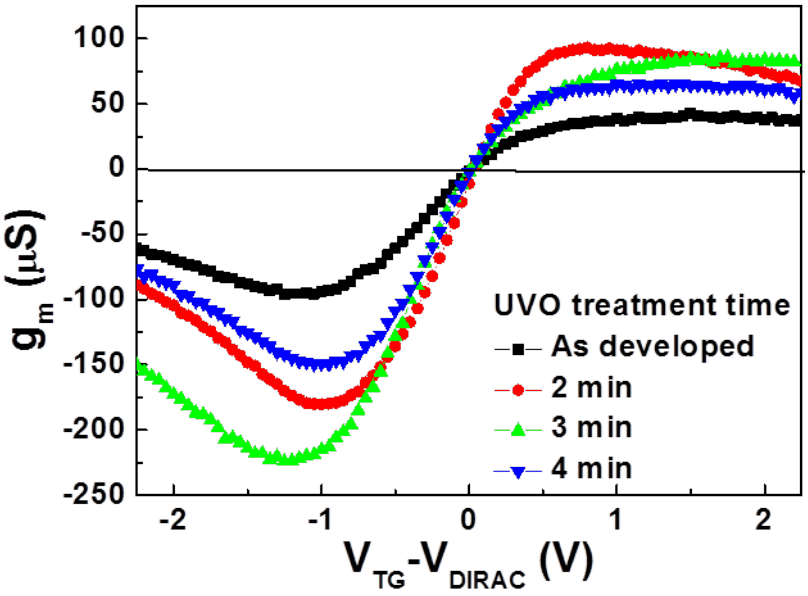


(a)

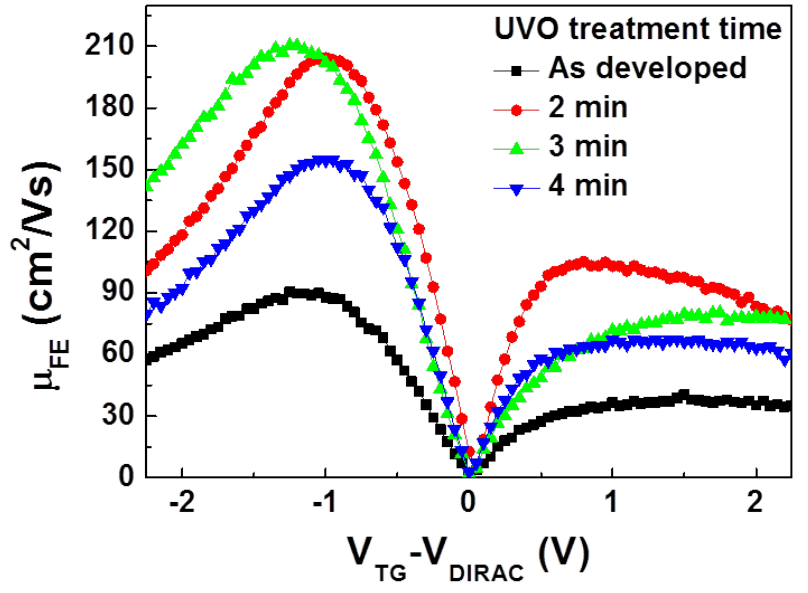


(b)

Figure 5.4. (a) Transfer characteristics of the drain current as a function of the top gate voltage (I_D-V_{TG}) and (b) total resistance as a function of the gate voltage (R_T-V_G) of GFETs with a overlapped S/D to gate structure and UVO_3 treated contacts.



(a)



(b)

Figure 5.5. (a) Transconductance and (b) filed effect mobiltiy of GFETs with overlapped S/D to gate structure and UVO_3 treated contacts.

The asymmetric behavior between the electron/hole currents can be understood as follows. Figure 5.6 shows the schematic of the band diagram in graphene under the metal. The graphene is doped and is subject to pinning. It is well known that the graphene in contact with Ni or Pd is p-type doped because of the difference in their workfunctions [9-11]. If graphene under the metal is p type doped, a negative gate biasing will cause a large hole current due to the low potential barrier formed at the p-p junction. On the contrary, a positive gate biasing will cause only a low electron current due to the high potential barrier formed at the p-n junction. We therefore relate the observed, much higher hole current than electron current to a p-type doping in graphene under the electrode metal.

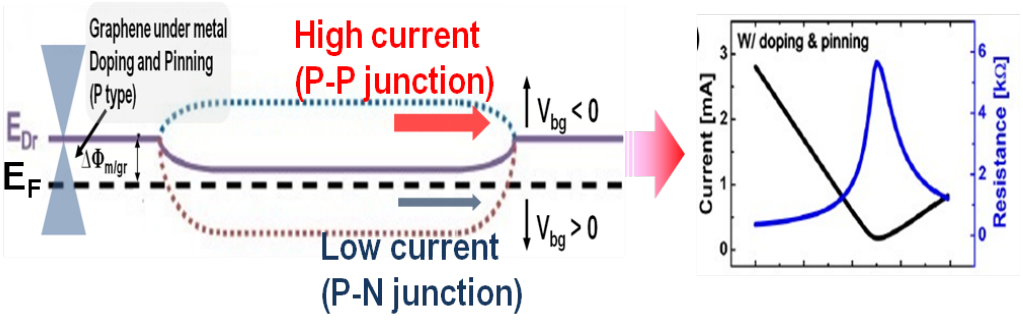
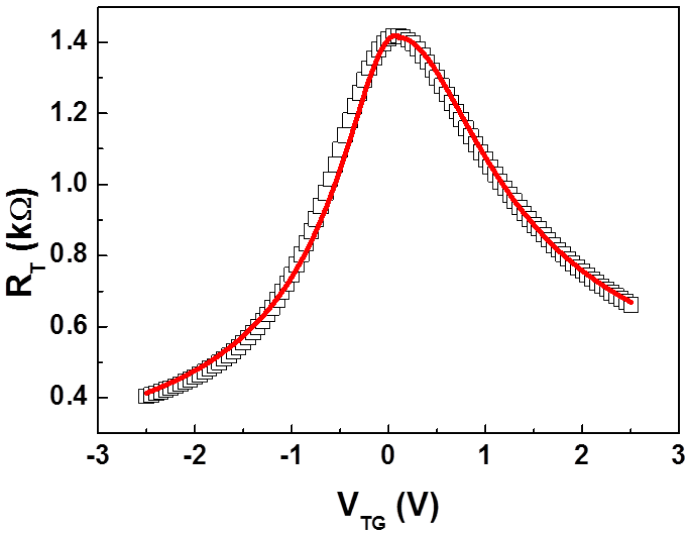
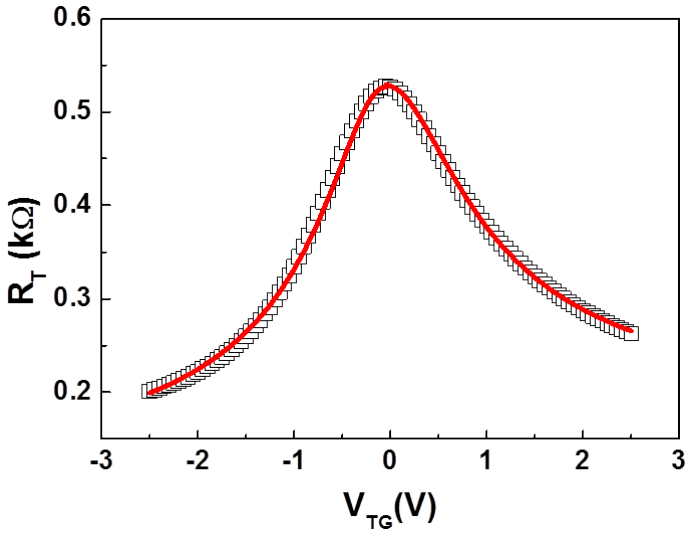


Figure 5.6. Schematic of band diagram in graphene under metal with doping and pinning.

Figures 5.7 (a)-(d) show the total resistance R_T versus the gate voltage V_G. The open squares are the experimental data and the red solid lines are the fitted curve using equation (3.2) in chapter 3, respectively. The fittings are in good agreement with the experiment in all devices. In these overlapped S/D to gate devices, the access resistance can be negligible and only the R_C should be the dominant factor in R_S. Figure 5.8 shows the normalized contact resistance as a function of the UVO_3 treatment time. As a result, we obtain a lowest contact resistance of 900 Ωμm in the device UVO_3-treated for 3 min. This value is comparable to or less than the reported values in the literature [12-14]. We therefore conclude that the UVO_3 treatment is quite promising in form the metal/graphene contacts for high performance TG-GFETs.



(a)


0.6
0.5
0.4
0.3
0.2
R_T (kΩ)
-3
-2
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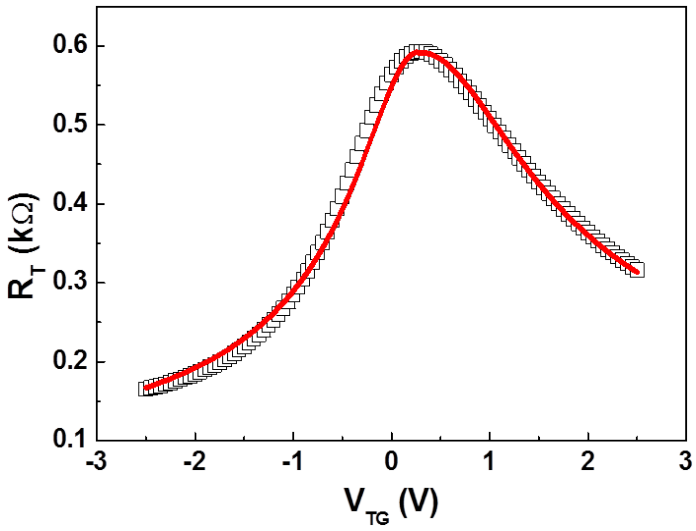
1
2
3
V_TG(V)

(b)


0.6
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R_T (kΩ)
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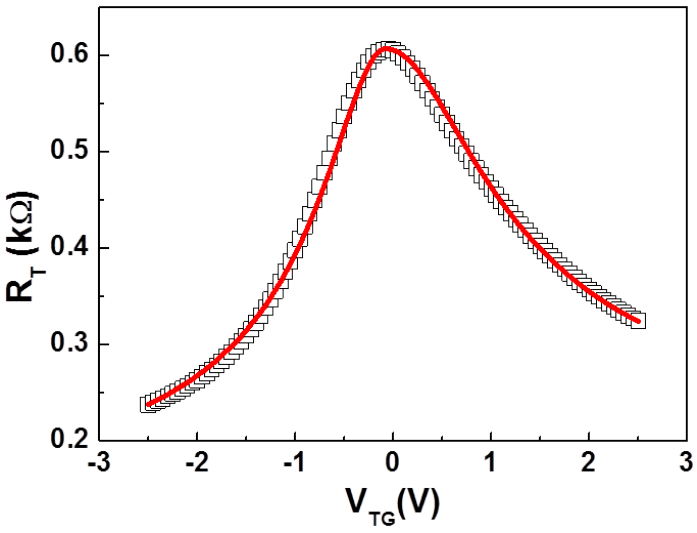
3
V_TG (V)

(c)



(d)

Figure 5.7. Measured R_T versus V_G (black square) of GFETs with overlapped S/D to gate structure and UVO_3 treated contacts (a) as developed (b) for 2 min (c) for 3 min (d) for 4 min and fitted result (red line) with equation, respectively.

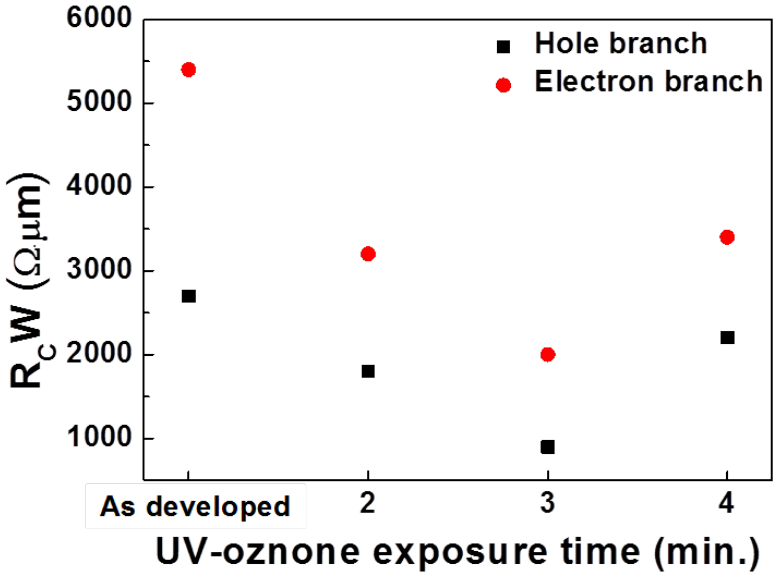


Figure 5.8. Normalized contact resistance as a function of UVO_3 exposure time in TG-GFETs.

When we compare the contact resistance R_C between BG-GFETs (Chapter 4) and TG-GFETs (this chapter), we find that the R_C of BG-GFETs is lower than that of the TG-GFETs. We will discuss the reason in the following. In case of the TG-FET, when the gate bias is applied the Dirac energy changes only in the channel region. A high potential barrier, will thus be formed at the edge part of the source and the drain regions. As a result, a small current will be injected from the source to the channel region, which effectively increases the contact resistance. In case of the global BG-FET, however, when the gate bias is applied the Dirac energy of graphene both under the metal and in the channel region will be simultaneously changed. Therefore, a low potential barrier is formed from the source to the channel region. As a result, a high current will be injected from the source to the channel region, which effectively decreases the contact resistance. Actually, it has also been reported that the back-gate independent contact resistance is much higher than the back-gate dependent contact resistance [9,15].

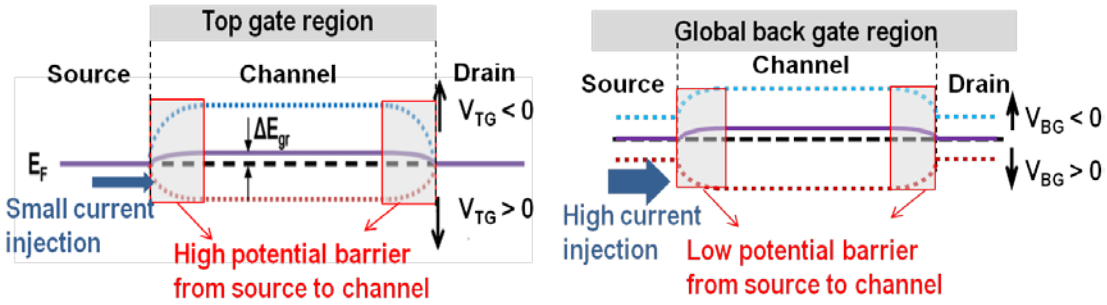


Figure 5.9. Schematics of band diagram of TG-GFET versus BG-GFET

5.4 Conclusion

We have succeeded in fabrication of TG-GFETs with overlapped S/D to gate structure and UVO_3 treated contacts. UVO_3 treatment effectively eliminates the residual photoresist and hence reduces the contact resistance at the M/G junctions. Reduction of the access region can also minimize the total resistance. As a result, a relatively low contact resistance of 900 Ωμm is obtained for the TG-GFET. The ON-current (I_{on}) is increased, and the field-effect mobility of 210 cm^2/Vs was obtained. UVO_3 processed M/G contact and overlapped S/D to gate structure are quite promising for realizing high performance GFETs.

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6

GFETs with solution-processed top gate and UV-Ozone-processed contacts

6.1 Introduction

As described by equation (3.2) in chapter 3, three primary parameters are affecting the total resistance in GFETs: channel mobility, access resistance and contact resistance. In other words, the performance of today's GFETs is primarily determined by these three parameters [1]. For betterment of the GFET performance, we therefore need to develop (1) a method to form gate dielectrics without losing the graphene's intrinsic properties [2-4], (2) a method to minimize the metal/graphene contact resistance [5-7], and (3) a device structure that minimizes the access resistance [8-10].

In chapters 2 and 3, we discussed the novel solution-processed gate dielectrics and its application to high performance GFETs. We demonstrated that the solution-processed gate dielectrics gives minimum defects, strains and dopings to graphene and is found quite effective to realize high intrinsic carrier mobilities.

In chapters 4 and 5, we discussed use of UVO_3-treated contacts and overlapped S/D to gate for reducing the series resistance. We confirmed that the UVO_3 treatment after a photolithographic process is quite effective in removing the PR residue without inducing substantial damages to graphene. By using the UVO_3 treatment, we obtained excellent electrical characteristics and low contact resistances. Furthermore, by introducing the overlapped S/D to gate structure, the total

resistance could be reduced by minimizing the access length.

In this chapter, we discuss fabrication of GFETs that include all the technologies described in previous chapters: the solution-processed gate dielectric, the UVO_3-treated contacts, and overlapped S/D to gate structure. The highest transconductance and field effect mobility have been obtained in this work.

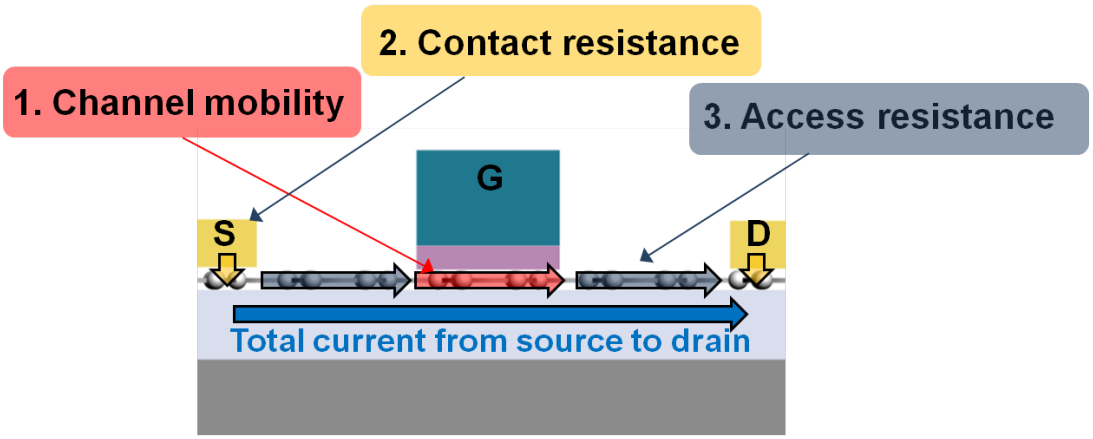


Figure 6.1. Schematic of three primary parameters in GFET.

6.2 Device Fabrication

The TG-GFET device fabricated in this chapter consists of the solution-processed gate dielectric, UVO_3 treated contacts, and overlapped S/D to gate structure. They were fabricated on a p-type Si wafer covered with a 90 nm-thick thermal SiO_2 layer. First, CVD graphene was transferred onto the Si substrate, which was cleaned with acetone, ethanol and deionized (DI) water. After defining the source and the drain regions by an image reversal process, the UVO_3 treatment was carried out for 3 min, based on the results obtained in chapters 4 and 5. The source and the drain electrodes (Ni/Au, 20/50 nm) were then formed on the graphene by electron-beam evaporation followed by a lift-off process. The samples were annealed in vacuum at 300 °C for 1 hour under the H_2/N_2 mixture ambient to remove the PR residue on the graphene channel. In order to form the top-gate dielectric layer, a 2 nm-thick Al layer was first deposited by electron-beam evaporation. The Al layer was then naturally oxidized at room temperature for 12 hours to become a seeding oxide layer, which absorbs the oxygen-related ad-species on the graphene. The spin-coating was carried out at a rotation speed of 4000 rpm for 20s. Subsequently, samples were exposed to an oxygen plasma at 30 W and 4 Pa for 2 min. Samples were then annealed at 250 °C in air for 2 hours. A 150 nm-thick Al layer as the gate electrode was deposited by an electron-beam evaporator and the gate electrode region was pattered by a photolithographic process. Finally, the Al and the Al_2O_3 layers were etched by H_3PO_4 to form the source and the drain region openings. The channel dimensions are 40 μm in width and 3 μm in length. The electrical characteristics were obtained at room temperature in air by using a semiconductor parameter analyzer (B1500, Agilent Technology).

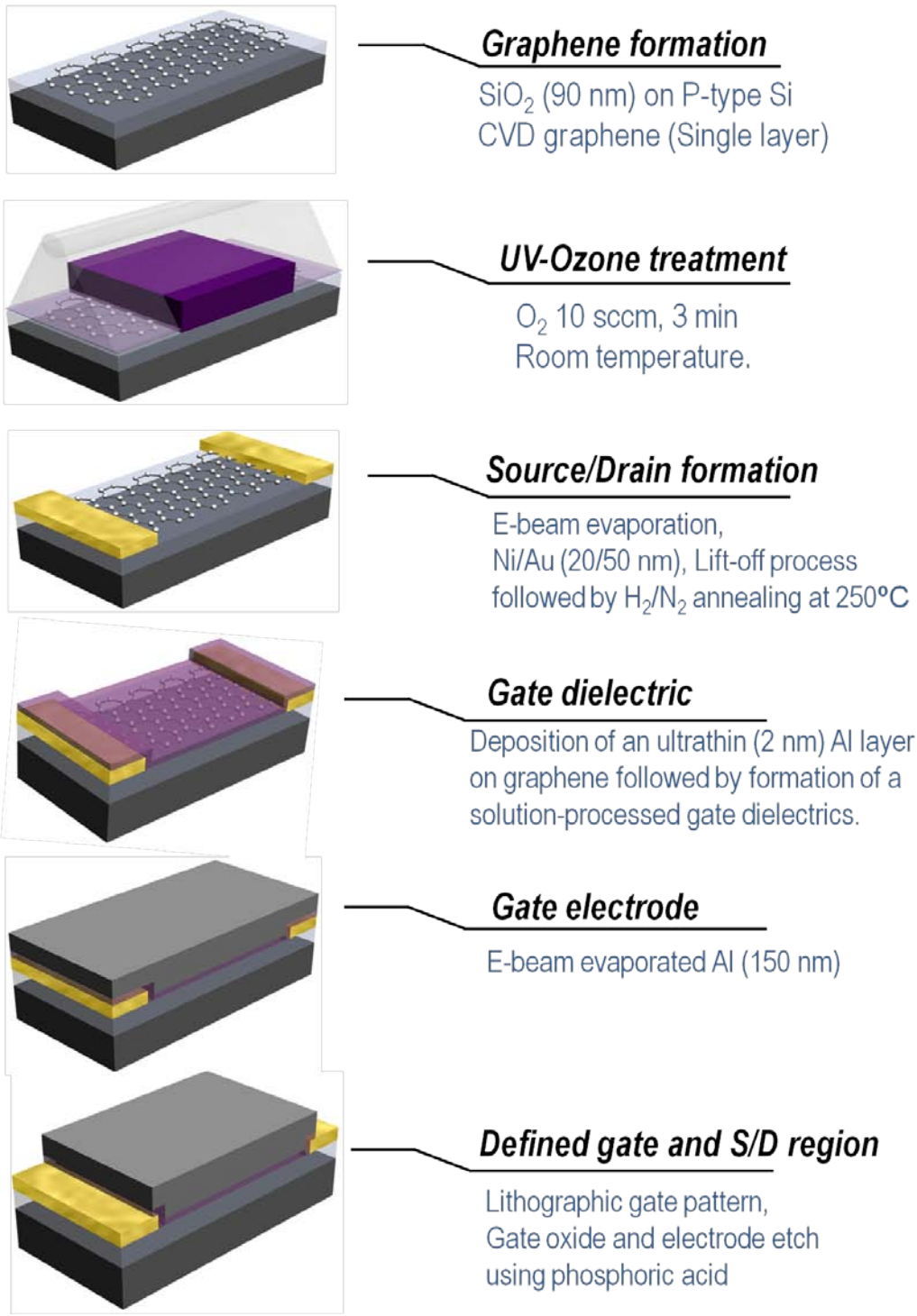
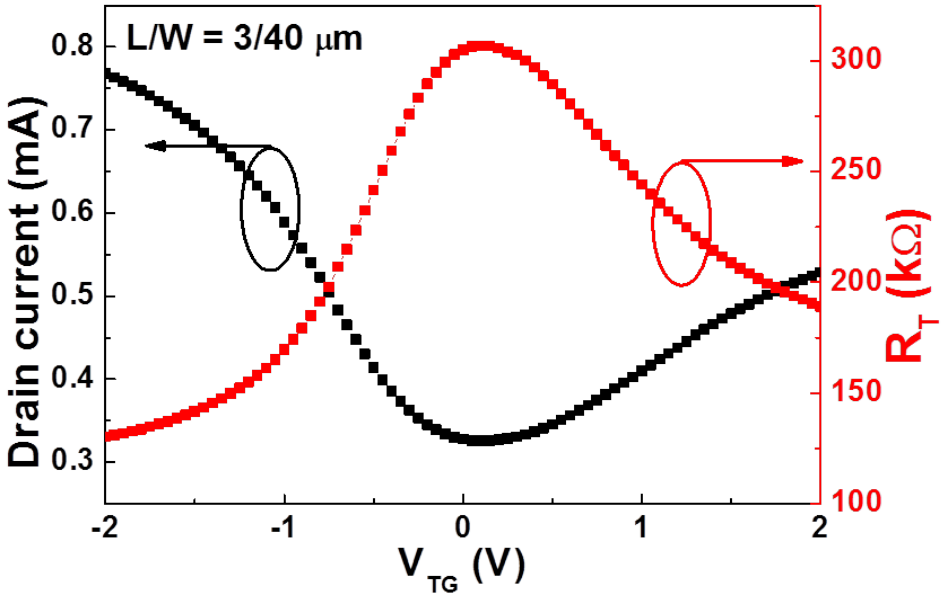


Figure 6.2. Fabrication sequence of TG-GFETs with solution-processed gate dielectric, UVO_3 treated contact and overlapped S/D to gate structure.

6.3 Results and Discussion

Figure 6.3 (a) shows the drain current and the total resistance R_T as a function of the gate voltage V_G. The drain voltage (V_D) is set at 100 mV. The device indicates a clear ambipolar conduction behavior with the Dirac voltage of around 0.1V. The resistance at the Dirac point was 0.3 kΩ, which can be compared to 0.6 kΩ of the device described in chapter 5, consisting of contacts processed with UVO_3 for 3min but not of the solution gate. This result clearly indicates that the solution-processed gate dielectric is effective in decreasing the total resistance. This can be attributed to increase of the conductance, resulting from the minimum hole doping and the minimum defects in the graphene channel layer.

Figure 6.3 (b) shows the transconductance and the field-effect mobility as a function of the gate voltage. These quantities are compared to other devices fabricated in this study in table 6.1. The proposed TG-GFET (Solution + UVO) shows the highest transconductance and the field-effect mobility among them. It is suggested that highest transconductance and the field-effect mobility are realized by minimizing the doping and the defect density in the graphene channel layer and by removing the contamination at the metal/graphene contacts.



(a)

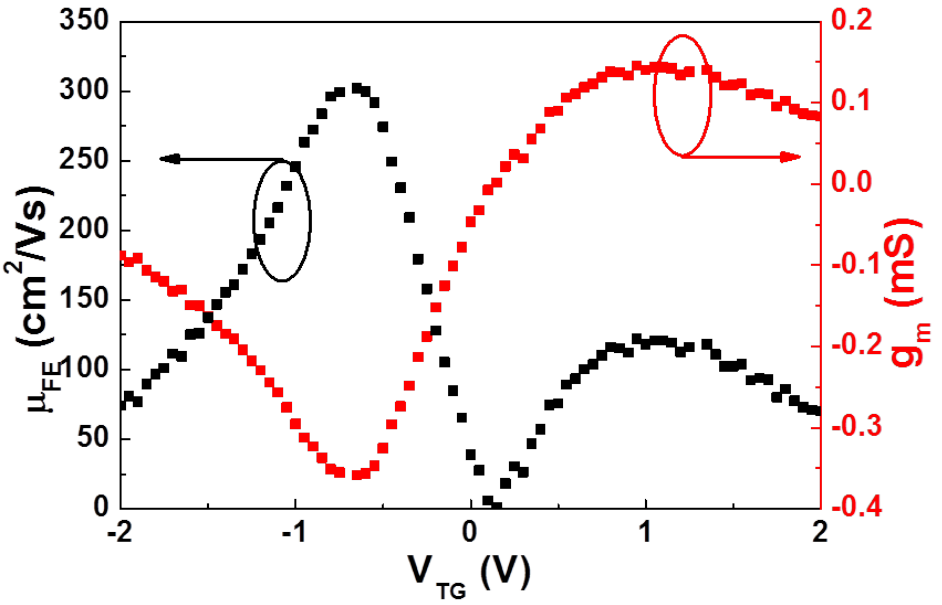


Figure 6.3. (a) Drain current and total resistance (R_T) and (b) Transconductance and field effect mobility as a function of the gate voltage.

Table 6.1. Comparison of transconductance and field effect mobility of fabricated device in the work

	Hole		**Electron**	
	g_m (μS)	**μ_{FE} (cm^2/Vs)**	**g_m (μS)**	**μ_{FE} (cm^2/Vs)**
Solution	*96*	*90*	*43*	*40*
UVO	*224*	*210*	*92*	*105*
Solution +UVO	*358*	*301*	*145*	*120*

Figure 6.4 shows the total resistance R_T versus the gate voltage V_G. The black squares are experimental data and the red solid line is a fitting by use of equation (3.2) in chapter 3. The fitting is in excellent agreement with the experiment. By this fitting, we extract the intrinsic carrier mobility μ_{int} of ~8600 cm^2/Vs, which is the highest value obtained in this study. The contact resistance of 900 Ω μm was also extracted (Table 6.2). These values are better than or comparable with those obtained in previous chapters. We therefore conclude that it is essential for realization of high performance GFETs to achieve not only high channel conductance but also low contact resistance, simultaneously.

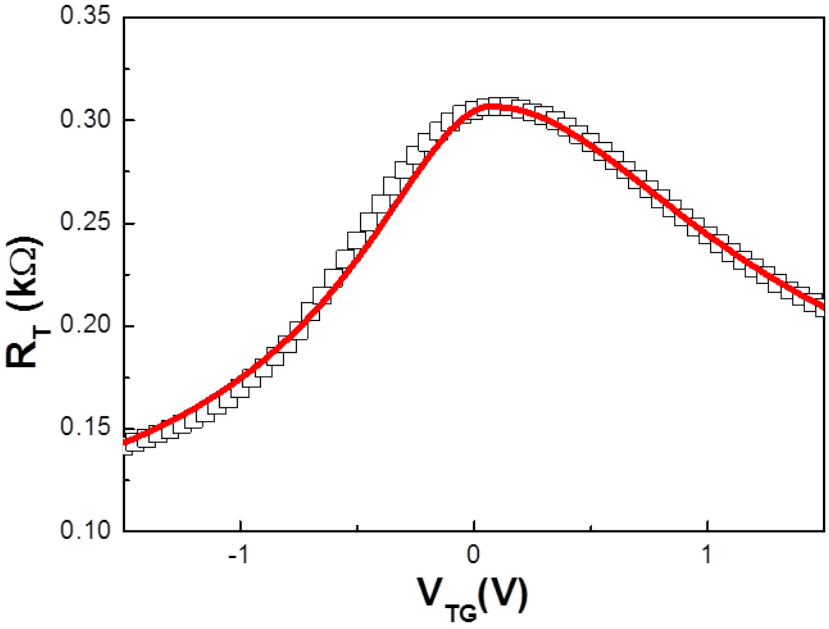


Figure 6.4. Total resistance R_T versus gate voltage V_G (black square) of the proposed GFETs and fitted result (red line) with equation (3.2), respectively.

Table 6.2. Comparison of intrinsic mobility and contact resistance of fabricated device in the work.

	$\mu_{int.}$ (cm^2/Vs)	R_c ($\Omega \cdot \mu m$)
Solution	e : 8430 h : 8400	-
UVO	-	*900*
Solution +UVO	e : 8650 h : 8620	*900*

6.4 Conclusion

The solution-processed gate dielectrics, the UVO_3-treated contacts, and a overlapped S/D to top-gate electrode have been combined to fabricate GFETs. Highest transconductance and field-effect mobility, not achievable by solution-gate or UVO_3-contacts alone, have been obtained. These high transconductance and field effect mobility values are attributed to both increase of the intrinsic mobility (due to the solution-gate) and reduction of the contact resistance. Combination of the solution-processed gate dielectric and UVO_3-treated contact is quite promising for realizing high performance GFETs.

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7

Conclusion

Graphene has attracted increasing attention as a strong candidate for the post-silicon channel material due to its exceptional physical, thermal, and electrical properties, such as ultrahigh carrier mobility, thermal and chemical stability, 2D structure and Si process compatible. This research has been focused on the betterment of the process and the design of graphene-based field-effect transistors (GFET) to optimize its performance. The following is the summary of each chapter.

Chapter 2. Solution-processed gate dielectric for GFETs

Based on a solution-process method, a gate dielectric Al_2O_3 thin film was successfully fabricated on graphene with a sufficiently high quality. Based on a systematic characterization of the film, a modified solution-process method, which consists of initial formation of ultrathin Al natural oxide, spin-coating of Al_2O_3 precursor liquid, oxygen plasma treatment, and PDA, has been proposed. It was found that the PDA at 250°C for 2 hours gives a minimum doping and strain to graphene and a highest dielectric constant to Al_2O_3. A strongly temperature-dependent doping behavior was found to exist, which can be further utilized in controlling the threshold voltage of GFETs.

Chapter 3. Electrical properties of GFETs with solution-processed top-gate

TG-GFETs with the gate dielectrics deposited by the modified solution method have been fabricated. The gate process consists of initial formation of a natural oxide layer of Al, spin-coating of

the sol-gel precursor for Al_2O_3, the oxygen plasma treatment, and PDA. PDA at 250 ºC was found ideal in achieving the high intrinsic carrier mobility (~8400 cm^2/Vs) in the PDA temperature range (200-300 ºC) tested. With this high potential, the modified solution-processed gate dielectrics are quite promising for realizing high performance GFETs.

Chapter 4. UV-ozone-processed contacts for GFETs

UVO_3 treatment has been demonstrated to be quite effective in reducing the contact resistance, which is related to removal of the interfacial contaminations. The UVO_3 treatment after the photolithographic process is found quite effective in removing the PR residue without inducing substantial damages to graphene. As a result, the transconductance and the filed-effect mobility characteristics are remarkably improved by the UVO_3 treatment of 3 min. Finally, a low contact resistance ranging from 100 to 400 Ωμm was obtained, which is comparable or less than the reported values made on the same material system. These results provide important insights for betterment of the GFET performance.

Chapter 5. Electrical properties of GFETs with a overlapped S/D to top-gate and UV-ozone-processed contacts

TG-GFETs with a overlapped S/D to gate structure and UVO_3-treated contacts have been successfully fabricated. The UVO_3 treatment effectively eliminates the residual photoresists and hence reduces the contact resistance at the M/G junctions. Reduction of the access region can also minimize the total resistance. As a result, a relatively low contact resistance of 900 Ω μm is obtained for the TG-GFET. I_{on} is increased, and the field-effect mobility of 210 cm^2/Vs was obtained. UVO_3 processed M/G contact and overlapped S/D to gate structure are quite promising for realizing high performance GFETs.

Chapter 6. GFETs with solution-processed top gate and UV-ozone-processed contacts

GFETs integrating all the technologies developed in chapters 2-5 have been fabricated: the solution-processed gate dielectrics, the UVO_3-treated contacts, and overlapped S/D to top-gate electrode. Highest transconductance and field-effect mobility, not achievable by the solution gate or the UVO_3-treated contacts alone, have been obtained. These high transport values are attributed to both the increase of the intrinsic mobility (due to solution gate) and the reduction of the contact resistance. It is therefore concluded that combination of solution-processed gate dielectric and UVO_3-treated contacts, as well as overlapped S/D to top-gate, is quite promising for realizing high performance GFETs.

Publications and Conference Proceedings

List of Publications

1. Myung-Ho Jung, **Goon-Ho Park**, Tomohiro Yoshida, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, “High-Performance Graphene Field-Effect Transistors With Extremely Small Access Length Using Self-Aligned Source and Drain Technique”, *Proceedings of IEEE*, 2013.

2. **Goon-Ho Park**, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, “Solution-processed Al_2O_3 gate dielectrics in graphene field effect transistors”, *Scientific reports*, preparing.

3. **Goon-Ho Park**, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, “High-performance graphene field-effect transistors with solution-processed Al_2O_3 gate dielectrics”, preparing.

4. **Goon-Ho Park** and Won-Ju Cho, "Reliability of modified tunneling barriers for high performance nonvolatile charge trap flash memory application", Applied Physics Letters, Vol. 96, Issue 4, pp.043503 (2010)

5. **Goon-Ho Park**, Myung-Ho Jung, Kwan-Su Kim, Hong-Bay Chung, Won-Ju Cho, "Tunneling barrier engineered charge trap flash memory with ONO and NON tunneling dielectric layers", Current Applied Physics, Vol. 10, Issue 1, pp. e13-e17 (2010)

International conference

1. **Goon-Ho Park** and Maki Suemitsu, "Reliability of nonvolatile memory using modified tunneling barrier and high-k charge trap/blocking layers", The 5th International Symposium and the 4th Student Organizing International Mini-Conference on Information Electronics Systems, 2012.

2. **Goon-Ho Park**, Myung-Ho Jung, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, "Oxygen-Plasma Formation of Alumina for a Gate Dielectric in Graphene Field Effect Transistors", 3rd International Symposium on Graphene Devices (ISGD), 2012

3. **Goon-Ho Park**, Myung-Ho Jung, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, "Plasma-oxidized Al_2O_3 for gate dielectrics in Graphene Field Effect Transistors", International Microprocesses and Nanotechnology Conference (MNC), 2012.

4. **Goon-Ho Park**, Won-Ju Cho and Maki Suemitsu, "Solution-Processed Al_2O_3 for a Gate Dielectric in Graphene Field Effect Transistors", TeraNano Student Seminar, 2013

5. **Goon-Ho Park**, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji, and Maki Suemitsu, "Solution-Processed Al_2O_3 for a Gate Dielectric in Top-Gated Graphene Field Effect Transistors", *26th International Microprocesses and Nanotechnology Conference*, 2013

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1. 朴 君昊, 鄭 明鎬, 全 春日, 吹留 博一, 吉田 智弘, 末光 哲也, 尾辻 泰一, 末光 眞希, “Graphene field effect transistor using a novel self-aligned technique for high speed applications”, 第 59 回応用物理学関係連合講演会, 2012

2. Goon-Ho Park, Myung-Ho Jung, Hirokazu Fukidome, Tetsuya Suemitsu, Taiichi Otsuji and Maki Suemitsu, “Al_2O_3 Gate dielectric formed by novel solution-process method for graphene field effect transistors”, 第 19 回 ゲートスタック研究会, 2014.

3. Goon-Ho Park, Hirokazu Fukidome, and Maki Suemitsu, “Al_2O_3 solution-processed gate dielectric for graphene transistor”, 第 27 回東北若手の会, 2014.

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1. 日本**学術振興会特別研究員** DC2

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