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Self-checking multiple-valued circuit based on dual-rail current-mode differential logic

Self-Checking Multiple-Valued Circuit
Based on Dual-Rail Current-Mode Differential Logic

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Abstract

A multiple-valued current-mode (MVCM) circuit based on dual-rail differential logic has been proposed for high-speed arithmetic systems at a low supply voltage. This paper presents a new totally self-checking circuit based on dual-rail MVCM logic, where almost all the basic components except a differential-pair circuit have been already duplicated, which results in small hardware overhead compared with a non-self-checking circuit based on dual-rail MVCM logic. Moreover, the performance of the proposed self-checking circuit is superior to that of full duplication of the non-self-checking circuit based on dual-rail MVCM logic in terms of transistor counts, switching delay and dynamic power dissipation under a 0.5-µm standard CMOS technology

1. Introduction

Fault-tolerance techniques, as well as high-performance system architectures and circuit design techniques [1]-[3], have become increasingly important in recent submicron VLSI chips. One of the key technologies for the detection of faults inside VLSI chips is to use a self-checking circuit that has the capability to test for the occurrence of a fault within the circuit by a normal input, as well as to detect an error at the input itself. Furthermore, by the use of self-checking techniques, transient and permanent faults can be also detected during normal operations [4], [5]. However, a self-checking circuit based on the conventional binary gates requires about twice as many transistors as the corresponding non-self-checking binary circuit, which limits a wide use of the self-checking system in the present VLSI chips.

On the other hand, an MVCM circuit based on dual-rail differential logic has been proposed for high-speed arithmetic systems at a low supply voltage. A dual-rail

MVCM circuit is used to make a signal-voltage swing small yet driving capability large. In fact, the use of dual-rail MVCM logic in a 1.5V-supply multiple-valued multiplier chip enables high-speed operations with reduced transistor and interconnection counts at low power dissipation in comparison with that of a corresponding binary CMOS one [6], [7]. Moreover, in the dual-rail MVCM circuit, there are three basic components, that is, an adder for current-mode linear sum, a comparator and a differential-pair circuit (DPC) to generate a dual-rail multiple-valued current output. These first two basic components except a DPC have been already duplicated.

In this paper, a totally self-checking circuit based on dual-rail MVCM logic is proposed to realize highly reliable VLSI systems with keeping high-speed operation capability. A new non-self-checking (NSC) DPC proposed here has a redundant function because one of the two outputs depends on only a single input in the NSC-DPC. Accordingly, a self-checking (SC) DPC can be designed by the duplication of the proposed NSC-DPC. That is, the dual-rail inputs in one NSC-DPC are shared by the dual-rail inputs in the other one, and where only a single output from each NSC-DPC is used as the resulting dual-rail outputs in the SC-DPC. Consequently, the use of the proposed DPC makes it possible to design a totally self-checking circuit with keeping high driving capability based on dual-rail MVCM logic, which results in small hardware overhead compared with the corresponding NSC circuit based on dual-rail MVCM logic.

To confirm the usefulness of the proposed self-checking circuit, its performance is compared with that of the corresponding full duplication of a dual-rail MVCM circuit in terms of transistor counts, switching delay and dynamic power dissipation under a 0.5-µm standard CMOS technology. As a result, the number of transistors and dynamic power dissipation in the proposed self-checking circuit is reduced to about 67 percent and 68

percent, respectively, in comparison with those of the full duplication of the dual-rail MVCM circuit under the same switching delay.

2. Model of a Multiple-Valued Self-Checking VLSI System

In this section, we describe an MVCM circuit model discussed here, and define a totally self-checking circuit against a single stuck-at fault in the VLSI system

2.1 Basic components of a multiple-valued VLSI

Figure 1 shows three basic components of the proposed MVCM circuit. By the combination of these components, we can realize any multiple-valued combinational circuits. A comparator is to compare an R-valued input X with a threshold value T, and to generate a binary output G where $X, T \in \mathbf{R} = \{0, 1, \cdots, R-1\}$ and $G \in \{0, 1\}$. If X is less than T, G becomes 0. Otherwise, G becomes 1. A DPC is to generate one of three multiple-valued differential-pair outputs (0, 0), (K, 0) and (0, K) in accordance with binary differential-pair inputs where its function is defined in Figure 1. An adder forms arithmetic sum of two multiple-valued inputs A and B where $A, B \in \mathbf{R}$. For example, Figure 2 shows a block diagram of an MVCM circuit whose function is given as

$$Z = \begin{cases} 1 & (X > T), \\ 0 & (X < T). \end{cases} \tag{1}$$

2.2 Definition of a totally self-checking circuit

Self-checking can be defined as the ability to verify automatically, whether there is any fault in logic without the need for externally applied test stimuli. We will consider only malfunctions in the circuit caused by single faults. The concept of a totally self-checking circuit, which can generate a detectable erroneous output for every fault from prescribed set during normal operations, is defined in the following [4]:

Fault Secure (FS): A circuit is fault secure if, for every fault from a prescribed set, the circuit never produces an incorrect code output for code inputs.

Self Testing (ST): A circuit is self-testing if, for every fault from a prescribed set, the circuit produces a non-code output for at least one code input.

Totally Self-Checking (TSC): A circuit is totally self-checking if it is both self-checking and fault secure.

Generally, a duplicated circuit is TSC. Figure 3 shows a self-checking circuit which has a fully duplicated structure of a single-rail MVCM circuit shown in Figure 2. Therefore, its hardware becomes twice as many as that

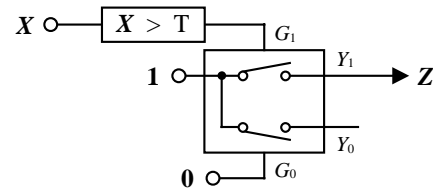**Figure 1.** Definition of basic components in an MVCM circuit.

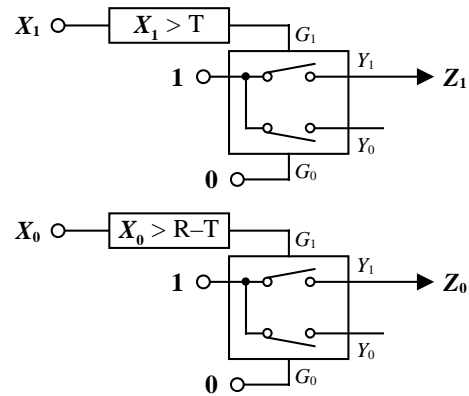**Figure 2.** Single-rail MVCM threshold detector.

Figure 3. Self-checking circuit with a fully duplicated structure of two single-rail MVCM threshold detectors.

of the circuit shown in Figure 2. In this self-checking R-valued logic circuit, the code words and non-code words are shown in Table 1. The dual-rail code words satisfy the

Table 1. 5-valued dual-rail code.

single-rail	dual-rail	Logic Value
X	(X_1, X_0)	
0	(0, 4)	"0"
1	(1, 3)	"1"
2	(2, 2)	"2" Code word
3	(3, 1)	"3"
4	(4, 0)	"4"
–	otherwise	Non-code word

Figure 4. Duplicated dual-rail MVCM threshold detector with complementary logic.

following relation.

$$X_1 + X_0 = R - 1 \qquad (2)$$

2.3 High-performance self-checking circuit based on dual-rail MVCM logic

In order to improve the performance of the single-rail MVCM circuit shown in Figure 3, DPCs must be controlled by dual-rail complementary inputs. Figure 4 shows a block diagram of a self-checking circuit using a dual-rail MVCM circuit. Its function is the same as that described by Eq. (1). In this circuit, its switching speed becomes higher than that of the self-checking circuit based on single-rail MVCM logic as shown in Figure 3 because of the large driving capability of DPC. But it requires twice as many input nodes and comparators as the corresponding single-rail MVCM circuit, which causes serious hardware overhead.

Figure 5 shows a block diagram of the proposed self-checking circuit based on dual-rail MVCM logic. Since the functions of two comparators, *C00* and *C01*, are same as two comparators, *C11* and *C10*, respectively, they can be shared to *C11* and *C10* as shown in Figure 5.

Now, let us discuss about the self-checking ability of Figure 5. The DPC has a redundant function, because it depends on only a single input G_1 as shown in Figure 1. As an example, Figure 6 shows a block diagram of the proposed self-checking circuit with a stuck-at-1 fault at the output G_1 of the comparator *C11*. The output of the comparator *C11* is connected to G_{11} and G_{00}. However, the output Z_0 in the *DPC2* depends on only G_{01}, so that *DPC2* operated correctly even when the S-a-1 fault happens at G_{00}. In this way, even if one comparator fails in the circuit of Figure 5, it satisfies the self-checking ability.
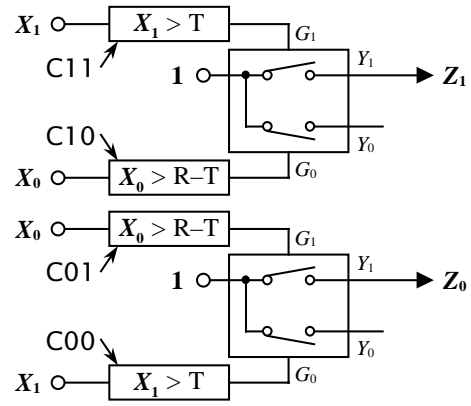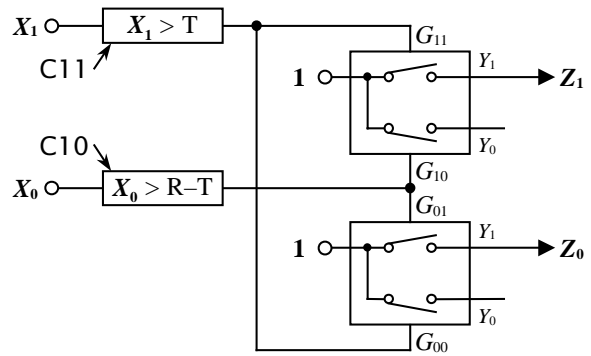

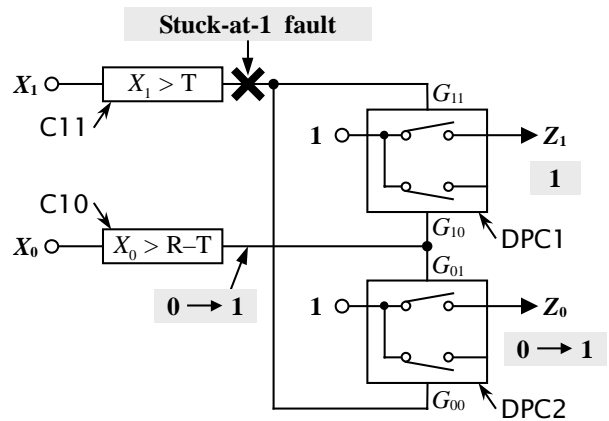**Figure 5.** Proposed dual-rail MVCM threshold detector.

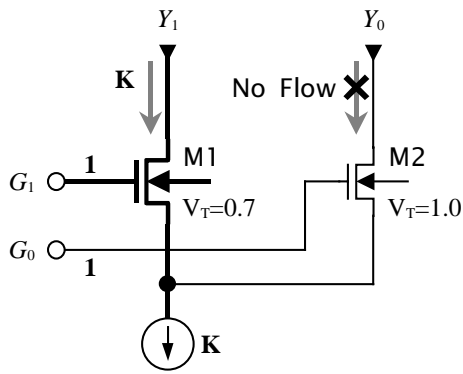**Figure 6.** Proposed dual-rail MVCM threshold detector with a stuck-at-1 fault.

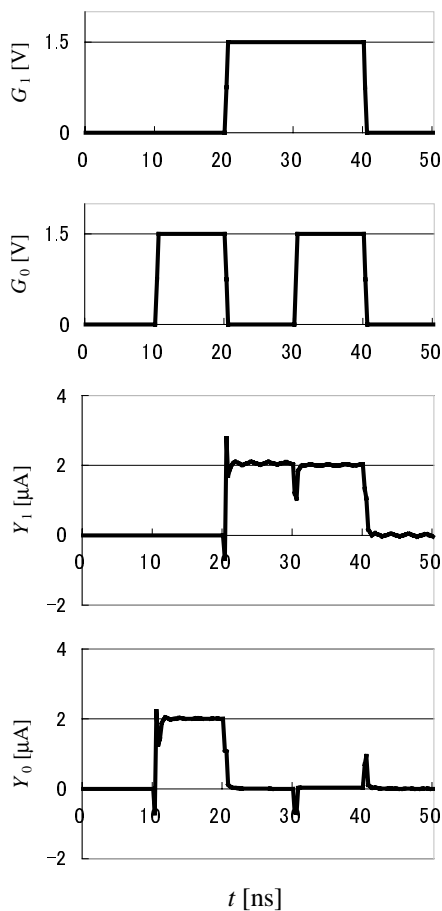**Figure 7.** Behavior of the proposed DPC.

Figure 8. Simulated waveforms of the circuit of Figure 7.

3. Design of a Multiple-Valued Self-Checking Circuit

Figure 7 shows the proposed DPC of Figure 1. The threshold voltage of the nMOS transistor *M1* becomes

Figure 9. Basic building blocks.

lower than that of the nMOS transistor *M2*. The lower threshold voltage increases current through transistor. Using this characteristic realizes the selective switching of *M1* when both gate voltages of *M1* and *M2* are same each other by just three transistors.

Figure 8 shows the HSPICE simulation of a DPC. The simulation clearly demonstrates that the expected correct code outputs (K, 0) are appeared when their inputs are (1,1). Figure 9 shows the relationship between the basic components and their circuit diagrams. Current mirror creates replicas of an input *X*. Current source creates a constant value *K*. MVCM circuits consist of these five components shown in Figure 9.

4. Evaluation

Figure 10 shows a circuit diagram of the proposed self-checking circuit shown in Figure 5. The output of the comparator is distributed to two DPCs, so that a compact self-checking circuit can be designed because of no additional comparators for dual-rail MVCM logic.

Table 2 summarizes the comparison of performances among three kinds of MVCM circuits using a
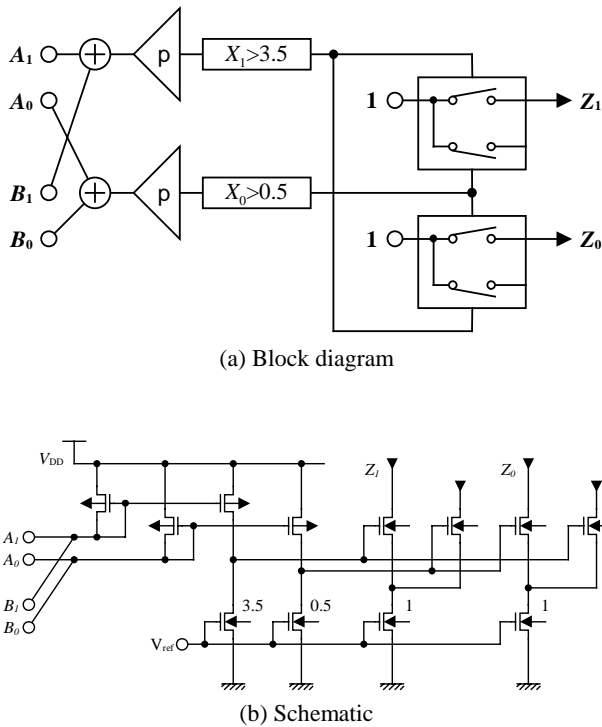
(a) Block diagram

(b) Schematic

Figure 10. Self-checking MVCM threshold detector.

Table 2. Comparison of three MVCM circuits.

	Non-self-checking MVCM circuit	Fully duplicated MVCM circuit	Proposed MVCM circuit
TSC	No	Yes	Yes
Supply Voltage [V]	1.5	1.5	1.5
Delay [ns]	3.5	3.5	3.5
Power dissipation [μW]	8.3	16.7	11.4
Number of Transistors	9	18	12

delay of the transistor in comparison with that of a normal transistor.

As a future problem, it is also important to design a DPC with small overhead of a switching delay and keeping small transistor counts.

conventional non-self-checking design, a fully duplicated design, and the proposed design, respectively. The use of the proposed NSC-DPC makes it possible to reduce the number of comparators in a self-checking circuit. As a result, in case of the same switching delay, the power dissipation and the number of transistors of the self-checking circuit using the proposed NSC-DPCs are reduced to about 68 percent and 67 percent, respectively, in comparison with those of the corresponding full duplication of an NSC dual-rail MVCM circuit under a 0.5-μm standard CMOS technology.

5. Conclusion

A new compact NSC-DPC based on dual-rail MVCM logic has been proposed, and is useful for the realization of a totally self-checking system with keeping high speed operations at a lower supply voltage. In fact, its performance is superior to that of the equivalent full duplication of an NSC dual-rail MVCM circuit in terms of transistor counts and power dissipation under the same switching delay.

Although the use of the transistor with a higher threshold voltage makes it possible to design a compact DPC with a redundant function, it increases the switching

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