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Multiple-Valued Content-Addressable Memory Using Metal-Ferroelectric-Semiconductor FETs

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Abstract

This paper presents a design of a non-volatile multiple-valued content-addressable memory (MVCAM) using metal-ferroelectric-semiconductor (MFS) FETs. An MFSFET is an important device with, a non-destructive read scheme. Multiple-valued stored data are directly represented by remnant polarization states that correspond to threshold voltages of an MFSFET. Since one-digit comparison between, multiple-valued input and stored data is performed by the combination of two different threshold operations, a one-digit comparator can be designed by two MFSFETs. The use of the one-digit comparator makes it possible to design a, compact MVCAM cell. It is evaluated that the performance of the proposed MVCAM is superior to that of some binary and multiple-valued CAMs in terms of bit density, peripheral-circuit complexity, access speed. and functionality.

1. Introduction

Real-time programmable and non-volatile memories with a one-transistor cell structure are one of the key modules in the present high-performance system LSIs. Ferroelectric(FE) memory devices have increasingly attracted attention because they are non-volatile memories with the capability of high-speed read and write operations. For example, FE capacitors are about, ten-times larger than that of the SiO_2 film, so that, they have a potential advantage to implement, high-density memories. A one-transistor memory cell can be implemented by only a single MFSFET with a non-destructive read operation.

It is well known that, in the present giga-scale system on-a-chip integration era, accelerating the evolution in chip density causes a communication bottleneck between memory and logic modules. A logic-in-memory structure: in which storage functions are distributed over a logic-circuit plane, is a key technology to solve the above problem. CAM is a typical application of such a logic-in-memory VLSI architecture. Until now, several high-performance CAMs have been reported [1]-[6]. However it has been difficult to solve the trade-off between real-time programmability and non-volatility with keeping a compact CAM cell circuit. A few challenging works, a MVCAM using FE devices: have been reported[6].

In this paper, a new design of an MVCAM using non-destructive FE devices such as MFSFETs is proposed. Multiple-valued stored data in the MVCAM cell are directly represented by threshold voltages of an MFSFET that can be programmed by controlling remnant polarization states. Multiple-valued one-digit comparison is performed by the logical product AND of two different, threshold operations. Since the use of precharge-evaluate logic makes it possible to implement, a two-input, AND gate by just wiring, an MVCAM cell can be designed by two MFSFETs. An MVCAM word circuit is also designed by series connection of the cell circuits together with precharge-evaluate logic, so that an n-digit MVCAM word circuit, can be realized by $2n$ MFSFETs. Moreover, the performance of the proposed MVCAM is compared with that of a binary dynamic CAM[2] and non-volatile MVCAMs[3],[5],[6] in terms of non-volatility, real-time programmability, a bit density, an execution speed, and peripheral-circuit simplicity. As a result,, it is demonstrated that its performance is superior to that of the other CAMs.

2. Review of MFSFETs

2.1 Characteristics of MFSFETs

An MFSFET structure is similar to a conventional metal-oxide-semiconductor(MOS) FET with the exception that the gate insulating layer is replaced by an active ferroelectric thin film. Figure 1 shows a cross-sectional view and a symbol of an MFSFET. An FE

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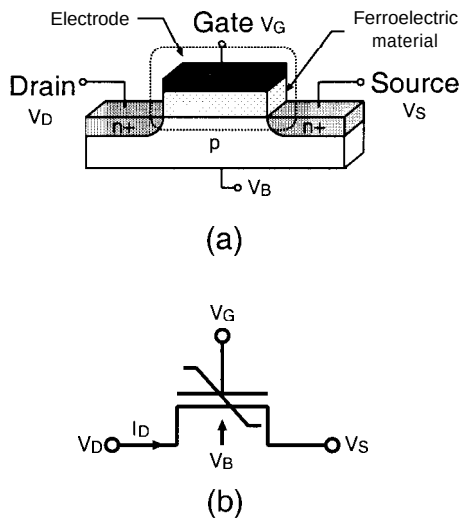

Figure 1. MFSFET structure, (a) Cross-sectional view, (b) Symbol.

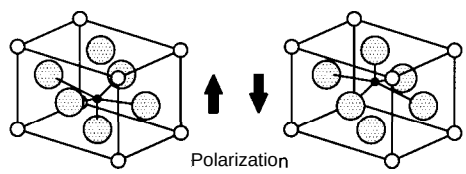

Figure 2. Perovskytestructure.

material c0nsist.s of a Perovskytestructure as shown in Figure 2, which is transformed when an atom at the center of a lattice causes a polarization by a shift from an electrically neutral state according to the external electric field which is determined by an applied voltage and thickness of FE thin films. This characteristic is represented by a hysteresis loop. Figure 3 shows polarization vs voltage hysteresis loops of the FE film. One of the most important characteristics in the FE material is to have a remnant polarization within the saturated hysteresis loop when the voltage across the FE film is zero. It, implies that the FE film can preserve information that corresponds to a remnant polarization state without, voltage supply, i.e. an MFSFET is capable of a non-volatile memory device. Recently: MFSFETs have been reported using the variety of the FE material such as $Bi_4Ti_3O_12$[7], $LiNbO_3$[8], and $SrBi_2Ta_2O_9$[9].

Figure 3 also shows an example of a binary data assignment with remnant polarization states. As the remnant polarization is determined by an applied voltage across the FE film, whose magnitude is larger than the coercive voltage V_C, a logic state, "1" or "0", can be written into the SIFSFET by the gate voltage V_G and the bulk voltage V_B. The required voltage applied to gate electrode of the MFSFET to write data is lower

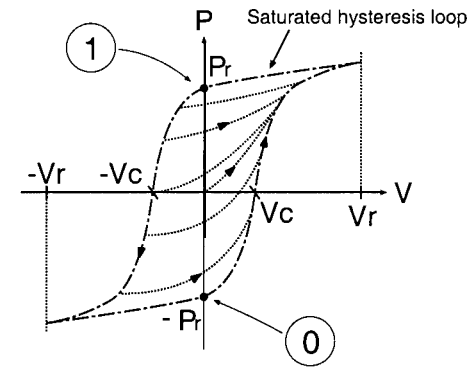

Figure 3. Hysteresis loop characteristics of an FE material.

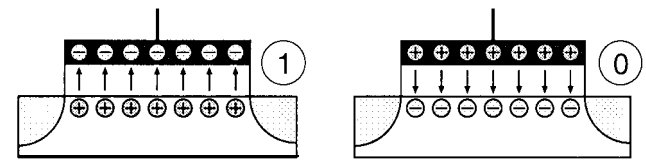

Figure 4. Compensation charge in the semiconductor surface.

than that of conventional non-volatile memory devices such as a floating-gate MOS transistor.

When the external voltage is removed, the remnant, polarization will induce an electric field which attracts positive (or negative) compensation charge to the semiconductor surface as shown in Figure 4. Therefore, the carrier density of a semiconductor at the interface will be inverted, which makes it possible to shift the threshold voltage. Figure 5 shows the threshold voltage corresponding to the MFSFET state "0" and "1". In a read scheme: V_B is fixed to the ground level. When read gate voltage V_{RF} is applied to V_G, the switching state in the MFSFET depends on the polarization state in the FE film, i.e. stored data. Therefore: stored data in the SIFSFET is read as "on" and "off" states. As V_{RF} is low enough, the polarizations state in the FE film remains the previous state. Therefore: the MFSFET can realize a non-destructive read operation.

Consequently, an MFSFET is capable of being used as a non-volatile memory device with a non-destructive read scheme. Principle of the operation is similar to a Floating-Gate MOS Transistor, but an MFSFET has the advantage of a high-speed and a low power write scheme due to the characteristic of FE films.

2.2 Multi-level threshold programming in MFSFETs

In an MFSFET, a stored value is represented by remnant polarization states. Therefore, several rem-

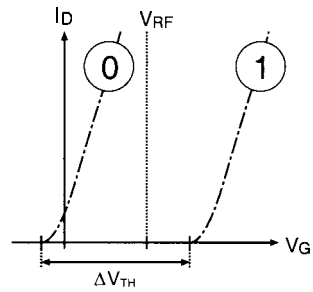

Figure 5. Relationship between threshold voltage and the remnant polarization states.

nant polarization states are required for multiple-valued data storage. For example, Figure 6 shows the relationship between four remnant polarization states and the assignment of four-valued data. Four remnant, polarization states are obtained by the following method. The polarization in an FE film moves on branches as shown in Figure 4. This means that P_{r0} and $-P_{r0}$ are produced by the transition of the polarization through $a \rightarrow h \rightarrow c$, and $d \rightarrow e \rightarrow f$, respectively.

Consider the storage of "2" in the four-valued logic into MFSFETs. Figure 7 shows the timing diagram and polarization states for a write scheme. First, V_{r1} is applied to the gate electrode of the MFSFET, and then zero is applied. At that moment: the polarization stays on a. Second, $-V_{r0}$ is applied. and then zero is applied. The polarization changes from a to c through b.Consequently, the remnant, polarization in FE films is P_{r0}, i.e. four-valued data "2" is stored.

Threshold voltages are shifted depending on remnant polarization states. If there are four remnant polarization states, we can utilize the four level threshold voltages. This characteristic is important, to design a CAM cell structure using MFSFETs.

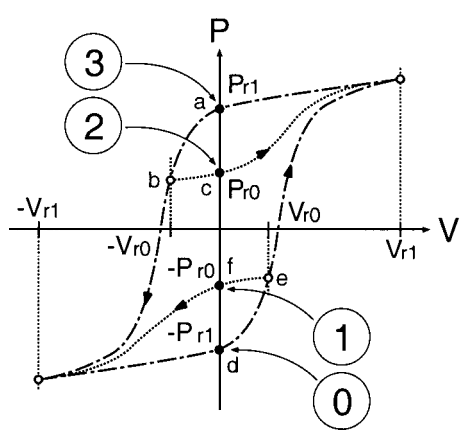

Figure 6. Four remnant polarizations states

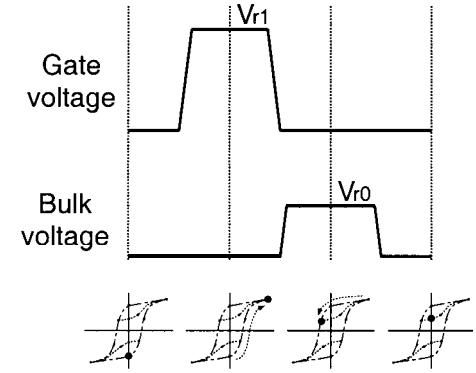

Figure 7. Timing diagram and the polarization state for a write scheme of a multiple-valued logic value.

3. Design of a Multiple-Valued Content-Addressable-Memory Using MFSFETs

CAM accomplishes a magnitude comparison between two kinds of R-valued input words, S(an n-digit external input, word) and B_i(an ith n-digit stored input word), and generates a binary output word, Z(m-bit output) as its comparison result. Figure 8 shows a general structure of an MVCAM. In the case of R-valued encoding, an input word S and the ith stored word B_i are expressed as follows:

$$S = \sum_{j=1}^{n} R^{n-j} \cdot s_j, \tag{1}$$

and

$$B_i = \sum_{j=1}^{n} R^{n-j} \cdot b_{ij} \tag{2}$$

where s_j and $b_{ij}(1 \leq j \leq n)$ indicate the jth digits of S and B_i, respectively: and $s_j, b_{ij} \in \{0, 1, \cdots, R-1\}$. s_1 and b_{i1} are the most significant digits, and s_n and b_{in} are the least significant digits, respectively. The magnitude compassion between S and B_i is defined as

$$G(S, B_i) = \begin{cases} 1 & \text{if } S > B_i, \\ 0 & \text{otherwise.} \end{cases} \tag{3}$$

The ith binary value z_i in Z is equal to $G(S, B_i)$.

In the following subsection, we discuss about a hardware algorithm of the magnitude comparison: and a circuit design for a high-performance MVCAM using MFSFETs.

3.1 Hardware algorithm

The magnitude comparison G(S. B_i) is represented by two kinds of threshold operations for each digit. One is the greater-than search operation, g_j, and the other

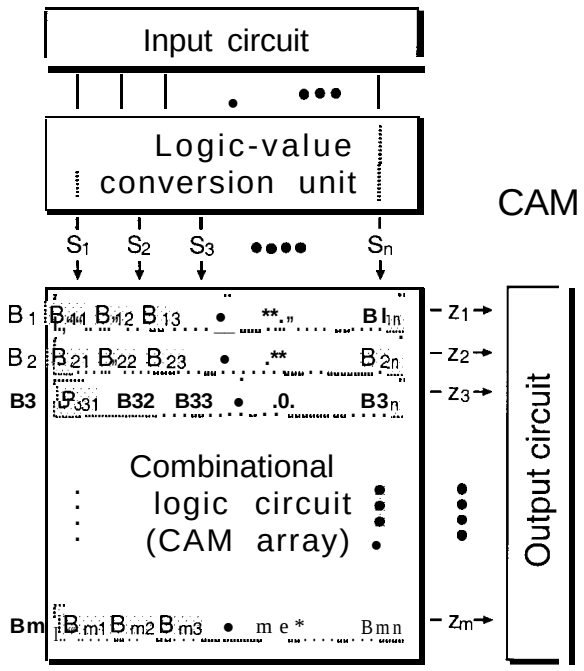

Figure 8. Structure of a CAM.

is the greater-than or equal-to search operation ge_j, between s_j and b_{ij}. These operations are defined as

$$g_j(s_j, b_{ij}) = \begin{cases} 1 & \text{if } s_j > b_{ij}, \\ 0 & \text{otherwise,} \end{cases} \quad (4)$$

and

$$ge_j(s_j, b_{ij}) = \begin{cases} 1 & \text{if } s_j \geq b_{ij}, \\ 0 & \text{otherwise.} \end{cases} \quad (5)$$

For example: let's consider the magnitude comparison between four-valued three-digit words, S and B, as

$$S = (s_1 s_2 s_3) = (321):$$
$$B = (b_1 b_2 b_3) = (320).$$

If B is greater than S, then one of the following conditions:

$$(a)\ g_1 = 1,$$
$$(b)\ ge_1 \text{ A } g_2 = 1,$$
$$\text{and } (c)\ ge_1 \text{ A } ge_2 \text{ A } g_3 = 1$$

must he at least satisfied. In this example:, the above condition (c) is satisfied because of $(s_1 = b_1), (s_2 = b_2)$ and $(s_3 < b_3)$.

In general, the magnitude comparison between n-digit words can be represented by using g_j and ge_j as

$$G(S, B_i) = g_1 \text{ V } (ge_1 \text{ A } g_2) \text{ V } (ge_1 \text{ A } ge_2 \text{ A } ge_3) \ldots \cdot\cdot \text{ V } (ge_1 \text{ A } ge_2 \text{ A} \ldots \text{ A } ge_{n-1} \text{ A } g_n). \quad (6)$$

where symbols **V** and **A** indicate binary logic operations: OR and AND, respectively. Eq.(6) is also transformed into

$$G(S, B_i) = g_1 \vee ge_1 \wedge (g_2 \vee ge_2 \wedge (\cdots \ldots (g_{n-1} \text{ V } ge_{n-1} \text{ A } g_n) \cdot\cdot)). \quad (7)$$

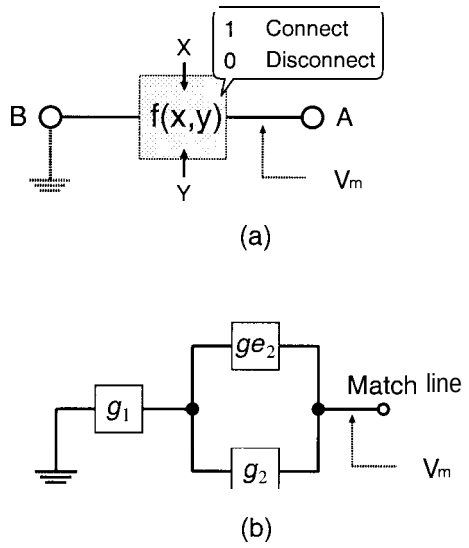

Figure 9. MFSFET-based pass gate, (a)Model, (b)Example.

We use a pass-transistor network[4],[5] to design the CAM circuit based on Eq.(7). In this concept: a function $f(x,y)$ which has two kinds of R-valued inputs x, y, and binary output are considered as a pass gate as shown in Figure 9(a). This pass gate is defined as

$$f(x, y) = \begin{cases} 1 & \text{A is connected to B,} \\ 0 & \text{otherwise.} \end{cases} \quad (8)$$

The result of $f(x, y)$ is obtained by the voltage of A which is precharged to V_m before operation. Where, B is connected to the ground level. The voltage of A depends on the result of $f(x,y)$. That is, the ML is discharged if $f(x, y)$ results in "1". Otherwise: the pass to discharge is broken and the A still remains V_m.

Two binary logic operators. AND and OR, can be easily realized by parallel and serial connections of pass gates. Figure 9(b) shows one example of realization of g_1 A ge_2 **V** g_2 using pass-gates which correspond to g_1, ge_2, and g_2, respectively. Consequently! $G(S, B_i)$ in Eq.(7) is realized by combination of gates. Figure 10 shows a block diagram of the MVCAM word circuit: in which an MVCAM cell consists of pass gates which correspond to g_j and ge_j, respectively.

3.2 CAM cell circuit design using MFSFETs

Two kinds of pass gates, g_j and ge_j, can be designed using threshold operations[10] between the threshold

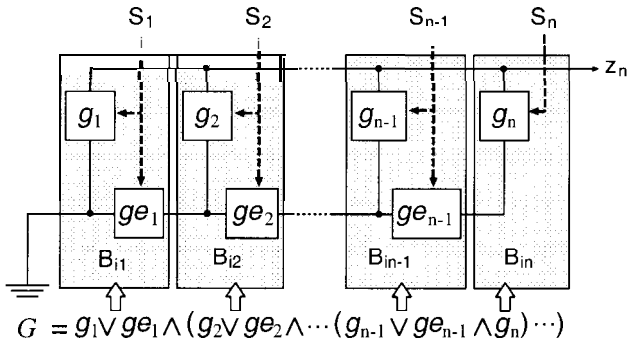

Figure 10. Block diagram of an MVCAM word circuit,.

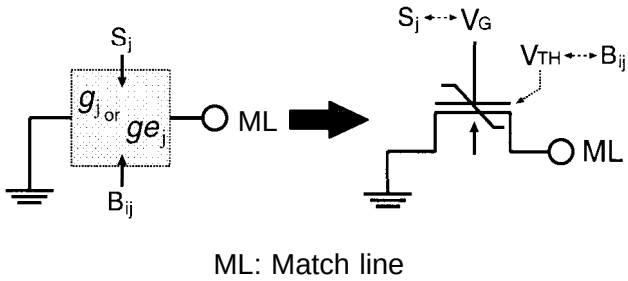

Figure 11. Realization of g_j and ge_j using MFSFETs

voltage V_{TH} and the gate voltage V_G of an MFSFET. The threshold voltage of the MFSFET represents the storage data. This means that the MFSFET can be considered to a pass gate which has two kinds of input V_G and V_{TH}, described in section 3.1. An external input s_i and a stored input b_{ij} correspond to V_G and V_{TH} as shown in Figure 11, respectively.

The function which is represented by the pass gate which consists of an MFSFET is determined by relationship between s_i and b_{ij} (that is, V_G and V_{TH}). Figure 12 shows relationship of the gate and threshold voltage which represents s_i and b_{ij} with regard of g_j and ge_j in the case of four-valued logic. Using this MFSFET, the CAM can be simply designed.

3.3 Overall structure of an MVCAM

Figure 13 shows the circuit diagram of a magnitude comparator between n-digit words. In this circuit,, precharge-evaluate logic is employed to provide low power dissipation and high speed processing with less area overhead. When the clock ϕ is in a low state, the match line is precharged to V_m. When ϕ goes to a high state. the match line is discharged depending on the relationship between S and B_i. Data input, for each cells are performed in parallel, and result of comparison are generated to z_i, simultaneously. Hence: this MVCAM accomplishes a read scheme in one step.

Figure 14 shows circuit diagrams for write opera-

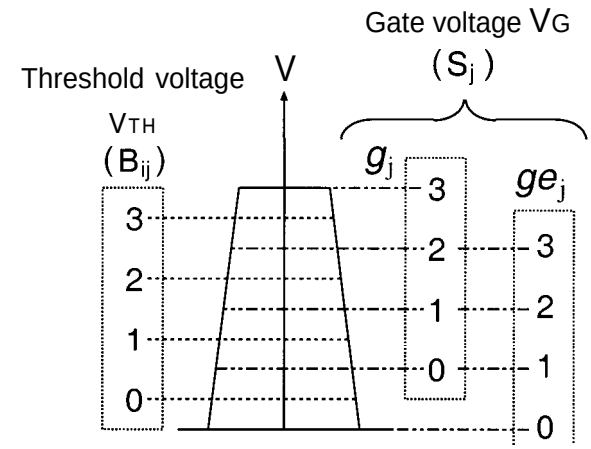

Figure 12. Four-valued threshold voltages and gate voltages of MFSFETs.

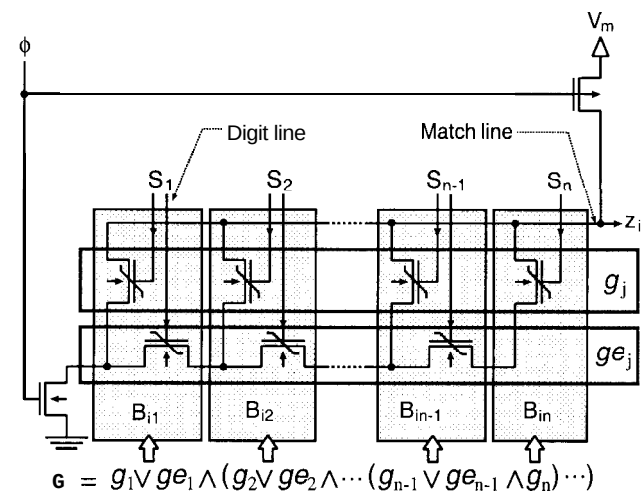

Figure 13. n-digit magnitude comparator based on a digit-parallel structure.

tions in the magnitude comparator. To discharge V_d and V_s for each MFSFETs, the voltage "3" is applied to MFSFETs which correspond to g_j. Then, the threshold voltage V_{TH} is programmed by V_g and V, as shown in Figure 7. To avoid changing the threshold voltage of every non-selected MFSFETs, the digit line or the plate line which connects with those MFSFETs maintains floating.

Table 1 summarizes an estimated performance of CAMs. MFSFETs can realize real-time programmable and non-volatile memories with a non-destructive read scheme, so that the data does not require a reprogram scheme. Therefore: its peripheral circuit for a reprogram operation can be reduced. Moreover, since an MFSFET can perform a threshold operation between V_G and V_{TH} which correspond to s_j and b_{ij}, respectively, a CAM cell is designed by two MFSFETs

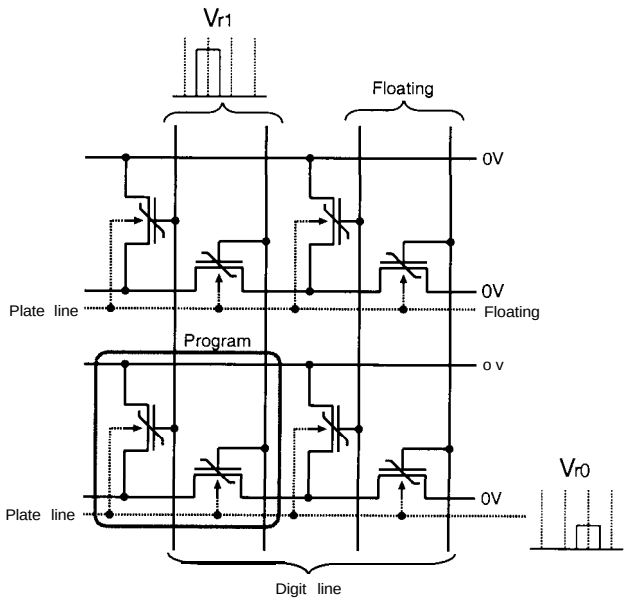

Figure 14. Write operation in a digit-parallel structure.

based on pass-transistor network. Consequently, the presented MVCAM can achieve the high-speed access scheme and high density .

4. Conclusion

A compact MVCAM with real-time programmability has been designed by using MFSFETs. Since a multiple-valued threshold operation is performed by using a single MFSFET whose multi-level threshold voltages correspond to remnant polarization states, a multiple-valued one-digit comparator can be designed by just two MFSFETs. Moreover. the use of the pre-charge-evaluate logic circuit makes an MVCAM word circuit compact,.

As a future research target,. it is also important, to develop high-performance VLSI circuit, with multiple-valued external inputs, multiple-valued stored inputs and binary outputs using MFSFETs.

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Table 1. Comparison of CAMs.

CAM	Type	Non-volatile	Real-time Programm-ability	Bit-density	Speed/bit	Peripheral Circuit Simplicity
Dynamic [2]	Binary	No	Yes	+	+	+
Floating-gate MOS Tr. based [3]	Binary	Yes	No	++	+	+
Floating-gate MOS Tr. based [5]	Multiple-valued	Yes	No	+++	+++	++
FE capacitor based [6]	Multiple-valued	Yes	Yes	+++	++	+
MFSFET based Digit-parallel	Multiple-valued	Yes	Yes	+++	+++	++