Multiple-valued logic-in-memory VLSI based on a floating-gate-MOS pass-transistor network

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FP 12.5: Multiple-Valued Logic-in-Memory VLSI Based on a Floating-Gate-MOS Pass-Transistor Network

T. Hanyu, K. Teranishi, M. Kameyama

Tohoku University, Sendai, Japan

A logic-in-memory structure, in which storage functions are distributed over a logic-circuit plane, is a solution to the communication bottleneck between memory and logic modules, one of the most serious problems in recent deep submicron VLSI systems.technology [1]. This logic-in-memory VLSI based on floating-gate MOS transistors merges storage and switching functions in a multiple-valued-input and binary-output combinational logic circuit that is useful for the realization of parallel arithmetic and logic circuits. Figure 1 shows a general structure of a 4-valued-input and binary-output combinational logic circuit. It has two kinds of inputs, external and stored constant inputs. In the logic-in-memory VLSI, a large number of stored data are distributed in not only word-parallel but also in digit-parallel manners.

Figure 2 shows a 4-valued-input binary-output pass-transistor network based on floating-gate MOS transistors. Four basic operations such as AND (serial connection of pass transistors), OR (parallel connection of pass transistors), a threshold literal (TL) and logic-value conversion (LVC) are used to represent arbitrary switching functions where these operations are defined in Figure 2a. Multiple-valued stored data are represented by the threshold voltage of a floating-gate MOS transistor, so that both multiple-valued threshold-literal and pass-switch functions can be merged by using a single floating-gate MOS transistor as shown in Figure 2b. Consequently, a compact pass-transistor network can be designed by using floating-gate MOS transistors as shown in Figure 2c.

A fully-parallel magnitude comparator between 4-valued external and stored data is a typical application of the logic-in-memory VLSI. Figure 3a shows the definition of TLs, g_j and ge_j. The TL and pass-switch functions are merged in a pass-transistor network where the merged pass switch is defined as shown in Figure 3b. Since 4-valued stored data are represented by the threshold voltage of the floating-gate MOS transistor, memory is by storing 4-level charge on the floating gate of the transistor. As a result, a pass switch with a 4-valued TL function uses only a single floating-gate MOS transistor where 4-valued external-input and stored constant-input data are represented by a gate voltage and a threshold voltage as shown in Table 1.

Figure 4a shows a magnitude comparison between 4-valued 3-digit words, $(s_1\ s_2\ s_3)$ and $(b_1\ b_2\ b_3)$, given by radix-4 number representation. According to the definition of a 4-valued pass switch shown in Figure 3c, a pass-transistor network for the magnitude comparison can be designed as shown in Figures 4b and 4c. To perform the pass-switch operation, the precharge-control and evaluate-control transistors are added as shown in Figure 4c. Two kinds of pass-switch operations for each input digit are realized by two different floating-gate MOS transistors, so that a general structure in case of n-digit word length can be designed by $(2n+1)$ transistors as shown in Figure 4d.

Figure 5 shows layout and circuit diagrams of the pass-transistor network with 4 floating-gate MOS transistors in a 0.8μm double-metal double-polysilicon EEPROM technology. Although the pass-transistor network is constructed by the mixture of serial and parallel connections of floating-gate MOS transistors, there is no hardware overhead in terms of interconnection area. Figure 6 shows a layout of the proposed logic-in-memory VLSI chip for 4-valued 16-digit magnitude comparison under the same process technology. Features are summarized in Table 2.

Table 3 shows the PSPICE simulation of the proposed logic-in-memory using a standard 0.8μm EEPROM technology. The number of execution steps is greatly reduced in the proposed logic-in-memory VLSI by the pass-transistor network, because highly parallel logic operations and storage functions are merged in the pass-transistor network. As a result, the execution speed of the proposed logic-in-memory VLSI is about 26 times and 6 times higher than those of both binary-CAM-based and conventional multiple-valued CAM-based implementations, respectively [2, 3]. The advantage of the number of execution steps also reduces power dissipation of the proposed logic-in-memory in comparison with that of other implementations because its precharge is only once for each execution cycle. Power dissipation of the logic-in-memory VLSI is reduced to about 21% and 24% of those of a binary CAM-based and conventional multiple-valued CAM-based implementations, respectively. The use of a floating-gate MOS transistor makes the area penalty of the pass-transistor circuit smaller.

References:

[1] Kautz, W., "Cellular Logic-in-Memory Arrays," IEEE Trans. on Computer, C-18, 8, pp.719—727, Aug., 1969.

[2] Yamagata,T., et al.,"A 288-kb Fully Parallel Content Addressable Memory Using a Stacked-Capacitor Cell Structure," IEEE J.Solid-State Circuits, SC-27, 12, pp.1927-1933, Dec., 1992.

[3] Hanyu, T., N. Kanagawa, M. Kameyama, "Design of a One-Transistor-Cell Multiple-Valued CAM," IEEE J.Solid-State Circuits, SC-31, 11, pp.1669—1674, Nov., 1996.

Logic value of input data	0	1	2	3	4
Gate voltage Vx	0.00V	1.25V	2.50V	3.75V	5.00V

Logic value of stored data	0	1	2	3
Threshold voltage Vt	0.63V	1.88V	3.13V	4.38V

Table 1: Voltages corresponding to 4-valued logic levels.

Technology	0.8- μm EEPROM double-metal double-polysilicon
Number of words	32,768-word
Capcity	1Mb
Chip size	50mm²
Power supply voltage	5 V
Execution time	50ns

Table 2: Features of a 4-valued logic-in-memory VLSI chip.

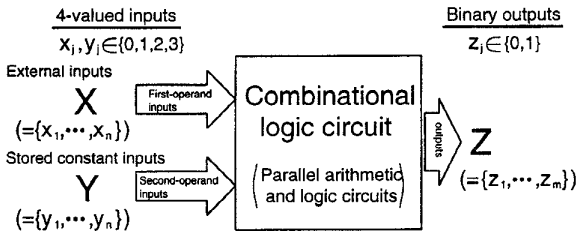

Figure 1: General structure.

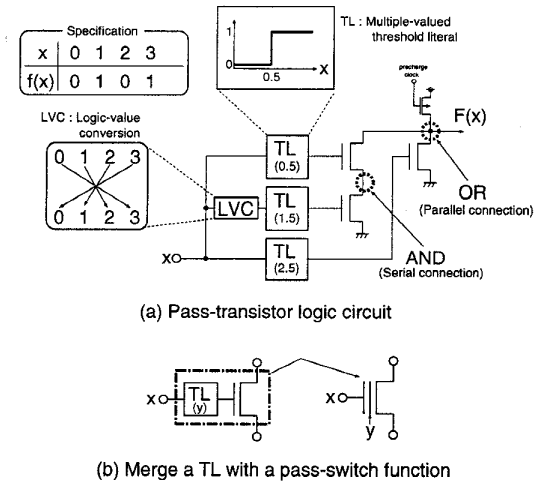

Figure 2: Design example.

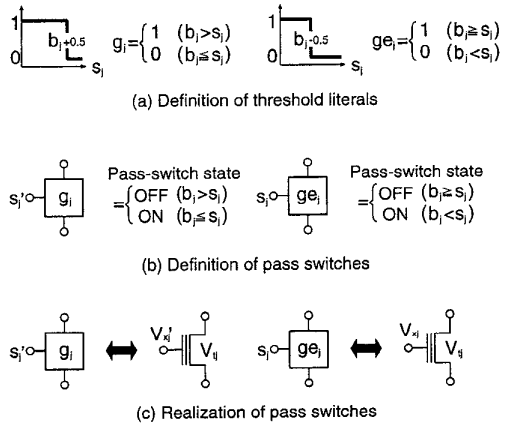

Figure 3: Floating-gate-MOS pass-transistor.

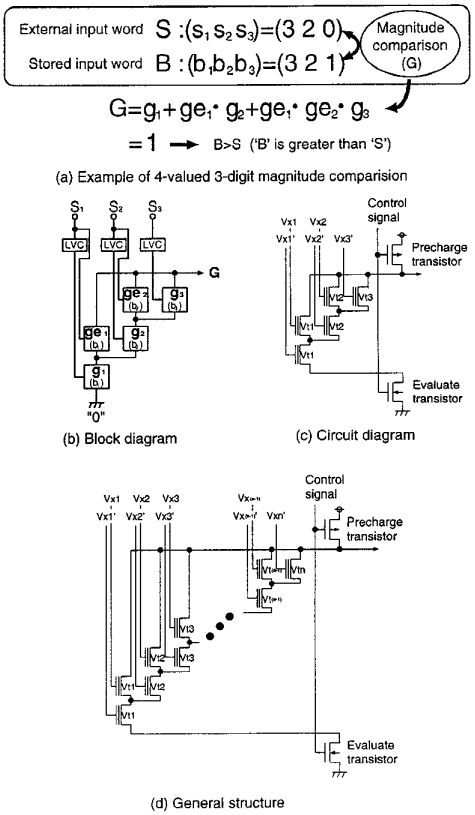

Figure 4: Magnitude comparator word circuit.

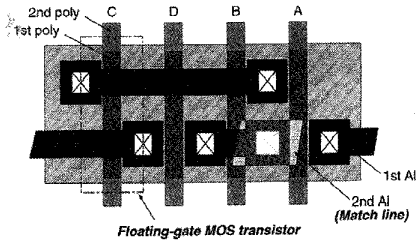

Figure 5: Floating-gate-MOS pass-transistor network.

Table 3 and Figure 6: See page 437.

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	Binary CAM	4-valued implementation	
		CAM	Proposed
Area/2bit	132μm²	21μm²	56μm²
Processing time /step	40nsec	20nsec	50nsec
No. of Execution steps	32	16	1
Execution time	1280nsec	320nsec	50nsec
Power dissipation /word	0.86mW	0.75mW	0.18mW

(PSPICE simulation based on a 0.8-μm EEPROM technology)

Table 3: Comparison of performances (32b 256 words).

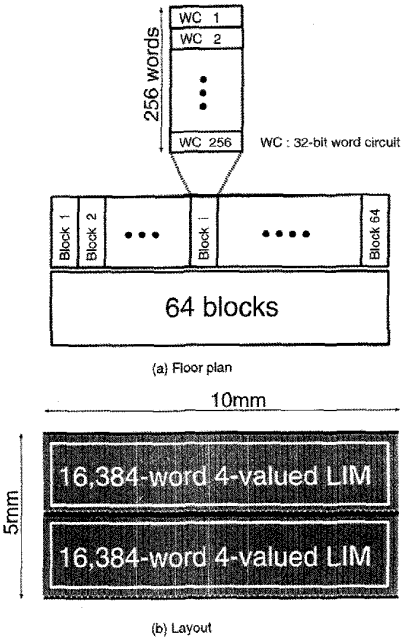

Figure 6: 4-valued logic-in-memory (LIM) VLSI chip.

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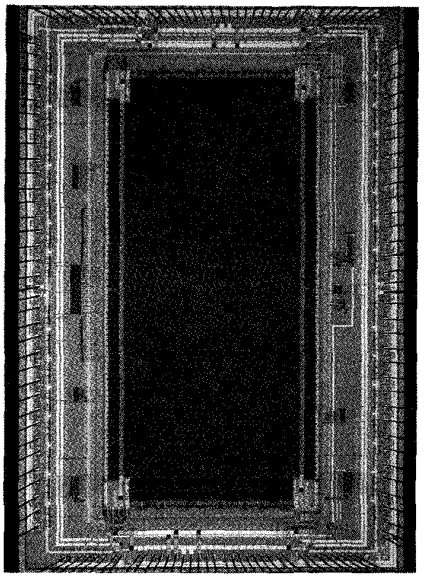

Figure 1: Chip micrograph.