Fully Source-Coupled Logic Based Multiple-Valued VLSI

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Abstract

A novel source-coupled logic (SCL) style using multiple-valued signals, called multiple-valued source-coupled logic (MVSCL), which operates with an input voltage swing of about 0.3V, is proposed for high-speed and low-power VLSI systems. A multiple-valued comparator, which is a key component, is realized by using differential-pair circuits (DPCs), so that its power dissipation can be greatly reduced while maintaining high-speed switching. Moreover, the current-source control allows steady current flow to cut off when the circuit is not active, thereby saving power dissipation. A 54×54-bit signed-digit multiplier based on MVSCL is designed in a 0.35-µm CMOS technology, and its performance is superior to both corresponding binary static CMOS and multiple-valued current-mode (MVCM) implementation.

1. Introduction

In the recent deep-submicron VLSI era, low-power circuit design while maintaining a high-speed switching capability at a small signal voltage swing is needed not only for battery-powered portable applications, but also to reduce the power dissipation of dedicated special-purpose VLSI processors because the extra current density in wires causes temporal or permanent malfunction due to voltage drops or electromigration [1]-[5].

A differential-pair circuit (DPC) is one of the most effective circuit technologies to reduce a signal voltage swing with maintaining high current-driving capability. In fact, DPC-based binary logic circuits have been proposed for high-speed operation with small signal voltage swing [6], [7]. However, the number of transistors required for DPC-based binary logic circuits becomes twice as many as that of a corresponding binary static CMOS realization, because pair of complementary voltage inputs together with complementary input-driving circuits are required for switching.

Since the number of basic components and associated transistor counts can be generally reduced in multiple-valued logic (MVL) circuits, it is possible that a judicious combination of DPC and MVL will make it possible to perform high-speed operations with reduced device and interconnect counts at low-power dissipation. Using partially DPC-based basic components, we have developed a dual-rail multiple-valued current-mode (MVCM) circuit, and its performance is superior to binary static CMOS circuit with almost the same transistor counts [8], [9]. However, the use of current comparator increases power dissipation due to the large steady current.

This paper presents the design and the implementation of a novel multiple-valued logic circuit called "multiple-valued source-coupled logic (MVSCL) circuit" for high-performance arithmetic in VLSI systems. In MVSCL integrated circuits, a DPC-based voltage comparator is used and operates with small signal voltage swing, so that low-power operation can be realized while maintaining high-speed switching. Moreover, controlling the gate voltages of current sources and current-to-voltage converters, the steady current flowing through inactive circuits can be cut off while maintaining short critical path.

As a typical application to arithmetic and logic VLSI systems, an MVSCL multiplier based on radix-2 signed-digit (SD) addition algorithm is designed. It is demonstrated that the power dissipation of the proposed multiplier is reduced to 69% of that of a dual-rail MVCM implementation under the normalized switching delay. Moreover, a prototype CMOS integrated circuit for the proposed circuit is fabricated in a 0.35-µm standard CMOS technology, and its basic operation is confirmed.

2. Principle of MVSCL Integrated Circuits

2.1 Basic components

Figure 1 shows the general structure of the MVSCL circuit which consists of three basic components.

1) *Linear summation circuit:* Using multiple-valued

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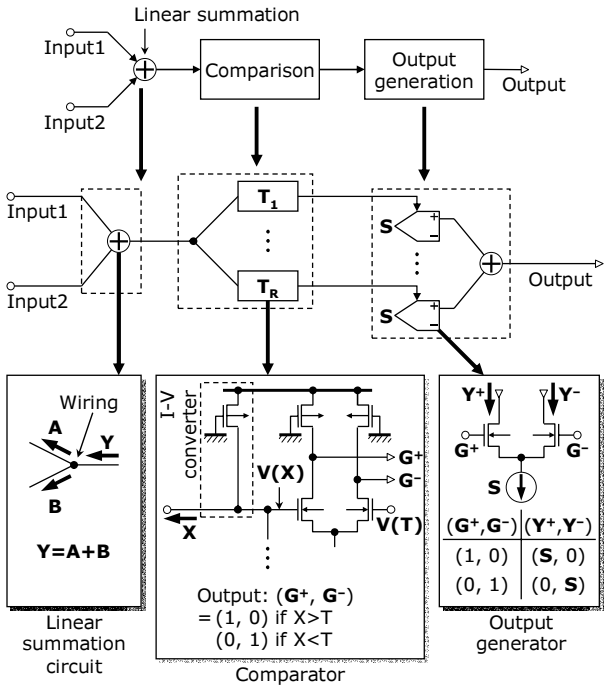
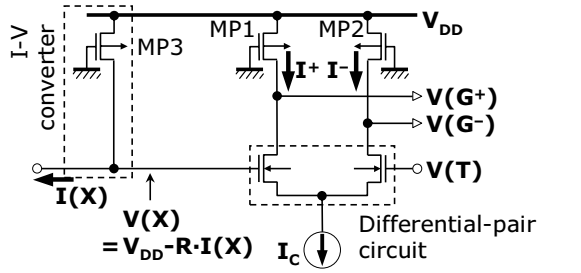


Figure 1. Basic components



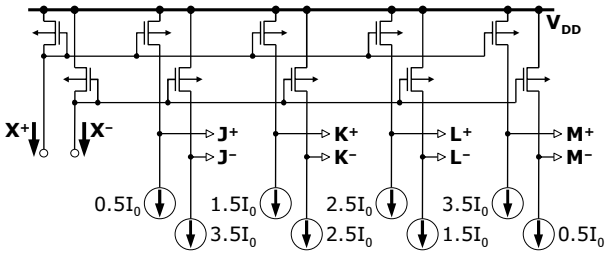
X	V(X)	I+	I-	V(G+)	V(G-)	(G+, G-)
>T	<V(T)	0	I_C	V_{DD}	V_{DD}-R_C·I_C	(1, 0)
<T	>V(T)	I_C	0	V_{DD}-R_C·I_C	V_{DD}	(0, 1)

Figure 2. Multiple-valued voltage-mode comparator

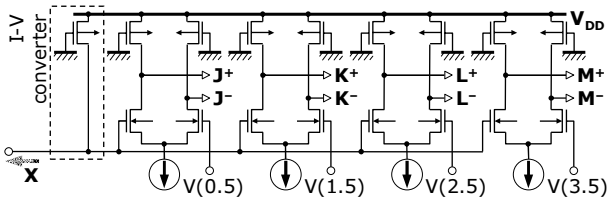
current signals, arithmetic summation can be performed by wiring without active devices, so that the resulting arithmetic circuits become simple.

2) *Comparator:* A comparator is to compare an input value X with a threshold value T, and to generate binary differential-pair outputs (G^+, G^-).
3) *Output generator:* An output generator is to generate multiple-valued differential-pair outputs (Y^+, Y^-) in accordance with binary differential-pair inputs (G^+, G^-) where its function is defined in Figure 1.

The logic functions of these components are the same



(a) Dual-rail MVCM comparator



(b) Proposed comparator

Figure 3. 5-valued comparators

Table 1. Comparison of 5-valued comparators

	Dual-rail MVCM	MVSCL
Supply voltage	1.0 V	3.3 V
Delay	620 ps	620 ps
Power dissipation	496 µW	256 µW

HSPICE simulation under
a 0.35-µm standard CMOS technology

as those of dual-rail MVCM logic circuits. On the other hand, in dual-rail MVCM logic circuits, the comparator compares the input current signal directly with the threshold current level, which causes large power dissipation. Consequently, it is important to develop a new low-power comparator.

2.2 Multiple-valued voltage-mode comparator

Figure 2 shows the principle underlying low-power operation in a multiple-valued voltage-mode comparator. In R-valued comparators, the current I(X), corresponding to the multiple-valued input X, is described as

$$\begin{cases} I(X) = X \cdot I_0 \\ 0 \le X \le R-1 \end{cases} \quad (1)$$

where I_0 is the unit current. Since the pMOS transistor MP3 always operates in the linear region, I(X) is converted into the voltage V(X) as follows:

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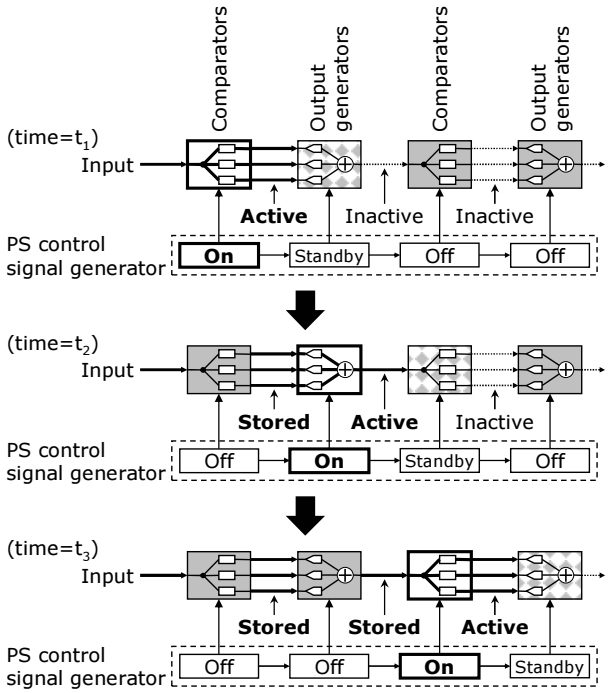

Figure 4. Current source control in the proposed circuit

$$\begin{cases} V(X) = k - \sqrt{k^2 - \frac{2}{\beta} \cdot I(X)} \\ k = V_{DD} - V_T \end{cases} \quad (2)$$

where V_T, β, and V_{DD} are the threshold voltage of MP3, the gain constant of MP3 and the supply voltage of the comparator, respectively.

When the supply voltage of the MVSCL circuit is 3.3V, the minimum voltage swing to be detected is about 0.3V. A differential-pair circuit (DPC) is useful for the detection of such small voltage. A DPC is to compare V(X) and V(T), and generates the binary output currents, I^+ and I^-, where V(T) is the voltage corresponding to T. The output currents are converted into binary voltages by the pMOS transistors MP1 and MP2, thereby results in the binary output voltages $V(G^+)$ and $V(G^-)$.

Table 1 summarizes the comparison between the proposed 5-valued comparator and the corresponding dual-rail MVCM comparator shown in Figure 3. The supply voltage of the dual-rail MVCM comparator is smaller than that of the proposed comparator, however the average of the steady current is over $10I_0$, where I_0 is about 40μA, so that it causes large power dissipation. In the proposed voltage-mode comparator, the total amount of steady current is $4I_C$, where I_C is about 20μA, so that the power dissipation of the proposed comparator can be reduced to about 51% in comparison with that of the corresponding dual-rail MVCM one.

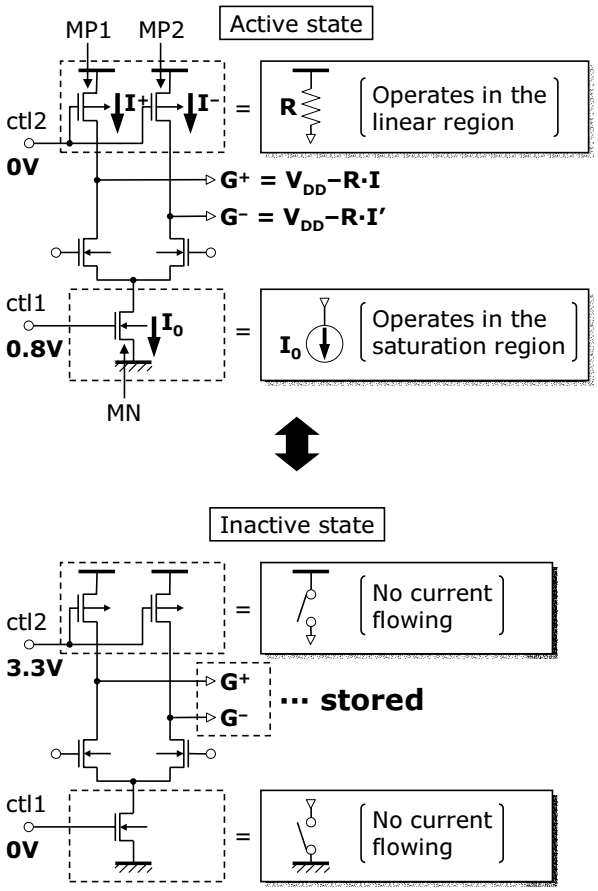

Figure 5. Circuit diagram of the proposed current source control

2.3 Low-power circuit design using current-source control

Figure 4 shows the current-source control scheme of the proposed MVSCL circuit. To reduce the power dissipation, the current of inactive components is cut off, which greatly reduces the power dissipation with maintaining high-speed operation [10].

Figure 5 shows the principle of current-source control for MVSCL circuits without additional active devices. When the component is active, the transistors MP1 and MP2 operate in the linear region and MN operates in the saturation region. When the component is inactive, no current flows through MP1, MP2 and MN. The difference between these states is only the gate voltages, ctl1 and ctl2. Consequently, using the above control scheme, the power dissipation of a MVSCL circuit can be greatly reduced without any increased critical path by direct gate-voltage control of the current source.

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Table 2. Current level

Logic value	–2	–1	0	1	2
X(i), Y(i), W(i), C(i), S(i)	—	0	I_0	$2I_0$	—
Z(i)	0	I_0	$2I_0$	$3I_0$	$4I_0$

(I_0: Unit current)

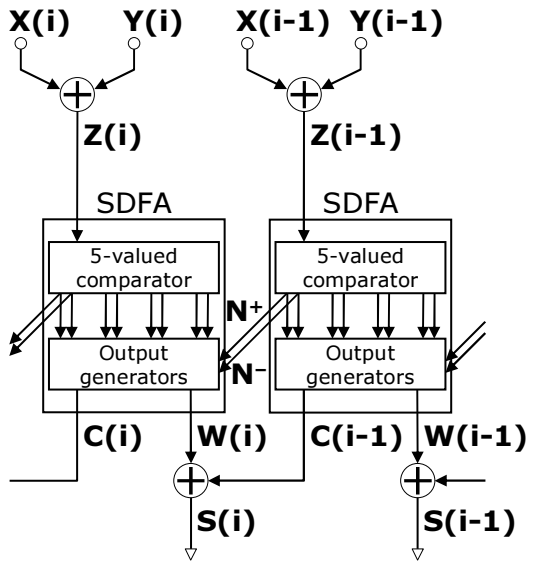

Figure 6. Radix-2 SD adder

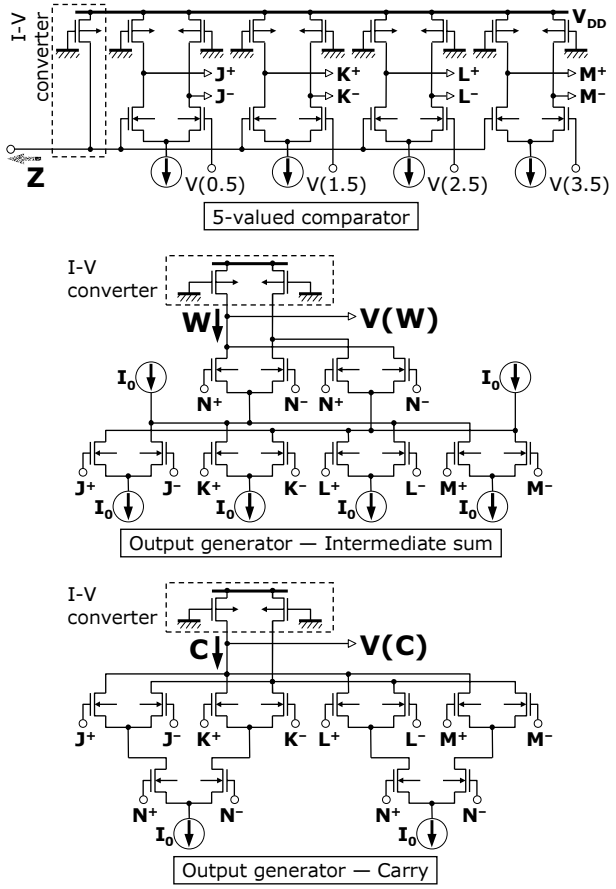

Figure 7. Circuit diagram of the proposed SDFA

3. Design of a Multiplier Based on Multiple-Valued Source-Coupled Logic

3.1 Radix-2 SD addition algorithm

The radix-2 SD number representation using a symmetrical digit set {–1, 0, 1} is defined as follows:

$$\mathbf{X} = (X(n-1)\cdots X(1)\,X(0)) = \sum_{i=0}^{n-1} X(i)\cdot 2^i \qquad (3)$$

where $X(i) \in \{-1, 0, 1\}$. The redundancy allows totally parallel arithmetic operations. The addition of two numbers, $\mathbf{X} = (X(n-1)\cdots X(1)X(0))$ and $\mathbf{Y} = (Y(n-1)\cdots Y(1)Y(0))$ is performed by three successive steps in each digit as

$$Z(i) = X(i) + Y(i) \qquad (4)$$

$$2C(i) + W(i) = Z(i) \qquad (5)$$

$$S(i) = W(i) + C(i-1) \qquad (6)$$

where the arithmetic sum $\mathbf{Z} = (Z(n-1)\cdots Z(1)Z(0))$, the intermediate sum $\mathbf{W} = (W(n-1)\cdots W(1)W(0))$, the carry $\mathbf{C} = (C(n-1)\cdots C(1)C(0))$ and the final sum $\mathbf{S} = (S(n)\cdots S(1)S(0))$ are $Z(i) \in \{-2, -1, 0, 1, 2\}$, $W(i) \in \{-1, 0, 1\}$, $C(i) \in \{-1, 0, 1\}$ and $S(i) \in \{-1, 0, 1\}$, respectively.

To retain the final sum S(i) within the set {–1, 0, 1}, C(i) and W(i) are determined by Z(i–1) together with Z(i) as follows:

$$\begin{cases} C(i)=1,\ W(i)=0 & \text{if } Z(i)=2 \\ C(i)=1,\ W(i)=-1 & \text{if } Z(i)=1 \text{ and } Z(i-1)\geq 1 \\ C(i)=0,\ W(i)=1 & \text{if } Z(i)=1 \text{ and } Z(i-1)<1 \\ C(i)=0,\ W(i)=0 & \text{if } Z(i)=0 \\ C(i)=0,\ W(i)=-1 & \text{if } Z(i)=-1 \text{ and } Z(i-1)\geq 1 \\ C(i)=-1,\ W(i)=1 & \text{if } Z(i)=-1 \text{ and } Z(i-1)<1 \\ C(i)=-1,\ W(i)=0 & \text{if } Z(i)=-2. \end{cases} \qquad (7)$$

The final sum is independent of the word length n because the carry-propagation chain is limited to one digit to left. Therefore the addition speed of the SD adder is higher than that of ordinary binary adders [11].

3.2 Design of an SD multiplier

In the proposed MVSCL circuits, each digit of the SD

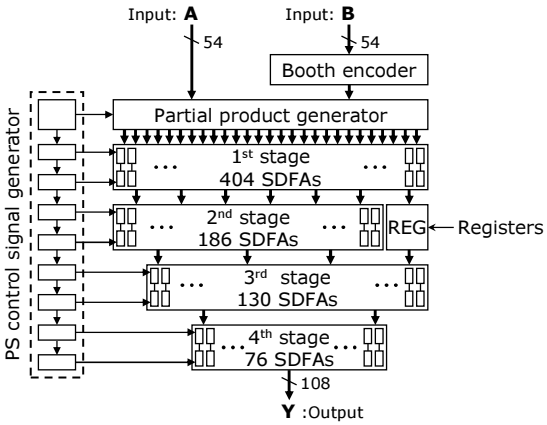

Figure 8. Block diagram of the proposed 54×54-bit multiplier

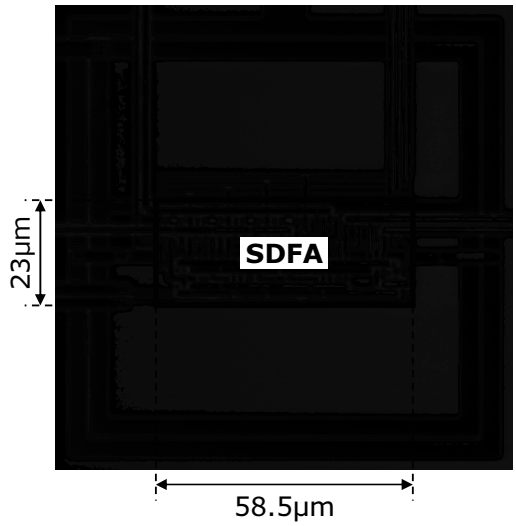

Figure 9. Chip photomicrograph

numbers corresponds to a multiple-valued current signal. Two adder inputs, the linear sum of two inputs, the intermediate sum, the carry and the final sum are represented as X(i), Y(i), Z(i), W(i), C(i) and S(i), respectively, whose current levels are given in Table 2.

The radix-2 SD adder can be designed as shown in Figure 6. The linear summation of (4) and (6) can be obtained by wiring without active devices. The operation of (5) is performed with an SD full adder (SDFA). The signals N^+ and N^- are used as the control signals to give the condition of $Z(i-1) \geq 1$ and $Z(i-1) < 1$ in (7). The linear sum Z(i) takes 5 values and decoded by a 5-valued voltage comparator. As a result, the SDFA circuit can be designed using 54 MOS transistors as shown in Figure 7.

A low-power multiple-valued multiplier is designed

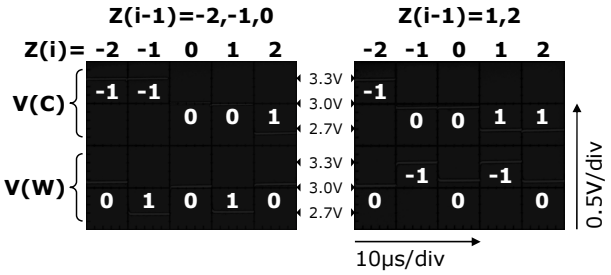

Figure 10. Measured waveforms

Table 3. Comparison of multipliers

	Binary static CMOS	Dual-rail MVCM	MVSCL
Supply voltage(s)	2.8 V	1.8 V, 1.0 V	3.3 V
Delay	7.64 ns	6.24 ns	6.24 ns
Power dissipation	106 mW	153 mW	106 mW
Area	5.32 mm^2	—	4.99 mm^2

HSPICE simulation under
a 0.35-μm standard CMOS technology

using the SDFAs as shown in Figure 8. Using the Booth algorithm, 27 partial products for 54-bit multiplication are generated from the partial product generator. Since SD addition can be performed by a binary-adder-tree scheme, 27 partial products are added in parallel by just four addition stages. Because of the proposed switched-current control scheme, only one of nine divided stages in the multiplier is controlled to be active.

4. Evaluation

4.1 Implementation of a prototype chip

To confirm the operation of the proposed MVSCL circuit, a prototype SDFA circuit is implemented using a 0.35-μm standard CMOS technology as shown in Figure 9. The effective size of the SDFA is 58.5μm × 23μm. The typical transfer characteristics of the SDFA for the case of $-2 \leq Z(i) \leq 2$ are shown in Figure 10.

4.2 Comparison of performance

Table 3 summarizes the comparison of SDFAs in terms of the delay and the power dissipation. The performance is estimated by HSPICE simulation based on a 0.35-μm standard CMOS technology. Using DPC-based MV

voltage comparators, the power dissipation of the proposed multiplier can be reduced to 69 % of a corresponding MVCM implementation under the condition of the same multiplication time. Moreover, under the same power dissipation, the operating speed of the proposed multiplier is 1.2 times faster than that of a binary CMOS multiplier.

5. Conclusion

The key technologies that realize low-power dissipation as well as high-speed switching have been presented. The use of SCL and MVL style makes the voltage swing for switching small with maintaining small hardware. Moreover, the use of current source control technique makes the waste steady current flow cut off, so that the static power dissipation becomes zero in this circuit. As a typical application to large-scale arithmetic systems, it is demonstrated that the maximum operating delay of the proposed 54×54-bit multiplier is evaluated to be 6.24ns under a 0.35-μm standard CMOS technology, whose performance is superior to that of a corresponding binary static one.

As a future problem, it is also important to save the static power dissipation still more while maintaining high-speed operation. One approach is the use of dynamic logic circuits. In the proposed circuit, the steady current becomes zero by using dynamic logic circuits. If the problem is successfully solved, we may well see an ultra-low-power multiple-valued VLSI chip for ultra-high-speed arithmetic and logic operations.

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