# Dual-Rail Multiple-Valued Current-Mode VLSI with Biasing Current Sources

Tsukasa Ike, Takahiro Hanyu and Michitaka Kameyama
*Department of Computer and Mathematical Sciences,*
*Graduate School of Information Sciences,*
*Tohoku University*
*Aoba-yama 05, Sendai 980-8579, Japan*
*tiles@kameyama.ecei.tohoku.ac.jp*

## Abstract

*A new current mirror with a biasing current source is proposed for high-performance arithmetic VLSI systems. The delay for the current mirror is inversely proportional to the input current. The use of a biasing current source makes the input current of the current mirror increased, which results in smaller switching delay. As a typical example of the proposed dual-rail multiple-valued current mode (MVCM) circuit, a radix-2 signed-digit full adder is designed by using a 0.35-μm CMOS technology. Its performance is superior to that of corresponding MVCM circuits without biasing current sources.*

## 1. Introduction

In the recent deep-submicron VLSI era, low-power circuit design with keeping a high-speed switching capability at a low supply voltage is needed not only for battery-powered portable applications, but also to reduce the power dissipation of dedicated special-purpose VLSI processors because the extra current density in wires may cause temporal or permanent malfunction due to voltage drops or electromigration [1]-[5].

A multiple-valued current-mode (MVCM) integrated circuit based on dual-rail differential logic has a potential advantage to realize a high-speed circuit at a low supply voltage, because the use of a differential-pair circuit (DPC) in a threshold detector, which is a key component of the MVCM circuit, makes a voltage swing small yet driving capability large [6]. Moreover, when several DPCs are not active in the MVCM circuit, the gate voltages of current sources in these corresponding DPCs can be turned off, which makes it possible to achieve a low-power dissipation with keeping a high-speed operation in the MVCM circuit [7].

The performance of the dual-rail MVCM circuit is determined by the performance of two basic components, a threshold detector (TD) and a current mirror. We have proposed a high-speed design of the TD in the previous work [8]. Using two supply voltages, the output voltage swing of comparators are adjusted to the required voltage swing for operating a DPC, which results in a lower power dissipation together with a higher switching speed. However, to achieve higher performance in the dual-rail MVCM circuit, it is also important to achieve higher performance in the current mirror.

In this paper, a new high-speed current mirror is proposed. The delay for the current mirror is inversely proportional to the input current. Hence, the delay under a small input current becomes too large in the conventional current mirror. In the proposed current mirror, a biasing current source is connected to the input node of the current mirror, which makes the input current increased. As a result, the operating speed of the proposed circuit becomes faster than the conventional one.

As a typical example, a signed-digit full adder (SDFA) with biasing current sources and two supply voltages is designed based on a 0.35-μm CMOS technology. As a result, the switching delay and the power dissipation can be reduced to 69% and 70%, respectively, of a corresponding SDFA without these two design methods.

## 2. Principle of a High-Speed Current Mirror with a Biasing Current Source

In this section, we consider the delay of the current mirror as the function of input current, and discuss the optimum design of the current mirror.

### 2.1 Basic components of a dual-rail MVCM VLSI

Figure 1 shows the basic components of the MVCM circuit.

1) *Wired-sum circuit:* In the MVCM circuits, arithmetic summation can be performed by wiring without active devices, so that the resulting arithmetic circuits become simple.

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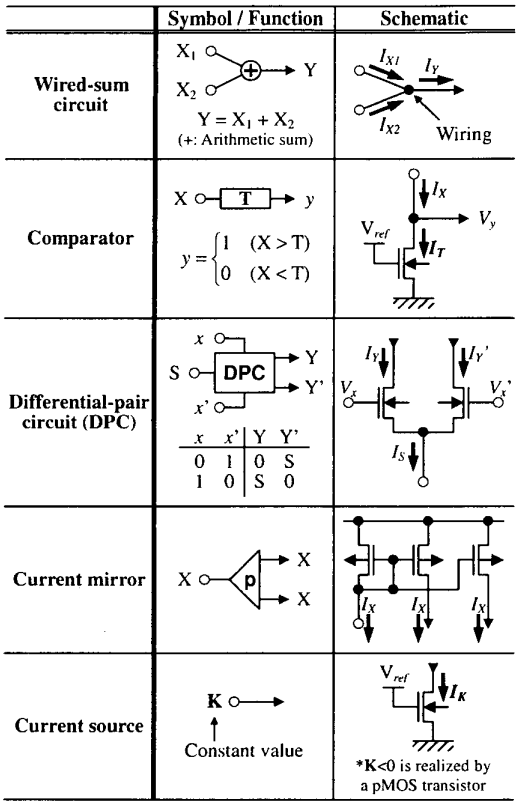



**Figure 1.** MVCM basic components

2) *Comparator:* A comparator is to compare an input current $I_X$ with a threshold current $I_T$, and to generate an output voltage $V_y$.
3) *Differential-pair circuit (DPC):* A DPC is to generate a multiple-valued differential-pair output (0, S) or (S, 0) in accordance with a binary differential-pair input where its function is defined in Figure 1.
4) *Current mirror:* A current mirror produces several replicas of an input current. The current mirror also has the function of inverting the current direction.
5) *Current Source:* A current source can be designed by an enhancement-mode nMOS transistor with the reference voltage $V_{ref}$. The current level is adjusted by the transistor size.

By the combination of these components, we can design high-performance MVCM circuits.

Figure 2 shows a design example of dual-rail MVCM circuits and the graph which shows the operating speed of each basic components. The delay for a wired-sum circuit

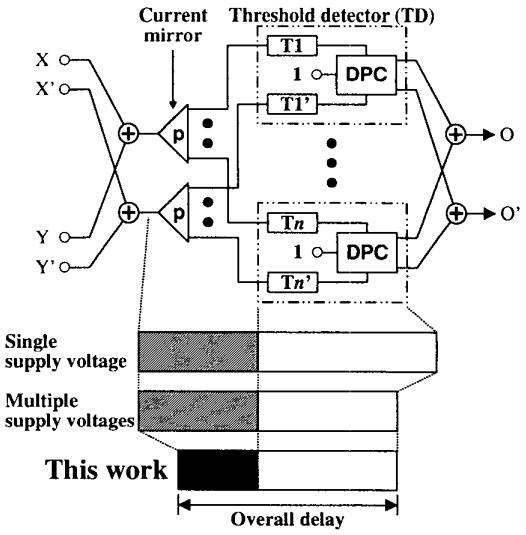



**Figure 2.** Switching delay in the series connection of the dual-rail MVCM circuit

is very small because wired-sum circuits consist of no active devices. Consequently, the operating speed of the dual-rail MVCM circuit is determined by the operating speed of a TD, which consists of two comparators and a DPC, and the current mirror. In the previous work, we proposed a high performance design of a TD, which results in a lower power dissipation together with a higher switching speed.

To achieve higher performance in dual-rail MVCM circuits, it is also important to achieve higher performance in current mirrors. In the following section, we discuss about a high-speed design of current mirrors.

## 2.2 Design of a high-speed current mirror using biasing current sources

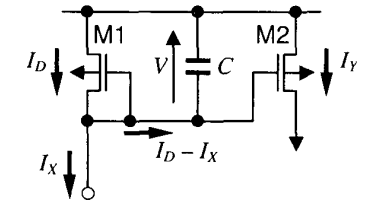
Figure 3(a) shows the schematic of the current mirror. In the $R$-valued MVCM circuit, the minimum and the maximum value of the input current $I_X$ are described as

$$I_{MIN} = 0 \quad (1)$$

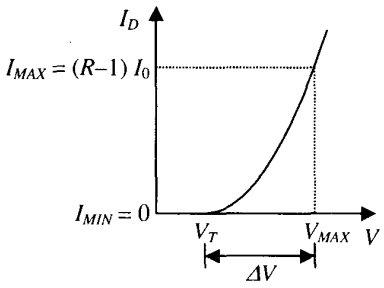
$$\text{and } I_{MAX} = (R - 1)\, I_0, \quad (2)$$

respectively, where $I_0$ is the unit current. The load capacitance $C$ is given by the sum of the gate capacitance of the pMOS transistor M1 and M2. The delay for the current mirror $t_{CM}$ is determined by the charge (or discharge) time for the load capacitance $C$ as follows:

$$t_{CM} \propto C \frac{V_{MAX} - V_{MIN}}{|I_D - I_X|}, \quad (3)$$

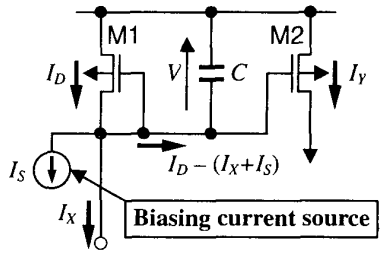



(a) Schematic

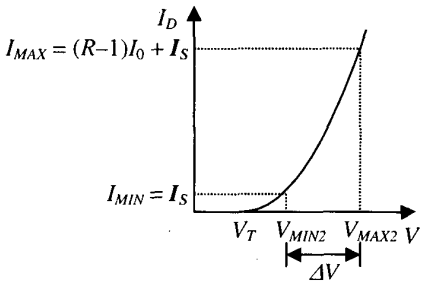



(b) $V$–$I_D$ characteristic

**Figure 3.** Conventional current mirror




(a) Schematic




(b) $V$–$I_D$ characteristic

**Figure 4.** Proposed current mirror

$$| I_D - I_X | \propto I_0 \tag{4}$$

where $V_{MAX}$ and $V_{MIN}$ are the voltage $V$ of the load capacitance $C$ when the input current $I_X$ is $I_{MAX}$ and $I_{MIN}$, respectively. By Eqs. (3) and (4), we can get the equation as follows:

$$t_{CM} \propto C\frac{\Delta V}{I_0}, \tag{5}$$

$$\Delta V = V_{MAX} - V_{MIN}. \tag{6}$$

By Eq. (5), to reduce the switching delay for the current mirror, it is important to reduce the voltage swing $\Delta V$ without reducing the unit current $I_0$.

Figure 3(b) shows the $V$–$I_D$ characteristic of Figure 3(a). Since the transistor M1 always operates in the saturation region, the drain current $I_D$ of the transistor M1 is described as

$$I_D = \frac{\beta}{2}(V - V_T)^2 \tag{7}$$

where $\beta$ is a gain constant of the transistor M1. Using Eq. (7), the voltage swing $\Delta V$ of the load capacitance $C$ is given as

$$\Delta V \propto \sqrt{I_{MAX} - I_{MIN}}\,. \tag{8}$$

By Eq. (8), by increasing both $I_{MIN}$ and $I_{MAX}$, the voltage swing $\Delta V$ can be reduced without reducing the unit current $I_0$.

Figure 4(a) shows the schematic of the proposed current mirror. In the proposed circuit, a biasing current source is connected to the input node of the current mirror. As a result, $I_{MAX}$ and $I_{MIN}$ are increased as follows:

$$I_{MIN} = I_S, \tag{9}$$

$$I_{MAX} = (R - 1)\, I_0 + I_S. \tag{10}$$

By Eq. (8), the voltage swing $\Delta V$ of the load capacitance $C$ becomes smaller than that of Figure 3. Simultaneously, since both $I_{MIN}$ and $I_{MAX}$ are increased by $I_S$, the unit current $I_0$ is the same as Figure 3. Consequently, the switching delay for the proposed current mirror becomes smaller than that of Figure 3.

## 2.3 Evaluation

The use of larger biasing current makes the switching delay for current mirrors small. However, the power dissipation of current mirrors is increased because the power dissipation of biasing current sources is proportional to the biasing current $I_S$. The use of the power-delay product is one of the efficient design methods to achieve the optimum performance.

Now, we design a simple dual-rail MVCM circuit shown in Figure 5. Figure 6 shows the power-delay prod-

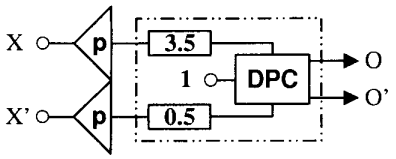



**Figure 5.** TD with current mirrors

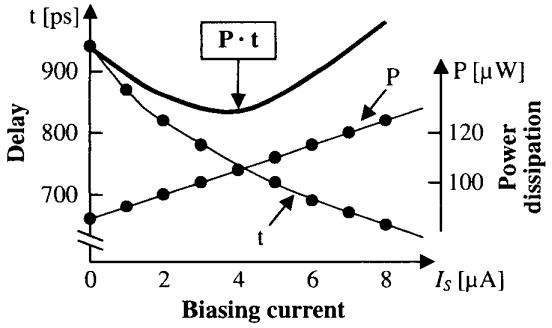



**Figure 6.** Power-delay product versus biasing current

uct versus biasing current $I_S$ in Figure 5 under a 0.35-μm standard CMOS technology. The power-delay product becomes smallest when the biasing current $I_S$ is 4μA.

Table 1 shows the performance of the circuit shown in Figure 5. Using both the proposed current mirror and the high-performance threshold detector, the delay and the power dissipation can be reduced to 70% and 80%, respectively, of the corresponding one without these high-performance basic components.

## 3. Design and Evaluation of a Signed-Digit Full Adder

As a typical application of the proposed MVCM circuits, a signed-digit full adder (SDFA) [9] is designed and evaluated.

### 3.1 Radix-2 SD addition algorithm

The radix-2 SD number representation using a symmetrical digit set {−1, 0, 1} is defined as follows:

$$\mathbf{X} = (X_{n-1} \cdots X_1 X_0) = \sum_{i=0}^{n-1} X_i \cdot 2^i \tag{11}$$

where $X_i \in \{-1, 0, 1\}$. The redundancy allows totally parallel arithmetic operations. The addition of two numbers,

**Table 1.** Comparison of TDs

(a) Delay

| | Conventional current mirror | Proposed current mirror |
|---|---|---|
| **Single supply voltage** | 1050 ps (100%) | 920 ps (87%) |
| **Multiple supply voltages** | 940 ps (89 %) | **740 ps (70 %)** |

(b) Power dissipation

| | Conventional current mirror | Proposed current mirror |
|---|---|---|
| **Single supply voltage** | 132 μW (100%) | 160 μW (121%) |
| **Multiple supply voltages** | 86 μW (65 %) | **106 μW (80 %)** |

$\mathbf{X} = (X_{n-1} \cdots X_1 X_0)$ and $\mathbf{Y} = (Y_{n-1} \cdots Y_1 Y_0)$ is performed by three successive steps in each digit as

$$Z_i = X_i + Y_i \tag{12}$$

$$2C_i + W_i = Z_i \tag{13}$$

$$S_i = W_i + C_{i-1} \tag{14}$$

where the arithmetic sum $\mathbf{Z} = (Z_{n-1} \cdots Z_1 Z_0)$, the intermediate sum $\mathbf{W} = (W_{n-1} \cdots W_1 W_0)$, the carry $\mathbf{C} = (C_{n-1} \cdots C_1 C_0)$ and the final sum $\mathbf{S} = (S_n \cdots S_1 S_0)$ are $Z_i \in \{-2, -1, 0, 1, 2\}$, $W_i \in \{-1, 0, 1\}$, $C_i \in \{-1, 0, 1\}$ and $S_i \in \{-1, 0, 1\}$, respectively.

To retain the final sum $S_i$ within the set $\{-1, 0, 1\}$, $C_i$ and $W_i$ are determined by $Z_{i-1}$ together with $Z_i$ as follows:

$$\begin{cases} C_i = 1, W_i = 0 & \text{if } Z_i = 2 \\ C_i = 1, W_i = -1 & \text{if } Z_i = 1 \text{ and } Z_{i-1} \geq 1 \\ C_i = 0, W_i = 1 & \text{if } Z_i = 1 \text{ and } Z_{i-1} < 1 \\ C_i = 0, W_i = 0 & \text{if } Z_i = 0 \\ C_i = 0, W_i = -1 & \text{if } Z_i = -1 \text{ and } Z_{i-1} \geq 1 \\ C_i = -1, W_i = 1 & \text{if } Z_i = -1 \text{ and } Z_{i-1} < 1 \\ C_i = -1, W_i = 0 & \text{if } Z_i = -2. \end{cases} \tag{15}$$

The final sum is independent of the word length $n$ because the carry-propagation chain is limited to one digit to left. Therefore the addition speed of the SD adder is higher than that of ordinary binary adders [10].

### 3.2 Design of a high-performance SDFA

The radix-2 SD adder can be designed using SDFAs as shown in Figure 7. In the dual-rail MVCM circuits, each

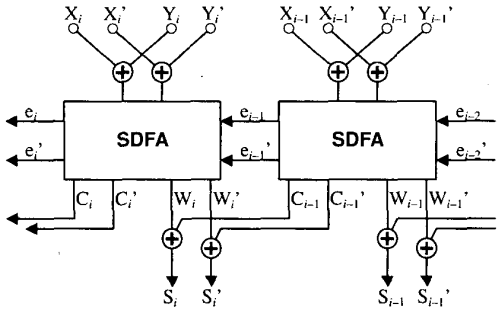



**Figure 7.** Radix-2 SD adder

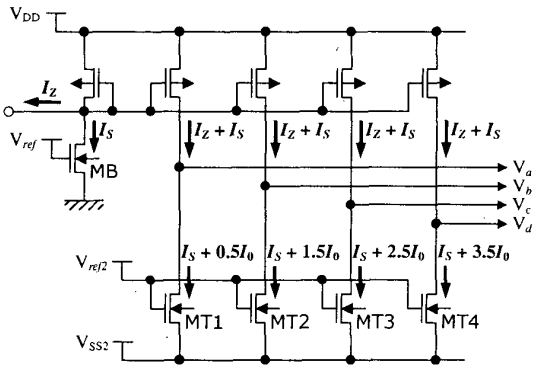



**Figure 9.** Schematic of the proposed input-value detector

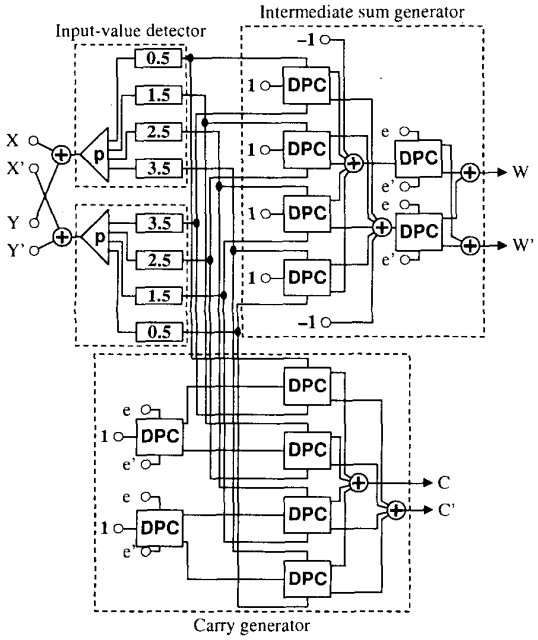



**Figure 8.** Block diagram of an SDFA

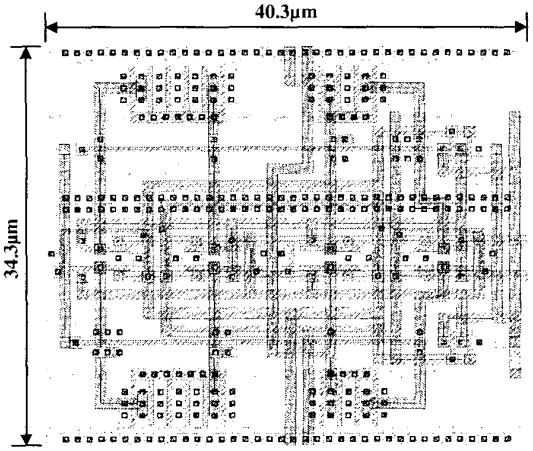



**Figure 10.** Layout of the proposed SDFA

digit of the SD numbers corresponds to a pair of complementary current signals. The arithmetic summation of Eqs. (12) and (14) can be obtained by wiring without active devices. The operation of Eq. (13) is performed with an SD full adder (SDFA). The control signals $e_i$ and $e_i$' are used to detect the conditions of $Z_{i-1} \geq 1$ and $Z_{i-1} < 1$ in Eq. (15).

Figure 8 shows the block diagram of a radix-2 SDFA using dual-rail MVCM circuit. An input-level detector is to compare 5-valued input with four reference currents and to generate four binary voltage outputs. An intermediate sum generator and a carry generator produce a pair of intermediate sum outputs and a pair of carry outputs, respectively, using the outputs of the input-value detector.

Figure 9 shows a schematic of the proposed input-value detector where $V_a$, $V_b$, $V_c$ and $V_d$ are four outputs of comparators, respectively. The biasing current source MB is connected to the input node of the current mirror, and the threshold current source MT1, MT2, MT3 and MT4 are increased for the biasing current $I_S$. The proposed current mirror is realized by adding just one transistor, which results in a high-speed switching.

Figure 10 shows the SDFA using proposed current

**Table 2.** Comparison of dual-rail MVCM SDFAs

| | Single supply voltage | Two supply voltages | Proposed |
|---|---|---|---|
| **Supply voltage(s)** | 1.8 V | 1.8 V<br>1.0 V | **1.8 V**<br>**1.0 V** |
| **Biasing current** | 0 μA | 0 μA | **4 μA** |
| **Delay** | 2.33 ns<br>(100%) | 2.00 ns<br>(86%) | **1.61 ns**<br>**(69%)** |
| **Power dissipation** | 645 μW<br>(100%) | 408 μW<br>(63%) | **450 μW**<br>**(70%)** |

HSPICE simulation
under a 0.35-μm standard CMOS technology

mirrors. Table 2 summarizes the performance of the proposed SDFA together with those of conventional SDFAs by HSPICE simulation under a 0.35-μm standard CMOS technology. In the proposed dual-rail MVCM SDFA, the switching delay for the current mirror becomes about 60% of the conventional current mirror in spite of the extra power dissipation of about 10%. Consequently, using both the high-performance TD and the current mirror, the switching delay and the power dissipation of the SDFA can be reduced to 69% and 70%, respectively, of the SDFA without these two high-performance basic components.

## 4. Conclusion

A new current mirror using a biasing current source has been proposed to achieve higher performance in dual-rail MVCM circuits. The use of the biasing current source makes the input current signal of the current mirror increased, which results in a high-speed switching. Moreover, using the power-delay product, a high-speed dual-rail MVCM circuit has been designed with saving the extra power dissipation. In fact, the performance of the proposed SDFA is superior to that of a corresponding MVCM circuit without high-performance basic components.

As a future prospect, it is also important to evaluate the efficiency of the dual-rail MVCM circuits with these two high-performance basic components in practical arithmetic VLSI processors.

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