Arithmetic-Oriented Multiple-Valued Logic-in-Memory VLSI Based on Current-Mode Logic

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Abstract

A new logic-in-memory architecture, in which storage elements are distributed over a current-mode logic-circuit plane by the use of floating-gate MOS transistors, is proposed to realize a compact arithmetic VLSI system. Since not only a storage function but also a voltage-mode linear summation and a voltage-to-current conversion are merged into a single floating-gate MOS transistor, the logic-in-memory VLSI becomes very compact with a high-performance capability. As an example, it is demonstrated that the effective chip area of the proposed four-valued current-mode full adder is reduced to 5% under the same switching speed in comparison with the corresponding binary CMOS implementation.

1. Introduction

Communication bottleneck between memory and logic modules is one of the most serious problems in recent deepsubmicron VLSI systems, for an example in the multimedia VLSI systems on a single chip [1]. A logic-in-memory structure, in which storage functions are distributed over a logic-circuit plane, is a key technology to solve the above problem [2]. When a small amount of storage is included in each cell of a logic-in-memory VLSI array, its VLSI array may be regarded either as a logically enhanced memory array, or as a logic array whose elementary gates and connections can be programmed to realize a desired logical behavior. However, the VLSI array is more complex to build and has lower storage density than a normal memory because of the overhead involved in the storage and logic elements.

From this point of view, a multiple-valued logic-in-memory VLSI architecture based on floating-gate MOS pass-transistor logic has been presented [3]-[5]. A floating-gate MOS transistor is generally used as a memory cell device of flash EEPROMs [6]. If a floating-gate MOS transistor can be utilized not only as a memory device but also as a logic gate, the circuit has a potential advantage of high-performance operations with less communication bottleneck between storage and logic elements.

On the other hand, multiple-valued current-mode (MVCM) integrated circuits have a potential advantage of the transistor counts as well as the wiring complexity in arithmetic VLSI chips because the frequently used linear summation can be performed simply by wiring[7]-[9]. However, a voltage input logic-in-memory design with floating-gate MOS transistors is essential to interchange voltage-mode logic circuits with current-mode ones. Therefore, it is necessary to realize a voltage-to-current converter.

This paper presents a new logic-in-memory VLSI based on current-mode logic which is suitable for arithmetic VLSIs. Three operations such as a storage function, a linear summation and a voltage-to-current conversion are merged into a single floating-gate MOS transistor. The linear conversion between a voltage and a current can be realized by a single MOS transistor because of the linearity between the gate voltage and the drain-to-source current. That linearity is due to the velocity saturation of channel carriers which is one of the short channel effects in the recent submicron devices[10]. In addition, the drain-to-source current of a floating-gate MOS transistor corresponds to the linear summation between the control-gate voltage and the stored voltage due to the charge on the floating gate.

As a typical example of the proposed MVCM logic-in-memory VLSI, a four-valued current-mode full adder

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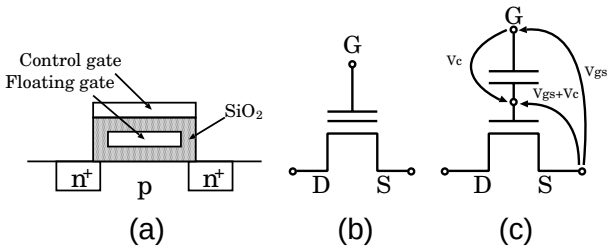
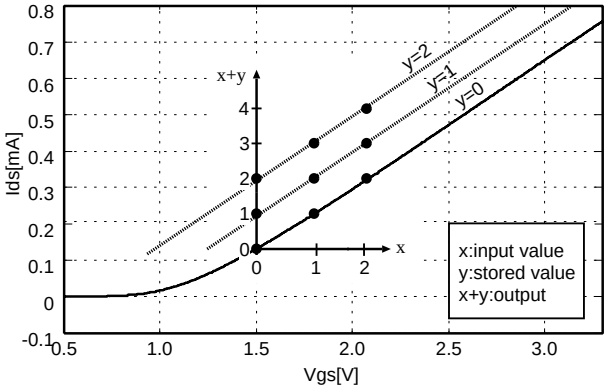


Figure 1. Floating-gate MOS transistor: (a)Cross-sectional view, (b)Symbol, (c)Equivalent circuit.



HSPICE simulation based on a 0.5μm CMOS technology

Figure 2. Characteristic of a floating-gate MOS transistor.

with a storage capability is also presented. It is demonstrated with a 0.5-μm CMOS technology that the effective chip area of the proposed full adder is reduced to 5% in comparison with that of the corresponding binary CMOS implementation under the same switching speed.

2. Basic components of an MVCM logic-in-memory VLSI

In this section, we discuss about basic components of an MVCM logic-in-memory VLSI.

2.1. Characteristics of a floating-gate MOS transistor

Figures 1(a) and (b) show a cross-sectional view and its symbol of a floating-gate MOS transistor which consists of a transistor with two gates, one of which is isolated from the circuit. If this floating gate acquires charge to represent a stored value, the charge remains there for a long period of time because the gate is insulated from its surroundings by silicon dioxide. Since the insulator exists between a control gate and a floating gate, each gate can be regarded as an electrode of a capacitor. Therefore, the equivalent circuit can be expressed by the combination of a MOS transistor and a capacitor as shown in Figure 1(c). If the floating gate acquires charge, a certain potential difference V_c appears on the capacitor. Hence, the effective gate voltage of the floating-gate MOS transistor corresponds to the linear summation of the input value V_{gs} and the stored value V_c. Thus, the use of a floating-gate MOS transistor makes it possible to shift the threshold voltage as

$$\begin{aligned} I_{ds} &= \frac{\beta}{2}(V_{gs} - V_{th})^2 \\ V_{th} &= V_{th0} - V_c. \end{aligned} \tag{1}$$

Figure 2 shows the $I_{ds} - V_{gs}$ characteristic of a floating-gate MOS transistor under a 0.5-μm CMOS parameter. With such submicron devices, short channel effects can not be neglected. One of the short channel effects is the velocity saturation of channel carriers. In a 0.5-μm channel, V_{ds}=3.3V results in an average field of 66kVcm^{-1} while electron velocity already saturates at around 20kVcm^{-1}. Most of the channel electrons drift with the constant saturation velocity. This results in a lower current than the expected current and it becomes proportional to $V_{gs} - V_{th}$ instead of to $(V_{gs} - V_{th})^2$[10].

Therefore, the effective input voltage can be shifted by the floating-gate and this effective input voltage is proportionally converted into the drain-to-source current as shown in Figure 2. The drain-to-source current I_{ds} is determined by an input voltage V_{gs} and a stored voltage V_c, and is expressed as

$$\Delta I_{ds} \propto \Delta(V_{gs} + V_c). \tag{2}$$

where V_{gs} and V_c correspond to an input value x and a stored value y, respectively, and I_{ds} corresponds to the output value.

Hence, a voltage-to-current conversion, a storage function and a linear summation between an input value and a stored value can be realized by a single floating-gate MOS transistor.

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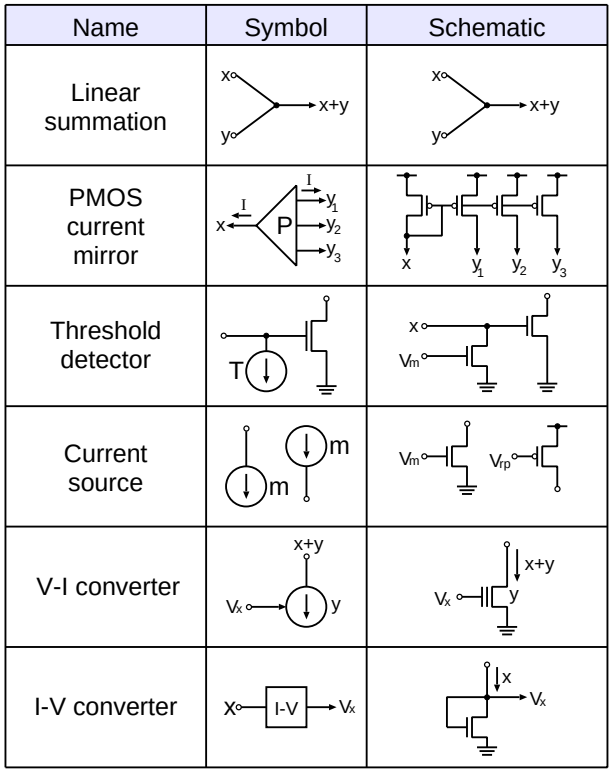


Figure 3. Basic building blocks.

2.2. Basic components

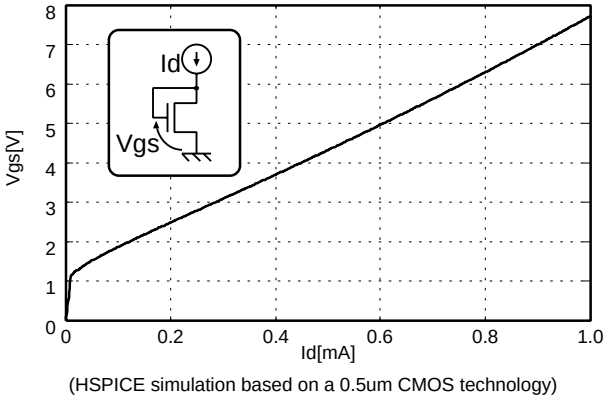
Figure 3 shows the basic building blocks of the proposed MVCM logic-in-memory circuit. By the combination of the proposed components, we can design a high-performance MVCM logic-in-memory VLSI.

1. Linear summation: The most attractive feature of MVCM logic circuits is the linear summation can be performed by wiring without active devices, so that the resulting arithmetic circuits become quite simple.

2. PMOS current mirror: A PMOS current mirror produces several replicas of an input current. The current mirror also has the function of inverting the direction.

3. Threshold detector: The function of a threshold detector is to detect an input current level and to regenerate the multiple-valued current.

4. Current source: A current source can be designed by an enhancement-mode NMOS (or PMOS) transistor with the reference voltage V_{rn} (or V_{rp}). The current level is adjusted by the transistor size.



(HSPICE simulation based on a 0.5um CMOS technology)

Figure 4. Characteristic of a current-to-voltage converter.

5. V-I converter: A voltage-mode input is converted into a current-mode output by the V-I converter. A voltage-mode linear summation between an input value x and a stored value y is also performed and the above result is proportionally converted into a current-mode output by a single floating-gate MOS transistor as shown in Figure 2. The slope of the output current versus the input voltage can be adjusted by the ratio of the channel width to the length of a transistor.

6. I-V converter: A current-mode output is converted into a voltage-mode output by the I-V converter. The output voltage is proportional to the input current because of the linearity of the $V_{gs} - I_d$ characteristic as shown as Figure 4. The slope of the output voltage versus the input current is adjusted by the ratio of the channel width to the length of a transistor as same as the V-I converter.

3. Design of an MVCM logic-in-memory VLSI

The design concept and the design example of an MVCM logic-in-memory VLSI are presented in this section.

3.1. General structure

Figure 5 shows a general structure of the MVCM logic-in-memory VLSI which has a voltage-mode input and voltage-mode outputs. The linear summation between a multiple-valued voltage-mode input

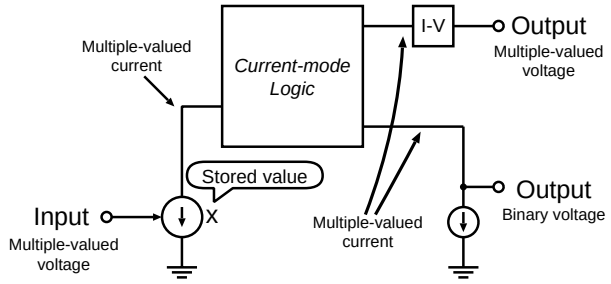


Figure 5. Overall structure of the MVCM logic-in-memory VLSI.

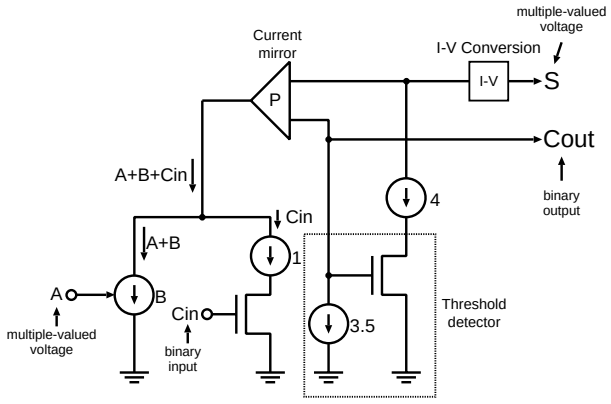


Figure 6. Circuit diagram of the four-valued full adder.

and a multiple-valued stored value is converted into a multiple-valued current by a floating-gate MOS transistor. The produced current is used as an input value of the MVCM logic circuit.

The output of the MVCM logic circuit can be converted into a binary voltage-mode output and/or a multiple-valued voltage-mode output by a threshold detector and/or an I-V converter circuit, respectively.

3.2. Design example of a four-valued full adder

Figure 6 shows a circuit diagram of a four-valued full adder based on an MVCM logic-in-memory structure which has a storage capability in the logic-circuit plane. It has two kinds of four-valued inputs, A (an external input) and B (a stored constant input), a binary input C_{in}, a binary output C_{out} and a four-valued output S. The addition of two numbers, $A(\in \{0,1,2,3\})$ and

Table 1. Relationship between logic values and input voltages

Logic value (A)	0	1	2	3
Control gate voltage [V]	0	0.5	1.0	1.5

Table 2. Relationship between logic values and current levels

Logic value (Z,S)	0	1	2	3	4	5	6	7
Current level [μA]	10	45	80	115	150	185	220	255

$B(\in \{0,1,2,3\})$ is performed as follows:

$$\begin{aligned} Z &= A + B + C_{in}, \\ C_{out} &= \begin{cases} 0 & \text{if } Z \le 3.5, \\ 1 & \text{otherwise}, \end{cases} \\ S &= \begin{cases} Z & \text{if } Z \le 3.5 \quad (C_{out} = 0), \\ Z - 4 & \text{otherwise} \quad (C_{out} = 1), \end{cases} \end{aligned} \tag{3}$$

where $S \in \{0,1,2,3\}$ and $C_{in}, Cout \in \{0,1\}$.

In this circuit, the addition of $(A+B)$ is performed by a single floating-gate MOS transistor, and the subsequent addition with C_{in} is done by just wiring. The carry output C_{out} is a voltage-mode output which is produced by a threshold detector. The sum S is produced by a constant current source and a threshold detector which is shared with that of the carry output. The final output of the sum is converted into a voltage-mode output by an I-V converter. The relationship between logic values and input voltages is shown in Table 1, and the relationship between logic values and current levels is shown in Table 2.

The peripheral circuit to distribute a four-valued input voltage in the logic-circuit plane and the program circuit for the floating-gate MOS transistors can be designed by using the almost same one in a multi-level flash memory[11].

3.3. Evaluation

Figure 7 shows a simulated transient characteristic of the four-valued full adder with 0.5-μm CMOS parameters. The input variable A is set to "0","1","2" and "3" at time intervals of 5[ns]. The other variables B and C_{in} are set to "2" and "0", respectively. The maximum delay of the carry output is evaluated to be about 0.8[ns]. Table 3.3 summarizes the comparison of full adders in terms of the switching delay and the

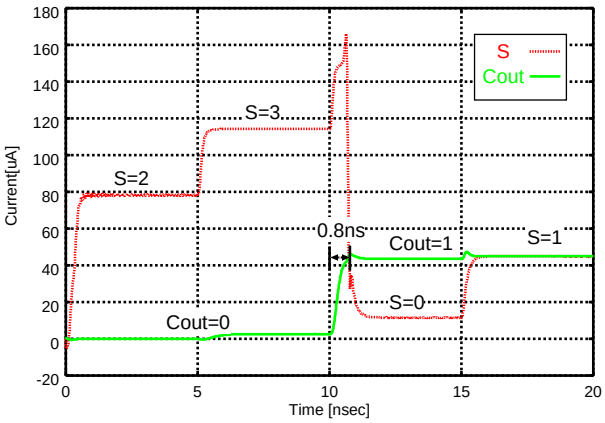


Figure 7. Transient characteristic of the four-valued full adder.

Table 3. Comparison of full adders

	Delay[2]	Area
2bit binary CMOS[1]	0.8ns	12000μm^2
Proposed	0.8ns	620μm^2

(HSPICE simulation based on a 0.5um CMOS technology)
[1] 2bit binary CMOS full-adder with 6Tr-SRAM cells
[2] Delay of the carry output

effective chip area. In the proposed circuit, a voltage-mode linear summation $(A+B)$ is performed, and it is converted into a current by a single floating-gate MOS transistor. Furthermore, a current-mode linear summation between the above result and C_{in} is realized by just wiring in the MVCM logic circuit. As a result, the effective chip area of the proposed MVCM logic-in-memory adder is reduced to 5% in comparison with that of the binary CMOS one.

4. Conclusion

A new VLSI architecture, in which storage functions are merged into an MVCM logic circuit, has been presented to realize an MVCM logic-in-memory VLSI with less area penalty. In the proposed design concept, a storage function and a linear summation are merged into a voltage-to-current conversion by using a single floating-gate MOS transistor, which makes it possible to integrate floating-gate MOS transistors into an MVCM logic circuit. Its performance is much superior to that of the corresponding binary CMOS implementation in terms of the chip area under the same switching speed. The proposed MVCM logic-in-memory architecture is suitable for image processing such as linear filtering or template matching. The write speed for charge injection onto a floating gate is quite low compared with that of SRAM or DRAM. However, in these image processing, it is not so serious because the filter masks or templates are fixed before processing and they are rarely changed.

As a future prospect of the multiple-valued logic-in-memory VLSI, it is important to establish a systematic design method including logic design. Moreover, it is interesting to design a multiple-valued hybrid-mode logic circuit which consists of current-mode and voltage-mode logic circuits using functional devices such as a floating-gate MOS transistor.

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