Low-Power Dual-Rail Multiple-Valued Current-Mode Logic Circuit Using Multiple Input-Signal Levels

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Abstract

A new high-speed and low-power threshold detector is proposed to realize high-performance arithmetic VLSI systems. In a conventional threshold detector with a single supply voltage, the input signal swing of a differential-pair circuit (DPC) is too large, which causes large power dissipation together with a long switching delay. The use of two kinds of supply voltages makes the input signal swing of the DPC small, which results in a lower power dissipation together with a higher switching speed. As a typical example of the proposed multiple-valued current-mode (MVCM) logic circuit, a radix-2 signed-digit full adder is designed by using a 0.35-μm CMOS technology. Its performance is superior to that of a corresponding MVCM logic circuit with a single supply voltage under the same transistor counts.

1. Introduction

In the recent deep-submicron VLSI era, low-power circuit design with keeping a high-speed switching capability at a low supply voltage is needed not only for battery-powered portable applications, but also to reduce the power dissipation of dedicated special-purpose VLSI processors because the extra current density in wires may cause temporal or permanent malfunction due to voltage drops or electromigration [1]-[5].

A multiple-valued current-mode (MVCM) integrated circuit based on dual-rail differential logic has a potential advantage to realize a high-speed logic circuit at a low supply voltage, because the use of a differential-pair circuit (DPC) in a threshold detector, which is a key component of the MVCM circuit, make a voltage swing small yet driving capability large [6]. Moreover, when several DPCs are not active in the MVCM logic circuit, the gate voltages of current sources in these corresponding DPCs can be turned off, which makes it possible to achieve a low-power dissipation with keeping a high-speed operation in the MVCM logic circuit [7].

However, the input voltage swing of a differential-pair circuit (DPC) becomes same as the output voltage swing of a comparator although the input voltage swing of the DPC can be small. Therefore, in the threshold detector with a single supply voltage, the input voltage swing of the DPC becomes too large, which causes large power dissipation together with a long switching delay.

In this paper, a new threshold detector with two supply voltages is proposed. The use of two different supply voltages makes the input voltage swing of the DPC small. As a result, a high-speed and low-power threshold detector can be realized.

As a typical example of high-performance arithmetic circuits based on dual-rail MVCM logic, a signed-digit full adder (SDFA) with multiple supply voltages of 2.0V and 1.0V is designed based on a 0.35-μm CMOS technology. As a result, the switching delay and the power dissipation can be reduced to 80% and 58%, respectively, of a corresponding SDFA with a single supply voltage of 2.0V.

2. Model of a High-Performance Multiple-Valued Integrated Circuit

In this section, we discuss about the relationship between the power supply and the switching speed of a threshold detector, and about the usefulness of multiple power supplies.

2.1 Basic components of a multiple-valued VLSI

Figure 1 shows the basic components of the MVCM logic circuit.

1) *Wired-sum circuit:* In the MVCM logic circuits, arithmetic summation can be performed by wiring without active devices, so that the resulting arithmetic circuits become simple.

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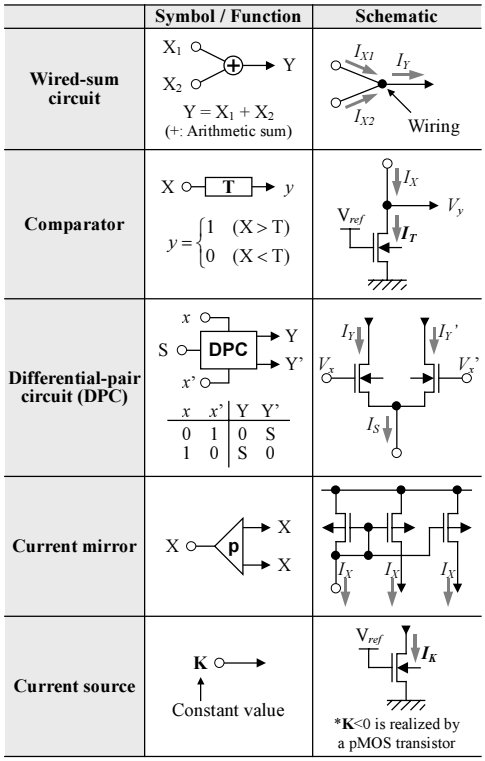


Figure 1. MVCM basic components

2) *Comparator:* A comparator is to compare an input current I_X with a threshold current I_T, and to generate an output voltage V_y.
3) *Differential-pair circuit (DPC):* A DPC is to generate a multiple-valued differential-pair output (0, S) or (S, 0) in accordance with a binary differential-pair input where its function is defined in Figure 1.
4) *Current Mirror:* A current mirror produces several replicas of an input current. The current mirror also has the function of inverting the current direction.
5) *Current Source:* A current source can be designed by an enhancement-mode nMOS transistor with the reference voltage V_{ref}. The current level is adjusted by the transistor size.

By the combination of these components, we can design high-performance MVCM logic circuits.

Figure 2 shows a design example of MVCM logic circuits where the outputs S and S' are obtained by wired sum of four threshold detector's outputs. Constant values –2, –1 and 1, connected to wired-sum circuits, are to generate 3-valued dual-rail outputs. The use of an analog adder makes the MVCM logic circuits compact because it can be realized by wiring without active devices. A threshold detector, which consists of three components: a differential-pair circuit (DPC) and two comparators, is a

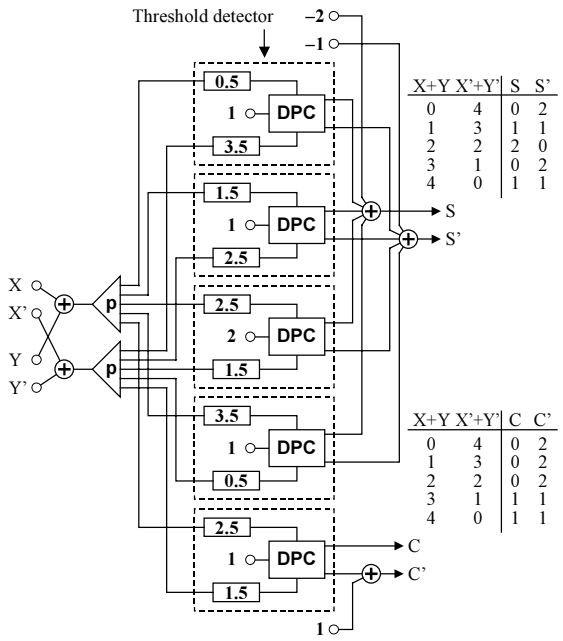


Figure 2. 3-valued half-adder

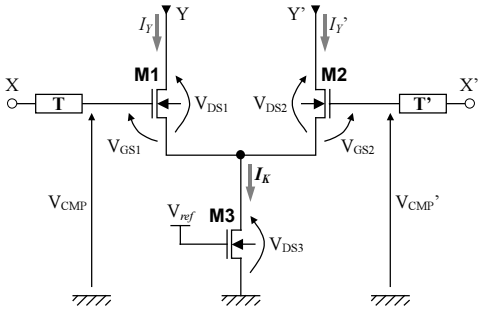


Figure 3. Threshold detector

key component to determine the operating speed of dual-rail MVCM logic circuits. In the following section, we discuss about a design of a new threshold detector.

2.2 Design of a dual-rail threshold detector with multiple supply voltages

The signal-voltage swing for switching in the dual-rail MVCM logic circuit becomes smaller than that of a conventional circuit with a single-rail input. Consequently, it is important to design a high-speed threshold detector using dual-rail complementary signals.

Figure 3 shows a schematic of a threshold detector including two comparators and a DPC. Assume that the output currents of Y and Y', and the constant current of the current source M3 are I_Y, I_Y' and I_K, respectively.

When the DPC works correctly, the following condition should be satisfied:

$$I_Y(SR) + I_Y'(SR) > I_K \quad (1)$$

where $I_Y(SR)$ and I_Y (SR) are I_Y and I_Y' when it is supposed that transistors M1 and M2 operate in the saturation region, respectively. Then M1 and M2 operate in the linear region, and I_Y and I_Y' are described as

$$I_Y = \frac{\beta}{2}(2(V_{GS1} - V_T)V_{DS1} - {V_{DS1}}^2) = f(V_{GS1})$$
$$I_Y' = \frac{\beta}{2}(2(V_{GS2} - V_T)V_{DS2} - {V_{DS2}}^2) = f(V_{GS2}). \quad (2)$$

Since the drain-to-source voltage V_{DS3} of the transistor M3 is increased so as to satisfy the following condition:

$$I_Y + I_Y' = I_K. \quad (3)$$

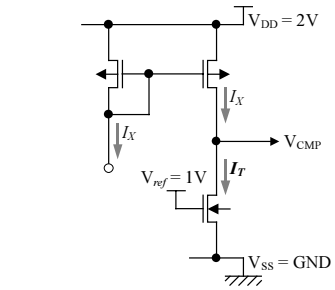
The input voltage swing V_{DPC} of the DPC

$$V_{DPC} = |V_{GS1} - V_{GS2}| \quad (4)$$

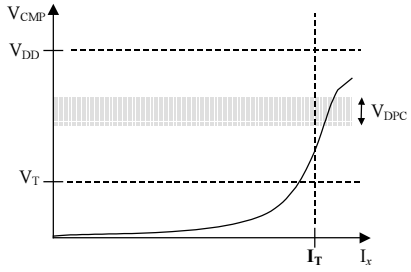
must be given by using Eq. (2) as

$$|f(V_{GS1}) - f(V_{GS2})| = I_K. \quad (5)$$

In a dual-rail MVCM logic circuit under a 0.35μm CMOS technology, V_{DPC} becomes about 0.3V.



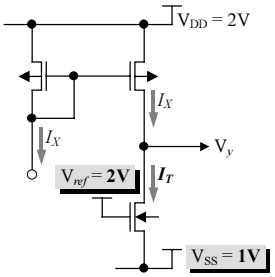
(a) Schematic



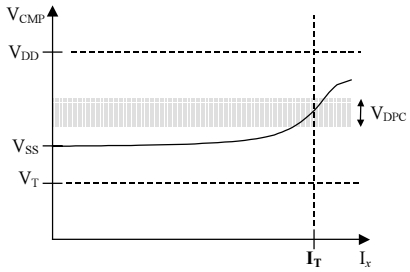
(b) Input-output characteristic

Figure 4. Comparator using a single power supply

Figure 4 shows a circuit diagram and a DC characteristic of a comparator. As shown in Figure 4 (b), the input voltage swing V_{CMP} is much larger than V_{DPC} in case of a single supply voltage, the operating region of V_{CMP} are not compatible with that of V_{DPC}, which causes larger switching delay together with larger power dissipation of the threshold detector.



(a) Schematic



(b) Input-output characteristic

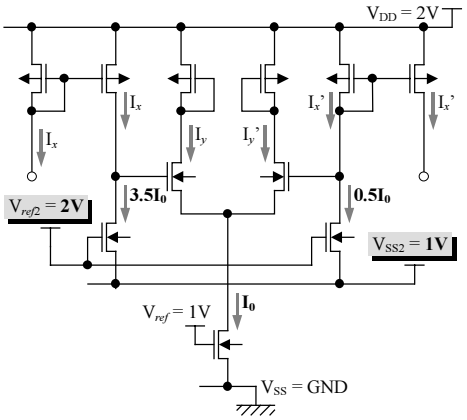
Figure 5. Schematic of the proposed comparator

Figure 5 shows a circuit diagram and a DC characteristic of a new threshold detector. When the supply voltage V_{SS} in the comparator is set to more than the ground level, the operating region of V_{DPC} becomes adjusted in the middle of V_{CMP}. In fact, when $V_{DD} = 2V$, $V_{SS1} = 0V$ and $V_{SS2} = 1V$ in the proposed threshold detector shown in Figure 6 and Table 1, its switching delay and its power dissipation are reduced to 75% and 77%, respectively, in comparison with those of a corresponding threshold detector with a single supply voltage.

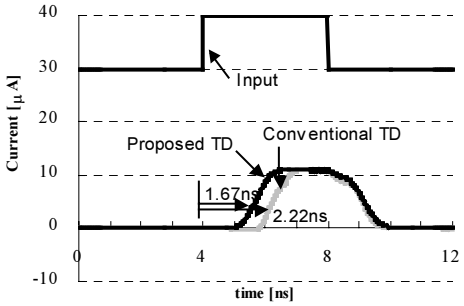
3. Design and Evaluation of an Arithmetic Circuit

As a typical application of the proposed MVCM logic circuits, a signed-digit full adder (SDFA) [8] is designed and evaluated.

3.1 Radix-2 SD addition algorithm



(a) Schematic



(b) Waveforms

Figure 6. Proposed threshold detector (T = 3.5)

The radix-2 SD number representation using a symmetrical digit set {–1, 0, 1} is defined as follows:

$$\mathbf{X} = (X_{n-1} \cdots X_1 X_0) = \sum_{i=0}^{n-1} X_i \cdot 2^i \tag{6}$$

where $X_i \in \{-1, 0, 1\}$. The redundancy allows totally parallel arithmetic operations. The addition of two numbers, $\mathbf{X} = (X_{n-1} \cdots X_1 X_0)$ and $\mathbf{Y} = (Y_{n-1} \cdots Y_1 Y_0)$ is performed by three successive steps in each digit as

$$Z_i = X_i + Y_i \tag{7}$$

$$2C_i + W_i = Z_i \tag{8}$$

$$S_i = W_i + C_{i-1} \tag{9}$$

where the arithmetic sum $\mathbf{Z} = (Z_{n-1} \cdots Z_1 Z_0)$, the intermediate sum $\mathbf{W} = (W_{n-1} \cdots W_1 W_0)$, the carry $\mathbf{C} = (C_{n-1} \cdots C_1 C_0)$ and the final sum $\mathbf{S} = (S_n \cdots S_1 S_0)$ are $Z_i \in \{-2, -1, 0, 1, 2\}$, $W_i \in \{-1, 0, 1\}$, $C_i \in \{-1, 0, 1\}$ and $S_i \in \{-1, 0, 1\}$, respectively.

To retain the final sum S_i within the set {–1, 0, 1}, C_i and W_i are determined by Z_{i-1} together with Z_i as follows:

Table 1. Comparison of two TDs (T=3.5)

	Conventional	Proposed
Supply voltage (Output generator)	2.0 V	2.0 V
Supply voltage (Comparator)	2.0 V	**1.0 V**
Delay	2.22 ns	**1.67 ns**
Power dissipation	160 μW	**124 μW**

$$\begin{cases} C_i = 1, W_i = 0 & \text{if } Z_i = 2 \\ C_i = 1, W_i = -1 & \text{if } Z_i = 1 \text{ and } Z_{i-1} \geq 1 \\ C_i = 0, W_i = 1 & \text{if } Z_i = 1 \text{ and } Z_{i-1} < 1 \\ C_i = 0, W_i = 0 & \text{if } Z_i = 0 \\ C_i = 0, W_i = -1 & \text{if } Z_i = -1 \text{ and } Z_{i-1} \geq 1 \\ C_i = -1, W_i = 1 & \text{if } Z_i = -1 \text{ and } Z_{i-1} < 1 \\ C_i = -1, W_i = 0 & \text{if } Z_i = -2. \end{cases} \tag{10}$$

The final sum is independent of the word length *n* because the carry-propagation chain is limited to one digit to left. Therefore the addition speed of the SD adder is higher than that of ordinary binary adders [9].

3.2 Design of a high-performance SDFA

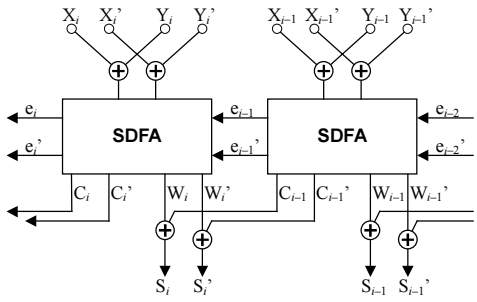


Figure 7. Radix-2 SD adder

The radix-2 SD adder can be designed using SDFAs as shown in Figure 7. In the dual-rail MVCM logic circuits, each digit of the SD numbers corresponds to a pair of complementary current signals. The arithmetic summation of Eqs. (7) and (9) can be obtained by wiring without active devices. The operation of Eq. (8) is performed with an SD full adder (SDFA). The control signals e_i and e_i' are used to detect the conditions of $Z_{i-1} \geq 1$ and $Z_{i-1} < 1$ in Eq. (10).

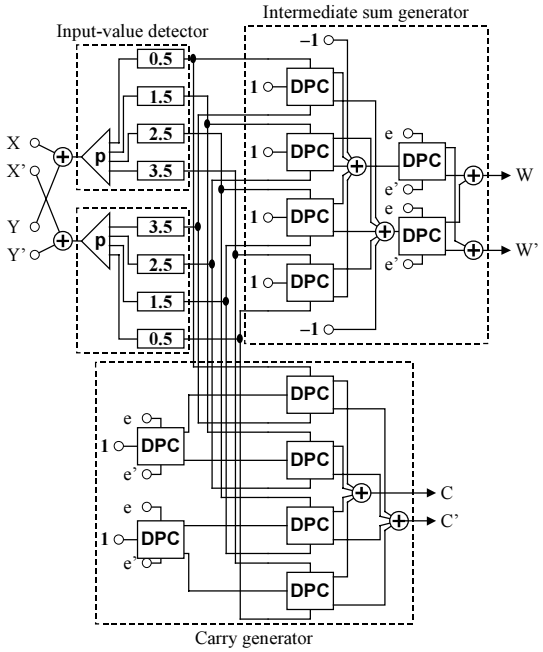


Figure 8. Block diagram of an SDFA

Figure 8 shows a block diagram of a radix-2 SDFA using dual-rail MVCM logic circuit. An input-level detector is to compare 5-valued input with four reference currents and to generate four binary voltage outputs. An intermediate sum generator and a carry generator produce a pair of intermediate sum outputs and a pair of carry outputs, respectively, using the outputs of the input-value detector.

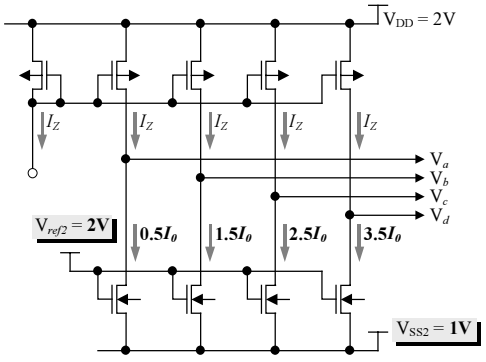


Figure 9. Schematic of the proposed input-value detector

Figure 9 shows a schematic of the proposed input-value detector where V_a, V_b, V_c and V_d are four outputs of comparators, respectively. The circuit structure except two additional supply voltages V_{SS2} and V_{ref2} is same as a corresponding MVCM circuit with a single supply voltage, which results in a high-speed switching and a low-power dissipation with less hardware overhead.

3.3 Evaluation

Table 2 summarizes the performance of the proposed SDFA together with those of a conventional SDFA by HSPICE simulation under a 0.35-μm CMOS technology. In the proposed dual-rail MVCM SDFA, the supply voltage of two input-value detectors, whose power dissipation is over 70% of total power dissipation, becomes half of the conventional SDFA. As a result, in the proposed dual-rail MVCM SDFA, the power dissipation can be reduced to 58% as well as the switching delay to 80% of a conventional dual-rail MVCM SDFA.

Table 2. Comparison of dual-rail MVCM SDFAs

	Conventional SDFA	**Proposed SDFA**
Supply voltage (Comparator)	2.0 V	2.0 V
Supply voltage (Output generator)	2.0 V	**1.0 V**
Delay	4.0 ns	**3.2 ns**
Power dissipation	363 μW	**212 μW**

4. Conclusion

A new threshold detector using multiple supply voltage has been proposed to achieve both high-performance and low-power dissipation in the MVCM logic circuit. The use of two different supply voltages makes the output voltage swing in the comparators small, which results in a high-speed switching. Since this additional supply voltage is lower than the conventional one, total power dissipation can be greatly reduced. In fact, the performance of the proposed SDFA is superior to that of a corresponding MVCM circuit using a single supply voltage.

As a future prospect, it is also important to evaluate the efficiency of the MVCM circuits with multiple supply voltages in practical arithmetic VLSI processors.

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