Static-Hazard-Free T-Gate for Ternary Memory Element and Its Application to Ternary Counters

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Static-Hazard-Free T-Gate for Ternary Memory Element and Its Application to Ternary Counters

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***Abstract*—The ternary T-gate can be used as a basic building block to construct both combinational and sequential circuits. Since the T-gate is one kind of tree-type universal logic module, any combinational circuit can be built up with modular logic arrays. For constructing ternary memory elements, however, the T-gate is required to be static hazard-free. A theoretical study is done on the necessary conditions for the practical realization of the static-hazard-free T-gate. On the basis of the result obtained, the static-hazard-free T-gate is realized using the ECL technique. The static-hazard-free T-gates obtained here can be used as building blocks to construct memory elements. Various memory elements such as D flip-flap-flop (FFF), D master–slave FFF, B master–slave FFF, and counting FFF is constructed easily. Using these memory elements, three different types of ternary counters can be designed and realized. They are an asynchronous signed ternary counter, a synchronous signed ternary counter, and a counter based on a shift register. Their design methods are discussed. These ternary counters are superior to the binary ones in that the up–down counting can easily be carried out by one input signal.**

***Index Terms*—Counter based on shift register, emitter coupled logic (ECL), feedback shift register (FSR), signed ternary number representation, static-hazard-free T-gate, symmetrical modulo-M counter, synchronous and asynchronous signed ternary counter, ternary memory element, up–down counting.**

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I. INTRODUCTION

THE TERNARY T-gate which constructs a complete system [1] can be used as a basic building block to construct both the combinational and sequential circuits

[2]. The T-gate will be easily implemented with the development of integrated circuit technology which makes it possible to produce a complex module on one chip. So far, the T-gate has been implemented by various electronic circuits [3]–[6]. Moreover, a systematic design method for synthesizing T-gate networks has been shown in [7]. However, the properties which are required of the T-gate for memory elements have not yet been studied in detail. Moreover, it has not been shown that various types of ternary memory elements and ternary counters can be realized by using T-gates as building blocks.

The T-gate for the memory elements must be static hazard-free for the change of a control signal. First, in this paper a theoretical study which is done on the necessary conditions for the practical realization of the static-hazard-free T-gate is presented. On the basis of the result obtained, the current mode circuit of T-gate which is static-hazard-free is designed and implemented as an example. This circuit is experimentally assured to be static hazard-free for the change of a control signal. The current mode technique is very suitable for integrated circuits, because it consists of only one n-p-n type of transistor and operating speed is principally very fast.

Using the static-hazard-free T-gates obtained here as building blocks, the ternary memory elements such as D-FFF, D master–slave FFF, B master–slave FFF, and counting FFF can be easily constructed. Their operating properties are studied theoretically and experimentally.

The practical ternary sequential circuit can systematically be realized on the basis of such memory elements. In this paper, three different ternary counters are designed and realized. Two of them are synchronous and asynchronous signed ternary counters based on the signed ternary number representation [8], [9]. The other one is a counter based on a shift register whose configuration corresponds to the bilateral ternary feedback shift register. In counting the ternary sequence, it is assumed that the counting pulse is return-to-zero (RZ) one. That is, the direct change from "1" to "−1" or vice versa is not allowed in counted pulses. If the direct change is allowed, it causes a static hazard and a misbehavior. Moreover, a positive pulse "1" is counted to the up direction while a negative pulse "−1" is counted to the down direction. Their synthesis methods and properties are discussed in view of constructing a ternary digital system.

II. Circuit Implementation of T-Gate for Memory Elements

A. Algebraic Analysis

The ternary T-gate is defined as [1], [2]

$$T(p,q,r;s) = p \cdot J_1(s) + q \cdot J_0(s) + r \cdot J_{-1}(s) \qquad (1)$$

where the variables p, q, r, and $s \in L = \{1,0,-1\}$, and where the product $\cdot$, the sum $+$, and J operators are defined as follows:

$$x \cdot y = \min(x,y), \qquad x + y = \max(x,y),$$

$$J_k(s) = \begin{cases} 1 & \text{if } s = k \\ -1 & \text{if } s \neq k. \end{cases}$$

Theorem 1:

$$T(p,q,r;s) = (p + h_1(s)) \cdot q \cdot (r + h_{-1}(s)) + p \cdot J_1(s) + r \cdot J_{-1}(s), \qquad (2)$$

where h operators are defined as

$$h_k(s) = \begin{cases} -1 & \text{if } s = k \\ 1 & \text{if } s \neq k. \end{cases}$$

Proof: h operators are expressed as $h_1(s) = J_0(s) + J_{-1}(s)$ and $h_{-1}(s) = J_1(s) + J_0(s)$ [9]. The given equation is expanded as follows:

$$\begin{aligned} F &= (p + h_1(s)) \cdot q \cdot (r + h_{-1}(s)) + p \cdot J_1(s) + r \cdot J_{-1}(s) \\ &= (p + J_0(s) + J_{-1}(s)) \cdot q \cdot (r + J_1(s) + J_0(s)) \\ &\quad + p \cdot J_1(s) + r \cdot J_{-1}(s) \\ &= q \cdot (p \cdot r + p \cdot J_1(s) + p \cdot J_0(s) + r \cdot J_0(s) \\ &\quad + J_1(s) \cdot J_0(s) + J_0(s) \cdot J_0(s) + r \cdot J_{-1}(s) \\ &\quad + J_1(s) \cdot J_{-1}(s) + J_0(s) \cdot J_{-1}(s)) \\ &\quad + p \cdot J_1(s) + r \cdot J_{-1}(s). \end{aligned}$$

Using the following relationships [9]

$$J_k(s) \cdot J_{k'}(s) = \begin{cases} J_k(s) & k = k' \\ -1 & k \neq k', \end{cases} \qquad x + x \cdot y = x$$

the equation becomes as

$$F = p \cdot q \cdot r + p \cdot J_1(s) + q \cdot J_0(s) + r \cdot J_{-1}(s).$$

Since $J_1(s) + J_0(s) + J_{-1}(s) = 1$,

$$\begin{aligned} F &= p \cdot q \cdot r \cdot (J_1(s) + J_0(s) + J_{-1}(s)) + p \cdot J_1(s) \\ &\quad + q \cdot J_0(s) + r \cdot J_{-1}(s) \\ &= p \cdot (q \cdot r + 1) \cdot J_1(s) + q \cdot (p \cdot r + 1) \cdot J_0(s) \\ &\quad + r \cdot (p \cdot q + 1) \cdot J_{-1}(s) \\ &= p \cdot J_1(s) + q \cdot J_0(s) + r \cdot J_{-1}(s). \end{aligned}$$

Therefore,

$$T(p,q,r;s) = (p + h_1(s)) \cdot q \cdot (r + h_{-1}(s)) + p \cdot J_1(s) + r \cdot J_{-1}(s). \quad \text{Q.E.D.}$$

The block diagram corresponding to (2) is shown in Fig. 1.

In realizing ternary memory elements, the T-gate is required to be static hazard-free as shown in Section III. Theorem 2 assures that the T-gate in (2) is static hazard-free.

Theorem 2: When p equals q, and the control signal s is changed from "1" to "0," then the output of the T-gate in (2) is static hazard-free. Similarly, when r equals q, and the control signal s is changed from "−1" to "0," then the output of the T-gate in (2) is static hazard-free.

Proof: In (2), let us consider the case where p equals q and s is changed from "1" to "0." As the $J_{-1}(s)$ is always "−1" and $h_{-1}(s)$ is always "1" even in the transient state

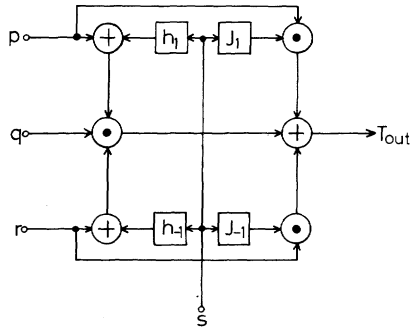


Fig. 1. Block diagram of a static-hazard-free T-gate.

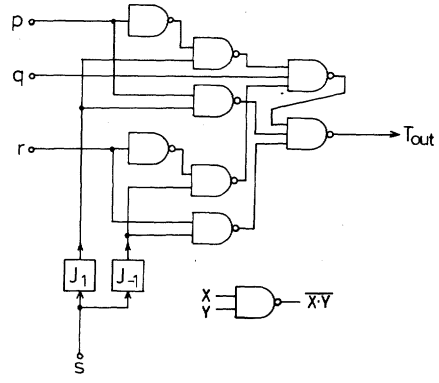


Fig. 2. Block diagram of a static-hazard-free T-gate consisting of ternary NAND gates.

of the control signal s, $T_{\text{out}} = (p + h_1(s)) \cdot q \cdot (r + 1) + p \cdot J_1(s) + r \cdot (-1) = (p + h_1(s)) \cdot q + p \cdot J_1(s)$. Then, T_{out} becomes as

$$T_{\text{out}} = (p + h_1(s)) \cdot p + p \cdot J_1(s) = p \cdot (p + h_1(s) + J_1(s)). \quad (3)$$

This indicates that T_{out} is always $p(= q)$ regardless of the transient state of the control signal s. Similarly, in the case where r equals q and s is changed from "-1" to "0," T_{out} is always $r(= q)$ regardless of the transient state of the control signal s. In other words, under the static conditions, the T-gate as shown in Fig. 1 is a static-hazard-free circuit. Q.E.D.

Corollary 1:

$$T(p,q,r;s) = \overline{\overline{p} \cdot J_1(s) \cdot q \cdot \overline{r} \cdot J_{-1}(s)} \cdot \overline{p \cdot J_1(s)} \cdot \overline{r \cdot J_{-1}(s)} \quad (4)$$

where ternary negation $\bar{x} = -x$. The static-hazard-free condition shown in Theorem 2 is also satisfied in (4). The block diagram corresponding to (4) is shown in Fig. 2. This circuit implementation is possible by the use of ternary NAND gates (ternary TTL's) presented in [6].

Proof: Using De Morgan's theorem [9], $T(p,q,r;s)$ in (2) becomes as follows:

$$T(p,q,r;s) = \overline{\overline{(p + h_1(s)) \cdot q \cdot (r + h_{-1}(s))} \cdot \overline{p \cdot J_1(s)} \cdot \overline{r \cdot J_{-1}(s)}} = \overline{\overline{p \cdot h_1(s)} \cdot q \cdot \overline{r \cdot h_{-1}(s)} \cdot \overline{p \cdot J_1(s)} \cdot \overline{r \cdot J_{-1}(s)}}. \quad (5)$$

Since $\overline{h_1(s)} = J_1(s)$ and $\overline{h_{-1}(s)} = J_{-1}(s)$, it is verified that (5) and (4) are identical. Obviously, the static-hazard-free condition will also hold in (4), because (5) is derived by the use of only De Morgan's theorem. Q.E.D.

B. Current Mode Circuit for Static-Hazard-Free T-Gate

In a current mode circuit, the saturation of the transistors is prevented to avoid delay caused by the storage effect. The major advantage of this group of digital circuits [also called emitter coupled logic (ECL)] is therefore its short propagation delay.

Fig. 3 shows the current mode circuit of the T-gate realized on the basis of the block diagram of Fig. 1. In designing a ternary ECL circuit, our attention must be turned to level shifting. Let the truth values "1," "0" and "-1" correspond to the voltages $2V_d$, 0, $-2V_d$, respectively. The voltage V_d is denoted as the forward voltage drop of the base-emitter diode of a transistor. The circuit is designed so that the operating point of the diodes is set at $V_d = 0.7$ V. The threshold voltage between "1" and "0" is set at V_d and the threshold voltage between "0" and "-1" is set at $-V_d$. These voltages V_d and $-V_d$ are generated at the points J and K in Fig. 3, respectively.

When the positive pulse "1" is applied to the control terminal s, causing Tr_1 to turn ON, the voltages of the points A and B, V_A and V_B will be $2V_d$ and $6V_d$, respectively. If the control terminal s becomes "0" or "-1," causing Tr_2 to turn ON, the voltages V_A and V_B become $6V_d$ and $2V_d$, respectively. Since the emitter of Tr_5 is connected with the emitter of Tr_3 through the level shift diodes D_1–D_4, this performs the operation of a wired OR function. Consequently, it can be seen that the voltages V_C and V_D correspond to $r + h_1(s)$ and $J_1(s)$, respectively. Similarly, the voltages V_E and V_F correspond to $r + h_{-1}(s)$ and $J_{-1}(s)$, respectively. All the transistors Tr_6, Tr_{12}, and Tr_{13} perform multiemitter AND functions; hence, the voltages V_G, V_H, and V_I are $p \cdot J_1(s)$, $r \cdot J_{-1}(s)$, and $(p + h_1(s)) \cdot q \cdot (r + h_{-1}(s))$, respectively. Now assume that one of the base voltages of Tr_{17}, Tr_{18}, and Tr_{19} is at the level "1." Under this condition, the transistor Tr_{20} remains OFF and V_L is equal to $5V_d$. When all the base voltages of Tr_{17}, Tr_{18}, and Tr_{19} are either "0" or "-1," Tr_{20} is turned ON and the voltage V_L goes to V_d. In the case where one of the base voltages of Tr_{21}, Tr_{22}, and Tr_{23} is either "1" or "0," the transistor Tr_{24} remains OFF and the voltage V_M is equal to $3V_d$. When all the base voltages of Tr_{21}, Tr_{22}, and Tr_{23} become "-1," the transistor Tr_{24} is turned ON and the voltage V_M goes to V_d. Since the voltages V_L and V_M are inputs of the emitter-follower OR circuit consisting of Tr_{25} and Tr_{26}, the circuit realized by Tr_{17}–Tr_{26} and D_{17}–D_{23} performs the operation of a ternary OR circuit. Therefore, T_{out} is verified to be $(p + h_1(s)) \cdot q \cdot (r + h_{-1}(s)) + p \cdot J_1(s) + r \cdot J_{-1}(s)$.

The T-gate thus obtained has an ability to restore the proper voltage level for all the inputs of p, q, r, and s. Fig.

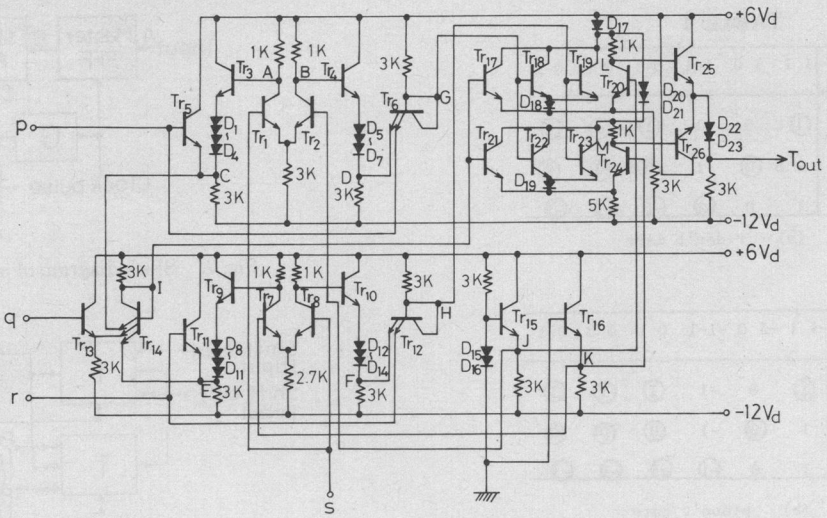


Fig. 3. ECL circuit for the static-hazard-free T-gate.

4(a) shows a characteristic of the T-gate which corresponds to the expansion of (1). It can clearly be seen that a static hazard exists in the change of a control signal s. However, as shown in Fig. 4(b), the current mode circuit of the T-gate which corresponds to the expansion of (2) is static hazard-free for the change of a control signal s.

III. Memory Elements

Ternary memory elements can easily be constructed by using the T-gates shown in Figs. 1 and 2 as building blocks. In this section, several types of memory elements which are useful for constructing a ternary digital system are presented.

A. The D-FFF

First, let us adopt the symbol of Fig. 5(a) for T-gate [3]. If the clock pulse of "1" is applied to the D-FFF of Fig. 5(b), then the output of D-FFF, T_{out} goes to the same state as the input signal D. As soon as the clock pulse CP returns to "0," the input signal D will be stored with the output T_{out} fed back into the terminal q. When the negative pulse "-1" is applied to the D-FFF, the output T_{out} is put into the state at the preset input which is given as a constant value in $L = \{1,0,-1\}$.

Table I shows the excitation of T_{out} in D-FFF. For example, assume that the present state is in A and the input p is "1." First, the clock pulse of "1" is applied and causes D-FFF to change its state from A to B. Since B is the unstable state, it changes into the stable state C immediately. When CP becomes "0" again, the state changes into the stable state D. Thus the state transition from A to D can be done, and as long as CP equals "0," the output T_{out} remains "1" regardless of the value p.

In this excitation table, the transition from $CP = 1$ to $CP = 0$ has to be considered carefully. In this transient time, if p equals q, there must not exist the static hazard for the change of the clock pulse CP. As described in Theorem 2, this static-hazard-free condition is satisfied and the operation of D-FFF is assured. Furthermore, it can be seen that an analogous behavior exists for the transition from $CP = -1$ to $CP = 0$.

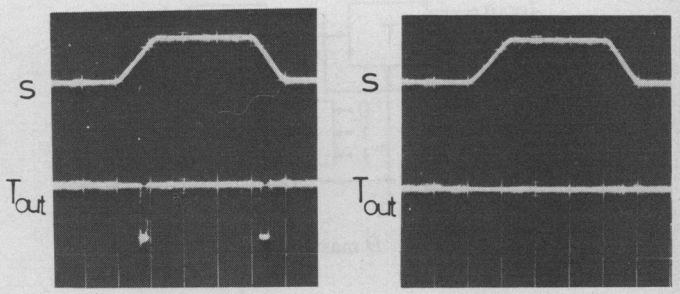


Fig. 4. (a) Input and output waveforms of the T-gate corresponding to the expansion of $p \cdot J_1(s) + q \cdot J_0(s) + r \cdot J_{-1}(s)$. (b) Input and output waveforms of the T-gate corresponding to the expansion of $(p + h_1(s)) \cdot q \cdot (r + h_{-1}(s)) + p \cdot J_1(s) + r \cdot J_{-1}(s)$.

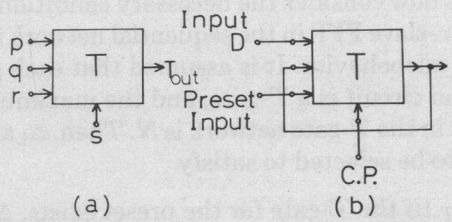


Fig. 5. (a) Symbol of T-gate. (b) D–FFF.

B. D Master–Slave FFF

Two D-FFF's can be combined into a D master–slave FFF as shown in Fig. 6. This construction seems to be conceptually the same as the master–slave FFF which is presented by Vranesic *et al.* [10]. When the clock pulse of "1" is applied to D master–slave FFF, the master responds to the input signal. The slave is disconnected from the master at this time, so the value of the output of the slave may not change while the master is responding to the input

TABLE I

C.P.,p / q	1 1	1 0	1-1	0 1	0 0	0-1
1	①C	0	-1	①D	①	①
0	1 B	⓪	-1	⓪A	⓪	⓪
-1	1	0	⓪	⓪	⓪	⓪

(a) r:don't care

C.P.,r / q	-1 1	-1 0	-1-1	0 1	0 0	0-1
1	①	0	-1	①	①	①
0	1	⓪	-1	⓪	⓪	⓪
-1	1	0	⓪	⓪	⓪	⓪

(b) p:don't care

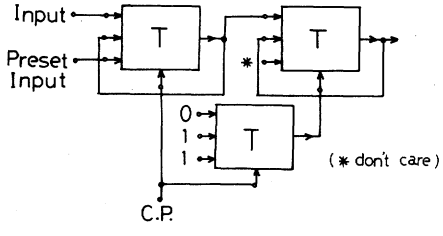


Fig. 6. *D* master–slave FFF.

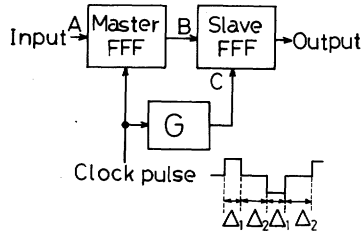


Fig. 7. Block diagram of a master–slave FFF.

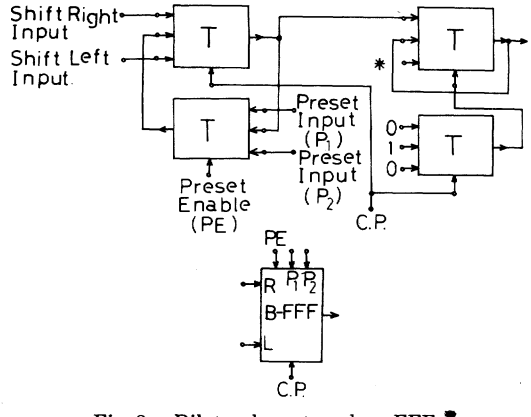


Fig. 8. Bilateral master–slave FFF.

signal. Then if CP returns to "0," the master is disconnected from the external input signal and "1," "0" or "−1" stored by the master is transferred into the slave. In the case where CP of "−1" is applied, the master and the slave simultaneously respond to the preset input which is given as a constant value in L.

Let us now consider the necessary condition where the D master–slave FFF in the sequential network is operated without misbehavior. It is assumed that each gate in the excitation circuit is a T-gate, and the maximum number of stages in the T-gate network is N. Then, Δ_1 and Δ_2 (Fig. 7) have to be selected to satisfy

$$\Delta_1 > \Delta_T \text{ (if the } T\text{-gate for the preset exists, } \Delta_1 > 2\Delta_T)$$

$$\Delta_2 > \Delta + (N+1)\Delta_T \tag{6}$$

where Δ_T and Δ are the delay time of T-gate and G, respectively.

In order to avoid the critical racing in the transient of CP, the input B in Fig. 7 must not change its value, until the input C has completely gone to "0." Thus,

$$\Delta_T > \Delta. \tag{7}$$

Therefore, the delay time of the gate G must be less than that of the ordinary T-gate, where the gate G in Fig. 7 corresponds to the T-gate $T(0,1,1;\text{CP})$ in Fig. 6. In order to satisfy this condition, it is better to implement the gate G as a unary function which is a function of one variable.

C. B Master–Slave FFF for Bilateral Ternary Shift Register

A bilateral master–slave FFF (B master–slave FFF) can be constructed by using four T-gates as shown in Fig. 8. First let us consider the case where PE (preset enable) is "0." On the arrival of the clock pulse of "1," the master responds to the shift right input (usually the output of the FFF of the previous stage). On the other hand, the clock pulse of "−1" causes the master to respond to the shift left input (usually the output of the FFF of the next stage). Thus, the circuitry of left and right shifting can be realized. However, as long as PE equals "0," the FFF cannot be preset to an arbitrary initial state. Let PE be "1" when CP equals "0." This time the master and the slave respond to the preset input P_1. Similarly, if PE becomes "−1" when CP is "0," then the master and slave respond to the preset input P_2. Thus the FFF can be preset to either of two arbitrary initial states when the clock pulse remains at "0."

The necessary condition is omitted where the B master–slave FFF in the sequential network is operated without misbehavior.

D. Counting FFF

A counting FFF (C–FFF) is a single input memory element with the state transition of Table II. The next state S' is the signed ternary sum of the present input I and the present state S. The present output C becomes the signed ternary carry of the present input I and the present state S. From this state transition table, the expressions for S' and C can be written as follows:

TABLE II

Present state S	Next state S'			Present output C		
	I = 1	I = 0	I =-1	I = 1	I = 0	I =-1
1	-1	1	0	1	0	0
0	1	0	-1	0	0	0
-1	0	-1	1	0	0	-1

$$S' = T(T(-1,1,0;S),S,T(0,-1,1;S);I)$$
$$C = T(T(1,0,0;I),0,T(0,0,-1;I);S). \quad (8)$$

This equation can be obtained by using a method presented in [7].

Fig. 9 shows that a C-FFF can be realized by B master–slave construction. When the logic level "1" or "−1" is somewhat greater than the level shifting voltage of diodes, then $T(1,0,0;I)$ and $T(0,0,-1;I)$ can be replaced by a simple limiter circuit using diodes and resistances.

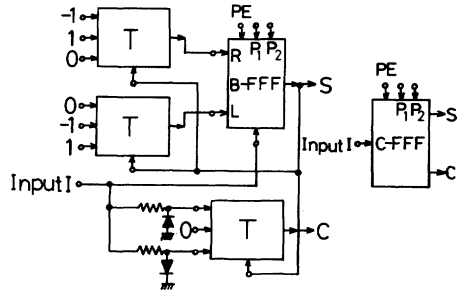


Fig. 9. Counting FFF.

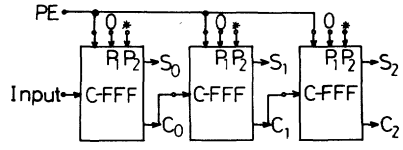


Fig. 10. Asynchronous signed ternary counter with three stages of C–FFF's.

IV. Ternary Counters

A counter is a sequential digital device that generates logic signals which can be interpreted as successive numbers. It is essentially a logic device representing numbers based on some code. In this section, ternary counters are classified into three categories, i.e., asynchronous counters, synchronous counters and counters based on shift registers which are very popular in the binary logic system. Let us assume some basic matters that are required for ternary counters.

1) The counting pulse is the return-to-zero (RZ) one. Otherwise, it must be transformed into the return-to-zero pulse by some logical operation.

2) A positive pulse "1" is counted in the up direction, and a negative pulse "−1" is counted in the down direction.

A. Asynchronous Signed Ternary Counter using C-FFF's

1) Basic Signed Ternary Counter: As it stands, a single C-FFF is a signed ternary counter capable of counting up to ±1. If positive pulses "1" are applied to the CP terminal, the counter output C generates one positive pulse every third positive pulse. On the other hand, if the negative pulses "−1" are applied into the CP terminal, the counter output C generates one negative pulse every third negative pulse. Thus, by induction it can be seen that pulses up to $\pm(3^N - 1)/2$ can be counted by the cascade chain of N stage C-FFF's. The counted result is represented by the signed ternary number representation $\Sigma_{i=0}^{N-1} S_i \cdot 3^i$, where S_i denotes the state of the $(i+1)$th C-FFF from the left-hand end. Fig. 10 shows the signed ternary counter realized by the cascade chain of three C-FFF's. The practical operating waveforms are shown in Figs. 11 and 12 by using a four channel synchroscope.

2) Symmetrical Modulo-M Counter: Let us define that a symmetrical modulo-M counter can count not only by numbers M but also by numbers $-M$. Furthermore, a 931 weighted code for ternary coded decimal is again being used. To accomplish this type of counters using C-FFF's, it is necessary to employ feedback into the PE terminal in the correct manner. A decoding circuit can be used to detect the $\pm M$ counts and all C-FFF's are preset into "0." For an example, a symmetrical modulo-10 counter can be designed as shown in Fig. 13. The decoder function detecting ±10 is given in (9) [7]:

$$T(T(0,T(1,0,0;S_2),0;S_1),0,T(0,T(0,0,1;S_2),0;S_1);S_0). \quad (9)$$

If the counter content becomes either "1 0 1" or "−1 0 −1" represented by the signed ternary number, PE terminals of C-FFF's are directly cleared to "0."

B. Synchronous Signed Ternary Counter

All FFF's are clocked at the same time in the synchronous counter. B-FFF's can be used to accomplish up–down counting in a single line. Combinational logic circuits are required to control B-FFF state changes at both the right shift input and the left shift input. The counter in Fig. 14 provides the operation of the symmetrical modulo-10 counter in the synchronous mode. According to the operation of the symmetrical modulo-10 counter, the state transition table can be expressed as shown in Table III. If up counting is done, the operation is determined by the outputs of the combinational circuits applied to the right shift inputs. If down counting is done, the operation is determined by the outputs of the combinational circuits applied to the left shift inputs. Thus, the combinational circuits applied to the right and left shift inputs can be separately designed.

C. Counter Based on Shift Register

1) General Synthesis of a Feedback Shift Register for the Counter: An N-stage bilateral ternary feedback shift register (FSR) for the counter is the highly structured sequential circuit shown in Fig. 15. Since the counted pulse

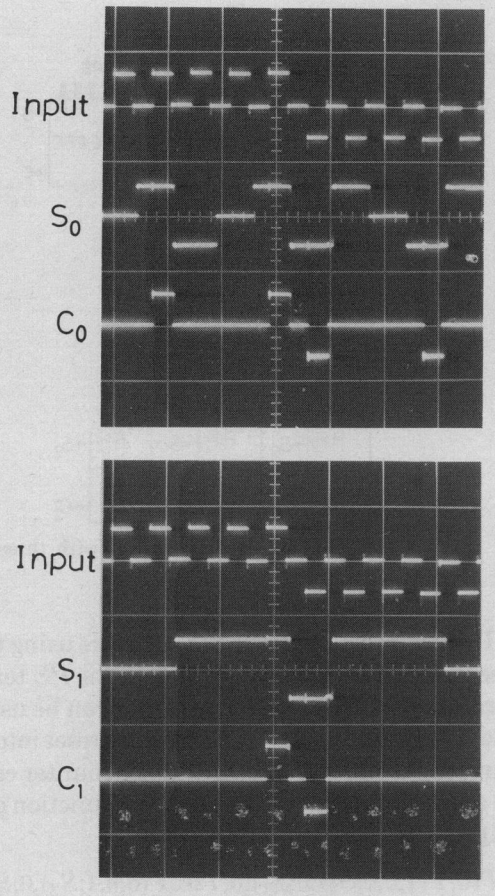


Fig. 11. Input and output waveforms of an asynchronous signed ternary counter (positive number).

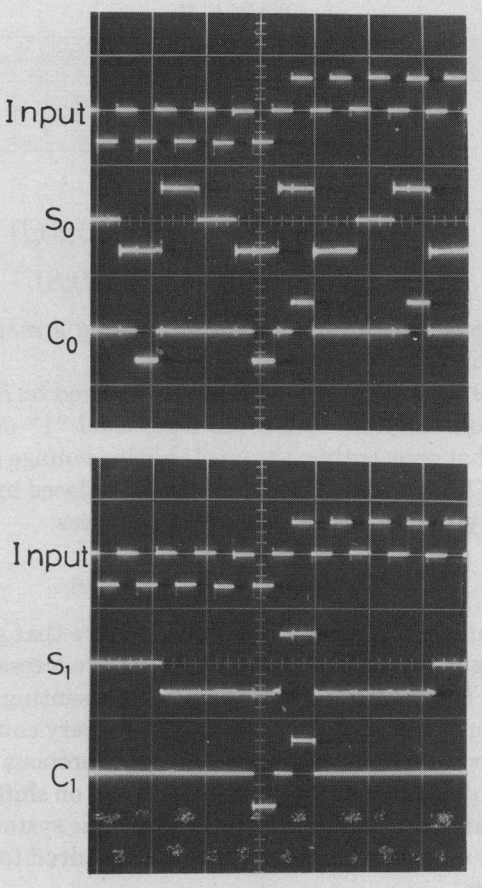


Fig. 12. Input and output waveforms of an asynchronous signed ternary counter (negative number).

is applied to the CP terminals of B-FFF's, the external inputs at the combinational circuits do not appear in Fig. 15. If up counting is done, i.e., right shift operation is performed, the combinational circuit f can affect only the excitation of stage 1, while the remaining stages are excited by the states of the previous stage; hence the memory excitation equations are

$$q_1' = f(q_1, q_2, \cdots, q_N)$$
$$q_i' = q_{i-1} \qquad (i = 2,3,\cdots,N) \tag{10}$$

where q_i' represents the next state of the state q_i.

Similarly, if down counting is done, i.e., left shift operation is performed, the memory excitation equations are

$$q_N' = g(q_1, q_2, \cdots, q_N)$$
$$q_{i-1}' = q_i \qquad (i = 2,3,\cdots,N). \tag{11}$$

Since we assume the counter consisting of an N stage shift register, there must be an N state-partitions $p(q_i)(i = 1,2,\cdots,N)$ similar to the case of binary logic [11]. The states of the sets of memory elements define a 3^N-state sequential machine, in which each state is assigned a unique ternary code, hence

$$\prod_{i=1}^{N} p(q_i) = \{0\}, \qquad \text{where } \{0\} \text{ is the 0-partition.} \tag{12}$$

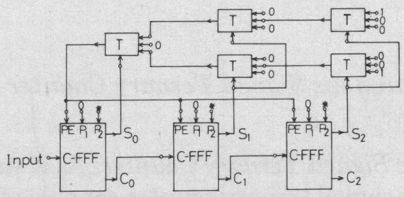


Fig. 13. Symmetrical modulo-10 counter in the asynchronous mode.

Suppose the up counter with transition matrix A is realized as an FSR. Let us write $pA = p'$ where p' is the partition on the next states of the counter induced by the partition p on the present states.

$$p(q_{i-1})A = p(q_i) \qquad (i = 2,3,\cdots,N). \tag{13}$$

If uth power transition matrix is indicated as $A^{(u)}$, then it follows that

$$p(q_1)A^{(u)} = p(q_{1+u}) \qquad (u = 1,2,\cdots,N-1). \tag{14}$$

Equation (14) indicates that if an appropriate state partition $p(q_1)$ is selected for the counter, then the remaining state partitions can be determined.

Since the counter in question is a permutation machine, $A^{(-1)}$ which is the inverse of the transition matrix A, always

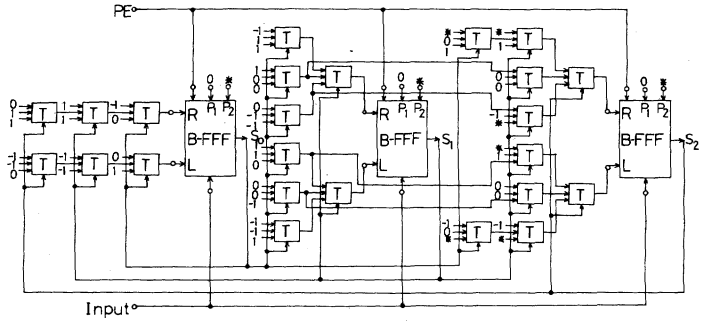


Fig. 14. Symmetrical modulo-10 counter in the synchronous mode.

TABLE III

Present state $S_2S_1S_0$	Next state ($C_P = -1$ (down count))	Next state ($C_P = 1$ (up count))
-1 0 0	0 0 0	-1 0 1
-1 0 1	-1 0 0	-1 1-1
-1 1-1	-1 0 1	-1 1 0
-1 1 0	-1 1-1	-1 1 1
-1 1 1	-1 1 0	0-1-1
0-1-1	-1 1 1	0-1 0
0-1 0	0-1-1	0-1 1
0-1 1	0-1 0	0 0-1
0 0-1	0-1 1	0 0 0
0 0 0	0 0-1	0 0 1
0 0 1	0 0 0	0 1-1
0 1-1	0 0 1	0 1 0
0 1 0	0 1-1	0 1 1
0 1 1	0 1 0	1-1-1
1-1-1	0 1 1	1-1 0
1-1 0	1-1-1	1-1 1
1-1 1	1-1 0	1 0-1
1 0-1	1-1 1	1 0 0
1 0 0	1 0-1	0 0 0

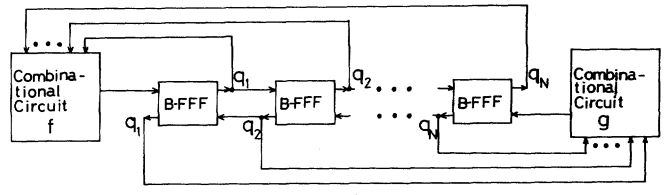


Fig. 15. Configuration of the bilateral ternary feedback shift register.

TABLE IV

State	q_1	q_2	q_3
0	-1	0	0
1	0	-1	0
2	0	0	-1
3	1	0	0
4	0	1	0
5	0	0	1

exists. By rewriting (13) and (14)

$$p(q_i)A^{(-1)} = p(q_{i-1}) \tag{15}$$

$$p(q_N)A^{(-u)} = p(q_{N-u}) \qquad (u = 1,2,\cdots,N-1). \tag{16}$$

Equations (15) and (16) indicate that down counting is carried out by the left shifting in the configuration of Fig. 15. Now let the present states PS be $(q_1,q_2,\cdots,q_N)$. By the right shifting, the next states will be

$$NS = (f(q_1,q_2,\cdots,q_N), q_1,q_2,\cdots,q_{N-1}). \tag{17}$$

Furthermore, if the left shifting is done on these states, the states will be PS again; hence

$$PS = (q_1,q_2,\cdots,q_{N-1}, g(f(q_1,q_2,\cdots,q_N), q_1,q_2,\cdots,q_{N-1})). \tag{18}$$

Therefore, the following relationship must be satisfied for all the values of $q_1,\cdots,q_N$ between the function f and g.

$$g(f(q_1,q_2,\cdots,q_N), q_1,\cdots,q_{N-1}) = q_N. \tag{19}$$

Particularly in the case where f is a unary function of q_N and g is a unary function of q_1,

$$g(f(q_N)) = q_N. \tag{20}$$

2) *One-of-N Counter:* A one-of-N counter, or a ring counter consists of N stages of B master–slave FFF's operating such that one and only one of FFF's is "1" or "−1" at a particular time. Let us design a mod-6 up–down counter. In respect to the up counting, the following partitions are obtained using (14)

$$p(q_1) = \left\{\frac{-1}{0};\frac{0}{1,2,4,5};\frac{1}{3}\right\}$$

$$p(q_2) = \left\{\frac{-1}{1};\frac{0}{2,3,5,0};\frac{1}{4}\right\}$$

$$p(q_3) = \left\{\frac{-1}{2};\frac{0}{3,4,0,1};\frac{1}{5}\right\}.$$

Since $p(q_1)\cdot p(q_2)\cdot p(q_3) = \{0\}$, the state assignment is uniquely determined as shown in Table IV. From this state transition table, the feedback function f becomes $q_1' = T(-1,0,1;q_3)$. Using (20), the feedback function g can also be obtained as $q_3' = T(-1,0,1;q_1)$. Thus, a one-of-N counter with three stages of B-FFF's is designed as shown in Fig. 16. These practical operating waveforms are shown in Fig. 17 (each q_i corresponds to the output F_{i-1} of the ith stage FFF).

Generally, a one-of-N counter consists of a circulating shift register with the output of the Nth stage FFF connected to the input of the first stage FFF through a ternary negation [1]. Before starting to count, only the left-hand end FFF of the register is preset to "−1," and the other FFF's are preset to "0." Each time the counted pulse becomes "1," this "−1" or "1" is shifted to the right. As to down counting, this "−1" or "1" is shifted to the left, so that the left-hand end FFF of the register is connected to

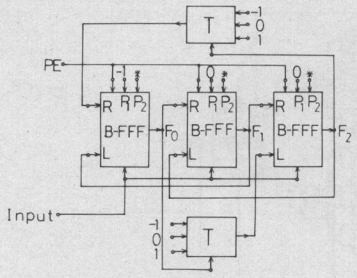
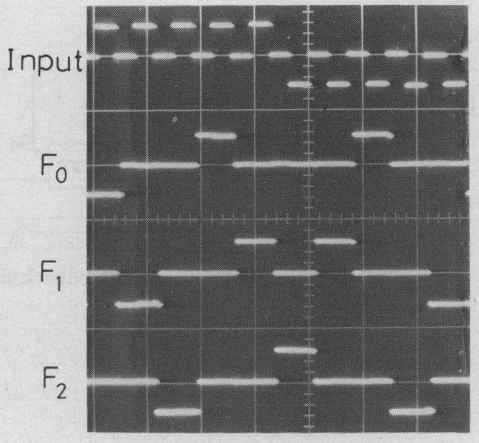


Fig. 16. One-of-N counter.



50 μsec/div., 5 V/div.

Fig. 17. Input and output waveforms of the one-of-N counter.

the right-hand end FFF of the register through a ternary negation. The advantage of a one-of-N counter is that it does not require decoding in order to obtain separate signal outputs for each number. The decoding output for the count n is given as $F_n \pmod N$. It is possible to use this as a ternary multiplex switch.

3) Switch Ring Counter: Let us design a mod-9 up–down counter. If the following $p(q_1)$ is taken as the first partition, then the partitions $p(q_2)$ and $p(q_3)$ can be obtained using (14) as

$$p(q_1) = \left\{\frac{-1}{4,5,6}; \frac{0}{7,8,0}; \frac{1}{1,2,3}\right\}$$

$$p(q_2) = \left\{\frac{-1}{5,6,7}; \frac{0}{8,0,1}; \frac{1}{2,3,4}\right\}$$

$$p(q_3) = \left\{\frac{-1}{6,7,8}; \frac{0}{0,1,2}; \frac{1}{3,4,5}\right\}.$$

Since $p(q_1) \cdot p(q_2) \cdot p(q_3) = \{0\}$, the state assignment is uniquely determined as shown in Table V. As a result, the feedback function f becomes as $q_1' = T(-1,1,0;q_3)$. Using (20) the feedback function g can also be obtained as $q_3' = T(0,-1,1;q_1)$. Thus, a switch ring counter can be realized as shown in Fig. 18. The practical operating waveforms are obtained in Fig. 19.

Generally, a switch ring counter can be realized such as below. If the right shift is done, then the output of the rightmost FFF is connected to the input of the leftmost FFF through a cycling gate [1], where a cycling gate is defined as $x \oplus 1 \pmod 3$ for the input x. If the left shift is done, then the output of the leftmost FFF is connected back to the rightmost FFF through a double-cycling gate, where a double-cycling gate is defined as $x \oplus -1 \pmod 3$ for the input x. By starting with the FFF's cleared to "0," this counter with N stages can represent $3N$ values. A switch ring counter is three-halves as efficient as a one-of-N counter, however, decoding is required to obtain a separate logic output for each number. But, the decoding is simple because only a two input ternary function is required for each. The decoding inputs for the count n are given as F_{n-1} and $F_n \pmod N$.

TABLE V

State	q_1	q_2	q_3
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	−1	1	1
5	−1	−1	1
6	−1	−1	−1
7	0	−1	−1
8	0	0	−1

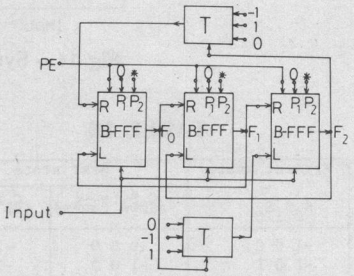
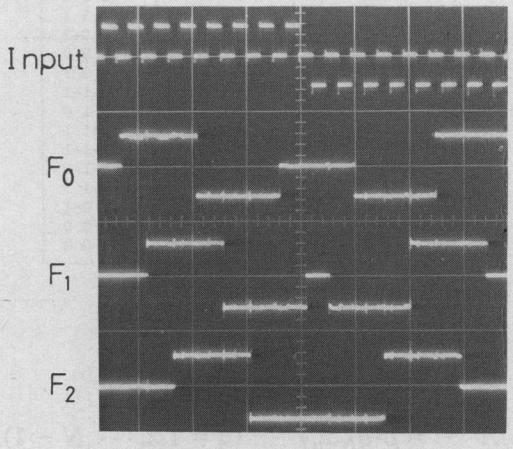


Fig. 18. Switch ring counter.



50 μsec/div., 5 V/div.

Fig. 19. Input and output waveforms of the switch ring counter.

V. Conclusion

The theoretical and experimental considerations are presented for the ternary T-gate as a static-hazard-free memory element. The memory elements are operated with the ternary clock pulse, which leads to the reduction of the number of input and output terminals. The ternary counter realized using T-gates are superior to the binary ones in that up–down counting can easily be carried out

by only one input signal. The ternary logic system can be constructed by using such T-gates as basic building blocks. It is expected that the T-gates are applied in ternary sequence generators and system control circuits.

The T-gate network will be important with the potentialities of the integrated circuit. Therefore, the development of the circuit aspects with high speed and reliability will be hoped for in the future. However, a number of transistors are required to realize a ternary digital system using T-gates. For example, a binary ECL T-gate [12] contains 33 elements (16 transistors, 2 diodes and 14 resistors), while a ternary ECL T-gate presented here requires 71 elements (26 transistors, 23 diodes and 22 resistors). Though this matter is a disadvantage from the point of view of the high density integration, the concept of T-gate is very useful for the notation of a logical function and simplifies the synthesis problem.

Acknowledgment

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