A 32×32-bit Multiplier Using Multiple-Valued MOS Current-Mode Circuits

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A 32×32-bit Multiplier Using Multiple-Valued MOS Current-Mode Circuits

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Abstract—A 32×32-bit multiplier using multiple-valued current-mode circuits has been fabricated in 2-μm CMOS technology. For the multiplier based on the radix-4 signed-digit (SD) number system, 32×32-bit two's complement multiplication can be performed with only three-stage SD full adders (SDFA's) using a binary-tree addition scheme.

The chip contains about 23 600 transistors and the effective multiplier size is about 3.2×5.2 mm², which is half that of the corresponding binary CMOS multiplier. The multiply time is less than 59 ns. The performance is comparable to that of the fastest binary multiplier reported.

I. Introduction

IT IS well known that multiple-valued logic (MVL) is a very attractive approach for ULSI or wafer-scale integration (WSI) because of the reduction of interconnection complexity and the number of active devices [1]. Recently, the advantage of MVL has been confirmed in various applications such as memories, image processors, arithmetic circuits, and so on [2]–[5]. However, very few LSI chips based on MVL have been fabricated. This paper describes new LSI-oriented multiple-valued CMOS current-mode circuits and the practical implementation of a 32×32-bit multiple-valued multiplier chip based on the radix-4 signed-digit (SD) number system [6].

In the SD number representation, carry propagation during addition and subtraction is always limited to one position to the left. This property of the number system is useful not only for addition but also for multiplication. Since multiple-valued coding is direct for the representation of the signed digit, the arithmetic circuits can be implemented very compactly by the use of multiple-valued circuits [7]. In particular, the multiple-valued bidirectional current-mode circuits proposed here are quite suitable for the implementation of SD arithmetic because the linear summation including polarity can be performed by simple wiring [5]. This property enables the interconnection complexity to be greatly reduced and the resulting arithmetic LSI circuits to be very compact.

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A 32×32-bit multiplier LSI with binary input and output has been designed using multiple-valued current-mode circuits and implemented in 2-μm CMOS technology. The multiplier, based on the radix-4 SD number system, is realized by a regular array structure using a three-stage binary-tree scheme [8], [9]. New hardware algorithms for a partial-product generation and an SD-to-binary conversion technique have also been developed for a high-speed compact multiplier. It is confirmed that the multiple-valued multiplier based on the SD number system is totally superior to the fastest binary multiplier [10] in terms of speed, power dissipation, and chip area.

II. Bidirectional Current-Mode Circuits

The most important concept of multiple-valued current-mode circuits is that of wired summation as introduced by Dao *et al.* with multiple-valued integrated injection logic [11]. However, such "single-directional" current-mode circuits are not always suitable for the implementation of arithmetic circuits based on a sign-symmetrical number representation such as the SD number system. The bidirectional current-mode circuits proposed here are essentially suitable for the implementation of SD arithmetic and facilitate wired summation including polarity. Fig. 1 illustrates the principle of bidirectional wired summation. From Kirchhoff's current law, the current z is equal to the sum of the two currents x and y. The current z is applied to successive bidirectional current-mode circuits, where polarity and current levels are detected and arithmetic operations are performed using several basic circuits. Fig. 2 provides a summary of available basic bidirectional current-mode circuits.

Fig. 3(a) shows a current source using a p-channel depletion-mode MOSFET. In the ideal case, the saturation value of the drain current I_d used as a constant current is written as

$$I_d = K(W/L)(V_T)^2 \tag{1}$$

where K, W, L, and V_T are, respectively, the transconductance parameter, the channel width, the channel length,

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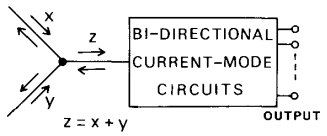


Fig. 1. Bidirectional wired summation.

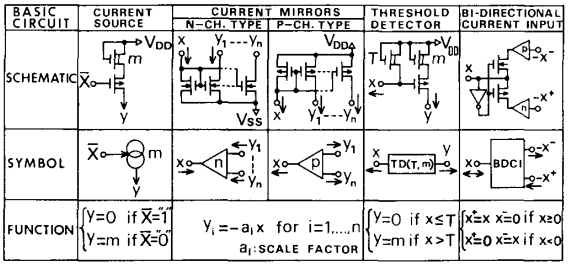


Fig. 2. Basic bidirectional current-mode circuits.

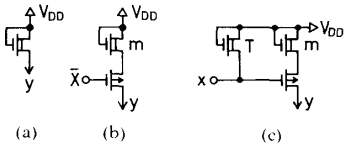


Fig. 3. Current sources and the threshold detector. (a) Current source. (b) Voltage-switched current source. (c) Threshold detector.

and the threshold voltage of the p-channel depletion-mode MOSFET. The unit current can be set at the specified value using dose control. This type of current source is quite insensitive to the fluctuation of the supply voltage V_{DD}, and requires no bias source or connection other than V_{DD}.

A voltage-switched current source can easily be implemented using a p-channel enhancement-mode MOSFET together with the current source as shown in Fig. 3(b). Using these current sources, a threshold detector can be constructed as shown in Fig. 3(c) [11], [12]. The function is given by

$$\left.\begin{aligned} y &= 0, \quad \text{if } x < T \\ y &= m, \quad \text{if } x \geq T \end{aligned}\right\} \tag{2}$$

where TI_a and mI_a are the threshold and the output currents, respectively, and I_a is a unit current. This threshold detector is denoted by $TD(T, m)$.

In the bidirectional current-mode circuits, a current mirror is used for three purposes. One is to invert the current direction, another is to produce replicas of an input current, and the other is the scaling of the input current. There are two types of current mirrors: NMOS and PMOS.

The polarity of the bidirectional current can be detected by a bidirectional current input circuit (BDCI) shown in Fig. 4(a). Let the current injected from V_{DD} through the current source x be defined positive, while the current flowing into the ground through the output of the NMOS current mirror y be defined negative. z is the current

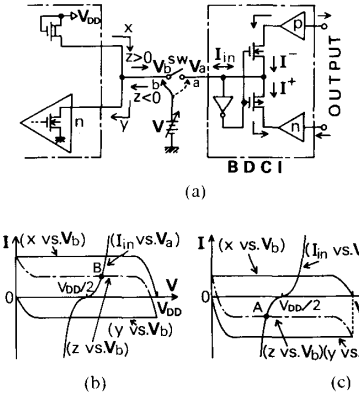


Fig. 4. Bidirectional current input circuits. (a) Schematic. (b) $I-V$ characteristics for $z > 0$. (c) $I-V$ characteristics for $z < 0$.

obtained from the wired summation of x and y. If x is greater than the absolute value of y ($|y|$), z is positive, while if x is less than $|y|$, z is negative. In case of $x = |y|$, z becomes zero. Fig. 4(b) and (c) shows the $I-V$ characteristics of x, y, and z in the cases of $z > 0$ and $z < 0$, respectively, when the switch SW is open, and a voltage source is connected to the point b. The $I-V$ characteristic of BDCI when the voltage source is connected to the point a is also shown in Fig. 4(b) and (c). The operation of BDCI is given by

$$\left.\begin{aligned} I^+ &= I, \quad I^- = 0, \quad \text{if } V > V_{DD}/2 \\ I^+ &= 0, \quad I^- = 0, \quad \text{if } V = V_{DD}/2 \\ I^+ &= 0, \quad I^- = I, \quad \text{if } V < V_{DD}/2 \end{aligned}\right\}. \tag{3}$$

When SW is closed and the voltage source is removed, the crossover points A and B will be determined as the operating points for $z > 0$ and $z < 0$, respectively. It is obvious that the positive and negative z values are equal to I^+ and I^-, respectively. Replicas of I^+ and I^- are obtained at the output of BDCI through current mirrors. Consequently, a bidirectional current can be decomposed into two single-directional currents by using BDCI.

III. Signed-Digit Arithmetic Circuits

The radix-4 SD arithmetic is used in the multiplier because of easy compatibility with the binary system and compactness of the implemented chip. The radix-4 SD number is represented by the following symmetrical digit set of seven values:

$$L = \{-3, -2, -1, 0, 1, 2, 3\}. \tag{4}$$

Any integer $X \in [-N, N]$, where $N = 4^n - 1$, can be coded as a sequence of radix-4 signed digits x_i according to

$$X = (x_{n-1} \cdots x_i \cdots x_0) = \sum_{i=0}^{n-1} x_i 4^i. \tag{5}$$

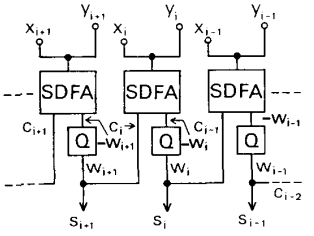


Fig. 5. Parallel SD adder.

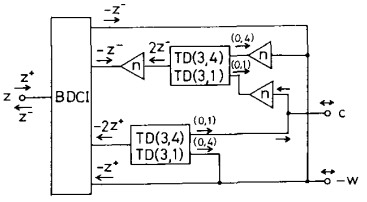


Fig. 6. Signed-digit full adder (SDFA).

In general, the number X is not uniquely coded in the SD number representation except for $X=0$. This redundancy in the number representation allows fast parallel operation.

The addition of two numbers $X=(x_{n-1}\cdots x_i\cdots x_0)$ and $Y=(y_{n-1}\cdots y_i\cdots y_0)$ is performed by the following three successive steps for each digit:

$$z_i = x_i + y_i \tag{6}$$

$$4c_i + w_i = z_i \tag{7}$$

$$s_i = w_i + c_{i-1} \tag{8}$$

where z_i is a linear sum of x_i and y_i, w_i is an intermediate sum, c_i is a carry, and

$$\left.\begin{aligned} z_i &\in \{-6,\cdots,0,\cdots,6\} \\ w_i &\in \{-2,-1,0,1,2\} \\ c_i &\in \{-1,0,1\} \end{aligned}\right\}. \tag{9}$$

It is obvious that $s_i \in L$. The final sum s_i can be obtained almost in parallel and the addition speed is independent of the word length.

Fig. 5 shows the parallel SD adder based on the bidirectional current-mode circuits. The addition steps of (6) and (8) can be performed by bidirectional wired summation without active devices. Equation (7) can be performed by the signed-digit full adder (SDFA) shown in Fig. 5. From (7) and (9), the intermediate sum w_i and the carry c_i can be obtained as follows:

$$\left.\begin{aligned} w_i &= z_i - 4, & c_i &= 1, & &\text{if } z_i \geqslant 2 \\ w_i &= z_i\ \ , & c_i &= 0, & &\text{if } -1 \leqslant z_i \leqslant 1 \\ w_i &= z_i + 4, & c_i &= -1, & &\text{if } z_i \leqslant -2 \end{aligned}\right\}. \tag{10}$$

From (10), the SDFA can be constructed by using the basic circuits of Fig. 2 and bidirectional wired summation as shown in Fig. 6. The SDFA is composed of 26 transistors. For the improvement of speed and dc characteristics, it is useful to reduce the number of cascaded current mirrors in the SDFA. One solution is to retain the intermediate sum w_i in inverted form.

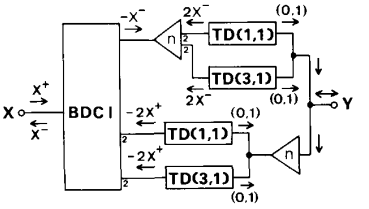


Fig. 7. Inverted quantizer with dynamic range from -2 to 2.

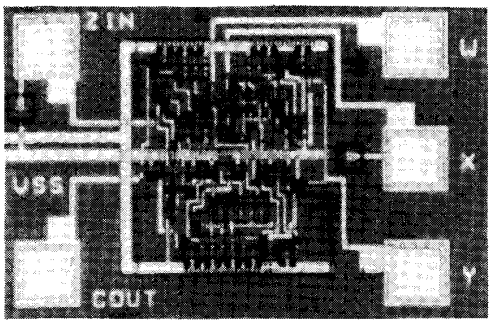


Fig. 8. Photomicrograph of the SDFA with the inverted quantizer.

In general, signal levels must be restored before their complete degradation. While the carry c_i is quantized by the threshold detector, the intermediate sum w_i is not quantized by the circuit of Fig. 6. Thus an inverted quantizer is essential for the output w_i. At the same time, the specified polarity can be obtained through the inversion operation. Fig. 7 shows the inverted quantizer having a dynamic range from -2 to 2 which is also composed of 26 transistors.

Fig. 8 shows a photomicrograph of an implemented SDFA with the inverted quantizer as a test circuit. The effective size is about $140\times205\ \mu m^2$. The characteristics of the implemented circuits are shown in Fig. 9, where the unit current is approximately 31 μA with transistor sizes of $L=2.8\ \mu$m and $W=9\ \mu$m, and a threshold voltage of 1.5 V. Fig. 9(a) shows the current transfer curve for the carry of the SDFA corresponding to (7). By using the inverted quantizer whose characteristic is shown in Fig. 9(b), the current transfer curve for the intermediate sum w_i of the SDFA is quantized as shown in Fig. 9(c). The worst-case delay time of the SDFA with the inverted quantizer is measured to be about 11 ns, while the simulated value using SPICE2 is 8.9 ns.

The minimum noise margin is about 10 μA (32 percent of the unit current) from Fig. 9(c). If the statistical variation from the desired output of the current source exceeds the noise margin, logical errors will occur. The variation of the current-source output current (ΔI) is mainly caused by the variation of the threshold voltage of the transistor (ΔV_T). The variation is represented as $\Delta I=(\Delta V_T/V_T)$

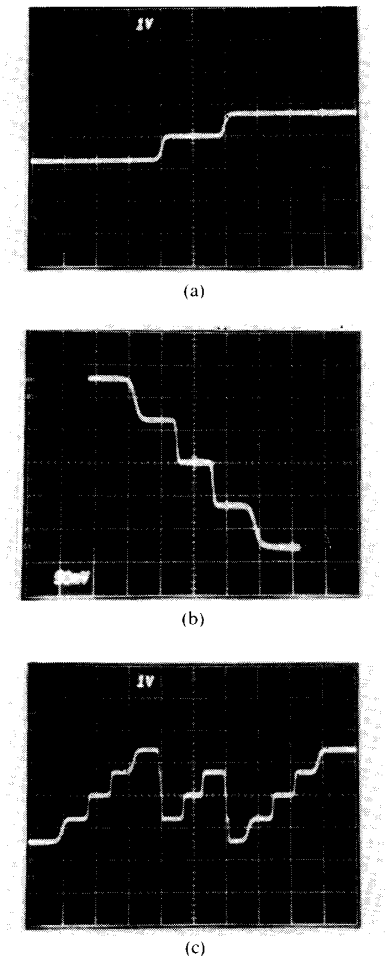


Fig. 9. Current-transfer curve of the SDFA and the inverted quantizer. (a) Carry of the SDFA—horizontal axis: input z(41 μA/div); vertical axis: carry output c(41 μA/div). (b) Inverted quantizer—horizontal axis: input x(24.4 μA/div); vertical axis: output y(24.4 μA/div). (c) Intermediate sum of the SDFA—horizontal axis: input z(41 μA/div); vertical axis: intermediate sum output (quantized) w(41 μA/div).

$\cdot(2+(\Delta V_T/V_T))I_a$. In case of $\Delta V_T = 50$ mV, $V_T = 1.5$ V, and $I_a = 31$ μA, ΔI becomes about 2 μA. This variation is not large enough to cause logical errors.

The speed is improved by the shrinking of minimum process feature sizes. However, the noise margin is decreased due to the channel-length modulation effect of the transistors used for the current source and the current mirrors. One solution for this problem is to use a special device with the reduced channel-length modulation effect. For example, a DSA MOS device will be useful [13].

IV. Multiplication Algorithm

For compatibility with the binary system, the signed-binary number (two's complement) representation is used at the input and the output of the multiplier, and the radix-4 SD number representation is used inside the multiplier. New algorithms for partial-product generation, an addition scheme, and SD-to-binary conversion are used to perform high-speed multiplication.

A. Generation of Partial Products

One of the most important techniques for the realization of a high-speed compact multiplier is to reduce the number of partial products. To reduce the number of partial products, the modified Booth's algorithm [14] is often used in binary multipliers. By the extension of the modified Booth's algorithm, a recording algorithm suitable for radix-4 SD number partial-product generation has been developed here.

Let Y be the multiplier in the n-bit two's complement number. Assume that n is a multiple of 8. The multiplier Y may be written as

$$Y = -y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} y_j 2^j \tag{11}$$

where $y_j \in \{0,1\}$. Equation (11) can be also expressed as follows:

$$\begin{aligned} Y &= (y_{n-5} + y_{n-4} + 2y_{n-3} + 4y_{n-2} - 8y_{n-1})2^{(n-4)} \\ &\quad \vdots \\ &\quad + (y_{4j-1} + y_{4j} + 2y_{4j+1} + 4y_{4j+2} - 8y_{4j+3})2^{4j} \\ &\quad \vdots \\ &\quad + (y_3 + y_4 + 2y_5 + 4y_6 - 8y_7)2^4 \\ &\quad + (y_{-1} + y_0 + 2y_1 + 4y_2 - 8y_3)2^0 \\ &= \sum_{j=0}^{n/4-1} (y_{4j-1} + y_{4j} + 2y_{4j+1} + 4y_{4j+2} - 8y_{4j+3})2^{4j} \end{aligned} \tag{12}$$

$$= \sum_{j=0}^{n/4-1} Q_j 16^j \tag{13}$$

where $y_{-1} = 0$ and $Q_j \in \{-8,\cdots,0,\cdots,8\}$ is defined as

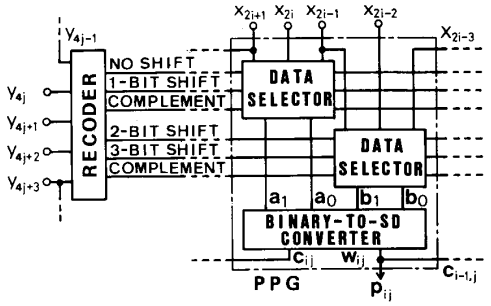
$$Q_j = (y_{4j-1} + y_{4j} + 2y_{4j+1} + 4y_{4j+2} - 8y_{4j+3}). \tag{14}$$

Consequently, the multiplier Y can be divided into $n/4$ groups, each of 5 bits. Each pair of two contiguous groups has one bit in common. Equation (13) can be rewritten as the following equation by considering two parts, one for j = odd and one for j = even:

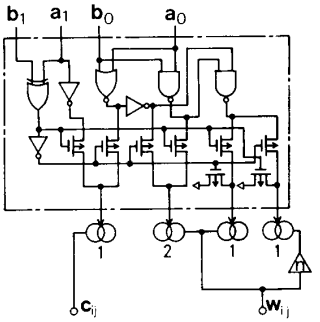
$$Y = \sum_{k=0}^{n/8-1} Q_{2k} 16^{2k} + \sum_{k=0}^{n/8-1} Q_{2k+1} 16^{2k+1}. \tag{15}$$

For the multiplicand X, the product P of X and Y can be written as

$$P = \sum_{k=0}^{n/8-1} Q_{2k} X 16^{2k} + \sum_{k=0}^{n/8-1} Q_{2k+1} X 16^{2k+1}. \tag{16}$$



(a)



(b)

Fig. 10. Partial-product generator (PPG). (a) Schematic. (b) Binary-to-SD converter.

For the reduction of the number of adder delays, the following two expressions for X are used:

$$X = -x_{n-1}2^{n-1} + \sum_{i=0}^{n-2} x_i 2^i,$$

for the product $Q_{2k}X$ (17)

$$X = \overline{x_{n-1}}2^{n-1} - \sum_{i=0}^{n-2} \overline{x_i}2^i - 1,$$

for the product $Q_{2k+1}X$ (18)

where $\overline{x_i}$ denotes the complement of x_i. Fig. 10(a) shows the partial-product generator (PPG) using the recoding algorithm. Q_j can be decomposed into an appropriately selected U_j and V_j as

$$Q_j = U_j + V_j \tag{19}$$

where $U_j \in \{-2,-1,0,1,2\}$ and $V_j \in \{-8,-4,0,4,8\}$ are given as shown in Table I. Q_jX can be written as

$$\begin{aligned} Q_jX &= U_jX + V_jX \\ &= A_j + B_j \end{aligned} \tag{20}$$

where $A_j = U_jX \in \{-2X, -X, 0, X, 2X\}$ and $B_j = V_jX \in \{-8X, -4X, 0, 4X, 8X\}$. Since the multiplicand X is represented as a two's complement binary number, the generation of A_j and B_j can be realized by shift and complement operations. The values $8X$, $4X$, and $2X$ correspond to 3-, 2-, and 1-bit left shift operations in X, respectively.

TABLE I
MAPPING FOR U_j AND V_j FROM Q_j

Q_j	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
U_j	0	1	2	-1	0	1	-2	-1	0	1	2	-1	0	1	-2	-1	0
V_j	-8	-8	-8	-4	-4	-4	0	0	0	0	0	4	4	4	8	8	8

TABLE II
MAPPING FOR EACH BIT OF A_{2k}, $a_{n,2k}$ (FOR MSB), $a_{i,2k}$ (FOR $i = 0 \cdots n-1$), AND d_{2k} (INCREMENT SIGNAL) FROM U_{2k}

U_{2k}	$a_{n,2k}$	$a_{i,2k}$	d_{2k}
2	$-x_{n-1}$	x_{i-1}	0
1	$-x_{n-1}$	x_i	0
0	0	0	0
-1	$-\overline{x_{n-1}}$	$\overline{x_i}$	1
-2	$-\overline{x_{n-1}}$	$\overline{x_{i-1}}$	1

TABLE III
MAPPING FOR EACH BIT OF A_{2k+1}, $a_{n,2k+1}$ (FOR MSB), $a_{i,2k+1}$ (FOR $i = 0 \cdots n-1$), AND d_{2k+1} (INCREMENT SIGNAL) FROM U_{2k+1}

U_{2k+1}	$a_{n,2k+1}$	$a_{i,2k+1}$	d_{2k+1}
2	$\overline{x_{n-1}}$	$-\overline{x_{i-1}}$	-1
1	$\overline{x_{n-1}}$	$-\overline{x_i}$	-1
0	0	0	0
-1	x_{n-1}	$-x_i$	0
-2	x_{n-1}	$-x_{i-1}$	0

TABLE IV
MAPPING FOR EACH BIT OF B_{2k}, $b_{n+2,2k}$ (FOR MSB), $b_{i,2k}$ (FOR $i = 0 \cdots n+1$), AND e_{2k} (INCREMENT SIGNAL) FROM V_{2k}

V_{2k}	$b_{n+2,2k}$	$b_{i,2k}$	e_{2k}
8	$-x_{n-1}$	x_{i-3}	0
4	$-x_{n-1}$	x_{i-2}	0
0	0	0	0
-4	$-\overline{x_{n-1}}$	$\overline{x_{i-2}}$	1
-8	$-\overline{x_{n-1}}$	$\overline{x_{i-3}}$	1

TABLE V
MAPPING FOR EACH BIT OF B_{2k+1}, $b_{n+2,2k+1}$ (FOR MSB), $b_{i,2k+1}$ (FOR $i = 0 \cdots n+1$), AND e_{2k+1} (INCREMENT SIGNAL) FROM V_{2k+1}

V_{2k+1}	$b_{n+2,2k+1}$	$b_{i,2k+1}$	e_{2k+1}
8	$\overline{x_{n-1}}$	$-\overline{x_{i-3}}$	-1
4	$\overline{x_{n-1}}$	$-\overline{x_{i-2}}$	-1
0	0	0	0
-4	x_{n-1}	$-x_{i-2}$	0
-8	x_{n-1}	$-x_{i-3}$	0

The value $-X$ can be obtained by first complementing the number X then adding 1 to its LSB. The shift and complement control signals are generated from the recoder which can be easily implemented by conventional CMOS gates. As a result, the shift and the complement operations in X are performed using the data selectors controlled by these signals as shown in Tables II–V. The partial product p_{ij}

corresponding to (20)

$$P_j = Q_j X = \sum_{i=0}^{n/2} p_{i,j} 4^i$$

can be generated by the following equations in the radix-4 SD number representation:

$$z_{i,j} = 2b_{2i+1,j} + b_{2i,j} + 2a_{2i+1,j} + a_{2i,j} \quad (21)$$

$$4c_{i,j} + w_{i,j} = z_{i,j} \quad (22)$$

$$p_{i,j} = w_{i,j} + c_{i-1,j}. \quad (23)$$

If $j = 2k$, $p_{i,j} \in \{-1,0,1,2,3\}$, because $z_{i,j} \in \{0,\cdots,6\}$, $c_{i,j} \in \{0,1\}$, and $w_{i,j} \in \{-1,0,1,2\}$. While, if $j = 2k+1$, $p_{i,j} \in \{-3,-2,-1,0,1\}$, because $z_{i,j} \in \{-6,\cdots,0\}$, $c_{i,j} \in \{-1,0\}$, and $w_{i,j} \in \{-2,-1,0,1\}$. For the partial-product generation for MSD, the following expression is used instead of (21):

$$z_{n/2,j} = -4b_{n+2,j} + 2b_{n+1,j} + b_{n,j} - a_{n,j} \quad (24)$$

where $z_{n/2,2k} \in \{-5,\cdots,3\}$ and $z_{n/2,2k+1} \in \{-3,\cdots,5\}$. The operations of (21) and (22) are performed by the binary-to-SD converter shown in Fig. 10(b) which can be implemented using binary CMOS gates, pass transistors, and voltage-switched current sources. Also (23) is performed by bidirectional wiring summation.

B. Addition of Partial Products

Based on the above partial-product generation, $n/4$ operands expressed as a radix-4 $(n/2+1)$-digit number are produced, where the operand is denoted by P_j (for $j = 0,\cdots,(n/4)-1$). The final product can be obtained by performing the multiple-operand addition of P_j's as follows:

$$P = \sum_{j=0}^{n/4-1} P_j 16^j. \quad (25)$$

The multiple-operand addition can be performed using two-input parallel SD adders in a binary-tree structure. For example, a 32×32-bit multiplier which contains eight operands composed of 17-digit partial products can be constructed by three-stage adders based on a binary-tree structure as shown in Fig. 11.

The linear sum $f_{i,j}$ at the input of the first-level SD adders is given by

$$f_{i,j} = p_{i,2k} + p_{i,2k+1} \quad (26)$$

where $p_{i,2k} (\in \{-1,0,1,2,3\})$ and $p_{i,2k+1} (\in \{-3,-2,-1,0,1\})$ are the partial products of the $(2k)$th and the $(2k+1)$th PPG groups, respectively, and where $f_{i,j}$ is limited to values between -4 and 4. Since the input dynamic range of the SDFA is from -6 to 6, it is possible to add the increment signals d_j and e_j together with the partial products. Unless this method is used, the input linear sum to the SDFA's exceeds its dynamic range due to the addition of d_j and e_j.

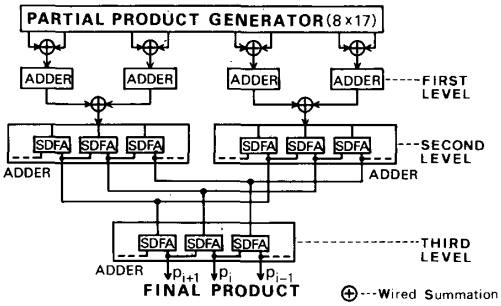


Fig. 11. Binary-tree scheme for the 32×32-bit multiplication.

Fig. 12 shows the example of 8×4-bit multiplication using the proposed algorithm, where the multiplicand $X = (1011)_2$ and the multiplier $Y = (00101010)_2$ in the two's complement form. The final product P $(= -4^4 + 3\times4^2 - 2\times4^0 = -210)$ of X $(= -2^3 + 2^1 + 2^0 = -5)$ and Y $(= 2^5 + 2^3 + 2^1 = 42)$ can be obtained with a single-level SD adder.

Generally, addition in the m-operand adder based on the binary-free scheme is performed with l-stage SDFA's where

$$l = \lfloor \log_2 m \rfloor \quad (27)$$

and $\lfloor x \rfloor$ denotes the smallest integer such that $\lfloor x \rfloor > x$. In the $n \times n$-bit multiplier, the number of partial products of m-operands expressed as radix-4 SD numbers becomes $n/4$ using the above recoding algorithm. Therefore, the number of adder stages l in an $n \times n$-bit multiplier is given by

$$l = \lfloor \log_2 (n/4) \rfloor = \lfloor \log_2 n - 2 \rfloor. \quad (28)$$

Fig. 13 shows the relation between the number of adder delays and the word length for various multipliers. In Fig. 13, the number of adder delays in a binary multiplier is defined as that number of adders necessary to reduce all the partial products into two operands. The number of adder delays for the SD multiplier is half of that of the fastest binary multiplier using a Wallace tree and modified Booth's algorithm for a word length of 32 bits [14], [15]. Also a tenfold reduction of the number of adder delays can be achieved compared with a 32×32-bit ordinary array multiplier.

C. SD-to-Binary Conversion

The final product P represented by the radix-4 SD number can be written as

$$P = (p_{n-1} \cdots p_i \cdots p_0) = \sum_{i=0}^{n-1} p_i 4^i \quad (29)$$

where $p_i \in \{-3,-2,-1,0,1,2,3\}$, for $i = 0,\cdots,n-2$ and $p_{n-1} \in \{-1,0,1\}$. The radix-4 signed digit p_i can be de-

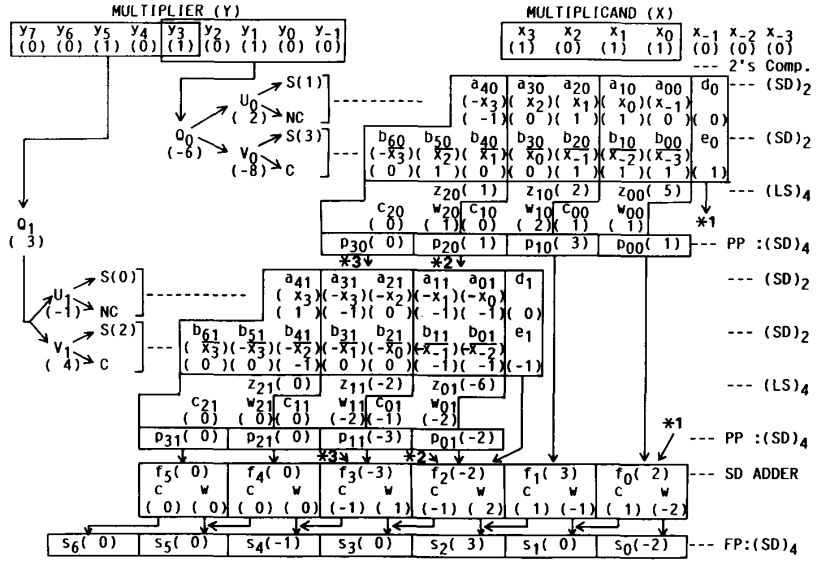


Fig. 12. Example of the 8×4-bit multiplication (C: complement; NC: no complement; $S(i)$: i-bit shift; PP: partial product; FP: final product; $(SD)_i$: radix-i SD number; $(LS)_4$: linear sum).

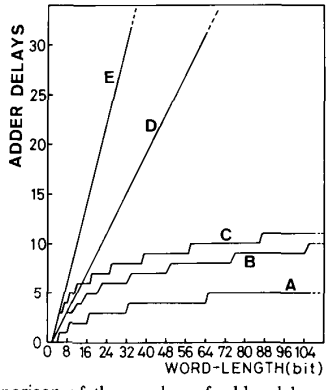


Fig. 13. Comparison of the number of adder delays in various multipliers (A: proposed SD multiplier; B: binary multiplier with Wallace tree (WT) and modified Booth's algorithm (MBA); C: binary multiplier with WT; D: binary multiplier with carry save adder (CSA) and MBA; E: binary multiplier with CSA).

composed into two symmetrical components (p_i^+, p_i^-) as follows:

$$\left.\begin{aligned} p_i^+ &= p_i, \quad p_i^- = 0, && \text{if } p_i \geq 0 \\ p_i^+ &= 0, \quad p_i^- = -p_i, && \text{if } p_i < 0 \end{aligned}\right\} \tag{30}$$

where $p_i^+, p_i^- \in \{0,1,2,3\}$ and $p_i = p_i^+ - p_i^-$. Since both $P^+ = (p_{n-1}^+ \cdots p_0^+)$ and $P^- = (p_{n-1}^- \cdots p_0^-)$ are the ordinary radix-4 weighted-number representation, these values can be easily decoded to two's complement binary numbers. Therefore, the conversion can be performed by subtraction using binary full adders. By the extension of the above conversion algorithm, a high-speed conversion technique using a radix-4 carry lookahead adder has been developed [8]. Consequently, the conversion can be completed with the delay of decoder and ten CMOS gates.

V. Implementation of the SD Multiplier

Fig. 14 shows a block diagram of the 32×32-bit SD multiplier which is composed of PPG's, parallel SD adders (PSDA's), a recoder, decoders, and SD-to-binary converters. The multiplication can be performed by a three-stage binary-tree addition scheme. The chip also contains input (X, Y) registers, an output (P) register, and a product selector.

Fig. 15 shows a photomicrograph of the SD multiplier. It is clear that the structure is very regular and the interconnections between the modules are very simple. The chip size is 4.92×7.00 mm^2, and the effective multiplier size is 3.16×5.23 mm^2 which is half of that of the fastest conventional binary multiplier [10].

In order to measure the multiply time, multiplication-control gates are inserted between the Y register and the recoder. The multiplication is started at the rising edge of the multiplication enable ME signal, and the multiplication results are latched in the P register at the falling edge of the ME. Thus, it is obvious that the minimum pulse width of the ME is the effective multiply time when the multiplication is performed correctly. The maximum delay time t_m of the multiplier is expressed as

$$t_m = t_p + 3t_s + 2t_q + t_d + t_c \tag{31}$$

where t_p, t_s, t_q, t_d, and t_c are the maximum delay times of the product generator, the SDFA, the inverted quantizer, the decoder, and the SD-to-binary converter, respectively. By substituting these delay times obtained from SPICE simulation using the 2-μm device parameters to (31), the multiply time is estimated to be 42 ns. Fig. 16 shows waveforms of the ME input and the product output (MSB), where the multiplicand $X = 00000100_H$ and the multiplier

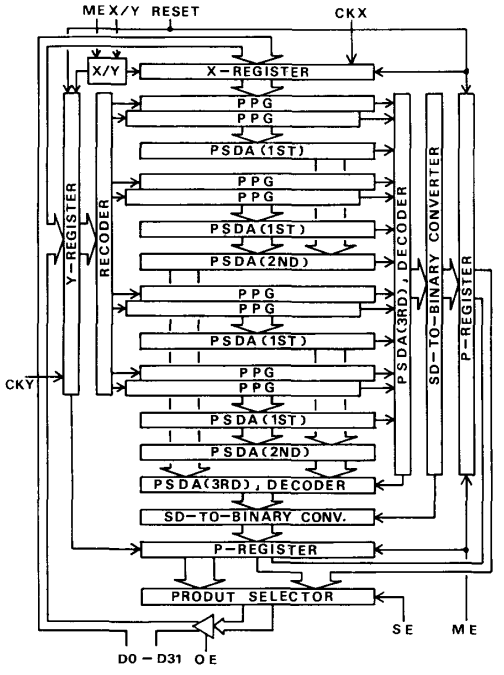


Fig. 14. Block diagram of the 32×32-bit multiplier.

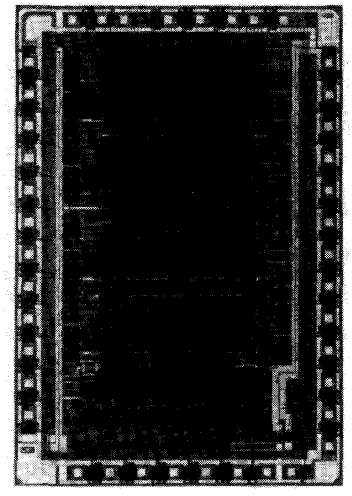


Fig. 15. Photomicrograph of the multiplier chip.

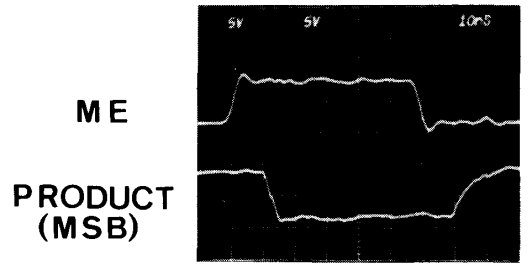


Fig. 16. Waveforms of the *ME* input and the product output (MSB).

TABLE VI
COMPARISON OF TWO IMPLEMENTED 32×32-BIT MULTIPLIERS

	The multiple-valued multiplier	The fastest binary multiplier
Multiply time (ns)	59	56
Number of interconnections	200	1,500
Number of transistors (current-mode)	23,600 (7,200)	45,000
Effective multiplier size (mm^2)	5.2 x 3.2 (16.6)	5.3 x 5.7 (30.2)
Power dissipation (W)	0.5	1
Technology	2 μm CMOS + depletion-mode pMOS	2 μm CMOS

$Y = 80000000_H$ in the hexadecimal representation. From Fig. 16, the multiply time is measured to be about 59 ns.

Table VI shows the comparison of actual performances of the implemented SD multiplier and the fastest binary multiplier presented at ISSCC'86. The multiply time is comparable to that of the fastest binary multiplier, because the number of cascaded adder chains is half, and because the delay time of the SDFA module is about twice compared with a binary full adder.

The number of transistors is approximately 52 percent of that for a binary multiplier. However, the effective area is determined not only with the number of transistors but also with the feature sizes of transistors and the interconnection. The feature sizes of transistors used for the current-mode circuits are relatively large compared with those used for CMOS gates, while the number of interconnections among the modules (PPG's, SDFA's, and the decoders) is approximately 13 percent of that of the fastest binary multiplier using the Wallace tree. Also, the regularity of the layout greatly contributes to the reduction of interconnection area in the multiple-valued multiplier. As a result, a 46-percent reduction of the effective area is achieved compared with the binary multiplier.

The multiple-valued multiplier is superior to the conventional one with regard to the power dissipation because of the reduction of the active devices. The number of transistors used for current-mode circuits is about 7200 and the other transistors are used for binary CMOS gates.

VI. CONCLUSION

This paper presents multiple-valued CMOS bidirectional current-mode circuits and their application to a high-speed compact multiplier. The implemented 32×32-bit multiplier based on the radix-4 signed-digit number system is totally superior to the fastest CMOS binary multiplier reported.

In submicrometer technology, however, it is difficult to control the saturated current of the MOS devices. There-

fore, the development of devices more suited to multiple-valued current-mode circuits remains a future problem.

The concept of the bidirectional current-mode circuits is potentially effective not only for the radix-4 SD number system but also for other-radix SD number systems and the symmetrical residue number system.

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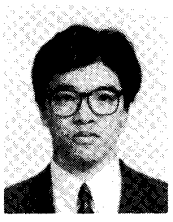

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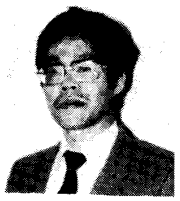

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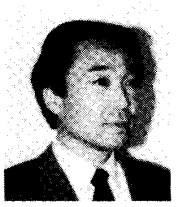

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