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journal or publication title	AIP Conference Proceedings 19th International Conference on NOISE AND FLUCTUATIONS-ICNF2007
volume	922
page range	43-46
year	2007
URL	http://hdl.handle.net/10097/51829

doi: 10.1063/1.2759633

Impact of the channel direction on the 1/f noise in SOI-MOSFETs fabricated on (100) and (110) silicon oriented wafers

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Abstract. In this paper we present the study of 1/f noise in SOI n- and p-MOSFET fabricated on Si(100) and Si(110) oriented wafers. A comparison of noise performances are first presented, then the impact of the in-plane channel direction on the low frequency noise for each device is investigated. A particular attention is made for transistors fabricated on Si(110) oriented substrates.

Keywords: SOI-MOSFET, 1/f noise, channel direction, surface orientation, silicon.
PACS: 72.70.+m, 73.40.Qv, 68.47.Fg, 73.50.Td.

INTRODUCTION

Noise is a limiting factor for electronic devices and especially for analog circuits. For decades researchers have studied noise to try to understand its origin in order to reduce or even suppress it. Among the several types of noise found in electronic devices, the 1/f noise also called low frequency noise or even "Flicker" noise is the one of concern for world leading electronic devices manufacturers. Its reduction is of prime importance for the development of new devices and circuits as well as the improvement of the working frequency. In the case of CMOS technology, several solutions are investigated in order to enhance the performances. Among these, the most popular approach is the reduction of the gate. As consequence the working frequency is enhanced but regrettably the 1/f noise level also increases. Since the current drivability of p-MOS based on (110) oriented silicon is 3 times larger than the one based on (100), a new approach is to develop a technology based on the (110) orientation [1]. Unfortunately, in these new devices the 1/f noise level is still too high to establish this technology as a viable competitor or even a future replacement for the current silicon CMOS technology. Though various problems must be solved in order to bring this technology to a higher level of performances, one of the main interest of this approach is the possibility to use only one substrate to fabricate devices on Si(100) and Si(110) oriented surfaces with the capability to choose between several channel directions such as in-plane <100> and <110> direction. The present work is related to this new technology, namely the noise study of SOI-MOSFET fabricated on Si(100) and (110) oriented substrates using different channel orientations.

CP922, *Noise and Fluctuations, 19th International Conference,* edited by M. Tacano, Y. Yamamoto, and M. Nakao
© 2007 American Institute of Physics 978-0-7354-0432-8/07/$23.00

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EXPERIMENTAL DETAILS

The entire fabrication process has been carried out in our super clean room at Tohoku University. SOI p- and n-MOSFET have been fabricated on Si(100) and Si(110) oriented wafers and for each of these several in-plane channel directions, namely the direction of the current path, have been lay out. The alkali-free-5-step cleaning process has been used in order to avoid the degradation of the micro-roughness and especially the formation at the Si/SiO_2 interface of (110) oriented micro-surfaces [2]. A 50nm/100nm thick SOI/BOX has been used and a 7.5 nm Kr/O_2 radical gate oxide has been formed. Drain current noise measurements were carried out using a Vector Signal Analyzer (AGILENT 89410A) connected to a low-noise preamplifier (Princeton Applied Research 5184) with contacts directly taken on wafer. Transistors were initially biased by a modular DC source (HP 4142B) in order to find the target bias point parameters. This source was then replaced by an Ultra-Low Noise DC Source (SHIBASOKU PA14A1) for the final noise measurement. All transistors had low frequency $1/f^{\nu}$ noise with $1<\nu<1.1$ in the measurement range from 10Hz to 100000Hz.

RESULTS

We can clearly see in Figure 1 that SOI-MOS transistors fabricated on Si(100) oriented wafers have a lower noise level than when fabricated on Si(110). Moreover, when we compare p and n-channel transistors, the p-channel fabricated on Si(100) presents the best noise performance while it becomes the worst when fabricated on Si(110).

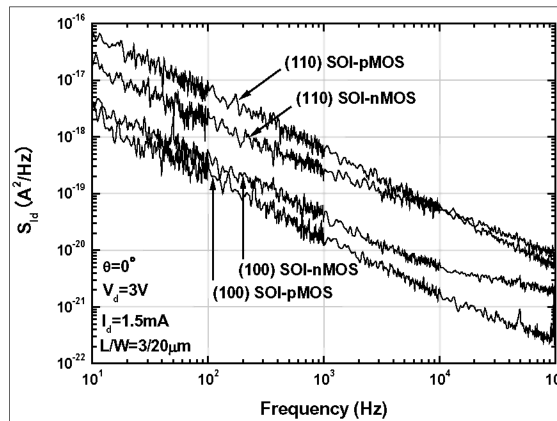

FIGURE 1. Low frequency noise for SOI p- and n-MOSFET fabricated on Si(100) and Si(110) oriented wafers. Geometrical characteristics as well as polarization point are identical for each transistor.

The impact of the channel direction on the 1/f noise and the drivability has been investigated in the case of Si(100) oriented wafers. For this study, we reported the angle made between the conventional channel direction, namely the <100> in-plane

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direction for Si(100) substrates and <110> in-plane direction for Si(110) substrates, with the channel direction of the studied transistor. As it has been several times reported in the literature [3-6], for n-channel transistors, the change in the channel direction is not affecting at all the overall device performances. However, in the case of the p-channel and at constant current, the overdrive gate bias must increase to counterbalance the drop of mobility when the channel direction is replaced from the direction <100> to the <110> one. We noticed no dependency with the low frequency noise.

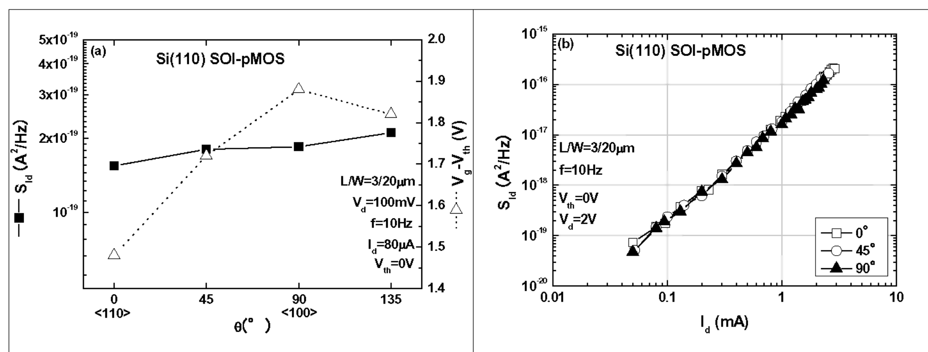

FIGURE 2. SOI-p-MOS transistor fabricated on Si(110), (a) Evolution of the spectral density of current and overdrive gate bias with the direction of the channel, (b) spectral density of current in function of the drain current for three different channel directions.

Figure 2 reports the study of SOI p-MOSFET fabricated on Si(110) oriented substrates. On figure 2a, as the channel direction goes progressively from the direction <110> to the <100> one, the applied overdrive gate bias increases to balance the drop of mobility in order to maintain a constant current. At the same time, we can see that the spectral density in current is not changing. The low frequency noise seems to not be affected by the channel orientation. This latter result is validated in the figure 2b.

The same approach has been carried out for the SOI n-MOSFET fabricated on Si(110) oriented wafers. From the figure 3a we can see that, contrary to the behavior of the previously studied device, the applied overdrive gate bias is decreasing as the channel direction goes progressively from the direction <110> to the <100> one. The mobility being enhanced by the change in channel direction, the applied overdrive gate tension must decrease to counterbalance it in order to preserve a constant current. Contrary to the others cases, we have here a dependence of the 1/f noise with the channel direction even if the current is maintained constant. The minimum noise level is found for the direction <110> and the maximum for the <100> one corresponding to a roughly 2 times increase. We reported on figure 3b the evolution of the 1/f noise with the drain current for the 2 main directions in oder to confirm this previous result. Then we can here also clearly see that the fact of changing the channel direction from the <110> one to the <100> one is affecting the 1/f noise. A ratio of 1.5 to 2 is found between the direction <110> and the <100> one.

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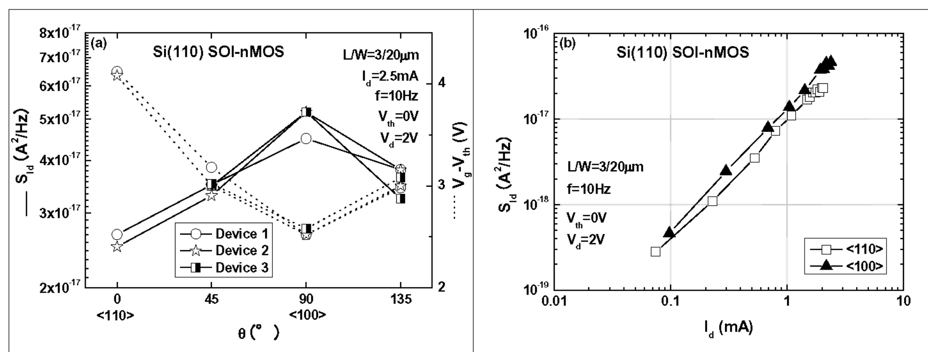

FIGURE 3. SOI-n-MOS transistor fabricated on Si(110), (a) Evolution of the spectral density of current and overdrive gate bias with the direction of the channel, (b) spectral density of current in function of the drain current for the channel direction <110> and <100>.

CONCLUSION

In this paper we shown that SOI-MOS transistors fabricated on conventional Si(100) oriented wafers present a lower 1/f noise level than the ones fabricated on Si(110) oriented wafers. Furthermore, in the case of the conventional orientation, the p-channel transistor presents the lower noise level while the n-channel becomes the lower when fabricated using the new orientation. Subsequently, we reveled that at a physical level the impact of the channel direction on the 1/f noise has been found to be relevant only for SOI-n-MOS Si(110) transistors.

ACKNOWLEDGMENTS

This work was conducted as a part of the project under Grant-in-Aid for Specially Promoted Research (project No. 18002004), supported by Japanese Ministry of Education, Culture, Sports, Science and Technology.

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