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In this letter, the formation of high density tungsten nanodots (W-NDs) embedded in silicon nitride via a self-assembled nanodot deposition is demonstrated. In this method, tungsten and silicon nitride are cosputtered in high vacuum rf sputtering equipment. The W-NDs with small diameters (1–1.5 nm) and high density ($\sim 1.3\times 10^{13}/\mathrm{cm}^2$) were achieved easily by controlling W composition; this is the ratio of total area of W chips to that of silicon nitride target. The metal-oxide-semiconductor memory device was fabricated with high density W-NDs floating gate and high-k HfO_2 blocking dielectric. A wide range memory window (0–29 V) was obtained after bidirectional gate voltages sweeping with range of $\pm 1 - \pm 23$ V. It is feasible to design the memory window with propriety power consumption for nonvolatile memory application. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3081042]

Recently, metal nanodot memories attracted the most attention as promising candidates for next generation nonvolatile memory (NVM).[1,2] Comparing with semiconductor nanodots,[3,4] metal nanodots have some advantages, such as higher density of states around the Fermi level and a wide range of available work functions. Therefore, the requirements of high charge storage capacity and long retention time can be realized. However, when integrating the metal nanodots into the memory device structure, there are still some challenges. First is the formation of high density nanodots to overcome the electrical fluctuation between memory cells. The main critical issue that limits the scaling of nanodots memory is the fluctuation of the electrical characteristics, which is attributed to the variability in dot size and dot density between devices.[5] Second, it is required to prevent metal/oxide reaction and metal diffusion during device integration process, which potentially degrade device performance.[6,7] In this work, to solve such issues, we propose a new NVM with high density tungsten nanodots (W-NDs) dispersed in silicon nitride. The silicon nitride is a good isolator to prevent the metal/oxide reaction as reported in a reference.[8]

2 in. p-type Si wafers with (100) orientation were cleaned with standard Radio Corporation of America (RCA) process, followed by thermal oxidation to form a 4.5-nm-thick tunneling oxide. Subsequently, W-ND films were deposited onto the tunneling oxide by a self-assembled nanodot deposition (SAND).[7,8] In this method, tungsten chips placed on a silicon nitride target were cosputtered in high-vacuum rf sputtering equipment [Fig. 1(a)]. The size of tungsten chip is in a length of 5 mm, a width of 5 mm, and a thickness of 1.5 mm. The W composition of sputter target was defined as the ratio of total area of tungsten chips to that of silicon nitride target. Figure 1(b) shows a high-resolution transmission electron microscopy (HRTEM) cross-sectional image of as-deposited W-ND film. The W composition of sputter target is ~30.8%. It was clearly observed that the W-NDs with high density were dispersed in the sputtered Si_xN_y film. The sizes and density are 1.5–2.0 nm and $\sim 9.6\times 10^{12}/\mathrm{cm}^2$, respectively. To evaluate the thermal stability of W-NDs, the post-deposition annealing (PDA) was performed at range of 400 °C–900 °C in N_2 ambient for 30 min. Figure 2 shows HRTEM cross-sectional images of W-NDs film with PDA at 800 and 900 °C. As shown in Fig. 2(a), after 800 °C PDA, the dot size and density were almost the same as the as-deposited W-NDs [Fig. 1(b)]. Based on the diffusion controlled agglomeration theory, it indicates that at 800 °C PDA for 30 min, the traveling distance of tungsten atom is much smaller than the distance between the W-NDs. The clear interface between W-ND and Si_xN_y indicates the quality improvement of W-NDs film by PDA. In contrast, after 900 °C PDA, the sizes of W-ND became 5–6 nm and the density decreased to $\sim 2\times 10^{12}/\mathrm{cm}^2$, as shown in Fig. 2(b). The

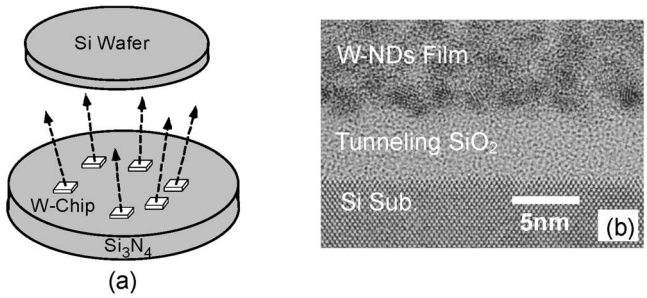

FIG. 1. (a) SAND and (b) HRTEM cross-sectional image of as-deposited W-NDs film produced with W composition of ~30.8%.

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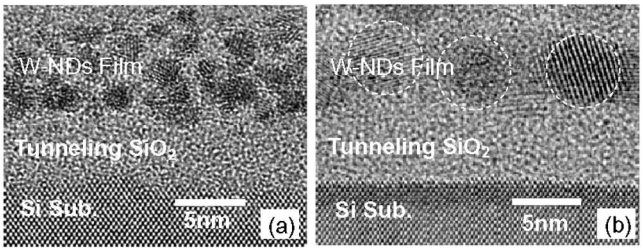

FIG. 2. HRTEM cross-sectional images of W-NDs films with PDA at various temperatures. The W composition of sputter target is ~30.8%. (a) W-NDs film with PDA at 800 °C. (b) W-NDs film with PDA at 900 °C.

result indicates that during 900 °C PDA for 30 min, the traveling distance of tungsten atom is near or larger than the distance between W-NDs, which is 1–2 nm. At this condition, the agglomeration was generated to lead to the growth of W-ND. The melting point of tungsten is as high as 3422 K, which is higher than silicon or other metals, and suggests the higher diffusion active energy. Another, the silicon nitride is a good diffusion barrier. Based on above analysis, the excellent thermal stability of W-ND in silicon nitride, which is higher that of other nanodots such as FePt or Si embedded in silicon oxide, can be explained.[9–11] It is worth noting that the excellent interface at the SiO_2/W-NDs film was observed even after 900 °C PDA, indicating that the W-NDs did not diffuse into the tunneling oxide during the annealing process.

In order to control the size and density of W-NDs, the sputter targets with different W compositions have been used. Figure 3(a) shows the density and average size of W-ND as a function of W composition. For these films, the PDA was performed at 800 °C. It was found that the W-ND density was increased first and then decreased with decreasing W composition. On the other hand, the W-ND average size was decreased and then tended to saturation with decreasing W composition. These results suggest that the dot size and density can be controlled by W composition. The maximum density of $\sim 1.3\times 10^{13}/\mathrm{cm}^2$ and small sizes of 1–1.5 nm were obtained at the W composition of ~16.5%, as shown in the HRTEM cross-sectional image of Fig. 3(b). The density is higher than other groups by one order of magnitude.[12–14]

In order to explore the potential of high density W-NDs for NVM application, we made a metal-oxide-semiconductor (MOS) capacitor with a W-ND floating gate. The fabrication process is as below. A 4.5-nm-thick tunneling oxide was thermally grown on *p*-type Si substrate. The 10-nm-thick

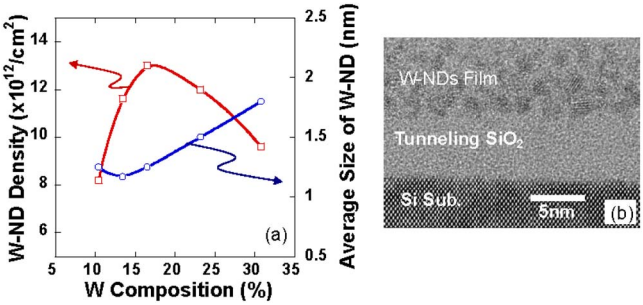

FIG. 3. (Color online) (a) The density and average size of W-ND as a function of W composition of sputter target. The PDA was performed at 800 °C. (b) HRTEM cross-sectional image of W-NDs film produced with W composition of ~16.5% and 800 °C PDA.

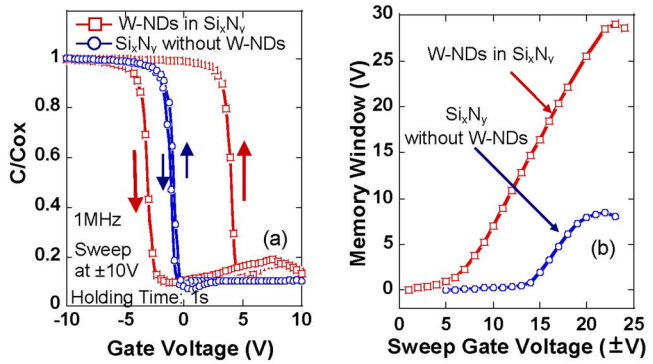

FIG. 4. (Color online) High-frequency *C-V* curves with sweeping gate voltage of ±10 V (a) and hysteresis memory window as a function of sweeping gate bias (b) for capacitors with and without W-NDs. The W-ND density is $\sim 1.3\times 10^{13}/\mathrm{cm}^2$.

W-ND film was deposited on a tunneling oxide by SAND with the W composition of ~16.5%, followed by PDA at 800 °C. The W-ND density is $\sim 1.3\times 10^{13}/\mathrm{cm}^2$. Subsequently, as a blocking dielectric, high-*k* HfO_2 was deposited as thick as 40 nm, and then annealed at 600 °C for 30 min. The dielectric constant of HfO_2 was estimated to be about $20\varepsilon_0$. Finally, an Al electrode with an area of $\sim 7\times 10^{-4}$ cm^2 was formed by thermal evaporation. As a reference, the MOS capacitor with a charge layer of Si_xN_y without W-NDs was fabricated simultaneously. The memory capacitors were measured at room temperature using an Agilent B1500A semiconductor parameter analyzer.

Figure 4(a) shows the *C-V* measurements at 1 MHz with bidirectional voltage sweeping from +10 to −10 V and from −10 to +10 V. In this measurement, the holding time of 1 s was applied. A large memory window of ~7 V was observed for W-NDs memory capacitor. In addition, the memory window is independent of the measurement frequency (not shown here), indicating that the memory window is not due to the interface traps. The memory window as a function of stress voltages was summarized from a series of *C-V* measurements, as shown in Fig. 4(b). These *C-V* measurements were carried out by applying stress voltages to the control gate with holding time of 1 s, followed by bidirectional voltage sweepings. When the sweeping gate voltage region is below ±14 V, considering the small memory windows of the reference sample with the silicon nitride without W-NDs, the large counterclockwise memory windows are obviously attributed to the storage of charges in W-NDs or related defects. In contrast, when the sweeping gate voltage is larger than ±14 V, the memory window can be attributed to both W-NDs and silicon nitride. Finally, the memory window tends to saturation or decrease with increasing sweep gate voltage, which is presumably due to the degradation of the tunneling or block insulators, that is, the stress-induced leakage current effect. In this work, the hysteresis memory window of ~1 V is observed under small sweeping gate voltage of ±5 V. The maximum memory window as large as 29 V was obtained for gate voltage sweeping at ±23 V. At sweeping gate voltages of ±8 and ±10 V, the memory windows are about 4 and 7 V, respectively. The wide range memory window suggests that it is easy to design the memory window with propriety power consumption. We calculated the charge density in W-NDs by a formula as reference.[15] At memory a window of ~29 V, the extremely

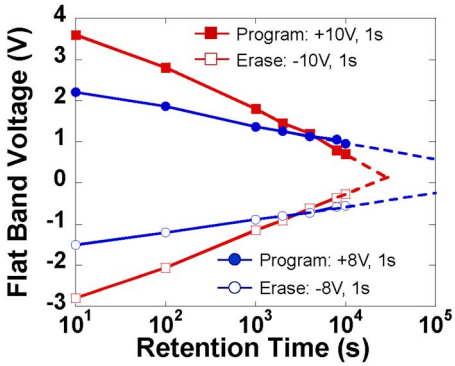

FIG. 5. (Color online) Retention characteristics at zero gate bias and room temperature for W-NDs MOS memory capacitor. The program/erase was done at ±8 and ±10 V for 1 s.

high trapped charge density of $\sim 8\times 10^{13}/\mathrm{cm}^2$ was obtained.

Retention characteristics at room temperature for W-NDs MOS memory capacitor were also investigated. Figure 5 shows the data retention characteristics after program/erase at ±10 and ±8 V for 1 s, respectively. As is observed, the memory window of ~1.0 V remained at a retention time of 10^4 s after ±10 V program/erase, namely, the charge loss of ~85%. By data extrapolation, the memory window is eliminated after 3×10^4 s. Comparing that with the case of ±8 V program/erase, the memory window of ~1.5 V remained at a retention time of 10^4 s. The charge loss is ~60%. The disappearing time of the memory window is expanded to 10^6 s. For achieving a long retention time, a low operation voltage is necessary. However, in such cases, a retention time of ten years is not expected. It had been reported that when the size of metal nanodot is less than 2 nm, the conduction band minimum will upshift due to the quantum confinement effect.[16] In this work, the W-NDs are 1–1.5 nm. Therefore the quantum confinement effect cannot be neglected, which presumably degrades the retention characteristics. The tradeoff between high density and quantum confinement effect may be solved by choosing metal nanodots with high work function to compensate for the conduction band upshift. We will discuss it in further work.

In conclusion, W-NDs in silicon nitride were formed by the SAND method. The W-NDs have excellent thermal stability until 800 °C PDA. The W-ND density was controlled by the W composition of sputter target. The density is increased first and then decreased with decreasing W composition. The extremely high density of $\sim 1.3\times 10^{13}/\mathrm{cm}^2$ and small sizes of 1–1.5 nm were formed with the W composition of ~16.5%. Such high density W-NDs and high-k HfO_2 blocking dielectric were used to investigate the memory characteristics. A wide range memory window was obtained, showing the possibility for NVM application. The short retention time is presumably attributed to the quantum confinement effect, which upshifts the conduction band. Because the SAND method is simple and rather effective for metal nanodot fabrication, it is feasible for a further exploration to optimize device performance and produce memory cells with potential applications.

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