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Formation of device-grade epitaxial silicon films at extremely low temperatures by low-energy bias sputtering

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Device-grade epitaxial single silicon layers have been formed at extremely low temperatures of about 300 °C by low-energy bias sputtering in conjunction with *in situ* substrate surface cleaning and an ultraclean processing environment. Dopant impurities in the target material are fully incorporated into the sputter-deposited silicon film and these impurities are 100% electrically activated without any additional heat cycles. An epitaxial silicon film having a resistivity as low as 0.0014 Ω cm has been obtained using a heavily arsenic-doped silicon block as a target material. A *p-n* junction diode formed by directly depositing a phosphorus-doped *n*-type epilayer on a *p*-type substrate indicates a reverse current level as low as 1.88×10^{-9} A/cm^2 at a reverse bias voltage of 5 V, thus verifying that the *in situ* substrate surface cleaning by low-energy Ar ion bombardment is very effective and damage free. The electrical characteristics of a grown film have shown a good correlation to the crystal structure of the film, which is primarily determined by the energy of ions concurrently bombarding the growing film surface.

I. INTRODUCTION

Integrated circuits or, more generally speaking, semiconductor devices, are constructed as a stacked structure of various thin films. Consequently, the performance and characteristics of devices are strongly influenced by the integrity of film interfaces as well as by the quality of films. Therefore, the formation of high-quality thin films having ideal interface characteristics is a key to realize high-performance devices for future ultralarge scale integration (ULSI). In addition, the reduction in processing temperature is also a key issue in future ULSI processing in order to suppress chemical reactions at the interfaces as well as to minimize autodoping and impurity diffusion effects for high-precision dopant profile control.

One of the most important targets of our research projects is to establish a total low-temperature process flow for device fabrication in which all thermal budgets are carried out below 500 °C. This includes oxidation, annealing of ion-implanted silicon layer, and silicon epitaxial growth.[1] Such a very low-temperature process flow will enable high cost performance manufacturing, high process flexibility, high reproducibility, and high chip yields, and most importantly will lead to the possibility of constructing novel device structures for future ULSI application. Among these, the growth of high-quality epitaxial silicon films at extremely low temperatures is most strongly requested.

Conventional epitaxial silicon growth processes using chemical vapor deposition (CVD) techniques are carried out typically at temperatures over 1000 °C for both film growth and substrate surface cleaning. Autodoping and solid-state diffusion effects cannot be avoided in such high-temperature processes. Recently, high-quality boron-doped epitaxial silicon (a doping range of 5×10^{14}–1×10^{20} cm^{-3}) was grown at 550 °C by ultrahigh vacuum CVD (UHV-CVD),[2] showing a reverse current density of a *p-n* junction as low as about 1×10^{-9} A/cm^2. The fabrication of bipolar transistors[3] and MOSFETs[4] by using low-temperature (below 800 °C) ultralow pressure CVD (U-LPCVD) with an argon sputter cleaning[5] was also reported, which showed a little higher reverse current density of about 10^{-8} A/cm^2. In both cases, the process temperatures were higher than 550 °C.

The MBE technique[6,7] is one of the candidates for performing very low-temperature epitaxial growth. However, a high-temperature heat treatment is usually requested for predeposition substrate surface cleaning. Very-low-temperature silicon epitaxial growth at temperatures below 300 °C has been reported using ion beam processes, such as partially ionized vapor deposition (PIVD),[8] ion beam epitaxy (IBE),[9] ion beam sputter deposition (IBSD),[10] and ionized cluster beam deposition (ICBD).[11] However, these processes have not succeeded in obtaining device-grade silicon epitaxial films. The range of ion energy used in these processes is much higher than typical interatomic binding energies in single-crystal silicon, resulting in the formation of damages in grown films.

One of the most promising methods in growing device-grade silicon epitaxial films with ideal interfaces is a low-kinetic energy particle process.[12-18] In this process all accelerated particles bombarding the film surface during film growth have a well-defined kinetic energy comparable to crystal interatomic binding energies of the film. Consequently, these low kinetic energy particles lose their energies mostly within one atomic layer on the film surface and are expected to interact very effectively with growing silicon films without creating damages. The process has been successfully applied to the low-temperature epitaxial growth of silicon[13-16] as well as to high performance aluminum[12,18,19] and copper metallization.[17]

The purpose of this paper is to report on our entire work on the formation of *in situ* doped device-grade silicon epitax-

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ial layers at an extremely low temperature of 300 °C by the low kinetic energy particle process. In this work, low-energy bias sputtering in conjunction with *in situ* substrate surface cleaning by low-energy ion bombardment has been utilized to realize such a low-temperature epitaxial growth process. It has been shown that the crystallinity of the grown film is controlled by the energy of bombarding ions during film growth. Dopant impurities in the target are fully incorporated into the lattice site of the sputter-deposited silicon film, being 100% electrically activated without any additional heat treatment. A *p-n* junction diode consisting of an *n*-type deposited film on a *p*-type substrate exhibits a reverse current level as low as 1.88×10^{-9} A/cm^2, thus verifying the formation of high quality films having high integrity interfaces.

The concept and features of the low kinetic energy particle process as well as the experimental apparatus used in this work are described in detail in Sec. II. Experimental conditions are shown in Sec. III. Section IV describes results and discussion, and the conclusion is given in Sec. V.

II. HIGH PERFORMANCE PROCESS TECHNOLOGY FOR LOW-TEMPERATURE THIN-FILM GROWTH

A. Concept of "low kinetic energy particle process"

In the process of epitaxial growth, a certain energy must be provided to surface adatoms so that they can migrate at the surface and find themselves at normal lattice sites to construct a single crystal. In conventional chemical vapor deposition (CVD) processes, this energy is provided as a form of thermal energy by heating the entire wafer. This leads to undesirable effects such as impurity redistribution in the epilayer or autodoping.

Instead of using thermal energy as an enhancement energy for processing, various ion beam processes[8-11] have been investigated to make use of kinetic energy of accelerated ions. One of the problems encountered in these processes is that the energy of ion bombardment is in a very high-energy regime typically of a hundred eV's to keV's. This results in the formation of crystalline damages both in the film and the substrate. Therefore, if kinetic energy is utilized in thin film growth, the bombardment energy of individual ions must be precisely controlled in a low-energy regime that does not cause any deleterious damages. Further difficulty of the conventional ion beam processes exists in the fact that the beam consists of species identical to that of the film to be deposited. Silicon ion beams or silicon cluster beams, for instance, have to be used to grow silicon films. One of the most important parameters in ion beam thin-film deposition processes is the total energy transfer (surface activation energy) given to a growing film surface, which is determined by the product of individual ion energy and bombarding ion flux density. If the total energy transfer is requested to increase, for instance, only the ion flux density should be increased while keeping the individual ion bombardment energy at an optimum value (if the ion bombardment energy is increased instead, damage will be generated). This means the increase in the surface activation energy necessarily accompanies the increase in the film growth rate. Consequently, it is impossible to control the surface activation energy and film growth rate independently in conventional ion beam processes. In other words, the surface activation energy density given to a unit thickness of the film cannot be controlled as an independent parameter. In low-temperature high-quality thin-film growth technology, the independent control of three principal process parameters, i.e., the individual ion bombardment energy, the ion flux density, and the film growth rate is most essential.

In order to give solutions to the above mentioned difficulties of conventional ion-beam processes, we have developed a low kinetic energy particle process. In this process, the surface activation energy is transferred as a form of kinetic energy (or momentum) by concurrently bombarding the growing film surface with low-energy ions of inert gas atoms such as Ar, He, and so forth. The ion species different from film constituent atoms are used as a vehicle of energy transfer. Furthermore, very low-energy regime was employed for the ion bombardment. Typical energies of individual bombarding ions concerned in this work are in the range of a few eV's to a few tens of eV's, which are comparable to typical interatomic crystal binding energies. As a result, very efficient interactions and energy transfer between the incoming ions and the constituent atoms at the film surface are expected to occur without causing any damages in the film. Since the surface activation due to low-energy ion bombardment occurs only just at the surface, i.e., in a few atomic layers at the surface, it is possible to realize epitaxial growth keeping the wafer temperature very low. When the ion bombardment in an extremely low-energy regime (a few eV's) is utilized, *in situ* substrate surface cleaning is also carried out very effectively. *In situ* substrate surface cleaning means the removal of adsorbed impurity molecules on the substrate surface such as moisture. Such unique features of the process have made it possible to grow high-quality epitaxial silicon layers at a temperature as low as 300 °C.

In order to realize such a process as a practical tool for wafer fabrication, the precise control of ion bombardment energy as well as the establishment of ultimate cleanliness of the process are most essential. The key issues realizing high performance processes, in general, are summarized in the following[20,21]:

(1) Ultraclean processing environment;
(2) Ultraclean wafer surface; and
(3) Perfect process-parameter control.

We have developed a rf-dc coupled mode bias sputtering system that meets all these requirements. The system is described in detail in the next section.

B. rf-dc coupled mode bias sputtering system[12]

A schematic of the rf-dc coupled mode bias sputtering system used in the present work is illustrated in Fig. 1. A 100-MHz rf power supply was employed to generate a high density plasma under a relatively low gas pressure of ~mTorr. Two dc power supplies are connected to the target and the wafer holder via low pass filters to separately control their dc potentials. Therefore, the ion energies incident on

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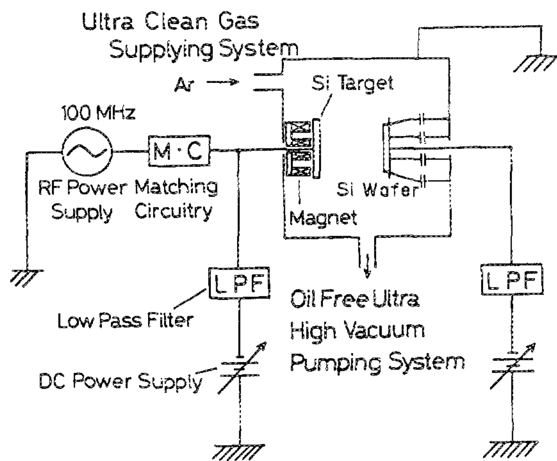

FIG. 1. Schematic of a rf-dc coupled mode bias sputtering system.

the target and the substrate are independently determined by these two external dc sources. The dc potential applied to the target determines the sputtering rate, i.e., the film growth rate, while that applied to the wafer holder determines the magnitude of ion energy for bombarding the film surface. Since the excitation frequency of 100 MHz is much higher than the ion frequency (typically 3 MHz), the ions cannot respond to the rf component of the sheath field and are accelerated only by the dc voltage component appearing across the sheath which is primarily determined by the external dc source. Therefore, the precise control of ion energy with negligibly small energy spread has become possible. On the other hand, the rf power input determines the plasma density, i.e., the ion flux supplied to the target and to the wafer. By adjusting the rf power, the target bias, and the wafer bias, the important process parameters in thin film growth, such as the film growth rate, the individual ion bombardment energy, and the ion flux density can be selected to any desired combinations. Thus, one of the key issues presented above, "perfect process-parameter control" has been established in this system.

An entire system was constructed based on the philosophy of ultraclean technology,[22] i.e., the oil-free ultrahigh-vacuum exhaust system, and ultraclean gas delivery system[23] was employed. As a result, the impurity levels in argon gas as low as several ppb or below (mainly H_2O) and a base pressure for the main vacuum chamber of 2×10^{-10} Torr was achieved. This is the achievement of another key issue, "ultraclean process environment." The realization of the remaining key issue, ultraclean wafer surface, will be described in reference to Fig. 2.

III. EXPERIMENT

p-type (100) silicon wafers, 3–5 Ω cm resistivity, were used as substrates. After cleaning with a conventional wet chemical process, wafers were etched in diluted HF, rinsed in ultrapure water, and dried by isopropyl alcohol vapor. Then a wafer was immediately loaded into the vacuum chamber, which was pumped down with a turbomolecular

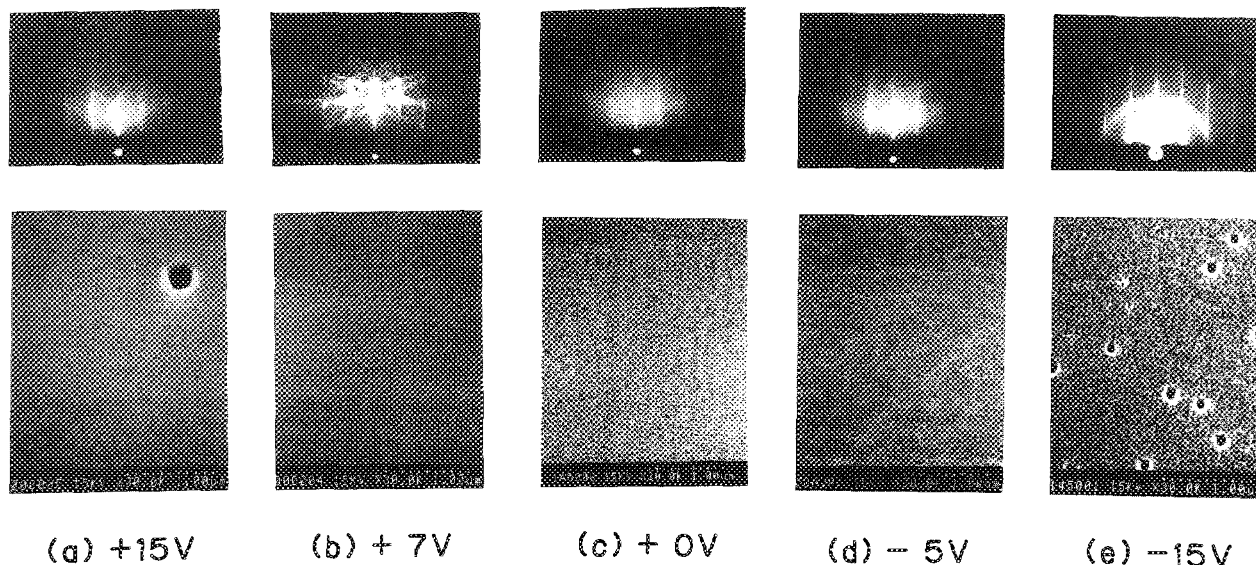

FIG. 2. Effect of *in situ* substrate surface cleaning condition on the crystallinity of epitaxially grown silicon films. Reflection electron diffraction patterns (top) and SEM micrographs of Wright-etched sample surfaces (bottom) are shown as a function of the substrate bias voltage applied during the cleaning operation, which was (a) + 15 V, (b) + 7 V, (c) 0 V, (d) − 5 V, and (e) − 15 V. Ion bombardment conditions during film growth are identical for all samples, i.e., the best condition for epitaxial growth.

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pump to pressures of 10^{-6}–10^{-7} Torr, and transported into the deposition chamber by a load lock. After performing *in situ* substrate surface cleaning by low-energy argon-ion bombardment, a silicon film was deposited under concurrent argon-ion bombardment. The wafer was heated to 300 °C both during the cleaning and the deposition operations. The determination of the wafer temperature is described in the Appendix B. Both the substrate surface cleaning and the film deposition were conducted under a variety of ion-bombardment conditions, which are summarized in Table I. Two diffferent kinds of targets were used for film deposition, i.e., a phosphorus-doped (111) FZ silicon wafer of 0.014 Ω cm resistivity and a heavily arsenic doped silicon block.

The crystal structure of a grown film was evaluated by reflection electron diffraction (RED) analysis and by high resolution transmission electron microscopy (HRTEM). The film surface was also observed by scanning electron microscopy (SEM) after the Wright etch. The dopant profile in the grown film was investigated by secondary ion mass spectroscopy (SIMS). Hall measurements were carried out to evaluate the electrical activation of dopants and the mobility of the film.

p-n junctions were fabricated to evaluate the sputter-deposited silicon films especially at the substrate-epilayer interface. After forming a 1000-Å-thick thermal oxide on a wafer, window patterns were opened in the oxide. Then an *n*-type silicon film of about 4000 Å thick was deposited by low kinetic energy particle process using the phosphorus doped target. After the deposited silicon film was delineated into island patterns so that they cover the entire window areas, aluminum metallization was carried out to form external electrodes. Finally, wafers were sintered at 300 °C for 30 min in a forming gas ambient (H_2:N_2 = 0.2 ℓ/min: 1.8 ℓ/min). It should be noted that the processing temperature never exceeds 300 °C both during and after the epitaxial growth process.

IV. RESULTS AND DISCUSSION

A. Optimizing ion bombardment conditions

Figure 2 demonstrates the effect of surface cleaning by low-energy argon-ion bombardment. For all samples, silicon films were grown using the identical conditions, i.e., the best condition for epitaxy to be discussed in reference to Fig. 3. Only the substrate bias voltage applied during the cleaning operation was varied as a parameter, leaving other conditions identical as given in Table I. The film growth rate was about 1 Å/s and approximately 4000-Å-thick films were grown. The top pictures are the reflection electron diffraction patterns obtained from the epitaxially grown films and the pictures at the bottom show the surface morphology of the film after the Wright etch as observed by SEM. The surface morphology of as deposited film exhibited a perfectly smooth mirror surface. Such a highly rugged surface appeared only after the Wright etch. It is seen from the figure that the best quality of the epitaxial silicon layer is obtained at a substrate bias voltage of + 7 V. Sharp Kikuchi lines are evident in the diffraction pattern and etch pits were not observed in the Wright-etched sample as shown in Fig. 2(b). When the substrate bias voltage is reduced from + 7 to − 15 V, degradation in the film quality is clearly observed.

TABLE I. Typical ion bombardment conditions.

Process parameter	*in situ* substrate surface cleaning	Film growth
Substrate temperature	300 °C	300 °C
Target bias voltage (V_t)	− 25 V	− 120–400 V
Substrate bias voltage (V_s)	+ 15–15 V	+ 20–15 V
rf power input	5 W	40 W
Argon gas pressure	8 m Torr	8 m Torr

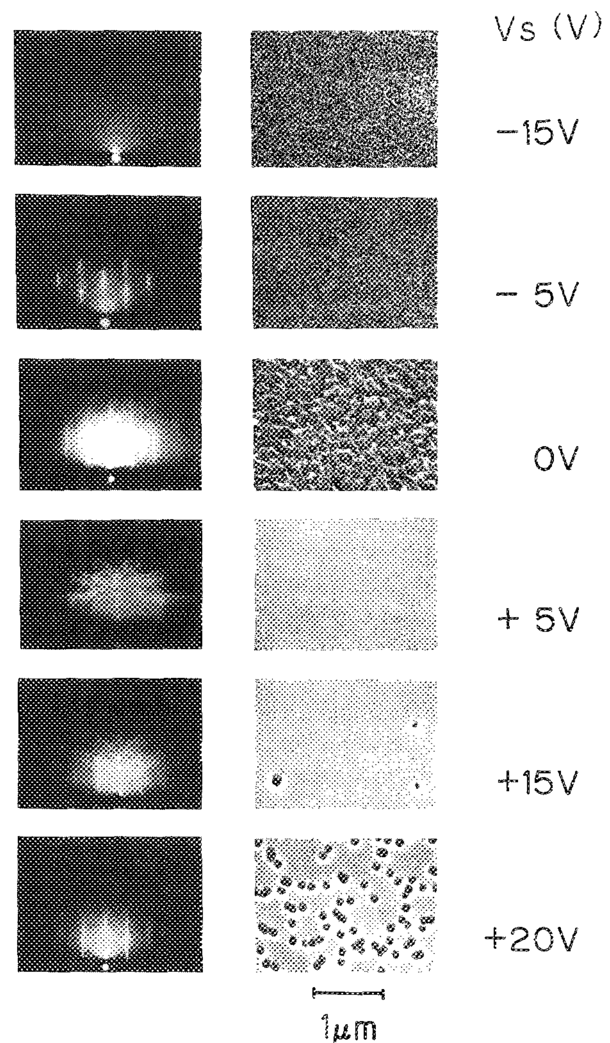

FIG. 3. Dependence of crystal structure on substrate bias voltage (V_s) with an identical target bias voltage of − 200 V. Reflection electron diffraction patterns (left column) and SEM micrographs of Wright-etched surfaces (right column) are shown as a function of V_s applied during the film growth. Here the optimum surface cleaning condition was employed for all samples. Other deposition conditions were also identical for all samples as indicated in Table I.

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The diffraction patterns become hazy [Fig. 2(c) and 2(d)] and a ring pattern appears [Fig. 2(e)]. In addition, the surface morphology of the Wright-etched sample becomes quite rough, showing the formation of high density defects in the grown film. This is because the energies of argon ions bombarding the surface were too excessive for the surface cleaning, thus damaging the substrate surface. As a result, highly defective silicon films were grown on the damaged substrate. The optimum ion bombardment condition for effective removal of contaminant species (such as adsorbed moisture molecules) from the substrate surface without causing any damages, has been obtained at a substrate bias voltage of + 7 V. One of the key issues for the high performance process "ultraclean wafer surface" has been thus realized.

On the other hand, the increase in the positive substrate bias voltage up to + 15 V has resulted in the deterioration of crystalline quality as indicated by the hazy diffraction pattern and the appearance of etch pits in the Wright-etched sample [Fig. 2(a)]. This resulted from the silicon deposition on the substrate surface occurring during the cleaning operation. The plasma potential was approximately 7 V under the cleaning condition, and the application of substrate bias in excess of 7 V caused the pushing up of the plasma potential since no electrode in the plasma can be positively biased with respect to the plasma. Since the estimated target bombardment energy at a substrate bias of + 15 V is approximately 40 eV which is nearly equal to the threshold energy for silicon sputtering by argon as determined from the linear extrapolation of the yield data in Ref. 22, sputtering of the target occurred during cleaning operation.

The period of surface cleaning was five minutes in this experiment. However, the increase in the period up to 30 min at the optimum condition ($V_s = +7$ V) did not change the crystallinity of grown films at all. This means damage-free surface cleaning has been achieved under the optimum condition of V_s, i.e., at $V_s = +7$ V. It should be noted that the surface cleaning operation introduced here is not the sputtering cleaning of the silicon surface in a usual sense. That is, if the surface layers are removed by Ar sputter etching, damages are introduced to the surface, and this is the case as shown in Figs. 2(c), 2(d), or 2(e). Since the ion bombardment energy for surface cleaning would be definitely in a few eV range (correct measurements were not carried out), only air molecules physically adsorbed on the surface are removed in the process.

A series of pictures shown in Fig. 3 demonstrates the crystallinity of grown silicon films as a function of substrate bias voltage applied during the film growth. The optimum surface cleaning condition was employed for all samples. The pictures in the left column and those in the right column represent the electron diffraction patterns and the Wright-etched sample surfaces observed by SEM, respectively (again, the surfaces of as deposited films were perfectly smooth). The target bias voltage was set at − 200 V and the substrate temperature was 300 °C, being common to all samples. The growth rate was about 1 Å/s and approximately 4000-Å-thick films were grown. At a substrate bias voltage of + 5 V, very sharp and strong Kikuchi lines are visible in the reflection electron diffraction pattern and the defect-free feature is evident in the Wright-etched sample. When the substrate bias was reduced from + 5 to − 15 V (which increases the ion bombardment energy), it is seen that the crystallinity of the film drastically deteriorates. The activation of growing film surface by ion bombardment with excess energies damages the film rather than to assist the crystal growth. On the other hand, the reduction in the ion bombardment energy by increasing the substrate bias from + 5 to + 20 V also deteriorates the film crystallinity. However, the degree of deterioration is much smaller as compared to the case of increasing the ion bombardment energy. At $V_s = +20$ V, Kikuchi lines become slightly weak and etch pits begin to appear in the Wright-etched sample. From these observations, the optimum ion bombardment condition exists for low-temperature silicon epitaxy, which was + 5 V of V_s under this specific experimental condition.

The HRTEM image of the film cross section at the surface, which was grown with the optimum deposition condition ($V_s = +5$ V), is shown in Fig. 4(a). A very clear lattice image in this figure demonstrates that a high-quality epitaxial silicon film was successfully grown at 300 °C. Formation of a very flat surface at the atomic level is also visible. Fig. 4(b) shows the HRTEM image of a silicon film grown at $V_s = -5$ V, demonstrating the formation of high density stacking faults in the silicon film. This resulted from the ion bombardment with an energy in excess of the optimum value. The difference in the ion energies in Figs. 4(a) and 4(b) is only 10 eV, which is enough to cause such a drastic change in the crystallinity. This fact indicates that high precision control of ion bombardment energy is quite essential in this process.

Figure 5 represents an HRTEM image taken at the interface between the epitaxial silicon layer and the substrate of the sample shown in Fig. 4(a). The lattice images of the substrate and the film perfectly match at the interface without any amorphous regions or defects. However, the interface is easily visible by the difference in the contrast. Although the reason for this is not clear at present, this might be originated from the elastic strain field and/or impurities incorporated at the interface.

The dependence of crystallinity on the combination of a target bias voltage (V_t) and a substrate bias voltage (V_s) is summarized as a map in Fig. 6. This map is approximately divided into three regions: a single-crystal region; a defective single-crystal region; an amorphous region. In the single-crystal region, the crystallinity changes depending on the substrate bias voltage is similar to those shown in Fig. 3 for $V_s = +5$– $+20$ V. The best quality films were obtained at bias conditions close to the boundary line. The defective single-crystal region is characterized by the HRTEM pictures shown in Fig. 4(b), while the amorphous region by halo reflection electron diffraction patterns as shown in Fig. 3 ($V_s = -15$ V). The boundary lines separating the adjacent two different crystal structure regions are approximately corresponding to equi-ion bombardment energy lines as discussed in Appendix A. Such results indicate that the crystallinity of a deposited film is essentially determined by the energy of argon ions concurrently bombarding a growing film surface.

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B. Dopant incorporation and electrical activation

In Fig. 7, phosphorus concentration profiles as measured by SIMS (secondary ion mass spectroscopy) analysis are given for (a) the phosphorus-doped silicon target and (b) for the epilayer grown using the target. The silicon film was deposited at $V_s = +5$ V and $V_t = -200$ V, i.e., at the optimum condition for epitaxy. It is seen from Fig. 7(b) that the concentration profile is very uniform within the grown layer and exhibits a very abrupt transition at the interface. Realization of such a well-defined impurity profile is of prime importance in application to high performance bipo-

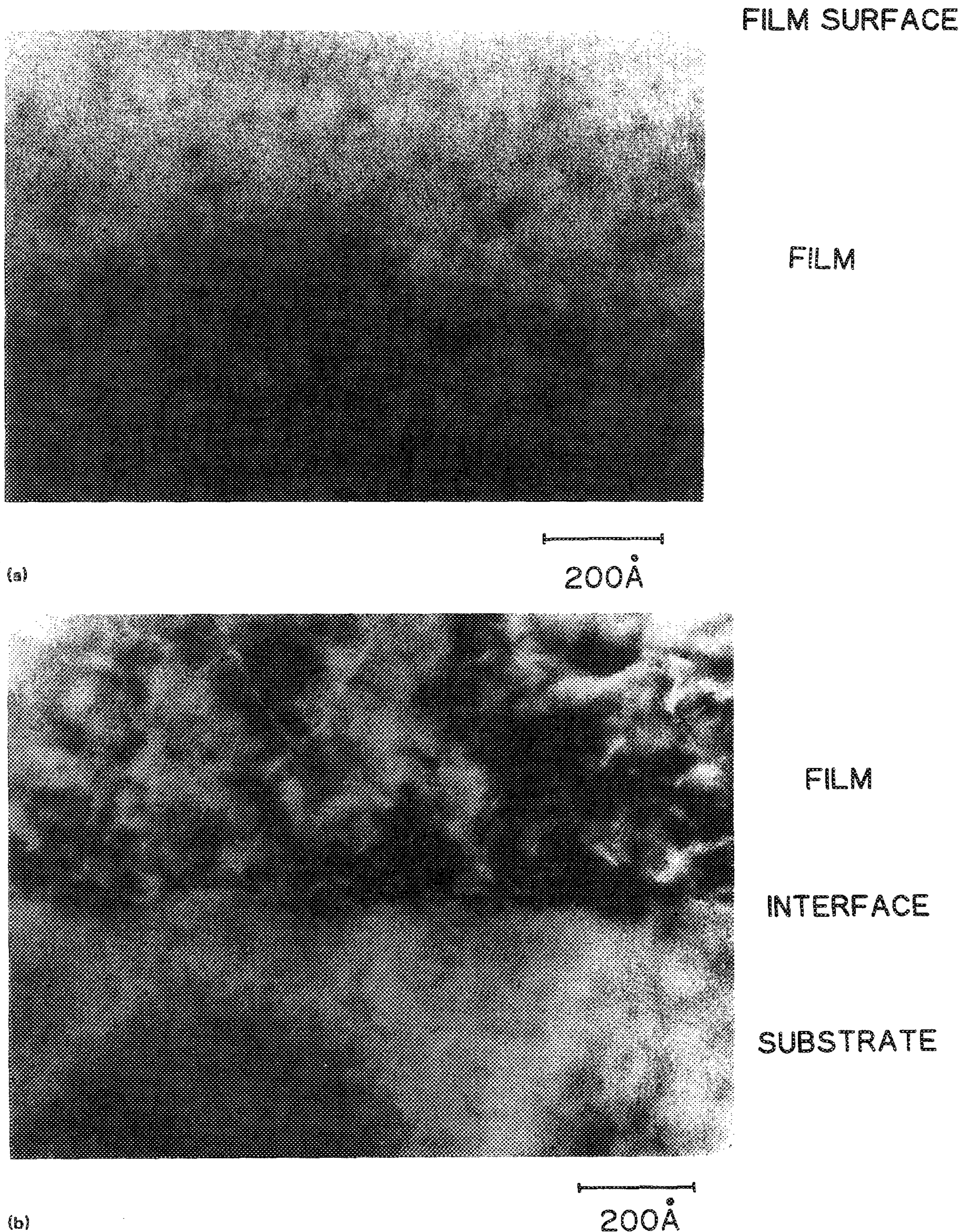

FIG. 4. (a) The HRTEM image of the film cross section at the surface which was formed under the optimum epitaxial growth condition. The electron beam was parallel to the ⟨110⟩ silicon axis. (b) The HRTEM image of the interface between the substrate and the deposited film formed under the inadequate epitaxial growth condition, i.e., ion bombardment energy was 10 eV higher than the optimum condition.

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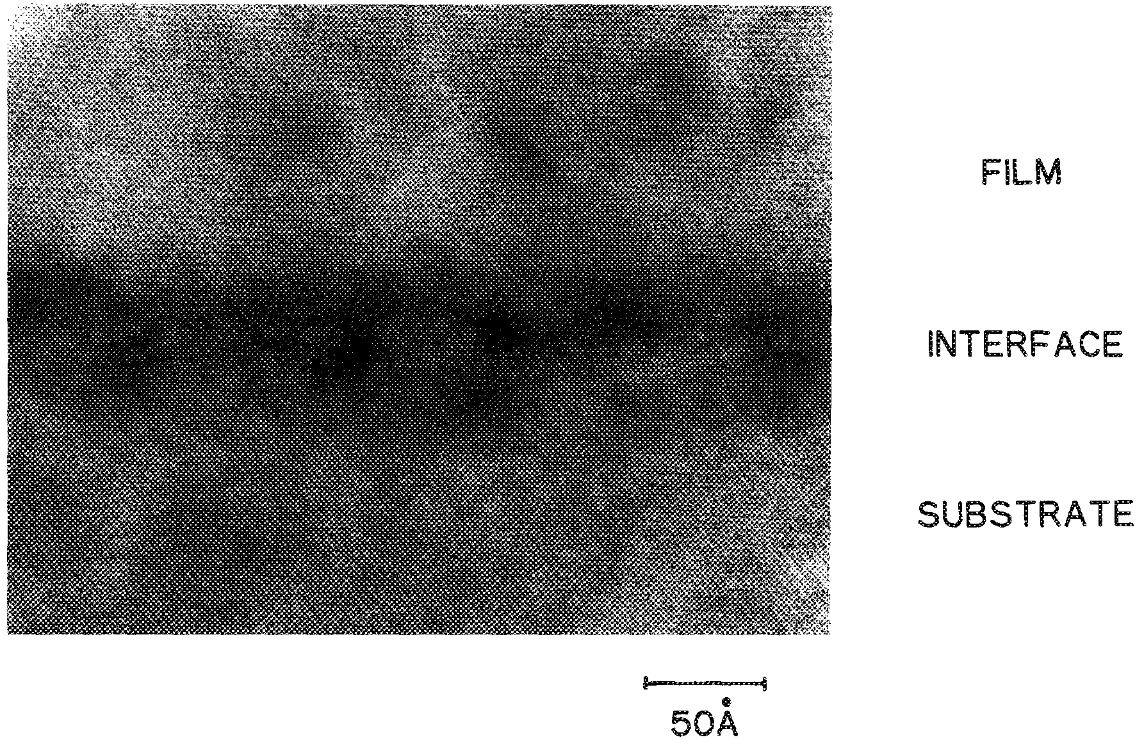


FIG. 5. The HRTEM image of the interface between the substrate and deposited film formed under the optimum epitaxial growth condition.

lar and CMOS devices that utilize epitaxial silicon layers with varying doping concentrations. It is important to note that the phosphorus concentrations in the film and in the target are approximately the same of $1.9\times10^{18}\ \mathrm{cm}^{-3}$ within an accuracy of the SIMS measurement. From this result, it is concluded that the dopant impurities in the target are fully incorporated into the deposited film without any loss. The dopant profile in the sample formed at $V_s = -15$ V and $V_t = -200$ V (at this condition, the resultant film was amorphous) was essentially the same as that in the single-crystal silicon shown in Fig. 7(b).

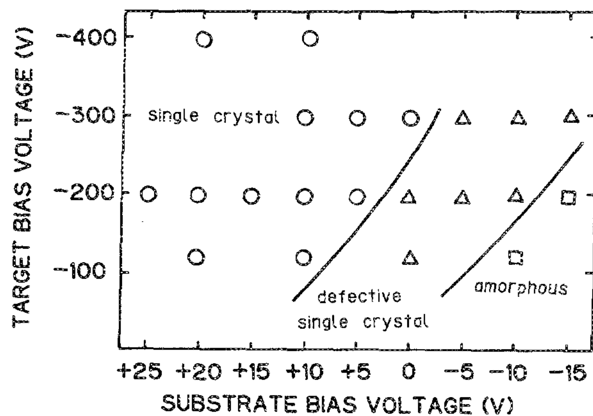
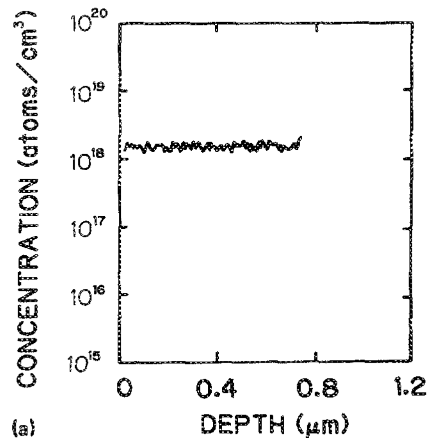


FIG. 6. Dependence of crystal structure on the substrate bias voltage (V_s) and the target bias voltage (V_t). Regions for single-crystal silicon, single-crystal silicon with high density defects, and amorphous silicon are shown.



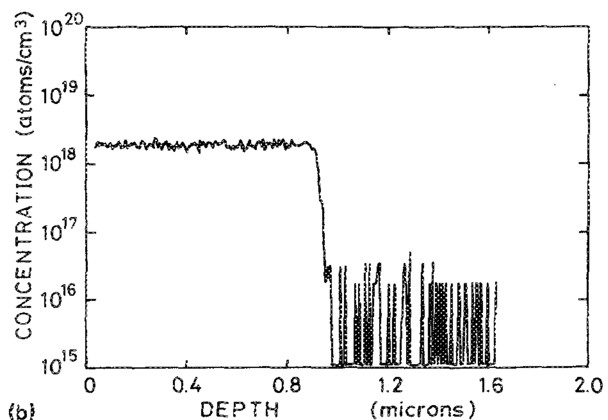


FIG. 7. Phosphorus concentration profiles (a) for the target and (b) for the epitaxially grown film.

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TABLE II. Dopant incorporation and electrical activation.

	Target	Epilayer
Dopant concentration (SIMS)	1.9×10^{18} cm^{-3}	1.9×10^{18} cm^{-3}
Carrier concentration	1.9×10^{18} cm^{-3}	1.9×10^{18} cm^{-3}
Electron Hall mobility	240 cm^2/V s	160 cm^2/V s
Resistivity	1.4×10^{-2} Ω cm	2.0×10^{-2} Ω cm

In order to investigate the electrical activation of incorporated impurities in the epitaxially grown layer, Hall measurements were carried out for both the target material and the epilayer grown at an optimum condition ($V_t = -120$ V and $V_s = +10$ V). The results are summarized in Table II. It is very important to note that the carrier concentrations are equal for the target and for the epilayer. It is concluded that the impurity in the target is fully incorporated into the lattice site of the epilayer. It is really a surprising result that a 100% electrical activation of dopants is achieved at a temperature as low as 300 °C. However, the resistivity of the epilayer is higher than that of the target, which is due to the decreased mobility measured for the film.

Figure 8 summarizes the results of Hall measurements for samples deposited at $V_t = -200$ V, showing the dependence of carrier concentration and Hall mobility on the substrate bias voltage. Gradual reduction in both Hall mobility and carrier concentration is seen for V_s values greater than $+10$ V, while abrupt reduction in carrier concentration is seen for V_s values smaller than $+5$ V, which indicates good correlation with the substrate bias dependence of crystallinity as is shown in Fig. 3.

Figure 9 shows the resistivity of a silicon film deposited using the phosphorus-doped silicon target as a function of the substrate bias voltage (V_s) for two different target bias voltages (V_t), -120 and -200 V. The resistivity becomes smallest at $V_s = +10$ and $+5$ V for $V_t = -120$ and -200 V, respectively. The V_s-V_t condition yielding the minimum of resistivity coincides well with that yields the best crystallinity of an epitaxially grown film (see Fig. 6). The overall dependence of resistivity on V_s has shown a good correlation with the crystallinity changes produced by ion bombardment with varying energies as described in Sec. IV A. In the case of $V_t = -200$ V, the resistivity of the film grown at $V_s = -5$ V in which high density of stacking faults were observed [see Fig. 4(b)] is nearly four orders of magnitude higher than that of the film formed at $V_s = +5$ V (which was a perfect single crystal). On the other hand, when V_s values were increased greater than $+5$ V, the resistivity increase is gradual, corresponding to the gradual degradation in the crystallinity as observed in Fig. 3.

When a heavily arsenic doped silicon target was used, a resistivity as low as 0.0014 Ω cm was obtained, indicating a large amount of donor impurities have been substitutionally incorporated into the silicon lattice sites and electrically activated in an epilayer grown at a temperature as low as 300 °C.

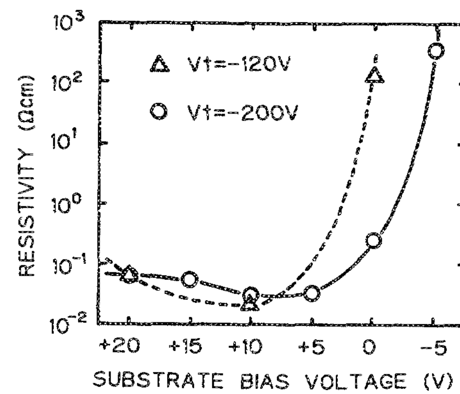

FIG. 9. Resistivity of a deposited silicon film as a function of the substrate bias voltage applied during the film growth for two different target bias voltages of -120 and -200 V.

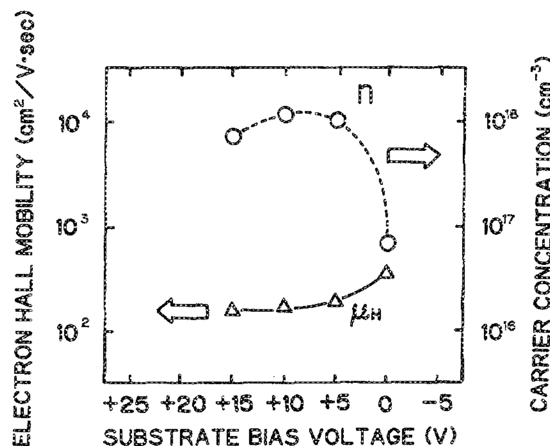

FIG. 8. Hall mobility and carrier concentration of a deposited silicon film ($V_t = -200$ V) as a function of the substrate bias voltage applied during the film growth.

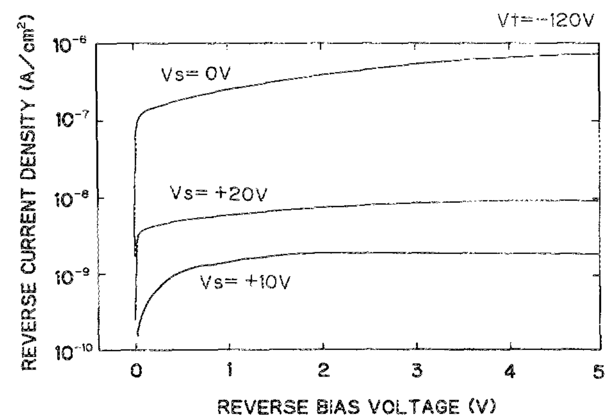

FIG. 10. Typical current-voltage characteristics of a 1×1 mm^2 p-n junction diodes fabricated by depositing an n-type epilayer directly on a p-type substrate. The film growth conditions were at $V_t = -120$ V and $V_s = +20$, $+10$, and 0 V.

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C. *p-n* junction characteristics

Figure 10 shows typical *I-V* characteristics of reverse biased *p-n* junctions. The diode size was 1×1 mm^2, and *n*-type epitaxial layers were grown on *p*-type substrates using the phosphorus-doped target. The growth conditions were $V_t = -120$ V and $V_s = +20$, $+10$, and 0 V. The current level at a reverse bias voltage of 5 V for the diode formed at the optimum condition for single-crystal growth ($V_s = +10$ V) is 1.88×10^{-9} A/cm^2, which is a very low reverse current level for diodes formed at such an extremely low temperature of 300 °C. Another sample ($V_s = +20$ and 0 V) shows much higher reverse current density than that formed at $V_s = +10$ V, again showing a good correlation with the crystallinity of epilayers.

The calculated depletion layer widths at a reverse bias voltage of 5 V for the *n* region and for the *p* substrate are 25.6 Å and 1.46 μm, respectively, indicating that the epitaxial layer-substrate interface is right in the midst of the depletion layer. It is worthwhile to note that such low reverse current diodes have been realized utilizing the original wafer surface as an interface of the *p-n* junction. Such remarkable results have been obtained through the establishment of the three key issues for high performance process discussed in Sec. II A.

In Fig. 11, the reverse-bias current of a 1×1 mm^2 *p-n* junction measured at a reverse-bias voltage of 3 V is shown as a function of the substrate bias voltage applied during the film growth. The data are shown for two different target voltages, viz., -120 and -200 V. The reverse-bias current level did not change appreciably at 3 and 5 V of the reverse bias voltage as is seen in Fig. 10. The data distribution within a wafer is represented by discrete points in the figure, showing very tight distribution. The minima observed in these curves correspond well to the V_s-V_t conditions yielding the best quality of the epitaxial silicon film. Again a good correlation has been obtained between the reverse-bias current level and the crystallinity, both of which change depending upon the substrate bias voltage applied during the film growth. All experiments described in this paper so far were carried out at a substrate temperature of 300 °C. Recently, further reduction in the epitaxial growth temperature down to 250 °C was achieved by optimizing the ion bombardment condition.[25,26] The reduction in the thermal energy by reducing the substrate temperature was compensated for by an increase in the total energy dose by ion bombardment. Here, the total ion flux for bombarding a growing film surface was increased keeping the individual ion energy at an optimum value of 25 eV. If the ion energy is increased, instead, the crystallinity degrades due to the defect formation. If a sufficient amount of ion flux is supplied, the epitaxial silicon growth at a room temperature will be, in principle, possible.[11]

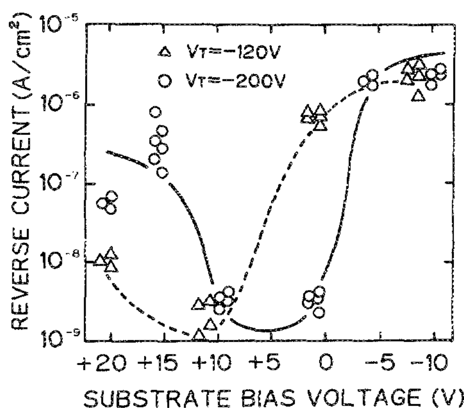

FIG. 11. Reverse bias current density in a 1×1 mm^2 *p-n* junction diode measured at a reverse bias voltage of 3 V as a function of the substrate bias voltage applied during the film growth.

V. CONCLUSION

The formation of device-grade epitaxial silicon films has been demonstrated at extremely low temperatures around 300 °C by low kinetic energy ion bombardment in conjunction with *in situ* substrate surface cleaning and ultra clean processing environment. The rf-dc coupled mode bias sputtering system was utilized to realize such a novel effect, where the film growth rate and the surface activation energy provided by low-energy ion bombardment were independently controlled.

Low-temperature *in situ* substrate surface cleaning was performed in order to obtain ultraclean wafer surface prior to the film deposition by very-low-energy ion bombardment. The crystal structure of a sputter-deposited silicon film was very sensitively changed by the energy of argon ions concurrently bombarding the growing silicon film surface. When the film was grown under the optimum condition, dopant impurities in the target material were fully incorporated into lattice sites of the epitaxially grown film and were 100% electrically activated without any additional heat cycles. When a heavily arsenic-doped silicon block was used as a target, an epitaxial silicon film having a resistivity as low as 0.0014 Ω cm was obtained. The *p-n* junction diodes utilizing the original wafer surfaces as their junction interfaces have exhibited quite low reverse-bias current levels of 1×10^{-9} A/cm^2, verifying the effectiveness of the *in situ* substrate surface cleaning by low-energy Ar-ion bombardment. Good correlations were observed between the electrical characteristics of the grown film such as the reverse bias current in a *p-n* junction or film resistivity to the crystal structure of the film, which was determined by low kinetic energy ion bombardment.

It should be commented that the addition of hydrogen to the Ar gas plasma would further improve the substrate surface cleaning process, resulting in improvements in the deposited film quality as well as the *p-n* junction interface characteristics. Such improvements in this novel low temperature process would make the low-kinetic energy process a key technology for future ULSI fabrication.

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versity. The authors wish to thank VLSI R&D Center, Oki Electric Industry Co., Ltd. for providing processed silicon wafers for the experiment, to T. Aiba, Canon Research Center, Canon Inc., to E. Aoyagi, Tohoku University, for the HRTEM observation on our samples, and to S. Yoshida and H. Takase, Canon Research Center, Canon Inc., for the SIMS measurements on our samples. This work is partially supported by the Grant-in-Aid for Scientific Research and Developmental Scientific Research (Nos. 62850050, 6240031, and 63850058) from the Ministry of Education, Science and Culture Japan.

APPENDIX A: PLASMA POTENTIAL MEASUREMENT

Figure 12 shows the floating potential of the target electrode (V_{ft}) as a function of the positive bias voltage applied to the substrate holder (V_s) for three rf powers. As is seen in the figure, V_{ft} is constant for V_s up to a certain value, above which V_{ft} increases (become less negative) linearly with an increase in V_s. The data for an rf power of 5 W, for instance, show a kink at about $V_s = +7$ V. The constant value of V_{ft} for V_s below the kink is the self-bias voltage appearing on the target, which is about -20 V for the rf power of 5 W. The self-bias voltage was alternatively determined by measuring the target current-voltage characteristics, in which the target bias voltage at zero current yielded the self-bias voltage. The results of these two measurements were in good agreement.

The V_s at the kink is interpreted as roughly equal to the plasma potential. As V_s increases, i.e., as the substrate holder potential approaches close to the plasma potential, a large number of electrons flow into the electrode, thus causing the deficit of electrons in the plasma, and the plasma potential eventually increases (become more positive). The pushing up of the plasma potential by the positively biased substrate holder electrode would presumably occur when the electrode potential becomes roughly equal to the plasma potential. And when it happens, the target floating potential is also pulled up, giving rise to the kinks in Fig. 12. This is why the V_s at the kink was taken as a measure of the plasma potential.

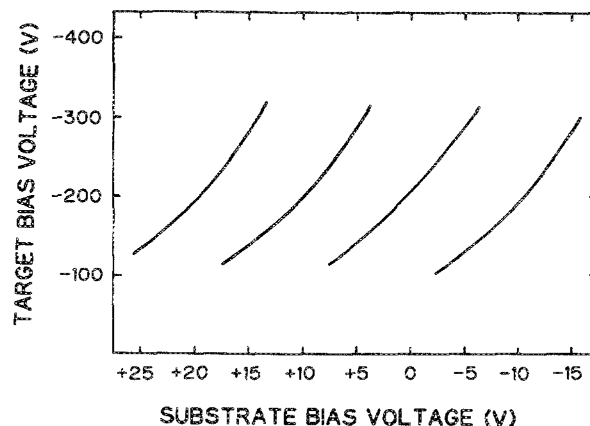

FIG. 13. Equi-ion-bombardment energy lines for the combination of V_s and V_t.

Figure 13 shows equi-ion-bombardment energy lines for the combination of V_s and V_t where the plasma potential was estimated from *I-V* characteristics of the substrate holder as described above. These lines are in good coincidence with the boundary lines separating different crystal structure regions in Fig. 6.

APPENDIX B: SUBSTRATE TEMPERATURE MEASUREMENT

Determination of the wafer temperature is most essential in this work. The methods for wafer heating and the temperature measurements are described here. Heating of a wafer was carried out using a tantalum heater mounted in the wafer holder, and the wafer temperature was measured using a two color pyrometer (2.05 and 2.35 μm) before and after film deposition through a view port of the vacuum chamber. The backside of the wafer used in this study was all

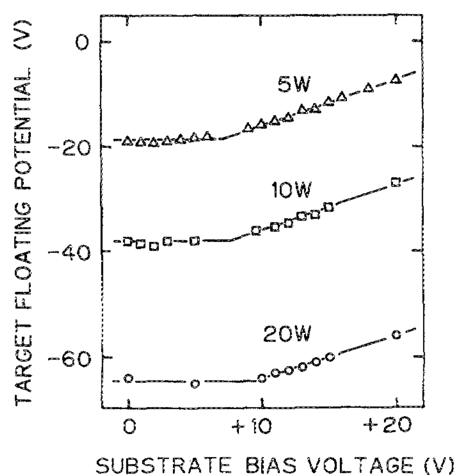

FIG. 12. Target floating potential (V_{ft}) as a function of substrate bias voltage (V_s) for three rf powers.

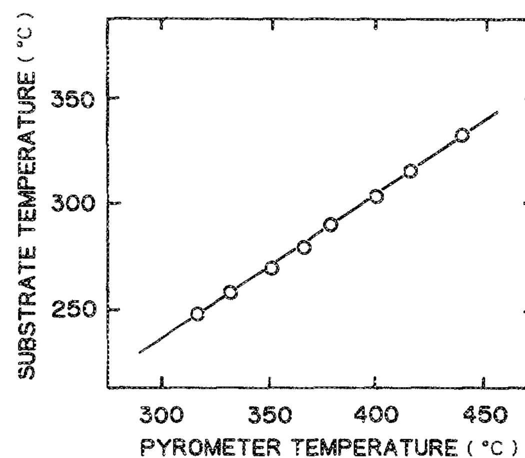

FIG. 14. Calibration curve between the true substrate temperature and the read of the pyrometer used for temperature measurement.

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metallized with a 0.3-μm-thick tungsten silicide layer in order to enhance the electrical contact between the wafer and the holder for dc biasing. Since this tungsten silicide layer very effectively shields the IR radiation from the wafer holder, only IR radiation from the wafer was detected at the pyrometer. It was read by the pyrometer and calibrated by directly measuring the wafer temperature by a separate technique. This was carried out using a thermocouple directly connected to a silicon wafer. The calibration curve thus obtained is presented in Fig. 14. As the result of such careful temperature calibration, we found that the temperature we cited in the previous articles (epitaxial temperature of 320–350 °C)[13-16] has to be corrected to 300 °C.

[1]T. Ohmi, *Proceeding of 1986 SEMI Technology Symposium* (Semiconductor Equipment and Materials International, 1986), p. A.1.

[2]B. S. Meyerson, F. K. LeGoues, T. N. Nguyen, and D. L. Harame, Appl. Phys. Lett. **50**, 113(1987).

[3]W. R. Burger and R. Reif, J. Appl. Phys. **63**, 383 (1988).

[4]W. R. Burger and R. Reif, IEEE Electron Device Lett. **EDL-7**, 2068 (1986).

[5]W. R. Burger and R. Reif, J. Appl. Phys. **62**, 4255 (1987).

[6]A. Ishizaka and Y. Shiraki, J. Electrochem. Soc. **133**, 666 (1986).

[7]T. Sugiyama and T. Itoh, J. Electrochem. Soc. **133**, 604 (1986).

[8]T. Itoh, T. Nakamura, M. Muromachi, and T. Sugiyama, Jpn. J. Appl. Phys. **16**, 553 (1977).

[9]P. C. Zalm and L. J. Beckers, Appl. Phys. Lett. **41**, 167 (1982).

[10]C. Schwebel, F. Meyer, G. Gautherin, and C. Pellet, J. Vac. Sci. Technol. B **4**, 1153 (1986).

[11]I. Yamada, F. W. Saris, T. Takagi, K. Matsubara, H. Takaoka, and S. Ishiyama, Jpn. J. Appl. Phys. **19**, L181 (1980).

[12]T. Ohmi, H. Kuwabara, T. Shibata, and T. Kiyota, ULSI Science and Technology/1988 **87-11**, 761 (1988).

[13]T. Ohmi, T. Ichikawa, T. Shibata, K. Matsudo, and H. Iwabuchi, Appl. Phys. Lett. **53**, 45 (1988).

[14]T. Ohmi, K. Matsudo, T. Shibata, T. Ichikawa, and H. Iwabuchi, Appl. Phys. Lett. **53**, 364 (1988).

[15]T. Ohmi, H. Iwabuchi, T. Shibata, and T. Ichikawa, Appl. Phys. Lett. **54**, 253 (1989).

[16]T. Ohmi, T. Ichikawa, T. Shibata, and H. Iwabuchi, Appl. Phys. Lett. **54**, 523 (1989).

[17]T. Ohmi, T. Saito, T. Shibata, and T. Nitta, Appl. Phys. Lett. **52**, 2236 (1988).

[18]T. Ohmi, H. Kuwabara, T. Shibata, N. Kowata, and K. Sugiyama, in *Proceedings 5th International IEEE VLSI Multilevel Interconnection Conference*, IEEE Catalog No. 88CH2624-5 (IEEE, New York, 1988), p. 446.

[19]H. Kuwabara, S. Saito, T. Shibata, and T. Ohmi, Dig. Tech. Papers, 1989 Symp. VLSI Technol., Kyoto, Vol. 71 (1989).

[20]T. Ohmi, Microcontamination **6**, 49 (1988).

[21]T. Ohmi, Oyo Buturi **58**, 193 (1989).

[22]T. Ohmi, N. Mikoshiba, K. Tsubouchi, S. Broydo, and C. M. Osburn, Eds., *ULSI Science and Technology/1988, 87-11* (The Electrochemical Society, Pennington, NJ, 1988), p. 761.

[23]T. Ohmi, J. Murota, Y. Kanno, Y. Mitsui, K. Sugiyama, T. Kawasaki, and H. Kawano, Eds., *ULSI Science and Technology/1988, 87-11* (The Electrochemical Society, Pennington, NJ, 1988), pp. 574 and 805.

[24]R. Behrisch, Ed., *Sputtering by Particle Bombardment* (Springer, Berlin, 1981), p. 168.

[25]K. Hashimoto, T. Ichikawa, H. Iwabuchi, T. Shibata, and T. Ohmi, in *Proceedings of 1989 International MicroProcess Conference, Kobe, Japan* (The Japan Society of Applied Physics, 1989), p. 116.

[26]T. Ohmi, K. Hashimoto, and T. Shibata (unpublished).

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