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Model for the substrate hole current based on thermionic hole emission from the anode during Fowler–Nordheim electron tunneling in *n*-channel metal-oxide-semiconductor field-effect transistors

Kiyoteru Kobayashi, Akinobu Teramoto, and Makoto Hirayama

ULSI Laboratory, Mitsubishi Electric Corporation, 4-1 Mizuhara, Itami, Hyogo 664, Japan

Yasushi Fujita

Ryouden Semiconductor System Engineering Corporation, 4-1 Mizuhara, Itami, Hyogo 664, Japan

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A model is proposed to explain the dependence of the substrate hole current in *n*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on applied electric field and on oxide thickness. Two types of devices were prepared: *n*-channel MOSFETs with gate oxides of 67, 86, and 131 Å and *p*-channel MOSFETs in which gate oxide thicknesses were almost equal to those in the *n*-channel MOSFETs. The carrier-separation technique was used in the *p*-channel MOSFETs, and the average energy of hot electrons entering the silicon substrate was obtained. The average energy of the hot electrons is related to the energy distribution of hot holes created by hot electrons emitted from the oxide into the n^+ polysilicon gate during the Fowler–Nordheim electron tunneling in the *n*-channel MOSFETs. The substrate hole current is numerically modeled as thermionic emission of the hot holes overcoming the energy barrier at the oxide- n^+ polysilicon interface. For the gate oxides ranging from 67 to 131 Å, the dependence of the substrate hole current on the electric field and on oxide thickness is explained by using the average energy of the hot electrons and the thermionic hole emission model. © 1995 American Institute of Physics.

I. INTRODUCTION

Dielectric instabilities and breakdown in electrically stressed silicon dioxide (SiO_2) have received a lot of attention because of their importance to reliability in silicon large-scale integration. It has been reported that oxide degradation occurs due to hole injection into the oxide.^{1–3} It has been suggested that oxide wearout and breakdown during the Fowler–Nordheim electron tunneling is attributed to hole generation and trapping at defect sites.^{4–11} It is, therefore, important to study the hole generation process.

Hole current appears in the *p*-type substrate of *n*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) when electrons are injected from the channel into the silicon oxide due to Fowler–Nordheim tunneling. Several authors have studied the substrate hole current.^{9,12–16} Weinberg and co-workers pointed out that impact ionization in the oxide is a difficult explanation for origin of the substrate hole current in the *n*-channel MOSFET with a 70 Å oxide, since the maximum energy that electrons can gain in such a thin oxide is too small to cause direct band-to-band impact ionization in the oxide.¹³ They also showed that, for oxides ranging from 70 to 825 Å, the ratio of the substrate hole current to the channel electron current is substantially reduced for thinner oxides at constant electric field.¹³ This is strong evidence against the model of electron tunneling from the silicon valence band for the oxides in this thickness range. They claimed that the substrate hole current is related to effects occurring in the oxide.¹³ The generation mechanism of the substrate current, however, remains difficult to explain. Chen *et al.* suggested that the substrate current in oxides thinner than 45 Å is dominated by the tunneling of the valence-band electrons.⁹ They also claimed that, for oxides thicker than 45 Å, electric fields higher than 8 MV/cm, and

applied gate voltages higher than 6 V, holes are generated in the oxide.⁹ The mechanism of hole generation, however, remains unknown. Fischetti quantitatively analyzed the following model.¹¹ The electrons injected into the oxide gain energy during their transport in the oxide. A significant fraction of electrons lose energy at the anode-oxide interface by emitting surface plasmons. The excited surface plasmons decay quickly into electron-hole pairs. A small fraction of these holes can be injected into the oxide. He calculated the quantum efficiency for one injected electron to produce the tunneling of one hole into the oxide,¹¹ but the effect of the oxide thickness was not taken into account. For oxides ranging from 245 to 957 Å, it has been presented that the substrate hole current at high fields can be quantitatively predicted by simulation and can be attributed mostly to band-gap ionization in the oxide.^{14,15}

As shown in the previous studies,^{9,13–16} the substrate hole current is very dependent on applied electric field and oxide thickness. There is, however, no quantitative explanation that determines such dependence of the substrate hole current for oxides ranging from 45 to 245 Å. It is still an interesting issue to discuss the origin of the substrate hole current for oxides in this thickness range. In this article, a model is proposed to explain the dependence of the substrate hole current in *n*-channel MOSFETs on the electric field in the oxide and on oxide thickness.

We prepared two types of devices: *n*-channel MOSFETs with gate oxides of 67, 86, and 131 Å, and *p*-channel MOSFETs in which the gate oxide thicknesses used were almost equal to those in the *n*-channel MOSFETs. The carrier-separation technique in *p*-channel MOSFETs measures the number of electron-hole pairs produced by hot electrons entering the silicon substrate from the oxide.^{17–20} The

number of pairs is then related to the average energy of the incident hot-electron distribution by the theory of Alig, Bloom, and Struck.^{17,18,21} We used the carrier-separation technique in the *p*-channel MOSFETs in order to obtain the average energy of hot electrons entering the silicon substrate. The average energy of the hot electrons is related to the energy distribution of hot holes produced near the anode-SiO₂ interface in the *n*-channel MOSFETs. The substrate hole current is numerically modeled as thermionic emission of the hot holes overcoming Si-SiO₂ energy barrier. For the oxides within the thickness range of 67–131 Å, we explain the dependence of the substrate hole current on the electric field in the oxide and the oxide thickness by using the average energy of the hot electrons and the thermionic hole emission model.

II. SAMPLE PREPARATION

p-type (100) silicon substrates with resistivity of 8.5–11.5 Ω cm were used in this study. *n*-channel transistors were fabricated on the *p*-type substrates with standard MOS technology. *p*-channel transistors were fabricated on the *n*-well regions in the *p*-type substrates. Gate oxides were simultaneously grown for both the *n*- and *p*-channel MOSFETs using pyrogenic oxidation at 820 °C. Gate electrodes were formed from *in situ* phosphorous-doped polysilicon. The thickness of the polysilicon film was 2000 Å and the phosphorous concentration was $5\text{--}7 \times 10^{20} \text{ cm}^{-3}$. The source-drain regions were doped by arsenic ion implantation for the *n*-channel, and by boron ion implantation for the *p*-channel MOSFETs. After the diffusion and aluminum metallization, all the devices were annealed in a 450 °C hydrogen ambient furnace. Gate oxide thicknesses in the *n*-channel MOSFETs were 67, 86, and 131 Å. The *p*-channel MOSFETs contained oxide thicknesses of 69, 87, and 130 Å which were almost identical to those in the *n*-channel MOSFETs. The oxide thicknesses t_{ox} were calculated from the capacitance using the relative dielectric constant of 3.85. The gate area in the *n*-channel MOSFETs was $8.1 \times 10^{-3} \text{ cm}^2$. The gate area in the *p*-channel MOSFETs was $1.0 \times 10^{-4} \text{ cm}^2$.

In the *n*-channel MOSFETs, the electron current was measured from the channel contact (source drain) and the hole current was measured from the substrate contact. In the *p*-channel MOSFETs, the hole current was measured from the channel contact and the electron current was measured from the substrate contact.

III. RESULTS AND DISCUSSION

A. Characteristics and modeling of substrate hole current in *n*-channel MOSFETs

In *n*-channel MOSFETs, the channel current $I_{n,\text{ch}}$ is due to the Fowler–Nordheim tunneling electrons injected into the oxide from the surface inversion layer when the gate is biased with grounded source and drain, as shown in Fig. 1. The hole current $I_{p,\text{sub}}$ appears in the *p*-type substrate. Figure 2 shows the channel current density $J_{n,\text{ch}}$ and the substrate cur-

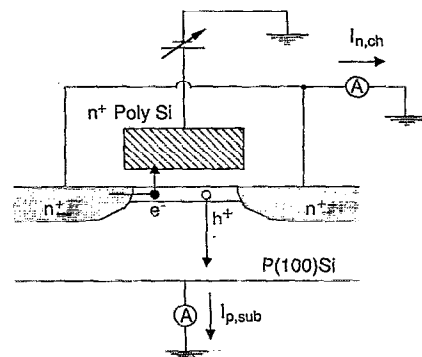


FIG. 1. Schematic of the experimental setup of an *n*-channel MOSFET for measuring the channel electron current $I_{n,\text{ch}}$ due to the Fowler–Nordheim tunneling and the substrate hole current $I_{p,\text{sub}}$. The gate is biased with grounded source and drain.

rent density $J_{p,\text{sub}}$ as functions of electric field E_{ox} for the 67, 86, and 131 Å oxides. The voltage across the gate oxide V_{ox} and the E_{ox} are defined by

$$V_{\text{ox}} = V_g - V_{\text{FB}} - 2\phi_F \quad (1)$$

and

$$E_{\text{ox}} = V_{\text{ox}} / t_{\text{ox}}, \quad (2)$$

where V_g is the voltage applied to the gate electrode, V_{FB} is the flatband voltage, and $2\phi_F$ is the surface potential for the silicon substrate-oxide interface. We can see that all $J_{n,\text{ch}} - E_{\text{ox}}$ curves exhibit the same Fowler–Nordheim characteristic, while $J_{p,\text{sub}}$ is smaller for the thinner oxide. The ratio $J_{p,\text{sub}} / J_{n,\text{ch}}$ vs V_{ox} is shown in Fig. 3(a). This ratio is a strong function of both V_{ox} and oxide thickness. The ratio is replotted versus E_{ox} in Fig. 3(b). The ratio is also a strong function of E_{ox} , and is substantially reduced with the reduction in oxide thickness. These results in Figs. 3(a) and 3(b) are in agreement with those of Weinberg and co-workers.¹³

We will explain the dependence of the substrate hole current on E_{ox} and t_{ox} on the basis of a model described in

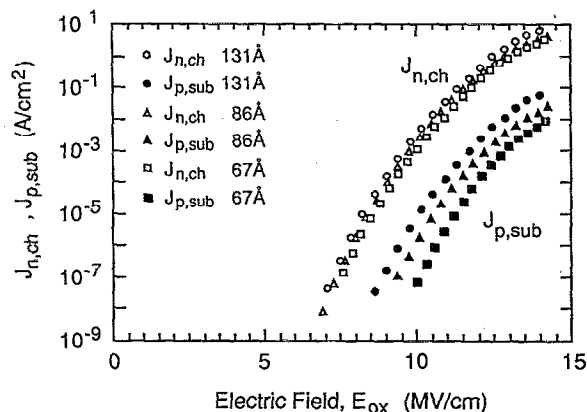


FIG. 2. The channel electron current density $J_{n,\text{ch}}$ and the substrate hole current density $J_{p,\text{sub}}$ as functions of the electric field in the oxide E_{ox} for the 67, 86, and 131 Å oxides.

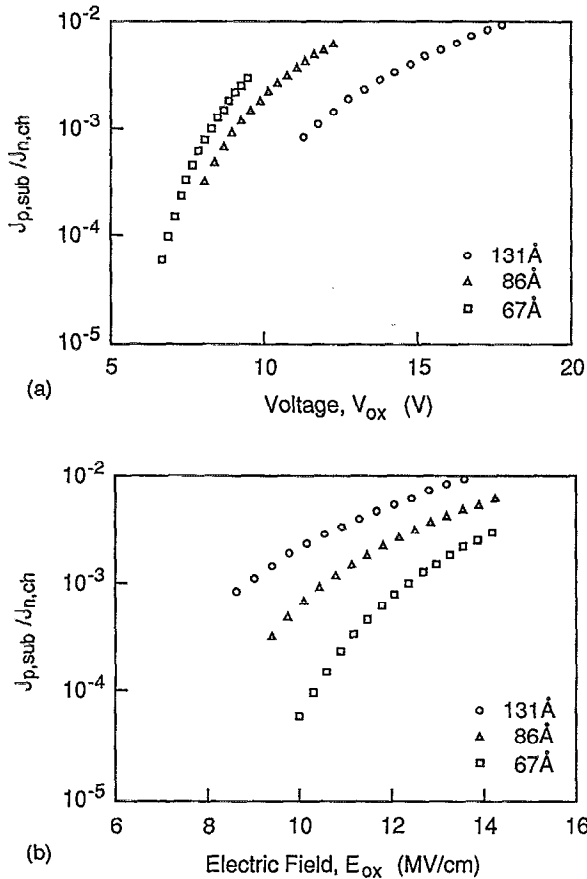


FIG. 3. (a) $J_{p,\text{sub}}/J_{n,\text{ch}}$ ratio as a function of the voltage across the oxide V_{ox} . (b) $J_{p,\text{sub}}/J_{n,\text{ch}}$ ratio as a function of the electric field in the oxide E_{ox} .

this paragraph. Figure 4 illustrates the schematic band diagram that shows the hole injection mechanism. Electrons are first injected into the conduction band of SiO_2 due to Fowler–Nordheim tunneling. Since the electric field is very high, electrons will gain kinetic energy from the field in the oxide and will lose energy by phonon scatterings.^{14,18,19} The

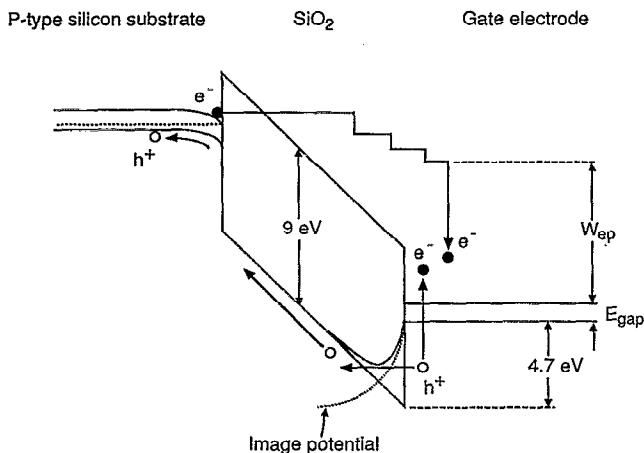


FIG. 4. Schematic energy-band diagram showing the emission of a hot electron from the SiO_2 into the gate electrode and the injection of a generated hole into the SiO_2 in an n -channel MOSFET.

electrons will become hot in the oxide. The hot electrons entering the anode (n^+ polysilicon) will lose energy by emitting phonons, by impact ionization, and possibly by creating plasmons,¹¹ and will produce electron-hole pairs. The energy of the electrons entering the n^+ polysilicon is converted in part to electron-hole pairs. The holes that are generated with enough energy to overcome the potential barrier at the oxide- n^+ polysilicon interface will be emitted into the valence band of the oxide,¹² and will contribute to the substrate hole current.

In the above model, the substrate hole current is explained as thermionic emission of the hot holes created by the hot electrons emitted from the oxide into the n^+ polysilicon. Here, a fraction of the hot holes in the high-energy tail of distribution can be emitted into the oxide. The emission probability of holes may be a function of the energy of the generated hot holes, and of the potential barrier height at the oxide-anode interface. As far as we know, there is no exact knowledge of the energy distribution of the hot holes. In order to derive the analytical formula in absence of the exact knowledge of the distribution, we assume the high-energy tail of the hot-hole distribution to have a Maxwell–Boltzmann distribution characterized by an effective hole energy W_{hg} , then at steady state the substrate hole current density can be written as

$$J_{p,\text{sub}} = qn_s \left(\frac{W_{hg}}{2\pi m_h^*} \right)^{1/2} \exp\left(-\frac{q\Phi_h}{W_{hg}}\right), \quad (3)$$

where n_s is the density of the generated holes at the oxide- n^+ polysilicon interface, q is the electric charge, m_h^* is the effective mass of a hole, and Φ_h is the energy barrier height for holes between the oxide and the n^+ polysilicon.

The image force lowers the barrier at the oxide- n^+ polysilicon interface. The Schottky-lowered barrier for the hole emission is expressed by

$$q\Phi_h = q\Phi_b - \beta E_{\text{ox}}^{1/2}, \quad (4)$$

where the Si- SiO_2 interface barrier $q\Phi_b$ is 4.7 eV,¹¹ and β is given by

$$\beta = (q^3/4\pi\epsilon_0\epsilon_{\text{ox}})^{1/2}. \quad (5)$$

Here ϵ_0 is the dielectric constant of free space and ϵ_{ox} is the dielectric constant of SiO_2 .

The energy of electrons entering the n^+ polysilicon gate is converted in part to electron-hole pairs. Several authors have studied the electron-hole-pair generation phenomena using the carrier-separation technique under negative gate bias in p -channel MOSFETs.^{17–20} Carrier separation measures the average energy of electrons transported at high fields from the gate into the silicon substrate.^{18,20} As the energy of the electrons emitted into the silicon substrate is increased, the number of electron-hole pairs created by one electron, i.e., the quantum yield γ , is increased.²¹ Holes and electrons can be independently counted by measuring the channel hole current and the substrate electron current. A measurement of the ratio between the hole and electron currents allows the determination of the average energy of the electrons emitted into the silicon substrate.^{18,20} We assume that the average energy of the electrons emitted into the

silicon substrate, which is measured by the carrier separation in a p -channel MOSFET, is equal to the average energy W_{ep} of the electrons entering the n^+ polysilicon gate in an n -channel MOSFET when the gate oxide thickness and the electric field in the oxide of the p -channel MOSFET are identical with those of the n -channel MOSFET. Chang and co-workers showed that the electric field in the depletion region in the p -channel MOSFET does not appreciably affect the electron-hole pair creation process in the silicon substrate.¹⁷ This fact supports the above assumption.

In Fig. 4, one primary electron emitted from the oxide into the n^+ polysilicon gate can lose part of its energy by creating an electron-hole pair and/or emitting phonons. The rest of the energy remains in the scattered primary electron. The pair creation process is characterized by a threshold energy below which the probability of pair creation is nil.²¹⁻²³ If a secondary carrier (a scattered primary, a created electron, or a created hole) has an energy higher than the threshold, its energy can be also lost by creating one more pair and/or emitting phonons. Carriers with energies in excess of the threshold have the probability of creating more pairs. The average number of the electron-hole pairs originated by one primary electron is the quantum yield in the n^+ polysilicon gate. The creation of one electron-hole pair requires the band-gap energy of Si. The initial kinetic energy of a primary electron minus the band-gap energy is shared out among the three secondary carriers (the scattered primary electron, the created electron, and the created hole) and the emitted phonons.²¹⁻²³ Kane computed the energy distribution of secondary carriers created by a primary electron for several primary energies.²³ In the result, we can see that the energy of the primary electron is several times higher than the average energy of the distribution of secondary carriers. At the subsequent pair-creation event, the kinetic energy of a secondary carrier minus the band-gap energy is distributed among the three-product carriers (one scattered secondary carrier and the newly created electron and hole) and the emitted phonons. Focusing on the energy of holes, the average energy of the distribution of the secondary holes will be several times higher than the average energy of the distribution of the scattered secondary holes or the holes created by the secondary carriers. Therefore, the secondary holes make up a significant part of the high-energy tail of the hot-hole distribution. Therefore, the secondary holes make up a significant part of the high-energy tail of the hot-hole distribution. At the first pair-creation event, the primary energy of the injected electron minus the band-gap energy is converted in part to the secondary hole. We assume that the energy of the secondary hole has a linear relation to the primary energy of the injected electron minus the band-gap energy. As a simple approximation of the high-energy tail, we take into account only the contribution of secondary holes. The shape of the energy distribution of hot holes is considerably affected by the distribution of the secondary holes. Then the effective hole energy with respect to the top of the Si valence band is approximately expressed as

$$W_{hg} = C(W_{ep} - E_{\text{gap}}), \quad (6)$$

where E_{gap} is the band-gap energy of Si, and C is a fitting

parameter which depends on the average ratio of the hole energy to the primary energy of the injected electron, and on the shape of the high-energy tail of the hot-hole distribution. The average energy W_{ep} of the electrons entering the n^+ polysilicon is determined from the carrier separation in the p -channel MOSFETs in Sec. III B. The coefficient C is taken to be constant, and is determined by fitting experimental data in Sec. III C.

The holes generated by the incoming hot electrons may be recombined with electrons in the n^+ polysilicon gate. This generation-recombination process is expressed by the following equation with the quantum yield γ

$$\frac{dN_h}{dt} = \frac{\gamma J_{n,\text{ch}}}{q} \frac{N_h - N_{h0}}{\tau_p}, \quad (7)$$

where N_h is the hole concentration per unit gate area, N_{h0} is the thermal-equilibrium hole concentration per unit gate area, and τ_p is the average hole lifetime in the n^+ polysilicon. At steady state, $dN_h/dt=0$ and

$$N_h - N_{h0} = \frac{\tau_p \gamma J_{n,\text{ch}}}{q}. \quad (8)$$

High-energy electrons are injected into the n^+ polysilicon gate from the oxide only, and may create electron-hole pairs near the oxide- n^+ polysilicon interface corresponding to the plane $x=0$. The generated holes diffuse inward in the n^+ polysilicon gate and are simultaneously recombined with electrons. The steady-state hole distribution within the n^+ polysilicon gate satisfies the equation

$$\frac{\partial p_n}{\partial t} = 0 = -\frac{p_n - p_{n0}}{\tau_p} + D_p \frac{\partial^2 p_n}{\partial x^2}, \quad (9)$$

subject to the boundary condition $p_n(0) = \text{const}$ and

$$\int_0^d [p_n(x) - p_{n0}] dx = N_h - N_{h0}. \quad (10)$$

Here $p_n(x)$ is the hole density at position x in the n^+ polysilicon gate, p_{n0} is the thermal-equilibrium hole density, D_p is the hole diffusion constant, and d is the thickness of the n^+ polysilicon gate. The solution of Eq. (9) is

$$p_n(x) - p_{n0} = \frac{N_h - N_{h0}}{L_p [1 - \exp(-d/L_p)]} \exp\left(-\frac{x}{L_p}\right), \quad (11)$$

where L_p is the diffusion length and is defined by $L_p \equiv \sqrt{D_p \tau_p}$. From Eqs. (8) and (11), the density of the generated holes at the oxide- n^+ polysilicon interface is given by

$$n_s = p_n(0) - p_{n0} = \frac{\tau_p \gamma J_{n,\text{ch}}}{q L_p} \frac{1}{1 - \exp(-d/L_p)}. \quad (12)$$

From Eqs. (3), (4), (6), and (12), we rewrite the substrate hole current density as

$$J_{p,\text{sub}} = A \gamma J_{n,\text{ch}} \left(\frac{C(W_{ep} - E_{\text{gap}})}{2\pi m_h^*} \right)^{1/2} \times \exp\left(-\frac{q\Phi_b - \beta E_{\text{ox}}^{1/2}}{C(W_{ep} - E_{\text{gap}})}\right), \quad (13)$$

where

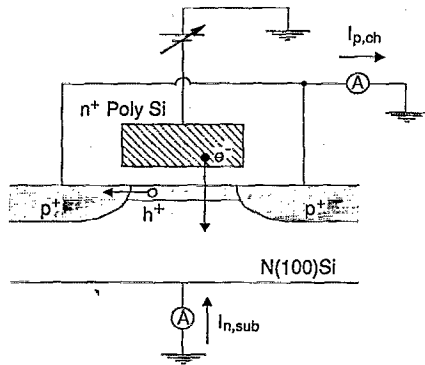


FIG. 5. Schematic diagram of a p -channel MOSFET showing an experimental setup for carrier separation.

$$A \equiv \frac{\tau_p}{L_p} \frac{1}{1 - \exp(-d/L_p)} \quad (14)$$

B. Determination of the average energy of incident electrons

We determine the average energy of the electrons entering the n^+ polysilicon gate in the n -channel MOSFETs in this section. Figure 5 illustrates the schematic diagram of a p -channel MOSFET showing an experimental setup for the carrier separation. Electrons injected from the gate into the oxide by Fowler–Nordheim tunneling are transported at a high field and become hot in the oxide. The hot electrons entering the silicon substrate lose energy by emitting phonons and by impact ionization, and they create electron-hole pairs in the substrate.^{17,21} The generated electron-hole pairs are separated. The generated holes are collected to the substrate surface and flow out the drain and source as a channel current $I_{p, ch}$. The generated electrons and the primary electrons entering the silicon substrate are measured as the substrate current $I_{n, sub}$. The quantum yield γ of the incoming hot electrons is given by¹⁷

$$\gamma = \frac{I_{p, ch}}{I_{n, sub} - I_{p, ch}} \quad (15)$$

Figure 6(a) shows the measured quantum yields as a function of the voltage across the oxide V_{ox} for the 69, 87, and 130 Å oxides. The oxide thicknesses in the p -channel MOSFETs were almost equivalent to those in the n -channel MOSFETs. The quantum yield γ is replotted in Fig. 6(b) as a function of E_{ox} and decreases with the reduction in oxide thickness. The quantum yield γ is related to the average energy of the hot electrons entering the silicon substrate by the theory of DiMaria *et al.*¹⁸ and Alig and co-workers²¹ and the relationship has been plotted by Chang and co-workers.¹⁷ The average energy W_{avg} of these hot electrons with respect to the bottom of the Si conduction band is shown in Fig. 7 as a function of E_{ox} .

As described in Sec. III B, we assume that the average energy W_{avg} of the hot electrons which is obtained from the carrier separation in a p -channel MOSFET is equal to the average energy W_{ep} of the electrons entering the n^+ polysilicon in an n -channel MOSFET when the gate oxide thickness

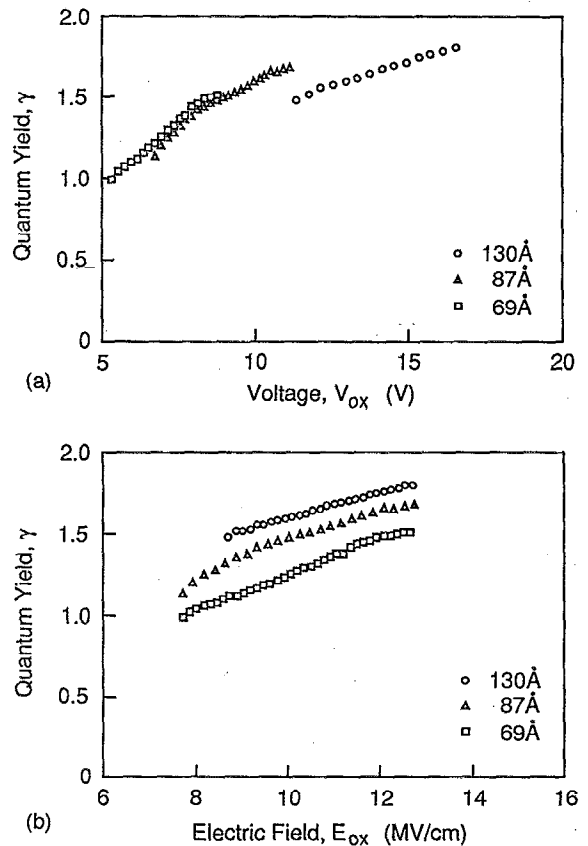


FIG. 6. Quantum yields γ of the hot electrons entering the silicon substrate in p -channel MOSFETs with the gate oxides of 69, 87, and 130 Å (a) as a function of the voltage across the oxide V_{ox} , and (b) as a function of the electric field in the oxide E_{ox} .

and the electric field in the oxide of the p -channel MOSFET are identical with those of the n -channel MOSFET.

C. Calculation of the substrate hole currents

In Fig. 8 the solid lines show the calculated results of the ratio $J_{p, sub}/J_{n, ch}$, which were obtained from Eq. (13) using the quantum yield γ from Fig. 6(b) and the average energy W_{avg} from Fig. 7. The experimental results of the ratio

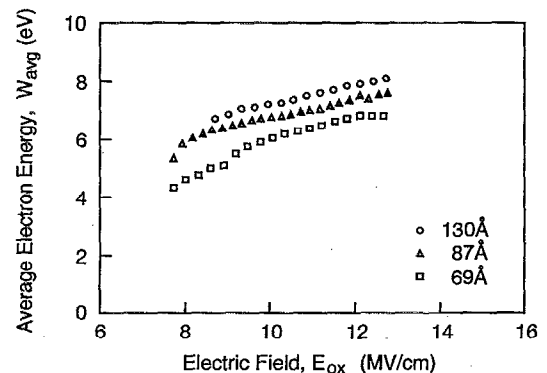


FIG. 7. The average energy W_{avg} of the hot electrons emitted into the silicon substrate with respect to the bottom of the Si conduction band as a function of the electric field in the oxide E_{ox} .

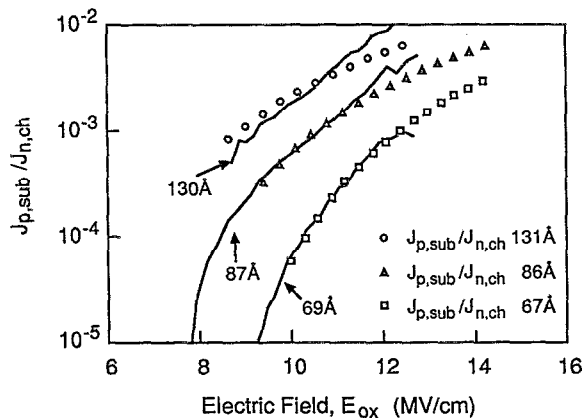


FIG. 8. $J_{p,\text{sub}}/J_{n,\text{ch}}$ ratios for three different oxide thicknesses as a function of the electric field in the oxide E_{ox} . Solid lines show the calculated results of the ratio $J_{p,\text{sub}}/J_{n,\text{ch}}$, which are obtained from Eq. (13) using the quantum yield γ from Fig. 6(b), and the average energy W_{avg} from Fig. 7. The experimental results of the ratio $J_{p,\text{sub}}/J_{n,\text{ch}}$ as a function of the electric field E_{ox} are plotted for the 67, 86, and 131 Å oxides.

$J_{p,\text{sub}}/J_{n,\text{ch}}$ as a function of the electric field E_{ox} are also plotted for the 67, 86, and 131 Å oxides in the n -channel MOSFETs. The calculated $J_{p,\text{sub}}/J_{n,\text{ch}}$ ratio, as well as the measured ratio, is increased as the oxide thickness is increased or the electric field E_{ox} is increased. The calculated results are in agreement with the measured $J_{p,\text{sub}}/J_{n,\text{ch}}$ ratio. The agreement between the experiment and the calculated result was obtained with the same set of parameters, where $A=0.0018$ s/m and $C=0.055$. We have successfully explained the dependence of the ratio $J_{p,\text{sub}}/J_{n,\text{ch}}$ on the oxide thickness and on the electric field. At the thicker oxide and the higher fields, the calculated values have a strong dependence on the electric field as compared with the experiment. This discrepancy may be due to the assumption of the Maxwell-Boltzmann distribution for the energy of hot holes, or due to the assumption used with regard to Eq. (6), that is, that the coefficient C , which depends on the average ratio of the energy of the secondary hole to the primary energy of the injected electron, is constant.

We have shown a simple model to explain the dependence of the substrate hole current on the electric field and oxide thickness. It has been reported that oxide instabilities occur due to hole injection into the oxide.^{1-3,11} It is generally accepted that oxide breakdown occurs when the substrate hole fluence reaches a constant value.⁹ Since the proposed model gives the substrate hole current as a function of electric field, we can predict the field dependence of the lifetime of gate oxides by dividing the value of the substrate hole fluence by the substrate hole current obtained from the model. This model is very useful to discuss the wearout of electrically stressed silicon dioxides.

IV. SUMMARY

A simple model has been proposed to explain the dependence of the substrate hole current in n -channel MOSFETs

on the electric field in the oxide and on the gate oxide thickness. We prepared n -channel MOSFETs with the gate oxides of 67, 86, and 131 Å and p -channel MOSFETs in which the oxide thicknesses used were almost equal to those in the n -channel MOSFETs. We used the carrier-separation technique in the p -channel MOSFETs and obtained the average energy of hot electrons entering the silicon substrate. The average energy of the hot electrons was related to the energy distribution of hot holes generated by the hot electrons emitted into the n^+ polysilicon gate during the Fowler-Nordheim electron tunneling in the n -channel MOSFETs. The substrate hole current is numerically modeled as thermionic emission of the hot holes overcoming the Si-SiO₂ energy barrier. For the oxides within the thickness range of 67–131 Å, we have satisfactorily explained the dependence of the substrate hole current on the electric field and on oxide thickness by using the average energy of the hot electrons and the thermionic hole emission model.

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