Study on Further Reducing the Epitaxial Silicon Temperature down to 250 °C in Low-Energy Bias Sputtering

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Study on further reducing the epitaxial silicon temperature down to 250 °C in low-energy bias sputtering

Tadahiro Ohmi, Keiichi Hashimoto, Makoto Morita, and Tadashi Shibata
Department of Electronics, Faculty of Engineering, Tohoku University, Aza-Aoba, Aramaki, Aobaku, Sendai 980, Japan

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The epitaxial silicon growth temperature has been reduced to as low as 250 °C by optimizing the ion bombardment condition in low-energy bias sputtering process. Independent and precise control of ion bombardment energy and ion flux density incident on a growing film surface is most essential to realize very low temperature epitaxy. It has been experimentally shown that the deficit in energy for epitaxial growth by reducing the substrate temperature is able to be compensated for by increasing the total energy dose on a film surface by low-energy ion bombardment. Increase in the impact energy of individual ions, however, results in the formation of high-density defects in the film. Therefore, the right direction to enhance the total energy deposition by ion bombardment is to increase the ion flux density while keeping the ion impact energy at an optimum value. As a result of such optimization, epitaxial growth of silicon has become possible at a temperature as low as 250 °C. The etch pit density in this low-temperature growth film is less than 3×10^3 cm^{-2}, the detection limit of our experiments. The carbon and oxygen concentrations in a grown film as measured by secondary ion mass spectroscopy increase with the background pressure, and these impurity concentrations are correlated to the crystallinity of the film. From these observations, the profound effect of contamination on the reduction of silicon epitaxial temperature is demonstrated.

I. INTRODUCTION

Lowering processing temperature for a total semiconductor device fabrication process is now becoming a critical issue in realizing ultralarge scale integration (ULSI) with deep submicron design rules. The reduction in the epitaxial silicon growth temperature, in particular, is quite essential not only for suppressing impurity redistribution and autodoping effects, but also to realize more advanced device structures. If epitaxial silicon can be grown at such a low temperature that the reactions between metal thin films and silicon do not occur, or at least, are well controlled, metal interconnects are able to be formed before the epitaxial silicon growth process. This will allow us to design total process integration with a great flexibility, thereby enabling us to fabricate more advanced device structures.

A considerable number of research works have been conducted on the study of low-temperature epitaxial silicon growth with *in situ* doping capability. In the case of chemical vapor deposition (CVD) process,[1–5] device grade epilayers have been obtained at 550 °C using an ultrahigh vacuum CVD technique.[2] Epitaxial silicon growth with a high deposition rate has been realized at 600 °C utilizing free-jet molecular flow CVD.[3] Molecular-beam epitaxy (MBE)[6–8] is one of the candidates for very low-temperature epitaxy. Although silicon epitaxy is certainly possible below 200 °C,[6] a high-temperature heat treatment under an ultrahigh vacuum is inevitable for substrate surface cleaning. The lowest surface cleaning temperature applied to MBE is around 800 °C.[7] In addition, difficulties are encountered in performing *in situ* impurity doping in MBE due to the different sticking coefficients of dopants and silicon atoms. Utilizing partially ionized MBE,[8] heavily arsenic-doped silicon epitaxial films have been grown successfully at 850 °C. However, the films grown at 750 °C exhibit high-energy (10-keV) ion-induced damages. Therefore, it is difficult to establish a real low-temperature process by MBE. On the other hand, very-low-temperature silicon epitaxial growth at temperatures below 300 °C has been reported using ion beam processes, such as partially ionized vapor deposition (PIVD),[9] ion beam epitaxy (IBE),[10] ion beam sputter deposition (IBSD),[11] and ionized cluster beam deposition (ICBD).[12] In these processes, kinetic energies provided to a growing film surface via ion bombardment is utilized as a substitute for the substrate heating. However, device-grade silicon epitaxial films have not been obtained so far with these processes. The range of ion energy used in these processes is much higher than typical interatomic binding energies in single-crystal silicon, resulting in the formation of damages in grown films.

On the other hand, use of much lower energies for bombarding a growing film surface has been proven to be very effective in growing defect-free epitaxial silicon layers at a temperature as low as 300 °C.[13–19] The cross-sectional transmission electron microscopy and defect etching (Wright etch) technique revealed that the film is defect-free single crystal.[17] By Hall measurement and SIMS (secondary ion mass spectroscopy) analysis of the impurity concentration, 100% incorporation of target dopants into a grown film as well as their full electrical activation at such a low deposition temperature were shown for a phosphorus-doped target of 1.9×10^{18} cm^{-3} impurity concentration.[16,18] *Pn* junction diodes fabricated by depositing *n*-epilayer directly on a *p*-type substrate showed fairly low leakage current of 1 nA/cm^2 at a reverse bias of 5 V, at which bias both a part of epilayer and

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the epilayer-substrate interface are included in the depletion layer.[16] Thus, the formation of high-quality *in situ* doped epitaxial silicon layers at 300 °C have been verified. The key feature of the process that we call "low-kinetic energy particle process" exists in the range of energy utilized for ion bombardment, which is in the range of a few eV's to a few ten eV's, comparable to or less than typical interatomic binding energies of atoms in a crystal. It was shown[17,18] that the ion energy of 25 eV is an optimum value for silicon epitaxy. Such low-energy ion bombardment is quite effective in activating the very surface layer of a film without introducing any damages in the film.

The purpose of the present work is to study how we can further reduce the epitaxial silicon growth temperature below 300 °C. The direction for optimizing ion bombardment conditions will be presented based on a series of experimental data. Discussion will be made in terms of two different means of energy transfer to a growing film. One is the substrate heating and the other is the low-energy Ar ion bombardment of a growing film surface. The detailed mechanism of energy transfer occurring at the film surface under low-energy ion bombardment is not fully understood at present. However, qualitative relationship between the energy provided through substrate heating and the film surface activation by low-energy ion bombardment will be discussed. And it will be shown that the deficit in the energy for epitaxy by reducing the substrate temperature is able to be compensated for by an increase in the total energy dose by ion bombardment. The point is how to increase the total energy dose in order to grow defect-free epilayers at a reduced temperature. In addition, we will also demonstrate the profound effect of impurities in the film growth ambient on the quality of an epilayer grown at a reduced temperature.

II. DIRECTION FOR LOW-TEMPERATURE EPITAXY

In order to grow films epitaxially on a substrate, sufficient amount of surface activation energy must be provided to a growing film surface. In the case of CVD technique, this energy is provided as a form of thermal energy by heating the entire wafer. Thus, high substrate temperature is generally required to obtain high-quality epitaxial silicon films.

So far the epitaxial silicon growth temperature by CVD has been decreased down to 550 °C.[2] In order to further reduce the epitaxial growth temperature, another energy source for surface activation is needed in addition to the substrate heating. We believe that low-energy ion bombardment of a growing film surface is the most promising way of providing such an energy. When an Ar ion having a kinetic energy in the range of a few tens of eV's hit a film surface, it would lose almost its entire energy within the top 2–3 atomic layers through inelastic nuclear collision. If the impact energy is lower than the interatomic binding energy of a crystal, interstitial atoms are not generated. Then such a collision would excite a number of spatially localized phonons in the very vicinity of the surface area where the ion hits. These excitations will immediately decay and the energy is lost as a heat flow through the substrate to the wafer holder which is held at a fixed temperature. Such a process is equivalent to a momentary temperature rise in a very localized area at the film surface. If the surface is subjected to continuous bombardment of low-energy Ar ions, a dynamical equilibrium will be reached and the very surface of a growing film is maintained at a certain "high temperature" state necessary for epitaxial growth to occur. This is what is meant by "surface activation." However, we cannot exclude the possibility of more direct interactions among incoming ions and surface adatoms, such as selective sputtering of silicon atoms at nonregular lattice sites as discussed in Ref. 20.

The most important parameters characterizing the low kinetic energy particle process are the kinetic energy of individual ions bombarding the growing film surface (ϵ_i) and the ion flux density incident on the film surface. The ion impact energy ϵ_i is determined by the difference between the plasma potential (V_p) and the externally applied substrate bias voltage (V_s), i.e., $\epsilon_i = V_p - V_s$. Here, V_p denotes the average dc component of the plasma potential. Since the excitation frequency of 100 MHz that we employed for the experiment is much higher than the ion frequency (typically 3 MHz), the ions cannot respond to the rf component of the sheath field and are accelerated only by the dc voltage component appearing across the sheath, which is primarily determined by the external dc source. Therefore, the precise control of ion energy with negligible small energy spread has become possible. We assumed the total energy given to a unit volume of the growing film is determined by the ion flux density relative to the film growth rate. Therefore, we have introduced a parameter, normalized ion flux (n_i), which is defined by the number of bombarding argon ions per single deposited silicon atom. The quantity is also known as the ion/atom ratio in the ion beam deposition process. n_i is calculated as the ratio of argon ion flux (F_i) to sputtered silicon atom flux (F_a), i.e., $n_i = F_i/F_a$, where F_i and F_a are derived from the measurement of the ion current and the film growth rate, respectively. Under our typical experimental setup (which is described in the experimental section), the ion current flowing into a 33-mm-diam wafer was $\sim$20 mA indifferent to target biases, resulting in the ion current density of $\sim$2.3 mA/cm^2. The film growth rate is determined by the target dc bias, which was $\sim$50 Å/min or 25 Å/min for $V_t = -200$ V or $V_t = -120$ V, respectively. The estimated values of n_i are given in Table I. Although the efficiency of energy transfer from incoming ions to surface adatoms is

TABLE I. Ion bombardment energy (ϵ_i) and normalized ion flux (n_i) under various ion bombardment conditions. (Plasma potential was 40 and 35 V for $V_t = -120$ and -200 V, respectively, at an rf power of 40 W.)

V_t(V)		V_s(V)			
		0	+5	+10	+15
−120	ϵ_i(eV)	40	35	30	25
	n_i			65–85	
−200	ϵ_i(eV)	35	30	25	20
	n_i			30–35	

not known, the energy given to an adatom as the result of the surface activation by ion bombardment would be proportional to the product of ϵ_i and n_i, and is able to be increased by increasing n_i and/or ϵ_i. Then, we can reduce the epitaxial growth temperature.

For realizing low-temperature epitaxy, by establishing precise control of all pertinent process parameters is most essential. Moreover, in order to eliminate disturbances arising from contaminants in the processing environment, the process must be performed under an ultraclean processing environment.[21]

III. EXPERIMENT

Silicon films were deposited using the rf-dc coupled mode bias sputtering system described in the previous papers.[18,20] A 100-MHz rf power supply is employed to generate a high-density plasma, and rf power input determines the plasma density. That is, the ion flux supplied to the wafer is controlled by the rf power. Two dc power supplies are connected to the target and to the wafer holder to control their dc potentials independent from the rf power input. The dc potential applied to the target (V_t) determines the sputtering rate, i.e., the film growth rate, while that applied to the wafer holder (V_s) determines the magnitude of ion energy for bombarding the film surface. In this way, the ion flux, ion energy, and film growth rate, which are the important parameters pertinent to the low kinetic energy particle process, are controlled independently and precisely by adjusting such externally controllable variables as the rf power input, substrate bias voltage, and target bias voltage.

The film growth was performed in an ultrahigh vacuum chamber whose ultimate pressure was 2×10^{-10} Torr, and ultraclean argon gas having moisture level of 2~3 ppb or less and the level of other impurities below 0.1 ppb was used.[22] However, when films were grown, the throttle valve separating the main chamber and the cryogenic pump was partially closed to control the working pressure to about 8 mTorr. The background pressure after the adjustment of the throttle valve opening was typically $0.7\text{–}1.2\times10^{-8}$ Torr, which determines the actual contamination level of the process.

The substrates used for epitaxial growth were either *p*-type (100) silicon wafers or *p*-type 4 °-off (111) silicon wafers. A heavily arsenic-doped silicon block was used as a target. The silicon epitaxial growth was performed under various ion bombardment conditions at substrate temperatures ranging from 200 to 325 °C. The wafer heating and temperature measurement techniques are described in the Appendix of Ref. 18. The ion bombardment conditions were changed by adjusting the external parameters, and the relationship between the external parameters (V_t and V_s) and the ion bombardment parameters (ϵ_i and n_i) is summarized in Table I. The estimation of plasma potential was carried out using the technique also described in the Appendix of Ref. 18. The rf power input and argon pressure were fixed at 40 W and 8 mTorr, respectively.

The conventional wet chemical processes were utilized for wafer cleaning: 5 min boiling in H_2SO_4/H_2O_2, ultrapure water rinsing, and HF/H_2O (1:50) etching for removing native oxides followed by ultrapure water rinsing and isopropanol (IPA) vapor drying. After drying, a silicon wafer was immediately loaded into the load-lock chamber, and then transferred into the process chamber. Prior to the film deposition, the *in situ* surface cleaning under the optimized condition described in Ref. 13 was carried out to remove physically adsorbed molecules onto the wafer surface during the air exposure in the clean room.

The crystallinity of a grown film was evaluated by reflection electron diffraction (RED) analysis as well as by defect etching technique (Wright etch) followed by scanning electron microscopy (SEM) observation. The resistivity of the *in situ* doped epitaxial silicon film was measured by a four-point probe method. The contaminant species in the film were investigated by secondary ion mass spectroscopy (SIMS).

IV. RESULTS

A. Necessity for high-precision control of ion bombardment energy

Figure 1 demonstrates the RED (reflection electron diffraction) patterns obtained from silicon films deposited on (100) silicon wafers at 300 °C. The thickness of a grown film was about 2000 Å and the total deposition time was about 80 min, giving the deposition rate of ~25 Å/min. The target bias voltage (V_t) was fixed at -120 V, while the substrate bias voltage (V_s) was changed with an increment of 2 V. That is, only one of the two important parameters, ϵ_i, was varied while keeping the ion flux density constant at n_i = 65–85 (see Table I). The ion bombardment energy is approximately 25 eV at $V_s = +15$ V with a target bias voltage (V_t) of -120 V as shown in Table I. (It was approximately 25 eV at $V_s = +5$ V when $V_t = -200$ V as in the case of Fig. 3 in Ref. 18.) The crystal structure of the film changes from amorphous ($V_s = -2\sim0$ V) to defective single crystal ($V_s = +4\sim+8$ V) and to single crystal with a higher crystallinity ($V_s > +10$ V). An epitaxial silicon film with the best crystallinity is obtained at $V_s = +14$ V as indicated

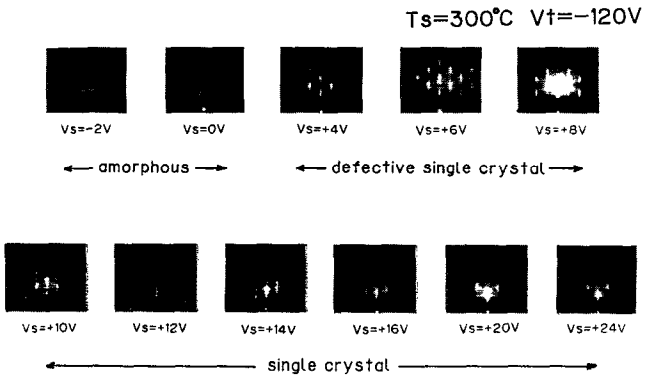


FIG. 1. Series of RED patterns obtained from epitaxial silicon films grown at 300 °C by changing the substrate bias voltage by a step of 2 V, thus changing the ion bombardment energy by 2 eV.

by the sharp Kikuchi lines. In the remainder of this paper, experimental data will be discussed in terms of a more physically meaningful parameter ϵ_i (ion bombardment energy).

In Fig. 2, the etch pit density is plotted as a function of ion impact energy ϵ_i. The etch pit density increases as the energy is either increased or decreased from the optimum condition of $\epsilon_i = 24$–26 eV. For samples grown at $\epsilon_i = 24$–26 eV, no etch pits were found in a total area of 3.2 μm $\times$ 1 cm observed by SEM. When ϵ_i is larger than 30 eV (V_s values less than 10 V), only rough surface was observed after Wright etch and the etch pit density measurement was not possible.

The resistivity of a deposited film is shown as a function of ϵ_i in Fig. 3. Since the resistivity is a very sensitive measure of the film crystallinity,[16] it is known that the best quality of a film is obtained at around $\epsilon_i = \sim 25$ eV, where the resistivity of the grown film becomes minimum of 3.2×10^{-3} Ω cm. Substantial increase in the resistivity occurs when ϵ_i is changed from the optimum condition. This observation is quite similar to that shown in Fig. 2. These results strongly suggest that the argon ion bombardment needs to be performed with a precisely controlled energy and with a negligible small spread of energy distribution, and how the ion bombardment energy is important to determine the crystallinity of a film.

The resistivity of the silicon film deposited at three different ion bombardment energies is shown in Fig. 4 as a function of the substrate temperature (T_s). The target bias for these samples was -200 V. The film thickness was ~ 2000 Å which was grown with a total deposition time of 40 min. The growth rate was then ~ 50 Å/min and the normalized ion flux density was $n_i = 30$–35 (see Table I). The film resistivity increases drastically at a certain critical temperature (T_c), indicating that a drastic degradation in the film crystallinity occurs below the temperature. Above this critical temperature ($T_s > T_c$), the resistivity does not change substantially. This result suggests that the lowest temperature for epitaxial growth does exist for each ion bombardment energy. This critical temperature strongly depends on the ion bombardment condition. It is interesting to note that the critical temperature (T_c) decreases with increasing ion bombardment energy. The T_c's for $\epsilon_i = 25$, 30, and 35 eV are 260, 240, and < 200 °C, respectively. This means that the increase in the ion bombardment energy would reduce the epitaxial silicon temperature. However, the resistivity above the T_c increases with an increase in ϵ_i, indicating that crystalline defects are generated in the film by excess ion bombardment energy.

Figure 5 shows SEM micrographs of as deposited silicon film surfaces (top) and Wright-etched surfaces (bottom). The ion bombardment condition was the same for all samples, i.e., $\epsilon_i = 30$ eV and $n_i = 30$–35, but the substrate temperature was changed from 300 °C down to 230 °C. With decreasing substrate temperature, the density of small mounds seen on as-deposited film surface increases, thus indicating the degradation of morphological quality. The degradation of crystalline quality is also evident from the increase in the etch-pit density with decreasing T_s as shown in the figure. These observations strongly suggest that the sur-

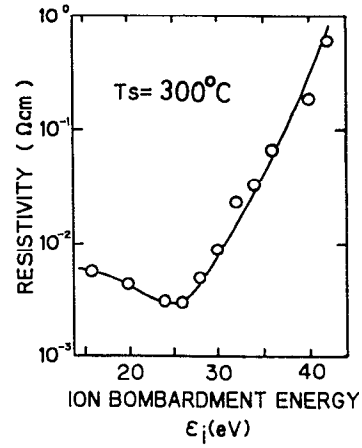


FIG. 3. The resistivity of a deposited silicon film as a function of the ion bombardment energy.

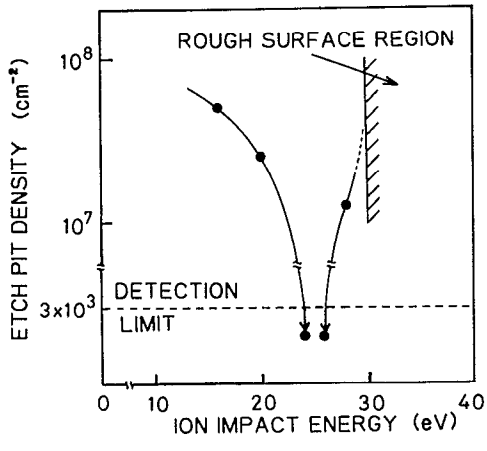


FIG. 2. The etch-pit density in a silicon film grown at 300 °C as a function of the ion bombardment energy.

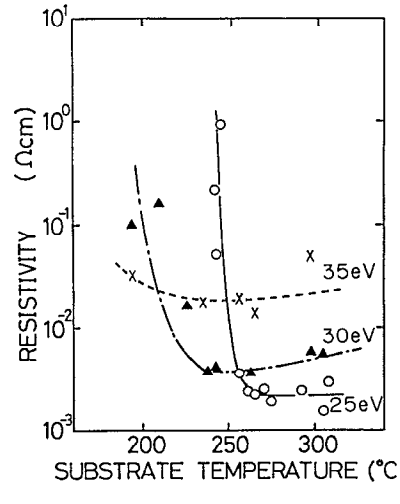


FIG. 4. Deposited silicon film resistivity as a function of the substrate temperature for three different ion bombardment energies.

face adatoms fail to find their normal lattice sites by the deficit in the thermal energy provided through substrate heating, resulting in the formation of crystalline defects in the grown film.

B. Optimizing ion bombardment conditions for low-temperature epitaxy

Figure 6 demonstrates the effect of reducing substrate temperature on the crystallinity of a grown film for three different ion bombardment conditions. In the top row, the results for silicon films deposited at $\epsilon_i = \sim 25$ eV and $n_i = 30$–35 are shown. A single-crystal epitaxial silicon film was obtained at 300 °C as indicated by the Kikuchi lines seen in the pattern. When the substrate temperature is reduced, the degradation in the film crystallinity is evident from the figure. At $T_s = 270$ ° C, the Kikuchi lines in the pattern becomes a little vague. As the substrate temperature is further reduced down to 250 °C, the RED pattern changes into a diffused ring pattern, indicating the formation of a highly disordered film. The surface of the Wright etched sample is shown in Fig. 7(b), showing the formation of high density defects. Deposition at $T_s = 200$ °C leads to the formation of an amorphous silicon film.

When the ion bombardment energy was increased by 10 eV ($\epsilon_i = 35$ eV) and the ion flux density was left unchanged ($n_i = 30$–35) as shown in the middle row, the crystallinity of the film deposited at 250 °C was much improved as is evident from the streak pattern. In addition, the epitaxial silicon growth was observed even at 200 °C. However, the crystallinity of the film deposited at 300 °C is definitely inferior to that of the film grown at 300 °C with $\epsilon_i = \sim 25$ eV and $n_i = 30$–35. The degradation in the film crystallinity observed at 300 °C would have resulted from the damage generation by ion bombardment with an energy in excess of the optimum value of 25 eV. The increase in resistivity above the critical temperature observed in Fig. 4 is related to this damage generation.

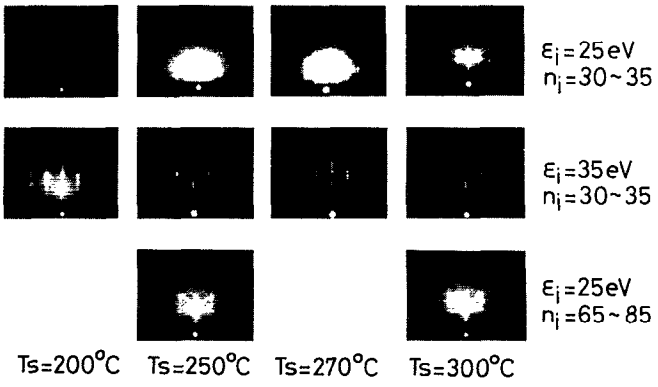


FIG. 6. Effect of the substrate temperature and the ion bombardment condition on the crystallinity of a grown film as evaluated by reflection electron diffraction (RED) analysis.

On the other hand, the RED patterns obtained from silicon films grown with the increased ion flux density $n_i = 65$–85) while keeping the individual ion bombardment energy at an optimum value of 25 eV are given at the bottom row of the figure. A single-crystal epitaxial silicon film was obtained at 250 °C. The resistivity of the film was almost the same as that of the best quality silicon film formed at 300 °C, i.e., 3.7×10^{-3} Ω cm, and no etch pits were observed on the Wright-etched sample surface as shown in Fig. 7(a). The etch-pit density of the film is less than 3×10^3 cm^{-2}, which is the detection limit of the present experiment.

C. Effect of environmental cleanliness

The effect of cleanliness in the processing environment on the crystallinity of deposited films is shown in Fig. 8. The film resistivity and etch-pit density are shown in Figs. 8(a) and 8(b), respectively, for three different base pressures of the chamber before the film deposition. The ion bombard-

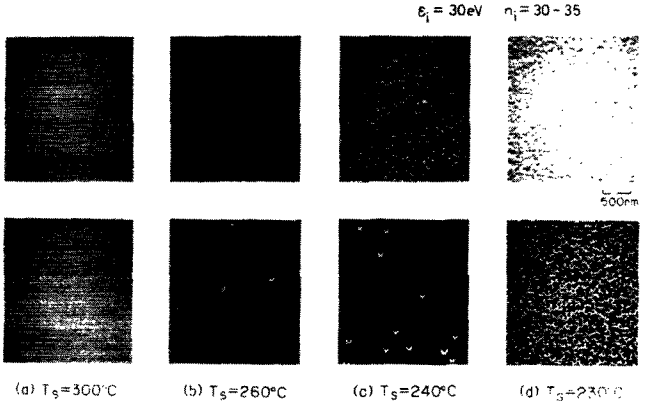


FIG. 5. SEM observation of as-deposited silicon film surfaces (top) and Wright-etched surfaces (bottom) for varying substrate temperatures.

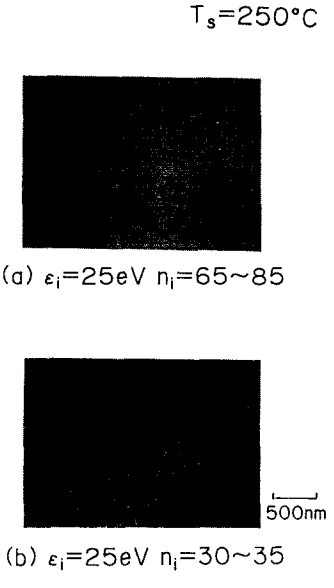
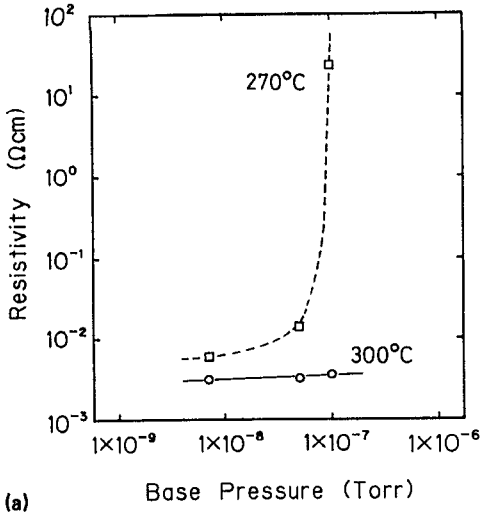


FIG. 7. SEM observation of Wright-etched surfaces of silicon films formed at 250 °C under two different ion bombardment conditions: (a) $\epsilon_i = 25$ eV, $n_i = 30$–35; (b) $\epsilon_i = 25$ eV, $n_i = 65$–85.



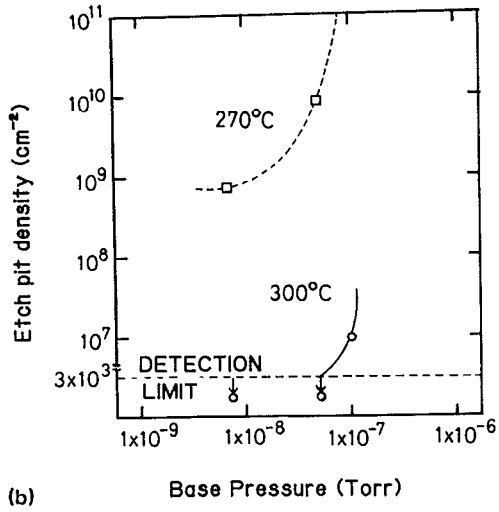


FIG. 8. The effect of the environmental cleanliness on the crystallinity of a deposited film. (a) The film resistivity and (b) the etch-pit density are shown as a function of the base pressure before film deposition.

ment condition was $\epsilon_i = 25$ eV and $n_i = 30$–35, viz., the condition optimized for epitaxy at 300 °C substrate temperature. Therefore, the crystallinity degrades when substrate temperature is reduced as indicated in Figs. 4 and 6. In order to enhance the effect of contamination on the film growth process, the substrate temperature was reduced to 270 °C. The results for 300 °C substrate temperature are also shown in the figure. The ion bombardment condition during the film growth was the same for all samples. It is clearly seen from the figure that both the resistivity and etch-pit density increase drastically with increase in the background pressure at 270 °C. However, such crystallinity degradation is negligible at 300 °C. This result suggests that the environmental cleanliness has a profound effect on the film crystallinity especially when the substrate temperature is reduced. It is concluded that the establishment of an ultraclean processing environment[21] is critically important for very low-temperature epitaxy.

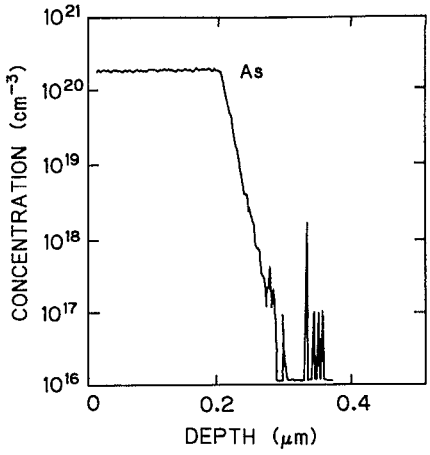


FIG. 9. The dopant impurity (As) profile in a grown film as measured by SIMS.

The typical dopant impurity (As) profile measured by SIMS is shown in Fig. 9 for a single-crystal silicon film grown at 300 °C. The dopant profile is well defined since the film growth temperature is as low as 300 °C. It is seen from the figure that dopant impurities distribute uniformly within the epitaxial layer at a concentration of 1.7×10^{20} cm^{-3}. The resistivity of bulk silicon having this impurity concentration (1.7×10^{20} cm^{-3}) is about 4.5×10^{-4} Ω cm. However, the lowest film resistivity obtained so far is 3×10^{-3} Ω cm. It is not verified at present whether the impurities are not fully activated and/or the drift mobility is reduced due to contaminant species in the epitaxial layer. We suspect the latter is the main reason for this increased resistivity. When a phosphorus-doped floating zone (FZ) silicon wafer of 0.0136 Ω cm resistivity was used as a target, 100% electrical activation of dopant impurities was achieved as shown in Ref. 18, where Hall mobility was lower than that of a bulk silicon having the same impurity concentration, approximately 70% of the bulk value.

Figure 10 demonstrates the oxygen, carbon, and argon profiles obtained from the epitaxial silicon layer grown at 300 °C by SIMS measurement. A very high concentration of argon is observed in the film. With such a high Ar content in

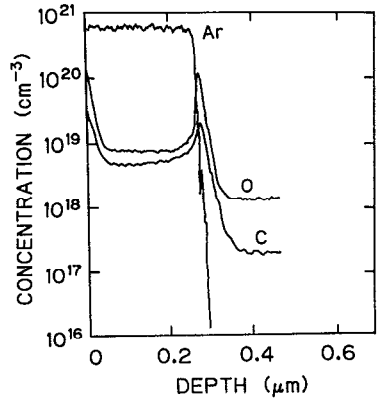


FIG. 10. SIMS argon, oxygen, and carbon profiles obtained from an epitaxially grown silicon layer.

the film, the film was stable for heat treatments in nitrogen up to 900 °C, showing no changes in crystallinity evaluated by RED and etching technique. However, when annealing was carried out at 1000 °C (for 30 min), etch pits were observed (9.5×10^{7} cm^{-2}) without any appreciable changes in the RED pattern. The carbon and oxygen concentrations are much higher than those in the substrate. This is due to the low deposition rate of less than 1 Å/s under an insufficient background pressure of about 10^{-8} Torr. If all residual gas molecules, mainly H_2O, arriving at the film surface are incorporated, impurity concentration would be about 5×10^{20} cm^{-3}. The impurity concentrations in Fig. 10 are much lower than the calculated value. The ion bombardment on the film surface would have an effect of reducing the impurity incorporation into the film. The pileup of impurities (oxygen and carbon) at the epilayer/substrate interface is also seen. This can explain the darker contrast region observed at the interface in the cross-sectional TEM (transmission electron microscope) micrograph shown in Fig. 3 of Ref. 17. The dependence of the carbon and oxygen concentration in the film on the base pressure before film deposition is shown in Fig. 11. The samples of the figure were the same as those in Fig. 8. It is clear that their concentrations are reduced with the decrease in the base pressure. And the reduction in the contamination level definitely improves the film crystallinity as indicated in Fig. 8(a) and 8(b).

Besides the importance of ultraclean processing environment for the film growth, preparation of ultraclean wafer surface before film deposition is also essential in the low-temperature epitaxy. In the low kinetic energy particle process, extremely low-energy (<2–3 eV) argon ion bombardment is employed to perform damage-free *in situ* substrate surface cleaning.[13] Figure 12 demonstrates the effect of the surface cleaning. The resistivity of the silicon film deposited with or without *in situ* surface cleaning is shown as a function of the air-exposure time. The wafers were wet-chemically cleaned with a diluted HF etch and ultrapure water rinsing at the final step, and then exposed to clean air for a certain period of time before setting into the sputtering chamber. Then the silicon growth was carried out using the optimum condition for epitaxy at 300 °C ($\epsilon_i = 25$ eV, $n_i = 30$–35). Degradation in crystallinity for air-exposure time larger than 1 h is evident even with *in situ* cleaning. This has resulted from moisture molecule adsorption and succeeding native oxide growth.[23] The fact indicates that the low-energy ion-bombardment surface cleaning desorbs surface adsorbed molecules but cannot remove native oxide. The SIMS data in Fig. 10 indicate that carbon and oxygen pile up at the interface. This also proves that the *in situ* surface cleaning is not yet perfect. Once the wafer surface is exposed to the air, native oxide layer is formed. *In situ* removal of native oxide should be conducted using the HF gas selective etching process,[24] and the removal of carbon should be performed by low-energy hydrogen ion (H^+) bombardment.

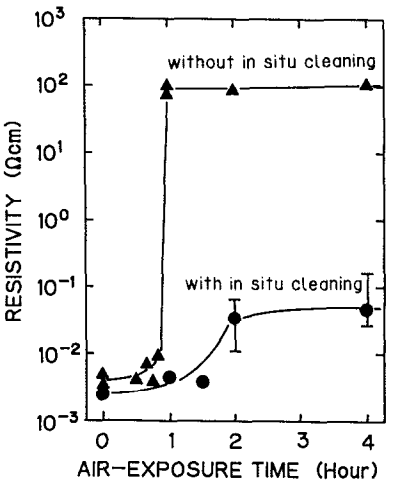


FIG. 12. The effect of the *in situ* surface cleaning by extremely low-energy Ar ion bombardment on the deposited Si film. Film resistivity is shown as a function of air-exposure time before setting into the sputtering chamber.

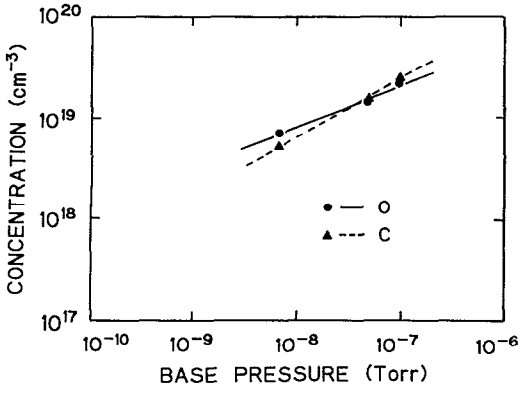


FIG. 11. The oxygen and carbon concentrations as a function of the base pressure before film deposition.

Moreover, it should be commented that a few metallic contaminant species were also detected in the film. These metals were iron, chromium, and nickel, coming from several metal component parts in the chamber such as the target clump and the shutter. The advanced plasma equipment in which such chamber material contamination will not occur is under development.[25] The mobility degradation in the film as discussed in reference to Fig. 9 can be explained by such contamination in the film.

V. DISCUSSION

In order to realize epitaxial growth, sufficient amount of surface activation energy must be provided so that surface adatoms can migrate at the surface and locate themselves at normal lattice sites. Supply of such energy can be performed either by substrate heating or by argon ion bombardment as we discussed in Sec. II. Let E_{tot} denote the total energy that a single deposited Si atom gains at the surface of a growing film. E_{tot} consists of two components, i.e., E_t, the thermal energy provided through substrate heating, and E_{ion}, the energy originated from surface activation by Ar ion bombardment. It is assumed that in order for silicon epitaxy to occur,

the total energy E_{tot} must be larger than a certain threshold value, E_{epi}, viz.,

$$E_{tot} = E_t + E_{ion} > E_{epi}. \quad (1)$$

Here E_t will be on the order of kT. The energy transfer process among the bombarding Ar ions and the Si adatoms involves a number of complex physical processes occurring at the surface, such as the collision of an incoming Ar ion with a Si atom in the top layers of the film and the resultant localized phonon excitation followed by the decay of the excitation and the interaction between the phonon and the adatom, and so forth. The detailed description of the process is beyond the scope of this paper. However, E_{ion} can be reasonably approximated as

$$E_{ion} \propto n_i \epsilon_i, \quad (2)$$

where ϵ_i is the bombardment energy of an individual ion and n_i the normalized ion flux. Complete disappearance of Bragg spots in the diffraction pattern at 250 °C (top row) in Fig. 6 can be interpreted as the inequality (1) did not hold due to the deficit in the thermal energy E_t as the result of 50 °C reduction in the substrate temperature. In order to compensate for the deficit in the thermal energy, ion energy E_{ion} must be increased. Since E_{ion} is proportional to $n_i \epsilon_i$, this can be achieved either by increasing n_i or ϵ_i. The results obtained by increasing ϵ_i is given in the middle row of Fig. 6.

Here the ϵ_i was increased by 10 eV as compared to the sample in the top row. Interesting to see is that streak patterns are obtained at 250 °C and that Bragg spots are also seen even at 200 °C. The deficit in the thermal energy has been compensated for by an increase in E_{ion} and epitaxial growth has occurred. However, it is important to note that no Kikuchi lines are observed even at 300 °C where the inequality (1) definitely holds. The crystallinity degradation is due to the excess ion bombardment energy that has produced damages in the film. Therefore it is concluded that the right way to increase the E_{tot} for silicon epitaxy at reduced temperature is to increase E_{ion} by increasing the normalized ion flux n_i while keeping the individual ion bombardment energy ϵ_i at the optimum value of 25 eV. This conclusion has been verified by the results shown in the bottom row of Fig. 6 where silicon films were grown with the condition of $\epsilon_i = 25$ eV and $n_i = 65$–85. Thus it has been experimentally demonstrated that the deficit in the thermal energy due to reduction in substrate temperature is able to be compensated for by the increase in ion bombardment energy. Decrease in substrate temperature by 50 °C corresponds to an average energy reduction of 0.0043 eV. In order to compensate for this reduction, however, it is requested to increase the total energy input by Ar ion bombardment for a single deposited silicon atom by about 25 eV × (75–35) = 1000 eV. Such a large difference between the thermal energy and the equivalent input ion energy indicates the inefficient transfer of Ar ion kinetic energy to the epitaxial growth process. The energy deposited on the film surface by the impact of a single Ar ion is immediately lost from the surface by heat conduction (diffusion) to substrate and very little contributes to the increase in the effective surface temperature which was discussed in Sec. II. We are basically assuming the energy transfer between the Ar ions and the surface adatoms as being carried out via activated film surface. This would not be a very efficient way of energy transfer. So far we have changed the value of n_i only by changing the film growth rate and have not conducted experiments in which the growth rate is changed under the identical normalized ion flux condition. Such experiments under a variety of parameter combinations must be carried out to further investigate the kinetics of the process.

We have found that the optimum ion bombardment energy was about 25 eV for epitaxy on the (100) silicon substrate. The value nearly agrees with that presented in Ref. 19. The authors demonstrated that the best epitaxial films were obtained when the substrate was bombarded with 23-eV mercury (Hg) ions during deposition. Moreover, they succeeded in forming epitaxial silicon films at temperatures not exceeding 300 °C by substituting low-energy and high-current-density ion bombardment for growth at an elevated temperature. In their work, the Hg triode discharge system was employed instead of our rf–dc coupled mode system. In either case, the success in realizing very low-temperature silicon epitaxy is attributed to the adequate choice of low-energy and high-flux-density ion bombardment.

Experimental results and their interpretation in terms of E_t and E_i presented so far indicate the interchangeability between E_t and E_i. Such interchangeability is very useful to understand the experimental results. The silicon epitaxy on the 4 °-off (111) silicon wafer was investigated in a similar way. The resistivity of the silicon film deposited on the (100) and the 4 °-off (111) silicon wafer is shown in Fig. 13 as a function of the ion bombardment energy at two different substrate temperatures. For most of the samples, the ion flux density (n_i) was 30–35, except for the 4 °-off (111) silicon wafer at 325 °C, where n_i was increased to 65–85. When the silicon film is epitaxially grown on (100) silicon substrates,

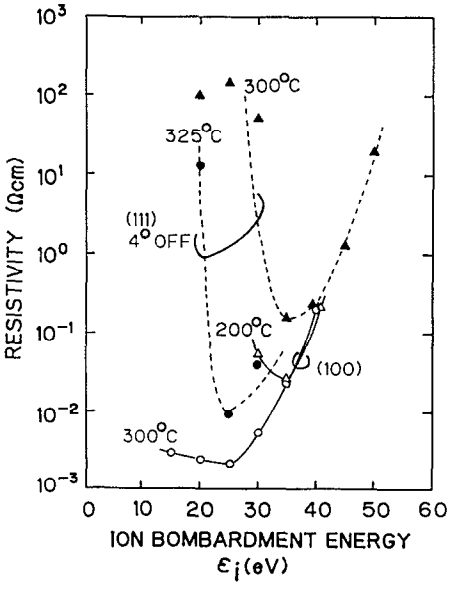


FIG. 13. The resistivity of the silicon film deposited on the (100) and 4 °-off (111) silicon wafer as a function of ion energy at two different substrate temperatures for each type of substrate.

ion bombardment energy which yields the minimum resistivity at a given substrate temperature shifts to higher values with decreasing T_s. The similar shift is observed when the 4 °-off (111) silicon wafer was used as a substrate. These shifts are due to the compensation for the deficit in thermal energy by increasing ion bombardment energy, as discussed so far. Although the substrate temperature as well as the ion flux density, used for epitaxy on the 4 °-off (111) substrate, are higher than those for epitaxy on the (100) substrate, the epitaxial silicon film on the 4 °-off (111) substrate does not show the resistivity as low as that of the epitaxial film on the (100) substrate. This means that the higher total energy is needed for silicon epitaxy on the 4 °-off (111) substrate than for that on the (100) substrate. That means the E_{epi} in the inequality is larger for a 4 °-off (111) surface than on a (100) surface. The (111) silicon surface is the closest packed surface and is the most stable one of all the crystal lattice planes. This means that the density of the kink or step where surface adatoms are incorporated into the lattice of silicon crystal is smaller than that on a (100) surface. This situation is improved by employing 4 °-off cutting of a (111) silicon surface, but the kink or step density is still smaller than that of the (100) silicon surface. Therefore, surface adatoms on a 4 °-off (111) surface must migrate longer distances than those on (100) surface. This is the reason why higher total energy is requested for epitaxy on the 4 °-off (111) substrate than for that on the (100) substrate.

The RED pattern from the best quality silicon film deposited on the 4 °-off (111) wafer is shown in Fig. 14. High-quality films exhibiting sharp Kikuchi lines have not been obtained so far. This would be due to the deficit in the total energy given by substrate heating and/or ion bombardment. However, this would be alternatively interpreted as the optimum ion bombardment energy for epitaxy on a (111) silicon surface is smaller than that on a (100) silicon surface. The RED patterns shown in the middle row of Fig. 6 all indicated streak patterns where excess ion bombardment energy is employed for film growth. Deficit in the total energy by reducing T_s below the critical temperature, the RED pattern changes into a halo pattern rather than to exhibit streaks as shown in the top row in the figure. From these observations, it is inferred that the optimum ion bombardment energy for (111) silicon homoepitaxy can be smaller than that for (100) silicon homoepitaxy.

The success in lowering the epitaxial silicon growth temperature by MBE and CVD techniques is mainly attributed to the cleanliness of the processing environment. The importance of environmental cleanliness for low-temperature epitaxy has also been demonstrated for low-energy bias sputtering process in reference to Figs. 8 and 11. The environmental cleanliness of the process is expressed as the ratio of the background pressure to the working pressure (which was typically 10^{-3} Torr in the present work). In order to make it as clean as the gas purity of ppb (10^{-9}), the background pressure must be decreased as low as 10^{-12} Torr. However, in this work, the throttle valve was partially closed to obtain a fixed working pressure at a limited gas flow rate, resulting in the background pressure degradation up to 10^{-8} Torr, much higher than the ultimate pressure in this vacuum

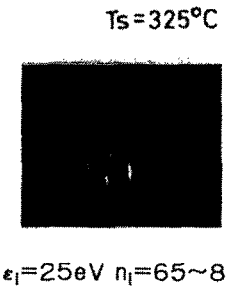


FIG. 14. Typical RED pattern obtained from the best quality silicon film obtained so far on the 4 °-off (111) silicon wafer. Deposition condition was $\epsilon_i = 25$ eV, $n_i = 65$–85, and 325 °C substrate temperature.

system (2×10^{-10} Torr). It is clear from Figs. 8 and 11 that the impurity concentration in the grown film is decreased by lowering the background pressure before film deposition. The background pressure is determined by the balance between the pumping speed of the vacuum pump and the outgas rate from the chamber inner surface. Therefore, a high pumping speed must be maintained during the process under gas flow. The throttle valve should be full open to control the working pressure. As long as cryogenic pumps are used, as in our case, the throttle valve must be controlled because employing a large amount of gas flow rate to establish mTorr—several 10 mTorr working pressures saturate the capacity of the pump in a short time and sometimes cause a temperature rise of cryopanels, resulting in reduced pumping speed. Turbomolecular pumps with large throughput and UHV (ultrahigh vacuum) capability must be used for ultraclean plasma processes.[26] At the same time the outgassing from the chamber inner surface must be minimized.[26] Furthermore, the impurity incorporation into the film is also decreased by the enhancement of the film growth rate. Therefore much larger deposition rate must be employed.

In our deposition system, the *in situ* surface cleaning was performed at the same temperature for film growth under extremely low-energy ion bombardment. Therefore, the entire process including the surface cleaning process has been conducted at 250 °C. Surface cleaning techniques utilizing argon ion bombardment have been explored in other works.[27–29] According to these works, the argon ion sputter cleaning is able to be characterized by the ion bombardment energy. When high ion energies ($\sim$1 keV) were used for native oxide removal,[27] bombardment at a high temperature of 800 °C resulted in permanent damage in the subsurface region of the substrate. On the other hand, the surface cleaning was successfully performed by sputtering at room temperature followed by 800 °C annealing to regrow the resultant amorphized silicon region. If low ion energies of a few hundred electron volts is utilized,[28,29] bombardment at elevated temperatures is quite effective in removing native oxide due to the enhanced sputtering yield of oxide. Using the substrate temperature of 750 °C, native oxide is removed without the production of net damage in the substrate. In these processes, however, process temperature must be raised above 600 °C, and the establishment of real low-temperature process is not possible. In the present work, extremely low energy (2–3 eV) Ar ion bombardment has been utilized for preparation of a clean surface at low temperatures. Using this cleaning technique, a damage-free surface

has been obtained at a low temperature, resulting in the low-temperature silicon epitaxy. However, the cleaning process is only effective to remove physically adsorbed molecules on a surface as is evident from Figs. 10 and 12, and the cleanliness of the surface is not perfect. In order to circumvent the difficulty, we are proposing and developing a closed manufacturing system in which wafers are processed completely isolated from air. The process has been proven to be very effective as a native oxide-free process.[26,30]

Judging from above discussions, it is expected that epitaxial silicon growth at room temperature is, in principle, possible if a sufficient amount of energy is provided by increasing ion flux density. However, this will not be realized until the perfect clean processing environment and substrate surface are both established.

VI. CONCLUSIONS

The direction for reducing epitaxial silicon growth temperature has been investigated by depositing silicon films on (100) and 4 °-off (111) silicon wafers at various substrate temperatures and ion bombardment conditions. The most important parameters for low-energy bias sputtering has been shown to be the ion bombardment energy and ion flux density, and the precise and independent control of these two parameters has been achieved by the rf-dc coupled mode bias sputtering system. The precise control of ion bombardment energy has been proven to be the first step to obtain the high-quality epitaxial silicon film. The crystallinity of the deposited film changes by changing ion energy only by 2 eV. The best-quality epitaxial silicon film is grown under ion energy of about 25 eV at 300 °C. On the other hand, the deficit in the thermal energy by reducing the substrate temperature is compensated for by increasing the energy provided by ion bombardment for surface activation. Increasing ion energy by 10 eV from the optimum energy of 25 eV, silicon epitaxy observed even at 200 °C. However, the ion bombardment with an excess energy causes damages in the grown film, thus the right direction to reduce the epitaxial temperature has been shown to increase the ion flux density while keeping the individual ion bombardment energy at an optimum value for epitaxy. The epitaxial silicon film thus obtained at 250 °C has the same crystalline quality as that of the best-quality film obtained at 300 °C. The decrease of 50 °C in the substrate in the substrate temperature has been compensated for by the increment of 35–50 in the normalized ion flux. The surface activation by increasing the ion flux density and the resultant enhancement of surface adatom migration is effective for reducing the epitaxial growth temperature. In addition, it is found that the larger surface activation energy is needed for the epitaxy on the 4 °-off (111) silicon wafer than for that on (100) silicon wafer. It is also shown that ultraclean processing environment and ultraclean surface are essential for very low-temperature epitaxy.

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