Reduction of Fixed-Pattern Noise of BASIS Due to Low Kinetic Energy Reactive Ion and Native-Oxide-Free Processing

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Abstract—**Reduction of fixed-pattern noise in Base-Stored Image Sensor (BASIS) is achieved with the newly developed processes based on the ultra-clean technology. One is low kinetic energy reactive ion etching to keep Si/ SiO_2 interface away from the plasma damage. The dark current decreases down to 0.4 nA/cm^2. The other of these processes is native-oxide-free processing to suppress the growth of native oxide on Si surface. The uniformity of current gain in a bipolar transistor has been improved with the introduction of these processing methods. Further, these methods have been confirmed to improve the Al to n^+ region contact exhibiting low and uniform contact resistance without any thermal annealing treatment.**

I. Introduction

IMAGE sensors for high-definition television systems [1], [2] require not only as many as 2 million picture sensing elements, but also wide dynamic range and high sensitivity. One such devices is an image sensor with amplification function in each picture cell [3]–[8].

The operational principle of this image sensor is that the signal charges generated by incident light in a photodiode are stored in a control electrode of a photo-transistor in order to amplify the signal charge. A bipolar imaging device using a capacitor-loaded emitter-follower circuit, which is called Base-Stored Image Sensor (BASIS), has been demonstrated experimentally to exhibit wide dynamic range of 70.6 dB in a linear image sensor [6].

In order to obtain such a wide dynamic range using the image sensor with an amplification function in each picture cell, it is essential that fixed pattern noise (FPN) should be negligibly small in the practical devices. FPN is mainly caused by the nonuniformities of dark current and current gain of the photo-transistor in each picture cell. Characteristics of dark current and current gain in a bipolar transistor were investigated, using monitor devices.

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This paper describes the improvement of uniformity achieved with a newly developed processes based on ultra clean technology [9]–[15]. One of these processes is low kinetic energy reactive ion etching to keep Si/SiO_2 interface away from plasma damage. The dark current at 45°C decreases down to 0.4 nA/cm^2 in comparison with the conventional one of 2.0 nA/cm^2 without any anneal treatment after etching. The other of these processes is native-oxide-free processing to suppress the growth of native oxide on the emitter n^+-Si surface. The uniformity of the current gain in a photo-transistor has been improved with the introduction of native-oxide-free processing, which consists of the following processes: N_2-gas-sealed wet cleaning using pure water with low dissolved oxygen (20 ppb), wafer drying, wafer transporting and loading to a processing chamber in N_2 gas ambient, and metal deposition by sputtering with low energy ion bombardment [11].

Further, Al to n^+ region contact has been confirmed to have low and uniform contact resistance without any anneal treatment using native-oxide-free processing.

The reduction of the dark current using low kinetic energy dry etching is described in Section II. The improvement of the uniformity of current gain and contact resistance is presented in Section III.

II. Low Kinetic Energy Dry Etching for Reduction of Dark Current

In this section, the authors describe reduction procedures of dark currents in BASIS, relating to dry etching time dependence of dark current, the recovery of dry etching damages by anneal treatment, and the relationship between damages and bombarding ion energy during dry etching. It is confirmed that low kinetic energy dry etching is able to prevent SiO_2/Si interface from generating the dark current.

A. Dark Current in BASIS

BASIS imager is composed of three elements: one n-p-n bipolar photo-transistor for amplification of carriers generated by light, one capacitor for the control of base voltage at storage and readout operations, and one p-MOS transistor for isolation between adjacent cells and clamp

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reset of base voltage, as shown in Fig. 1 [8], where the photodiode consists of a base-collector junction of the n-p-n bipolar photo-transistor. Electron-hole pairs generated by incident light are separated by the electrical field in the base-collector depletion region, releasing electrons to the collector. Holes are collected and stored in the base region. Therefore, the leakage current flowing into the base region becomes dark current in BASIS. The origin of the leakage current is classified into two groups. One is the surface current via the Si/SiO_2 interface states. It accounts for about 80% of the total dark current in a conventional BASIS. The other is the dark current, which is composed of the generation current in the base-collector depletion region and the diffusion current from the substrate.

In this paper, our attention is focused on the surface leakage current. The dark current in the surface region is found to vary drastically with the polysilicon etching procedure of the p-MOS gate and the capacitor. After the dry etching procedure of polysilicon layer with a thickness of 4000 Å on the p-base layer and impurity concentration of 1×10^{17} cm^{-3} through oxide film of 350 Å in CF_4–O_2 mixed gas plasma, the dark current level increases two and a half times more than that of the samples fabricated by using the wet etching of the solvent ($HF:HNO_3:H_2O = 1:60:60$). This result indicates that the dark current in the surface region is mainly caused by the plasma-induced damages during dry etching; i.e., the oxide to silicon interface damages resulting in degradation of electrical properties.

B. Dark Current Increase Due to Dry Etching

Fig. 2 illustrates the dark current density as a function of polysilicon dry etching time, where the current density is measured as a reverse current of the base-collector junction with an area of 2.5×10^{-4} cm^2 at a reverse-bias voltage of 3 V. The sample preparation is the same as that of the previous one [6]–[8].

As shown in Fig. 2, the dark current density scarcely increases in proportion to the etching time until the time when the polysilicon layer is just etched off, but it increases rapidly with the increase of the over-etching time just after the etching point of the polysilicon layer. It is seen in Fig. 2, furthermore, that the nonuniformity of the dark current in a wafer increases in proportion to the over-etching time just after the etching point. This means that the dry-etching-induced damages became remarkable during the over-etching when the oxide film in the p-base region is exposed to the etching plasma environment. An increase of fluctuations of the dark current due to the over-etching gives rise to an increase of FPN of BASIS.

C. Recovery of Dry-Etching-Induced Damage by Anneal Treatment

The following experiment was carried out to investigate the characteristics of the over-etching-induced damages, particularly the recovery properties of the anneal treatment.

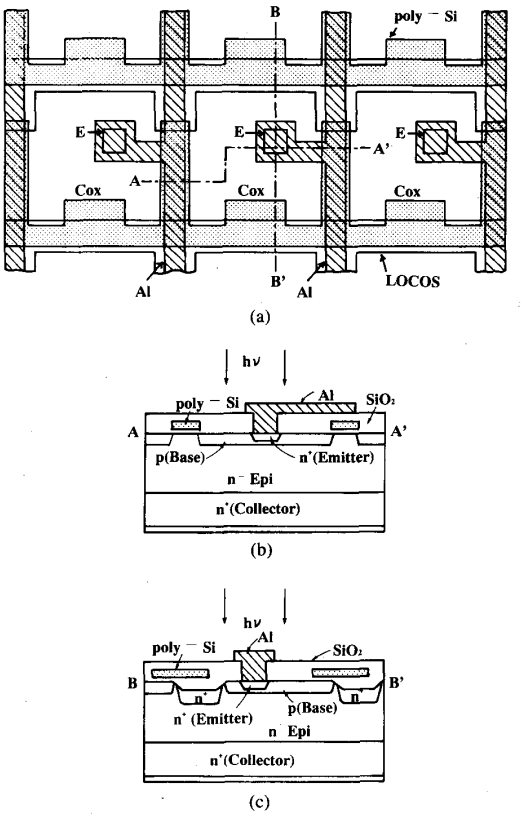

Fig. 1. (a) Schematic layout of BASIS imager showing three unit cells along with horizontal line. E is the contact hole for n^+ emitter region. C_{ox} is the capacitor for the control of base voltage. (b) Cross-sectional view along with AA' line of the plan view (a). (c) Cross-sectional view along the BB' line of the plan view (a).

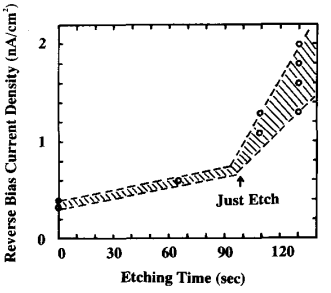

Fig. 2. Dark current density as a function of polysilicon dry etching time. The dark current is measured by the reverse-bias current of the base-collector junction having an area of 2.5×10^{-4} cm^2 at a bias of 3 V. Dry etching is carried out by CF_4–O_2 mixture gas plasma.

An oxide layer of 650 Å is formed on a p-n junction with a boron diffused area of 400×400 μm^2 in an n-type substrate with a resistivity of 0.2 Ω · cm (Fig. 3(a)). The p-n junction covered with the oxide is exposed to the CF_4–O_2 mixed gas plasma exited by RF of 100 W and 13.56 MHz at the working pressure of 150 mtorr during 60 s

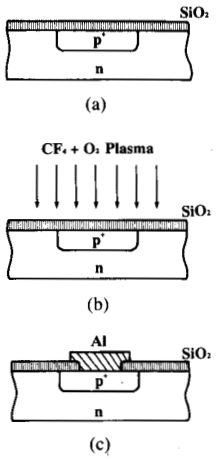

Fig. 3. The process flow for a sample to investigate characteristics of the damages caused by exposure to plasma through an oxide layer.

(Fig. 3(b)). The bombardment ion energy on the wafer surface under this condition is measured to be about 180 eV [16]. After this process, the oxide with thickness of more than 400 Å still remains on the p-n junction. Then, the contact hole to p^+ region is wet-etched and Al film is deposited by electron-beam evaporation (Fig. 3(c)). Before going to the Al metallization process, most of the samples have suffered thermal annealing in N_2 or (N_2 + H_2) environment.

Fig. 4 shows the effect of thermal annealing on the reverse current density of the p-n junction. The reverse current density at room temperature varies from 0.1 to 0.5 nA/cm^2 before the anneal treatment, which is much larger than the 0.03 nA/cm^2 of samples without the plasma exposure. It is confirmed that this tendency is very similar to the previous results, i.e., the increase of dark current in the n-p-n dipolar photo-transistor. In the case of the anneal treatment in N_2 gas ambient for 30 min, a temperature as high as 1000°C is required to anneal out the damages due to the exposure to the plasma environment. On the other hand, in the case of N_2/H_2 gas ambient ($N_2:H_2 = 9:1$), the damages are removed by the anneal treatment for 30 min at temperatures as low as 400°C, as shown in Fig. 4. Judging from the results, it is assumed that an exposure of the oxide-covered p-n junction to the plasma yields dangling bonds in the Si/SiO_2 interface, and that the dangling bonds can be terminated by hydrogen atoms with anneal treatment in N_2/H_2 gas ambient.

D. Low Kinetic Ion Energy Dry Etching

In order to confirm that high-energy ions in the plasma produce the damages [17], we evaluated the bombarding-ion energy dependence of the reverse current as shown in Fig. 5. The horizontal axis is the bombarding ion voltage V_{bomb}, which is defined by the difference between the plasma potential and the substrate electrode voltage. The vertical axis is the increment of the reverse current density of the p-n junction normalized by the bombarding ion flux

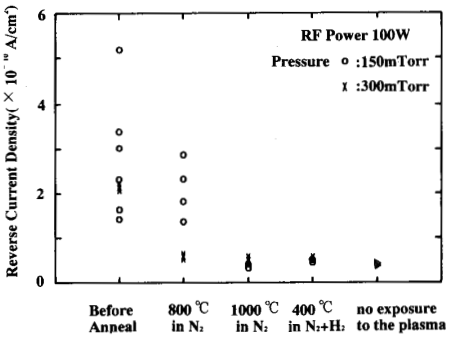

Fig. 4. Anneal treatment dependence of the reverse current density of the p-n junction exposed to plasma environment.

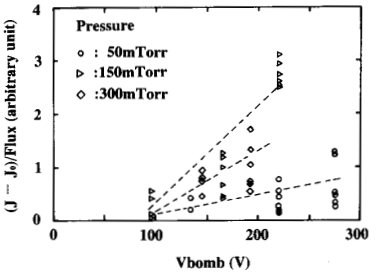

Fig. 5. The bombarding ion energy dependence of the reverse current density normalized by the bombarding ion flux, where J and J_0 are the reverse current density of the p-n junction with and without exposure to the plasma environment, respectively.

density in order to evaluate the damages caused by unit flux density. The sample preparation is the same as to that in Fig. 3. It is seen from Fig. 5 that the reverse current density starts to increase in proportion to the bombarding ion energy greater than a critical ion energy, i.e., 90 eV. The critical ion energy is maintained at the same level, such as 90 eV, for variations of gas working pressure from 50 to 300 mtorr.

As a result, dark current in the surface region is completely eliminated by the introduction of a two-step RIE for polysilicon where the polysilicon is etched by reactive ions having low bombarding energy, lower than 90 eV at the final stage, and the total dark current of 0.4 nA/cm^2 is achieved without any anneal treatment. It is equivalent to that found in the samples fabricated by wet etching.

III. Native-Oxide-Free Processing for Uniform Current Gain

The uniformity of current gain is essential to BASIS with very low level FPN. This section describes the problems of conventional polysilicon emitter, characteristics of native oxide growth, the necessity of native-oxide-free processing, and experimental results of contact resistance and uniformity of current gain of the bipolar transistor.

A. Conventional Polysilicon Emitter

The performance of bipolar transistors has been considerably improved by use of polysilicons as a diffusion source and a contact for the shallow emitter. This self-aligned structure enables the circuit with the bipolar transistor to realize high density and high speed. In the polysilicon emitter, the polysilicon/monosilicon interface structure greatly affects the bipolar transistor characteristics. From XTEM examination, it is found that the oxide layer exists at the interface and its thickness is about 20 Å. It has been reported [18]–[21] that a bipolar transistor with a low base current has been obtained by growing this thin oxide layer at the interface. This oxide is considered to act as a tunneling barrier against hole injection into the polysilicon. It is, however, difficult to control both the thickness and the quality of the oxide because the native oxide layer [22], [23] grows even at room temperature in air and in pure water where there oxygen and water coexist (moisture). Therefore, it is considered difficult for the conventional polysilicon emitter structure to realize uniform current gain of photo-transistors on the entire wafer surface.

B. Native Oxide Growth

Fig. 6 shows the thickness of the native oxide as a function of the exposure time of wafers to air at room temperature, where the moisture level in the air is about 1.2%. The growth rate of the native oxide on the n^+-Si is faster than that on lightly doped or p^+-Si. Therefore, it is rather impractical to control the thickness of the native oxide layer grown on the n^+ emitter surface. On the other hand, it is indicated from Fig. 6 that the native oxide hardly grows during 7 days in air where the H_2O concentration is set at very low level (less than 0.1 ppm). These results clearly indicate that the native oxide growth at room temperature requires the environment of co-existence of oxygen and moisture.

Fig. 7 shows the native oxide thickness as a function of the immersion time of wafers in ultra pure water at room temperature for different dissolved oxygen concentrations such as 9, 0.6, and 0.04 ppm in water. The growth rate of the native oxide on the n^+-Si is faster than that on the n-Si in pure water at the initial stage but tends to saturate to the film thickness of 10 Å while the native oxide growth continues on the n-Si. This result corresponds to a previous result in air. The native oxide thickness becomes thin as the dissolved oxygen concentration is lowered. Judging from these results on the native oxide growth in air and in pure water, the native oxide growth on the Si wafer surface at room temperature requires co-existence of oxygen and moisture.

C. Native-Oxide-Free Processing

In order to suppress the native oxide growth on the Si surface, it is necessary i) to use ultra pure water with low dissolved oxygen concentration, ii) to cover the wafer rinsing vessel by gas ambient with low oxygen concentration to prevent the diffusion of oxygen in the ambient into the ultra pure water and iii) to lower the moisture in the ambient during the wafer transport to the equipment.

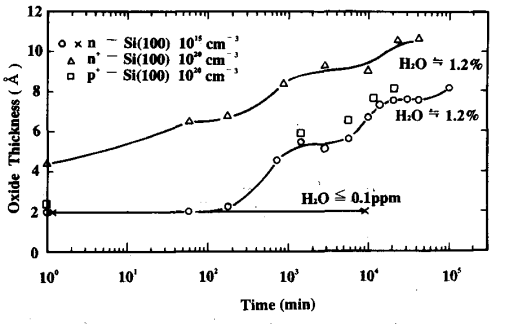

Fig. 6. Thickness of native oxide plotted as a function of the exposure time of wafers to air at room temperature, where the moisture levels are set at 1.2% and a level of less than 0.1 ppm.

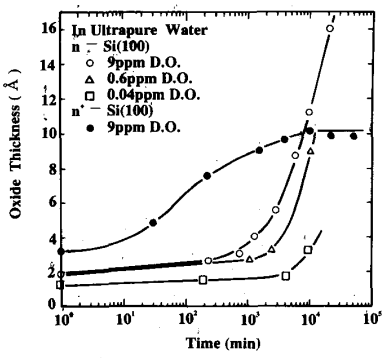

Fig. 7. Thickness of native oxide as a function of immersion time of wafers in ultrapure water at room temperature for different dissolved oxygen concentrations such as 9, 0.6, and 0.04 ppm.

Therefore, new wet cleaning apparatus has been developed in which ultra pure water and a diluted HF vessel are sealed by N_2 gas. Fig. 8 shows the block diagram of this equipment which consists of N_2 gas lines to form N_2 ambient and to dry the wafer surface. The supply system of ultra pure water and the real time monitors of the oxygen concentrations in the equipment and of the dissolved oxygen in the rinsing water are also mounted on this apparatus. By using this apparatus, the wafer is chemically etched with diluted HF acid dip, rinsed in the pure water with low dissolved oxygen of 20 ppb, dried by blowing N_2 gas, and put into the water case to be transported to a processing chamber in N_2 ambient with an oxygen concentration of less than 10 ppm. We call this process the N-process.

In order to confirm the effect of the N_2-gas-sealed rinsing and drying process on the suppression of the native oxide growth, the existence of a native oxide layer on the n^+-Si surface has been evaluated by X-ray photo-electron spectroscopy (XPS). Fig. 9 illustrates the XPS Si_{2p} spectra from silicon oxide on the n^+-Si surface obtained by the N-process and by the conventional process (C-pro-

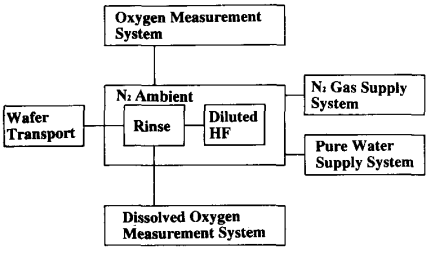

Fig. 8. Block diagram of newly developed wet cleaning equipment.

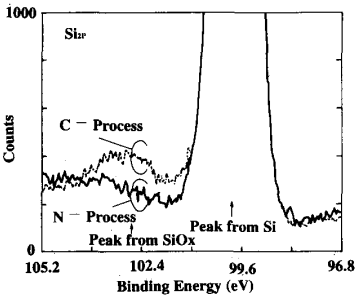

Fig. 9. XPS Si_{2p} spectra of n^+-Si surface in the N-process (solid line) and the C-process (dashed line).

cess). The difference between the N-process and the C-process is the dissolved oxygen concentration in the ultra pure water at the rinsing process (20 ppb in the N-process, 600 ppb in the C-process) and the environment in the rinsing, drying, and transporting (pure N_2 gas environment in the N-process, and air in the C-process) as shown in Table I. The area of Si_{2p} peaks from SiO_x ($0 < x \leqq 2$), which corresponds to the thickness of the native oxide on the Si surface, is significantly lower in the N-process than that in the C-process in Fig. 9. The N-process, therefore, is very effective in preventing the native oxide layers from growing on the n^+-Si surface.

D. Contact Resistance

To evaluate the electrical properties of the n^+-Si surface, the contact resistance is measured by the four-point probe Kelvin method [24]. The n^+ regions are formed by implanting 1×10^{16} cm^{-2} of arsenic at 70 keV and annealing at a temperature of 1000°C for 10 min in N_2 gas ambient. As a result, the sheet resistance and the surface carrier concentration of the n^+ region are 30 $\Omega/\square$ and 0.8×10^{20} cm^{-3}, respectively. In the Al sputtering chamber [25], the *in situ* substrate surface cleaning [26] is carried out in order to remove the absorbed impurity molecules such as moisture molecules by low kinetic energy Ar ion bombardment with an energy of 2 or 3 eV at the working gas pressure of 8×10^{-3} torr, and then Al films are deposited on the substrate under the optimum condition of bombarding Ar ion of 50 eV at the working pressure of 3×10^{-3} torr at room temperature. The measured contact resistance of samples in the N-process becomes as small as 0.4 $\mu\Omega \cdot cm^2$ without any thermal treatment, as illustrated in Fig. 10. This value is nearly equal to the conventional value obtained after 450–500°C anneal [27], [28]. Furthermore, it is seen from Fig. 10 that nonuniformity of the contact resistance in the wafer in the N-process is decreased by a factor of 3 compared to that in the C-process. Therefore, this N-process is very effective in obtaining low and stable emitter contact resistance of the photo-transistor in each picture cell.

TABLE I
PROCESS FLOW OF NEWLY DEVELOPED N_2 GAS SEALED PROCESS (N-PROCESS) AND CONVENTIONAL PROCESS (C-PROCESS)

Process Flow			Newly Developed Process (N-Process)	Conventional Process (C-Process)
Wet cleaning	diluted HF dip	ambient	N_2	air
	rinse	ambient	N_2	air
		dissolved oxygen	20 ppb	600 ppb
Wafer transport		ambient	N_2	air
Al deposition			bias sputtering	bias sputtering

The N-process consists of N_2 gas sealed cleaning and drying process, wafer transport in N_2 environment, and Al deposition by low-energy ion bombardment bias sputtering. All these processes are indispensable to obtain good electrical properties of the metal to Si interface. Ignoring any one of these processes leads to the degradation of these characteristics. As for wafer transport, the contact resistance and its nonuniformity become degraded when the wafer surface is exposed to the clean room atmosphere at a temperature of 23°C and relative humidity of 40% for 30 min after the cleaning and drying in N_2 gas ambient, as shown in Fig. 11. From this result, it is confirmed that the wafer transport in N_2 environment is also important for the native-oxide-free processing.

E. Uniformity of Current Gain

We have fabricated bipolar transistors in order to confirm that the native-oxide-free processing improves the uniformity of current gain. An n^+ emitter region (100×100 μm^2) on a p-base layer is formed by implanting 5×10^{15} cm^{-2} of arsenic at 70 keV and annealing at a temperature of 1050°C for 30 min in N_2 gas ambient. The contact layer for the n^+ emitter region is not fabricated by LPCVD polysilicon by Al deposited by rf-dc coupled mode bias sputtering [11], [25]. This is because the residual oxygen and moisture in LPCVD chamber gives rise to the oxidation of the n^+ emitter surface under relatively high temperature of about 600°C prior to polysilicon deposition, while, in the rf-dc coupled mode bias sputter, Al is deposited under the base pressure of 10^{-10} torr at room temperature [11], [25]. The absence of oxygen and moisture suppresses the growth of oxide on the n^+-Si surface. The collector and the base current are observed as a function of the base—emitter bias for samples fabricated

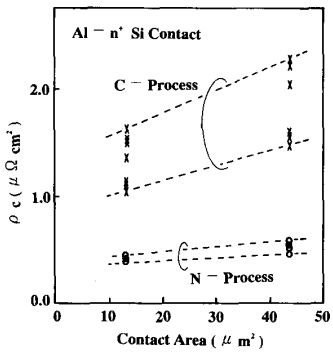

Fig. 10. Contact resistances of Al to n^+-Si as a function of contact hole size in the N-process and the C-process.

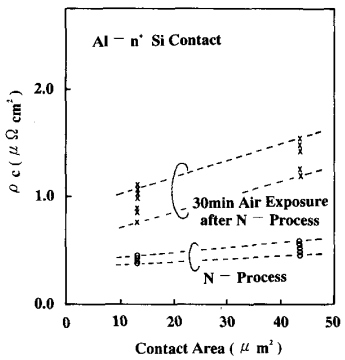

Fig. 11. Wafer transport ambient dependence of contact resistances of Al to n^+-Si as a function of contact hole size.

in the N-process and the C-process, as illustrated in Fig. 12. No difference in the collector current has been found between the N-process and the C-process because the difference of the contact resistance in the two processes can be neglected owing to the large contact area. The difference in the base current, however, is very clear in Fig. 12, which becomes more significant in the lower base current region. The base current in the C-process is always smaller than that of the N-process. The holes injected into the n^+ emitter region from the p base are able to reach the interface of the metal and Si because the junction depth of the n^+ emitter is about 0.2 μm. The native oxide layer formed in the C-process is as thin as 2–3 Å, but is considered to play a role of a barrier layer against the holes.

Further, the nonuniformity of the base and collector current of the bipolar transistors in a wafer is measured, which is defined as

$$\frac{\Delta I}{\bar{I}} = \frac{I - \bar{I}}{\bar{I}} \tag{1}$$

where I is base or collector current and $\bar{I}$ is the average value of I in a wafer.

The nonuniformity of the collector current $\Delta I_c/\bar{I}_c$ in either process is as negligibly small as 0.2%. On the other

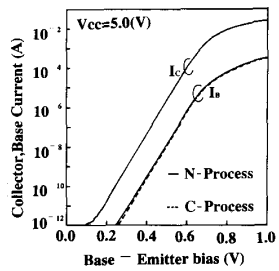

Fig. 12. Gummel plots of bipolar transisters fabricated in the N-process (solid) and the C-process (dashed).

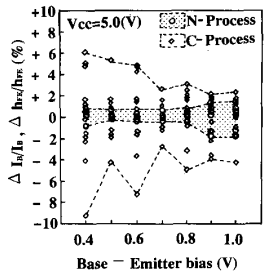

Fig. 13. Nonuniformity of base current and current gain as a function of base-emitter bias.

hand, the nonuniformity of base current $\Delta I_B/\bar{I}_B$ in the C-process is larger than that in the N-process as shown in Fig. 13. This result corresponds to the dc characteristics of (N or C) process dependence of base and collector current.

This is because in the C-process the fluctuation of the native oxide layer on each n^+ emitter surface causes nonuniformity of the recombination rate of holes injected into the n^+ emitter region at the metal–Si interface.

On the other hand, the nonuniformity of the current gain h_{FE} is given by

$$\frac{\Delta h_{FE}}{\bar{h}_{FE}} = \left\{ \left(\frac{\partial h_{FE}}{\partial I_c} \Delta I_c \right)^2 + \left(\frac{\partial h_{FE}}{\partial I_B} \Delta I_B \right)^2 \right\}^{1/2} = \left\{ \left(\frac{\Delta I_c}{\bar{I}_c} \right)^2 + \left(\frac{\Delta I_B}{\bar{I}_B} \right)^2 \right\}^{1/2} \tag{2}$$

because the nonuniformity of the base current is independent of that of the collector current. From the experimental results

$$\left| \frac{\Delta I_c}{\bar{I}_c} \right| \ll \left| \frac{\Delta I_B}{\bar{I}_B} \right|. \tag{3}$$

Consequently, the nonuniformity of current gain h_{FE} is mainly determined by that of the base current

$$\frac{\Delta h_{FE}}{\bar{h}_{FE}} \cong \frac{\Delta I_B}{\bar{I}_B}. \tag{4}$$

The uniform current gain has been achieved by the native-oxide-free processing due to the improvement of the uniformity of the base current.

IV. Conclusions

A future image sensor is required to realize a much higher resolution as well as higher quality. An imager with amplification capability in each picture cell is one of the promising devices with high sensitivity and wide dynamic range. In order to realize such an imager, it is necessary to get rid of FPN, which is mainly caused by nonuniformity of both dark current and current gain of the phototransistor in each cell.

The total dark current of 0.4 nA/cm^2 is achieved by suppressing nearly all dark current generated at the SiO_2/Si interface using low kinetic ion energy dry etching technique. On the other hand, the nonuniformity of current gain in the bipolar transistor is caused by the native oxide layer on the n^+ emitter region because it is difficult to control both the thickness and the quality of the native oxide. In order to solve the problem, native-oxide-free processing has been developed; N_2-gas-sealed wet cleaning using pure water with low dissolved oxygen (20 ppb), wafer drying, wafer transporting, and wafer loading to the processing chamber in N_2 gas environment and metal deposition by sputtering with low-energy ion bombardment. The uniformity of current gain has become less than 2% in a wide range of collector current by the introduction of this newly developed processing technique.

From both experimental results of monitor transistors, the emitter dark voltage nonuniformity ΔV_{Ed} and the dynamic range are assumed to be 0.5 mV and 70 dB, respectively, for a typical area sensor using the analytical equations of BASIS [29]. The main component of the nonuniformity ΔV_{Ed} is caused at the transient reset and readout operation due to the nonuniformity of current gain rather than that of dark current. Therefore, further improvement of the current gain uniformity is required to obtain a wider dynamic range.

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