Dependence of thin-oxide films quality on surface microroughness

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Dependence of Thin-Oxide Films Quality on Surface Microroughness

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Abstract—**Effect of silicon surface microroughness on electrical properties of thin-oxide films such as breakdown electric field intensity (E_{BD}) and time-dependent dielectric breakdown (Q_{BD}) have been studied, where microroughnesses of silicon surface and silicon dioxide surface are evaluated by the scanning tunneling microscope (STM) and the atomic force microscope (AFM), respectively. An increase of surface microroughness has been confirmed to severely degrade the E_{BD} and Q_{BD} characteristics of thin-oxide films having thickness of 8–10 nm and to simultaneously decrease channel electron mobility. An increase of surface microroughness has been demonstrated to mainly originate from wet chemical cleaning processing based on RCA cleaning concept, particularly the ammonium-hydrogen peroxide cleaning step. In order to keep the surface microroughness at an initial level, the content ratio of $NH_4OH/H_2O_2/H_2O$ solution has been proved to be set at 0.05 : 1 : 5 and the room-temperature DI water rinsing has been confirmed to be introduced right after the $NH_4OH/H_2O_2/H_2O$ cleaning step in conventional RCA cleaning procedure.**

I. Introduction

IN MANUFACTURING processes of submicrometer and deep-submicrometer ULSI's, surface microstructure and surface cleanliness of substrates are going to increase their significance as crucial for device performance and reliability [1], [2]. So far, substrate surface cleaning procedures have generally been carried out based on RCA cleaning concept [3], which has been confirmed to effectively eliminate substrate surface contaminations such as particulate, organic, and metallic materials [4]. On the other hand, a continuous decrease of device dimension is going to increase the importance of surface microroughness on device performance and reliability, where devices consist of very-thin-oxide films and very-shallow junctions. It has already been reported that the surface microroughness of substrates is mainly caused by an alkaline solution treatment such as NH_4OH in RCA cleaning process and that the NH_4OH content in $NH_4OH(28\%):H_2O_2(30\%):H_2O$ solution is recommended to be reduced to the mixing ratio of 0.25 : 1 : 5 from the conventional ratio of 1 : 1 : 5 to suppress the increase of surface microroughness, where the surface microroughness has been evaluated by optical random reflection [5].

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In this paper, the influence of surface microroughness on electrical characteristics of thin-oxide films such as breakdown electric field intensity (E_{BD}), charge to breakdown (Q_{BD}), and channel electron mobility has been studied, where the surface microroughness is varied through $NH_4OH/H_2O_2/H_2O$(APM) cleaning procedure.

The experimental procedure is described in Section II, and experimental results are shown and discussed in Section III. Conclusion are given in Section IV.

II. Experimental

Wafers used in these experiments are phosphorus (p)-doped n-type CZ (100) wafers with a resistivity of 8–12 $\Omega \cdot$ cm and an average surface miocroroughness of 0.2 nm, where native oxides are etched by an advanced buffered hydrogen fluoride with low NH_4F concentration of 17% and surfactants (advanced surface active BHF) for 1 min in order to suppress further increase in surface microroughness [6], [7]. Since surface microroughness is mainly varied by APM cleaning procedure in wet chemical processing, wafer surfaces are treated with APM solutions having various NH_4OH mixing ratios for 10 min at 85°C. At the final stage of wet chemical processing, wafers are rinsed in ultrapure water including dissolved oxygen of less than 0.6 ppm for 5 min and dried by ultra-clean N_2 gas blow to prevent the growth of native oxides [8]–[10]. The surface microroughness before and after the cleaning procedure has been evaluated using scanning tunneling microscope (STM: SAM3100, SEIKO Electronic Inc.). Surface microroughness widely varies depending on NH_4OH mixing ratio in the APM solution and the succeeding ultrapure water rinsing procedure. Wafers having various surface microroughnesses are oxidized at 900°C in ultra-clean dry oxygen ambient [11]. Then, aluminum films are deposited on these thermal oxide films to fabricate MOS diodes without field oxides for evaluation of their electrical characteristics. Surface microroughness of oxide films is evaluated by atomic force microscope (AFM: AS-0.5, Digital Instruments) and their thickness by ellipsometry.

III. Results and Discussion

A. Measurement of Surface Microroughness

Scanning tunneling microscope (STM) has been widely used to investigate surface microstructure of conductive materials because of its high spatial resolution and its ca-

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pability of nondestructive observation, where native oxides of conductive materials such as semiconductors must be eliminated before STM measurements. Thus native oxide removal procedure has a great significance for the STM evaluation. So far, diluted HF cleaning is very popular to eliminate native oxides on silicon surfaces at the final stage of wet chemical processings. We have revealed, using XPS, that the native oxide is eliminated by diluted HF and advanced BHF. Diluted HF cleaning has been confirmed to give run-to-run fluctuations, particularly for fixed charge densities of thin-oxide films formed on n-type CZ wafer due to its poor wettability, as shown in Fig. 1, so that native oxides are eliminated by using advanced BHF in this experiment resulting in run-to-run fluctuation-free oxidations, as shown in Fig. 1 [6], [7].

This remarkable difference mainly comes from the difference of surface microroughness of n-type CZ wafers treated in different chemical solutions, as shown in Fig. 2, where average surface microroughnesses (*Ra*) are illustrated for three different chemical cleaning procedures for 10 min such as diluted HF (0.5%), conventional BHF having NH_4F concentration of 35–38%, and advanced surface active BHF having NH_4F concentration of 17% and surfactant. It is clearly seen in Fig. 2 that average surface microroughness and its fluctuation level become smallest in advanced surface active BHF cleaning. Here, the *Ra* means an average value of surface microroughness obtained by an average of 15 data. The influence of surface microroughness on fixed charge density is considered to come from an increase of imperfections in oxide films such as Si_2O_3, dangling bond, and void.

Surface microroughness of oxide films has been confirmed to reflect the substrate surface microroughness by an atomic force microscope (AFM) evaluation. Correlation of the surface microroughness of silicon and silicon dioxide of substrates having two different surface microroughness of 0.2 and 0.7 nm is shown in Fig. 3, where the thickness of oxide films is 5 nm. It is seen from Fig. 3 that the surface microroughness of silicon dioxide is clearly seen to strictly depend on the surface microroughness of the substrate.

B. Surface Microroughness by Wet Cleaning Processing

Existence of surface microcontaminations such as particulates, organic and metallic impurities, and native oxide has been demonstrated to degrade device performance and reliability, as well as production yield. Before starting the succeeding processing, then, these impurities are removed by wet chemical reactions such as oxidation, reduction, or a combination process based on the RCA cleaning concept proposed by Kern in 1970 [3]. The RCA cleaning concept has not placed any importance on surface microroughness, because, at that time, the pattern dimension of devices was very large, at the level of 10 μm with thick gate oxides in the order of hundreds of nanometers. In this study, at first, the surface microroughness is evaluated for typical cleaning solutions such as $H_2SO_4(98\%)/H_2O_2$ (30%), $HCl(36\%)/H_2O_2$, and $NH_4OH(28\%)/H_2O_2$ as shown in Figs. 4 and 5. Fig. 4 shows the surface microroughness of silicon wafers treated

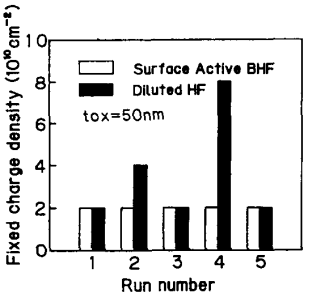

Fig. 1. Run-to-run fluctuations of fixed charge densities for oxide films formed on n-type CZ substrate after diluted HF and advanced surface active BHF etching.

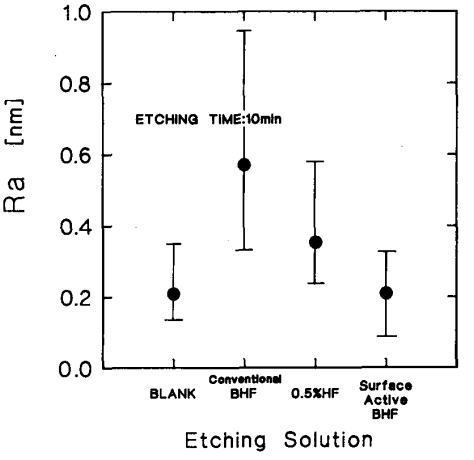

Fig. 2. Relationship between surface microroughness of n-type CZ wafer and various etching solutions, where blank wafer means a wafer treated in advanced BHF for 1 min.

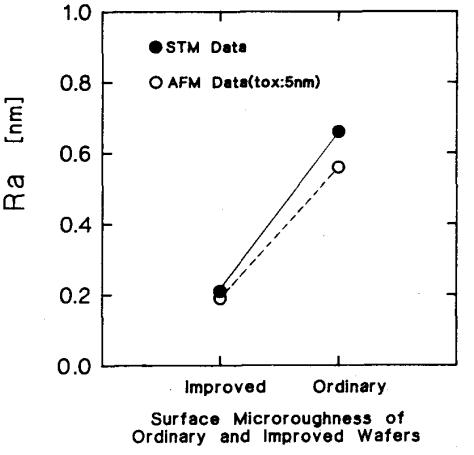

Fig. 3. Correlation of the surface microroughness of Si and SiO_2 for two substrates with microroughness of 0.2 and 0.7 nm, where the surface microroughness of Si and SiO_2 are evaluated by STM and AFM, respectively.

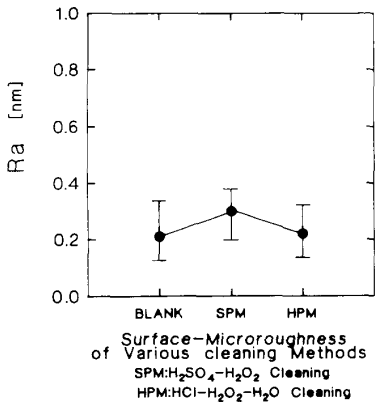

Fig. 4. Surface microroughness is plotted for HPM cleaning and fourth time cyclic SPM cleaning.

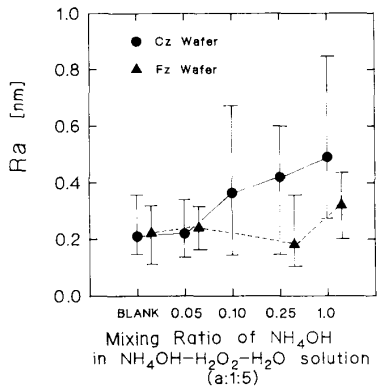

Fig. 5. Relationship of surface microroughness of CZ and FZ wafers to APM cleaning with various NH_4OH mixing ratios.

by $H_2SO_4:H_2O_2$ in the ratio of 4:1(SPM) and $HCl:H_2O_2:H_2O$ in the ratio of 1:1:6 (HPM). It is recognized from Fig. 4 that wet chemical procedures in SPM and HPM solutions scarcely influence the increase in surface microroughness. A small increase of surface microroughness in SPM cleaning mainly comes from its fourth time cyclic repetition of SPM and advanced surface active BHF cleaning. We next checked the dependence of surface microroughness of the CZ and FZ wafers on APM solutions as shown in Fig. 5, where the NH_4OH mixing ratio is changed from 1:1:5 to 0.05:1:5 at temperatures of 85°C. The surface microroughness of CZ wafer gradually increases with an increase of the NH_4OH mixing ratio in APM solution. On the other hand, the surface microroughness of FZ wafer dependence on NH_4OH mixing ratio becomes less significant. It is seen from Fig. 5 that the surface microroughness and its fluctuation are maintained at the same level as that of initial wafers when the NH_4OH mixing ratio is decreased down to 0.05 compared to the conventional ratio in APM solution. Typical STM images of wafers treated in APM solutions with a mixing ratio of 0.05:1:5 and 1:1:5 are shown in Fig. 6(a) and (b). CZ wafers have been shown to be very weak for alkaline solution cleaning to maintain their surface smoothness compared to FZ wafers, as shown in Fig. 5. From these results, surface microroughness in wet processing is considered to originate from nonuniform existence of a Si vacancy cluster in CZ substrates, where Si vacancy concentration has been estimated to be higher in CZ wafers than that in FZ wafers from their growth mechanism. Influence of point defects such as Si vacancy on surface microroughness in wet chemical processings will be described in detail in a forthcoming article [12].

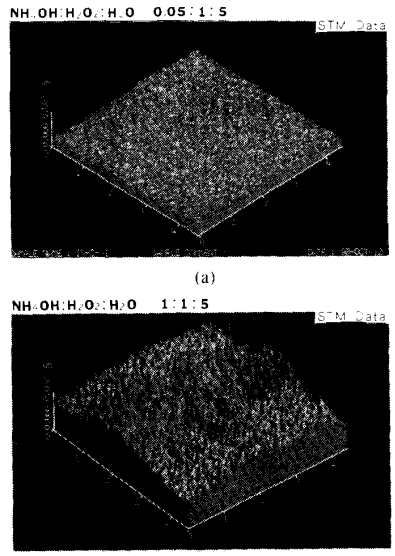

Fig. 6. Typical STM images of wafer surfaces treated in APM cleaning with a mixing ratio of 0.05:1:5(a) and 1:1:5(b). Measured area is 4.5 × 4.5 μm^2.

In Fig. 5, it has been demonstrated that the APM solution with a mixing ratio of 0.05:1:5 (improved APM) exhibits surface-microroughness-free cleaning capability. Then, the entire RCA cleaning process is evaluated by the introduction of improved APM solution. Fig. 7 shows surface microroughness of wafers treated by the entire RCA cleaning process with four different NH_4OH mixing ratios in the APM solution. Even if the improved APM solution is introduced, an increase of surface microroughness is observed as shown in Fig. 7. The result indicates that there exist other factors causing surface microroughness in cleaning processing in addition to the excess NH_4OH mixing ratio in the APM solution. In order to make this problem clear, we have evaluated the influence of the succeeding step of APM cleaning on surface microroughness, as shown in Fig. 8, where two succeeding steps 2 and 3 of the APM cleaning procedure are tested in addition to the conventional process 1 such as

1: $NH_4OH/H_2O_2/H_2O \rightarrow$ hot DI water $\rightarrow$ RT DI water rinsing,

2: $NH_4OH/H_2O_2/H_2O \rightarrow$ 0.1%HCl $\rightarrow$ hot DI water rinsing,

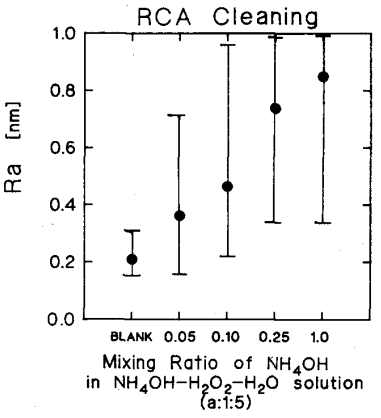

Fig. 7. Surface microroughness of wafer treated in a complete RCA cleaning process having four different NH_4OH mixing ratios in the APM solution.

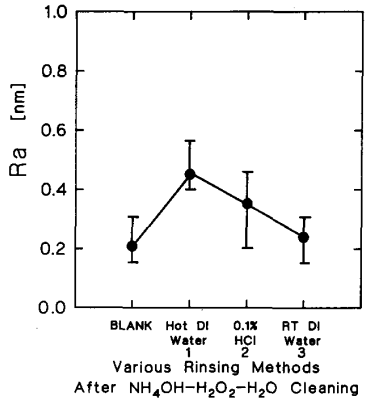

Fig. 8. Influence of succeeding steps of APM cleaning on surface microroughness, i.e., 1: APM → hot DI water → RT DI water, 2: APM → 0.1%HCl → RT DI water, 3: APM → RT DI water → hot DI water.

3: $NH_4OH/H_2O_2/H_2O$ → RT DI water rinsing → hot DI water.

Here, the improved APM cleaning has been used. It is seen in Fig. 8 that the surface microroughness increases due to the conventional hot DI water rinsing procedure even if an improved APM cleaning process is used. According to Fig. 8, the introduction of room-temperature (RT) pure water rinsing right after the APM cleaning has been confirmed to prevent an increase of surface microroughness while the diluted HCl cleaning is not enough to suppress an increase of surface microroughness. This comes from the fact that the NH_4OH is introduced to the succeeding hot DI water rinsing vessel by adsorbing on the wafer and the wafer cassette in the conventional wet chemical processing, resulting in changing the hot DI water to an alkaline solution with $pH = 8.0$. The alkaline solution is well known to increase the surface microroughness particularly at high temperatures. Thus it has been shown that the surface smoothness of substrates can be maintained by introducing a combination of an improved APM cleaning process and a succeeding room-temperature DI water rinse, i.e., the advanced APM cleaning.

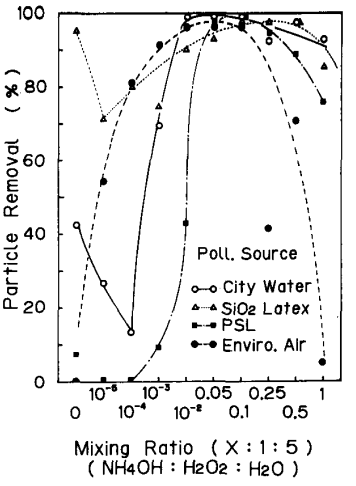

Fig. 9. Particle removal efficiencies are plotted as a function of NH_4OH mixing ratio in APM cleaning for four different particles such as PSL, silica latex, particles from city water, and particles from outside air.

A combination of room-temperature DI water rinsing and succeeding hot DI water rinsing just after the APM cleaning step has already been confirmed essential to completely eliminate particles, particularly organic particles from wafer surfaces [13]–[15].

C. Particulate and Metallic Impurity Removal Efficiencies

So far, it has been demonstrated that the advanced APM cleaning maintains the surface smoothness of substrates. The APM cleaning is mainly used to remove particulates from wafer surface. Thus particulate removal efficiency of the APM cleaning is evaluated for various NH_4OH mixing ratios as shown in Fig. 9, where four different particulates such as polystylene latex (PSL), silica latex, particulates from city water, and particulates from outside air have been evaluated. These results clearly indicate that the particulate removal efficiency is optimized at the NH_4OH mixing ratio ranging from 0.05 to 0.10 compared to the conventional mixing ratio [13]–[15]. In an on-going study, we are looking for the reason why particulates from outside air are not almost completely removed by the APM solution with the conventional mixing ratio.

Furthermore, the metallic contaminant removal capability of the APM cleaning has been evaluated for typical metallic impurities such as Fe, Ni, and Cu by Total Reflection X-Ray Fluorescence (TRXRF) (TREX610: Technos Inc.) with a very small glancing angle such as 0.05°, as shown in Fig. 10, where wafer surfaces have been contaminated to the level of 10^{12}–10^{13} atoms/cm^2 by dipping them into the DI water containing Fe, Ni, and Cu of 100 ppb for 60 min. After 60-min dipping in the DI water, wafer surfaces are covered by native oxides [8]. The re-

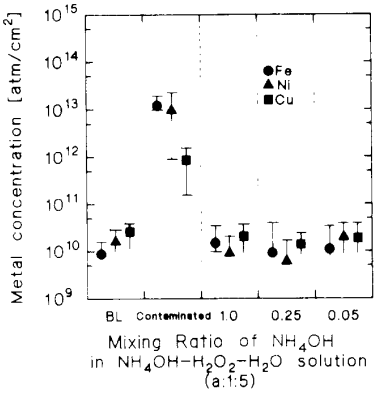

Fig. 10. Metallic impurities removal efficiency by APM cleaning having three different NH_4OH mixing ratios for Fe, Ni, and Cu.

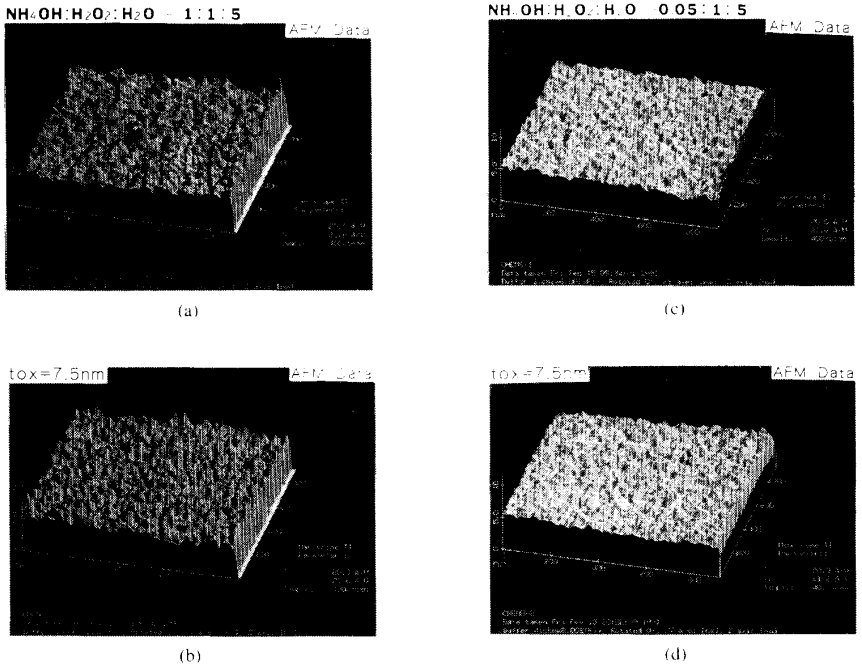

Fig. 11. Typical AFM images of substrate surface and oxide film surface, where substrate is treated by APM cleaning with mixing ratio of 1:1:5 in (a) and its oxidized surface in (b) while substrate is treated by APM cleaning with mixing ratio of 0.05:1:5 in (c) and its oxidized surface in (d). Oxide film thickness is 7.5 nm.

maining surface metallic impurities on wafers treated in the APM solution are almost identical as those of a blank sample, even if the NH_4OH mixing ratio is varied from the conventional mixing ratio to 5%. The APM solution has been confirmed to be very effective in eliminating particulates and metallic contaminants from wafer surfaces even when the NH_4OH mixing ratio is decreased down to 5% of the conventional ratio.

D. Influence of Surface Microroughness on Electrical Characteristics of Thin-Oxide Films

With reduction of minimum dimensions in ULSI devices, the thickness of oxide films, such as gate oxides and storage capacitor oxides, is going to decrease continuously, so that the quality of very-thin-oxide films must be improved to guarantee device performance and reliability, as well as production yield. In this experiment, we have confirmed the existence of a very close interrelationship between the electrical characteristics of thin-oxide films, such as dielectric breakdown field intensity E_{BD} and charge to breakdown Q_{BD} on the surface microroughness of the substrate, i.e., Si–SiO_2 interface microroughness.

At first, it is very important to note that the surface of oxide films severely reflects the surface microroughness of substrates as shown in Fig. 11(a)–(d). Here, the sur-

face images of substrates and oxide films are obtained for two different samples with oxide films of 7.5-nm thickness by using AFM where one sample is treated in conventional APM solution, as shown in Fig. 11(a) and (b), and the other in the advanced APM, Fig. 11(c) and (d). The oxide film surface continuously reflects surface microroughness of the substrate even if oxide thickness is increased up to hundreds of nanometers [16].

MOS diodes with an area of 1.6×10^{-4} cm^2 have been fabricated by evaporating aluminum films on oxide films having thickness of 9.8 and 8.2 nm for substrates with various surface microroughnesses. Breakdowns field intensity E_{BD} is defined by the applied voltage giving a diode current of 1×10^{-4} A. Dielectric breakdown field intensity E_{BD} has been confirmed to increase with a decrease of surface microroughness as shown in Fig. 12, with sharpening of its distribution as shown in Fig. 13, where the histogram of E_{BD} distribution is illustrated for two samples with an average surface microroughness of 0.8 nm in Fig. 13(a) and 0.2 nm in Fig. 13(b). Since these MOS diodes are fabricated without field oxides, electric field intensity tends to concentrate at the edge of the aluminum electrode due to the fringing effect. Fig. 14 shows liquid crystal images of these MOS diodes, where hot spots appear along the electrode edge for a diode with an average surface roughness of 0.2 nm, as shown in Fig. 14(b), while hot spots are widely distributed in the entire area of the aluminum electrode in the MOS diode with an average surface microroughness of 0.8 nm, as shown in Fig. 14(a).

Next, the charge to breakdown Q_{BD} has been evaluated at a field intensity of 9.5 MV/cm for these MOS diodes with an area of 1.60×10^{-4} cm^2, as shown in Fig. 15, where the breakdown is defined by the diode current increasing up to 1×10^{-5} A. It is clearly seen from Fig. 15 that the value of Q_{BD} rapidly increases with a decrease of surface microroughness. The Q_{BD} characteristics strictly relate to the reliability of ULSI devices having very-thin-oxide films. Results obtained in Figs. 14 and 15 clearly indicate the importance of substrate surface smoothness in future advanced ULSI particularly for reliability.

With a reduction of device dimension, the thickness of the inversion layer is going to decrease due to an increase of impurity concentration in the substrates, so that the Si–SiO_2 interface microroughness has a strong influence on the channel mobility of carriers. Here, the influence of surface microroughness has been evaluated on electrical characteristics of n-MOS transistors with a substrate impurity concentration of 4.5×10^{17}/cm^3, an oxide thickness of 10 nm, channel length (L) of 7 μm, gate width (W) of 100 μm, and junction depth of 1.0 μm. Fig. 16 shows typical current–voltage characteristics for two transistors with an average surface microroughness of 0.6 nm (dashed line) and of 0.3 nm (solid line), and where the threshold voltage is 0.88 V (dashed line) and 0.75 V (solid line). The surface microroughness is varied by the NH_4OH mixing ratio in the APM solution. It is clearly seen in Fig.

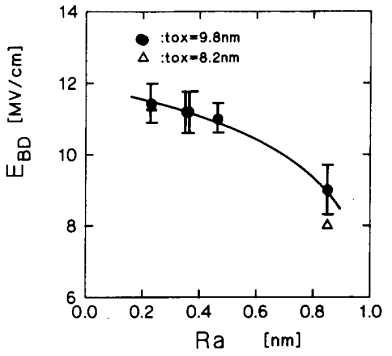

Fig. 12. Dielectric breakdown field intensity (E_{BD}) plotted as a function of average surface microroughness for two oxide films having a thickness of 9.8 and 8.2 nm formed on n-type substrate.

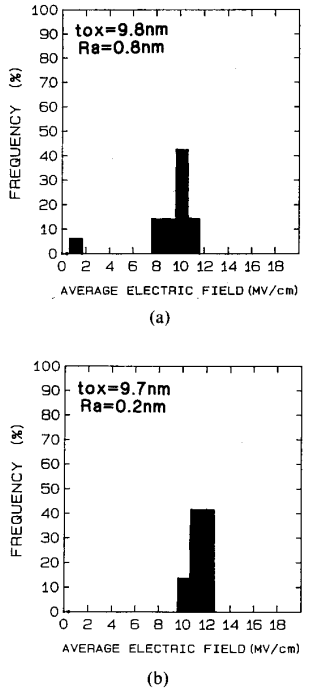

Fig. 13. Dielectric breakdown histograms for oxide film of 9.8-nm thickness having average surface microroughness Ra = 0.8 nm in (a) and oxide film of 9.7-nm thickness having average surface microroughness Ra = 0.2 nm in (b).

16 that the saturation current increases with a decrease of surface microroughness. The transconductance g_m of the MOS transistor is demonstrated experimentally to improve by decreasing the Si–SiO_2 interface microroughness, resulting in an improvement of speed performance of ULSI where the propagation delay is approximately given by the ratio of load capacitor C_L to transconductance g_m. The channel mobility of electrons in these MOS transistors has been calculated as a function of surface microroughness from these current–voltage characteristics at a drain voltage of 4 V, as shown in Fig. 17, where

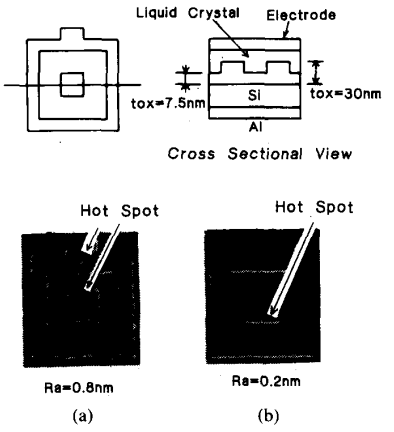

Fig. 14. Liquid crystal images of MOS diodes with an average surface microroughness of 0.8 nm(a) and 0.2 nm(b). Diode structures are illustrated.

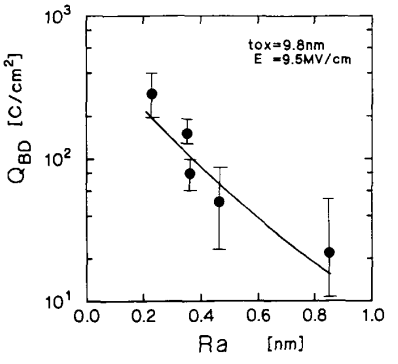

Fig. 15. Surface microroughness dependence of Q_{BD} (C/cm^2) under a constant fieldof 9.5 MV/cm.

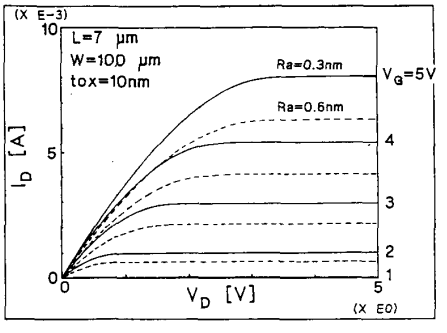

Fig. 16. Typical current–voltage characteristics for two MOS transistors with average surface microroughness of 0.6 nm (dashed line) and 0.3 nm (solid line).

the channel mobility of electrons u_c is derived by the current–voltage characteristic in the saturation region, i.e.,

$$I_D = \frac{\mu_c W C_{ox}}{2L} (V_G - V_{TH})^2.$$

The channel mobility of electrons has been confirmed to increase from 170 cm^2/V · s at an average surface microroughness of 1.5 nm to 370 cm^2/V · s at an average surface microroughness of 0.2 nm. Bulk mobility of electrons in the p-type substrate with an impurity concentration of $4.5 \times 10^{17}/\text{cm}^{-3}$ is about 400 cm^2/V · s from the Irvin curve. In the saturation current region, channel mobility suffers from scattering of the Si–SiO_2 interface microroughness [17]. Detail discussions on channel mobility of carriers will be published in forthcoming article [18].

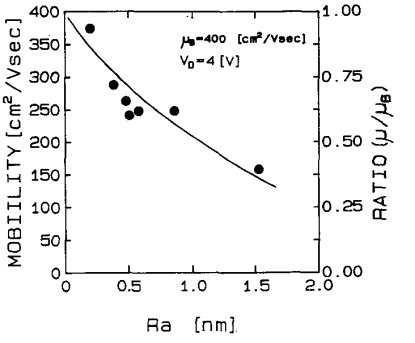

Fig. 17. Relationhip of channel electron mobility (μ_c) to Si–SiO_2 interface microroughness obtained in the current saturation region, where the channel electron mobility normalized by the bulk electron mobility is also plotted.

These results clearly indicate the importance of surface microroughness on MOS transistor performances, particularly its speed performance as well as reliability.

IV. Conclusions

It has been experimentally demonstrated that the quality of thin-oxide films is strictly governed by the surface microroughness of substrates where the surface microroughness has been evaluated by the scanning tunnel microscope (STM) and the atomic force microscope (AFM). The surface microroughness of oxide films has been proven to strongly depend on the microroughness of their substrates. The electric breakdown field intensity E_{BD} and charge to breakdown Q_{BD} have been confirmed to increase with a decrease of surface microroughness with accompanying improvement of their run-to-run uniformity, resulting in an improvement of device reliability and production yield. Moreover, the decrease of surface microroughness has been confirmed to increase the transconductance of the MOS transistor due to an improvement in channel mobility of carriers resulting in an improvement of speed performance of ULSI. In order to maintain an excellent surface smoothness, wet chemical cleaning processing has been improved by an introduction of a low NH_4OH mixing ratio in the $NH_4OH/H_2O_2/H_2O$ cleaning process with a mixing ratio of 0.05 : 1 : 5 and following with a room-temperature DI water rinse right after the $NH_4OH/H_2O_2/H_2O$ cleaning to prevent the introduction of the NH_4OH adsorbed to wafers and the wafer cassette to the hot DI water cleaning vessel. Initial surface smoothness has been demonstrated experimentally to be

maintained at the same level by the introduction of these new wet chemical cleaning processes for CZ and FZ wafers. It is very important that the initial surfaces of the wafers are as smooth as possible. We have shown that the $NH_4OH/H_2O_2/H_2O$ solution exhibits excellent particulate and metallic impurity removal capability even if the NH_4OH mixing ratio is decreased down to 0.05 of the conventional ratio.

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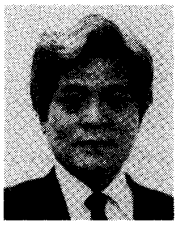

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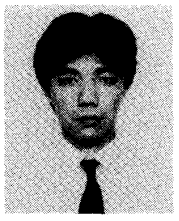

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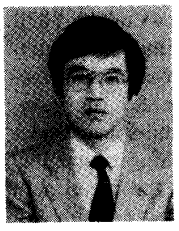

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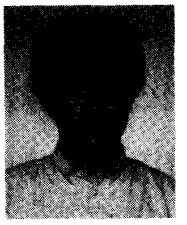

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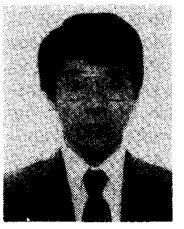

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