A Real-Time Center-of-Mass Tracker Circuit Implemented by Neuron MOS Technology

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A Real-Time Center-of-Mass Tracker Circuit Implemented by Neuron MOS Technology

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***Abstract*— A new-architecture integrated circuit has been developed as a key element of a system that can real-time track the center of mass of an moving image on a two-dimensional (2-D) pixel array. The circuit has been implemented using a high-functionality transistor called neuron MOSFET (neuMOS or νMOS for short), hence having a very simple circuit configuration. A quasi-two-dimensional algorithm is assumed for system in the circuit. A one-dimensional (1-D) array of neuron MOS circuits automatically finds the center-of-mass location using the image intensity distribution projected onto x or y axis. The unique feature of the circuit is that it accepts analog inputs without A/D conversion but produces binary outputs, thus providing a very smooth interfacing between the real world and digital systems. Test circuits have been fabricated by a double-polysilicon CMOS process and their operation has been experimentally demonstrated.**

***Index Terms*—Center of mass, neuron MOS, source follower.**

I. Introduction

CENTER-OF-MASS (COM) detection of an image on a two-dimensional (2-D) pixel array is a very important operation in image processing. The COM, or the first moment of the object's intensity distribution, represents the position of an object. Therefore, it is utilized for the object tracking of a robot using a visual feedback system [1]. Since the real-time response of a system is the most important concern in such applications, the COM of an image needs to be detected with minimum latency. However, sequential digital computing schemes cannot meet this requirement. A large volume of 2-D image data must be all A/D converted in the first place by pixel-by-pixel bases and then sequentially computed by a general purpose computer. Such schemes are very time consuming due to the data conversion and transfer bottle necks. In order to resolve the difficulty, several focal plane processing schemes have been proposed based on analog [2]–[5] as well as digital techniques [1] in which photo sensors are fused into the array of fine grain parallel processing elements.

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A position-detective sensor proposed by Ishikawa and Shimojo [3] is an example of such parallel sensors implemented by analog circuits. The sensor has a latticed network structure in which a current source and linking resistors are provided at each node. The network works as a Poisson equation solver and the values of the zeroth moment (total mass) and the first moment (centroids) are obtained from the boundary potentials of the circuit, where the area integral was reduced to the boundary integral using Green's theorem [3]–[5]. Integrated imaging chips have been developed employing the resistor grid and photo-sensor-cell array architectures [6], [7]. The orientation of an object was also obtained by detecting the second moments of the image intensity distribution [6]. The output signals of these circuits are all analog, therefore they must be A/D converted for interfacing to digital systems.

A digital architecture in which a SIMD digital processor having A/D conversion capability is integrated at each pixel has been developed [1]. Such a system can present a very versatile feature and can carry out various image processing tasks such as averaging, edge enhancement/detection, orientation detection, optical flow, etc., in addition to the moment detection. The output is provided in a digital format, thereby providing an easy interfacing to digital systems. However, cost must be paid for the increased hardware volume at each pixel, which must be traded off with the image resolution.

The COM tracker circuit of this paper presents a unique architecture in which the input image signals are handled in an analog domain to some extent but binary decision (thresholding) is immediately given to the analog computation results at a very primitive device level. Therefore, the outputs are always digital. The circuit has a very simple configuration and operates very fast. Such a unique architecture of the circuit has been developed using a multiple-input-terminal, high-functionality transistor called neuron-MOSFET (νMOS or neuMOS for short) [8]. The device is capable of performing the weighted summation of multiple input signals and thresholding based on the sum at a single transistor level. Due to its functional similarity to the mathematical model of a biological neuron [9], it bears the name. The versatile features of the device have been demonstrated by applications to binary logic circuits [10]–[12], a neural network having an on-chip self-learning capability [13], [14], multi-valued circuits [15], [16], and flexible-computing architecture circuits for intelligent data processing [17]–[19].

In Section II, the organization of a νMOS center-of-mass (COM) tracker circuit is explained and its operation is demonstrated by experiments conducted on fabricated test circuits.

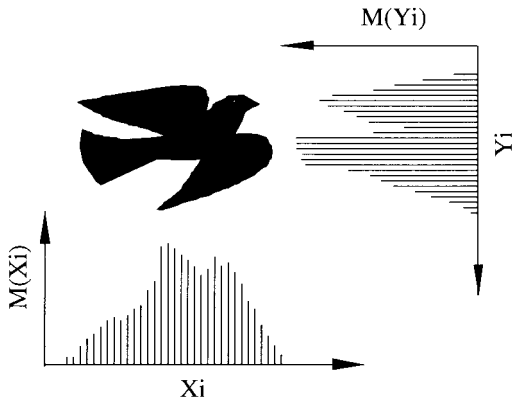


Fig. 1. Hardware computing algorithms for center of mass (COM) detection. Data processing is carried out on 1-D image intensity distribution obtained by X and Y projection.

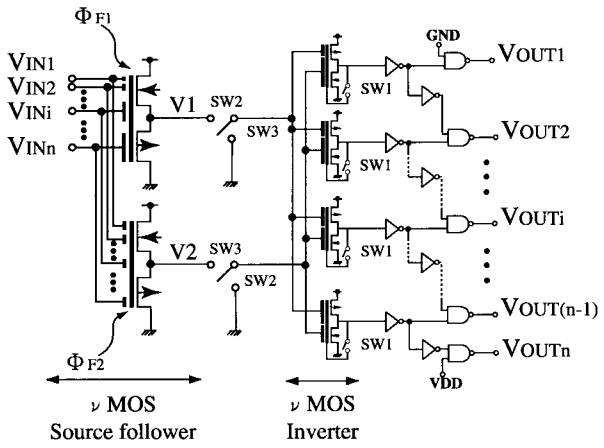


Fig. 2. Circuit diagram of COM (center of mass) tracker circuit.

The analysis of the circuit operation and a circuit technique to enhance the precision of computation are presented in Section III. A two-staged COM circuit architecture has been developed in order to handle a sensor array having a large number of pixels, which is presented in Section IV. Experimental verification of the circuit operation by fabricated test circuits is also demonstrated. Finally, conclusions are given in Section V.

II. Circuit Organization and Operation

A. COM Tracker Circuit Design

In Fig. 1, the basic hardware computing algorithms for COM detection is schematically explained. As is evident in the figure, the processing is carried out on one-dimensional (1-D) data obtained by projecting the two-dimension intensity distribution of an image onto the horizontal and vertical axis, and therefore it is quasi two dimensional processing. Such image data projection can be carried out easily using x, y accessible image sensors like BASIS [20], [21] or CMOS sensors [22]. The sensor output signals are capacitively coupled to a νMOS floating gate and accumulated along a single row or a single column, then being read out via νMOS source follower configuration. In this paper, the image acquisition and projection circuities were not fabricated. The COM-detection circuits were designed and fabricated assuming such projection data are available and provided by separate circuits.

The x-component of the location of COM X_G is calculated from the zeroth and the first moments of the projected intensity distribution as

$$X_G = \frac{\sum_{i=1}^{n} M_i X_i}{\sum_{i=1}^{n} M_i} \tag{1}$$

where X_i is the position on the abscissa and M_i the mass of the ith thread. The y-component Y_G is obtained similarly.

The circuit implementation of COM detection algorithm of Fig. 1 is illustrated in Fig. 2. Instead of calculating X_G according to (1), X_G was obtained by searching for X that satisfies the equation:

$$X \cdot \sum_{i=1}^{n} M_i = \sum_{i=1}^{n} M_i X_i. \tag{2}$$

In the input stage there are two complementary νMOS source followers composed of depletion-mode NMOS′ and PMOS′, which calculates $\sum M_i X_i$ and $\sum M_i$. The inputs $V_{\mathrm{IN}1}$–$V_{\mathrm{IN}n}$ are analog voltages representing the thread masses. They are capacitively coupled to the floating gate of the top source follower with coupling capacitance C_i proportional to the coordinate X_i, namely $C_i \propto i$. Here $i(i = 1, 2, \cdots, n)$ is the integer and n the total number of threads. The potential of the floating gate in the top source follower ϕ_{F1} is calculated as

$$\begin{aligned}\phi_{F1} &= \frac{C_1 V_{\mathrm{IN}1} + C_2 V_{\mathrm{IN}2} + \cdots + C_n V_{\mathrm{IN}n}}{C_1 + C_2 + \cdots + C_n} \\ &= \frac{V_{\mathrm{IN}1} + 2 \cdot V_{\mathrm{IN}2} + \cdots + n \cdot V_{\mathrm{IN}n}}{1 + 2 + \cdots + n}.\end{aligned} \tag{3}$$

In the general νMOS formula, like [8, eq. 1], for instance, C_0 representing the sum of the gate-oxide capacitances between the floating gate and the NMOS and PMOS channels appear in the denominator. However, this is not the case in (3). In the source follower configuration, the effect of C_0 can be neglected because the channel voltage is almost equal to the floating gate potential due to the source follower action of the circuit, and therefore, no charging occurs for C_0.

The result of the first moment calculation $\sum M_i X_i$ appears at the output of the top source follower as

$$V_1 = \frac{\sum_{i=1}^{n} M_i \cdot i}{\frac{n(n+1)}{2}}. \tag{4}$$

(Here, the voltage gain of the νMOS source follower is assumed as unity for simplicity, i.e., $V_1 = \phi_{F1}$. A more accurate discussion taking the actual nonunity gain into account is given in Section III.) The inputs are coupled to the bottom source follower with identical coupling capacitors, thus yielding the

zeroth moment $\sum M_i$ as

$$V_2 = \frac{\sum_{i=1}^{n} M_i}{n}. \tag{5}$$

These values are then transferred to the second-stage circuits via switches 2 and 3.

The second stage is composed of νMOS inverters that work as comparators. They compare the two quantities, $X \cdot \sum M_i$ and $\sum M_i X_i$, and turn on where the inequality $X \cdot \sum M_i > \sum M_i X_i$ holds. The COM coordinate X_G is obtained as the location where 0-to-1 transition occurs. The operation of the νMOS comparator is explained using Fig. 3(a) and (b).

In the reset cycle of a νMOS inverter, SW1 is closed and the floating gate is shorted to the output as shown in Fig. 3(a). As a result, the νMOS inverter is biased at the most sensitive point in the transition region, i.e., at the inversion threshold condition ($\phi_F = V^*_{\rm INV}$: the inversion threshold voltage of the νMOS inverter). At the same time, SW2 is closed and V_1 is fed to the input-gate 1 while the input gate 2 is grounded. Then SW1 is opened and the floating gate is made in the floating condition. After this reset cycle, the evaluation is started by closing SW3. As shown in Fig. 3(b), V_2 is fed to the input gate 2 while grounding the input gate 1. As the result of this operation, the floating gate potential ϕ_F of the νMOS inverter becomes

$$\phi_F = \frac{V_2 C_2 - V_1 C_1}{C_{\rm TOT}} + V^*_{\rm INV} \tag{6}$$

where $C_{\rm TOT} \equiv C_0 + C_1 + C_2$ (C_0: the capacitance between the floating gate and the ground). In the ith comparator the input capacitances C_1 and C_2 are designed as

$$C_1 : C_2 = 1 : \frac{2_i}{n+1}. \tag{7}$$

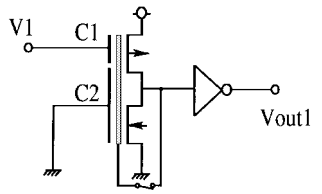
By substituting (4), (5), and (7) into (6), we obtain the condition for $\phi_F \geq V^*_{\rm INV}$ as

$$i \cdot \sum_{i=1}^{n} M_i \geq \sum_{i=1}^{n} M_i \cdot i. \tag{8}$$

Therefore the νMOS inverter works as a comparator and turns on when $X \cdot \sum M_i$ is greater than $\sum M_i X_i$. The center of mass is identified as the location where 0-to-1 transition occurs, which is detected by a simple logic circuit shown in Fig. 2.

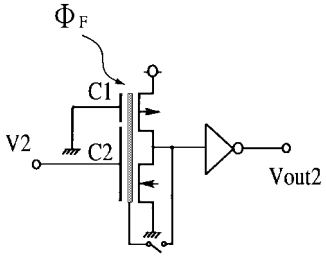
B. Experimental Results

A test circuit of a nine-input COM detector having the architecture of Fig. 2 was designed assuming a typical industry process, i.e., a 0.5 μm CMOS technology. The circuit was simulated by HSPICE and the results are demonstrated in Fig. 4(a). The parameters used for simulation are given in Table I. The test data given to the circuit are also shown in the figure which has the COM at position no. 4. The output was monitored at a negative logic node, and it is seen that the output corresponding to position no. 4 is low when ENABLE signal is high. Hence the circuit works as expected. The short drop in the output no. 6 is caused by the noise arising from



SW1 = "ON "
SW2 = "ON "

(a)



SW1 = "OFF "
SW3 = "ON "

(b)

Fig. 3. Operation of νMOS comparators in the second stage of the COM tracker: (a) reset cycle and (b) evaluation cycle.

TABLE I
SIMULATION PARAMETERS

	Inverter	Source follower
NMOS	W/L=1μm/0.5μm	W/L=2μm/0.5μm
	V_{TN}=1V	V_{TN}=-1V
	Well: 3×10^{16}cm^{-3}	
PMOS	W/L=2μm/0.5μm	W/L=4μm/0.5μm
	V_{TP}=-1V	V_{TP}=1V
	Substrate concentration : 1×10^{16}cm^{-3}	

Tox (Gate) =10nm, Tox (Poly) = 30nm

μ_N/μ_P=2

the switching transition of SW2 and SW3 (see Fig. 2). This results in the small variation in the floating gate potential of the νMOS inverter which is amplified by multiple inverter stages and appears at the output. The switching noise is sensitive to the biasing condition and happened to occur at the output no. 6 in this example. The similar noise effect occurring at the same locution is also observed in the experiment [Fig. 4(b)]. From the simulation, the COM detector designed using 0.5-μm design rule is capable of computing the COM location in less than 40 ns. The average current of this circuit is about 2 mA and dissipates the average power of 10 mW at 5 V power supply. The design optimization for minimizing the power dissipation was not conducted in the present work.

The characteristic feature of the present circuit is that the output signal is given by a digital flag appearing at the COM

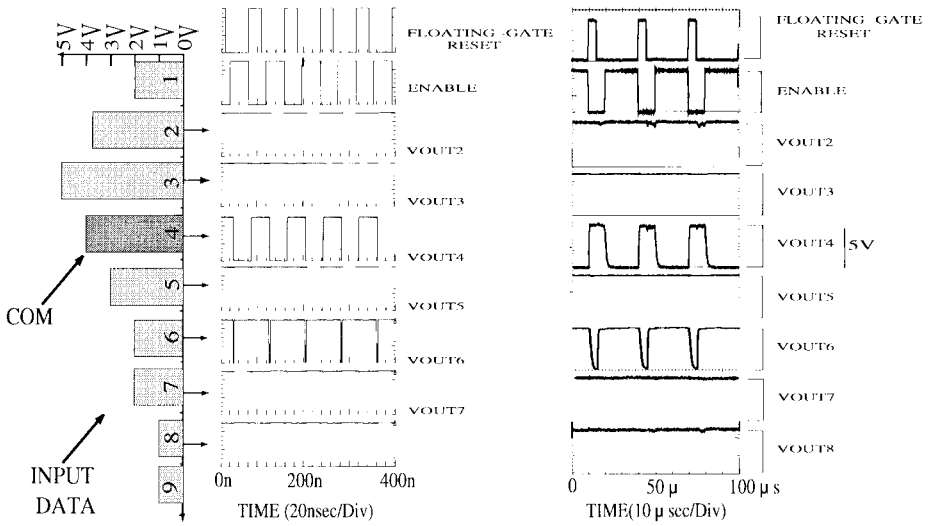


Fig. 4. Simulation and measurement results of 9-input COM detector circuit. (a) Simulation was carried out on a circuit designed in 0.5-μm CMOS technology. (b) Measurement was done on test circuits shown in Fig. 5 (3-μm CMOS). Slow operation of the measured data is due to the loading effect caused by direct probing without buffers.

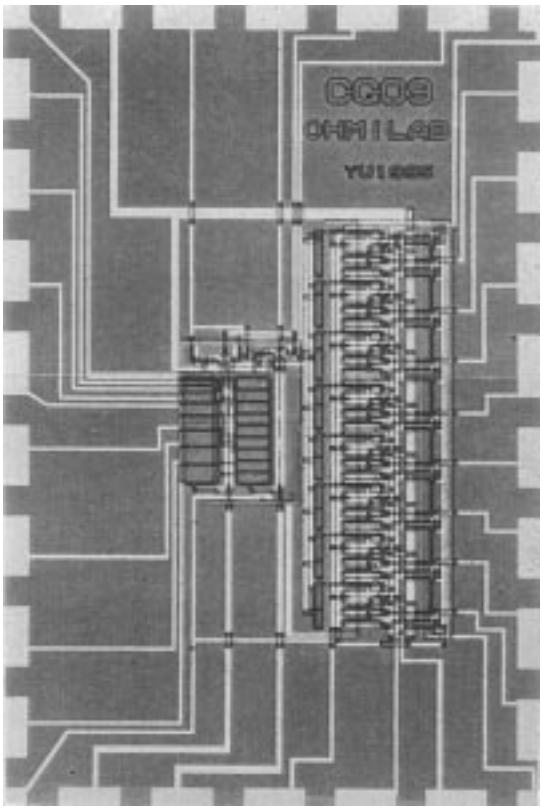


Fig. 5. Photomicrograph of the test circuit of nine-input COM detector fabricated by Tohoku University Standard 3-μm double-polysilicon CMOS process.

location while input signals are all analog. This provides a smooth interfacing to digital systems. This is in contrast to previous works [3], [23].

The center of gravity circuit presented in [23] is approximately the same both in the transistor count and the chip real estate. However, The circuit in [23] requires an additional A/D converter to obtain a digital output. This would approximately double the chip real estate. In addition the input signal can not take the rail-to-rail full voltage swing because the MOS saturation characteristics are utilized is the analog computation. In the present circuit, however, the rail-to-rail linearity in computation is guaranteed as discussed in the next section. The circuit proposed in [3] was implemented using discrete op amps. The transistor count estimated for silicon implementation is also approximately the same with that of the present work. The major part of the circuit of [3] is devoted for calculating $\sum M_i$ and $\sum M_i X_i$, which is performed by only two νMOS source followers in our work. The rest of our circuit is the νMOS comparator array utilized to present digital flags at output nodes.

As discussed above, the present paper provides a very simple hardware for COM detection with high speed performance and smooth interfacing to digital systems. The application of the circuit to fuzzy processor is now in progress [24]. The technology is intended to use is real-time intelligent robot control where minimizing the latency is of primary concern.

A photomicrograph of the test circuit of a nine-input COM detector is shown in Fig. 5. The test chip was designed and fabricated in a 3-μm double-polysilicon CMOS technology, a standard process run by students at Tohoku University. The measured wave forms are summarized in Fig. 4(b). The parameters of the fabricated test circuit are shown in Table II. The measurement results closely reproduce the behavior obtained by simulation. The large delay seen in the results of the fabricated test circuit is due to the loading effect because the output node was directly probed without buffer circuitries.

III. Analysis of Circuit Operation Accuracy

As shown above, the operation of the COM detector has been verified by simulation as well as by experimental results. However, the circuit has a tendency to produce incorrect results if the COM is located near the edges. In Fig. 6, we show the simulation results for a nine-input COM detector with

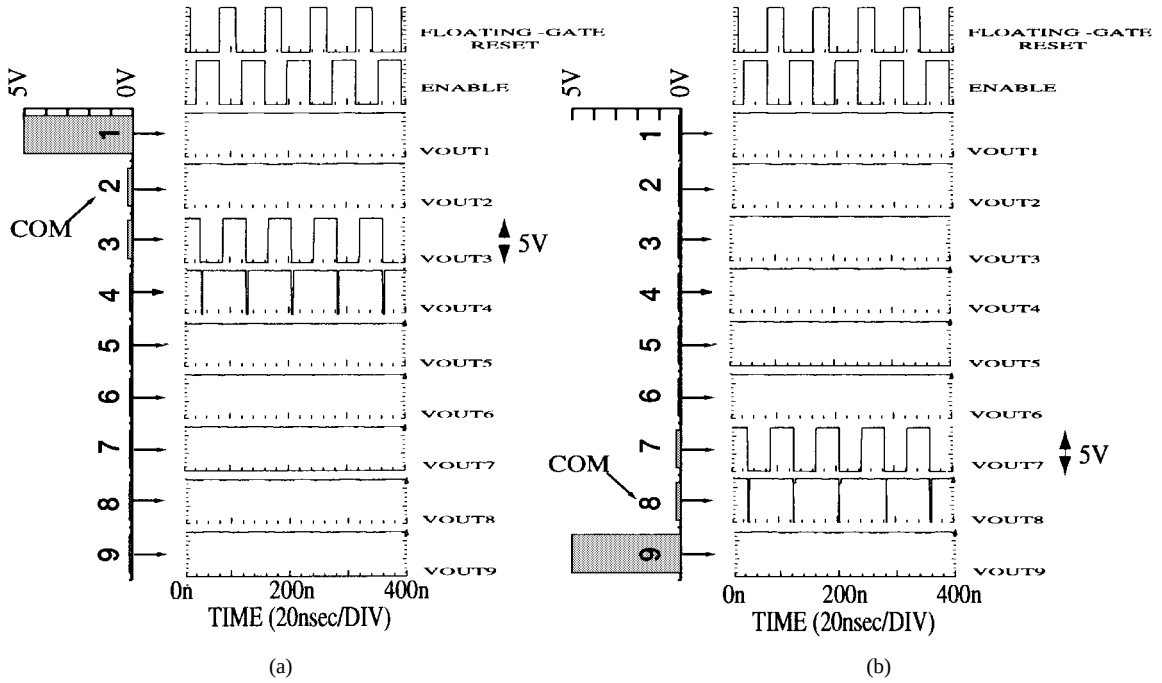


Fig. 6. Simulation results for nine-input COM detector. The COM was placed at position 2 (left) and position 8 (right).

TABLE II
DEVICE/PROCESS PARAMETERS OF FABRICATED TEST CIRCUITS

	Inverter	Source follower
NMOS	W/L=6μm/3μm	W/L=12μm/6μm
	V_{TN}=1V	V_{TN}=-1V
	Well: $3\times10^{15}cm^{-3}$	
PMOS	W/L=12μm/3μm	W/L=24μm/6μm
	V_{TP}=-1V	V_{TP}=1V
	Substrate concentration : $1\times10^{15}cm^{-3}$	

Tox (Gate) = 500Å, Tox (Poly) = 1500Å

μ_N/μ_P=2

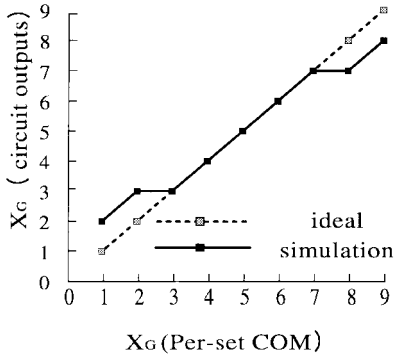


Fig. 7. Relationship between the correct (pre-set) COM and the COM-tracker output (HSPICE simulation).

the COM situated at positions 2 and 8. However, as shown in the figure, the output is low at positions 3 and 7 for the real COM locations at positions 2 and 8, respectively. In order to investigate this phenomenon, the input data are given in a δ-function-like form. Namely, we set the input corresponding to the COM high at 5 V and all other inputs low at 0 V. Then the COM position was changed from 1 through 9 and the output of the COM detector was observed. The relation between the correct (pre-set) COM and the output of the COM detector is shown in Fig. 7. It is seen that errors occur at positions 1–2 and 8–9. The reason for this can be found in the I/O characteristic of the source follower used in the COM detector.

Fig. 8 shows the I/O characteristic of the νMOS source follower used in the COM detector. The same V_{IN} is given to all input terminals simultaneously. The abscissa represents the input to the νMOS source follower (V_{IN}) while the ordinate represents the output. The solid line shows the characteristic of an ideal source follower and the broken line is the simulated result. If m is the slope of the broken line and the offset of the source follower is D, the simulated result can be approximated as

$$V_{\text{out}} = D + mV_{\text{in}}. \tag{9}$$

Using this relation, the floating gate potential for the comparator becomes

$$\phi_F = \frac{(C_2 - C_1)D + m(V_2C_2 - V_1C_1)}{C_{\text{TOT}}} + V^*_{\text{INV}}. \tag{10}$$

In order for the comparator to work correctly, the comparator output must be determined only by the sign of $(V_2C_2 - V_1C_1)$. As seen in the above equation, the output is now influenced by the offset D. When $(C_2 - C_1)$ is small the effect of D is negligible. However, when $(C_2 - C_1)$ is large, the effect of D can no longer be neglected and leads to an error. This happens when the COM is located near the edges.

The problem caused by the source follower offset can be overcome by the circuit scheme shown in Fig. 9. The νMOS comparator shown in Fig. 9(a) is basically the same as that mentioned previously in Fig. 3 except that the inputs are

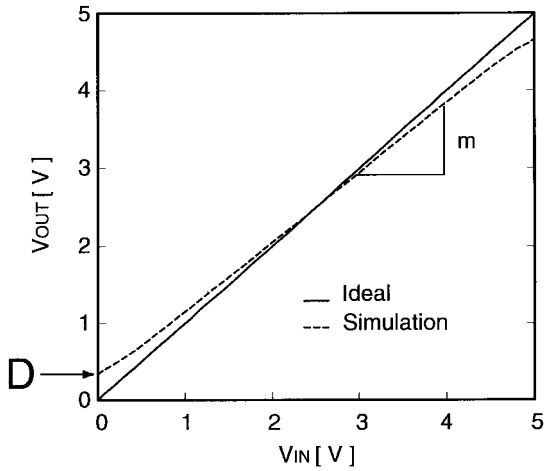
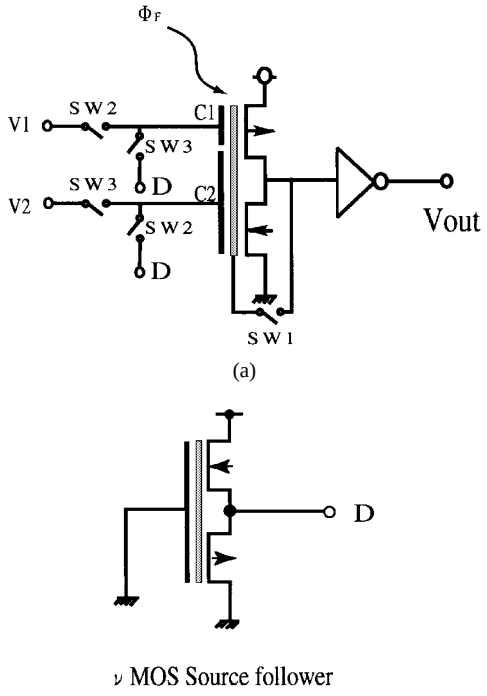


Fig. 8. I/O characteristic of νMOS source follower used in the COM detector. The same V_{IN} is given to all input terminals simultaneously.



(a)

(b)

Fig. 9. New circuit scheme to cancel the offset of input-stage νMOS source followers. (a) Modification in νMOS comparator where the ground terminal was replaced by a constant voltage source D. (b) Circuit producing the constant voltage D equal to the source-follower offset.

connected by switches, not to the earth, but to a constant voltage source having the analog value equal to the source follower offset D. A precise value of the analog voltage D can be generated quite easily using the circuit shown in Fig. 9(b). This is a νMOS source follower having identical dimensions to those of input-stage νMOS source followers. All input terminals are grounded, thus producing an identical offset voltage D. The floating gate potential of the comparator then becomes

$$\phi_F = \frac{m(V_2C_2 - V_1C_1)}{C_{\mathrm{TOT}}} + V^*_{\mathrm{INV}}. \tag{11}$$

D does not appear in the equation. Hence the influence of the source follower offset D has been eliminated effectively using the above scheme.

The simulation results for a COM detector using the above mentioned scheme to cancel the source follower offset is shown in Fig. 10. The pre-set COM's are at positions 2 and 8. As shown in the figure, the outputs of the COM detector are also at 2 and 8. Hence the cancellation scheme works correctly.

In order to investigate the effectiveness of the proposed cancellation scheme, we again set the input corresponding to the COM high at 5 V (all other inputs low at 0 V) and changed the position of the COM from 1 through 9. The relation between the correct (pre-set) COM and the output of the COM detector is shown in Fig. 11. The circuit yields a correct response for any location of the COM.

IV. Multiple-Stage COM Tracker Circuit

In the circuit of Fig. 2, the coordinate index X_i is represented by the magnitude of the coupling capacitor of the νMOS. Therefore, the computation accuracy will be degraded when the number of inputs increases. In order to resolve the problem, a multiple-staged architecture has been developed. For the multiple-staged architecture, the input signals are divided into n sub-blocks, each containing s input signals, as shown in Fig. 12. We can write the location of the global COM X_G as

$$X_G = \frac{\sum_{j=1}^{n} M_j X_j}{\sum_{j=1}^{n} M_j} \tag{12}$$

where X_j is the location of the local COM in the jth block, M_j is the lumped mass of the block. If $s \cdot (j-1)$ is taken as the origin of the jth block, and ΔX_j is the location of the local COM of the jth block as measured from the origin, then X_j is expressed as

$$X_j = s(j-1) + \Delta X_j. \tag{13}$$

By substitution (13) into (12), we obtain the global COM X_G as

$$\begin{aligned} X_G &= \frac{\sum_{j=1}^{n} M_j[s(j-1) + \Delta X_j]}{\sum_{j=1}^{n} M_j} \\ &= \frac{S\sum_{j=1}^{n} M_j(j-1)}{\sum_{j=1}^{n} M_j} + \frac{\sum_{j=1}^{n} M_j \Delta X_j}{\sum_{j=1}^{n} M_j} \\ &= X'_G + \Delta X_G \end{aligned} \tag{14}$$

where X'_G is the location of the block in which the global COM exists, ΔX_G is the position of the global COM in the local coordinate in the block. Therefore, if we know the value

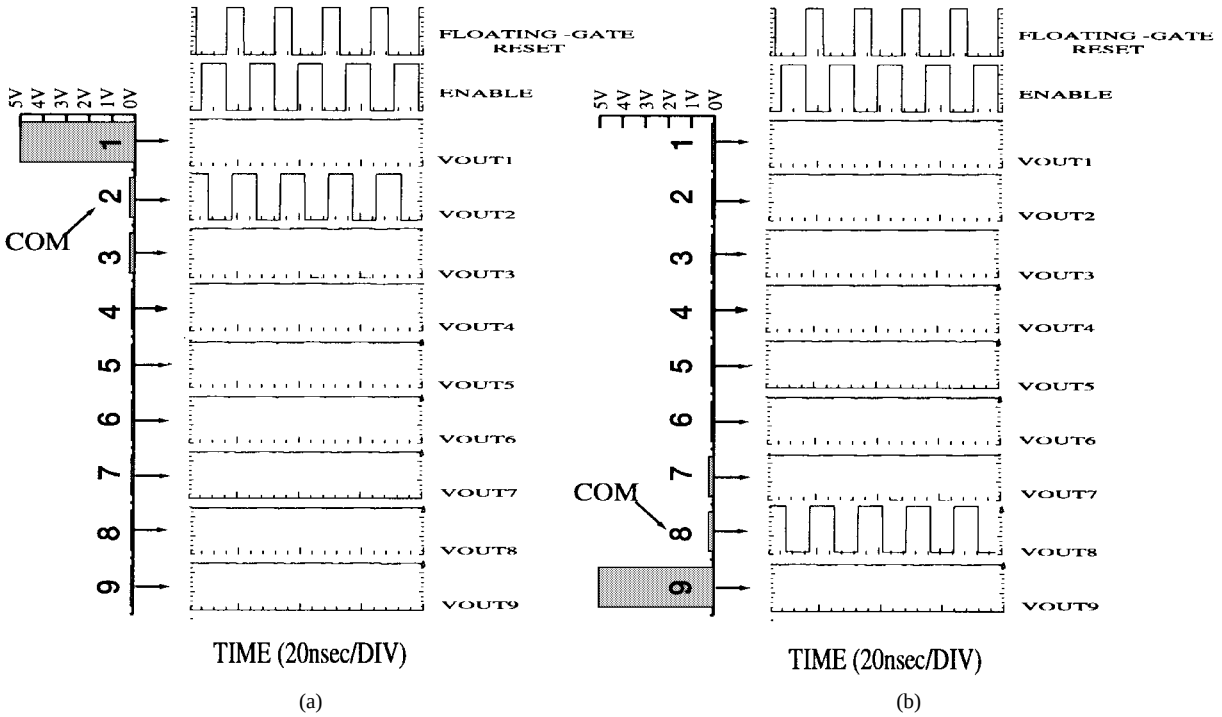


Fig. 10. Simulation results for COM detector employing the offset cancellation scheme.

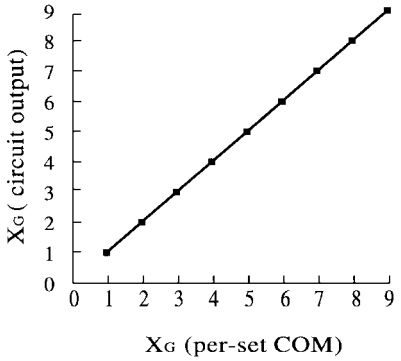


Fig. 11. Relationship between correct (pre-set) center of mass and COM detector output when the offset cancellation scheme was employed.

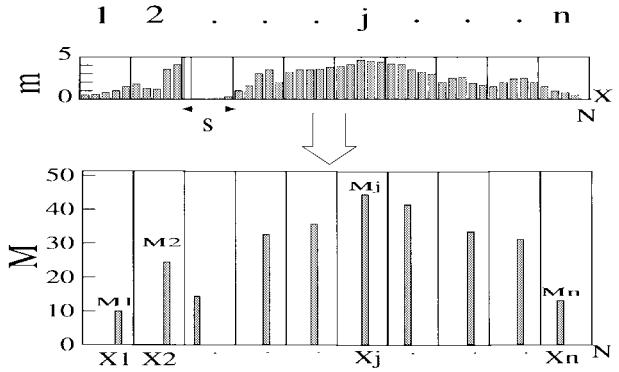


Fig. 12. N input signals are grouped into n sub-blocks each containing s input signals.

of X'_G and ΔX_G, then the global COM location X_G can be obtained. The problem of finding X'_G is exactly the same as locating the COM described in Section II. Then X'_G can be determined by the same COM detector circuit shown in Fig. 2 which is called "global location detector."

The block diagram for a multiple-staged COM detector is shown in Fig. 13. In order to determine ΔX_G, two new circuit blocks A and B are included as shown in the figure. The circuit block A computes $M_j \times \Delta X_j$ using a νMOS source follower where ΔX_j is represented by the magnitude of the input capacitance. The voltage representing the lumped mass M_j is applied to one of the n input terminals of the νMOS source follower which is selected by the location of the local COM ΔX_j.

The circuit block B, which we call "deviation detector," has a similar architecture as that of the COM detector shown in Fig. 2. The only differences are that the top source follower has all identical input capacitances and that $M_j \times \Delta X_j$ and

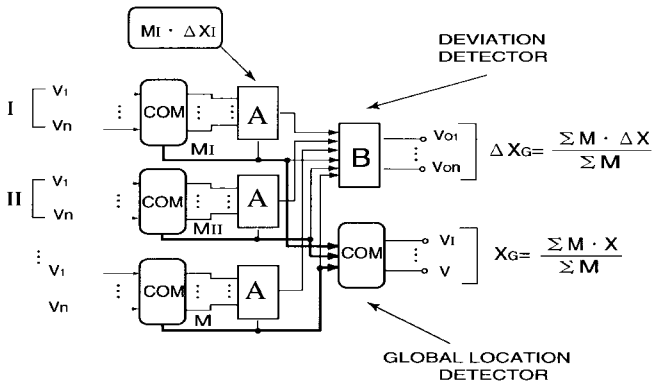


Fig. 13. Block diagram of multiple-stage COM detector.

M_j $(j = 1, 2, \cdots, n)$ are given to the top source follower inputs and the bottom source follower inputs, respectively. The circuit indicates the location of the global COM in the local

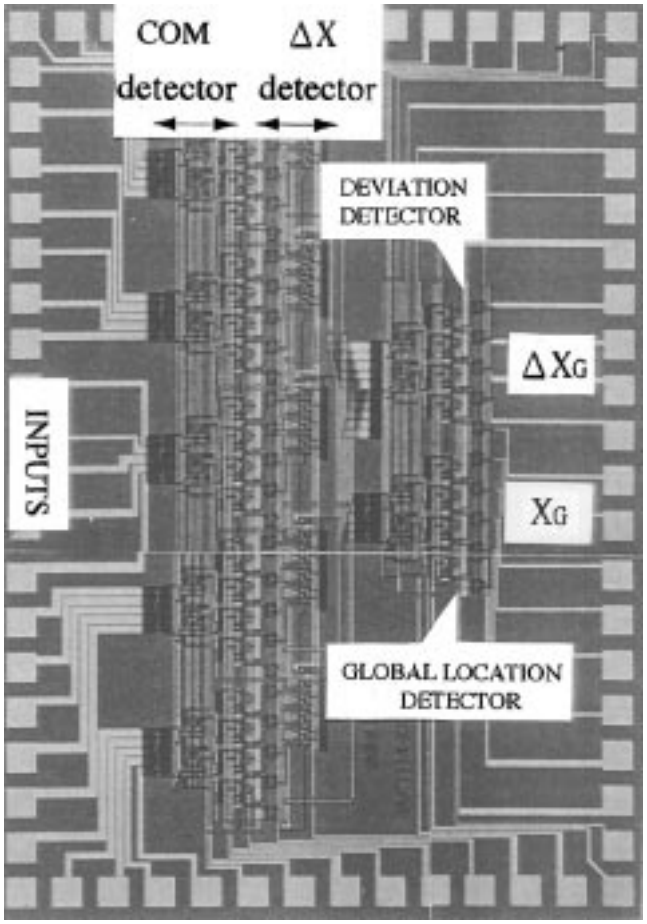


Fig. 14. Photomicrograph of the test circuit of two-staged COM detector for 25 (5×5) inputs.

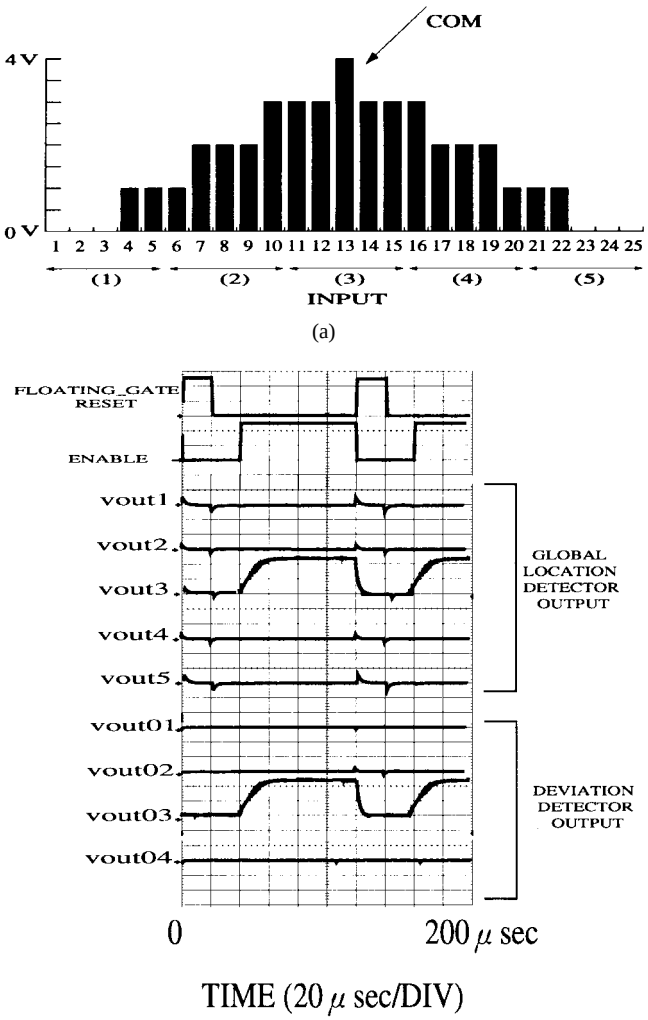


Fig. 15. Measurement results of the test circuit shown in Fig. 14.

coordinate of the block in which the global COM exist. The location of the COM in $s \times m$ input signals is thus obtained as $X'_G + \Delta X_G$.

The test circuit of a two-staged COM detector for 25 inputs is shown in Fig. 14. As is seen in the measurement results in Fig. 15, the location of the COM is indicated by high output voltages in the global location detector and the deviation detector as $X'_G = 3$ and $\Delta X_G = 3$, respectively. (Positive logic nodes were monitored.) It should be noted that the computation for detecting the COM location is carried out in the analog regime, but the output is given by the flag appearing at an appropriate node. Therefore, the output is given by a digital code. This is one the most important features of the νMOS hardware computing scheme that allows a very smooth interfacing to digital systems.

V. Conclusions

A new architecture for a center of mass (COM) detection circuit using neuron MOS circuit technology has been described. It is shown by HSPICE simulation for test COM circuits designed in a 0.5-μm CMOS technology that the νMOS COM tracker can detect the location of COM well within 40 ns By employing a new source-follower-offset cancellation scheme in the νMOS comparators as well as by introducing a multistaged COM tracker architecture, a high-accuracy detection of COM for a large number of pixel data has been established. The parallel computing architecture by νMOS circuits and the quasi 2-D algorithm has made it possible to perform COM detection very fast using a very simple hardware. One of the most important features of the νMOS circuit technology is that a νMOS system receives analog input signals without A/D conversion and produces binary codes as outputs, thereby providing a very smooth interfacing between the analog real world and the digital computer world.

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