



# Multiple-Input Neuron MOS Operational Amplifier for Voltage-Mode Multivalued Full Adders

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TABLE VII  
COMPARISON OF DYNAMIC POWER DISSIPATION

No. of Stages(N)	No. of Taps(M)	P <sub>serial</sub> (mw)	P <sub>lowy</sub> (mw)	P <sub>ours</sub> (mw)	% Improve over serial
2	2	0.0341	0.1151	0.1151	-237.36
3	2	0.0469	0.1151	0.1151	-145.60
4	2	0.0596	0.1151	0.1151	-93.08
5	2	0.0724	0.1151	0.1151	-59.07
6	2	0.0851	0.1151	0.1151	-35.24
7	4	0.1151	0.1624	0.1151	0.00
8	4	0.1279	0.1624	0.1151	9.97
9	2	0.1234	0.1151	0.1151	6.69
10	2	0.1361	0.1151	0.1151	15.43
11	2	0.1489	0.1151	0.1151	22.67
12	4	0.1789	0.1624	0.1151	35.64
13	4	0.1916	0.1624	0.1151	39.92
14	4	0.2044	0.1624	0.1151	43.67
15	2	0.1999	0.1151	0.1151	42.40
16	4	0.2299	0.1624	0.1151	49.92
17	2	0.2254	0.1151	0.1151	48.92
18	2	0.2381	0.1151	0.1151	51.65
19	4	0.2681	0.1624	0.1151	57.06
20	2	0.2636	0.1151	0.1151	56.33
21	2	0.2764	0.1151	0.1151	58.34
22	2	0.2891	0.1151	0.1151	60.18
23	2	0.3019	0.1151	0.1151	61.86
24	4	0.3319	0.1624	0.1151	65.31
25	2	0.3274	0.1151	0.1151	64.83
26	4	0.3574	0.1624	0.1151	67.79
27	4	0.3701	0.1624	0.1151	68.90
28	2	0.3656	0.1151	0.1151	68.51

- 1) approximately three times the increase in the number of switch requirements;
- 2) changing one-clock flip-flops to two-clock flip-flops;
- 3) doubling the number of XOR gate requirements.

This will result in increased overhead when implementing high-order polynomials. Using the proposed polynomials to implement the double output realization, the number of switch requirements can be reduced.

#### IV. CONCLUSION

A previous paper by Lowy defined a family of low-power LFSR's based on a switch minimization procedure and presented an excellent method to increase the throughput of the sequence generator. This paper, which was motivated by Lowy's paper, has pointed out the following advantages of using nonprimitive polynomials with two taps in implementing low power LFSRs: 1) the number of switch requirements is reduced from the order of  $M + N$  to the order of  $N$  and 2) the average percentage of distinct test patterns is around 91% for  $2^{N+2}$  cycles. Our proposed polynomial works fairly well for

even-order polynomials and it works well for most of the seeds. A trial and testing is required for odd-order polynomials to get a good seed that generates the highest percentage of distinct patterns. Our developed software, written in C, is capable of performing this trial and testing job.

For larger sized LFSR's ( $N > 8$ ), our structure consumes much less power than the conventional LFSR's. The percentage of power improvement ranges up to 68.51% for  $N = 28$ , which is indeed an encouraging figure.

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### Multiple-Input Neuron MOS Operational Amplifier for Voltage-Mode Multivalued Full Adders

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**Abstract**—A CMOS operational amplifier employing the multiple-input-terminal transistor called neuron MOSFET (or  $\nu$ MOS) as pair transistors has been developed. The circuit can perform a variety of analog voltage summation/subtraction operations in a very simple circuitry. The self-offset-cancellation capability has been implemented by a clocked  $\nu$ MOS technique. As a result, high-accuracy voltage-mode signed-digit computation has become possible. The  $\nu$ MOS operational amplifier has been applied to build a carry-propagation-free multivalued full adder circuit based on the radix-4 seven-valued signed-digit number system. The circuit operation has been verified by test circuits fabricated by Tohoku University standard double-polysilicon CMOS process with a 3- $\mu$ m rule.

**Index Terms**—Carry-propagation-free adders, multiple-valued logic, neuron MOS.

#### I. INTRODUCTION

Multivalued logic is now drawing considerable attention as a promising candidate for building future integrated circuits [1]–[4]. Reduction in the number of interconnects, increased memory capacity [5] per cell, and enhanced functionality per unit circuit are the attractive features. The carry-propagation-free addition by employing

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a multivalued redundant signed-digit (SD) number system [6] is one of the most attractive features in enhancing the computational power of a system.

Multiply and accumulate is the most basic operation required in various signal processing algorithms, and enhancing its operational speed is highly essential. However, the propagation of ripple carries in conventional full adder circuitry is severely limiting the speed performance. The problem can be resolved by carry-look-ahead circuitries. However, the cost must be paid for increased circuit complexity. In contrast, multivalued addition algorithms using a redundant SD number system can give the opportunity to build carry-propagation-free full adders [6]. The radix-4 SD number system was first applied to build a  $32 \times 32$ -bit multiplier using multivalued current-mode circuitry [7], demonstrating an enhanced computational power with reduced transistor counts. The redundant binary (radix-2 SD system) was utilized in [8] and [9] with multivalued circuitry and in [10] with binary logic circuitry. A multiple-input-terminal device, neuron MOSFET ( $\nu$ MOS) [11], has been successfully applied to multivalued logic circuits [12], [13]. However, the addition of two voltage signals produces not a linear sum but a weighted average of the two due to the capacitance coupling principle of the  $\nu$ MOS operation. This is not very suited to build SD adders.

The purpose of this paper is to present a new architecture CMOS operational amplifier (op. amp.) designed for the first time using a pair of  $\nu$ MOS transistors in the input stage. Multiple input terminals are provided at both inverting and noninverting input terminals, thereby enabling linear voltage addition without voltage gain loss. A self-offset-cancellation operation has been introduced based on the clocked  $\nu$ MOS circuitry [14] in order to guarantee high accuracy analog computation. The application of the  $\nu$ MOS operational amplifier to multivalued SD full adders has been explored and is described in this article.

## II. NEURON MOS OPERATIONAL AMPLIFIER

A  $\nu$ MOS [11] is a regular MOS transistor except its gate electrode is made electrically floating and is capacitively coupled to multiple input terminals. Linear weighted summation of input voltage signals is carried out on the floating gate as a result of charge sharing among multiple capacitors and the transistor action is controlled by the weighted sum of input signals. When the weighted sum controls the on/off actions of the MOS, the device emulates the mathematical model of a neuron [15], thus bearing the name. When a  $\nu$ MOS is utilized in a source follower configuration, the result of summation can be read out as a voltage signal [11]. However, the result is the weighted average of multiple voltage signals and the linear addition cannot be performed. For this reason, we merged the  $\nu$ MOS technology into an operational amplifier circuitry, thus enabling the linear addition of multiple voltage signals.

The circuit diagram of a  $\nu$ MOS op. amp. is given in Fig. 1(a).  $\nu$ M1 and  $\nu$ M2 represent  $\nu$ MOS transistors and are enhancement-mode NMOS. If the floating gates of the  $\nu$ MOS ( $\nu$ M1 and  $\nu$ M2) are regarded as regular MOS gates, the circuit is a well-known CMOS op. amp. composed of a differential  $V$ - $I$  converter amplifier at the input stage and an  $I$ - $V$  converter amplifier in the second stage. An NMOS current sink is connected to the common source of the  $\nu$ MOS pair and two PMOS current sources are connected to their drains as load elements. They provide identical sink/source currents of  $I_0$ , thus making the total output current constant, namely  $I^+ + I^- = I_0$ .

When  $\phi_F^+ = \phi_F^-$ , the  $V$ - $I$  converter sources the bias current of  $I^+ = I^- = I_0/2$  to the current mirror load consisting of NMOS M3 and M4. Here, M3 and M4 are sized so that their drain voltages V3 and V4 are biased to  $V_{DD}/2$  under the bias current. PMOS M5 and M6 serve as cascode load, thus minimizing the drain voltage

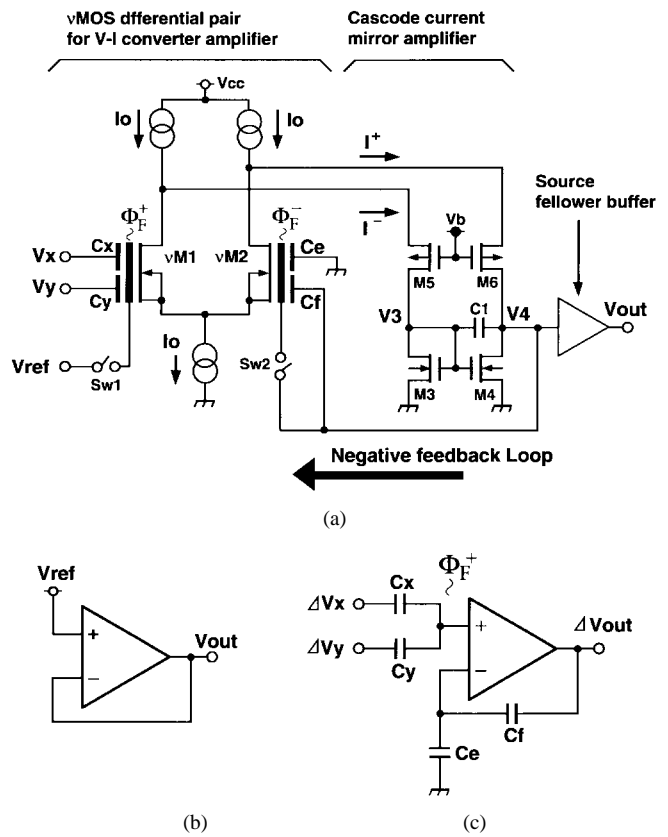


Fig. 1. (a) Circuit diagram of  $\nu$ MOS op. amp. (b) Equivalent diagram of  $\nu$ MOS op. amp. in reset mode. (c) Equivalent diagram in operation mode.

variation in  $\nu$  M1 and  $\nu$  M2. The difference in the voltages  $\phi_F^+$  and  $\phi_F^-$  is amplified with a large voltage gain and appears at node V4. The new features of the circuit have been created by the capacitance coupling of the  $\nu$ MOS input gates. This is explained by equivalent representations given in Fig. 1(b) and (c).

In the reset mode with SW1 and SW2 being turned on, the circuit becomes a voltage follower [Fig. 1(b)], and both  $\phi_F^+$  and  $\phi_F^-$  are reset to  $V_{ref}$ . This is the so-called imaginary short. At this moment, the inputs  $V_x$  and  $V_y$  are also biased to  $V_{ref}$ .  $V_{ref}$  was set at  $V_{DD}/2$  in the present application. In the operation mode, SW1 and SW2 are turned off, and signals are applied to the  $V_x$  and  $V_y$  terminals [Fig. 1(c)]. Then the circuit becomes a noninverting amplifier and amplifies  $\Delta\phi_F^+ = \phi_F^+ - V_{DD}/2$  by the voltage gain of  $(1 + C_e/C_f)$ . By setting  $C_x = C_y$ , we obtain  $\Delta\phi_F^+ = (\Delta V_x + \Delta V_y)/2$ . If we choose  $C_e = C_f$ , the voltage gain becomes 2 and  $\Delta V_{out} = \Delta V_x + \Delta V_y$ . Here,  $\Delta\phi_F^+$ ,  $\Delta V_{out}$ ,  $\Delta V_x$ , and  $\Delta V_y$  all represent the deviations from the reference voltage  $V_{ref}(= V_{DD}/2)$ .

In the above explanation, we assumed for simplicity that  $C_0$ , the parasitic coupling capacitance between the floating gate and the substrate (p-well), is negligibly small as compared to input capacitances, i.e.,  $C_x = C_y \gg C_0$ . However, this is not essential. In the case of nonnegligible  $C_0$ , it becomes  $\Delta\phi_F^+ = \gamma(\Delta V_x + \Delta V_y)$  where  $\gamma = (C_x + C_y)/(C_0 + C_x + C_y)$ . We can obtain  $\Delta V_{out} = \Delta V_x + \Delta V_y$  by setting  $C_e/C_f = 1/\gamma - 1$ . The main component of  $C_0$  is the MOS gate capacitance and is well-approximated by the gate oxide capacitance when the MOS is turned on. Therefore, it is regarded as a constant and is well taken into account in the design stage. In the circuit of Fig. 4, however, the effect of the parasitic capacitance  $C_0$  was made negligibly small by taking  $\nu = 0.97$  and the ratio was set at  $C_e/C_f = 1$ .

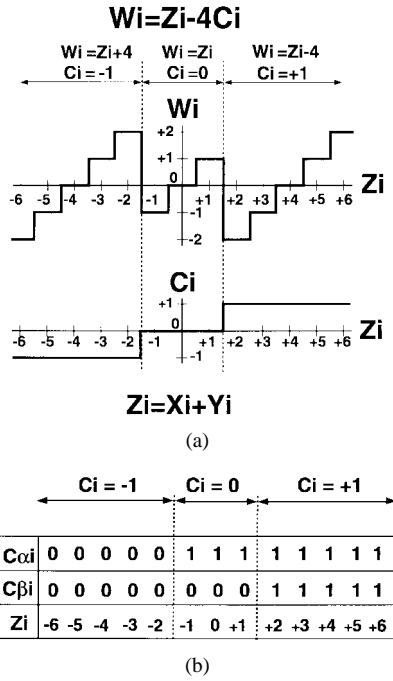


Fig. 2. Illustration of radix-4 SD addition algorithm. (a) Algorithm for radix-4 SD redundant full adder. (b) Two-bit carry signals,  $C_{\alpha i}$  and  $C_{\beta i}$ , representing carry  $C_i$ .

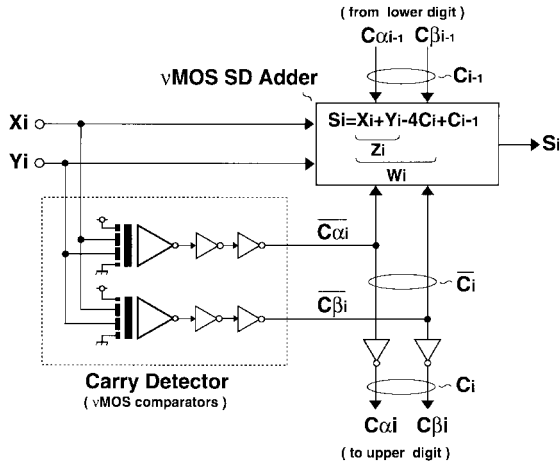


Fig. 3. Block diagram of  $\nu$ MOS SD full adder circuit.

In this circuit, a well-known auto zeroing technique in comparators has been employed and merged into the  $\nu$ MOS differential pair to achieve a self-offset-cancellation capability. Since only the voltage difference from  $V_{ref}$  is amplified after the offset cancellation, the offset is not amplified. Only a small offset error remaining in the reset cycle appears in the final summation results.

It should be noted here that this offset error does not propagate to the following stage. This is because the following stage  $\nu$ MOS op. amp. circuit also amplifies only the difference signal. This is important for carrying out multivalued logic operations in multiple cascaded stages because the offset error neither propagates nor accumulates. Although the offset error is eliminated by the self-offset-cancellation operation, the gain error cannot be canceled and propagates and accumulates from stage to stage. However, the accurate gain adjustment is rather easy in the op. amp. circuitry because the gain is determined solely by the capacitance ratio. In contrast, the accurate matching of pair transistors characteristics for eliminating offset is not so easy. We believe this is the most important

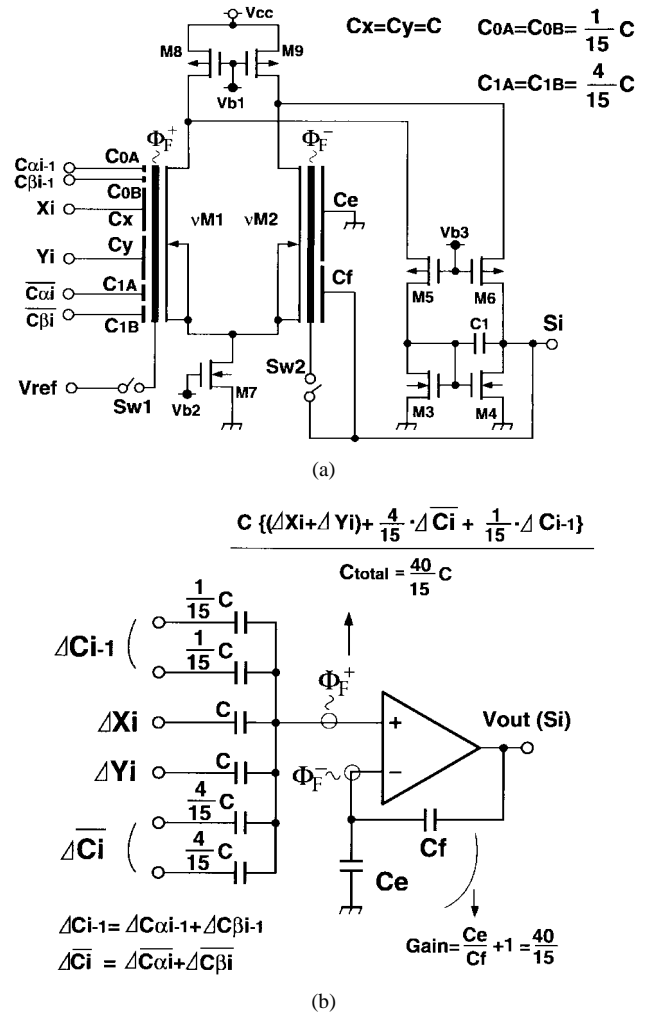


Fig. 4. (a) Circuit diagram of six-input  $\nu$ MOS op. amp. designed for SD full adder and (b) its equivalent representation.

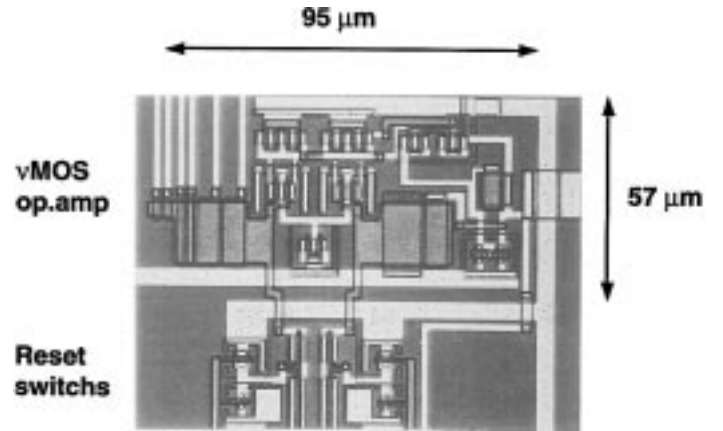


Fig. 5. Photomicrograph of a test circuit of  $\nu$ MOS SD adder fabricated by  $3\text{-}\mu\text{m}$  double-poly CMOS process (Tohoku University Lab. standard processing).

feature of the  $\nu$ MOS op. amp. in the application to multivalued logic gates handling large radix numbers.

### III. APPLICATION TO CARRY-PROPAGATION-FREE MULTIPLE-VALUED FULL ADDER

The algorithm for the radix-4 SD redundant full adder is illustrated in Fig. 2(a). Two input variables  $X_i$  and  $Y_i$ , taking values between

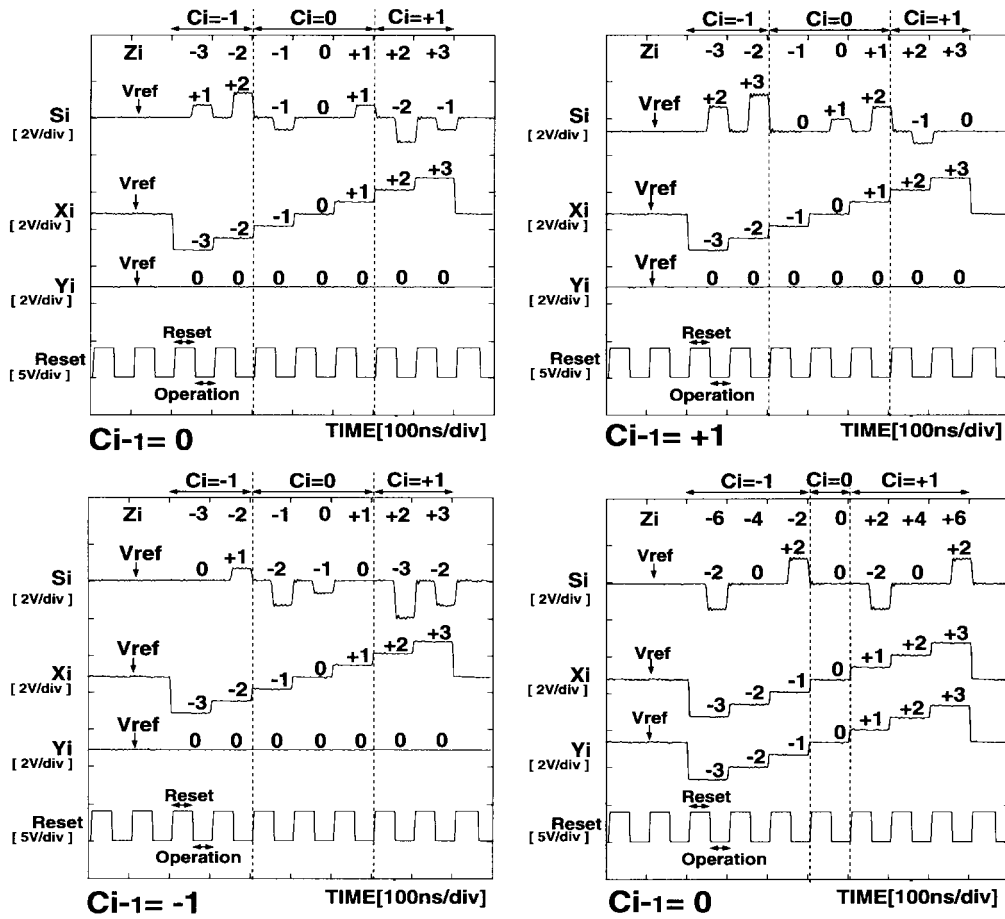


Fig. 6. Measured waveform of  $\nu$ MOS op. amp. SD adder.

$\pm 3$ , are summed up, yielding the linear sum  $Z_i$  between  $\pm 6$ . The intermediate sum  $W_i$  is generated either by subtracting 4 from  $Z_i$  or adding 4 to  $Z_i$ , thus limiting the range of  $W_i$  to within  $\pm 2$ . At the same time, the carry  $C_i$  of  $\pm 1$  is generated and sent to the upper digit. As a result, the sum of  $W_i + C_{i-1}$  never exceeds the range of  $\pm 3$ , and therefore, carries do not propagate beyond the neighbor. In our  $\nu$ MOS implementation, the carry  $\pm 1$  is represented by 2-bit binary signals,  $C_{\alpha i}$  and  $C_{\beta i}$ , as shown in Fig. 2(b).

Fig. 3 illustrates the organization of a  $\nu$ MOS full adder by a block diagram. The  $\nu$ MOS SD adder consists of a six-input  $\nu$ MOS op. amp. while the carry detector consists of two  $\nu$ MOS comparators. The  $\nu$ MOS comparator consists of a single stage  $\nu$ MOS inverter followed by two stages of regular CMOS inverters as shown in the figure.

The circuit diagram for the six-input  $\nu$ MOS op. amp. designed for the SD adder is illustrated in Fig. 4(a). The final sum  $S_i$  is calculated as

$$S_i = X_i + Y_i - 4C_i + C_{i-1}. \quad (1)$$

$X_i$  and  $Y_i$  are two SD numbers to be added, taking values from  $-3$  to  $+3$ . A voltage step of  $V_{DD}/15$  is assigned to the separation between logic levels. The variable 0 is represented by the DC level of  $V_{DD}/2$ .  $X_i$  and  $Y_i$  are both coupled to the  $\nu$ MOS floating gate via  $C_x$  and  $C_y$  with an identical coupling capacitance of  $C$ . The carry signals,  $C_{\alpha i-1}$  and  $C_{\beta i-1}$ , are binary signals representing the carry from the lower digit and need to be added to  $S_i$  with weights equivalent to the unit of the logic level. Therefore, the coupling capacitors are made  $1/15$  of  $C$ .  $C_{\alpha i}$  and  $C_{\beta i}$  are the carry signals representing  $C_i$  and must be subtracted from  $S_i$  with a weighting factor of four. Therefore, the coupling capacitors are made four times larger than

those for  $C_{\alpha i-1}$  and  $C_{\beta i-1}$  and inverted binary signals are coupled to the floating gate. The total of six input coupling capacitors was designed as approximately equal to 700 fF which is much larger than the gate oxide capacitance of  $\nu$ MOS1 ( $\nu$  M1) of 25 fF.

The unit logic level of  $V_{DD}/15$  is determined in the following manner. Since the maximum logic level of  $S_i$  can be 13 before reducing  $C_i$ , at least 13 voltage levels need to be handled on the floating gate. Adding two more levels as margins to the voltage rails requires  $V_{DD}$  to be divided into 15 unit logic levels. After  $C_i$  reduction,  $S_i$  takes a voltage between 1.5–3.5 V for 5 V supply where excellent linearity of the  $\nu$ MOS op. amp. in the noninverting amplifier configuration is preserved.

The  $\nu$ MOS op. amp. in the operation mode is represented in Fig. 4(b) as an equivalent circuit. All input variables are difference signals from  $V_{ref}(=V_{DD}/2)$  and  $\Delta\phi_F^+$  are determined as

$$\Delta\phi_F^+ = \frac{C \left[ (\Delta X_i + \Delta Y_i) + \frac{4}{15} \Delta \bar{C}_i + \frac{1}{15} \Delta C_{i-1} \right]}{\frac{40}{15} C}. \quad (2)$$

Both  $\Delta \bar{C}_i$  and  $\Delta C_{i-1}$  take the value of  $-V_{DD}$ , 0 or  $V_{DD}$ . If we determine the ratio of the feedback capacitances  $C_e/C_f$  as  $1 + C_e/C_f = 40/15$ , it cancels the factor in the denominator of (2) and we obtain the final sum  $S_i$  as in (1). In this manner the SD adder is implemented by a single multi-input  $\nu$ MOS op. amp.

A photomicrograph of a test circuit of the  $\nu$ MOS op. amp. SD adder is shown in Fig. 5. The circuit was fabricated by Tohoku University standard double-polysilicon CMOS process with a 3- $\mu$ m layout rule. The measured results are demonstrated in Fig. 6 for three

different values of the carry from the lower digit, i.e.,  $C_{i-1} = +1$ , 0 and  $-1$ . The circuit behaves exactly as expected.

The circuit performance was compared in terms of speed and power among various implementations: a radix-4 seven-valued SD full adder by  $\nu$ MOS op. amp., that by MV current-mode circuitry [7], and the binary logic implementation of a radix-4 six-valued SD full adder composed of two radix-2 three-valued SD full adders [10]. HSPICE simulation was carried out on each circuit assuming a  $0.8\text{-}\mu\text{m}$  CMOS process. The delay times were 1.7, 2.3, and 1.6 ns, and power dissipation was 1.7, 2.51, and 3.26 mW, for  $\nu$ MOS, current mode, and binary implementations, respectively. The power-delay product is the smallest for the  $\nu$ MOS implementation. The transistor counts were 46, 53, and 96, respectively. Again,  $\nu$ MOS yields the smallest number, but it needs 12 capacitors. The area of  $\nu$ MOS implementation is largely depends on the coupling capacitor design as shown in Fig. 5.

#### IV. CONCLUSIONS

An analog voltage summation circuitry has been developed using  $\nu$ MOS concepts in an operational amplifier configuration. As a result, a carry-propagation-free multivalued full adder circuit based on the radix-4 seven-valued signed-digit number system has been implemented by a very simple circuit configuration. Moreover, the self-offset-cancellation capability of the  $\nu$ MOS op. amp. has greatly enhanced the accuracy of analog computation. Namely, the output offset voltage appearing in a multivalued logic gate does not increase with the increase in the number of input terminals and the output offset does not propagate to the next stage, thus making it very promising for implementing multivalued logic integrated circuits. Although we have achieved a high-accuracy multivalued logic computation, the data definitely need some quantization stages in the course of multiple stage processing for restoring the properly quantized levels. For this purpose the quantizer circuit described in [13] gives a good solution.

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### Further Results for Noise in Active RC and MOSFET-C Filters

G. Efthivoulidis, L. Tóth, and Y. P. Tsididis

**Abstract**—Noise due to resistors and op amps in active RC and MOSFET-C filters is considered. Bounds for the signal-to-resistive noise ratio and signal-to-op amp noise ratio in state-space filters are given.

#### I. INTRODUCTION

The signal-to-noise ratio is limited in active integrated filters due to technological restrictions and inherent limitations of active circuits. For this reason, there has been a considerable effort to characterize this quantity and investigate its fundamental limits [1]–[6].

Classical results on active filter noise are applicable to integrated filters (cf. [7]–[12]; many more references can be found in [5]). Noise in state-space active filters has been analyzed with the state-space method, and the optimal value of signal-to-noise ratio of these filters has been found [4]. Bounds for signal-to-noise ratio in transconductor-C filters are given in [4] and [6].

The noise due to resistors in active RC and MOSFET-C filters of arbitrary topology with power dissipation constraint has been examined in [5], where a bound for signal-to-noise ratio is given. In this brief we expand our results to the practically relevant case of limited total on-chip capacitance. In addition, we consider the noise due to operational amplifiers.

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