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Highly Robust Ultrathin Silicon Nitride Films Grown at Low-Temperature by Microwave-Excitation High-Density Plasma for Giga Scale Integration

Katsuyuki Sekine, Yuji Saito, Masaki Hirayama, and Tadahiro Ohmi, *Fellow, IEEE*

***Abstract*—This paper focuses attention on electrical properties of ultra-thin silicon nitride films grown by radial line slot antenna high-density plasma system at a temperature of 400 °C as an advanced gate dielectric film. The results show low density of interface trap and bulk charge, lower leakage current than jet vapor deposition silicon nitride and thermally grown silicon oxide with same equivalent oxide thickness. Furthermore, they represent high breakdown field intensity, almost no stress-induced leakage current, very little trap generation even in high-field stress, and excellent resistance to boron penetration and oxidation.**

***Index Terms*—Dielectric film, MOS capacitors, thin film.**

I. Introduction

THE PROGRESS of MOS LSI technology has been based on the shrinking of MOSFET's. Along with downsizing MOSFET's for more than 25 years, the gate oxide equivalent thickness of MOSFET's has continued to be reduced. Since the invention of MOS device, thermally grown silicon oxide, the prevailing gate dielectric for Si based MOS devices, has remarkable electrical properties that are unmatched by other materials. However, transistor scaling is driving gate oxide equivalent thickness to down 3 nm and below, when direct tunneling current becomes significant. Ultra-thin silicon oxide below 3 nm is not expected to be robust enough for future transistor gate dielectric application. In order to continue downsizing MOSFET's, thermally grown silicon oxide will be replaced by higher dielectric-constant films, for example Ta_2O_5 and Si_3N_4.

Furthermore, it is necessary to introduce metal substrate silicon-on-insulator (SOI) devices in future high-speed (>1 GHz) ULSI circuits [1]. In order to fabricate metal substrate SOI devices, all of manufacturing processes have to be done as low as 550 °C to avoid unexpected reaction between Si and metals. Moreover, to realize ultra-high integration devices with precise doping profile control, all of manufacturing processes must be done as low as 550 °C to prevent rediffusion of impurities previously formed in substrate. In order to establish total low-temperature processing below 550 °C, lowering the process temperature of high-integrity silicon nitride film formation is a critical issue. However, the conventional thermal nitridation of silicon surface uses high-temperature process over 1200 °C [2]. The growth temperature of plasma-enhanced nitridation exceeds 900 °C [3], [4]. Only few studies [5], [6], have explored lowering the growth temperature of silicon nitride by direct nitridation of silicon surface.

Recently jet vapor deposition (JVD) silicon nitride has been studied [7] and has shown excellent electrical results [8]. JVD silicon nitride films are deposited at room temperature, however, they needs high-temperature annealing at 800 °C to improve their electrical properties. Such a high-temperature annealing prevents from precise control of dopant profile formed previously in the substrate and enhances unexpected reaction between Si and metal.

A radial line slot antenna (RLSA) [9] high-density plasma system [10] can form high-integrity silicon nitride film at a temperature of 400 °C [11]. The purpose of this paper is to investigate electrical properties of ultra-thin silicon nitride film grown by RLSA high-density plasma system.

II. Experimental

Fig. 1 illustrates a newly-developed microwave-excitation plasma system featuring using radial line slot antenna (RLSA). This system is characterized by low ion bombardment energy less than 7 eV, high plasma density above 10^{12} cm^{-3}, low electron temperature below 1.3 eV and excellent uniformity less than 1% on 300 mm diameter wafer [10]. The low electron temperature is one of the factors that lower ion-bombarding energy. Plasma excitation space is enclosed with quartz cylinder to avoid any contamination from the surrounding spaces. In the direct nitridation of silicon surface, Ar/N_2 or $Ar/N_2/H_2$ or Ar/NH_3 mixed gases were used. The applied microwave power density and frequency were 5 W/cm^2 and 8.3 GHz, respectively. The substrate temperature was as low as 400 °C. Background pressure was 10^{-9} torr. Cz n-type (100) silicon wafers with a resistivity 3–5 Ω·cm and Epi p-type (100) wafers with resistivity 10–15 Ω·cm were used. Before direct nitridation, silicon surface was treated by modified RCA cleaning [12]. A MIS [$Al/Si_3N_4/Si(100)$] capacitor of 10^{-4} cm^2 and 10^{-3} cm^2 in area was fabricated to evaluate electrical properties. The Al electrodes with thickness of about 1 μm were deposited by evaporation. Ultra-thin silicon nitride films were grown by direct nitridation of silicon surface employing RLSA high-density plasma (Ar/N_2, $Ar/N_2/H_2$, or Ar/NH_3 mixed plasma) at 400 °C. Post metal annealing was carried

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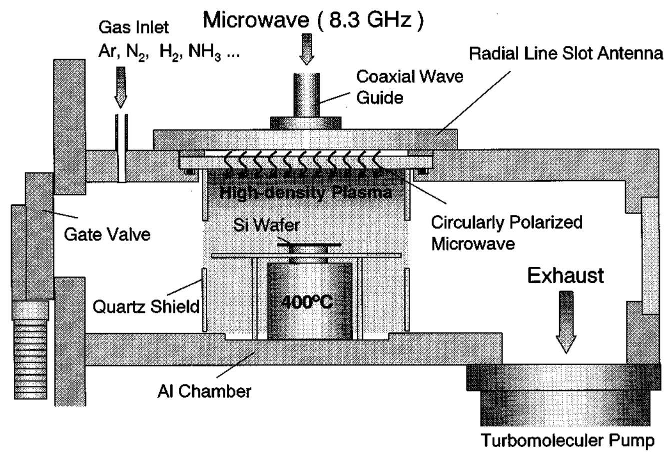

Fig. 1. Schematic of newly developed microwave-excitation plasma process equipment by using radial line slot antenna (RLSA).

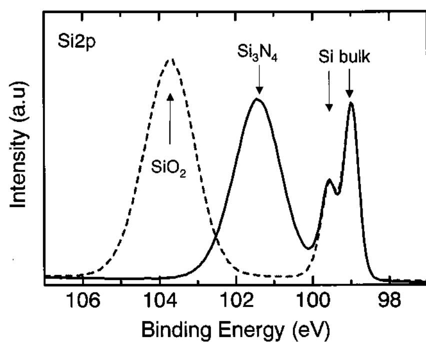

Fig. 2. Si2p XPS spectra of silicon nitride film grown by using high-density plasma at 400 °C. XPS spectra of thermally grown silicon oxide are also shown as a reference.

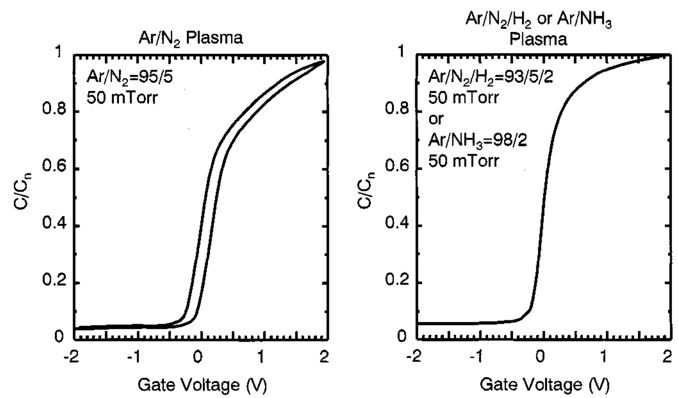

Fig. 3. C–V curve of silicon nitride grown by Ar/N_2 plasma and $Ar/N_2/H_2$ or Ar/NH_3 plasma, respectively.

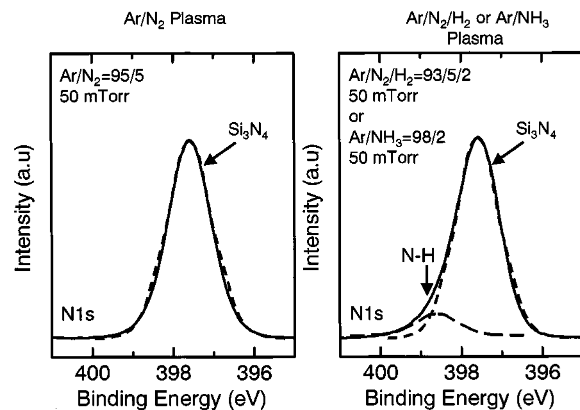

Fig. 4. N1s XPS spectra of silicon nitride film grown by Ar/N_2 plasma and $Ar/N_2/H_2$ or Ar/NH_3 plasma, respectively.

out at 400 °C in N_2/H_2 =90/10 mixing gas for 30 min. The equivalent oxide thickness (EOT) used in this study was obtained from high-frequency (1 MHz) capacitance–voltage (C–V) data in strong accumulation using a dielectric constant of 3.9. In constant current stress test, stressing current density was fixed at 10 mA/cm^2.

III. Results and Discussion

Fig. 2 shows Si2p X-ray photoelectron spectroscopy (XPS) spectrum of silicon nitride film grown at 400 °C by high-density plasma. Si2p XPS spectrum of thermally grown oxide is also shown in this figure as a reference. The intensity of Si2p3/2 from silicon substrate is normalized. The shape and position of chemically shifted Si2p peak due to nitridation of silicon surface shows that the silicon nitride film is nearly stoichiometric and Si-O_x bond does not exist in the silicon nitride film at all.

Fig. 3 shows C–V curves of silicon nitride grown by Ar/N_2 and $Ar/N_2/H_2$ or Ar/NH_3 (these two behave in the same way). There are humps due to interface traps and hysteresis attributed to charge traps in the silicon nitride film observed in C–V data of nitride film grown by Ar/N_2 plasma. On the other hand, hysteresis and hump do not exist in C–V data for nitride films grown by $Ar/N_2/H_2$ or Ar/NH_3 plasma. The hysteresis free silicon nitride can be realized at a temperature as low as 400 °C.

N1s XPS spectrums of RLSA silicon nitride film grown by Ar/N_2 and $Ar/N_2/H_2$ or Ar/NH_3 are shown in Fig. 4. N–H is identified with Si_3N_4 in XPS spectrum of RLSA silicon nitride grown by $Ar/N_2/H_2$ or Ar/NH_3 plasma. The hysteresis of C–V curve attributed to charge traps in silicon nitride film can be improved dramatically by terminating dangling bond in silicon nitride with hydrogen ($Ar/N_2/H_2$ or Ar/NH_3 case).

Fig. 5 shows J–V curves of silicon nitride grown by Ar/N_2 and $Ar/N_2/H_2$ or Ar/NH_3. The leakage current attributed to charge traps in silicon nitride film can be improved by terminating dangling bond in silicon nitride with hydrogen.

Fig. 6 shows high-frequency and quasistatic C–V curves of MIS capacitor with silicon nitride gate dielectric. There is no perceptible hysteresis attributed to charge trap in silicon nitride film at all. The excellent match between high-frequency and quasistatic C–V curve indicates low density of interface trap. The interface trap density of $1{\sim}3 \times 10^{11}$ (eV^{-1} cm^{-2}) at mid gap can be achieved at a temperature of 400 °C. The interface trap density can be improved below mid 10^{10} (eV^{-1} cm^{-2}) level by increasing growth temperature up to 500 °C. From capacitance of silicon nitride and physical thickness measured by spectroscopic ellipsometry, relative dielectric constant of 6.7 was calculated.

Fig. 7 represents the Fowler–Nordheim plot of the J–V curve of silicon nitride with 3.7 nm (EOT). In four decades, the J–V

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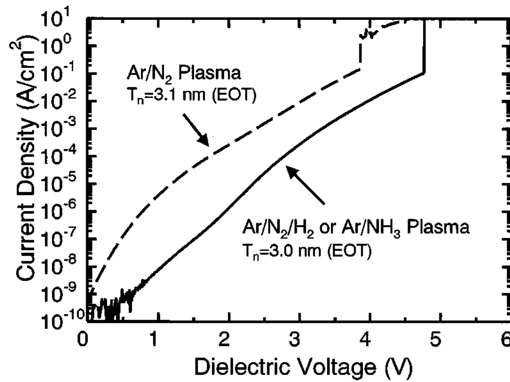

Fig. 5. J–V curves of silicon nitride grown in Ar/N_2 and $Ar/N_2/H_2$.

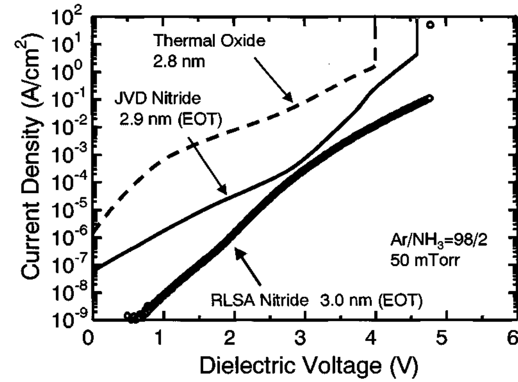

Fig. 8. J–V curves of various silicon nitride films with EOT around 3.0 nm.

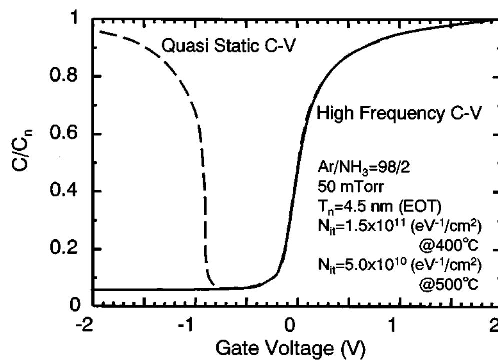

Fig. 6. High-frequency and quasistatic C–V curves of RLSA silicon nitride film.

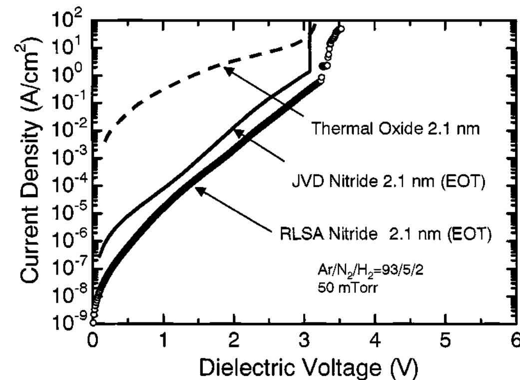

Fig. 9. J–V curves of various silicon nitride films with EOT of 2.1 nm.

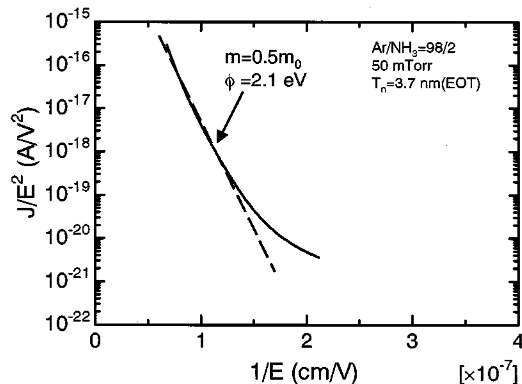

Fig. 7. Fowler–Nordheim plot of J–V curve of silicon nitride with 3.7 nm (EOT).

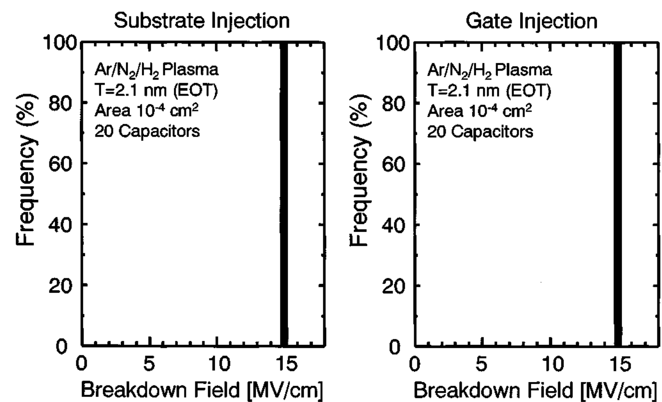

Fig. 10. Breakdown field intensity distribution of silicon nitride with EOT of 2.1 nm, substrate injection, gate injection.

curve shows excellent fit to Fowler–Nordheim tunneling. Assuming an effective mass of 0.5 times the free electron mass and using EOT, the electron barrier height is 2.1 eV. In conventional silicon nitride film, the dominant current component is due to the Pool–Frenkel conduction mechanism [13]. However, in silicon nitride film grown by RLSA high-density plasma, Fowler–Nordheim tunneling current is dominant in higher electric field region. This is due to decreasing trap density in silicon nitride. In lower electric field region, direct tunneling current plays major role.

Figs. 8 and 9 show J–V curves of silicon nitride with EOT of 2.1 and 3.0 nm, respectively. The leakage current of silicon nitride grown by RLSA high-density plasma is the lowest compared to those of thermal oxide [14] and JVD silicon nitride [14]. The reason for the tunneling current is much lower in silicon nitride film compared to thermally grown silicon oxide for a given EOT, despite having a lower barrier height than thermally grown silicon oxide, is because of its higher physical thickness which is more than the effect of barrier height differences.

Fig. 10 shows the breakdown field intensity (E_{BD}) distribution of silicon nitride film with EOT of 2.1 nm. High E_{BD} of over 15 MV/cm with excellent uniformity can be obtained for both polarities. These data are compatible to high-quality thermally grown silicon oxide.

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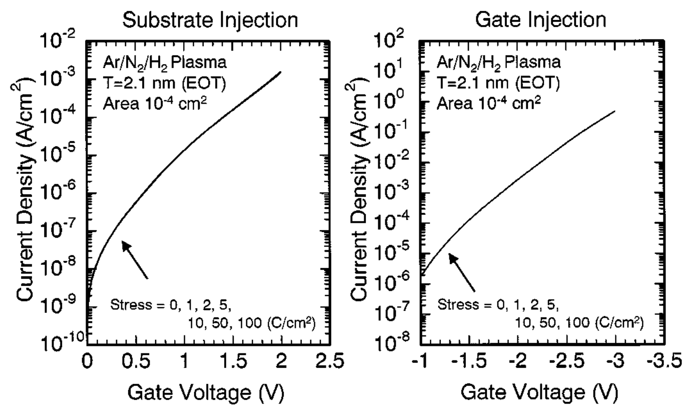

Fig. 11. Stress-induced leakage current of silicon nitride with 2.1 nm (EOT), substrate injection, gate injection.

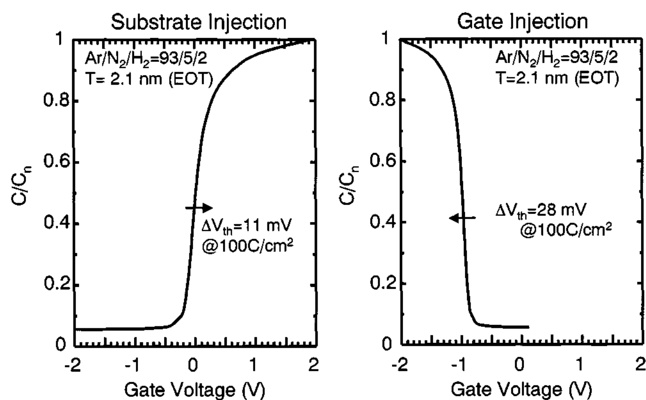

Fig. 12. Stress-induced C–V curve shift of silicon nitride with 2.1 nm (EOT), substrate injection, gate injection.

The stress-induced leakage current (SILC) for both polarities of current injection in MIS capacitor with 2.1 nm (EOT) silicon nitride is shown in Fig. 11. After constant-current stressing of 100 C/cm2, there is no discernible SILC for both polarities at all. The robustness of these films is demonstrated.

Fig. 12 shows stress-induced C–V shift of silicon nitride with 2.1 nm (EOT) for both polarities of current injection. After constant-current stressing of 100 C/cm^2, Vth shifts are only 11 mV for substrate injection and 28 mV for gate injection, respectively. Fig. 13 shows gate voltage shift of the silicon nitride with 2.1 nm (EOT) under the constant-current stress. After 10 C/cm^2 of constant-current stress, gate voltage shifts are only 18 mV for substrate injection and 30 mV for gate injection. These results show very little trap generation even in high-electric-field stress. These results are far better than the best results recently reported [15].

Fig. 14 shows how silicon nitride grown by RLSA high-density plasma system can resist to boron penetration. The substrate doping concentration was measured by high-frequency C–V curve in depletion region. For the silicon nitride film with 2 nm (EOT), no boron penetration took place at a temperature as high as 1000 °C for as long as 30 min, while a 5-nm thick thermally grown silicon oxide shows more than four orders magnitude increase in the surface doping condition.

The resistance to oxidation of silicon nitride layer is shown in Fig. 15. The EOT of silicon nitride is not increased after 800

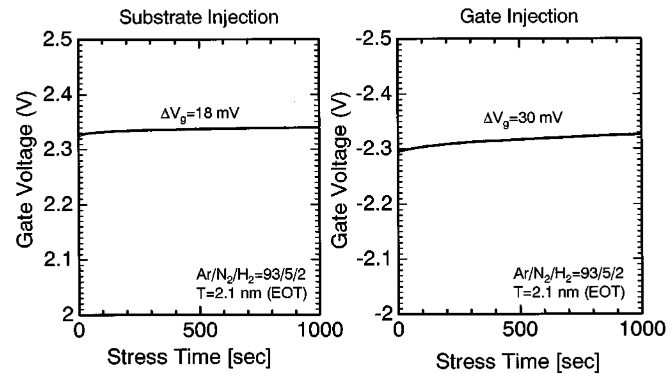

Fig. 13. Gate voltage shift under constant current stressing (10 mA/cm^2), substrate injection, gate injection.

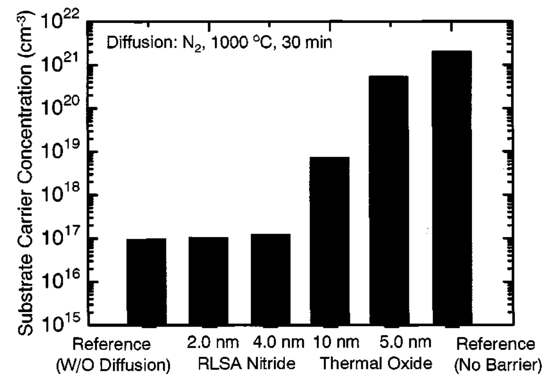

Fig. 14. Substrate boron concentration after drive in annealing at 1000 °C for 30 min.

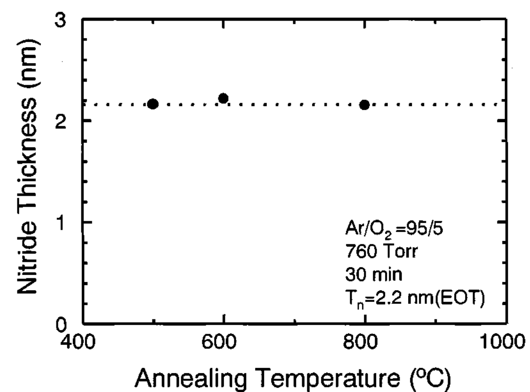

Fig. 15. Silicon nitride thickness after oxidation.

°C oxidation as long as 30 min. A 2.2-nm thick silicon nitride has excellent resistance to oxidation even at a temperature of 800 °C. The silicon nitride can be used as a barrier layer in order to suppress growth of unexpected silicon oxide layer between silicon substrate and high dielectric films.

IV. Conclusion

Highly robust ultra-thin silicon nitride films can be realized by direct nitridation of silicon surface at 400 °C employing RLSA high-density plasma system. The silicon nitride films have low density of interface trap and bulk charge enough to be used as a gate dielectric application. The gate leakage current

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is dramatically improved by the RLSA silicon nitride film compared to JVD silicon nitride films and thermally grown silicon oxide films with same EOT. Furthermore, they represent high breakdown field intensity, almost no stress-induced leakage current, very little trap generation even in high-field stress, and excellent resistance to boron penetration. They also have high resistance to oxidation to be used as a barrier layer between silicon substrate and high dielectric content materials for future gate dielectric structure. The scaling limit of gate dielectric can be overcome by the silicon nitride grown by RLSA plasma.

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Prior to 1972, he served as a Research Associate in the Department of Electronics of Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multi-valley diffusion, and frequency limitation of negative differential mobility due to an electron transfer in the multi-valleys, high-field transport in semiconductor such as unified theory of space-charge dynamics in negative differential mobility materials, Bloch-oscillation-induced, negative mobility and Bloch oscillators, and dynamics in injection layers. In 1972, he moved to Tohoku University, Sendai, Japan, where he is presently a Professor at the New Industry Creation Hatchery Center (NICHe). He is currently engaged in researches on high-performance ULSI such as ultra-high-speed ULSI: current overshoot transistor LSI, HBT LSI and SOI on metal substrate, base store image sensor (BASIS) and high-speed flat-panel display, and advanced semiconductor process technologies, i.e., ultra-clean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very-low-temperature Si epitaxy particle bombardment, crystallinity control film growth technologies from single-crystal, gain-size-controlled polysilicon and amorphous due to low kinetic energy particle bombardment, highly selective CDV, highly selective RIE, high-quality ion implantation with low-temperature annealing capability, etc., based on the new concept supported by newly developed ultra-clean gas supply system, ultra-high vacuum-compatible reaction chamber with self-cleaning function, and ultra-clean wafer surface cleaning technology. He has published 700 original papers and has 600 patent applications.

Dr. Ohmi received the Ichimura Award in 1979, the Teshima Award in 1987, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, the Okouchi Memorial Technology Prize in 1991, The Minister of State for Science and Technology Award for the promotion of invention 1993, the Invention Prize and 4th International Conference on Soft Computing (IIZKA' 96) Best Paper Award in 1996, and the IEICE Achievement Award in 1997. He serves as the President of the Institute of Basic Semiconductor Technology-Development (Ultra Clean Society). He is a Member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electronics of Japan, the Japan Society of Applied Physics, and the ECS.

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