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Current Drive Enhancement by Using High-Permittivity Gate Insulator in SOI MOSFET's and its Limitation

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***Abstract*—Speed enhancement effect by using high-permittivity gate insulator in SOI MOSFET and its limitation were investigated by two-dimensional device simulator and circuit simulator. The SOI structure is suitable to have excellent current drive by using high-permittivity gate insulator. Although the gate capacitance increases as a function of its dielectric constant, the current drive does not increase proportionally due to the inversion capacitance. According to the simulation results of the delay time, when the pulse waveforms driven by a CMOS inverter are propagated through 1mm-long interconnects, the delay time significantly reduces at the dielectric constant value of around 25 (Ta_2O_5). Thus, it is worthwhile using Ta_2O_5 for gate insulator to achieve high-speed operation. Furthermore, the reduction of source parasitic series resistance is a key issue to realize the highest current drive by using high-permittivity gate insulator in SOI MOSFET.**

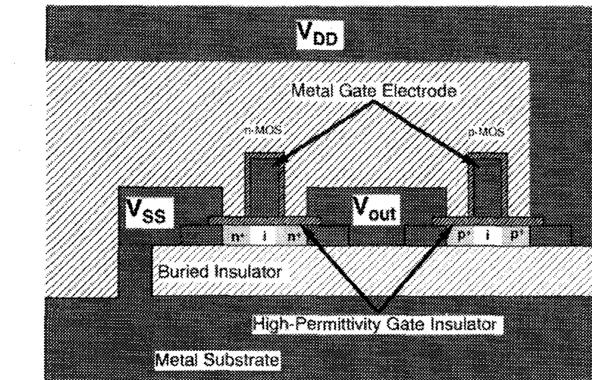

Fig. 1. Schematic cross section of SOI CMOS on metal substrate.

I. Introduction

HIGHER operation speed in a system is being required continuously. In a microprocessor equipped with a huge number of long interconnects as well as transistors, Bi-CMOS configuration has been mainstream in 1990's owing to its high current drive. As ULSI device structure becomes complicated, however, the number of Bi-CMOS process steps terribly increases. Furthermore, as supply voltage becomes lower, bipolar devices, whose switching threshold voltage is governed by the potential barrier of p-n junction, have a serious problem of degrading their current drive. In the next generation, full CMOS configuration will be desirable [1], [2]. One promising proposal to increase the current drive of ultra-small MOSFET's is to use a high-permittivity gate insulator. But, the usefulness and limitation of high-permittivity gate insulator instead of SiO_2 has not yet been presented in detail.

In order to realize ultra-high-speed microprocessors with around 10-GHz clock rate, the use of a metal substrate instead of Si substrate is essential. The pulse waveforms with 100-ps pulse width are seriously degraded after propagating through 1mm-long interconnect due to the power consumption in Si substrate [3]. As the skin depth, $(2/\mu\omega\sigma)^{1/2}$, of electromagnetic waves constituting voltage pulse becomes smaller than Si substrate thickness, a guided wave propagation along the interconnect occurs instead of plane wave propagation with accompanying longitudinal electric field component in Si substrate resulting in severe attenuation of the signal. Since the resistivity of metal is orders of magnitude lower than Si, such attenuation can be kept at an acceptable level. The metal substrate is inevitable for high-speed operation around 10-GHz clock rate. But, even if a metal substrate structure is introduced to ULSI, the voltage pulse of less than 50 ps cannot be transferred without attenuation because of the skin depth effect [2].

When metal substrate is employed, the device structure should be SOI (Si on Insulator). The ultra-thin SOI MOSFET is a candidate for the devices in a sub-halfmicron regime owing to the suppression of the short-channel effect [4], [5] and many other attractive advantages [6]–[8]. Furthermore, it was reported that the use of aluminum (ρ: $2.76\,\mu\Omega\cdot$cm) instead of heavily doped poly-silicon (ρ: $500\,\mu\Omega\cdot$cm) for gate electrode material is effective for high-speed driving of long interconnects [9].

Another problem of ULSI devices in microprocessor is power consumption. This factor limits the critical dimension of ULSI devices instead of material properties. Since it is necessary that the heat generated in the active regions of the MOSFET is immediately removed away, AlN, which has high heat conductivity (λ: 250 W/mK), is used for buried insulator instead of SiO_2(λ: 1.4 W/mK). In addition, AlN film has compatibility with the thermal expansion coefficient of Si. High-permittivity gate insulator, metal gate electrode SOI

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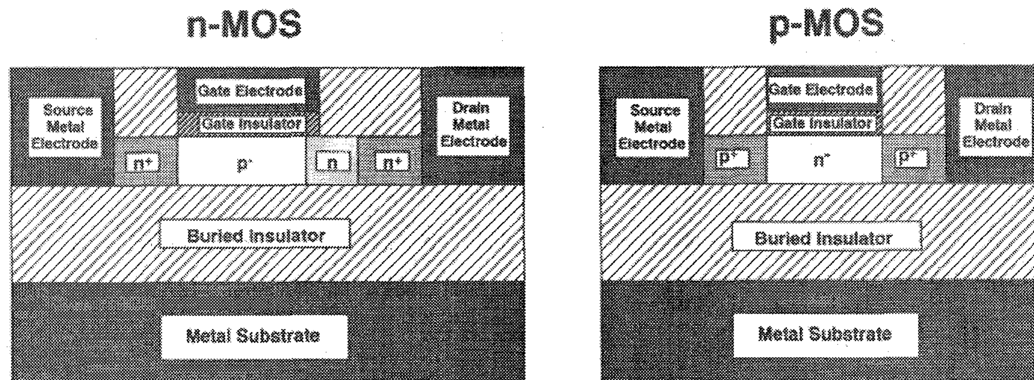

Fig. 2. Cross section of the simulated n-type and p-type MOSFET structure. $T_g = 5$ nm, $T_{si} = 10$ nm, $T_b = 1\,\mu$m. $V_{dd} = 1.0$ V, $V_{th} = +0.3$ V (n-MOS) /−0.3 V (p-MOS). $W/L = 1.0\,\mu\text{m}/0.1\,\mu$m. LDD concentration for n-type MOSFET is 1×10^{19} cm^{-3}.

CMOS on metal substrate, promising the operation speed of 10-GHz clock rate, is shown in Fig. 1.

In this paper, as the first step to realize metal substrate SOI MOSFET with high-permittivity gate insulator, the enhancement effect of current drive by using high-permittivity gate insulator in metal substrate SOI MOSFET and its limitation were investigated.

II. Simulated Conditions

The structure of the simulated n-type and p-type SOI MOSFET on metal substrate is shown in Fig. 2. These parameters were selected to enlarge the current drive and suppress the short-channel effect. The channel length and width are 0.1 μm and 1.0 μm, respectively, if not mentioned below. The channel doping concentration is set at 1×10^{14} cm^{-3} for both n-type and p-type transistor cases in order to suppress the carrier mobility degradation due to the impurity scattering [10]. The thicknesses of gate insulator, SOI film, and buried insulator were fixed at 5.0 nm, 10.0 nm, and 1.0 μm, respectively. As the buried insulator thickness increases, the current drive becomes larger [11]. The decrease of SOI film thickness leads to good subthreshold characteristics [12], [13]. Thus, the control of the channel doping concentration and the buried insulator thickness enlarges the current drive, and that of SOI film thickness suppresses the punchthrough current. The supply voltage (V_{dd}) is 1.0 V. The dielectric constant of the gate insulator varies from 3.9 to 100. Threshold voltage is defined as the gate voltage at which a tangent line with maximum slope to the $I_{ds} - V_{gs}$ characteristics in the linear region crosses the V_{gs} axis. The work functions of gate metal were selected so that the threshold voltages for n-type and p-type MOSFET's become +0.3 V and −0.3 V, respectively. It is necessary to develop the fabrication technology of mid-gap material for gate electrode in order to control the threshold voltage [14].

Asymmetric lightly-doped drain (LDD) structure [15] and single drain (SD) structure were used for n-type and p-type MOSFET, respectively. In particular, n-type MOSFET has a slightly overlapped LDD structure [16] without the operation of the parasitic bipolar transistor [17] and with the maximum current drive.

In this work, simulations were performed by a two-dimensional device simulator, VENUS-2D/B, in which drift-diffusion model was implemented, and by a circuit simulator, HSPICE. In this device simulation, the model does not take into account the contact resistance.

III. Results and Discussions

The I-V characteristics of n-type SOI MOSFET and n-type bulk MOSFET with Ta_2O_5 for gate insulator are shown in Fig. 3. Their threshold voltages are set at +0.3 V. As shown in the inset of Fig. 4, in bulk MOSFET (Epi structure) [18], substrate impurity concentration, ground plain concentration and junction depth are 1×10^{14} cm^{-3}, 1×10^{18} cm^{-3} and 10 nm, respectively. In Fig. 3(b), the drain-source voltage is 0.1 V. Although S factors of SOI MOSFET and bulk MOSFET are 65 mV/d., saturation drain current of SOI MOSFET is twice as large as that of bulk MOSFET. Fig. 4 shows the channel depth profile of electron concentration for n-type SOI MOSFET and n-type bulk MOSFET with Ta_2O_5 for gate insulator. This distribution is located at the center of the channel, and the origin of x-axis indicates the interface between Ta_2O_5 and Si. For SOI device, electron is widely distributed in SOI layer [19], while for bulk device, it is just gathered in the channel surface. Namely, in the case of 0.1-μm channel bulk MOSFET with Epi structure, the increase of the potential at the bottom of epi layer is suppressed due to a punchthrough stopper, resulting in its poor current drive. Thus, SOI structure is sufficient to obtain the effect on Ta_2O_5 gate insulator.

Fig. 5 shows the dependence of threshold voltage and subthreshold swing on the channel length with SiO_2 (ϵr: 3.9) and Ta_2O_5 (ϵr: 25) for gate insulator. For Ta_2O_5, the short-channel effect is sufficiently reduced even when channel length is in the sub-0.1- μm range. It is because the controllability of the charge under Ta_2O_5 is better than that under SiO_2. Fig. 6 shows the saturation drain current vs. dielectric constant of gate insulator for n-type MOSFET with 0.1- μm channel length. The threshold voltages of n-type MOSFET having various gate insulators are fixed at $+0.30 \pm 0.03$ V. As the dielectric constant increases, the saturation drain current becomes larger. The use of high-permittivity gate insulator is not only to suppress the short-channel effect but also to enlarge

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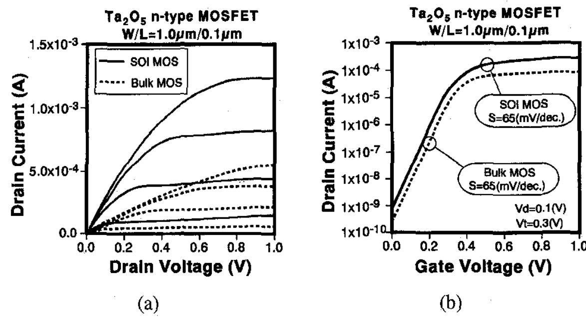

Fig. 3. I-V characteristics of n-type Ta_2O_5/SOI and Ta_2O_5/bulk MOSFET. (a) Id–Vd characteristics; V_{gs} is ranged from 0.4 V to 1.0 V stepped by 0.2 V. (b) Id–Vg characteristics; $V_{ds} = 0.1$ V. Channel width and length are set at 1.0 μm and 0.1 μm, respectively. Threshold voltages of SOI and bulk MOSFET are 0.3 V.

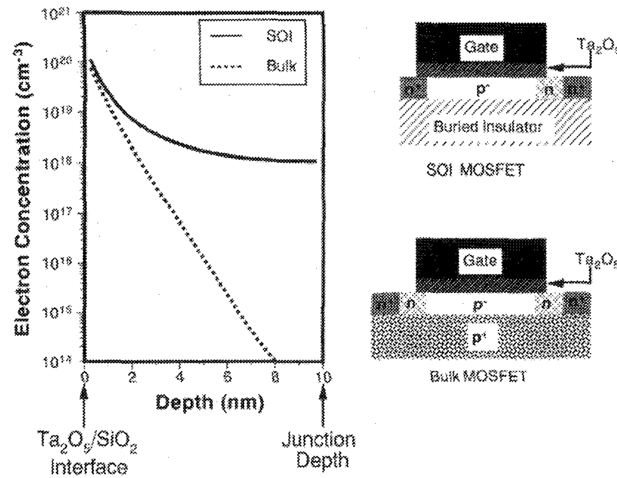

Fig. 4. Depth distribution of electron concentration in the center of channel for n-type SOI and n-type bulk MOSFET. $V_{ds} = V_{gs} = 1.0$ V.

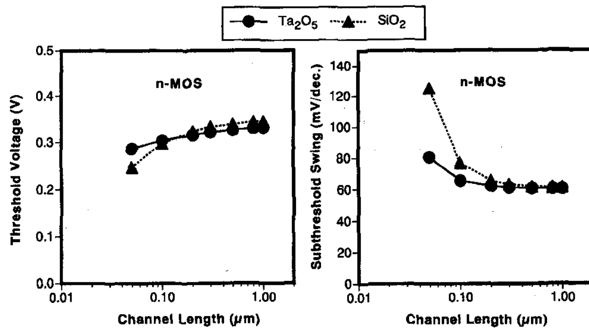

Fig. 5. Dependence of threshold voltage and subthreshold swing on effective channel length for n-type SOI MOSFET with Ta_2O_5 or SiO_2 for gate insulator.

the current drive without their trade-off relation. However, the current drive does not increase linearly and does not agree with the usual theory [20]. The result suggests that the current drive enhancement is limited by the increase of gate capacitance. It is considered that the inversion capacitance cannot be neglected as the gate capacitance increases.

The gate insulator thickness and the inversion layer width converted in SiO_2 thickness as a function of the dielectric constant are shown in Fig. 7. The higher permittivity gate

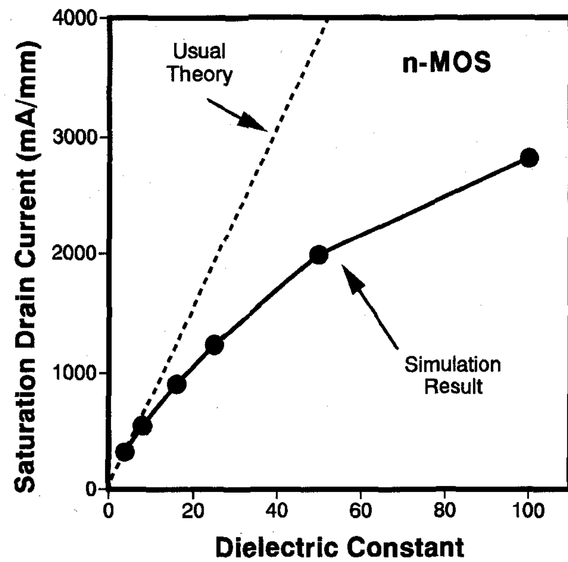

Fig. 6. Dependence of saturation drain current on dielectric constant of gate insulator. Channel length is 0.1 μm. Circle shows simulation results and dashed line shows usual theory.

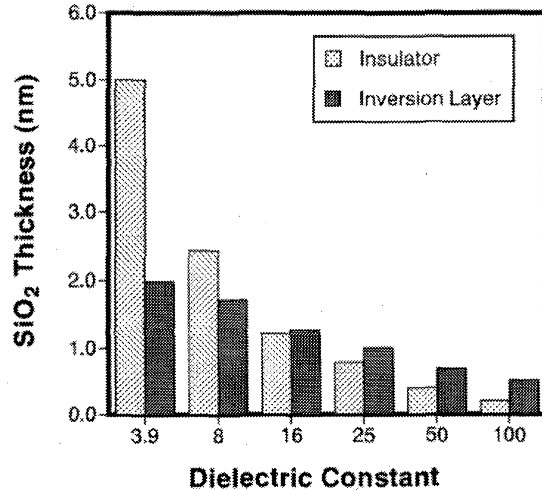

Fig. 7. Gate insulator thickness and inversion layer width converted in SiO_2 thickness versus dielectric constant of gate insulator. Channel length is 0.1 μm.

insulator makes the inversion charge density higher and the inversion layer width more narrow. This means that the large gate electric field induces a large amount of the inversion charges and strongly attracts the charge. This data shows that as the dielectric constant of gate insulator becomes larger, the inversion layer width cannot be ignored and then the inversion capacitance becomes the dominant factor. Fig. 8 shows the relationship between the effective gate capacitance and the dielectric constant of gate insulator. This characteristics almost matches with the trend in Fig. 6. It suggests that the reason of degraded current drive is the potential drop in the inversion layer.

In general, as SOI film thickness is reduced, source/drain series resistance of SOI MOSFET's becomes severe, especially

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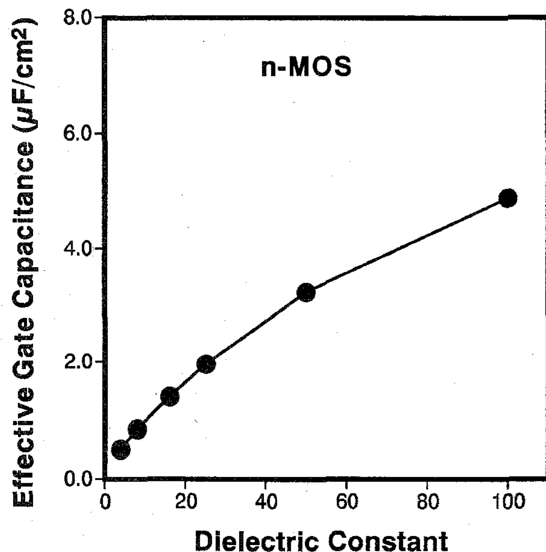

Fig. 8. Effective gate capacitance as a function of dielectric constant of gate insulator. Channel length is 0.1 μm.

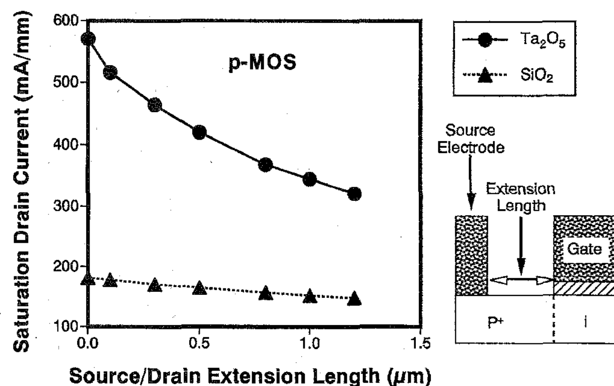

Fig. 9. Saturation drain current as a function of source/drain extension length. p-type MOSFET having Ta_2O_5 or SiO_2 for gate insulator was simulated. Channel length is 0.1 μm.

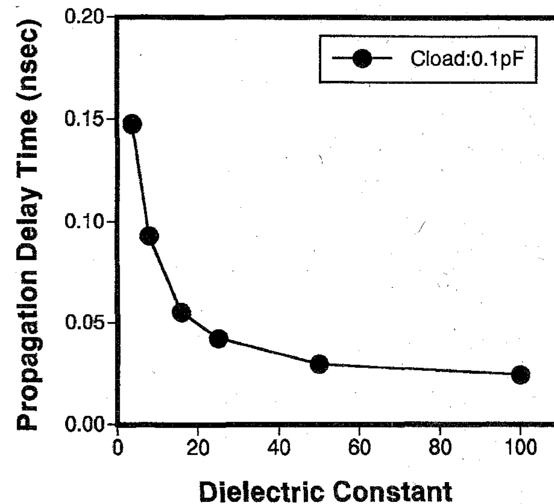

Fig. 10. Propagation delay time for CMOS inverter as a function of the dielectric constant of gate insulator when load capacitance is set at 0.1 pF. The parasitic capacitance of 1-mm interconnect is 0.1 pF. $L_n/L_p = 0.1\,\mu\text{m}/0.1\,\mu\text{m}$. $W_n/W_p = 1.0\,\mu\text{m}/2.1\,\mu\text{m}$.

for p-type MOSFET [21]–[23]. Fig. 9 shows the saturation drain current for p-type MOSFET as a function of source/drain extension length. The extension length is defined as the distance between the gate insulator edge and the source/drain metal contact edge. The increase of the extension length significantly degrades the current drive due to the negative feedback effect [19] of source parasitic series resistance. When the extension length is 1.0 μm, the decrease ratio of the saturation drain current for Ta_2O_5 is 40% of the saturation drain current of p-type MOSFET with null extension length. Moreover, the current drive degradation for Ta_2O_5 is more remarkable than that for SiO_2. For Ta_2O_5, the negative feedback effect of source resistance is significant because of the large amount of current drive, that is, an extremely low channel resistance, and therefore the reduction of the parasitic resistance is crucial.

Fig. 10 shows the propagation delay time for a CMOS inverter as a function of the dielectric constant of gate insulator, when the load capacitance is 0.1 pF. This load capacitance of 0.1 pF means the parasitic capacitance of 1mm-long interconnect. In this case, the channel width of p-type MOSFET is selected as the one where the on-currents of both, n-type and p-type MOSFET's, have the same value. With the increase of dielectric constant of gate insulators, the propagation delay time becomes significantly shorter around $\epsilon r = 25$ (Ta_2O_5), and then does not decrease significantly for larger values of the dielectric constant. The current drive enhancement effect by using high-permittivity gate insulator is saturated when the dielectric constant is greater than 25 due to the inversion capacitance. The use of Ta_2O_5 for gate insulator is a key issue to achieve ultra-high-speed performance of SOI CMOS.

IV. Conclusion

The structure of high-permittivity gate insulator SOI CMOS on metal substrate is proposed. Compared with bulk structure, SOI structure is sufficient to have high current drive. SOI MOSFET with Ta_2O_5 (ϵr: 25) for gate insulator has extra-large current drive, thus resulting in the ultra-high-speed response. Although the dielectric constant becomes greater than 25, the current drive enhancement effect is limited by inversion layer capacitance. Moreover, it is crucial to realize this high current drive by reducing the negative feedback effect of source resistance in high-permittivity gate insulator MOSFET case.

Acknowledgment

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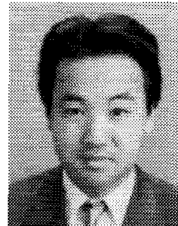

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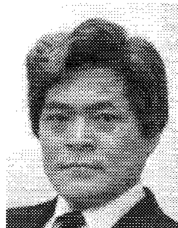

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