Neuron MOS Binary-Logic Integrated Circuits - Part II: Simplifying Techniques of Circuit Configuration and their Practical Applications

Neuron MOS Binary-Logic Integrated Circuits—Part II: Simplifying Techniques of Circuit Configuration and their Practical Applications

Tadashi Shibata, *Member, IEEE*, and Tadahiro Ohmi, *Member, IEEE*

Abstract—**In Part II of the paper, the fundamental circuit ideas developed in Part I [1] are applied to practical circuits and the impact of *neuron MOSFET* on the implementation of binary-logic circuits is examined. For this purpose, two techniques to simplify the circuit configurations are presented. It is shown that the input-stage D/A converter circuit in the basic configuration can be eliminated without any major problems, resulting in improved noise margins and speed performance. Then the design technique for symmetric functions is presented, which is especially important when the number of input variables is increased. The νMOS logic design is characterized by a dramatic reduction in the number of transistors as well as of interconnections. It is shown that a full adder circuit, for instance, can be constructed by only 8 transistors, while conventional CMOS design requires 50 transistors. In the case of flash A/D converter design, even more drastic effects are demonstrated, i.e., 16 transistors for a 3-b A/D converter as compared to 174 transistors by conventional CMOS design. However, such decrease in transistor count comes at a cost in process tolerance due to the multivalued nature of the device operation. Test circuits were fabricated by a typical double-polysilicon CMOS process and the measurement results are presented. Finally issues related to noise margins and speed performance of νMOS circuits are discussed.**

I. Introduction

In PART I of this paper, we have developed fundamental techniques of designing binary-logic circuits using *Neuron MOS Transistor* (neuMOS or νMOS) [1], a highly functional device simulating the behavior of biological neurons [2], [3]. The purpose of Part II is to exploit practical applications of the design concept developed in Part I and to examine the impact of νMOS circuit technology on logic ULSI implementation. Two approaches to simplify the basic νMOS circuit configuration are discussed in the first place. Then the experimental verification of designed circuits is presented for a full adder and a 3-b flash A/D converter. The noise margins and speed performance of νMOS circuits are also discussed.

Manuscript received December 11, 1992. This work was partially supported by the Ministry of Education, Science and Culture of Japan under Grant-in-Aid for Scientific Research 04402029. The review of this paper was arranged by Associate Editor S. Furukawa.

The authors are with the Department of Electronic Engineering, Tohoku University, Aza-Aoba, Aramaki, Aoba-ku, Sendai 980, Japan.

IEEE Log Number 9207586.

II. Elimination of Input-Stage D/A Converter

The basic configuration of νMOS logic circuits presented in Part I [1] employs a D/A converter circuit at the input stage which translates the combination of binary input signals into a single multivalued variable V_P that we call a principal variable. Then the design of a νMOS binary-logic circuit reduces to the definition of a functional form of the so-called universal literal function in the terminology of multivalued logic [4]. Such interpretation of νMOS logic circuits is quite straightforward and easy to understand, and in particular, is most suited for explaining the design principles. This is the reason why we have retained the D/A converter throughout the explanation in Part I. However, we can eliminate the D/A converter without any major disadvantages.

The D/A converter elimination simplifies the circuit configuration, thereby improving the integration density as well as the speed performance, while with a slight penalty of increased number of interconnects. The last issue is not essential and can be easily resolved by pattern layout as shown in Figs. 1 and 3. Since the only difference is the replacement of a single principal-variable line by multiple parallel input lines, there appears no complexity of interconnect crossing or no excess area required for extra interconnections.

The D/A converter-less version of the exclusive OR(XOR) circuit is shown in Fig. 1 in which the configuration of the pre-input-gate inverter (inverter *A*) is explicitly shown (to be compared to the circuit diagram in [1, fig. 2]). The two binary input signals X_1 and X_2 are directly coupled to the floating gates of the two νMOS inverters via capacitors having the weight ratio of 1 : 2. Since the analog mixing of the X_1 and X_2 signals takes place at the floating gate level, the net result of applying X_1 and X_2 via two separate capacitors reduces to giving a single voltage signal V_P via a single capacitor of $C_1 + C_2$. This V_P can be regarded as the principal variable in this case and is expressed as

$$V_P = (\tfrac{1}{3} X_1 + \tfrac{2}{3} X_2) V_{DD} \tag{1}$$

taking a four-level value of 0, $V_{DD}/3$, $2V_{DD}/3$, or V_{DD} as indicated on the abscissa of Fig. 2(a). In the original FPD representation using a D/A converter (see [1, fig. 3(a)]),

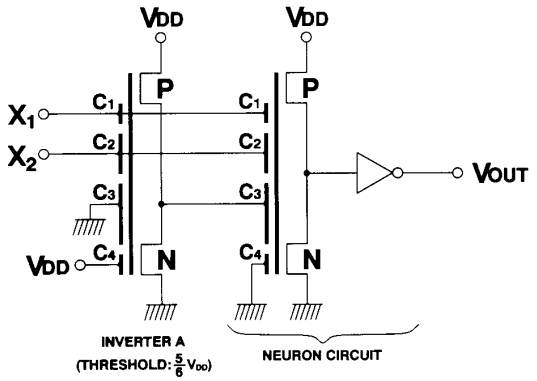


Fig. 1. Exclusive-OR circuit for two-input variables X_1 and X_2: the D/A converter-less version of the circuit shown in [1, fig. 2] (Part I of the paper).

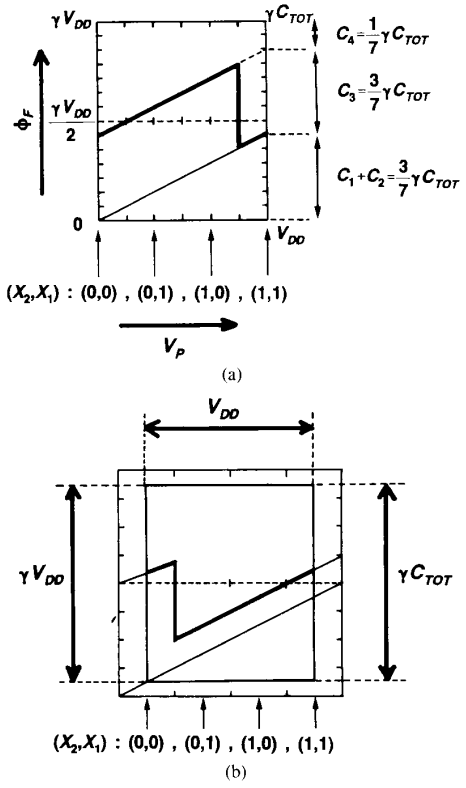


Fig. 2. (a) FPD in reduced-zone scheme for the νMOS inverter in the neuron circuit in Fig. 1 (b). The conversion relation from the original FPD representation to the reduced-zone scheme representation.

however, V_P is given by

$$V_P = (\tfrac{1}{4} X_1 + \tfrac{1}{2} X_3) V_{DD} + \tfrac{1}{8} V_{DD} \qquad (2)$$

which takes the value at the center of each divided section on the abscissa of FPD having an identical span of $V_{DD}/4$ as shown in Fig. 2(b). Accordingly, the FPD representation must be slightly modified as given in Fig. 2(a) which represents the FPD for the νMOS inverter in the neuron circuit in Fig. 1. From the FPD pattern, it is known that the circuit works as XOR. The magnitude of coupling capacitances as well as the pre-input-gate inverter threshold can be determined from the FPD.

From a practical point of view, the original FPD representation like the one in Fig. 2(b) is much easier to use in designing logic. Therefore, we recommend the following procedure. First, draw a FPD pattern in the original representation that matches the target function, and then convert it into the modified representation. The conversion relation is also illustrated in Fig. 2(b). If the original FPD representation is cut at the periphery of the diagram by $V_{DD}/8$ on the right and left, and by $\gamma V_{DD}/16$ at the top and bottom, the resultant diagram is the modified FPD representation. The full scale of the horizontal and vertical axes of the new diagram should be read as V_{DD} and γV_{DD} (and also γC_{TOT}), respectively. We call this new FPD representation for A/D converter-less circuits *Reduced Zone Scheme.*

III. Design of Symmetric Functions

If the result of calculation is invariant against the exchange of any input variables, the Boolean function is called "*symmetric.*" Almost all functions bearing special names, such as AND, OR, NOR, NAND, XOR, XNOR, etc., fall into this category. The design for such symmetric functions is much easier to carry out than for asymmetric functions because the weight factors to multiply input variables need not be taken into account. This greatly simplifies the circuit configuration, especially for logic with a number of input variables.

An example is a full adder circuit shown in Fig. 3. Quite interesting to note is that the circuit is composed of only 8 transistors (4 νMOS' and 4 regular MOS'). Since typical CMOS design requires 50 transistors to implement a full adder, a dramatic reduction in the number of transistors as well as of interconnects has been acheived by νMOS design. In the circuit diagram, the νMOS inverter #2 and the ordinary inverter #3 constitute a neuron circuit that calculates XOR of three input signals X, Y, C_0, namely the sum. The νMOS inverter #1 acts as a pre-input-gate inverter for the main νMOS inverter #2 and, at the same time, calculates the carry C for the upper bit. A photomicrograph of a test circuit fabricated by a double-polysilicon CMOS process is also given in the figure.

The FPD in the reduced-zone scheme for the νMOS inverter #2 is shown in Fig. 4(a). Since the logic state of a symmetric function is determined only by the number of 1's in the input variables, the principal variable in this case is represented by $V_P = nV_{DD}/3$, where n is the number of 1's in the group of X, Y, C_0. In Fig. 4(a), all possible combinations of input variables are indicated on the abscissa, while the target function (the desired output pattern) is given on top of the FPD. This relationship specifies the truth table for the function to be implemented.

Another circuit simplifying technique has been also employed in drawing the FPD pattern in Fig. 4(a) to reduce the number of input gates. The base line surpasses the threshold line and contributes to activate the νMOS

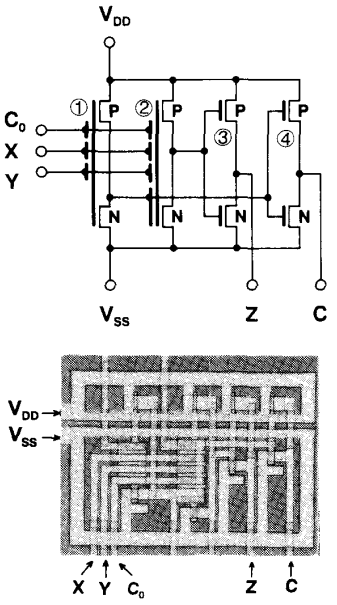


Fig. 3. νMOS full adder circuit composed of only 8 transistors.

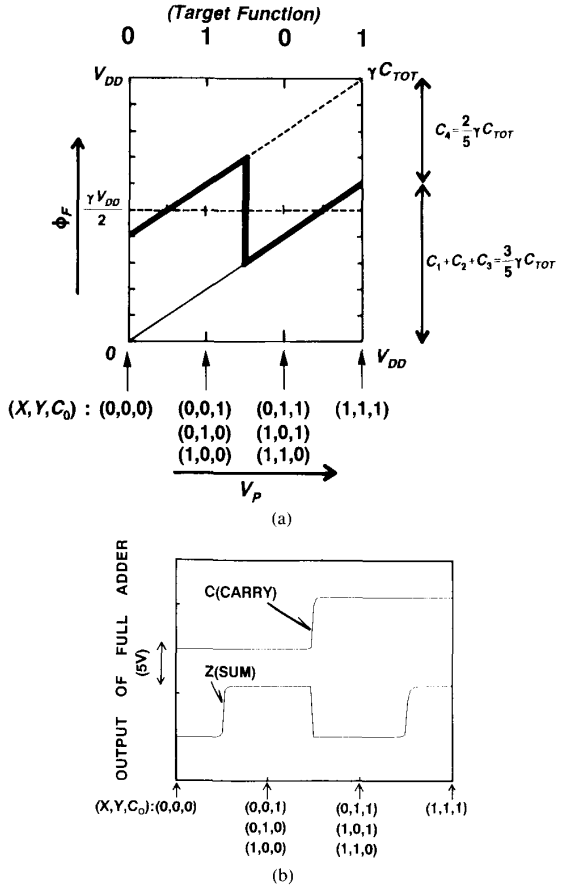


Fig. 4. (a) FPD in the reduced-zone scheme for the νMOS inverter #2 in Fig. 3. (b) Measured output characteristics of Z (sum) and C (carry) as a function of an analog voltage given to X, Y, C_0, simultaneously.

inverter #2 for $(X, Y, C_0) = (1,1,1)$. This should be compared, for instance, to the FPD pattern for XNOR in [1, fig. 3(b)], where the extra gate 3 is utilized to boost the base line. The pre-input-gate νMOS inverter (inverter #1) works just as a regular inverter with a threshold of $\gamma V_{DD}/2$. Therefore, its output becomes low for $n = 2$ and 3, yielding the carry signal at the output node C. The measured output characteristics are given in Fig. 4(b). Here the abscissa represents the analog input voltage applied simultaneously to all of the input terminals, which corresponds to the principal variable and is varied from 0 to 5 V. The circuit exactly functions as a full adder.

It is interesting to note that only two-stage inverters (#1 and #2) are sufficient to carry out the basic logic operations of 3-input exclusive-OR which requires a very complicated circuit configuration when built using only switching transistors. The roles of ordinary inverters #3 and #4 in Fig. 3 are nothing more than those of buffer amplifiers. The fact clearly exemplifies how the enhancement in the functional capability of an elemental transistor is important in simplifying the total circuit configuration.

As another example demonstrating the dramatic effect of νMOS design on the simplification of binary-logic circuit configuration, a 3-b flash A/D converter was designed and its circuit diagram is shown in Fig. 5. The circuit converts an analog input signal V_a into 3-b binary signals A_0, A_1, A_2. Here A_0 is the least significant bit and is calculated by the neuron circuit composed of the νMOS inverter #4 and the ordinary inverter #1. The FPD for the νMOS inverter #4 is given in Fig. 6(a). Here the input signal V_a is taken as a principal variable and the expected output pattern is "01010101." since a similar simplification technique as discussed in reference to Fig. 4(a) is employed here, the base line surpasses the threshold line at $V_a = 7V_{DD}/8$. The measurement results on a fabricated test circuit are shown in Fig. 6(b), which clearly demonstrates the 3-b A/D converter operation.

In order to examine the impact of νMOS design, a 3-b flash A/D converter was designed by conventional CMOS circuits. The circuit has 7 comparators at the input stage to distinguish 8 signal levels and the rest of the circuit is used for logic operations to decompose the level information into 3-b binary signals. The total number of transistors used in the circuit was 174. However, the number of transistors used in the circuit of Fig. 5 is only 16. It should be noted that the basic logic operations to convert V_a into three binary signals are conducted by only five νMOS inverters (#4–#8), and that the ordinary inverters (#1–#3) are working just as buffer amplifiers. A similar comparison was also made for the design of a 4-b flash A/D converter, resulting in the number of transistors of 28 by νMOS design versus 398 by the conventional CMOS design.

A substantial portion of the total job for executing an entire logic operation is shared at each νMOS transistor level, which reduces the load for the entire circuit to carry out and consequently simplifies the total circuit configuration. Assigning more jobs to each elemental transistor,

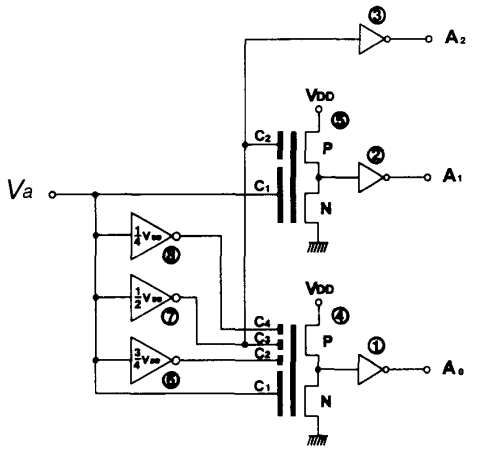


Fig. 5. Circuit diagram of a 3-b flash A/D converter implemented by νMOS design. The circuit is composed of only 16 transistors.

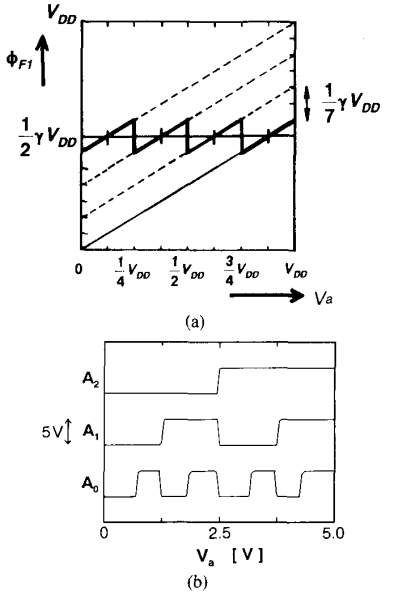


Fig. 6. (a) FPD pattern for the νMOS inverter #6 in the 3-b flash A/D converter shown in Fig. 5. (b) Its measured dc output characteristics.

we believe, is a key to simplify ULSI circuits and systems.

IV. Noise Margins of νMOS Circuits

In the D/A converter-less version of νMOS circuits, all signals transferred among νMOS inverters are binary. Therefore, the characteristic feature of νMOS binary-logic circuits is best expressed as *multivalued* operation within the νMOS inverter and *binary* operation outside the νMOS inverter. Due to the multivalued nature of the device operation, νMOS circuits inherently bear the problem of reduced noise margins.

The *S/N* ratio of an input signal is not degraded at the floating-gate level because both signal and noise at an input gate are reduced by the same factor determined by the coupling capacitance. The problem of the noise margin reduces to the level of accuracy at which we can determine the value of the floating-gate potential ϕ_F and the inversion threshold voltage V^*_{INV}.

A. Nonlinear Capacitance Effect

As an inherent problem related to the device structure, the effect of nonlinear capacitors is discussed in the following. Since ϕ_F is determined via capacitance coupling, the accuracy of each capacitance value is of prime importance. Among all C_i's in [1, eq. (1)], C_0, the capacitance between the floating gate and the substrate, exhibits nonlinear characteristics. C_0 is composed of the gate capacitances of NMOS and PMOS transistors in a νMOS inverter and a parasitic field MOS capacitor. The former is well approximated by the gate oxide capacitance because we are concerned about the conditions of both transistors when they are on. However, the latter changes according to the variation in the depletion layer width underneath the field oxide.

The variation in γ (the floating-gate gain factor defined by [1, eq. (3)] due to this effect was calculated assuming $\gamma = 0.9$ with interpoly-oxide thickness to gate-oxide thickness ratio of 1.5, gate oxide thickness of 100 Å, field oxide thickness of 0.5 μm, substrate doping of 3×10^{16} cm^{-3}, the area of floating gate on field oxide of 1.5 times the area of input gate to floating gate overlapping. When ϕ_F is changed from 0 to 5 V, the surface band bending underneath the field oxide increases by 0.115 V and the depletion layer width increases by 704 Å, resulting in a variation of γ of about 0.19%. This induces the deviation in the inverter threshold $\gamma V_{DD}/2$ of 4.28 mV. The value is negligibly small for the condition considered here.

B. Floating-Gate Charge Effect

Another important factor affecting the accuracy of inversion threshold V^*_{INV} is the net charge in the floating gate Q_F. After the fabrication processes, some charges are left in the floating gate, thereby causing fluctuations of inversion threshold from device to device. However, such residual charges can be canceled to zero by the UV (ultraviolet light) irradiation technique well known for EPROM erasing. Fig. 7 demonstrates the results of experiments carried out for single νMOS transistors. It is shown that the threshold voltages fluctuating at the initial stage beautifully converge to a single value equal to the designed value.

C. Level Accuracy

Deviations in important device parameters due to the insufficient control of fabrication processes must be minimized by employing noise-free manufacturing which eliminates all possible factors causing fluctuations in the process results by ultra clean technology [5]–[7]. The accuracy at controlling these parameters determines the minimum voltage swing of ϕ_F to distinguish two separate logic states (corresponding to the magnitude of each divided section on the abscissa of FPD), thus the number of logic states that can be handled in a νMOS inverter.

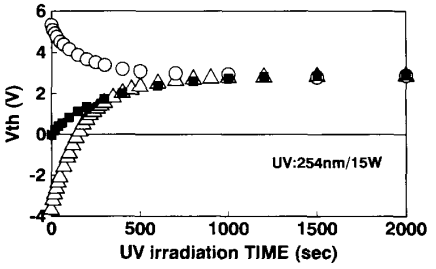


Fig. 7. UV erasing characteristics of νMOS transistors. The initial threshold voltages of test νMOS transistors were changed by electron injection to or extraction from the floating gate, and then UV irradiation experiments were carried out.

Here we introduce a term "Level Accuracy" to specify the tightness of process control required for the fabrication of νMOS chips. The level accuracy is defined as the number of divided sections on the abscissa of FPD, each representing an individual logic state. The circuits represented by FPD's in Fig. 3(a), (b) and [1, fig. 4] are all circuits of 4-level accuracy, while inverter #4 in the 3-b A/D converter of Fig. 5 is that of 8-level accuracy. The 4-b D/A converter, on the other hand, needs 16-level accuracy. In general, n-bit processing per single νMOS inverter gate requires 2^n-level accuracy (or 2^n-1 level accuracy in the case of the reduced zone scheme—see Fig. 2(a)), thus the tightness of process control becomes increasingly stringent as the number of input signals increases.

In the case of symmetric functions discussed in Section III, however, n-bit parallel processing per single νMOS inverter gate can be performed by only $(n + 1)$-level accuracy (n-level accuracy for reduced zone scheme), presenting a very powerful technique of designing circuits of higher functional capabilities. The full adder design is one of the examples, in which 3-input exclusive-OR is implemented by only 3-level accuracy (reduced-zone scheme design). A circuit accepting eight parallel bits at a single gate and calculating the sum and carries by two stages of νMOS inverters can be composed by 8-level accuracy, which is easily realizable by the present level of processing and manufacturing technologies. If the circuit is designed for nonsymmetric inputs (i. e., all 8 inputs are weighted), 256-level accuracy is required, which is by no means practical.

V. Speed Performance

The time required for the linear-weighted sum calculation of multiple input signals conducted by charge sharing among a number of capacitors is the order of dielectric relaxation time in the gate electrode material and is negligibly small. The input capacitance of each input gate is nearly equal to or smaller than its coupling capacitance, being comparable to that of a conventional MOSFET. This is because the sum of all other coupling capacitances is connected to the input-gate capacitance not in parallel but in series. Then the major factor that determines the switching speed of a νMOS inverter is the current driving capabilites of NMOS and PMOS transistors driven by the floating gate. The transconductance of a νMOS transistor as seen from input gate i is reduced according to the relation

$$g_m^{(i)} = \frac{\partial I_D}{\partial V_i} = \frac{\partial I_D}{\partial \phi_F} \cdot \frac{\partial \phi_F}{\partial V_i} = \frac{C_i}{C_{\mathrm{TOT}}} g_m^* \tag{3}$$

thus reducing the switching speed.

In order to make speed performance comparisons between νMOS and conventional CMOS circuits, SPICE simulations were carried out for nine-stage ring oscillators constructed by cascading three full adder circuits. In the case of νMOS circuit, the full adder of Fig. 3 was employed and X and Z terminals were used as an input and output by setting $C_0 = V_{DD}$ and $Y = 0$ as the worst case. The signal path in the full adder contains two νMOS inverters #1 and #2 and a CMOS inverter #3, making a total of nine stages of inverters in the ring oscillator. In the case of conventional CMOS, a full adder circuit was constructed based on NAND logic, and similar connections were made.

Parameters assumed for both cases were as follows: gate oxide thickness 30 nm; channel length $L = 1$ μm for all transistors; channel width $W = 1$ μm for NMOS, and $W = 3$ μm for PMOS in inverter configurations; β_R(β-ratio) = 1. In CMOS multiple-input NAND circuits, W (accordingly β) of NMOS was multiplied by the number of inputs in each case. In νMOS circuit, the coupling capacitances of each input gate were made all equal to the sum of NMOS and PMOS gate capacitance (4.6 fF). Only the W's of NMOS and PMOS in νMOS inverter #1 were tripled taking fan-out into account because it must drive both Z (sum) and C (carry) cricuits. Parasitic effects such as interconnect capacitance and resistance, source/drain capacitance, etc., were not included. Under these conditions, the oscillation period of the nine-stage ring oscillator τ was calculated for three threshold setting conditions, namely, $|V_{\mathrm{TH}}| = 0.5$, 1, and 1.5 V for both N- and PMOS's. For νMOS, $\tau = 2.25$, 2.70, and 3.74 ns when $|V_{\mathrm{TH}}| = 0.5$, 1, and 1.5 V, respectively. For CMOS, on the other hand, $\tau = 2.03$, 2.46, and 3.12 ns when $|V_{\mathrm{TH}}| = 0.5$, 1, and 1.5 V, respectively. The value of C_i/C_{TOT} in (3) for νMOS inverter in this example is 1/6, namely the g_m is decreased by a factor 6 as compared to CMOS circuits. However, the CMOS is faster than νMOS by no more than only 10–20%. This is due to the larger load capacitances for CMOS arising from multiple-input NAND gate and more parallel gates to drive. The effective g_m reduction in νMOS in case of the minimum logic swing, however, can be a dominant speed-limiting factor and further studies on improving the speed performance of νMOS circuits are critically required.

The comparisons of power dissipation were carried out for the ring oscillators mentioned above between νMOS and CMOS designs. The ratio of the average power of a νMOS ring to that of a conventional CMOS ring was 2.39, 1.71, and 0.915 for $|V_{\mathrm{TH}}| = 0.5$, 1, and 1.5 V, respectively.

VI. Conclusions

The fundamental design principles developed in Part I of the paper for neuron MOS binary-logic circuits have been applied to practical circuits and their impact on binary logic circuit implementation has been examined. Two techniques to simplify the circuit configurations have been introduced. One is the elimination of the input-stage D/A converter and the other is the design technique for symmetric functions. The latter is particularly important to build circuits receiving a number of input variables while assuring larger noise margins than circuits designed for nonsymmetric functions. It is demonstrated that the transistor count as well as interconnections can be dramatically reduced by νMOS designs as compared to conventional CMOS design counterparts. The designs have been experimentally verified by fabricating test circuits using a typical double-polysilicon CMOS process. From these observations, we conclude that the enhancement in the functional capability of an elemental transistor more than that of a mere switching device is very effective in reducing the complexity of the total circuit. This is one of the most promising ways to realize ultra large scale integration of logic circuits. νMOS is one of the candidates in the direction of this approach. Finally it has been pointed out that νMOS circuits inherently bear the issues of reduced noise margins due to the multivalued nature of device operation and reduced transconductance resulting from the drive of a floating gate by multiple input gates through capacitance coupling. Research for resolving these issues is now in progress and the results will be presented in future articles.

Acknowledgment

The authors wish to thank K. Kotani and T. Yamashita for their contributions to device fabrication. The concept of reduced zone scheme in the floating-gate potential diagram representation is due to the suggestion by K. Kotani. Part of this work was carried out in the Super Clean Room of the Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University.

References

[1] T. Shibata and T. Ohmi, "Neuron MOS Binary-Logic Integrated Circuits—Part I: Design fundamentals and soft-hardware-logic circuit implementation," *IEEE Trans. Electron Devices*, vol. 40, pp. 570–576, Mar. 1993.

[2] —— "An intelligent MOS transistor featuring gate-level weighted sum and threshold operations," in *IEDM Tech. Dig.*, 1991, pp. 919–922.

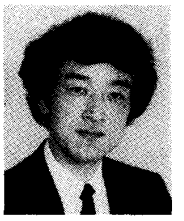
[3] —— "A functional MOS transistor featuring gate-level weighted-sum and threshold operations," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1444–1455, 1992.

[4] K. C. Smith, "Multiple-valued logic: A tutorial and appreciation," *Computer*, pp. 17–27, Apr. 1988.

[5] T. Ohmi, N. Mikoshiba, and K. Tsubouchi, "Super clean room system-ultra clean technology for submicron LSI fabrication," in S. Broydo and C. M. Osburn, Eds., *ULSI Science and Technology/1987(PV87-11)*. Pennington, NJ: Electrochem Soc., 1987, pp. 761–785.

[6] T. Ohmi, "Future trends and applications of ultra clean technology," in *IEDM Tech. Dig.*, 1989, pp. 49–52.

[7] T. Ohmi and T. Shibata, "Scientific manufacturing in the 21st century," in The Electrochemical Society *Interface*, pp. 32–37, Winter 1992.



Tadashi Shibata (M'79) was born in Hyogo, Japan, on September 30, 1948. He received the B.S. degree in electronic engineering and the M.S. degree in material science both from Osaka University, Osaka, Japan, and the Ph.D. degree from the University of Tokyo, Tokyo, Japan, in 1971, 1973, and 1984, respectively.

From 1974 to 1986, he was with Toshiba Corporation, where he worked as a researcher on the R&D of device and processing technologies for ULSI's. He was engaged in the development of microprocessors, EEPROM's, and DRAM's, especially in the process integration and the research of advanced processing technologies for their fabrication. From 1984 to 1986, he worked as a production engineer at one of the most advanced manufacturing lines of Toshiba. During the period of 1978 to 1980, he was a Visiting Research Associate at Stanford Electronics Laboratories, Stanford University, Stanford, CA, where he studied laser-beam processing of electronic materials including silicide, polysilicon, and superconducting materials. Since 1986, he has been Associate Professor at the Department of Electronic Engineering, Tohoku University. He is now engaged in the research and development of ultra-clean technologies. His main interest is in the area of low-temperature processing utilizing very-low-energy ion bombardment for the promotion of processes as well as in the development of the ultra-clean ion implantation technology to form defect-free ultra-shallow junctions by low-temperature annealing. He is currently working on the research of advanced device structures and their circuit applications.

Dr. Shibata is a member of Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, and the IEEE Electron Device Society.

Tadahiro Ohmi (M'81) was born in Tokyo, Japan, on January 10, 1939. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, in 1961, 1963, and 1966, respectively.

Prior to 1972, he served as a Research Associate in the Department of Electronics of Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multi-valley diffusion, and frequency limitation of negative differential mobility due to an electron transfer in the multi-valleys, high-field transport in semiconductor such as unified theory of space-charge dynamics in negative differential mobility materials. Bloch-oscillation-induced negative mobility and Bloch oscillators, and dynamics in injection layers. He is presently a Professor in the Department of Electronics, Faculty of Engineering, Tohoku University. He is currently engaged in researches on high-performance ULSI such as ultra-high-speed ULSI: current overshoot transistor LSI. HBT LSI, and SOI on metal substrate, base store image sensor (BASIS), and high-speed flat-panal display, and advanced semiconductor process technologies, i.e., ultra-clean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very-low-temperature Si epitaxy particle bombardment, crystalinity control film growth technologies from single-crystal, grain-size-controlled polysilicon and amorphos due to low kinetic energy particle bombardment, *in situ* wafer surface cleaning technologies due to low kinetic energy particle bombardment, highly selective CVD, highly selective RIE, high-quality ion implantations with low-temperature annealing capability, etc., based on the new concept supported by newly developed ultra-clean gas supply system, ultra-high vacuum-compatible reaction chanber with self-cleaning function, ultra-clean wafer surface cleaning technology, etc. His research activities are as follows: 260 original papers and 190 patent applications. He received the Ichimura Award in 1979, the Teshima Award in 1987, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, and the Okochi Memorial Technology Prize in 1991. He serves as the President of the Institute of Basic Semiconductor Technology-Development (Ultra Clean Society).

Dr. Ohmi is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, the Japan Society of Applied Physics, and the ECS.