Neuron MOS Binary-Logic Integrated Circuits - Part I: Design Fundamentals and Soft-Hardware-Logic Circuit Implementation

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Neuron MOS Binary-Logic Integrated Circuits—Part I: Design Fundamentals and Soft-Hardware-Logic Circuit Implementation

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Abstract—**In this part of the paper, we describe the fundamental designing principles of binary-logic circuits using a newly developed highly functional device called *Neuron MOS Transistor(νMOS)*. νMOS is a single MOS transistor simulating the function of biological neurons. In order to facilitate the logic design procedures employing this new-concept transistor, a graphical technique which we call Floating-Gate Potential Diagram has been developed. It is shown that any Boolean functions can be generated using a common circuit configuration of two-stage νMOS inverters. One of the most striking features of νMOS binary-logic application is the realization of a so-called *Soft Hardware Logic Circuit*. The circuit can represent any logic functions such as AND, OR, NAND, NOR, Exclusive-NOR, Exclusive-OR, etc., by adjusting external control signals without any modifications in its hardware configuration. The circuit allows us to build real-time reconfigurable systems. Test circuits were fabricated by a double-polysilicon CMOS process and their operations were experimentally verified.**

I. Introduction

THE GENERAL direction of technological development toward silicon ULSI (Ultra Large Scale Integration) system implementation is the enhancement in the integration density by miniaturizing physical dimensions of transistors. With such a scaling approach, however, a number of severe limitations are now being encountered in terms of the device performance and reliability [1], [2]. The problems arise mostly from the smallness of devices. In addition, long and entangled interconnections must be formed in order to establish mutual communications among a huge number of transistors on a chip. This also imposes a number of difficulties in terms of the routing design, multilevel interconnects formation, and circuit performance, and reliability [3].

We have developed a new functional MOS transistor called "*neuron MOSFET (νMOS)*" which simulates the function of biological neurons [4], [5]. The device is a multi-input MOS transistor which accepts multiple input signals, calculates the weighted sum of all input signals, and then controls the on and off states of the transistor. This function is exactly what is needed for an artificial neuron model to work [6] and the device is no doubt most suitable to construct neural networks [7]. In this study, however, we have intended to extract the maximum utilization of the very powerful functional capability of neuron MOSFET's in the implementation of binary logic circuits and to find solutions to the above mentioned problems.

Then the purpose of the paper in two parts is to provide enough details concerning the νMOS binary-logic circuit design and the text is prepared in order to serve as a practical guide for readers to design their own circuits. In Part I of the paper, the designing principles of νMOS logic circuits are explained using a graphical representation called Floating-gate Potential Diagram. Then the circuit of a new concept which we call *Soft Hardware Logic Circuit* is introduced. The experimental verification of these circuit ideas is also presented. In Part II (to be published), we will deal with more practical issues such as the techniques of simplifying the circuit configuration and application to practical circuits like full adders and flash A/D converters. The speed performance and noise margins of νMOS circuits will also be discussed in Part II.

II. Neuron MOSFET (νMOS)—A Brief Review

As shown in Fig. 1(a), a νMOS is an ordinary MOSFET except that its gate electrode is made floating and that the potential of the floating gate (ϕ_F) is determined via capacitive coupling with multiple input gates [4], [5]. The floating-gate potential is given by

$$\phi_F = \frac{C_1 V_1 + C_2 V_2 + \cdots + C_n V_n}{C_{\mathrm{TOT}}} \tag{1}$$

where

$$C_{\mathrm{TOT}} = \sum_{x=0}^{n} C_i$$

the total capacitance including C_0. Here C_0 denotes the capacitance between the substrate and the floating gate, which can be well approximated by the gate oxide capacitance provided that the inversion layer is formed underneath the gate oxide [5]. The charge in the floating gate Q_F is taken 0, which is valid under thermal equilibrium

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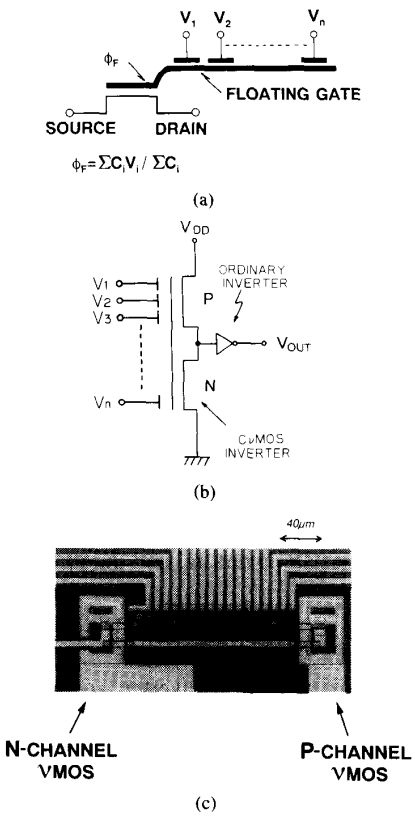

Fig. 1. (a) Symbolic representation of a neuron MOS transistor. (b) Neuron circuit composed of a complementary νMOS inverter and an ordinary CMOS inverter. (c) Photomicrograph of a C-νMOS inverter test circuit (16-input) fabricated by a double-polysilicon CMOS process. A conservative safety design rule was employed, where the gate lengths of NMOS and PMOS were 6 and 3 μm, respectively, and the metal pitch was 6 μm line width and 3 μm space.

and is easily achieved by UV erasing technique as will be shown in Part II of the paper (see Fig. 7). When ϕ_F is smaller than the threshold voltage of the transistor as seen from the floating gate (V^*_{TH}), the transistor is off. When ϕ_F exceeds V^*_{TH}, the transistor turns on. This is all of the operational principle of a νMOS transistor. The principle is extremely simple and involves nothing complicated or esoteric. Such simplicity in the device operation, however, is critically important in designing more complicated circuits and in building more sophisticated systems using the device as a basic element. The detailed analysis of νMOS transistors as well as of elementary circuit blocks along with their experimental verification are presented in our previous paper [5].

One of the most basic circuit blocks to construct νMOS binary logic is a neuron circuit which is composed of a complementary νMOS inverter and an ordinary CMOS inverter as shown in Fig. 1(b). The circuit outputs 1 or 0 depending on whether the weighted sum of all input signals is larger than V^*_{INV} (the inversion threshold of the νMOS inverter as seen from the floating gate) or not, respectively, thus representing the function of a neuron. A photomicrograph of a complementary νMOS inverter fabricated by a double-polysilicon CMOS process is shown in Fig. 1(c).

III. Logic Circuit Design Using Floating-Gate Potential Diagram

In this section, the design procedures of νMOS logic circuits are explained in detail taking exclusive-OR (XOR) and exclusive-NOR (XNOR) functions for two binary-signal inputs as examples.

A. Basic Circuit Configuration

The most fundamental configuration of a νMOS logic circuit is presented in Fig. 2. The circuit receives binary signals X_1 and X_2 as the input and gives a binary signal output of V_{OUT}. This particular circuit given as an example represents XOR of X_1 and X_2. The output stage of the circuit is a neuron circuit of Fig. 1(b) being composed of a 3-input-gate complementary νMOS inverter and an ordinary inverter. The input stage of the circuit is a complementary νMOS source-follower [5] which serves as a single-stage D/A converter. The circuit converts a 2-b binary signal input, X_1 and X_2, into a four-level analog signal V_P which we call a principal variable. The conversion relation for this circuit, which relates X_1, X_2 to the principal variable V_P, is indicated on the abscissa of Fig. 3(a). The operation of this circuit is briefly explained in the following.

The floating-gate potential of the D/A converter circuit is determined as $\phi_F = (C_1X_1 + C_2X_2)/C_{TOT}$, where C_1 and C_2 are the coupling capacitors of X_1 and X_2 gates, respectively, and designed as $C_1/C_2 = 1/2$. Therefore, ϕ_F is proportional to $X_1 + 2X_2$, the analog value represented by X_1 and X_2. Since both the n-channel and p-channel νMOS transistors in the circuit are made in a slight depletion mode, the circuit maintains an output voltage V_P by balancing the currents flowing in these two transistors. By equating the saturation-regime currents in these two devices, we obtain the relation

$$V_P = \Phi_F - \frac{\sqrt{\beta_R}\, V^*_{Tn} + V^*_{Tp}}{\sqrt{\beta_R} + 1}$$

where $V^*_{Tn}(<0)$, $V^*_{Tp}(>0)$ are the depletion-mode thresholds for n-νMOS and p-νMOS transistors as seen from the floating gate and β_R the β ratio of n-νMOS to p-νMOS (see [5, eq. (11)]). If it is designed, for instance, as $\beta_R = 1$, $|V^*_{Tn}| - V^*_{Tp} = V_{DD}/4$, and $(C_1 + C_2)/C_{TOT} = 3/4$, the above equation reduces to

$$V_P = (\tfrac{1}{4}X_1 + \tfrac{1}{2}X_2)\,V_{DD} + \tfrac{1}{8}V_{DD} \qquad (2)$$

where X_1, X_2 represent 1 or 0, yielding the conversion relation shown on the abscissa of Fig. 3(a). Here V_{DD} denotes the power supply voltage. The circuit can be described as an n-νMOS source-follower circuit utilizing p-νMOS as an active load. More detailed treatment of the circuit design and analysis including the substrate bias ef-

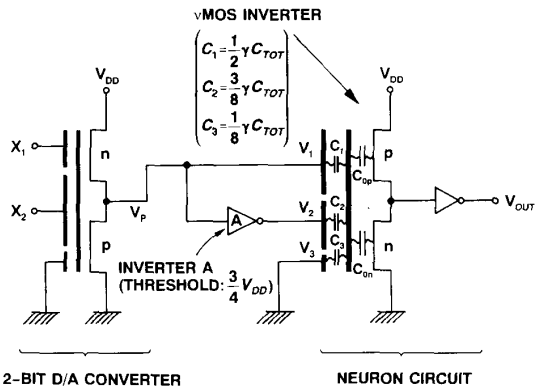

Fig. 2. Basic configuration of a νMOS binary-logic circuit, where the circuit is designed to implement Exclusive-OR (XOR) of X_1, X_2 as an example. Designed values of coupling capacitances are given in the figure, where γC_{TOT} represents $C_1 + C_2 + C_3$.

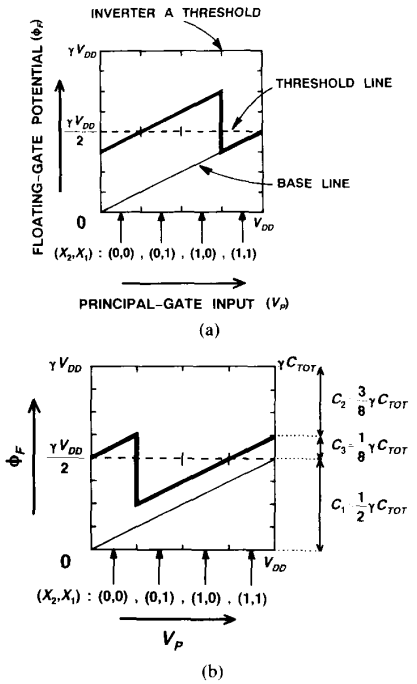

Fig. 3. (a) Floating-gate Potential Diagram (FPD) for the main νMOS inverter in Fig. 2, representing XOR function for binary variables X_1 and X_2. (b) FPD pattern representing Exclusive-NOR (XNOR) of X_1, X_2. The ordinate scale on the right is used to determine the magnitude of coupling capacitances.

fect will be described in a separate article. It should be noted here, however, that the D/A converter circuit can be removed without any major disadvantages as we will discuss in Part II of the paper. The only reason we retain the circuit here is that it is much easier to explain the principle of νMOS logic circuit operation including the D/A converter.

The principal variable is connected to the principal gate, the gate having the largest coupling capacitance (C_1), of the νMOS inverter. The standard design for the principal gate is

$$C_1 = \frac{\gamma C_{\mathrm{TOT}}}{2}$$

where γ is the floating-gate gain defined by

$$\gamma = \frac{C_1 + C_2 + \cdots + C_N}{C_{\mathrm{TOT}}}. \tag{3}$$

Therefore, γC_{TOT} represents the subtotal of the input-gate coupling capacitances. The principal variable is also connected to inverter A (which we call a pre-input-gate inverter) and its output is given to the second input gate of the νMOS inverter. This two-stage inverter configuration in which both inverter A and the νMOS inverter share the common input signal V_P and the output of the former is linked to the input of the latter is the very essence of implementing binary-logic circuits using νMOS. Any νMOS logic circuit has the same basic configuration with variations in the magnitude of coupling capacitances, the number of pre-input-gate inverters, and the threshold voltage of the inverters.

B. Floating-Gate Potential Diagram

The on and off of a νMOS inverter, and accordingly the high (V_{DD}) and low (0) outputs of the neuron circuit, respectively, are solely determined by the potential of the floating gate. Therefore, the circuit operation is understood in a very straightforward manner by analyzing the variation of ϕ_F as a function of other parameters such as the input voltages to the multiple input gates and the capacitive coupling coefficients.

In Fig. 3(a), ϕ_F of the νMOS inverter in Fig. 2 is shown as a function of the principal variable, i.e., the input voltage to the principal gate ($V_1 = V_P$). Such representation is called a Floating-gate Potential Diagram (FPD), and is used very extensively in the design and analysis of νMOS circuits. When V_1, V_2, V_3 are all at V_{DD}, ϕ_F takes the maximum value of γV_{DD}, which specifies the upper limit of the ordinate in the FPD. The baseline represents the variation of ϕ_F when $V_2 = V_3 = 0$ and only the principal gate voltage is varied from 0 to V_{DD}. The maximum is $\gamma V_{DD}/2$ because $C_1 = \gamma C_{\mathrm{TOT}}/2$. The inversion threshold V^*_{INV} of the νMOS inverter as seen from the floating gate is set at the standard value of $\gamma V_{DD}/2$, which is indicated in the figure as the threshold line. The design techniques of such νMOS inverters are described in [5] (see [5, eq. 15]).

As is evident from the figure, V_P alone cannot upset the νMOS inverter. In order to turn on the νMOS inverter, the assistance of other signals V_2, V_3 are essential. In the example shown in Fig. 2, the inverter A has an inversion threshold of $3V_{DD}/4$. Therefore, its output is high (V_{DD}) for $V_P < 3V_{DD}/4$, and boosts the level of the baseline by $3V_{DD}/8$ via capacitive coupling. For this purpose, the coupling capacitance C_2 is designed as $3\gamma C_{\mathrm{TOT}}/8$. However, this bias is removed when the inverter turns on, i.e., when $V_P > 3V_{DD}/4$. As a result, the overall variation of the floating-gate potential ϕ_F would be the one shown by

the bold line in the figure. The neuron circuit gets fired when the line surpasses the threshold line. Namely, the circuit gives an output of 1 when either X_1 or X_2 is 1 and the other is 0. This is nothing more than the realization of XOR function.

XNOR function can be also realized using the same circuit configuration if V_3 is set at V_{DD} and the inverter A threshold is changed to $V_{DD}/4$. The FPD for this case is given in Fig. 3(b). The fixed bias V_{DD} supplied to gate 3 boosts the level of the baseline by $\gamma V_{DD}/8$. And the inverter A further increases ϕ_F by $3V_{DD}/8$ until V_P reaches its threshold $V_{DD}/4$. Thus the function of XNOR is realized. By assigning proper values to V_{IA} (the inversion threshold of the inverter A) and the coupling capacitances C_2, C_3, we can arbitrarily select the places where 1 appears as a function of V_P, that is, we can generate any logic functions using the same circuit configuration.

It is convenient to use the ordinate scale of FPD to determine the magnitude of capacitance coupling coefficients. If the upper limit of FPD (γV_{DD}) is read as γC_{TOT} (the total of the all input-gate capacitances), the scale represents the value of the capacitance. Therefore, the general design procedure goes as in the following. At first, draw an FPD pattern to represent the desired logic function. Then the threshold of a pre-input-gate inverter (i.e., inverter A) and the values of coupling capacitances are determined from the abscissa and ordinate of the FPD, respectively.

Some of the design examples are shown by FPD patterns in Fig. 4. If gate 3 is removed in the circuit of Fig. 2 and C_2 is increased to $\gamma C_{\mathrm{TOT}}/2$, for instance, the circuit represents a NAND function (Fig. 4(a)). Using this configuration, the NOR function is obtained by making $V_{IA} = V_{DD}/4$ (Fig. 4(b)). AND and OR functions can be realized much more simply (Fig. 4(c) and (d)).

From the examples shown above, it is evident that any binary-logic function can be generated using the basic configuration given in Fig. 2. It should be noted that the circuit also represents a so-called universal literal function in the terminology of multiple-valued logic system [8] if the principal variable V_P is regarded as a four-valued variable. The single-stage D/A converter in the input stage translates the combination of binary input signals into a single multivalued variable V_P.

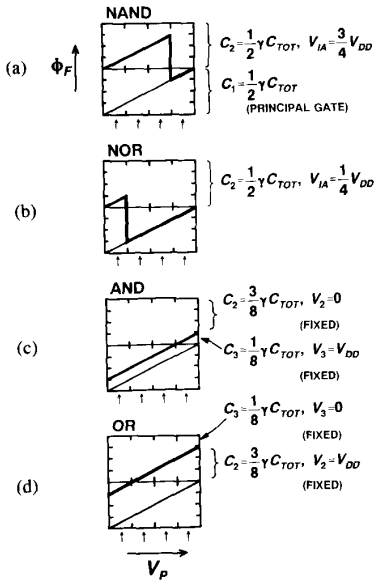

Fig. 4. FPD patterns representing: (a) NAND; (b) NOR; (c) AND; (d) OR.

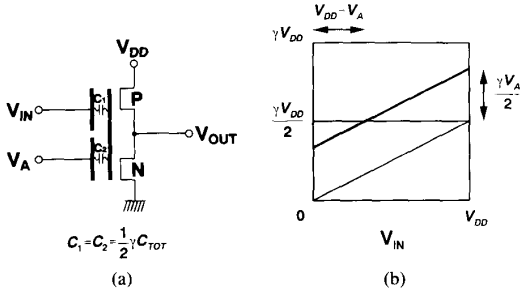

Fig. 5. (a) Complementary νMOS inverter with two input terminals: V_{IN} (signal input terminal) and V_A (control-signal terminal). The inversion voltage as seen from V_{IN} is given by $V_{DD} - V_A$. (b) FPD representation of the circuit in (a).

C. Threshold Voltage Adjustment

The essence of assigning a specific logic function to the circuit is the selection of coupling capacitances and the inversion threshold of the pre-input-gate inverter. The magnitude of the capacitance can be specified, for instance, by designing the poly-2 (input gate) pattern to poly-1 (floating gate) pattern overlap in the case of a double polysilicon process. On the other hand, the adjustment of threshold voltages is usually done by the ion implantation of dopants to channel regions. However, specifying many kinds of threshold voltages complicates the fabrication process, and further narrows the total process window because each threshold voltage must be adjusted to the specified value simultaneously. However, such threshold voltage adjustment is very simply done by using the concept of variable threshold transistor or inverter (see [5, Sections II-A and II-C]).

Fig. 5(a) shows a complementary νMOS inverter with two input gates of identical capacitances, and its FPD is shown in Fig. 5(b), where the abscissa represents V_{IN}, the input voltage to the inverter. As is evident from the figure, the magnitude of the boost to the baseline is half of γV_A and the apparent inversion threshold as seen from gate 1 is given by

$$V_{IA} = V_{DD} - V_A. \tag{4}$$

Therefore, the threshold voltage adjustment in individual inverters can be done by applying a constant dc bias voltage to the other input gate, while using inverters with all identical inversion threshold voltages. A dc bias can be

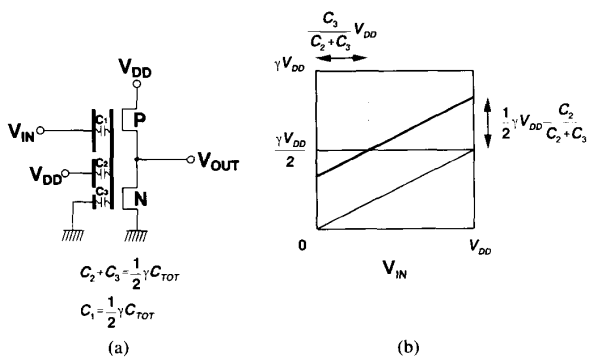

Fig. 6. (a) C-νMOS inverter whose inversion threshold is determined by the capacitance ratio of C_2/C_3. (b) Corresponding FPD representation.

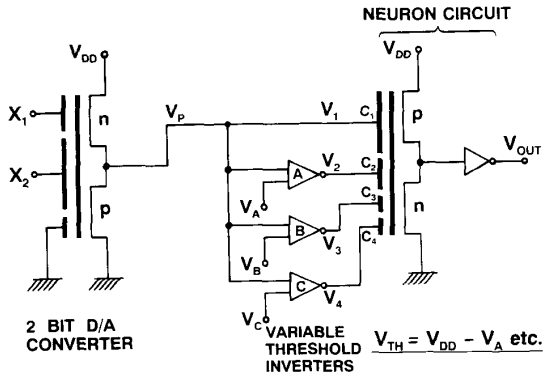

Fig. 7. *Soft Hardware Logic (SHL) Circuit* which can represent all 16 Boolean functions for two-input variables X_1, X_2 by adjusting external signals V_A, V_B, V_C.

generated, for instance, by the resistance division of the supply voltage V_{DD}. However, in order to avoid the increase in power dissipation and to guarantee the accuracy of dc voltage levels, threshold adjustment should be done as shown in Fig. 6, where the threshold is determined by the ratio of C_2/C_3; therefore, by the design of the patterns of 2 and 3. If the ratio C_2/C_3 is taken as 2/1, for instance, the threshold voltage can be defined by 2-b binary variables given to these two gates.

IV. Soft Hardware Logic Circuit

It has been demonstrated that any logic functions can be generated using the common circuit configuration of Fig. 2 by the selection of a pre-input-gate inverter threshold, the magnitude of coupling capacitances (C_2, C_3), and a constant dc bias (0 or V_{DD}) given to gate 3. If these parameters are made variable by external control signals, we can construct a circuit which changes its logic function upon request. This is the circuit of a new concept which we call a *"Soft Hardware Logic (SHL)" Circuit.* An example of a 2-input-variable SHL circuit is given in Fig. 7.

Since variable threshold inverters with configuration of Fig. 5(a) are used as pre-input-gate inverters A, B, and C, their inversion thresholds are determined by external signals V_A, V_B, and V_C, respectively, according to (4). C_2 $(=3\gamma C_{\mathrm{TOT}}/8)$ in Fig. 2 was replaced by two separate capacitances of $C_2 = 2\gamma C_{\mathrm{TOT}}/8$ and $C_3 = \gamma C_{\mathrm{TOT}}/8$ in the present circuit, and the effective coupling capacitance is changed by the combination of these elemental capacitors.

The circuit operation is very easily understood in terms of FPD. If control signals are selected as $V_A = V_B = V_{DD}/4$ and $V_C = V_{DD}$, the pre-input-gate inverter thresholds are determined as $V_{IA} = V_{IB} = 3V_{DD}/4$ and $V_{IC} = 0$. Accordingly, V_2 and V_3 are high (V_{DD}) until V_P reaches $3V_{DD}/4$, and V_4 is low (0) for all V_P's. As a result, we obtain a FPD pattern identical to that in Fig. 3(a) for the 4-input-gate νMOS inverter in Fig. 7, thus realizing XOR function. It is obvious that we can obtain a FPD pattern of XNOR function (Fig. 3(b)) by setting $V_A = V_B = 3V_{DD}/4$ and $V_C = 0$. As a matter of fact, the *Soft Hardware Logic (SHL) Circuit* shown in Fig. 7 can represent all possible 16 Boolean logic functions for two binary-signal inputs by the combination of external control signals.

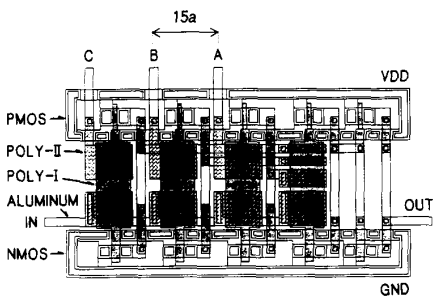

Fig. 8. An example of pattern layout for the *SHL Circuit* shown in Fig. 7. The length scale is indicated using the minimum feature size a. Experimental results given in Fig. 9 were obtained from a test circuit employing a safety design rule of $a = 3$ μm.

Fig. 8 shows an example of pattern layout for the SHL circuit shown in Fig. 7 which was designed based on a double-polysilicon CMOS process. The D/A converter at the input stage is not shown in the figure. The floating-gate gain γ is designed as 0.9 assuming the interpoly-oxide thickness to gate oxide thickness ratio of 1.5. The poly-1 to poly-2 coupling area was placed over the well boundary region. Various test circuits were fabricated by a typical double-polysilicon CMOS process and the circuit operation was tested. Fig. 9 demonstrates the examples of measurement results where the circuit output (V_{OUT}) is shown as a function of the analog input signal V_P. The circuit behaves exactly as expected, representing AND, OR, XOR, XNOR, and INHIBIT ("0010") functions. The FPD patterns for the respective functions are also given in the figure. More extensive experimental analysis of the circuit operation along with the fabrication process details will be reported in a separate article.

In order to specify the functional form in an *SHL Circuit*, three four-valued variables must be assigned for V_A,

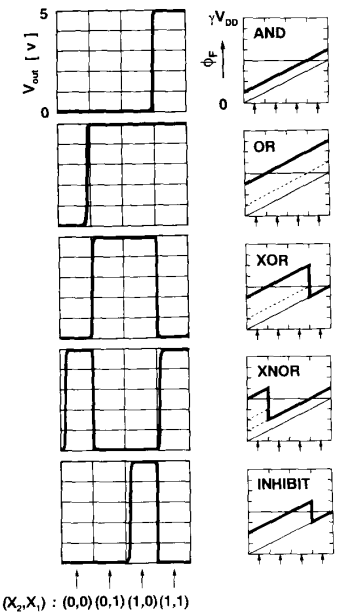

Fig. 9. Measured output characteristics of the *SHL Circuit* given in Fig. 7 shown as a function of V_P. AND, OR, XOR, XNOR, and INHIBIT functions are shown as examples along with their corresponding FPD patterns.

V_B, and V_C. On the other hand, it is also possible to specify the function by binary signals as is discussed in reference to Fig. 6. Then 6-b binary variables are utilized to specify the 16 functional forms. However, this is redundant. We have also developed a nonredundant *SHL Circuit* in which the 16 functional forms are specified by just 4-b binary variables.[1]

V. Conclusions

The principles of νMOS binary-logic circuit design have been described in detail and the circuit operation has been verified by test circuits fabricated by a double-polysilicon CMOS process. The design procedures have been made very simple and straightforward by the introduction of a graphical technique called Floating-gate Potential Diagram, in which the potential variation of the floating gate in the main logic-determining νMOS inverter is indicated as a function of input variables. A circuit of a new concept called *Soft Hardware Logic Circuit* has been developed. The circuit can represent any logic functions such as AND, OR, NAND, NOR, Exclusive-NOR, Exclusive-OR, INHIBIT, etc., by adjusting external control signals without any modifications in its hardware configuration. This circuit concept is really attractive in building more intelligent systems because it allows us to construct real-time reconfigurable systems. It is also possible to develop a highly flexible ASIC chip in which an *SHL Circuit* is utilized as a versatile elemental logic cell representing any functional forms. The chip function is created using metal masks by giving either the power supply voltage V_{DD} or the ground potential V_{SS} to each threshold setting node in pre-input-gate inverters. In Part II of the paper, we will deal with more practical issues such as the techniques of simplifying the circuit configuration and application to practical circuits like full adders and flash A/D converters. The speed performance and noise margins of νMOS circuits will also be discussed in Part II.

[1]The idea of nonredundant *Soft Hardware Logic Circuits* is proposed by K. Kotani and the circuit configuration will be presented in our later publication.

Acknowledgment

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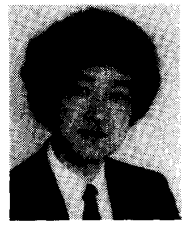
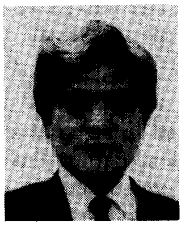


Tadashi Shibata (M'79) was born in Hyogo, Japan, on September 30, 1948. He received the B.S. degree in electronic engineering and the M.S. degree in material science both from Osaka University, Osaka, Japan, and the Ph.D. degree from the University of Tokyo, Tokyo, Japan, in 1971, 1973, and 1984, respectively.

From 1974 to 1986, he was with Toshiba Corporation, where he worked as a researcher on the R&D of device and processing technologies for ULSI's. He was engaged in the development of microprocessors, EEPROM's, and DRAM's, especially in the process integration and the research of advanced processing technologies for their fabrication. From 1984 to 1986, he worked as a production engineer at one of the most advanced manufacturing lines of Toshiba. During the period of 1978 to 1980, he was a Visiting Research Associate at Stanford Electronics Laboratories, Stanford University, Stanford, CA, where he studied laser beam processing of electronic materials including silicide, polysilicon, and superconducting materials. Since 1986, he has been Associate Professor at the Department of Electronic Engineering, Tohoku University. He is now engaged in the research and development of ultra-clean technologies. His main interest is in the area of low-temperature processing utilizing very-low-energy ion bombardment for the promotion of processes as well as in the development of the ultra-clean ion implantation technology

to form defect-free ultra-shallow junctions by low-temperature annealing. He is currently working on the research of advanced device structures and their circuit applications.

Dr. Shibata is a member of Japan Society of Applied Physics, the Institute of Electronics, Information and Communication Engineers of Japan, and the IEEE Electron Device Society.



Tadahiro Ohmi (M'81) was born in Tokyo, Japan, on January 10, 1939. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, in 1961, 1963, and 1966, respectively.

Prior to 1972, he served as a Research Associate in the Department of Electronics of Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multi-valley diffusion, and frequency limitation of negative differential mobility due to electron transfer in the multi-valleys, high-field transport in semiconductors, such as unified theory of space-charge dynamics in negative differential mobility materials, Bloch-oscillation-induced negative mobility and Bloch oscillators, and dynamics in injection layers. He is presently a Professor in the Department of Electronics, Faculty of Engineering, Tohoku University. He is currently engaged in researches on high-performance ULSI such as ultra-high-speed ULSI: current overshoot transistor LSI, HBT LSI, and SOI on metal substrate, base store image sensor (BASIS), and high-speed flat-panal display, and advanced semiconductor process technologies, i.e., ultra clean technologies such as high-quality oxidation, high-quality metallization due to low kinetic energy particle bombardment, very-low-temperature Si epitaxy particle bombardment, crystalinity control film growth technologies from single-crystal, grain-size-controlled polysilicon and amorphos due to low kinetic energy particle bombardmnent, *in situ* wafer surface cleaning technologies due to low kinetic energy particle bombardment, highly selective CVD, highly selective RIE, high-quality ion implantations with low-temperature annealing capability, etc., based on the new concept supported by newly developed ultra-clean gas supply system, ultra-high vacuum-compatible reaction chamber with self-cleaning function, ultra-clean wafer surface cleaning technology, etc. His research activities are as follows: 260 original papers and 190 patent applications. He received the Ichimura Award in 1979, the Teshima Award in 1987, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, and the Okochi Memorial Technology Prize in 1991. He serves as the President of the Institute of Basic Semiconductor Technology-Development (Ultra Clean Society).

Dr. Ohmi is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Electrical Engineers of Japan, the Japan Society of Applied Physics, and the ECS.