Revolutional Progress of Silicon Technologies Exhibiting Very High Speed Performance Over a 50-GHz Clock Rate

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Revolutional Progress of Silicon Technologies Exhibiting Very High Speed Performance Over a 50-GHz Clock Rate

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***Abstract*—Current silicon technologies are now facing very severe standstill, i.e., the operation speed is strictly limited at a clock rate of about 3.8 GHz due to the limitation of the thinning of the gate insulator film thickness because of its large amount of leakage currents through the current thermal oxide films. This typical disadvantage of current silicon technologies has been completely overcome by introducing the newly developed radical-reaction-based semiconductor manufacturing instead of the current molecule-reaction-based semiconductor manufacturing, i.e., direct nitridation films such as Si_3N_4 where the gate leakage current through the insulator films has been confirmed to be decreased by a factor of at least three orders of magnitude. The speed performance of silicon large-scale integrations is enhanced to exhibit a clock rate of more than 50 GHz by introducing the balanced complementary MOS on a silicon (551) surface substrate using 3-D-structured MOS transistors, where new key technologies must be introduced, namely: 1) direct nitridation gate insulator film Si_3N_4 for 3-D MOS transistors; 2) atomic-order flat-gate insulator film/silicon interface; 3) drastically decreased series resistance of the source and drain electrodes by a factor of two orders of magnitude; and 4) introduction of the accumulation-mode MOS transistors instead of the inversion-mode MOS transistors.**

***Index Terms*—CMOSFET circuits, silicon, metal–insulator–semiconductor (MIS) devices.**

I. Introduction

RADICAL-REACTION-BASED semiconductor manufacturing [1] has been developed using microwave-excited high-density plasma with very low electron temperatures where reactions are promoted by the reactivity of the radical itself such as oxygen radicals (O^*) for surface oxidation and NH radicals (NH^*) for surface nitridation, so that the process temperatures are lowered compared to those of current molecule-reaction-based semiconductor manufacturing, such as silicon surface oxidation at about 400 °C [2]–[4] and silicon surface direct nitridation at about 600 °C [5]–[8]. The radical-reaction-based surface oxidations and surface nitridations are characterized by very high integrity insulator films compared to current thermal oxide films such as low leakage current, very low interface state density, and very low 1/f noise level on a silicon surface of any crystal orientation, and the same oxidation and the same nitridation speed on a silicon surface of any crystal orientation [1]–[10]. On the other hand, the current thermal oxidation is well known to form relatively high integrity SiO_2 films only on silicon (100) surface, so that the MOS transistor structure is limited to the 2-D planar structures on the silicon (100) surface in current silicon large-scale integration (LSI) manufacturing technology. Thus, the performance of the planar silicon CMOS on silicon (100) surface is completely regulated by its very poor pMOSFET performance such as poor current drivability and poor transconductance, which are about one third of those of the nMOSFET. The radical-reaction-based surface oxidations and surface nitridations have introduced a revolutionary change in silicon technologies where 3-D-structured MOS transistors are completely available, as shown in Fig. 1(a) and (b), where the S-factor is plotted as a function of channel direction on Si (100) surface. It is seen in Fig. 1(a) that the 3-D MOS transistors that are fabricated by oxygen radical oxidation at 400 °C exhibit very excellent transistor performance, having S-factors ranging from 64 to 69 mV/dec, where the 3-D transistors that are fabricated by current thermal

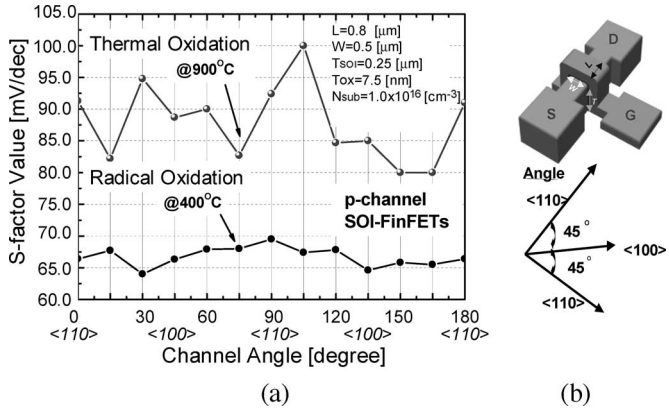

Fig. 1. (a) Measured subthreshold swing (S-factor) versus the channel angle of fabricated p-channel SOI FinFETs and (b) schematic explanation of FinFETs that are fabricated along various channel angles on (100) silicon surface.

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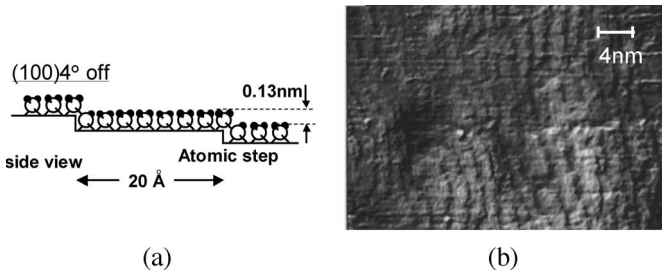

Fig. 2. (a) Schematic view of the atomic steps of the Si (100) surface 4° off toward [010] and (b) scanning tunneling microscope image of the Si (100) 4° off toward [010] after Hydrogen fluoride/Hydrochloric acid = 1 : 19 treatment of the wet oxide film that was obtained at 1000 °C.

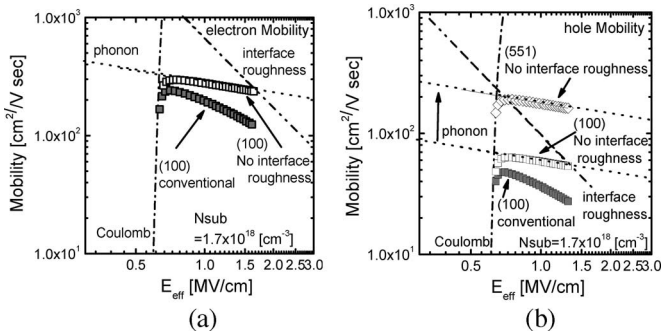

Fig. 3. (a) Electron and (b) hole mobility versus internal effective electric field toward the vertical direction in silicon channel.

oxidations exhibit very poor performance, such as S-factors ranging from 80 to 100 mV/dec. This result indicates that a very high integrity gate insulator film is formed on a silicon surface of any orientation in a very uniform manner by radical oxidation. The authors have already confirmed that, using the radical-reaction-based semiconductor manufacturing, pMOSFET transistors that are fabricated on silicon (551) surface along the ⟨110⟩ direction exhibit excellent current drivability that is completely similar to that of nMOSFET transistors on silicon (100) surface, leading to the realization of a balanced CMOS where the nMOSFET and pMOSFET transistors exhibit the same current drivability with the same effective device dimension [11]. Here, the silicon (551) surface is 8° off from the silicon (110) surface; it is very hard to be roughened even by alkali solutions [12], while the silicon (110) surface is very easily roughened.

II. New Concept of Very-High-Performance Silicon LSIs

In order to establish very-high-speed-performance silicon LSIs, we must develop four key technologies, along with device dimension miniaturization and a thinner and high-integrity gate insulator film.

1) Three-dimensional MOS transistor on silicon (551) surface, of which a high-integrity gate insulator film is realized by radical-reaction-based insulator film formation processes, i.e., radical oxidation and radical nitridation.
2) Atomic-order flatness of the gate insulator/silicon interface in order to improve electron and hole mobility by eliminating interface roughness scattering.

   Fig. 2 shows an example of the realized atomic flat silicon (100) surface 4° off toward the [010] direction [13]. Fig. 3(a) and (b) shows the electron and hole mobility as functions of the effective electric field toward the vertical direction in the silicon channel, where points that are indicated by "(100) conventional" are extracted by a real device. Mobility characteristics when interface roughness is adequately suppressed are shown in the figures. In Fig. 3(b), hole mobility on (551)-orientation surface is also shown. High mobility characteristics of electrons and holes can be realized by introducing a (551) silicon surface instead of the current (100) silicon surface, very high integrity gate insulator films such as Si_3N_4 and/or $Pr_3Si_6N_{11}/Si_3N_4$, and an atomic-order flat gate insulator/silicon interface.
3) Drastic decrease of the series resistance of the source and drain electrodes by a factor of two orders of magnitude to maximize the current drivability and the transconductance of MOS transistors.

   Fig. 4(a) shows the schematic view of the source and drain electrode series resistances R_S and R_D, respectively, in MOSFETs. The negative feedback effect to the transconductance that is induced by these resistances is shown in the following equations:

$$g_{\mathrm{meff}} = g_{\mathrm{mi}} \left(1 - \frac{I_D \cdot R_S}{(V_{GS} - V_{\mathrm{th}})}\right) \text{ in the saturation region} \tag{1}$$

$$g_{\mathrm{meff}} = g_{\mathrm{mi}} \left(1 - \frac{I_D \cdot (R_S + R_D)}{V_{DS}}\right) \text{ in the linear region} \tag{2}$$

   where g_{mi} and g_{meff} are the intrinsic and apparent transconductance of MOSFETs, respectively. Fig. 4(b) and (c) shows the energy band diagram of the n^+- or p^+-silicon and contact metals for the source and drain electrodes, and the relationship between the contact resistance and work-function difference between the n^+- or p^+-silicon and contact metals, respectively. From Fig. 4(a)–(c), it is clearly shown that the series resistances seriously degrade the current drivability and the apparent transconductance of MOS transistors having higher intrinsic transconductance when the conventional midgap metal material is used for the source and drain electrode contacts. To eliminate the negative feedback effect to the current drivability and the transconductance that is induced by the series resistance, different contact metal materials must be introduced for the source and drain electrode contacts of the nMOSFET and pMOSFET, of which barrier heights toward n^+ or p^+ silicon are at least less than 0.3 eV, resulting in a very small contact

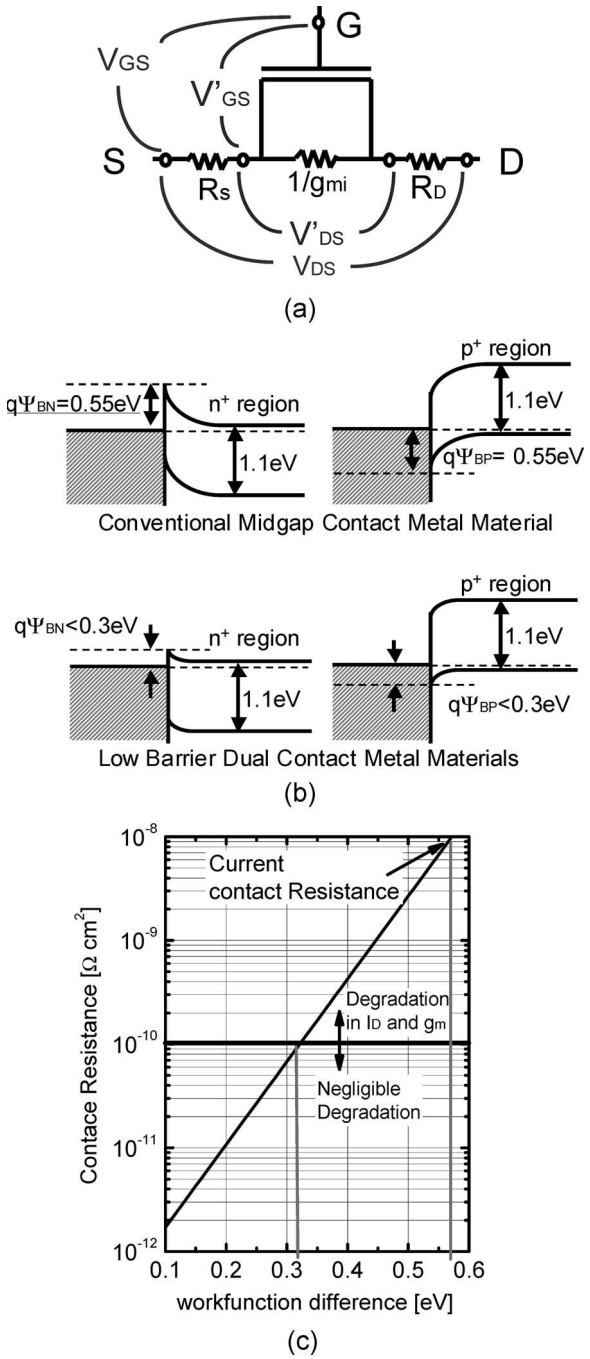

Fig. 4. (a) Schematic view of the source and drain series resistances in MOSFET. (b) Energy band diagram of the source and drain contacts and metal contact for the (upper) conventional midgap metal material and (bottom) low-energy barrier height contact metal materials to each n^+ and p^+ region. (c) Contact resistance versus work-function difference between n^+- or p^+-silicon and contact metals.

resistance, such as $1 \times 10^{-10}\ \Omega \cdot \mathrm{cm}^2$ from the conventional $1 \times 10^{-8}\ \Omega \cdot \mathrm{cm}^2$ [14].

4) An introduction of accumulation-mode MOS transistors on SOI silicon substrates instead of current inversion-mode MOS transistors.

The reasons for this transition will be explained in the next section.

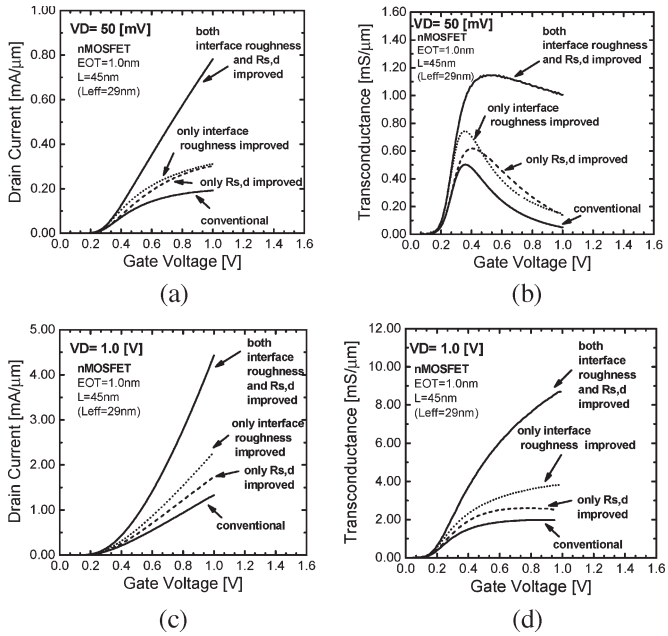

Fig. 5. (a) and (c) I_D–V_G and (b) and (d) g_m–V_G characteristics of nMOSFETs of which the effective channel length is 29 nm, for cases where there is no improvement on source and drain series resistances R_S and R_D, respectively, and interface roughness (conventional). (Dashed line) Only the source and drain resistances are improved. (dotted line) Only the interface roughness is improved. (Solid line) Both of them are improved. The drain voltage is 50 mV for (a) and (b), and 1.0 V for (c) and (d).

III. Typical Simulation Results

For 45-nm-technology-node nMOSFETs having a channel length of 29 nm and a gate insulator film of 1.0 nm, the drain current and the transconductance are plotted in Fig. 5(a)–(d) as a function of gate voltage at drain voltages of 50 mV in (a) and (b) and 1.0 V in (c) and (d) for upcoming technology advancements such as: 1) very small source and drain electrode series resistance (contact resistance ranging from $1 \times 10^{-8}\ \Omega \cdot \mathrm{cm}^2$ to less than $1 \times 10^{-10}\ \Omega \cdot \mathrm{cm}^2$); 2) atomic-order flat interface of gate insulator/silicon (from current $1.5 \sim 2.0$ nm peak to valley roughness to 0.13 nm peak to valley, i.e., one atomic step of Si (100) surface); and 3) a combination of these new technologies. It is very clear that the drain current and the transconductance are enhanced particularly at higher gate bias voltages by the combination of an atomic-order flat gate insulator film/silicon interface and drastically decreased source and drain electrode series resistances. The I_D–V_D characteristics of the nMOSFET and pMOSFET will be improved by introducing these technologies, as shown in Fig. 6, where (a) and (b) show the impact of the atomic-order flat Si/insulator interface and very low series resistance to the silicon (100) surface CMOS current drivability. Silicon (551) surface planar-structure CMOS is introduced in Fig. 6(c) where the pMOSFET and nMOSFET channels are formed on $\langle 110 \rangle$ and $\langle 100 \rangle$ directions, respectively. The current drivability of the nMOSFET on (551) surface $\langle 100 \rangle$ direction is about two thirds of that of the pMOSFET on (551) surface $\langle 110 \rangle$ direction. In addition, a 3-D-structured nMOSFET is introduced to establish the balanced CMOS on silicon (551) surface in Fig. 6(d). It is very clearly understood in Fig. 6(d) that the nMOSFET and pMOSFET exhibit completely similar

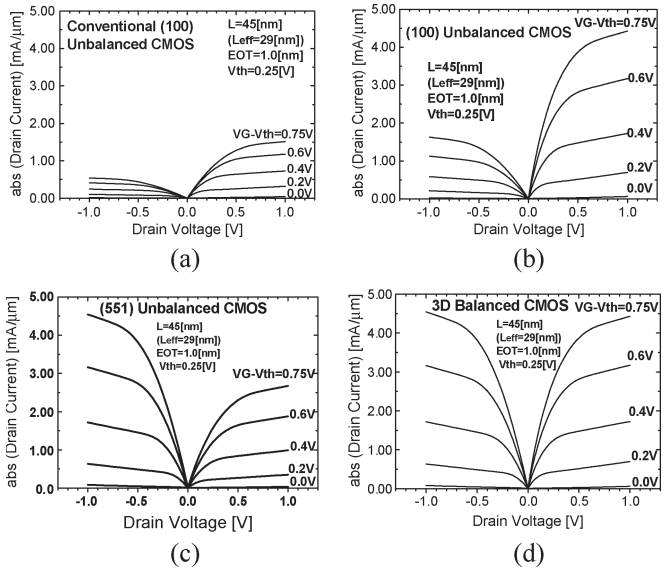

Fig. 6. I_D–V_D characteristics of (a) (100) surface conventional unbalanced CMOS; (b) (100) surface unbalanced CMOS that is realized by suppression of the source and drain resistances, and interface roughness; (c) (551) surface unbalanced CMOS; and (d) balanced CMOS realized by introducing (551) surface orientation for pMOSFET and 3-D nMOSFET.

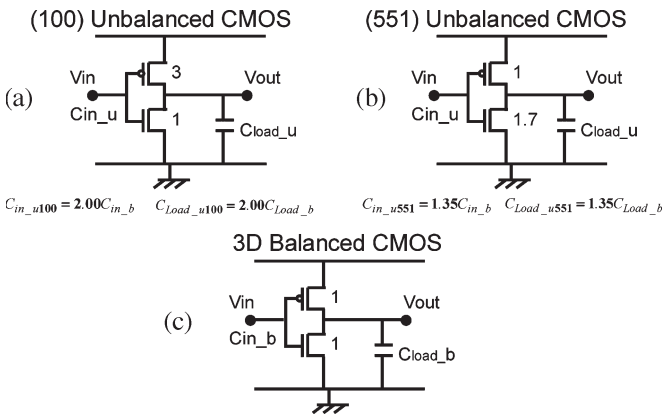

Fig. 7. Schematic views of the inverter configurations for the (100) surface unbalanced CMOS in (a), the (551) surface unbalanced CMOS in (b), and the balanced CMOS in (c).

and very high current drivability. Three typical CMOS inverter circuits are illustrated in Fig. 7(a)–(c) for the (100) surface unbalanced CMOS in (a), the (551) surface unbalanced CMOS in (b), and the (551) surface 3-D balanced CMOS in (c). Since the current drivability is equally balanced at very high performance in (c), the channel widths for the pMOSFET and nMOSFET are minimized compared to (a) and (b). Then, both the input and load capacitances of the balanced CMOS for digital LSI applications are reduced to 1/2.0 compared to the (100) surface unbalanced CMOS and 1/1.35 compared to the (551) surface unbalanced CMOS. The balanced CMOS and the (551) surface unbalanced CMOS have been confirmed to exhibit very excellent high speed performance compared to the conventional CMOS and the (100) surface unbalanced CMOS, as shown in Fig. 8, where the balanced CMOS and the (551) surface unbalanced CMOS inverters completely respond to a 100-GHz clock operation speed. So far, inversion-mode

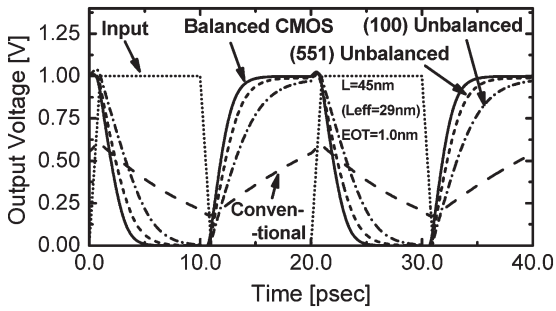

Fig. 8. SPICE simulation result of the output response of a one-stage inverter with fan-out equals to 3 that was constructed by the (100) surface conventional unbalanced CMOS, the (100) surface unbalanced CMOS, the (551) surfaced unbalanced CMOS, and the balanced CMOS.

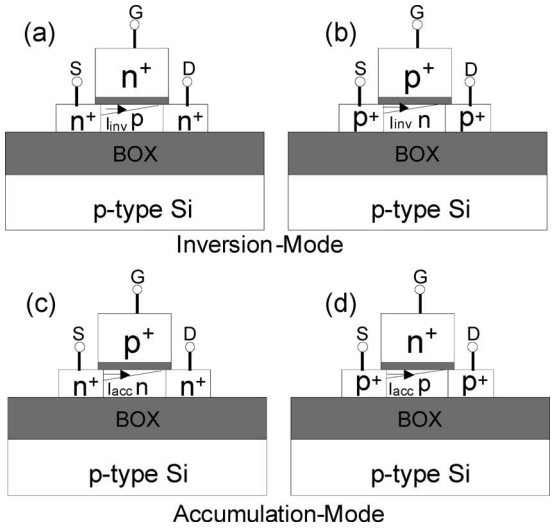

Fig. 9. Schematic views of the inversion-mode fully depleted SOI (a) nMOSFET and (b) pMOSFET, and the accumulation-mode (c) nMOSFET and (d) pMOSFET. For accumulation-mode complementary MOSFETs, the impurity type of the channel is the same as that of the source and drain regions, and the normally off characteristics are achieved by the work-function difference between the silicon channel and gate regions.

MOS transistors [Fig. 9(a) and (b)] are widely used in the field of silicon LSIs, but, currently, accumulation-mode MOS transistors [Fig. 9(c) and (d)] must be introduced in silicon LSIs [15]–[17]. The reason is given as follows: The directions of the electric field in the thin-gate insulator film and in the silicon channel region are the same those in the inversion-mode MOS transistors for the OFF-state and the ON-state, as shown in Fig. 10(a) and (b), while the electric field directions are opposite in the accumulation-mode MOS transistors for the OFF-state and the ON-state. Thus, the voltage swing can be enlarged for the accumulation-mode MOS transistor LSI compared to that of the inversion-mode MOS transistor LSI having the same equivalent oxide thickness (EOT, 1.0 nm) of the gate insulator film, such as 1.3 V compared to 1.0 V when the maximum electric field intensity in the gate insulator is maintained at 8 MV/cm, corresponding to a gate leakage current density of 0.1 A/cm^2 for the Si_3N_4 gate insulator film, and 1.45 V compared to 1.15 V when the maximum electric field intensity in the gate insulator film is 10 MV/cm, corresponding to a gate leakage current density of 1 A/cm^2. Additionally, since the depletion

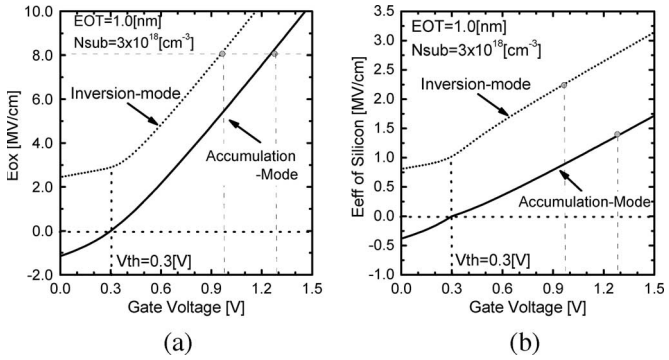

Fig. 10. Electric-field intensities in the gate insulator film in (a) and in the silicon channel region in the vertical direction in (b) as a function of gate voltage for the inversion-mode and accumulation-mode nMOSFETs.

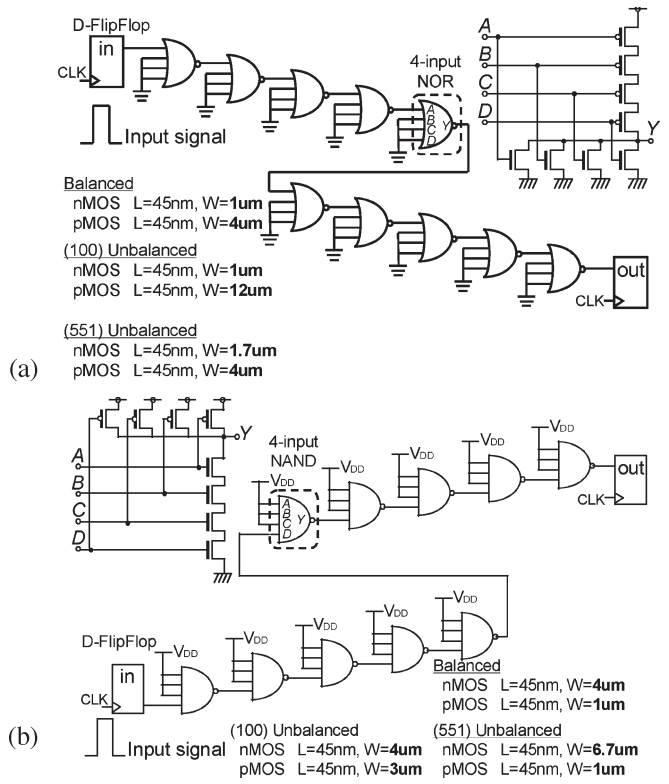

Fig. 11. SPICE simulation condition of the four-input ten-stage CMOS (a) NOR and (b) NAND gate circuits for 50-GHz clock operation.

charge does not exist when the accumulation-mode CMOS is on, E_{eff} for the accumulation-mode CMOS is lower than that for the inversion-mode CMOS for a gate overdrive voltage [16], [17]. Thus, the mobility of electrons and holes for the LSI operation is effectively higher for the accumulation-mode CMOS than for the inversion-mode CMOS [16], [17]. Then, to investigate the impact of the new technologies to the LSI speed performance, the output response of two critical path models of four-input ten-stage CMOS NOR and NAND gate circuits that are constructed by the silicon CMOS with new technologies are examined. The schematic diagram of these circuits is shown in Fig. 11(a) and (b). The critical path of a four-input NOR gate consists of four series-connected pMOSFETs from input A to output Y. Similarly, the critical path of a four-input NAND

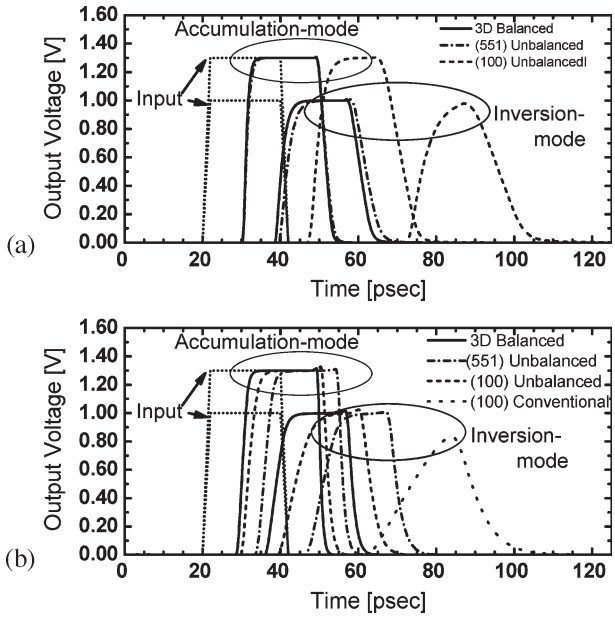

Fig. 12. SPICE simulation result of the output response of the four-input ten-stage CMOS (a) NOR and (b) NAND gate circuits for 50-GHz clock operation. CMOS is constructed by conventional (100) surface unbalanced CMOS, (100) surface unbalanced inversion-mode and accumulation-mode CMOS, (551) surface unbalanced inversion-mode and accumulation-mode CMOS, and balanced inversion-mode and accumulation-mode CMOS. The applied supply voltages for the inversion-mode CMOS and the accumulation-mode CMOS are 1.0 and 1.3 V, respectively. Only for the balanced accumulation-mode CMOS, the output response is sufficiently fast for over 50-GHz clock operation speed. For the NOR circuit that was constructed by conventional unbalanced CMOS, the input signal of 50-GHz clock propagates only until the fifth stage, and the final output does not change from 0.0 V at all.

gate is composed of four series-connected nMOSFETs. The conditions of the simulation are shown in Fig. 11(a) for the NOR gate circuits and Fig. 11(b) for the NAND gate circuits. Here, four-input ten-stage NOR and NAND circuits are equivalent to 20 fan-out-of-four inverter gates. Transistor gate widths are determined to equivalently balance the current drivability of nMOSFETs and pMOSFETs in each case. On the silicon (100) surface, since the current drivability of the nMOSFET is higher than that of the pMOSFET, the NOR gate area is larger than the NAND gate area for the same output current drivability. Similarly, the NAND gate area is larger than the NOR gate area for the case of silicon (551) surface because the current drivability of pMOSFET is higher than that of nMOSFET on the silicon (551) surface. Such gate area differences correspond to the difference in input and load capacitances of each circuit condition and highly affect the simulation results. Fig. 12(a) and (b) shows the results of the output response of the four-input ten-stage CMOS NOR and NAND gate circuits. The difference of the voltage swing between the accumulation-mode CMOS and the inversion-mode CMOS induces great operation speed difference, as shown in Fig. 12, where the output response is plotted for four-input ten-stage CMOS NOR and NAND gate circuits for a 50-GHz clock operation speed. Fig. 12 indicates that only the balanced accumulation-mode CMOS exhibits sufficient output response for 50-GHz clock operation speed where the balanced accumulation-mode CMOS is operated at 1.3 V, which is 0.3 V higher than that of the

TABLE I
CMOS STRUCTURES AND MAXIMUM LSI OPERATION CLOCK RATES

	Device Structure	Maximum Clock rate
Planer	Conventional (100) CMOS (Inversion-Mode)	5 GHz
	(100) Unbalanced CMOS (Inversion-Mode)	1 0GHz
	(100) Unbalanced CMOS (Accumulation-Mode: SOI)	20 GHz
	(551) Unbalanced CMOS (Inversion-Mode)	20 GHz
	(551) Unbalanced CMOS (Accumulation-Mode: SOI)	40 GHz
3-Dimentional	Balanced CMOS (Inversion-Mode)	30 GHz
	Unbalanced CMOS (Accumulation-Mode: SOI)	60 GHz

balanced inversion-mode CMOS. As a critical path, ten stages of four-input logic gates are enough to implement various functions to the silicon LSI chip. Table I summarizes the relationship between various CMOS structures and the maximum operation clock rates of LSIs that are constructed by various CMOS structures that are determined by the critical path simulations. Since the delay of a critical path determines the operation speed of an LSI, consequently, simulation results indicate that the balanced accumulation-mode CMOS will establish very high speed performance silicon LSI over 50-GHz clock rate even at a 45-nm technology node.

IV. CONCLUSION

An introduction of 3-D-structured MOS transistors is available using radical-reaction-based semiconductor manufacturing, leading to an introduction of the balanced CMOS on silicon (551) surface. The operation speed of silicon balanced CMOS LSI is enhanced to over 50-GHz clock rate at a technology node of 45 nm by introducing new technologies such as directly nitrided Si_3N_4 gate insulator films, atomic-order flat interfaces of gate insulator films to the silicon channel region, drastically decreased series resistances of source and drain electrodes, and accumulation-mode MOS transistors instead of the current inversion-mode MOS transistors. Thus, silicon MOS transistor performance such as the current drivability and the transconductance are scheduled to be enhanced up to a very high speed without accompanying an increase of leakage currents through the gate insulator films having an EOT in the range of 0.5 to 1.0 nm, so that the speed performance of silicon LSIs is going to exhibit over 50-GHz clock rate by concurrently introducing advanced interconnect technologies such as Cu–Mg (2%) interconnects having very excellent migration resistance [18] and interlayer low-κ dielectric of nonporous fluorocarbon (CFx) films having low dielectric constant of less than 1.9 and very high melting temperature of higher than 500 °C [1].

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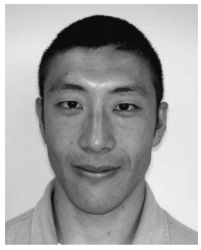

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